Charge storage and transport in single-walled carbon nanotube field-effect transistors

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**NANYANG
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**CHARGE STORAGE AND TRANSPORT
IN SINGLE-WALLED CARBON NANOTUBE
FIELD-EFFECT TRANSISTORS**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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Charge Storage and Transport in Single-Walled Carbon Nanotube Field-Effect Transistors

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School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Li Hong

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Summary

This thesis presents the main findings achieved during my PhD project on electron transport properties of carbon nanotubes (CNTs) and CNT based electronic devices. It consists of two parts: (1) hysteresis effects in CNT field-effect transistors (CNTFETs) and (2) single-electron/hole transport properties in CNTFETs.

Hysteresis in our CNTFETs is caused by charge trapping around the single-walled CNT (SWNT)-channel. First of all, the thermally activated charge trapping/detrapping processes are studied through the temperature dependence of hysteresis window. The hysteresis window size is reduced by $> 50\%$ when temperature is decreased from 295 to 16 K because thermally activated charge hopping into and out of the trapping centers is suppressed at low temperatures. Secondly, the sources of trapping centers are found to be the foreign species absorbed around the SWNT-channel, such as surfactants, impurities, traps in bottom gate oxide, water molecules and even ammonia molecules, etc. Thirdly, a technique for eliminating hysteresis has been developed. Annealing process (300 °C) in vacuum followed by Si_3N_4 and SiO_2 passivation is found to be an efficient way. Hysteresis-free devices are obtained after passivation at 300 °C because the surface water and surfactant molecules desorb at this temperature in vacuum. However, new traps may locate at the dielectric/SWNT interface and the bulk of the low-density dielectrics (deposited by a PECVD). Lastly, the influences of trapped charges in Si_3N_4 have been investigated. Through applying voltage pulses to a global back-gate and a local top-gate,

“globally” and “locally” distributed pre-trapped charges near the CNT-channel can be induced, respectively. The locally pre-trapped holes and electrons keep the CNT channel at “ON” and “OFF” states for the top-gate sweeping, respectively. Therefore, the trapped charges in the source/drain contact regions and SWNT-body could effectively influence the channel conductance through the “Schottky barrier modulation” and “bulk switching”, respectively.

Single-electron/hole transports with the Coulomb blockade effects are studied using three types of CNT-based electronic devices. In the first type, significant Coulomb oscillations are found in specially constructed CNTFETs that consist of long SWNTs bridging the source/drain electrodes and short SWNTs attached to the source/drain contacts. The oscillation peaks fade away gradually with increasing temperatures up to 70 K. The I_{DS} contour plot in the V_{DS} - V_{GS} plane shows “diamond”-shaped current forbidden regions at 15 K. In the second type of the devices, short-SWNT channel (< 100 nm) FETs with asymmetric drain and source contacts are fabricated with a self-alignment technique. The Coulomb oscillation peaks superimposed on the transfer curves of an n-type CNTFET (on/off ratio $\sim 10^7$) are observed up to 100 K. The activation energy at the Al/SWNT contact is found to be smaller than those at the Au/SWNT contact, by a factor of > 2 for all V_{GS} . The third type of the devices has single, double or multiple SWNT gates that control SWNT-channel conductance. Significant Coulomb blockade characteristic are observed in the double-SWNT-gated CNTFETs. A pair of potential barriers is induced by the double-SWNT-gates so that a single-electron/hole transistor working in the classic regime with the Coulomb blockade effects is formed.

Chapter 1

Introduction

1.1 Motivation

Microelectronics has experienced an inconceivable development in the past 40 years. In the past, transistor's performance and density were doubled every 3 years (known as Moore's Law).¹ However, when the devices are miniaturized to a scale of sub-50 nm, many physical problems will constrain further developments in the way predicted by Moore's Law. For instance, when tunneling through the ever-thinner gate oxide layers becomes significant and the layers begin to leak current. Critical requirements in lithography increase the fabrication costs. It is clear to everyone that the productivity development of silicon technology must slow down at some point. To find out alternatives for further development, many efforts have been made to develop advanced technology and new materials. For instance, high- κ dielectric materials² are used to solve the gate leakage problems, strained-silicon³ FET are employed to improve the carrier

mobility, carbon nanotubes,⁴ organic films,⁵ and DNA⁶ based molecular devices with a bottom-up fabrication process are investigated for overcoming lithography limit.

Single-walled carbon nanotube (SWNT), which represents an ideal material for molecular/nano electronic devices, is one of the most promising candidates for nanoelectronic applications. The inherent advantages of SWNTs over other candidates are as following:⁴

- Carrier transport is one-dimensional (1-D). This characteristic reduces phase space for scattering of the carriers and opens up a possibility of ballistic transport.
- All chemical bonds of the C atoms are satisfied and there is no need for chemical passivation of dangling bonds as in silicon. This implies that SWNT electronics would not be bound to use SiO₂ as gate oxide.
- The strong covalent bonding makes SWNTs high mechanical stability (Young's modulus about ten times higher than that of steel) and thermal stability, and immunity to electromigration. Current handling capability can be as high as 10⁹ A/cm².
- Both transistors and interconnects can be made out of semiconducting (s-) and metallic (m-) SWNTs, respectively.

However, the applications of SWNTs are very limited at present stage. Two major bottlenecks need breakthrough: (1) large-scale integration of SWNTs into circuits, and (2) predictable and controllable electronic performances of SWNT-based devices. Therefore, study of carrier transport in SWNTs is crucial for fabricating reliable and reproducible SWNT-based devices. Among various instability factors, uncontrollable hysteresis is the most harmful one. Thus, in my PhD project, I have investigated hysteresis phenomena in

our CNTFETs systematically, and summarized the main findings in the first half of this dissertation. In addition, SWNT is a type of 1-D materials and semiconducting SWNT does provide an ideal platform for the study of single-electron/hole transport properties. Unique and interesting phenomena associated with single-electron/hole transport have been found in the project, and the relevant observations and discussions will be the focus of the second half of this dissertation.

1.2 Objectives

The main objectives of my PhD project are as follows:

- ◆ To study the mechanisms of the hysteresis phenomenon in CNTFETs. First of all, CNTFETs with apparent hysteresis effects are fabricated. Then, a systematic investigation is carried out on the hysteresis phenomenon for the purpose of obtaining a clear physical picture for the phenomenon.
- ◆ To control the hysteresis in a well-defined manner. Techniques to increase, decrease, and eliminate hysteresis in CNTFETs are developed.
- ◆ To study the carrier transport in SWNTs under the influence of charge trapping. The influence of charge trapping on switching mechanism of Schottky-barrier-CNTFETs is studied in details.
- ◆ To investigate single- or few-electron transports in SWNTs. Single-electron transport in SWNT-based devices are investigated systematically.

1.3 Major contributions of this dissertation

The main contributions of this PhD project are listed as following:

1. Hysteresis effects in Schottky-barrier (SB) CNTFETs have been studied, systematically. In general, hysteresis is widely accepted to be caused by charge trapping. First of all, CNTFETs with large hysteresis window ($\Delta V_{th} \sim 20$ V) were fabricated. Then, the hysteresis window was studied at different pressures and temperatures. Hysteresis windows shift was found to be caused by metal-electrode and SWNT work function change due to air (oxygen) exposure. Hysteresis window size was reduced by more than 50% when temperature was decreased from 295 to 16 K because the trapping and detrapping rates were reduced at low temperatures. Two interesting points are observed. First of all, hysteresis reduction of ~ 12 V occurred in the range of 200 to 250 K, i.e., hysteresis was extremely sensitive to temperature in this range. This characteristic may enable the devices to be used as temperature sensors. We attributed the finding to the decrease of thermionic emission current component, which is exponentially proportional to the temperature variation ($\ln I \propto 1/T$). Below 200 K, tunneling, instead of thermionic emission, through the Schottky barriers dominated the channel current. Since tunneling current is less sensitive to the Schottky barrier height variation, which can be affected by charge trapping, than thermionic emission current, hysteresis slightly varied below 200 K. Secondly, the reduction ($\sim 67\%$) of hysteresis window was mainly caused by shift of reverse sweeping curve. It is noted that reverse (Forward) sweeping is dominated by electron (hole) trapping. Thus, the findings imply: (1) electron trapping is more sensitive

to temperature variation, and/or (2) the density of trapped electrons are higher than that of trapped holes.

2. The source of trapping centers was revealed in CNTFETs and techniques to induce, reduce and eliminate hysteresis were developed. Water molecules adsorbed in CNTFETs were suggested by some researchers to be the major cause of trapping centers, and the hysteresis could be eliminated just by remove adsorbed water. On the contrary, hysteresis in our devices could only be reduced by 40% after annealing in dry air. The remaining hysteresis (60%) suggests that other trapping centers, in addition to water molecules, could play a significant role in the CNTFETs. The unknown trapping centers were suggested to be foreign species adsorbed on the device surface, such as surfactants (Triton X 100, $C_{14}H_{22}(C_2H_4O)_{10}$), impurities introduced during SWNT-bridging and burning off processes, and traps in the bottom gate oxide (thermally grown SiO_2). Furthermore, ammonia (NH_3) was also found to play a role of trapping center. Those trapping centers were found to be closely related to adsorbed water molecules. It was found that water helped the adsorption of NH_3 , and hence increased the amount of trapping centers. Meanwhile, the hysteresis was influenced by the back-gate voltage sweeping rate, indicating that the trapping centers associate with slow charge trapping processes. In addition, an annealing process (300 °C) in vacuum followed by Si_3N_4 or SiO_2 passivation was found to eliminate the hysteresis under some conditions, i.e., moderate sweeping range and thick passivation layer. Owing to the interface traps at the dielectric/SWNT interface, and bulk traps in the low-density dielectrics (deposited by a plasma-enhanced chemical vapor deposition system), large sweeping range still caused

significant hysteresis. The results showed that hysteresis was controllable through the trapping centers. Absorbents including water molecules and impurities, and interface/bulk traps in the bottom gate oxide are the main sources of trapping centers in the CNTFETs without passivation. The adsorbed water molecules and impurities induced trapping centers probably associate with a slow charge trapping process and continuous energy level distribution. In contrast, the trapping centers in passivated CNTFETs are mainly caused by interface and bulk traps in the passivation layer (Si_3N_4 and SiO_2), and the energy levels associated with these trapping centers are discrete, and then greater back-gate voltages (larger sweeping range) are necessary to activate the charging/discharge process.

3. Global and local charge trapping on the carrier transport in SWNTs were investigated. Partially top-gated CNTFETs were fabricated to study charge trapping distribution effects in the devices. Through applying voltage pulses to a global back-gate and a local top-gate, “globally” and “locally” distributed pre-trapped charges near the CNT-channel can be induced, respectively. For the back-gate voltage sweeping, the transfer curves were shifted due to the trapped charges, which result in significant decreases in the field-effect mobility for both hole and electron transport. Local potential fluctuations caused by the trapped charges could be responsible for the observations. The locally pre-trapped holes and electrons kept the device at “ON” and “OFF” states for the top-gate sweeping, respectively. Overall, the globally trapped charges affect the channel conductance, threshold voltage, field-effect mobility and hysteresis window, mainly through modulating the Schottky contact barriers. On the contrary, locally trapped

charges influence the device characteristics mostly likely by changing local energy barriers near the top gate without affecting the contact barriers.

4. Single-electron transports with Coulomb blockade effects were studied in SWNTs. The Coulomb blockade effects are found in three types of devices. In the first type of devices, we have observed significant Coulomb oscillations in specially constructed CNTFETs that consist of long SWNTs bridging the source/drain electrodes, and short SWNTs attached to the source/drain contacts. The oscillation peaks disappeared gradually with increasing temperatures up to 70 K. Current contour plot in V_{DS} - V_{GS} plane showed diamond-shaped current forbidden regions at 15 K. The Coulomb oscillations could be interpreted as follows: (1) charges trapped in the short SWNTs could be quantized; and (2) the electrostatic potential at the long-tube/electrodes contacts could be influenced by the charges stored in the short SWNTs. As a result, the channel current could be modulated by the charged short SWNTs. In the second types of devices, short-channel (< 100 nm) CNTFETs with asymmetric drain and source contacts were fabricated with a self-alignment technique. Coulomb oscillation peaks superimposed on the transfer curves of an n-type CNTFET (on/off ratio $\sim 10^7$) were observed up to 100 K. However, the oscillation current amplitudes are unequal under positive and negative V_{DS} . Single-electron tunneling current component remains unchanged when V_{DS} is reversed. The asymmetric current amplitude is mainly caused by unequal thermionic emission current over different barriers height at the source/drain contacts. Above 100 K, thermionic emission with activation energy dominates the current. The activation energy at the Au/SWNT contact are larger than those at the Al/SWNT contact, by a factor of > 2

for all V_{GS} , owing to the work function differences between 3-D metal and 1-D SWNT. In atmosphere environment, the devices showed significant diode-like effects with a maximum current rectification ratio $\sim 10^4$, implying that this type of devices have great potential to be used as diodes. In the third type of devices, SWNTs were used as gate electrodes to confine a quantum dot in SWNT-channel. The SWNT-gates are 4 and 7 nm in height, respectively, and the distance between them is ~ 300 nm. A pair of potential barriers is induced by the double-SWNT-gates, and hence a single-electron/hole transistor working in the classic regime with Coulomb blockade effects is formed. The Coulomb oscillations showed strong bias and temperature dependence. Coulomb diamonds were observed for both single-hole and -electron tunneling. Voltages applied to the SWNT-gates determine the tunneling barrier height, and thus modify the characteristics of Coulomb oscillations and diamonds. The unequal capacitances calculated from the Coulomb diamonds indicate that the tunneling barrier pair is asymmetric.

1.4 Organization of this dissertation

Chapter 1 introduces the motivations, objectives, major contributions and organization of the dissertation.

Chapter 2 gives a review of carbon nanotube electronic properties, including classification of carbon nanotubes, electronic structure of SWNT, density of electronic state, and energy gap. Various carbon-nanotube-based devices are summarized.

Chapter 3 presents a systematic investigation on hysteresis effects in CNTFETs. The mechanism of hysteresis in the CNTFETs is discussed. Various trapping centers are studied to control the hysteresis. An annealing process followed by the dielectric passivation is used to eliminate hysteresis.

Chapter 4 describes the effects of charge trapping in partially top-gated CNTFETs. Globally trapped charges along the entire channel and locally trapped charges in the middle of the channel have different effects on device characteristics.

Chapter 5 shows a novel structure to study single-electron transport in SWNTs. Single-electron transport with Coulomb blockade effects are studied in details. Coulomb oscillations and Coulomb diamonds are observed and analyzed.

Chapter 6 presents the single-electron transport in short-channel (<100 nm) CNTFETs with asymmetric drain and source contacts. A quantitative description of the carrier transport process in the device is proposed. At room temperature, the devices could work as perfect Schottky diodes with great current rectification ratio (maximum value $> 10^4$).

Chapter 7 describes a novel technique for fabricating CNT-gated CNTFETs. Single-electron/hole transport in a double-SWNT-gated CNTFET is discussed.

Chapter 8 concludes the entire project and gives recommendations for future work.

Chapter 2

Carbon Nanotubes and Relevant Devices

2.1 Classification of carbon nanotubes

Carbon has various forms such as diamonds, graphite, fullerenes, carbon fibers and carbon nanotubes. Carbon nanotubes (CNTs) were first found by Oberlin *et al.* in 1976.⁷ However, CNTs had not attracted much attention until Iijima's finding in 1991.⁸ A CNT could be regarded as a hollow cylinder by rolling up of one or more layers of graphene. A single CNT may consist of up to several tens of graphene shells with adjacent shell separation of ~ 0.34 nm, which is called multi-walled carbon nanotubes (MWNTs). Two years later, Iijima & Ichihashi,⁹ and Bethune *et al.*¹⁰ synthesized SWNT, which contains only one graphene layer. Recently, double-walled carbon nanotubes (DWNTs) also attracted a lot of attentions.¹¹ However, SWNTs are the most promising candidate for nanoelectronic applications because of their simple structure, hence more predictable electronic properties.

2.2 Structure of single-walled carbon nanotubes

A SWNT could be 1 nm in diameter and from a few micron meters to several centimeters in length; hence it has huge aspect ratio (i.e., length/diameter). Thus, a single SWNT is one-dimensional with a certain axial symmetry, called chirality.

2.2.1 Chiral Vector: $\vec{C}_h$

Fig 2.1 (a) shows an unrolled honeycomb lattice of the nanotube. $\vec{OB}$ is the direction of the nanotube axis, $\vec{OA}$ indicates the circumference of the nanotube. By rolling the honeycomb sheet so that points O and A coincide each other (and points B and B' overlap), a SWNT is constructed. The vector $\vec{OA}$ and $\vec{OB}$ define the chiral vector $\vec{C}_h$ and translation vector $\vec{T}$ of the carbon nanotube, respectively. $\vec{C}_h$ can be expressed by two real space unit vectors $\vec{a}_1$ and $\vec{a}_2$ (see Fig 2.1 (a)) of the hexagonal lattice:

$$\vec{C}_h = n \vec{a}_1 + m \vec{a}_2 \equiv (n, m) \quad (n, m \text{ are integers, } 0 \leq |m| \leq n) \quad (2.1)$$

If $n = m$, i.e., $\vec{C}_h = (n, n)$, it corresponds to an armchair nanotube, as shown in Fig 2.1 (b).

In the case of $m = 0$, or $\vec{C}_h = (n, 0)$, a zigzag nanotube is formed (Fig 2.1 (c)). All other (n, m) chiral vectors correspond to chiral nanotubes (Fig 2.1 (d)).

The diameter of the carbon nanotube, d , is given by L / π , where L is the magnitude of $\vec{C}_h$ or the circumferential length of the carbon nanotube:

$$d = L / \pi, \quad L = |\vec{C}_h| = a \sqrt{n^2 + m^2 + nm}, \quad (2.2)$$

where the lattice constant of the honeycomb lattice $a = 0.249$ nm.

Fig 2.1 (a) An unrolled graphene layer with honeycomb lattice. When we connect sites O with A , and B with B' , a nanotube can be constructed. $\overrightarrow{OA}$ and $\overrightarrow{OB}$ define the chiral vector $\overrightarrow{C_h}$ and translation vector $\overrightarrow{T}$ of a carbon nanotube, respectively. Special tube types include armchair tubes (n, n) (b) and zigzag tubes $(n, 0)$ (c). All other tubes are called chiral tubes (d).

The chiral angle θ is defined as the angle between the vectors $\overrightarrow{C_h}$ and $\overrightarrow{a_1}$, with a value range of $0 \leq |\theta| \leq 30^\circ$, because of the hexagonal symmetry of the honeycomb lattice.¹² θ denotes the tilt angle of the hexagons with respect to the direction of the nanotube axis, and specifies the spiral symmetry,

$$\cos \theta = \frac{\overrightarrow{C_h} \cdot \overrightarrow{a_1}}{|\overrightarrow{C_h}| \cdot |\overrightarrow{a_1}|} = \frac{2n + m}{2\sqrt{n^2 + m^2 + nm}}. \quad (2.3)$$

In particular, zigzag and armchair nanotubes correspond to $\theta = 0^\circ$ and $\theta = 30^\circ$, respectively.

2.2.2 Translational vector: $\vec{T}$

The translation vector $\vec{T}$ is defined to be the unit vector of a 1-D CNT. $\vec{T}$ is parallel to the nanotube axis and is normal to the chiral vector $\vec{C}_h$, as shown in Fig 2.1

(a), $\vec{T}$ can be expressed in terms of $\vec{a}_1$ and $\vec{a}_2$ as:

$$\vec{T} = t_1 \vec{a}_1 + t_2 \vec{a}_2 \equiv (t_1, t_2), \text{ (where } t_1, t_2 \text{ are integers)} \quad (2.4)$$

and

$$t_1 = \frac{2m+n}{d_R}, \quad t_2 = -\frac{2n+m}{d_R}, \quad (2.5)$$

where d_R is the greatest common divisor of $(2m+n)$ and $(2n+m)$, and is given by

$$d_R = \begin{cases} q & \text{if } n-m \text{ is not a multiple of } 3q \\ 3q & \text{if } n-m \text{ is a multiple of } 3q, \end{cases} \quad (2.6)$$

where q is the greatest common divisor of (n, m) .

The magnitude of the translation vector, $\vec{T}$, is given by

$$T = \frac{\sqrt{3}L}{d_R} \quad (2.7)$$

2.2.3 Unit cells and Brillouin zones

The unit cell of a CNT in real space is given by the rectangle generated by $\vec{C}_h$ and $\vec{T}$, i.e., the dashed rectangle $OAB'B$ shown in Fig 2.1 (a). The number of hexagons, N , in the unit cell is determined by the integers (n, m) and is given by¹³

$$N = 2(m^2 + n^2 + nm)/d_R. \quad (2.8)$$

The addition of each hexagon to the honeycomb structure in Fig 2.1 (a) corresponds to the addition of two carbon atoms. Since there are $2N$ carbon atoms in the unit cell, there must be N pairs of bonding π and anti-bonding π^* electronic energy bands. The reciprocal lattice vectors $\vec{K}_1$ in the circumferential direction and $\vec{K}_2$ along the nanotube axis are obtained from the relation $\vec{R}_i \cdot \vec{K}_j = 2\pi\delta_{ij}$, where $\vec{R}_i$ and $\vec{K}_j$ are, respectively, the lattice vectors in real and reciprocal space. They can be expressed as

$$\vec{K}_1 = (-t_2 \vec{b}_1 + t_1 \vec{b}_2)/N, \quad \vec{K}_2 = (m \vec{b}_1 - n \vec{b}_2)/N \quad (2.9)$$

where $\vec{b}_1$ and $\vec{b}_2$ are the reciprocal lattice vectors of the two-dimensional graphite. The reciprocal vectors, $\vec{K}_1$ and $\vec{K}_2$ for a $\vec{C}_h = (4, 2)$ chiral nanotube are shown in Fig 2.2.

The first Brillouin zone of this one-dimensional material is the line segment WW' . Since $N\vec{K}_1 = (-t_2 \vec{b}_1 + t_1 \vec{b}_2)$ corresponds to a reciprocal lattice vector of the two-dimensional graphite, two wave vectors that differ by $N\vec{K}_1$ are equivalent. Because t_1 and t_2 do not have a common factor except for unity, none of the $N-1$ vectors $\mu \vec{K}_1$ (where $\mu = 1, \dots, N-1$) are reciprocal lattice vectors of two-dimensional graphite. Thus the N wave vectors $\mu \vec{K}_1$ ($\mu = 0, \dots, N-1$) give rise to N discrete k vectors, as indicated by the $N = 28$ parallel line segments in Fig 2.2, which arise from the quantized wave vectors associated with the periodic boundary conditions on $\vec{C}_h$. The length of all the parallel lines in Fig 2.2 is $2\pi/T$, which is the length of the one-dimensional first Brillouin zone. Because of the

translational symmetry of $\vec{T}$, we have continuous wave vectors in the direction of $\vec{K}_2$ for a CNT of infinite length.

Fig 2.2 The Brillouin zone of a CNT is represented by the line segment WW' , which is parallel to $\vec{K}_2$. The vectors $\vec{K}_1$ and $\vec{K}_2$ are reciprocal lattice vectors corresponding to $\vec{C}_h$ and $\vec{T}$, respectively. The figure corresponds to $\vec{C}_h = (4, 2)$, $\vec{T} = (4, -5)$, $N = 28$, $\vec{K}_1 = (5\vec{b}_1 + 4\vec{b}_2)/28$, $\vec{K}_2 = (4\vec{b}_1 - 2\vec{b}_2)/28$.¹⁰

2.3 Electronic structure of SWNTs

The interesting electrical properties of CNTs are in a large part due to the peculiar electronic structure of graphene. In Fig 2.3 (c), the energy dispersion relations of 2-D graphene are shown throughout the Brillouin zone and the inset shows the energy dispersion relation along the high symmetry axes of the dotted triangle ΓMK shown in Fig 2.3 (b). The upper half of the energy dispersion curves describes the π^* -energy anti-bonding band, and the lower half is the π -energy bonding band. The upper π^* band and the lower π band are degenerated at the K points through which the Fermi level passes. Since the density of states at the Fermi level is zero, 2-D graphene is a zero-gap semiconductor.

Fig 2.3(a) The unit cell and (b) Brillouin zone of two-dimensional graphene are shown as the dotted rhombus and the shaded hexagon, respectively. $\vec{a}_i$ and $\vec{b}_i$ ($i = 1, 2$) are unit vectors and reciprocal lattice vectors, respectively. (c) The energy dispersion relations for 2-D graphite are shown throughout the whole region of the Brillouin zone. The inset shows the energy dispersion along the high symmetry directions of the triangle ΓMK shown in (b).^{10,13}

For the nanotube structure, there is an additional quantization arising from the confinement of electrons in the circumferential direction in the tube. When the energy dispersion relations of 2-D graphene, $E_{g2D}(k)$ at line segments shifted from WW' by $\mu \vec{K}_1$ ($\mu = 0, \dots, N-1$) are folded so that the wave vectors parallel to $\vec{K}_2$ coincide with WW' as shown in Fig 2.2, N pairs of 1-D energy dispersion relations $E_\mu(k)$, are obtained. These 1-D energy dispersion relations are given by¹⁰

$$E_{\mu}(k) = E_{\text{g2D}}(k \frac{\vec{K}_2}{|\vec{K}_2|} + \mu \vec{K}_1), \quad (\mu = 0, \dots, N-1, \text{ and } -\frac{\pi}{T} < k < \frac{\pi}{T}) \quad (2.10)$$

The N pairs of energy dispersion curves correspond to the cross sections of the two-dimensional energy dispersion surface shown in Fig 2.3 (c), where cuts are made on the lines of $k \frac{\vec{K}_2}{|\vec{K}_2|} + \mu \vec{K}_1$. If for a particular (n, m) nanotube, the cutting line passes through a K point of the 2-D Brillouin zone, where the π and π^* energy bands of two-dimensional graphene are degenerated by symmetry, the one-dimensional energy bands have a zero energy gap. In other words, the density of states at the Fermi level has a finite value for these carbon nanotubes. Such tubes therefore are metallic. If, however, the cutting line does not pass through a K point, the carbon nanotubes are expected to show semiconducting behavior, with finite energy gaps between the valence and conduction bands.

A metallic energy band is determined by the fact that the ratio of the length of the vector $\vec{YK}$ to that of $\vec{K}_1$ is an integer. Since the vector $\vec{YK}$ can be expressed as

$$\vec{YK} = \frac{2n+m}{3} \vec{K}_1, \quad (2.11)$$

The condition for metallic nanotubes is that $(2n+m)$ or equivalent $(n-m)$ is a multiple of 3. In particular, the armchair nanotubes denoted by (n, n) are always metallic, and the zigzag nanotubes $(n, 0)$ are only metallic when n is a multiple of 3.

For all metallic nanotubes, independent of their diameter and chirality, the density of states per unit length along the nanotube axis is a constant given by

$$N(E_F) = \frac{8}{\sqrt{3}\pi a \gamma_0} \quad (2.17)$$

where a is the lattice constant of the graphene layer and γ_0 is the nearest-neighbor C-C tight binding overlap energy.

Fig 2.4 Electronic densities of states for (5, 5), (7, 1) and (8, 0) nanotubes showing van Hove singularities characteristic of one-dimensional systems. The (5, 5) armchair nanotube is metallic for symmetry reasons. The (7, 1) chiral tube displays a tiny gap owing to curvature effects, but will display a metallic behavior at room temperature. The (8, 0) zigzag tube is a large gap semiconductor.¹³

Fig 2.4 compares the density of states for metallic (5, 5) and (7, 1) and semiconducting (8, 0) zigzag nanotubes. What is important is the density of states near the Fermi level E_F located at $E = 0$. This density of states for (8,0) tube has a value of zero. Thus, it is a semiconducting nanotubes. In contrast, (5,5) and (7,1) tubes are for metallic nanotubes.

The energy gap for semiconducting nanotubes depends upon the reciprocal nanotube diameter R ,¹⁰

$$E_g = \frac{\gamma_0 a_{C-C}}{R}, \quad (2.18)$$

where $a_{C-C} = \frac{a}{\sqrt{3}}$ is the nearest-neighbor C-C distance on a graphene sheet. But it is independent of chiral angle of the semiconducting nanotube.

2.4 Observation of carbon nanotubes

A single CNT could be observed under various microscopes, such as transmission electron microscopy (TEM), scanning electron microscopy (SEM), scanning tunneling microscopy (STM) and atomic force microscopy (AFM).

Fig 2.5 TEM images of a) a SWNT^{14a} b) a DWNT, c) a MWNT⁷ and d) a SWNT bundle (cross sectional view).^{14b} One hole indicates a single SWNT.

The TEM images of a SWNT^{14a}, DWNT and MWNT⁷ are shown in Fig 2.5 (a), (b) and (c), respectively. The graphene layers are clearly observed by TEM. The cross section of a SWNT bundle^{14b} is observed, as shown in Fig 2.5 (d). One hole represents a single SWNT. STM images shown in Fig 2.6 present the atomic structure of CNTs.¹⁵ The black arrows show the directions of the transition vectors. Moreover, the hexagonal structure of a 6-carbon ring could be observed clearly. The STM images, from which the chiral vector and lattice constant could be obtained, are direct evidences of the atomic structure of CNTs. CNTs must lay on a conducting surface to obtain good STM images. However, CNTs are situated on insulating layers in most of the CNT-based devices. Thus, STM is not frequently used to obtain images of devices. AFM and SEM are heavily used for imaging CNTs in devices though they provide relatively worse resolution. We will discuss the AFM and SEM images in the following chapters.

Fig 2.6 STM images for SWNTs with different chiralities.¹⁵ Arrows indicate the direction of translation vector, T .

2.5 Development of CNT-based devices with FET structure

Since FET geometry is the most commonly used structure for CNT-based devices, I focus on the review of CNTFETs. The first batch of CNTFETs were reported in 1998.^{16,17} A semiconducting nanotube connected to two metal-electrodes showed the characteristics of a field-effect transistor. By applying voltage to a gate electrode, the nanotube could be switched from a conducting to an insulating state. The transistor structure is shown in Fig 2.7. CNTs played the role of a “channel”, while the two metal-electrodes functioned as the “source” and “drain” electrodes. A heavily doped silicon wafer was used as the “gate” electrode, so-called back-gate. The channel current decreased with increasing gate voltage, indicating that the conductance through s-SWNTs was dominated by holes. The transfer curves saturated for negative gate voltages. These CNTFETs behaved as p-type FETs and had an ON/OFF current ratio of $\sim 10^5$. Over the past decade, the performance of CNTFETs has been improved by decreasing contact resistance, shortening source and drain distance, changing gate structure, decreasing gate oxide thickness and employing high- κ insulator, which will be discussed in detail later.

Fig 2.7 A schematic cross section of CNTFETs. A single CNT bridges the gap between two gold electrodes. The silicon substrate is used as the back-gate.¹⁶

2.5.1 Improvement of the contacts between CNTs/metals

Although functional, the aforementioned transistors had a high parasitic contact resistance ($\geq 1 \text{ M}\Omega$), low transconductance $g_m \sim 1 \text{ nS}$, and high inverse subthreshold slope $S \sim 1\text{-}2 \text{ V/dec}$. These unsatisfactory characteristics were to a large extent due to poor contacts.⁴ Two common methods are used to improve the contacts. One is annealing that is adapted by IBM group. In their transistors, s-SWNTs were placed on top of the SiO_2 film, Co (or Ti) source and drain electrodes were deposited on the s-SWNTs. Thermal annealing at 400°C (for Co), or 820°C (for Ti) in an inert ambient lead to a stronger coupling between the metal and the CNTs, and hence a small contact resistance.¹⁸ The other method is to use appropriate metal-electrodes. Javey *et al.*¹⁹ selected palladium, a noble metal with high work function and good “wetting” interactions with CNTs, as the electrode materials and obtained a large “ON” state conductance that was very close to the ballistic transport limit of $\frac{4e^2}{h}$.^{20,21,22} The contact improvement was suggested to be caused by a reduced or eliminated barriers for holes.

2.5.2 Gate structures

The most widely used gate structure for CNTFETs in the past was the doped silicon substrate as back gates and thermally grown SiO_2 as gate dielectric.^{16,17, 23} However, local gates that could address different nanotube transistors on a common chip are required for the integration of multiple transistors. Several new gate structures of CNTFETs have been developed, including bottom aluminum gates with subnanometer-

thick native Al_2O_3 dielectrics,²⁴ bottom tungsten gates with SiO_2 ,²⁵ top-gate with 2~20-nm-thick SiO_2 dielectrics.^{26,27} In addition to the local address ability, these gate structures show progressively improved CNTFET characteristics. For instance, the inverse subthreshold slope S is approaching the theoretical value^{26,28} due to decreased oxide thickness²⁶ and high- κ dielectrics.²⁸ CNTFETs fabricated with electrolyte gate²⁹ and polymer gate^{30,31} demonstrated strong gate-channel coupling with improved device characteristics. An electrolyte gate with a dielectric constant of about 80 could lead to an extremely high transconductance of $\sim 20 \mu\text{S}$.²⁹

2.5.3 Dielectric materials and their thickness

The performances of CNTFETs can also be improved by decreasing the gate oxide thickness. Wind *et al.*²⁶ compared the characteristics of a top-gated (15 to 20-nm-thick SiO_2) and a back-gated (120-nm-thick SiO_2) CNTFET fabricated on the same SWNT and found that those top-gate devices exhibited excellent electrical characteristics. The threshold voltage of the top-gated CNTFET was only -0.5 V, significantly lower than that under the bottom-gated operation, -12 V. Similarly, the drive current and the transconductance are much higher for the top-gating. Using a simple model, Heinze *et al.*³² concluded the scaling rule of the subthreshold slope with oxide thickness and pointed out that the change in the oxide thickness is equivalent to simply rescaling the gate voltage by $V_{\text{scal}} \propto t_{\text{ox}}^{1/2}$, thus S scales as $t_{\text{ox}}^{1/2}$ and the transconductance scales as $\propto t_{\text{ox}}^{-1/2}$, well explaining the performance improvement of CNTFETs due to the decreasing of oxide thickness.

High- κ dielectrics have been actively pursued to replace SiO_2 as gate insulator for silicon devices.⁴ The relatively low κ of SiO_2 (3.9) limits its use in transistors as gate length scales down to tens of nanometers. High- κ gate insulators afford high capacitance without relying on ultra-small film thickness, thus allowing for efficient charge injection into the transistor channels and meanwhile reducing direct-tunneling leakage currents.²⁸ Experimental results show that ZrO_2 ,²⁸ HfO_2 ,^{33,34,35} Al_2O_3 ²⁴ and SrTiO_3 ³⁶ have been successfully used as the gate insulators in CNTFETs.

2.5.4 Different transfer characteristics of CNTFETs: p-type, n-type and ambipolar characteristics

Up to date, CNTFETs have shown p-type, n-type and ambipolar characteristics. Typically, CNTFETs fabricated in ambient air exhibit p-type characteristics.^{16,17,19,28,29,36,37,38} However, for future nanotube-based electronics, the ability to “dope” nanotubes selectively to achieve different conducting types is highly desired. Several methods have been developed to achieve n-type CNTFETs. It is found that CNTFETs can be converted from p- to n-type simply by annealing the devices in vacuum,^{39,40} or in inert gases¹⁸ or hydrogen.²⁸ Doping p-type CNTFET with potassium^{39,41,42,43} is another approach, and has been used to build CNT p-n diodes⁴⁴ and complementary logic gates.^{24,39} In this method, evaporated potassium vapor are adsorbed on the surface of SWNTs.⁴¹ By coating polyethylenimine (PEI) on the top of SWNTs,^{45,46} n-type doping can also be realized. Recent results suggest that p- and n-type behavior can be controlled easily using polymer electrolyte gate.^{30,31} Lu *et al.*³⁰ show that mixing

different concentrations of 2,3-dichloro-5,6-dicyanobenzoquinone (DDQ) into a lithium percolate/poly(ethylene oxide) (PEO) mixture could achieve both p- and n-type CNTFETs. Similarly, by varying the electron donating and accepting ability of the chemical groups of the host polymer, unipolar p- or n-type devices that are stable at room temperature in air have been fabricated by Siddons *et al.*³¹ Using these polymer gates, one can also obtain ambipolar CNTFETs^{30,31} that can operate as switches for electrons and holes depending on the sign of the gate voltage. The ambipolar characteristics are also found during annealing a p-type CNTFET covered with SiO₂ in vacuum or in an ambient atmosphere.¹⁸ The CNTFETs fabricated with large-diameter (3-5 nm) SWNTs (small band gap ~ 0.4 eV) typically exhibit ambipolar characteristics.^{47,48} For small-diameter (1.4 nm) SWNTs, ambipolar behavior is observed in air with very thin gate oxide (10 nm).⁴⁹ In addition, these ambipolar CNTFETs can be converted to p-type ones with an asymmetric gate structure with respect to the source and drain electrodes.⁴⁹

2.5.5 Switching mechanisms of CNTFETs

So far, three models have been proposed to interpret CNTFET operation. First of all, conventional metal oxide semiconductor field-effect transistor (MOSFET)-like behavior has been reported for large diameter carbon nanotubes (3-5 nm). The rather small energy gap of the CNT channels allows carriers injection from the metal contact into the valence band of the CNTs without a substantial Schottky barrier.^{19,50} It is mainly the potential barriers at the contacts that control the current for these devices. CNTFETs with extremely long channel length ($> 300 \mu\text{m}$)^{51,52} also exhibit MOSFET-like behavior.

In this case, the contact resistance is insignificant, so the resistance of the channel is dominated by bulk-CNT resistance. Secondly, the CNTFETs fabricated from larger band gap CNTs behave as the Schottky barrier (SB)-FETs.^{33,34,53} In this case, the gate field determines the thickness of the Schottky barriers at the metal-CNT interface and makes them more or less transparent for tunneling from the source or drain electrodes into the CNT channels. Several observations support this mechanism. First, the output characteristics are observed to be strongly dependent on which side of the nanotube is connected to the source and drain. This can not be explained by conventional MOSFET mechanism where the saturation currents under large positive and negative V_D would be comparable since both sets of curves are symmetrical with respect to $V_D = 0$. Another evidence for this model is that the inverse subthreshold slope S shows independent of channel length³⁴ but increase with oxide thickness. The related experimental data can be fitted well by the SB model but not by the conventional MOSFET model.³³ Furthermore, S is temperature dependent at high temperatures but levels off at temperatures below about 200 K, suggesting a carrier tunneling process.³³ The SB model can also provide a reasonable explanation to the effects of O_2 on the performance of CNTFETs.⁵³ So far, the theory development of conduction mechanism are completed for common FET geometry. However, new conduction mechanisms are needed for complicated device structures.

Thirdly, another operation model is the band-to-band (BTB) tunneling reported by Appenzeller *et al.*⁵⁴ BTB tunneling means tunneling from the conduction into the valence band of an s-SWNT and vice versa, as observed using a dual-gated CNTFET structure.

Different from a conventional device where the Fermi distribution ultimately limits the gate voltage range for switching the device on or off, current flow is controlled in this mode by the valence and conduction band edges in a bandpass-filter-like arrangement. A small S value of ~ 40 mV/dec has been obtained at room temperature, much smaller than the theoretical limit value of 60 mV/dec with conventional MOSFETs. Therefore, due to the unique electrical properties of CNT, such as low dimensionality, relatively small bandgap and quasiballistic transport, careful treatment on the conduction theories must be carried out when CNT-based devices become more and more complicated.

2.5.6 Various CNT-related devices based on FET geometry

Although CNTFETs is still in an early research stage, they have shown amazing performance parameters, for instance, high drive current, high transconductance,⁴ etc. Several applications, including logic circuits,^{24,25,28,39,40} memories,^{55,56,57,58} chemical sensors,^{59,60,61} p-n junction diodes⁶² and light emission devices^{63,64,65} have been demonstrated and shown promising performances. However, many challenges remain before these molecular electronic devices become useful nano devices. Most challenges are from the materials issues. So far, no technique could produce a single type of CNT and separation techniques or/and breakdown process^{66,67} have to be used in fabricating CNTFETs. Controllable placement of CNT onto desired locations is difficult. Spin-coating CNT suspension onto structured wafers^{16,17,24,26} is a simple process. However, the random distribution and orientation of CNTs and the CNT contamination on the entire sample surface are major drawbacks. Directly growing CNTs from one electrode to

another is a relatively controllable process.^{39,47} Unfortunately, this approach causes the catalyst contamination and poor selectivity of CNTs. Both of the commonly used methods at present can not meet the demands of large scale integration. Moreover, some stability issues are still under investigations, such as hysteresis,^{56,57,58} CNT/metal interface^{33,34,53} and so on.

Chapter 3

Hysteresis in CNTFETs

3.1 Literature review of hysteresis in CNTFETs

With the background knowledge of most aspects of CNTs, we come to the core of the first half of this project, i.e., hysteresis in CNTFETs. Fuhrer *et al.* reported the first CNTFET memory based on the hysteresis effects in 2002.⁵⁵ As shown in Fig 3.1 (b), a pronounced hysteresis loop (≈ 6 V) was observed when the gate voltage was swept from -10 to +10 V and then swept back. The arrows in the figure indicate the sweeping directions of the gate voltage. The hysteresis loop is formed by the shift of threshold voltage of the CNTFET.

Fig 3.1 a) AFM image of the CNTFET. The scale bar is 1 μm. b) I_{sd} - V_g curve of the CNTFET. c) Four read/ write cycles of the CNTFET memory at room temperature.⁵⁵

Fig 3.1 (c) demonstrates the memory operation based on the hysteresis loop. The state of the device is read at the source-drain voltage (V_{sd}) of 500 mV and gate voltage (V_g) of -1 V. Writing and erasing operations are performed by pulses of gate voltage to ± 8 V. A current (I_{sd}) of > 1 μA may be switched as shown in Fig 3.1 (c). After an initial decay (~ 50 s), I_{sd} remains constant. The hold time of the memory exceeds 5000 seconds. The author explained the memory effect by charge storage in the dielectric layer just below the SWNT channel. The electric field at the SWNT/SiO₂ interface for $V_g = 10$ V is

estimated as $E = \frac{V_g}{KR_t \ln(R_g / R_t)} \sim \frac{V_g}{23R_t}$,⁶⁸ where $K = 3.9$ is the dielectric constant of

SiO₂, $R_t = 1.35$ nm is the SWNT radius, and $R_g = 500$ nm is the dielectric thickness. Thus $E > 0.3$ V/nm, which is comparable to the breakdown field for SiO₂ (~ 0.25 V/nm), is obtained. Therefore, electrons are easily injected into the dielectric from the SWNT and remain trapped in metastable states until the polarity is reversed. Moreover, it is reasonable to expect movement of the charges in the dielectric at $E = 0.3$ V/nm. Another possible reason is that at such high electrical fields the gas molecules around the SWNT may experience corona discharge, and ionized gas could transport charges to the

dielectric surface. In addition, it is also possible that the high electric field causes a rearrangement of adsorbents on the SWNT, for example, oxygen. The above statements are for sweeping gate voltage from positive to negative; in which electrons are the major carriers at first. The mechanisms are also applicable for sweeping gate voltage from negative to positive; in which holes are the major carriers initially.

Furthermore, the amount of charges stored ΔQ could be obtained from the amount of threshold voltage shift, as $\Delta Q = C_g * \Delta V_{th}$, where $C_g = 54$ aF is the gate capacitance and may be determined directly from low-temperature Coulomb blockade measurements, and $\Delta V_{th} = 6$ V is the shift of the threshold voltage. Hence, $\Delta Q = 3.24 \times 10^{-16}$ C is obtained, that is, around 2000 electrons have been trapped. The carrier mobility μ could also be determined from Fig 3.1 (b) as $\mu = \frac{L^2}{C_g} \frac{dG}{dV_g}$,⁶⁹ where L is the channel length, C_g is the gate capacitance, and $\frac{dG}{dV_g}$ could be obtained from the linear portion of Fig 3.1(b), is calculated for holes as ~ 9000 cm²/V.s (~ 450 cm²/V.s in pure silicon). As a summary, one can see CNTFET has following merits:

- Extremely high carrier mobility ($\mu \approx 9000$ cm²/V.s for hole).
- Small geometrical capacitance ($C_g \approx 54$ aF).
- Enhanced electric field due to cylindrical geometry ($E_{ox} \sim 0.3$ V/nm).

These merits guarantee that local charge density affect the global conductance, as well as high charge injection capability. Therefore, the CNTFET is ideal as a charge-detecting

device. This is an inherent advantage for CNTFET to be used for nanoscale memory device application.

Radosavljević and co-workers reported the nonvolatile memory (NVM) based on n-type CNTFET.⁵⁷ The device was investigated in high vacuum to study the charge traps in bulk SiO₂. As shown in Fig 3.2, the hysteresis increases steadily as V_g -sweeping range increases. This indicates that the hysteresis originates from avalanching injection into bulk oxide traps. Taking Fig 3.2 (c) as an example, after a sweep from -20 to $+20$ V, the threshold voltage moves toward a more positive value (-7 to 2 V); indicating injection of electrons into oxide traps. Electrons are injected from the CNTFET channel, where the electric field is the highest due to the cylindrical device geometry. Fig 3.2 (d) illustrates for electrons injected from CNTFET channel. A memory cell consisting of an n-CNTFET and a $1\text{ M}\Omega$ load resistor is shown in inset of Fig 3.2 (e). Read ($V_{in} = 0$) and write ($V_{in} = +20$ or -20 V) are applied to input terminal (gate). Logical “1” (“0”) is defined as $V_{out} = 1$ V (0 V). To write a “1” (“0”) to the memory cell, V_{in} is switched rapidly to -20 V ($+20$ V) and back to 0 , so that the CNTFET is “on” (“off”) at the read voltage ($V_g = 0$). The outputs as a function of time while a series of data bits is written are shown in Fig 3.2 (e).

Fig 3.2 a)-c) I - V_g curves in high vacuum with $V_{ds} = 0.5$ mV. The sweeping range of V_g is increased from a) to c). d) Diagram of avalanche injection of electrons into bulk SiO_2 from CNTFET channel. e) Data of a nonvolatile molecular memory cell.⁵⁷

Cui *et al.* have investigated the charge storage stability in CNTFET.⁵⁶ They found the charges stored in CNTFET are very stable for more than 12 days at room temperature. Fig 3.3 shows the memory effect at 84 and 12 K. It is noted that the curve measured at 12 K displays numerous sharp peaks originating from single-electron charging of the tube. They also found that reproducible switching could be detected down to 5 K. The persistence of hysteresis at low temperature is not due to the mobile ions within the dielectric since ion hopping is frozen out at liquid-helium temperature (~ 4 K) due to the high associated activation energy. Therefore, they concluded that the mechanism for charge storage in dielectric is not enough to explain the memory effect observed in CNTFETs.

Fig 3.3 Memory effects in an annealed SWNT FET bundle at low temperatures (84 and 12 K).⁵⁶

Kim and co-worker suggested that the hysteresis in CNTFET is caused by charges trapped by water molecules around the nanotubes, including SiO₂ surface-bound water proximal to the nanotubes.⁷⁰ As shown in the inset of Fig 3.4 (a), the CNTFET comprises fully suspended SWNTs over the gate by 2 μm . The hysteresis loop at $V_{\text{ds}} = 10$ mV in ambient air for the device is shown in Fig 3.4 (a). As displayed in Fig 3.4 (b), the hysteresis quickly decreased to near zero after it was placed in vacuum. The author suggested that the charge trapping by water is an important cause of the hysteresis in CNTFETs exposed to the ambient environment. There are two types of water charge traps. Type 1 consists of water molecules weakly adsorbed on the SWNT surface, and these water molecules can be easily removed by pumping as the case in Fig 3.4. Type 2 involves SiO₂ surface-bound water in close proximity to the nanotubes, as shown in Fig 3.4 (c). This finding implies that the carbon nanotube humidity sensors could be explored with suitable water-sensitive coatings. Moreover, hysteresis is almost eliminated when the traps around SWNT-bulk (suspended structure shown in Fig 3.4 (a)) are

removed. Thus, one can conclude, from this work, that the SWNT-bulk instead of the contacts of the CNTFETs play the dominant roles in hysteresis.

Fig 3.4 a) Hysteresis recorded for suspended SWNT FET exposed to ambient air at $V_{ds} = 10$ mV. Inset: A SEM image and a schematic structure of the device. b) Vanished hysteresis recorded with the same device immediately after placing it in vacuum. c) Schematic drawing depicting water molecules hydrogen bonding to the surface Si-OH groups.⁷⁰

Choi *et al.* demonstrated the SWNT-based nonvolatile memory device using $\text{SiO}_2\text{-Si}_3\text{N}_4\text{-SiO}_2$ (ONO) layers as a storage node.⁷¹ The structure of the CNT-flash memory is shown in Fig 3.5 (a). The memory device consists of a top gate structure with a channel width of a few nanometers and the ONO layer (14 nm) embedded between the SWNT and gate electrode. Fig 3.5 (b) shows a SWNT with diameter of 3 nm, length of 1 μm attached between two Au/Ti electrodes. The SWNT channel is completely covered by the ONO film so that atmosphere does not influence the electrical transport property of the SWNT. Two small hysteresis loops are observed at 5 K with different sweeping ranges of V_g . The hysteresis loops is caused by charges trapped in ONO layer. Fig 3.5 (d) shows a quantized increment of threshold voltage of 60 mV when the charging voltage is

changed continuously. The author suggested that each trap site containing charge in the ONO layer of the memory device acts like a quasi-quantized energy state for the flash memory.

Fig 3.5 a) Schematic structure of CNT-based NVM with an ONO charge trap. b) AFM image of the SWNT attached between two metal electrodes. c) I_{sd} - V_g at $V_{sd} = -0.9V$. Two loops correspond to V_g sweeping range of $\pm 8V$ (inner loop) and $\pm 20V$ (outer loop). d) I_{sd} - V_g after charging the ONO storage node with different pulse amplitudes.⁷¹

Star and co-worker combined CNTFETs with a photosensitive polymer to fabricate optoelectronic memory devices.⁷² Two types of photosensitive CNTFET devices were prepared. For the first type of devices, a composite of polymer and nanotubes was deposited from solution onto Si wafers with previously patterned electrical contacts. Its structure and performances are shown in Fig 3.6. The UV illumination modulates the conductivity of the device. However, the modulation ($\frac{\Delta I_{SD}}{I_{SD}}$) is not efficient. This may be caused by the fact that the contact resistance is very high and the

channel of the device consists of both m- and s-SWNTs. For the second type of devices, a polymer layer was deposited over the contacts and SWNTs by drop-casting of 0.05 μL of PmPV (0.1% wt) solution in CHCl_3 from a micropipet. Its structure and performances are shown in Fig 3.7. The polymer itself does not significantly modify the device properties. However, when the device is illuminated with 365-nm light, the transfer characteristic shifts toward positive gate voltage. The threshold voltage change is 2 V. The devices recover slowly, requiring hours to reach their original conductance, when the light is turned off. The memory operation of the devices in air at room temperature is shown in Fig 3.7 (b). The I_{SD} versus time response to UV illumination is measured under alternating V_{G} . The offset of V_{G} is 1 V, amplitude = 4 V and frequency = 1 KHz. Recall that the solution-deposited CNTFETs showed no optoelectronic memory behavior. In contrast, the polymer-coated CNTFETs showed clear optoelectronic memory behavior. Therefore, the authors concluded that the proximity of nanotubes to the silicon oxide substrate is necessary for long-term memory.

Fig 3.6 a) SEM image of PmPV/CNT composite deposited on Si wafer with patterned Au electrodes. b) Current measured during UV illumination cycles in air. The shaded and unshaded region regions mark the UV-on and –off periods, respectively. Inset: schematic device geometry.⁷²

Fig 3.7 Response of PmPV polymer-coated CVD-grown CNTFETs to UV light ($\lambda = 365$ nm). a) I_{SD} - V_G in air with $V_{SD} = 1$ V at UV-off (blue curves) and UV-on (red curves) conditions. Inset: schematic device geometry. b) Memory operation in air at room temperature.⁷²

One more notable published work is modeling of hysteresis by Robert-Peillard *et al.*⁷³ In their model, a CNT contacted to side electrodes and laid on a SiO₂ layer. A model

with full axial symmetry, instead of a planar one, was used. The solution to the planar geometry differed from the axial one near the contacts only. The shift of the threshold voltage was due to the injection and the trapping/detrapping of carriers in the SiO_2 , located within 3 nm around CNT. These trapped electrons created an additive potential to the external potential felt by the CNT charge carriers. The external potential on the CNT could be expressed as the sum of the gate voltage and the potential created by trapped charges in the oxide. The influences of two model parameters, sweeping rate (SR) and the range of the gate voltage ($-V_G^{\text{Max}}$, V_G^{Max}), on the hysteresis (H) were investigated in details.

Fig 3.8 Threshold voltage versus V_G calculated over a full cycle of V_G for different gate voltage ranges. SR = 1 V/s. Inset: width of the hysteresis as a function of V_G^{Max} .⁷³

As shown in Fig 3.8, H increased linearly with the increase of V_G^{Max} for large enough V_G^{Max} . H would saturate at some value depending on the density of available traps. It is obvious in Fig 3.9 that the slower V_G was swept, the larger the density of injected electrons. Though the simulated curves were not exactly the same as experimental observation,⁴⁴ the simulated trends were as expected.

Fig 3.9 Threshold voltage versus V_G calculated over a full cycle of V_G for different SR. $V_G^{\text{Max}} = 10$ V. Inset: semilog plot of the width of the hysteresis as a function of SR.⁷³

From the literature review of hysteresis in CNTFETs, we note that the following progresses have been made so far. Firstly, very clear hysteresis loops have been observed in CNTFETs. Secondly, memory operations based on the hysteresis loops have been demonstrated. Thirdly, some researchers have implemented novel designs such as ONO NVM and optoelectronic memory. Lastly, it is widely accepted that the memory effect in CNTFET is caused by charge storage in the device. However, the origins, distributions and influences of the trapping centers on electrical properties of CNTs are still under argument.

3.2 Device fabrication

3.2.1 SWNT-suspension preparation

Our high-purity SWNTs (95%) were purchased from Materials and Electrochemical Research Corporation. The SWNTs were grown by arc-discharge method. The as-prepared SWNT has average diameter of 1.4 nm (obtained from Raman

spectrum), and length up to 20 μm . The SWNTs are in form of bundles. Fig 3.10 shows the TEM images and the AFM image of the tubes in deionized (DI)-water suspension. On an average, the bundle is very big and wrap around to each other. Therefore, further treatment to the suspension is necessary before device fabrication.

Fig 3.10 a) TEM image of SWNT bundles in DI water. The scale bar is 20 nm. b) Enlarged view of SWNT bundles. c) AFM image of SWNT bundles in suspension (1% wt Triton X 100 in DI water) without sonication.

The treatment is implemented in two steps. Firstly, surfactants are added into the SWNTs suspension of DI water. The surfactants could be sodium dodecylsulfate (SDS), sodium dodecylbenzenesulfonate (SDBS) or Triton X 100.⁷⁴ Secondly, the suspension is put into the ultrasonic cleaner for agitation. The SWNT bundles are found to become much thinner after the treatment. Unfortunately, the SWNTs are also severely shortened. The dispersion of the SWNTs in the suspension depends on the type of surfactants, as well as the time duration of ultrasonic agitation. Triton X 100 is heavily used in the following work.

3.2.2 Substrate and electrodes preparation

The substrate is a silicon wafer capped with a thermally grown SiO_2 layer. The metal electrodes on the substrate are deposited using standard lithography, electron-beam evaporation and lift off. The electrodes typically consist of an Au layer on top of a Ti layer, which is used to increase the adhesion between the Au layer and SiO_2 surface. AFM images of the electrodes made from a “cross” patterns and the schematic structure of the substrate with electrodes are shown in Fig 3.11 (a) and (b), respectively. Any adjacent pair of electrodes could act as the “source” and “drain” electrodes. The distance between two electrodes varies from 1 to 5 μm .

Fig 3.11 a) AFM image of 4 electrodes made from a “cross” pattern mask. b) Schematic structure of the substrate with patterned electrodes.

3.2.3 Ac dielectrophoresis technique⁷⁵

With the SWNTs suspension and the substrate with patterned electrodes, we now proceed to the manipulation of the SWNTs. Take the “cross” electrodes as an example, the set up of the ac dielectrophoresis method is shown in Fig 3.12 (a). An ac bias voltage

was applied between two electrodes. The suspension was agitated in the ultrasonic container for 20-30 mins and then a drop of it was introduced onto the structured wafers, on which an ac bias was applied. The peak-to-peak value of the ac source (sine wave) was within 16 V and the frequency was fixed at 6 MHz. The resistance between the two electrodes is typically decreased to several $K\Omega$ up to tens of $M\Omega$ after SWNTs bridged the electrodes; depending on the characteristics of the contacts and bridged SWNTs. Once the resistance drop was detected, the ac bias was turned off immediately. Then the wafer was rinsed using DI water to clean the wafer surface. The number of SWNTs between the electrodes depends on the deposition time and SWNT concentration of the suspension.

Fig 3.12 a) SEM image of four Au/Ti electrodes (white parts) on a Si/SiO₂ wafer. Ac bias voltage is applied between two adjacent electrodes, as indicated in the figure. AFM images of SWNTs bridging the adjacent electrodes for a deposition time of b) 50 s and c) 300 s, respectively. The black arrows label the direction of the electric field.⁷⁵

The mechanism for this method is as follows. Two forces can drive CNTs in the suspension to the electrodes. One is the electrophoretic force due to charge, the other is the dielectrophoretic force due to the dielectric constant difference between CNTs and the

solvent medium. The time-averaged dielectrophoretic force can be expressed approximately as follows:

$$\vec{F} \propto \epsilon_m \frac{\epsilon_p - \epsilon_m}{\epsilon_p + 2\epsilon_m} \nabla E_{\text{rms}}^2, \quad (3)$$

where ϵ_m and ϵ_p are the dielectric constant of the solvent medium and the SWNTs, respectively, E_{rms} is the average electric field strength. $\epsilon_m = 18.3\epsilon_0$ for IPA as solvent and $\epsilon_p = 2000\epsilon_0$, $2 \sim 5\epsilon_0$, $15\epsilon_0$ for m-SWNTs, s-SWNTs and graphite, respectively. Since the high frequency ac bias is used here, the electrophoretic force does not affect the motion of the SWNTs because of time averaging effect. Since the permittivity of the SWNTs is larger than the other contaminations (for example, amorphous carbon) in the suspension, contamination was rarely found between electrodes under the high frequency bias.

3.2.4 Electrical breakdown

Most of the bridged SWNTs bundles in between two electrodes are a mixture of m- and s-SWNTs. Since the conductance of s-SWNTs display strong dependence on the gate voltage, we can switch off them by adjusting the gate voltage V_g . Most current will pass through m-SWNTs after the s-SWNTs are switched off. With a sufficiently high V_{ds} , a large current passes through the m-SWNTs and generates enough heat to burn them off, leaving the s-SWNTs essentially intact. $I_{\text{d}}-V_{\text{ds}}$ at different V_{gs} before and after the electrical breakdown are shown in Fig 3.13 (a) and (c), respectively.⁷⁵ The on/off ratio ($I_{\text{ON}}/I_{\text{OFF}}$) increases from 2 up to 10^6 after breakdown as shown in Fig 3.13 (d). A high on/off ratio indicates that the current is dominated by s-SWNTs and almost all of the m-

SWNTs are burnt off. Fig 3.13 (b) shows the I_d - V_{ds} curves during the breakdown process. The apparent current drops in curve 1 and 3 indicate breakdown of m-SWNTs in two sweep of V_{ds} . Curve 2 is the I_d - V_{ds} after the first breakdown shown in Curve 1. During the breakdown process, $V_g > 14V$ is maintained to completely deplete the s-SWNTs; while V_{ds} is swept from 0 to a big value gradually.

Fig 3.13 a) I_d - V_{ds} at a series of V_g for an as-prepared device. b) I_d as a function of V_{ds} during the burn-off process. c) I_d - V_{ds} at a series of V_{gs} of the device after burn-off process. Inset: Schematic cross section of a back-gate CNTFET. d). I_d - V_g curve at $V_{ds} = -150$ mV.⁷⁵

The mechanism of the electrical breakdown is as follows. Carbon nanotubes have strong C-C bonds, and their current carrying capacities exceed $10 \mu A/nm^2$. Therefore, the oxidation due to heat generated by large current begins from the sites of defects and dangling bonds on the SWNTs. The m-SWNTs may be not burnt off together at one time. The author suggest that the outmost m-SWNTs in the bundle are burnt off first due to

being fully exposed to oxygen, while the inner m-SWNTs are more stable and need a higher current to burn off.

3.3 Temperature-dependent hysteresis in CNTFETs

As discussed in section 3.1, the origin of the hysteresis is well accepted as charge storage around the CNT-channel. The trapping/detrapping process is associated with an energy activation process. Thus, the temperature and pressure dependence of the hysteresis have been investigated in order to fully understand the phenomenon.

Very significant hysteresis characteristics of the source-drain current versus gate voltage are found in our CNTFETs, which possess ambipolar characteristics. High-purity SWNTs were dispersed in an aqueous solution with surfactant (1% wt Triton X 100). The average diameter and length of the SWNTs are about 1.4 nm and several micrometers, respectively. This suspension was introduced onto pre-structured Au/Ti electrodes on p-type silicon substrates with 500-nm thermally grown SiO₂. The CNTFETs are fabricated using ac dielectrophoresis technique⁷⁵ and electric breakdown process.⁶⁶ The schematic structure of the back-gated CNTFET and its AFM image are shown in Fig 3.14 (a) and (b), respectively. The source and drain electrodes are made of 20-nm Ti /70-nm Au, and the distance between the electrodes is about 2 μm .

Fig 3.14(a) Schematic structure of a back-gated CNTFET. (b) AFM image of a SWNT bundle bridging the source and drain electrodes.

The I_{ds} - V_{gs} curve in Fig 3.15 (a) shows a significant hysteresis loop, which is about 20 V at $I_{ds} \sim 4$ nA. The left arrow in Fig 3.15 (a) indicates a gate voltage sweeping from -20 to $+20$ V, a forward sweeping; while the right arrow indicates a gate voltage sweeping from $+20$ to -20 V, a reverse sweeping. Defining the threshold voltage (V_{th}) as the gate voltage at which the drain current is not more than 0.1% of its saturation value, one can see that the V_{th} of p-type conduction shifts towards left for 8 V (from point A to A') when the pressure is decreased from 760 to 0.1 Torr. While the shift for the reverse sweeping is 6.5 volts (from point B to B'). These shifts of V_{th} move the saturation region towards left. As a result, the current at $V_{gs} = -20$ V in Fig 3.15 (b) is smaller than that in Fig 3.15 (a). The above characteristics have been reproduced for different V_{ds} levels between 250 and 750 mV.

To explain the large shift of V_{th} shown in Fig 3.15 (A to A' and B to B'), we need to review the effects of oxygen on the work function of the Au electrodes. The Fermi level of SWNT is suggested to pin near the valence band edge because of adsorption of oxygen.⁴ While, the adsorption of oxygen slightly increases the work function of the gold electrode.¹⁸ When the pressure decreases, oxygen weakly adsorbed on the SWNT could desorb. This would move the Fermi level towards the middle of the bandgap of SWNT. As a result, the energy barrier for holes tunneling through the contact might increase, while that for electron might decrease. This explains our observation that threshold voltages shift to the left (A to A' and B to B') and p-type saturation current decreases in Fig 3.15 (b) compared to that in Fig 3.15 (a).

Fig 3.15 I_{ds} - V_{gs} curves measured at $V_{ds} = 500$ mV. Hysteresis observed at room temperature and a pressure of (a) 760 Torr, and (b) 0.1 Torr.

Temperature effects on the hysteresis loop are studied under a pressure of 0.1 Torr. As the temperature is decreased from 295 to 16 K, the p-type threshold voltages tend to shift to zero volts for the forward (diamond-dotted curve in Fig 3.16) and reverse (square-dotted curve in Fig 3.16) sweeping. Hence, the magnitude of hysteresis (see triangle-dotted curve in Fig 3.16), i.e., the difference between diamond-dotted and square-dotted curve, is decreased by ~ 12 V. It is noted that the shift of forward curves is about 4 V and that of reverse curves is about 8 V. That is the reduction of hysteresis window size (12 V) is mainly caused by the shift of reverse sweeping curves ($8/12 \sim 67\%$). The reason could be that temperature variation has different effects on electron (reverse sweeping) and hole (forward sweeping) trapping. The observation suggests that electron trapping is easier to be affected by temperature variation than hole trapping.

It is widely accepted that the hysteresis is caused by charge storage around the SWNTs. In our devices, the origin of the charge trapping centers are most likely to be the adsorbents, such as the Triton X 100 molecules, $C_{14}H_{22}O(C_2H_4O)_{10}$. In addition, H_2O molecules⁷⁰ adsorbed on SWNTs during the fabrication process of the devices could also play a role of trapping centers. It is reasonable to assume that the big Triton X 100 molecules cover most of the surface of the SWNT bundle, while O_2 and H_2O molecules cover the rest area. TEM image of the SWNTs shown in Fig 3.17 (b) indicates that the SWNTs were covered by a layer of foreign species. Since the SWNTs are dispersed in the DI water solvent, water molecules are very easily adsorbed onto the SWNT bundles. The structure of the device (Fig 3.14 (a)) makes it easy to be affected by oxygen and water molecules because of large contact surface area exposed to air.

Fig 3.16 Threshold voltage shift with temperatures at 0.1 Torr and $V_{ds} = 500$ mV.

Fig 3.17 (a) TEM images of a SWNT bundle consist of more than 5 SWNTs (The scale bar is 20 nm). (b) Enlarged view of (a).

Decreasing temperature reduces the thermal energy and enhances the difficulty for the carriers to be injected into or get out of the trapping centers. Hence, their contribution to the hysteresis loop is restricted. This could be the reason why the hysteresis loop tends to become smaller when the temperature decreases. The saturation of hysteresis below 200 K could be caused by the suppression of thermionic emission of carrier injection into the trapping centers. In addition, as the temperature is sufficient low, the thermally activated mobile ions could still hop among the shallow trapping centers. This could explain why the hysteresis does not disappear even at 16 K.

The conclusions drawn from the above work are summarized as follows:

- The pressure influences the performances of the devices. This agrees well with the suggestion that oxygen change the work function of the Au electrodes.
- The hysteresis loop decreases with decreasing temperature. This is consistent with the thermally activated charge trapping/detrapping processes.
- The hysteresis loop is not eliminated even at 16 K and 0.1 Torr. This implies that charge trapping due to water molecules⁷⁰ only is not enough to explain the remaining significant hysteresis in the vacuum and low temperatures. Hence, Triton X 100 is suggested to be another important trapping center in our CNTFETs.

3.4 Ammonia-induced hysteresis in CNTFETs

Next, ammonia is introduced and its influence on the hysteresis is studied. So far, it is widely accepted that the adsorbed water,⁷⁰ alcohol⁶⁰ and oxide⁷⁶ play significant roles

of trapping charges in CNT-based devices. Moreover, my previous work suggests that the adsorbents including the surfactant molecules could be other important trapping centers. As a result, pronounced hysteresis occurs in the transfer curves. As discussed in section 3.1, some other materials have also been employed to induce charge traps in CNT-based devices, for example, $\text{SiO}_2\text{-Si}_3\text{N}_4\text{-SiO}_2$ (ONO) layer,⁷¹ photosensitive polymer⁶ etc. Although ammonia (NH_3) has not been used to generate charge traps intentionally yet, it has already attracted much attention in CNTFET-based NH_3 sensors.^{77,78,79} However, some fundamental issues are still not clear. For example, which sites of adsorbed NH_3 molecules (on the CNT channel or at the CNT/electrode contacts) has a significant impact on the performance of CNTFETs?⁸⁰ How do NH_3 molecules adsorb to the CNTFETs?⁵⁹ Could the adsorbed NH_3 trap charges? In this paper, I address the issue for trapping effects induced by NH_3 molecules through observing the variation of the hysteretic behavior in CNTFETs.

Fig 3.18 a) Schematic diagram of a back-gated CNTFET. b) SEM image of a typical CNTFET used in this work.

SWNTs were dispersed in deionized water with 1% wt Triton X 100. After ultrasonic-agitation using a tip-sonicator (MISONIX sonicator 3000) at a power of 480 watt/liter, the suspension was centrifuged (SIGMA sartorius 2-16) with 6461 g for 2 hrs.⁸¹ Then, the up 50% supernatant was carefully decanted. The average diameter of the SWNT bundles in the well-prepared suspension is less than 10 nm. Au (40 nm)/Ti (10 nm) electrodes were pre-structured on heavily boron-doped <100> silicon (resistivity is about 0.01 Ω .cm) wafer capped by 200-nm thermally grown SiO₂ layer. The SWNTs were placed across the electrodes using ac dielectrophoresis technique.^{75, 82} A schematic diagram and a SEM image for a typical back-gated CNTFET are shown in Fig 3.18 (a) and (b), respectively. Electrical breakdown process⁶⁶ was applied to the as-prepared CNTFETs to burn off the metallic SWNTs in the channel. Current on/off ratio of the CNTFETs are $\sim 10^3$.

Fig 3.19 Hysteresis loops of the device at NH_3 concentrations of 0 ppm (red squares), 60 ppm (blue circles) and 80 ppm (orange rhombs), respectively. The arrows (gray) indicate the directions for V_{gs} sweeping.

The well-prepared CNTFETs were characterized in a chamber with different NH_3 concentrations. The flow rate of the diluted NH_3 gas was 500 sccm. Desirable NH_3 concentrations were obtained by diluting NH_3 with nitrogen. The time duration of NH_3 exposure between two successive concentrations was 10 minutes. As shown in Fig 3.19, the square-shaped (red), circle-shaped (blue) and rhomb-shaped (orange) curves are hysteretic characteristics of a typical device at NH_3 concentration of 0 ppm, 60 ppm and 80 ppm, respectively. The hysteresis loops are obtained by sweeping V_{gs} from -7.5 to $+7.5$ V (forward sweeping) and then back to -7.5 V (reverse sweeping) while keeping source-drain voltage (V_{ds}) fixed at 0.5 V. The hysteretic behavior under 0 ppm of NH_3 may be caused by gate oxide and/or adsorbents (including surface water) traps. Since the geometry of the device is analog to a cylinder on a plate, the electric field is much higher at the SWNT/ SiO_2 interface than elsewhere. The value of the electric field is estimated as

$$E = \frac{V_{\text{gs}}}{\epsilon_r R_t \ln\left(\frac{R_g}{R_t}\right)},^{70} \text{ where } V_{\text{gs}} \text{ is the gate voltage, } R_t = 2.5 \text{ nm is the SWNT-channel radius}$$

obtained from AFM height measurement, $R_g = 200$ nm is the gate oxide thickness, and $\epsilon_r = 3.9$ is the dielectric constant of the gate oxide (SiO_2). Thus, the electric field at the SWNT/ SiO_2 interfaces for $V_{\text{gs}} = 7.5$ V is estimated as 0.2 V/nm. It is noted that the electric field is even higher in the region nearby the source/drain contacts due to the local gating effect from V_{ds} . Therefore it is reasonable to expect mobile ions in the gate oxide just under the SWNT to response to the external electric field. Similarly, the high electric field around the SWNT may enable charge injection into other trapping centers around it.

Threshold gate voltages, V_{thA} (mark A in Fig 3.19) and V_{thB} (mark B in Fig 3.19) for the forward and reverse sweeping, respectively, are defined so that $I_{ds} = 2$ nA under $V_{ds} = 0.5$ V. Three trends can be found in Fig 3.19. First, V_{thA} shifts from 0.2 to -2.5 V, while V_{thB} remains almost unchanged. Second, the hysteresis loops change very little as NH_3 concentration exceeds 60 ppm. Lastly, the saturation current (at $V_{gs} = -7.5$ V) is decreased from 1.2 to 0.35 μ A as NH_3 concentration is increased to 60 ppm. It has been shown experimentally that NH_3 adsorption leads to the bulk doping of the CNT body rather than the adjustment of the work function of Au electrodes.^{83,84} This might be a reasonable explanation why the p-type conduction current decreases after NH_3 exposure, as shown in Fig 3.19.

Fig 3.20 Threshold voltages V_{thA} (orange squares), V_{thB} (magenta triangles) and hysteresis-loop size (blue rhombs), respectively, as a function of NH_3 concentrations from 0 to 300 ppm.

The most interesting point here is the different NH_3 effects on V_{thA} and V_{thB} in the forward and reverse sweeping. It is noted that the threshold voltage shift due to NH_3 adsorption only occurs in the forward, but not in the reverse sweeping. This leads to an extra increase in hysteresis loop width, in addition to the original hysteresis, $\Delta V_{\text{th}}(0 \text{ ppm}) \sim 5 \text{ V}$. The dependence of the hysteretic behavior (for the same device as that used in Fig 3.19) on various NH_3 concentrations from 0 to 300 ppm is summarized in Fig 3.20. V_{thA} shifts towards negative V_{gs} with increasing NH_3 concentration as shown by the square-shaped (orange) curve. In contrast, V_{thB} at different concentrations remains almost at the same value (see the triangle-shaped (magenta) curve). The hysteresis-loop size or the threshold voltage differences ($\delta V_{\text{th}} = V_{\text{thB}} - V_{\text{thA}}$) are shown as the rhomb-shaped (blue) curve. The additional hysteresis can be attributed to the charge traps caused by NH_3 or NH_3 -related clusters. On one hand, the donated electrons from adsorbed NH_3 molecules are transferred into the SWNT channel and partially compensate holes, resulting in a decrease in the hole current. On the other hand, the donor ions (NH_4^+) could partially neutralize the negatively charged groups on the SiO_2 surface. The NH_4^+ ions produce a positive electrostatic potential around the SWNT channel. This positive electrostatic potential should lead to an additional suppress for the current. As a result, V_{thA} shifts towards the negative gate voltage. However, the behavior of V_{thB} is associated with a different charging process in the reverse sweeping. When V_{gs} is at the most positive voltage (+7.5 V), accumulated electrons might be extracted out from the SWNT channel and neutralize the NH_4^+ ions. This electron trapping process erases the positive potential caused by NH_4^+ ions so that V_{thB} is not significantly influenced. However, the adsorbed

NH₃ molecules would be ionized again when V_{gs} reaches a sufficiently large negative value. However, we note that the hysteresis may vary about 200 mV if two repeated sweeping are carried out. The reason is the dynamic charge trapping during gate voltage sweeping. Therefore, a 200 mV error bar should be included in the hysteresis plot.

NH₃ adsorption could occur in the following ways: (1) NH₃ could bind to hydroxyl groups on the SiO₂ substrate;⁵⁹ (2) NH₃ could interact with the pre-adsorbed oxygen species and bind through them,⁸⁵ and (3) NH₃ may be dissolved in a water monolayer that might exist on the surface of the testing devices. In addition, water molecules may be weakly adsorbed on the SWNT surface or strongly adsorbed through SiO₂ surface bound in close proximity to the SWNTs. A schematic diagram shown in Fig 3.21 (a) illustrates NH₃-related bonds. In order to study the effects of various kinds of adsorbed NH₃ molecules on the charge trapping process, the devices were annealed in dry air at 200 °C for more than 2 hrs and then kept them in dry air at room temperature for about 20 hrs. After the treatment, the devices were found to become pure p-type (not shown here) and the saturation current recovered to the value before introducing NH₃ gas. A new group of the NH₃ exposure experiments were performed with the annealed CNTFETs. The main features of the response of the devices to NH₃ still remain. ΔV_{th} before (the same as the rhomb-shaped curve in Fig 3.20) and after annealing are shown in Fig 3.22 for comparison. One can see that the hysteresis-loop size is reduced by 2 ~ 3 V (about 50%). Furthermore, the additional hysteresis due to NH₃-related charges traps is also decreased from 2.2 to 1.5 V on average.

Fig 3.21 Schematic drawing for NH_3 adsorption (a) before and (b) after annealing.

Fig 3.22 Hysteresis- loop sizes before and after annealing.

It is well accepted that adsorption of oxygen shifts the Fermi level of SWNTs close to the valence band.⁴ Typical as-prepared CNTFETs prepared from IPA and deionized water (SDS as surfactant) suspensions show p-type characteristic.^{4,86} However, 9 out of 10 CNTFETs prepared using Triton X 100 as the surfactant are found to show ambipolar characteristics. A tentative interpretation is that Triton X 100 molecules adsorbed in the devices may change the work function of Au electrodes so that the Fermi level of Au electrodes approaches to the middle of the SWNT bandgap,⁸⁷ resulting in ambipolar characteristics.⁸⁶ However, it is noted that Triton X 100 molecules could be decomposed at 200 °C. This can explain why our ambipolar CNTFETs become p-type after the annealing. Notably, the adsorption energies of H₂O (143 meV) and NH₃ (149 meV) to SWNTs are much smaller than that for oxygen (509 meV).⁸⁰ As a result, the dry-air-annealing process could completely desorb the water molecules weakly adsorbed on the SWNTs and partially remove the SiO₂ surface-bound water molecules. Hence, the NH₃ adsorption through the water molecules is most likely removed. The schematic diagram for the NH₃ adsorption after annealing is shown in Fig 3.21(b).

The number of trapped electrons can be estimated using $\Delta Q = C * \Delta V_{th}$, where C is the gate oxide capacitance, which is about 0.5 aF and can be obtained directly by a Coulomb blockade measurement⁸⁸ at 15 K (details will be discussed in Chapter 5). Therefore, the additional charge trapping by NH₃ at 60 ppm ($\Delta V_{th} = 2.5$ V as shown in Fig 3.20) is 7.8 electrons, much smaller than those transferred by NH₃ in deionized water solution (40 electrons).⁸⁵ A theoretical study predicts that one NH₃ molecule can donate 0.04 electrons.⁸⁹ Thus, there could be 195 NH₃ molecules actually participating the

charge-transfer process at 60 ppm before the annealing. In contrast, the acting NH_3 molecules adsorbed could be about 117 after the annealing, suggesting a significant reduction of the number of adsorption sites for NH_3 molecules. These numbers are much smaller than that reported in Ref 85 (~23000 for a NH_3 concentration of 1.2 M). The difference is understandable by taking the NH_3 phase into account. We use gas-phase NH_3 , which is more difficult to be adsorbed on SWNTs than ammonia solution used by them. In addition, NH_3 concentration here (300 ppm) is much smaller than that used in Ref 85 (1.2 M, equivalent to 2% of the total molecules are NH_3).

The conclusions drawn from the above works are as following,

- The charge-trapping effects caused by NH_3 molecules through the hysteretic behavior of CNTFETs have been studied. In forward V_{gs} sweeping, the threshold voltage shifts to negative V_{gs} sensitively with increasing NH_3 concentration up to 60 ppm and it remains almost unchanged from 60 ppm to 300 ppm. However, the threshold voltage for reverse V_{gs} sweeping does not change significantly.
- This observation is repeatable for different NH_3 concentrations and for both ambipolar (before annealing) and unipolar p-type (after annealing) CNTFETs. The influences on the threshold voltage suggest that adsorbed NH_3 molecules could play a role of not only electron donors, but also electron/hole trapping centers.

3.5 Elimination of hysteresis in CNTFETs

Though a well-controlled hysteretic behavior of CNTFETs is useful for electronic memory applications, it is undesirable for transistor applications. Hence, a passivation method is developed to reduce the hysteresis in CNTFETs. In addition, the devices with passivation layers⁹⁰ are found to become n-type from p-type or ambipolar. In the following, I report on the introduction of the Si_3N_4 and SiO_2 dielectric layers passivation to eliminate the hysteresis, and study the influences of the passivation on the performances of CNTFETs.

Fig 3.23 Device A before the top Si_3N_4 layer was deposited (a) I_{ds} - V_{ds} curves at different V_{bgs} (back-gate voltage) from -8 V to +8 V with a step size of 4 V. (b) Transfer curves in forward V_{bgs} (back-gate voltage) sweeping (from -8 V to +8 V) and reverse V_{bgs} (back-gate voltage) sweeping (from +8 V to -8 V) at $V_{ds} = 500$ mV. Upper inset: SEM image of a SWNT bundle bridging two Au electrodes (The white scale bar is 500 nm). Lower inset: schematic measurement setup. The ports labeled with S, D, and BG represents the Source, Drain, and Back-gate, respectively.

In this work, the highly purified SWNTs were dispersed in deionized water with 1% wt sodium n-dodecyl sulfate (SDS) as the surfactant. The suspension was ultrasonically agitated for 2 mins, and then centrifuged at 6461 g for 2 hrs. Finally, the upper 50% supernatant was carefully decanted. The Au (40 nm)/Ti (10 nm) source/drain contacts are patterned on heavily boron-doped <100> silicon wafer (resistivity is about 0.01 $\Omega\cdot\text{cm}$) capped by a 200-nm thermally grown SiO_2 layer. The distance between a pair of electrodes is about 1 to 2 μm . CNTFETs were fabricated using ac dielectrophoresis technique and electrical breakdown processes. The as-prepared CNTFETs typically show p-type characteristics and significant hysteresis in the plot of the source-drain current (I_{ds}) versus back-gate voltage (V_{bgs}). After being measured and tested, those devices were coated with a layer of Si_3N_4 (using a mixed flow gases of 100 sccm diluted 4% silane gas, 30 sccm ammonia gas and 1000 sccm nitrogen gas at 300 °C with 40 W RF power for 8 mins) or SiO_2 (using a mixed flow gases of 100 sccm diluted 4% silane gas, 20 sccm nitrous oxide gas and 1000 sccm nitrogen gas at 300 °C with 60 W RF power for 8 mins) using a Plasma-Therm 790 plasma-enhanced chemical vapor deposition (PECVD) system. Finally, the top-gate electrodes were fabricated. All measurements and tests were carried out in atmosphere environment using a HP 4156B semiconductor parameter analyzer.

Fig 3.24 Device A after the top Si_3N_4 layer and gate electrode were prepared (a) I_{ds} - V_{ds} curves at different V_{bgs} (back-gate voltage) from -8 to +8 V with a step size of 4 V. (b) Transfer curves in forward V_{bgs} (back-gate voltage) sweeping (from -8 to +8 V) and reverse V_{bgs} (back-gate voltage) sweeping (from +8 to -8 V) at $V_{ds} = 500$ mV. Inset: schematic measurement setup.

DC characteristics of Device A before coating top-gate dielectric are shown in Fig 3.23. Fig 3.23 (a) shows I_{ds} versus V_{ds} (source-drain voltage) at different back-gate voltages (V_{bgs}) from -8 to 8 V with a step size of 4 V. The p-type characteristics of CNTFETs have been attributed to oxygen adsorption.^{4,42} Oxygen causes the Fermi level of SWNT situated very close to the valence band. Hence, the Schottky barrier for holes is significantly smaller than that for electrons. As shown in Fig 3.23 (b), the circle-shaped and square-shaped curves are the forward (from -8 to +8 V) and reverse (from +8 to -8 V) sweeping in V_{bgs} , respectively. An anti-clockwise hysteresis loop is formed with a maximum V_{bgs} shift of 4 V (V_{bgs} changes from ~ 4 to ~ 8 V at $I_{ds} = 1$ nA). The hysteresis phenomenon has been suggested to be caused by charge storage around the SWNT channel.⁵⁵ Due to geometry of the devices, the electric field is greatly enhanced at SWNT/SiO₂ interfaces than elsewhere. The enhanced electric field could be estimated using $E = \frac{V_{gs}}{\epsilon_{gd} r \ln(\frac{t_{gd}}{r})}$,⁵⁵ where V_{gs} is the gate voltage, $r = 3$ nm (the SWNT bundle radius obtained from AFM height measurement), $t_{gd} = 200$ nm (the back-gate dielectric thickness), and $\epsilon_{gd} = 3.9$ (the dielectric constant of SiO₂). Thus, the electric field at SWNT/SiO₂ interfaces for $V_{gs} = 8$ V is estimated to be 0.16 V/nm. It is noted that the electric field could be even higher near the source/drain contacts due to local gating effect caused by V_{ds} . Under such a high local electric field, charges could transfer between the SWNT-channel and traps in SiO₂ layer and/or adsorbed molecules, such as water and alcohol.^{70,76}

After a 106-nm thick Si_3N_4 layer is deposited on Device A, n-type characteristic is observed as shown in Fig 3.24 (a). The n-type characteristic might be caused by the removal of oxygen adsorbed on SWNT channel during the deposition of Si_3N_4 layer. This is consistent with the findings by other groups, i.e., desorption of oxygen by annealing CNTFETs in vacuum or inert gas promotes p- to n-type conversion.^{4,18} Oxygen desorption could cause the Fermi level to shift towards the conduction band so that the Schottky barrier for holes becomes much higher than that for electrons. Since our devices have been heated in the PECVD chamber up to 300 °C at 10 mTorr prior to the Si_3N_4 deposition, most of the adsorbed oxygen molecules could desorb. Compared to Fig 3.23 (b), the V_{bgs} shift is significantly reduced from ~ 4 to ~ 0 V at $I_{\text{ds}} = 1$ nA (see Fig 3.24 (b)). Since coating the top-gate dielectric layer is not likely to affect those traps in the back-gate dielectric, we suggest that the significant hysteresis in Fig 3.23 (b) is mainly caused by adsorbents instead of the possible traps in the back-gate dielectrics. In addition, it is noted that the saturation current decreases from ~ 370 nA at $V_{\text{bgs}} = -8$ V to ~ 170 nA at $V_{\text{bgs}} = +8$ V, while the minimum current level remains almost unchanged. The reduction in saturation currents could be caused by the higher Schottky barrier for electrons in the converted n-type device than that for holes in the as-prepared p-type device.

Fig 3.25 (a) I_{ds} - V_{ds} curves at different V_{tgs} (top-gate voltage) from -8 to +8 V with a step size of 4 V. (b) Transfer curves in forward V_{tgs} (top-gate voltage) sweeping (from -8 to +8 V) and reverse V_{tgs} (top-gate voltage) sweeping (from +8 to -8 V) at $V_{ds} = 500$ mV. Inset: schematic measurement setup. Port TG represents the top-gate electrode.

Fig 3.25 (a) and (b) show I_{ds} - V_{ds} curves at different top-gate voltages (V_{tgs}) and hysteretic characteristic for Device A, respectively. The saturation current is ~ 510 nA at $V_{tgs} = 8$ V. The difference between the saturation currents for the back- and top-gate cases is likely due to a better gate coupling with the top-gate contact. The gate capacitance (C_{gs})

could be estimated by $\frac{2\pi L \epsilon_{gd} \epsilon_0}{\ln(2 \frac{t_{gd} + r}{r})}$,⁹¹ where $L = 1500$ nm is the length of the SWNT

channel, ϵ_{gd} is the dielectric constant of gate dielectrics, ϵ_0 is the permittivity in vacuum, t_{gd} is thickness of the gate dielectrics and $r = 3$ nm is the radius of SWNT channel. Thus, the back-gate capacitance is ~ 66 aF with $\epsilon_{gd} = 3.9$ and $t_{gd} = 200$ nm, and the top-gate capacitance is ~ 152 aF with $\epsilon_{gd} = 7.8$ and $t_{gd} = 106$ nm. Higher gate capacitance, hence better gate coupling, may result in a higher saturation current. However, a clockwise hysteresis loop with a maximum gate voltage shift of ~ 1.5 V is observed. This could be caused by the poor quality of PECVD grown Si_3N_4 layer which may have many traps.⁹²

Fig 3.26 Device B after the top SiO₂ layer was deposited (a) I_{ds} - V_{ds} curves at different V_{bgs} (back-gate voltage) from -8 to +8 V with a step size of 4 V. Inset: I_{ds} - V_{ds} curves before the top SiO₂ layer was deposited. (b) Transfer curves in forward V_{bgs} (back-gate voltage) sweeping (from -8 to +8 V) and reverse V_{bgs} (back-gate voltage) sweeping (from +8 to -8 V) at $V_{ds} = 750$ mV. Left inset: schematic measurement setup. Right inset: transfer curves before the top SiO₂ deposition.

Device B is another CNTFET coated with 520-nm thick top SiO₂ layer. Fig 3.26(a) shows the I_{ds} - V_{ds} curves at different back-gate voltages (V_{bgs}) after introducing SiO₂ top-gate dielectric. Compared to its as-prepared transfer curves prior to the top SiO₂ coating as shown in the inset of Fig 3.26 (b), one can see that Device B has converted to n-type. The capped Device B is hysteresis-free with its back-gate electrode (V_{bgs}), as shown in Fig 3.26(b).

Our results of top-gated CNTFETs with the top Si₃N₄ layer are consistent with Ref 93, where a thermal chemical vapor deposition process (at 800 °C) was used to coat the top Si₃N₄ layer. These suggest that low-RF power process with PECVD is a proper technique for top-gate dielectric deposition. It is also noted that our results are significantly different from Ref 94, whose authors suggested that the CNTs were destroyed by oxygen-related species through chemical reaction when PECVD was used to deposit the top SiO₂ layer. They found that their CNTFETs with top Si₃N₄ coating showed p-type characteristics. In our experiments, a low RF power was used for the top-gate dielectrics deposition to minimize the potential damage to SWNTs. Furthermore, our deposition temperature was about 300 °C, while their deposition temperature was about 225 °C, at which desorption of oxygen may be incomplete, resulting in p-type characteristics in their devices.

The conclusions drawn from this work are as follows:

- Si₃N₄ and SiO₂ layers have been introduced as the top-gate dielectrics on back-gated p-type CNTFETs. After the top-gate dielectrics were deposited, the devices are found to convert to n-type with both back- and top-gate configurations.

➤ Significant hysteresis observed in the as-prepared back-gated CNTFETs is eliminated almost completely after coating the top-gate dielectrics. The hysteresis in back-gated CNTFETs is more likely to be caused by charge storage associated with foreign molecules adsorbed around the SWNT channels.

3.6 Conclusions

Significant hysteresis has been found in our CNTFETs. Temperature and pressure-dependence of hysteretic phenomena are consistent with the thermally activated charge-trapping model. Hysteresis loop size is decreased when temperature is decreased from room temperature down to 16 K because the thermally activated hopping of carriers into and out of the trapping centers is difficult at low temperatures. Ammonia-related trapping centers are found in our CNTFETs. These trapping centers are surface water-related, which can be reduced by annealing in dry air. Elimination of hysteresis by capping the device with dielectric layers at high temperatures in vacuum is achieved. The results show that the major source of trapping centers in our uncovered device is gas adsorption-related.

Chapter 4

Global and Local Charge Trapping in CNTFETs

4.1 Introduction

A clear picture of transport mechanism in CNTFET has been a hot argument issue since the invention of the devices. In the early stage, the CNT-channel conductance in CNTFETs was controlled by the semiconducting nature of the CNT channel. Not long after, it was found that CNTFETs could work as the Schottky barrier (SB) devices. Later on, it has been found that a partial gate, which is used to control the electrostatic field of bulk-CNT instead of CNT/metal contacts, can also switch a CNTFET with large current on/off ratio (bulk switching). A detailed review on both switching mechanisms will be carried out in this section.

4.1.1 Schottky-barrier switching

According to the SB model, a barrier (for electron transport) with the height of $\phi_B = \Phi_{\text{metal}} - \chi_{\text{SWNT}}$, where Φ_{metal} is the metal work function and χ_{SWNT} is the electron affinity in SWNT, forms at the metal/SWNT contact. Similarly, a barrier (for hole

transport) with the height of $\phi_B = x_{\text{SWNT}} + E_g - \Phi_{\text{metal}}$ also exists. Therefore, carriers must tunnel through the SB to enter the CNT-channel. Moreover, due to the small band gap of SWNT ($E_g \sim 600$ meV in this work), some carriers that are thermionically activated could be injected over the small SB. Tunneling and thermionic emission over the SB are considered to be the two main transport mechanisms for CNTFETs. These two mechanisms compete each other to determine the channel current at high temperature ($T > 100$ K usually).⁹⁵ The back-gate voltage generates a global electrostatic field to control the width of SB, hence the transparency of the contacts.

We take Ref 95 as the main reference for the hole transport in the SB-CNTFETs. The conclusions are also applied to electron transport in the SB-CNTFETs. Fig 4.1 simulates the transfer curves of a CNTFET with 10-nm-thick gate oxide (SiO_2) at different temperatures ranging from 300 to 50 K. The schematic band diagrams (for hole transport and $\Phi_B = 300$ meV) at the SB contact of the device are the inset to the figure. Moreover, simulation results of the other CNTFET with 2-nm-thick gate oxide ($\Phi_B = 150$ meV) are shown as the inset of Fig 4.1. There are two interesting characteristics in the I_d versus $1000/T$ curves: (1) the curve becomes more linear when V_{gs} is increased positively, and (2) two regimes are seen in one curve, i.e., above and below 200 K. The authors suggest that thermionic emission dominates the transport at sufficiently positive V_{gs} and $T > 200$ K. Otherwise, tunneling determines the current.

The extracted barriers heights versus gate voltage for different device parameters are shown in Fig 4.2. The valence band of the SWNT bends downwards under positive V_{gs} , hence holes must overcome the barrier to be injected from the drain to source.

Tunneling is impossible since the barrier is too thick ($\sim$ channel length). If the device is in “OFF” region, i.e., there is no carrier in the channel, increase in V_{gs} will be directly cause a corresponding change in barrier. Therefore, the curve Φ_B - V_{gs} is linear between B and C,

Fig 4.1 Simulated T -dependent current as a function of V_{gs} for a CNTFET ($t_{ox} = 10$ nm and $\Phi_B = 300$ meV). $T = 300, 200, 150, 100$, and 50 K from top to bottom. The inset shows $I_d(1/T)$ for another simulation with $t_{ox} = 2$ nm and $\Phi_B = 150$ meV at $V_{gs} = -0.2, -0.1$, and 0 V (from top to bottom).

Fig 4.2 Barrier height as evaluated assuming thermionic emission theory as a function of V_{gs} for various FETs. (i) $m^* = 0.1 m_0$, $t_{ox} = 2$ nm, and $t_s = 1.4$ nm, (ii) $m^* = 1.0 m_0$, $t_{ox} = 2$ nm, and $t_s = 1.4$ nm, (iii) $m^* = 0.1 m_0$, $t_{ox} = 10$ nm, and $t_s = 1.4$ nm, (iv) $m^* = 1.0 m_0$, $t_{ox} = 10$ nm, and $t_s = 5$ nm.

as shown in Fig 4.2. Tunneling will set in after point B, which is the flat-band voltage of the device. Hence, Φ_B at point B is exactly the Schottky barrier height for hole transport. In the limit of a thick gate oxide (or a two-terminal device), a large size semiconductor (as in a conventional 3-D semiconductor) or for a large effective mass (m^*), the thermionic emission limit is reached indicated by the line A-B-C. There is no dependence of Φ_B on V_{gs} up to 0 V, the barrier height is true for the entire V_{gs} region.

4.1.2 Partial top-gate switching

When a top-gate is far from the source and drain contacts, gate electric field will not affect the contact barriers. The transport through the channel would be purely controlled by electrostatic field in bulk SWNT. We take Ref 54 as the main reference to review a band-to-band tunneling process. As shown in Fig 4.3 (a), the partial-gate length was about 1/3 of the channel length to minimize the influence of the partial-gate voltage on the potential barriers at the source and drain contacts. The partial-gate oxide was 4-nm thick Al_2O_3 and the global back-gate oxide was 200-nm thick SiO_2 . The back-gate was biased at a negative value to switch on the p-type device. Then the top-gate was swept from -1.5 to 0.5 V as shown in Fig 4.3(b). The top-gate screens the electric field of the back-gate since it was situated in between the back-gate and SWNT-channel. There are two branches, i.e., the p-type and n-type branch, in the transfer curves. The inverse subthreshold swing $S = 65$ mV/dec for the p-type branch, approaching the limit of conventional MOSFETs at room temperature, i.e., 60 mV/dec. However, the inverse subthreshold swing $S = 40$ mV/dec for the n-type branch, implying that tunneling instead

Fig 4.3 (a) SEM of a band-to-band tunneling device. The schematic in the bottom portion of the figure shows the vertical arrangement of gates, contacts, and nanotubes. (b) $I_d(V_{gs-Al})$ for a drain voltage of $V_{ds} = -0.5$ V and $V_{gs-Si} = -3$ V. Simulated electrical characteristics are for three different t_{ox-Al} and $t_{ox-Si} = 10$ nm with corresponding values for the dielectric constants of 5 and 4, respectively.⁵⁴

of thermionic emission dominates the electron transport. Band-to-band (BTB) tunneling was proposed to explain the n-type branch. The simulated energy band diagrams are shown in Fig 4.3(b) to illustrate the BTB process. The segment of SWNT underneath the partial top-gate is electrostatically doped to be n-type, meanwhile, the adjacent part of SWNT are electrostatically doped to p-type by the back-gate. Hence a very short transition region (delineated by the pair of dashed lines) could be formed at the p-n junction. The barrier is so thin that the holes in the valence band could directly tunnel into the conduction band. The transition region length in case of CNT is a function of tube diameter and gate oxide thickness rather than only doping of the channel. This property

allows one to obtain substantial tunneling current and abrupt switching of the device by a combination of thin CNT and gate oxide.

4.2 The effects of globally and locally trapped charges

Although a robust passivation layer or a thin gate dielectric layer could decrease the effects of the hysteresis, it was not completely eliminated in most cases. The worst thing is that the hysteresis varies with the device fabrication processes, post-fabrication treatment details and even measurement conditions. Further investigations on the effects of the hysteresis are necessary. In this work, we examine the effects of trapped charges at the metal/CNT contacts and CNT body on the CNT-channel conductance separately.

Fig 4.4 (a) AFM image before the partial top-gate fabrication and surface profile along line A-B. (b) AFM image and schematic configuration for a partially top-gated CNTFET. “S”, “D”, “GBG” and “PTG” represent source, drain, global back-gate and partial top-gate terminals. The units of the dimensions are μm.

A SWNT bundle was bridged between a pair of Ti/Au electrodes separated by 6-9 μm using ac dielectrophoresis technique. The substrate was heavily doped p-type Si coated with 500-nm-thick thermally grown SiO_2 , which serves as the back-gate dielectric. After the electrical breakdown process, a 50-nm thick Si_3N_4 film⁹⁴ was deposited using a plasma-enhanced chemical vapor deposition (PECVD) system at a deposition rate of 26 nm/min using a mixed flow gases of 100-SCCM 10% silane gas (diluted by hydrogen gas), 20-SCCM 99% ammonia gas and 500-SCCM nitrogen gas. The deposition temperature and RF power were 300 °C and 40 W, respectively. Then, the top-gate (Ti/Au) was fabricated by the standard lithography technique and lift-off process. The AFM images of the device are shown in Fig 4.4. Globally trapped holes and electrons were introduced by applying a voltage pulse of -25 V (named pulse 1) and +25 V (named pulse 2) to the back-gate, respectively. In contrast, voltage pulses of -4.5 V (named pulse 3) and +4.5 V (named pulse 4) were only exerted on the top-gate to inject trapped holes and electrons near the top-gate, respectively. The durations of all voltage pulses were 20 seconds and source-drain voltage (V_{DS}) was fixed at 0.25 V for all experiments.

Fig 4.5 (a) Source-drain current versus global back-gate voltage curve in ambient environment at $V_{DS} = 0.25$ V when the partial top-gate is floating. (b) Schematic energy band diagrams at $V_{BGS} = 0$ V for the forward (■) and reverse (●) sweeping. (c) I_{DS} - V_{BGS} curves at $V_{DS} = 0.25$ V after applying pulse 1 (blue rhombi) and pulse 2 (red circles), respectively. Inset: the same curves plotted in log scale.

Fig 4.5 (a) shows the source/drain current (I_{DS}) versus the global back-gate voltage (V_{BGS}) prior to applying any voltage pulses with the floating top-gate. The sweeping direction of V_{BGS} follows $\mathcal{A} \rightarrow \mathcal{B} \rightarrow \mathcal{C} \rightarrow \mathcal{D} \rightarrow \mathcal{A}$. In the following, “forward sweeping (FS)” refers to the voltage sweeping from negative to positive and “reverse sweeping (RS)” means an opposite-direction sweeping. Pulses 1 and 2 significantly affect I_{DS} versus the partial top-gate voltage (V_{TGS}) curves as shown in Fig 4.6 (a). The sweeping direction of circle-shaped transfer-curves follows $\mathcal{A} \rightarrow \mathcal{B} \rightarrow \mathcal{C} \rightarrow \mathcal{D} \rightarrow \mathcal{A}$, where $\mathcal{A}$, $\mathcal{B}$ ($\mathcal{D}$) and $\mathcal{C}$ refer to the points of maximum p-type conductance, minimum conductance and maximum n-type conductance, respectively. The effects of pulses 3 and 4 on I_{DS} - V_{TGS} curves are shown in Fig 4.6 (c). The device remains at “ON” state with $I_{DS} \sim 100$ nA for both FS- and RS- V_{TGS} sweeping after applying pulse 3. In contrast, the device stays at “OFF” state with I_{DS} of ~ 0.4 nA after applying pulse 4.

Origin of the hysteresis in our devices could be trapped charges located (1) in adsorbed water molecules or/and IPA on the surface of CNT-channel,^{70,76} (2) on the Si_3N_4 film due to surface charges, (3) in the bulk of SiO_2 film, (4) in the bulk of Si_3N_4 film, and (5) at the $\text{Si}_3\text{N}_4/\text{CNT}/\text{SiO}_2$ interface.⁹⁶ The water-related traps are usually found to dominate in as-prepared CNTFETs before coating the top dielectric-layer. However, this possibility could be ruled out here, as most of the adsorbed molecules desorb at 300°C during coating the top Si_3N_4 layer, which isolates the CNT-channel from air later on. Since the surface-trapped charges caused by dangling bonds on Si_3N_4 film are located 50 nm (top-gate dielectric layer thickness) away from the CNT-channel, their effects could be much less than the traps in the Si_3N_4 bulk and those at the $\text{Si}_3\text{N}_4/\text{CNT}$ interface,

which are located much closer to the CNT-channel. Moreover, the charge traps in the high-quality thermally grown SiO₂ is negligible in comparison with those in PECVD-deposited Si₃N₄. Therefore, in our partially top-gated CNTFETs, charge traps are most likely to originate from the bulk Si₃N₄ layer and Si₃N₄/CNT/SiO₂ interfaces.

In Fig 4.5 (a), I_{DS} at $V_{BGS} = 0$ V in the FS-curve nearly equals the maximum I_{DS} (at $V_{BGS} = +20$ V), suggesting that the Au/SWNT contact barriers for electrons could be minimized, as shown in Fig 4.5(b) (i). In contrast, I_{DS} at $V_{BGS} = 0$ V in the RS-curve is very close to the minimum I_{DS} (at $V_{BGS} = 4$ V), indicating that electrons and holes should face nearly equal potential barriers ($E_e \approx E_h$), as shown in Fig 4.5(b) (ii). The sweeping-direction-dependent conductance at $V_{BGS} = 0$ V can be attributed to the charge-trapping effects. The electric field induced by the global-back gate at the SiO₂/SWNT interface can be estimated by $E_{BGS} \approx \frac{V_T}{\epsilon_r r \ln(t/r)}$,⁵⁵ where $\epsilon_r = 4$ is the dielectric constant of SiO₂, $r \approx 5$ nm (obtained from Fig 4.4 (a)) is the radius of the SWNT-channel consisting of a SWNT bundle, $t = 500$ nm is the thickness of the back-gate dielectric and V_T is the total external potential seen by the charge carriers flowing in the channel. V_T is the sum of V_{BGS} and the potential induced by trapped charges. For $V_T \sim V_{BGS} = 20$ V without trapped charges, $E_{BGS} \sim 217$ MV/m is obtained. This electric field is sufficient to inject charges from the CNT-channel into the surrounding trapping centers. These charge-trapping centers located in Si₃N₄ film are likely to be caused by trivalent silicon atoms according to amphoteric model.⁹⁷ One dangling bond and three satisfied bonds with three nitrogen atoms are associated with a trivalent silicon atom. There are three possible charge states,

i.e., positive (hole trapping), neutral and negative (electron trapping) corresponding to the cases where zero, one and two electrons are attached to the dangling bond, respectively. Two discrete transitional energy levels associated with hole trapping/neutral states and electron trapping/neutral states, respectively.

The FS-curves shown in Fig 4.5 (c) were measured after applying pulses 1 and 2, respectively. The applied voltage pulses significantly influence the transconductance (dI_{DS}/dV_{BGS}), which reflects the variation of field-effect mobility, $\mu_{CNTFET} \propto |dI_{DS}/dV_{BGS}|$.⁹⁸ In comparison with the rhomb-shaped transfer curve, μ_{CNTFET} of hole-conduction branch of the circle-shaped transfer curve decreases by a factor of ~ 1.4 ($\approx 50/35$) (see inset for the same pair of curves plotted in log scale). We attribute the degradation in μ_{CNTFET} to the local potential fluctuations caused by the trapped charges, which could scatter hole transport in the CNT-channel. The observation that μ_{CNTFET} of transfer curves with applied pulse 1 is larger than that with applied pulse 2 may suggests (1) pre-trapped holes have less effect on hole transport than pre-trapped electrons, or (2) the number of pre-trapped holes is much smaller than that of pre-trapped electrons. The latter suggestion is consistent with Lee *et al.*'s findings,⁹⁹ where the number of trapped electrons is much larger than that of trapped holes in Si_3N_4 film. However, for the electron-conduction branches, μ_{CNTFET} under the influences of both pulse 1 and 2 are comparable. The reason could be that the negative V_{BGS} sweeping overwrites the effects of pulse 2, and hence both curves are dominated by hole trapping in the electron-conduction branches.

Fig 4.6 (a) I_{DS} - V_{TGS} curves at $V_{DS} = 0.25$ V after applying pulse 1 (blue rhombi) and pulse 2 (red circles), respectively. (b) Schematic energy band diagrams at (i) point A and (ii) C in (a). (c) I_{DS} - V_{TGS} curves at $V_{DS} = 0.25$ V after applying pulse 3 (blue rhombi) and pulse 4 (red circles), respectively. Inset: schematic energy band diagrams after applying pulse 3 (solid-lines) and pulse 4 (dotted-lines).

Fig 4.6 (a) shows the effects of globally trapped charges on V_{TGS} -sweeping characteristics. The circle-shaped curves (after applying pulse 2) are taken as an example for discussion. The sweeping direction follows $\mathcal{A} \rightarrow \mathcal{B} \rightarrow \mathcal{C} \rightarrow \mathcal{D} \rightarrow \mathcal{A}$. The energy band diagrams at point A and C are illustrated in Fig 4.6 (b) to interpret the carrier transport process. It is noted that the charges induced by pulse 1 and 2 are distributed along the whole channel, including the Au/SWNT contacts and SWNT body. Thus, the pre-trapped electrons induced by pulse 2 shift the entire energy bands upwards, reducing the barriers for holes and thus enhance the hole transport. However, $V_{\text{TGS}} = -4$ V somewhat suppress the hole transport as shown in Fig 4.6 (b) (i). In contrast, the electric field induced by $V_{\text{TGS}} = +4$ V and its fringing field move the energy bands in the center of the channel downwards, as shown in Fig 4.6 (b) (ii). As a result, the energy barriers at the source/drain side are significantly narrowed so that electrons could tunnel into the channel.

Here, the channel conductance is determined by three factors: (1) the pre-trapped electrons induced by pulse 2, (2) the electric field of V_{TGS} and (3) the trapped charges induced by V_{TGS} sweeping. Firstly, the charge trapping effects arising from pulse 2 determine the position of the circle-shaped curves. For instance, the voltage difference between B and B' is 1.4 V, implying a trapped charge difference (caused by the difference between effects of pulse 1 and 2) of $\Delta Q = C_{\text{TGS}} \times \Delta V_{\text{th}} \approx 1.1 \times 10^4 |q|$ ($q = -1.6 \times 10^{-19}$ is the element charge) with $C_{\text{TGS}} \approx \frac{2\pi\epsilon_0\epsilon_r l}{\ln(2h/r)} = 1.3$ fF,⁷⁰ where thickness $h = 50$ nm and dielectric constant $\epsilon_r = 7.8$ for the top-gate dielectric of PECVD-deposited Si_3N_4

layer, and the SWNT-channel radius of $r = 5$ nm and length of $l = 8.8$ μm obtained from the AFM images shown in Fig 4.4. Secondly, the effect of V_{TGS} sweeping could overwrite the effects of pulse 1 and 2 (see Fig 4.6 (b)) since the device could be switched “ON” and “OFF” effectively.

Thirdly, the individual effect of V_{TGS} -induced trapped charge could be extracted from the threshold voltage shift ($\Delta V_{\text{th}} = 2.2$ V), i.e., the voltage difference between point B and D. The trapped charges are $1.8 \times 10^4 |q|$ and the density of the trapped charges is equivalent to $2|q|$ per nm. However, it is noted that the effective length of the electric field of V_{TGS} is between 1.5 and 8.8 μm because of the unknown fringing field. That is the density of the trapped charges induced by V_{TGS} sweeping is a value between $2|q|$ and $7.6|q|$ per nm. Applying similar estimations to Fig 4.5 (a), we have $\Delta Q = 4.6 \times 10^4 |q|$ with $C_{\text{TGS}} \approx 0.4$ fF and $\Delta V_{\text{th}} = 20$ V. The equivalent density of the trapped charges is $\approx 5.2|q|$ per nm. Considering the average value ($2|q|$ and $7.6|q|$), the effective charge trapping effects induced by $|V_{\text{BGS}}| \approx 20$ V could be comparable $|V_{\text{TGS}}| \approx 4$ V.

In contrary to the above estimation, holes and electrons induced by pulses 3 and 4, respectively, have very strong effects on $I_{\text{DS}}-V_{\text{TGS}}$ characteristics, as shown in Fig 4.6 (c). Under the influences of the pre-trapped holes (rhombi) induced by pulse 3, the channel remains at “ON” state during V_{TGS} sweeping. However, in presence of pre-trapped electrons (circles) induced by pulse 4, the channel keeps at “OFF” state during V_{TGS} sweeping. Different from the pre-trapped charges induced by pulses 1 and 2, which shift the energy bands globally, the pre-trapped charges induced by pulses 3 and 4 only shift the energy bands locally (see inset to Fig 4.6 (c)) around the top-gate. Since pulse 3 is -

4.5 V with duration of 20 seconds, some pre-trapped holes could not be neutralized by trapped electrons up to $V_{TGS} = +4$ V during sweeping. These excess pre-trapped holes “permanently” shift the energy band downwards. Therefore, the channel could remain at “ON” states for both FS- and RS- V_{TGS} sweeping. In contrast, the energy bands were shifted upwards before sweeping (see dotted-lines in inset to Fig 4.6 (c)) owing to the pre-trapped electrons induced by pulse 4. Similarly, the excess pre-trapped electrons induced by pulse 4 increases energy barriers, which could not be overcome by electrons at $V_{TGS} = +4$ V, so that the channel keeps at “OFF” states during V_{TGS} sweeping.

Strikingly, the bistable states are not erasable by the V_{TGS} sweeping from -4 V to +4 V, but could be overwritten by 20-second voltage pulses of $V_{TGS} = \pm 4.5$ V. The reasons are twofold (1) the Si_3N_4 layer is rich of trapping centers, and (2) the duration of the voltage pulse is so long that I_{DS} saturated, implying that trapping/detrapping process reached equilibrium. In contrast, the duration of V_{TGS} sweeping (± 4 V) is much shorter than 20 seconds, resulting in incomplete charging of the trapping centers. This is consistent with Vijayaraghavan *et al.*'s findings, where the voltage pulse charging time (holding time) must exceed a critical value for the trapping/detrapping equilibrium.^{100,101}

The amount of trapped charges in the contact regions is closely related to the number of available trapping centers and electric field in the regions. Effective thickness of SB is found to be comparable to the global back-gate oxide thickness (500 nm in this work).¹⁰² Thus, the total length of the Schottky contact regions is estimated to be $\sim 2 \times 500$ nm. For simplicity, the trapped charges are considered to be uniformly distributed in the entire channel when voltage pulses are applied to the global back-gate in the above

discussions. So, the number of trapping centers in the contact regions could be 11% ($\approx 1/8.8$) of the total number of trapping centers in the whole channel. Actually, the electric fields at the contact regions are higher than elsewhere owing to the fringing effects at the source and drain electrodes,¹⁰³ and hence induce more trapped charges there. Therefore, the number of trapped charges in the contact regions could be significantly large when the voltage pulses are applied to the global back-gate. Moreover, charges trapped in the contact regions should have strong influences on the Schottky contacts.

The conclusions obtained from this work include:

- Influences of the distribution of trapped charges on CNT channel conductance of CNTFETs have been studied. Through applying voltage pulses to a global back-gate and a local top-gate, “globally” and “locally” distributed pre-trapped charges near the CNT-channel can be induced, respectively.
- For the back-gate voltage sweeping, the transfer curves are shifted due to trapped charges, which result in significant decreases in the field-effect mobility for both hole and electron transport. Local potential fluctuations caused by the trapped charges could be responsible for the observations.
- The locally pre-trapped holes and electrons keep the device at “ON” and “OFF” states for the top-gate sweeping, respectively, probably due to the global and local energy band bending.
- Therefore, the trapped charges at S/D contact regions and SWNT-body could both effectively influence the channel conductance through “Schottky barrier modulation” and “bulk switching”, respectively.

Chapter 5

Single-Electron/Hole Transport in CNTFETs

5.1 Introduction

Due to the scaling down of electronic devices, very few electrons/holes are involved in the transport process. Thus, single-electron transport properties are crucial because of the low dimensionality of the nanoscale devices. A simple circuit involving single-electron transport will be introduced in this section.

5.1.1 Single-electron transistors

Single electron/hole devices are very promising for future nanodevices with low-power consumption, fast speed and ultra-high density integration. Various material systems such as Si/SiO₂^{104,105,106} and GaAs^{107,108} have been used to fabricate SEDs/SHDs. Ref 109 is used as the main reference for the background of a SET. As shown in Fig 5.1, a single electron transistor (SET) consists of a quantum dot (QD) connected to source and drain through tunneling capacitors (C_1 and C_2) and to the gate through a common capacitor (C_g). The QD is so small that the energy levels of it become discrete. Any

potential change will cause an electrostatic change in the QD. Electrons can only flow between the QD and source (drain) electrode, other than the gate electrode. The total electrostatic energy of a dot with N electrons is $\frac{Q^2}{2C} = \frac{(Ne)^2}{2C}$, where C is the total capacitance of the QD. The total capacitance is the sum of the dot capacitance to source (C_1), drain (C_2) and gate (C_G), i.e., $C = C_1 + C_2 + C_G$. One regime that allows a detailed study of electron transport through a SET is the sequential tunneling limit. In a sequential tunneling process, electric current will flow when an electron can tunnel onto the QD and subsequently off from it to the other electrode. When a state is available between μ_S (the electrochemical potential of the source electrode, also called the Fermi level of the source electrode) and μ_D , the sequential tunneling process can occur via this state while changing the number of electrons on the QD between N and $N+1$. In this case, a large current will flow and the device is at “ON” state. On the other hand, a small current (by a direct tunneling through the device if possible) will flow if there is no available state situated in between μ_S and μ_D .

The total energy is $U(N+1) = \sum_{i=1}^N E_i + \frac{(Ne)^2}{2C}$, where E_i is the chemical potential of the dot with i electrons, i.e., the energy of the orbital of the dot that the i -th electron would occupy if there were no electron-electron interaction, when N electrons reside on the QD. The electrochemical potential, the minimum energy required for adding the N -th electron by definition, is $\mu_N = U(N) - U(N-1) = E_N + (N-1/2)\frac{e^2}{C}$. Therefore, if one more

electron is added onto the QD, we need $\mu_{N+1} = \mu_N + \frac{e^2}{C} + \Delta E$, where $\Delta E = E_{N+1} - E_N$ is the results of quantized excitation spectrum of the dot. A single electron that tunnels onto the QD has to overcome the charge addition energy $E_{\text{add}} = E_C + \Delta E$, where $E_C = \frac{e^2}{C}$ is the charging energy.

It is necessary for the lifetime (Δt) of an electron on the QD to be long enough so that the Coulomb blockade could be clearly observed. This requirement is equivalent to having a large enough tunnel capacitor (could be viewed as a capacitor connected to a resistor in parallel). The lifetime Δt could be estimated by using RC-time constant: $\Delta t = RC$, where R is the resistance between the QD and source or drain electrode and C is the total capacitance to the QD. To measure an energy difference of $\Delta E = E_C$, according Heisenberg's uncertainty relation, the lifetime must fulfill $\Delta E \cdot \Delta t = \frac{e^2}{C} \cdot RC > h$.

Thus, we get two conditions for clearly observing the Coulomb blockade: (1) $R > \frac{h}{e^2} \sim 25.8 \text{ k}\Omega$, and (2) $E_C + \Delta E \gg k_B T$.

Fig 5.1 (a) a schematic of a single electron transistor and its parameters. (b) the corresponding energy band diagram of the device.

Depending on whether ΔE is larger than $k_B T$, or not, a SET has different names. When $\Delta E < k_B T$, it is called a “classic dot” SET, while when $\Delta E > k_B T$, a “quantum dot” SET. In classical dot regime, a tunneling electron can access what is in effect a continuum of excited states of the dot, and the overall conductance can be described by the tunneling rate averaged over many electronic levels. On the contrary, in the quantum dot regime, each quantum states of the dot can be identified and specific tunneling rates are assigned to each quantum state. The various energies in a SET model are summarized in Fig 5.2.¹¹⁰ In a “classic dot” regime, some quantities become negligible compared to E_C , such as ΔE and γ (named intrinsic broadening).

Fig 5.2 The summary of various energies of a SET in an energy diagram.¹¹⁰

Next, we come to the DC characterization of a SET. As shown in Fig 5.3 (a), the channel current (I) could be represented using a 3-D plot by taking I , V_g and V_d as the z , y and x axis, respectively. I - V_d plot (Fig 5.3 (b)) could be extracted by cutting the surface along x -axis direction at a fixed V_g . Similarly, I - V_g plot (Fig 5.3 (c)) could be obtained by cutting the surface along y -axis at a fixed V_d . A clear current suppress region could be seen in I - V_d curve. This region is called the Coulomb blockade gap. The gate electrode influences the current by changing the position of electronic states in the QD. More precisely, $\Delta V_G = \frac{C}{|e|C_G} [E_N - E_{N-1} + \frac{e^2}{C}]$ could be obtained by considering the electrostatic energy contribution of the gate electrode through C_G . One can see that V_G could manipulate the position of E_N , hence the “ON” and “OFF” states of the SET

devices. ΔV_G , the oscillation period in Fig 5.3 (c), is usually called gate modulation period.

Fig 5.3 Characteristics of a SET (a) I - V_g - V_d diagram (b) I - V_d curves (Coulomb blockade gap) (c) I - V_g curves (Coulomb oscillations).

Another important characteristic of a SET is the stability diagram as shown in Fig 5.4.¹¹¹ The circuit shown in Fig 5.1 could be analyzed from the electrostatic energy change δE , when an electron tunnels onto the island.

$$\delta E = \frac{(Q_0 - (N+1)e)^2}{2C_\Sigma} - \frac{(Q_0 - Ne)^2}{2C_\Sigma}, \quad (5.1)$$

where N is an integer describing the number of electrons and $|Q_0| < e$ is the background charge of the island. In order to find out the relevant Legendre transformed free energy of the island, the work done by the voltage V_d and V_g must be subtracted. In case 1, an

electron tunnels onto the QD from C_1 . V_g supplies the charge $e \frac{C_g}{C_\Sigma}$ to capacitor C_g and

thus does the work $eV_g \frac{C_g}{C_\Sigma}$. Similarly, V_d does the work $eV_d \frac{C_2}{C_\Sigma}$ for capacitor C_2 . No

work is done for C_1 since source is common. Thus we have the change of the free energy

$$\begin{aligned} \Delta F_1^+ &= \frac{(Q_0 - (N+1)e)^2}{2C_\Sigma} - \frac{(Q_0 - Ne)^2}{2C_\Sigma} - eV_g \frac{C_g}{C_\Sigma} - eV_d \frac{C_2}{C_\Sigma}, \\ &= \frac{e}{C_\Sigma} \left(e(N + \frac{1}{2}) - Q_0 - C_g V_g - C_2 V_d \right), \end{aligned} \quad (5.2)$$

where the superscript “+” and subscript “1” mean tunneling onto the island from tunneling junction C_1 . For the electron to tunnel onto the QD, ΔF_1^+ has to be negative when the thermal path is neglected. Thus, a blockade for an electron to tunnel onto the QD over C_1 occurs when

$$e(N + \frac{1}{2}) > Q_0 + C_g V_g + C_2 V_d, \quad (5.3)$$

In case 2, the free energy change for an electron to tunnel onto the island over C_2 is

$$\begin{aligned} \Delta F_2^+ &= \frac{(Q_0 - (N+1)e)^2}{2C_\Sigma} - \frac{(Q_0 - Ne)^2}{2C_\Sigma} - eV_g \frac{C_g}{C_\Sigma} - eV_d \left(\frac{C_2}{C_\Sigma} - 1 \right) \\ &= \frac{e}{C_\Sigma} \left(e(N + \frac{1}{2}) - Q_0 - C_g V_g + V_d (C_1 + C_g) \right), \end{aligned} \quad (5.4)$$

In this case, an additional term eV_d accounts for the tunneling of the electron itself changing the charge on C_2 . Hence, we obtain the blockade condition for case 2 as

$$e(N + \frac{1}{2}) > Q_0 + C_g V_g - V_d(C_1 + C_g), \quad (5.5)$$

Similarly, the blockade conditions for case 3 (electron tunnels off the QD from C_1) and 4 (electron tunnels off the QD from C_2), respectively, are obtained as

$$e(N - \frac{1}{2}) < Q_0 + C_g V_g + V_d C_2, \quad (5.6)$$

and

$$e(N - \frac{1}{2}) < Q_0 + C_g V_g - V_d(C_1 + C_g), \quad (5.7)$$

Therefore, two inequalities are obtained from equation 5.3, 5.5, 5.6 and 5.7 as

$$e(N - \frac{1}{2}) < Q_0 + C_g V_g - V_d(C_1 + C_g) < e(N + \frac{1}{2}), \quad (5.8)$$

and

$$e(N - \frac{1}{2}) < Q_0 + C_g V_g + V_d C_2 < e(N + \frac{1}{2}), \quad (5.9)$$

Therefore, equations 5.8 and 5.9 together with a fixed N define a “diamond”-shaped blockade region. At the boundary of the blockade region, the slope of the boundary line is

obtained as $\frac{C_g}{C_1 + C_g}$ and $-\frac{C_g}{C_2}$ from equation 5.8 and 5.9, respectively. Therefore, the

capacitance ratio of C_1 , C_2 to C_g could be obtained from the slopes of the boundary line of a Coulomb “diamond”.

To obtain the gate modulation period ΔV_g , V_d is set to zero, then

$\Delta V_g = \frac{e(N + \frac{1}{2}) - e(N - \frac{1}{2})}{C_g} = \frac{e}{C_g}$ is obtained. Similarly, the height of the the “Coulomb

diamond” could also be obtained by solving

$$\Delta V = \frac{e(N + \frac{1}{2}) - C_g V_g - Q_0}{C_2}$$

and

$$\Delta V = \frac{e(N - \frac{1}{2}) - C_g V_g - Q_0}{C_1 + C_g}$$

Hence we obtain $\Delta V = \frac{e}{C_s}$, where $C_s = C_2 - C_1 - C_g$.

Fig 5.4 The stability diagram of a SET. The diamonds correspond to the Coulomb blockade regions. From the slopes and the diamond period, the capacitances C_1 , C_2 and C_g could be determined.

5.1.2 Single-electron transport in CNTFETs

As one can see, CNT is a nature candidate for SET fabrication because of its tiny volume. Various single-charge tunneling induced Coulomb blockade characteristics have been found in CNT-based devices. The Coulomb blockade characteristics in short (~ 200 nm) ropes of SWNT at 1.3 K were firstly reported by Bockrath *et al.*¹¹² Postma *et al.*¹¹³ demonstrated room-temperature Coulomb blockade characteristics using a small SWNT quantum dot (~ 20 nm). These Coulomb blockade characteristics, which were observed either at very low temperatures,^{112,114,115} or in short CNTs,^{113,116,117} are caused by CNT quantum dots in the channels.

Fig 5.5 (a) conductance G vs. gate voltage V_g at temperatures from 282 to 1.5 K for a metal-on-tube device. The device noise (conductance fluctuations in time) has been filtered from all traces except the one at 133 K where its amplitude is at a maximum. (b) Profile of a Coulomb blockade peak in another device between 16 and 1.7 K. (c) peak heights vs. T for the peak in (b). The solid curve illustrates $G \sim 1/T$. (d) peak area vs. T .¹¹⁸

Ref 118 is taken as the main reference for review of single-charge transport in CNTFETs. As shown in Fig 5.5 (a), the Coulomb oscillations are obtained below 50 K, implying that the tunneling resistance is significant and the SWNT-rope is segregated into a “quantum dot”. Fig 5.5 (b) shows a single peak from (a) after zoom in. The height of the peak, plotted in Fig 5.5 (c) approaches a $1/T$ dependence as T decreases, while the area under it, plotted in Fig 5.5 (d) approaches a constant. These observations imply that at the lowest T the device reaches the so-called “quantum dot” regime, defined by when the single-particle level spacing ΔE exceeds $k_B T$ and transport consequently occurs via one specific quantum transition for each Coulomb blockade peak. The observed peak sizes and spacings are randomly distributed, implying that there are multiple quantum dots involved in the transport. These quantum dots might be formed in parallel by several

conducting tubes within a rope, or in series within a single tube which is effectively broken up into segments by disorder.

Fig 5.6 shows the Coulomb diamond plot of a tube-under electrode device. At the peak points, the ground state energies for N and $N+1$ electron on the dot are degenerate. The charging energy is $U = eV_{\text{max}}$, in the constant-interaction model of the Coulomb blockade. The capacitance of a SWNT is estimated as $C \sim \epsilon_0 \epsilon_r L$, and hence,

$$U = \frac{e^2}{C} \sim \frac{e^2}{\epsilon_0 \epsilon_r L} \sim \frac{5 [\text{meV}]}{L [\mu\text{m}]}, \text{ where } \epsilon_r = 4 \text{ for a SiO}_2 \text{ (neglect the geometrical factors}$$

which depend on the exact configuration of electrodes and are difficult to estimate). $L \sim 0.6 \mu\text{m}$ is obtained for $U = 8 \text{ meV}$ in this case. The extra white lines outside the “diamonds” in Fig 5.6 (c) correspond to alignment of excited states. The level spacing with that expected for electrons with the appropriate dispersion confined to a 1-D box of

$$\text{length } L \text{ is estimated by } \Delta E = \frac{dE}{dk} \frac{\Delta k}{2} = \hbar v_F \frac{\pi}{2L} = \frac{1 [\text{meV}]}{L [\mu\text{m}]}.$$

Hence $L \sim 0.5 \mu\text{m}$ is estimated for a level spacing $\Delta E \sim 2 \text{ meV}$ in this case. Both estimations indicate that the segment of length of $L \sim 0.5 \mu\text{m}$, which is approximately the lithographically defined contact separation for the device. This finding implies that the evaporated metal strongly perturbs the tubes underneath it and the electron states are extended along the molecule lying over the contacts.

Fig 5.6 (a) G - V_g for a device at 4.2 K showing a regular series of Coulomb blockade peaks. (b) I - V characteristics taken at the center of a peak (V_{g1}) and in between peaks (V_{g2}). (c) Grey scale (bias spectroscopy) plot of dI/dV vs. V_g and V at 4.2 K in the same range of V_g (lighter = more positive).

Moreover, the conversion factor from gate voltage to the electrostatic dot potential could be estimated by $\alpha = \frac{U}{e\Delta V_g} \sim 0.16$, where $\Delta V_g \sim 50$ mV is the gate modulation period obtained from Fig 5.6 (c).

5.2 Carbon-nanotube-based single-electron transistors

As mentioned in the previous section, single-charge charging a small “island” is not observable unless the condition that the Coulomb charging energy (e^2/C_Σ) exceeds thermal energy ($k_B T$, where C_Σ is the total capacitance of the “island”) is satisfied. Hence temperature and dimension of the “island” are two important factors for observing the

Coulomb blockade characteristics. In this work, we use long SWNT bundles as channels in CNTFETs to demonstrate significant Coulomb blockade characteristics below 70 K.

The Raman spectrum of our SWNTs on Si/SiO₂ substrate is shown in Fig 5.7 (a). From the relationship between the radial breathing mode (RBM) frequency and average diameter, i.e., $\omega_{\text{RBM}} \approx 248/D$,¹¹⁹ D is estimated to be around 1.4 nm. The large ratio of G⁺ peak (high-frequency component at 1592 cm⁻¹) to G⁻ peak (low-frequency component at 1565 cm⁻¹) suggests that the SWNTs are dominated by semiconducting ones.^{79,120} The average diameter of the SWNTs is reconfirmed using TEM as shown in Fig 5.7 (b) (SWNTs in deionized water), from which one can see that the diameters of the SWNTs are very uniform. The length of the SWNTs, obtained from the AFM measurement, is up to several micrometers. The SWNTs are dispersed in deionized water with 1% wt Triton X 100. After ultrasonic-agitation using a tip-sonicator (MISONIX sonicator 3000) at a power of 480 watt/liter for 2 mins, the suspension is centrifuged (SIGMA sartorius 2-16) at 6461 g for 2 hrs. Then, the up 10% supernatant was carefully decanted. The average diameter of the SWNT bundles in the well-prepared suspension is less than 10 nm. The suspension is then ultrasonically agitated (a SONICOR S-402C ultrasonic cleaner with 1610 W dissipated in a volume of 39 liters) for more than 80 hrs. After this process, the SWNTs are found to be severely shortened (see short SWNTs in Fig 5.8). Next, some well-dispersed SWNT suspensions are added to the shortened-SWNT suspension and agitated for another 2 hrs. Finally, the corresponding suspensions are dropped onto Au (40 nm) /Ti (10 nm) electrodes pre-structured on heavily boron-doped <100> silicon substrates (resistivity is about 0.01 Ω.cm) capped by a thermally grown SiO₂ layer (200

nm). The SWNTs are placed across the electrodes using ACDEP technique.^{75,82} Device A is fabricated using the mixed suspension containing both short and long SWNTs. For comparison, Device B is fabricated using long-SWNT suspension without shortened SWNTs.

Fig 5.7 (a) Raman spectrum for our SWNTs. (b) TEM images for the SWNTs dispersed in deionized water. $D \approx 1$ nm represents the diameter of a single SWNT. The white scale bar is 20 nm.

Fig 5.8 (a) The AFM image of Device A. The white scale bar is 500 nm. (b) Profile analysis for (a) using Digital Instrument Nanoscope III software. (c) The I_{ds} - V_{gs} curves in atmosphere environment at $V_{ds} = 250$ mV.

An electrical breakdown process⁶⁶ is applied to burn off the metallic SWNTs in the channel if the current on/off ratio¹²¹ of the as-prepared device is less than 10^3 . Otherwise, an electrical heating process¹²² is applied to improve the contacts. The electrical heating process is similar to breakdown process, but a smaller sweeping range of source-drain voltage (V_{ds}) is applied. The contact resistance is greatly reduced after this process. A tapping-mode Digital Instrument Nanoscope is used to characterize the topography of the devices. The AFM image of Device A (Fig 5.8 (a)) shows that a long SWNT bundle bridges the electrodes and several short SWNTs are only attached to the source/drain electrodes, which are separated by 1-2 μm . As shown in Fig 5.8 (b), the profile of the black line shows that the thicknesses of the long and short SWNT bundles are around 2 and 7 nm, respectively. The TEM image of SWNTs with Triton X 100 as surfactant is shown in Fig 5.9. In comparison with Fig 5.7 (b), the SWNTs become blurred. In addition, one can see that the thickness is not uniform throughout the SWNTs in Fig 5.8 (b). Both observations suggest that the SWNT bundles are coated with a thin layer of Triton X 100.

Fig 5.9 TEM image of a SWNT bundle coated by a thin layer of Triton X 100. Dashed circle delineate a blurred SWNT bundle. The white scale bar is 100 nm.

Fig 5.10 Bias-dependent Coulomb oscillations at 15 K with different V_{ds} for (a) SHC and (b) SEC condition, respectively.

The $I_{\text{ON}}/I_{\text{OFF}}$ ratio, which is about 10^4 at $V_{\text{ds}} = 250$ mV for Device A (Fig 5.8 (c)), implies that the channel is dominated by semiconducting SWNTs. In addition, this device has significant ambipolar⁸⁷ and hysteresis⁵⁵ characteristics in the source-drain current (I_{ds}) versus gate voltage (V_{gs}) curves in atmosphere environment. Interestingly, it shows significant ambipolar Coulomb oscillations^{123,124,125} at low V_{ds} and low temperatures. The bias-voltage-dependent ambipolar Coulomb oscillations at 15 K and 0.03 mbar are shown in Fig 5.10 (a), which contains three oscillation peaks, and Fig 5.10 (b), which contains four oscillation peaks, for single-hole-charging (SHC) and single-electron-charging (SEC) condition, respectively. The oscillating current increases with increasing V_{ds} from 10 to 100 mV.

The Coulomb oscillations also show strong temperature dependence as shown in Fig 5.11 (a) and (b) for SHC and SEC condition, respectively. The oscillation peaks disappear gradually as the temperature is increased up to 70 K for SHC condition. In contrast, the current becomes unstable and the oscillations are distorted for SEC condition. The current contour plots¹²⁶ in $V_{\text{gs}}-V_{\text{ds}}$ plane are shown in Fig 5.12 (a) and (b), both of which contain three “diamond”-shaped contour line free regions, where $I_{\text{ds}} < 1$ pA, for SHC and SEC condition, respectively. The levels of current are color-coded. It is noted that the Coulomb “diamonds” are distorted.

The Coulomb oscillations could be explained by the Coulomb blockade model.¹²⁷ To our knowledge, there are two possibilities to observe Coulomb blockade effects in CNTs. First, CNTFETs work as conventional single-electron transistors,¹²⁶ in which the CNT channels act as charge “islands” and the two contacts between channel and

electrodes serve as tunneling barriers. The coupling of the channel to electrodes is suggested to change as a function of gate voltage so that current oscillation occurs.^{128,129} Depending on the quality of the SWNTs, it is possible to observe Coulomb oscillations in a long SWNT channel theoretically. However, it is unlikely to be the reason in our case since we did not find similar oscillations in common CNTFETs such as Device B that only consists of a long SWNT bundle without any short SWNTs located around the contacts (see inset of Fig 5.13 (b) for AFM image). As shown in Fig 5.13 (a), its transfer curve in atmosphere environment is very similar to that of Device A in terms of ambipolar characteristic, hysteretic characteristic and subthreshold slope. However, it is noted that the transfer curve of Device A in forward sweeping (from -7.5 V to +7.5 V) contains several peaks, while that of Device B is very smooth. The I_{ds} - V_{gs} curves at 15 K with small V_{ds} (5 mV and 10 mV) for Device B are shown in Fig 5.13 (b). In contrast to Device A, no regular oscillation is observed.

Second, the Coulomb blockade effect in SWNTs could be caused by quantum dots in series, while the dots may be induced by disorder of the electronic states.¹³⁰ Our observations may not result from electronic states disorder effects in the SWNT channel, because (1) the Coulomb oscillations only occur in the threshold region, and (2) the channel of Device A consists of a long bundle instead of a single SWNT. With a SWNT channel (1.5 μm in length and 1.4 nm in diameter) similar to those used in our CNTFETs, Martel *et al.*¹⁸ did not observe regular oscillations even at 4 K. With the same process as that of Device A, we fabricated the other four devices with mixture of long and short SWNTs and all of them show regular ambipolar oscillations at 15 K.

Furthermore, we exclude the effect of trapped charges here. If the charging effect is due to the random trapping centers in the oxide, the oscillation should not be periodic and repeatable. As observed in Chapter 3, the hysteresis saturate when $T < 100$ K. Therefore, we exclude the charge hopping into the random trapping centers. We noted that the hysteresis is negligible for small V_{gs} sweeping range (< 2 V in Figure 5.11) at low temperature.

We interpret the observations in the frame of single electron memory model.¹³¹ When the SWNTs are manipulated using ACDEP technique, both long and shortened SWNTs are weakly coupled¹³² to the Au electrodes through a thin layer of Triton X 100, which could act as an extra tunnel barrier.¹³³ We suggest that the electrical heating process could break through the thin Triton X 100 layer and improve the electrical contacts between the long SWNT-channel and electrodes. This explains the current increments after the electrical heating process. However, the contacts between the short SWNTs and electrodes remain unchanged since no current flows through the short SWNTs. The short SWNTs, which are located so near to the long-tube/Au contact that the charges stored in them could influence the contact-tunneling barrier, may serve as memory nodes.¹³⁴ In contrast, the long SWNT bundle acts as an electrometer.¹³⁵

Fig 5.11 Temperature-dependent Coulomb oscillations for (a) SHC ($V_{ds} = 40$ mV), and (b) SEC ($V_{ds} = 60$ mV) condition, respectively. The solid (gray) lines with label A to G indicate the current peaks and valleys. The curves in (b) for 25 K, 35 K and 60 K are offset by 10 pA, 20 pA and 30 pA, respectively, for clarity.

CNTFETs are well accepted to work as Schottky barrier transistors.⁵³ Therefore, the energy barriers at the source and drain contacts predominantly control the CNT-channel conductance. Once a single or a quantum of charge tunnels into the memory node, its local electrostatic potential³² will be superimposed with the global electrostatic potential induced by V_{gs} . At the threshold region, where the channel current is very small, the effects of the local and global electrostatic potentials on the tunneling current could be comparable. Since positive (negative) gate voltage could only attract electrons (holes), the local electrostatic potential must have an opposite effect to the global electrostatic potential. Thus the tunneling barrier thickness and height would increase due to the local electrostatic potential, and consequently the channel conductance would decrease. Because the short SWNT is ultra small, the Coulomb blockade must occur once a charge is stored in it. Thus the variation of the local electrostatic potential, hence the variation of total electrostatic potential, could be discrete due to the quantized charges tunneling into the memory node. The discrete variation in the total electrostatic potential leads to the channel current oscillations. The oscillations vanish when V_{gs} is so large that the effect of local electrical potential induced by the memory nodes is negligible compared to that induced by the global electrostatic potential. It is noted that the position and size of the memory nodes are not well controlled in the device, there are probably more than one memory node participating the charging process. This could explain the distortion of our Coulomb diamonds. Furthermore, the electrostatic potential interplay between the memory node and electrometer may be another reason for the Coulomb “diamond” distortion.

The temperature-dependent I_{ds} shown in Fig 5.11 are consistent with thermally activated transport, with activation energy E_a that varies with the gate voltage ($I(V_{gs}, T) \propto e^{-E_a(V_{gs})/kT}$, where k is Boltzmann's constant). E_a versus V_{gs} shown in Fig 5.14 (a) consists of a linear region ($-2.7 \text{ V} < V_{gs} < -1.8 \text{ V}$) and a nonlinear region ($-3.8 \text{ V} < V_{gs} < -2.7 \text{ V}$). In the linear region, the memory nodes have not been charged. The thermal activated transport with $E_a = |E_F - E_v|$, where E_v is the edge of the valence band and E_F is the Fermi level, dominates the current. V_{gs} controls the position of E_v solely, and the activation energy varies linearly with V_{gs} .¹³³ E_a is expected to reach a maximum of half the energy bandgap if E_F is situated at the midgap. Since the current is suppressed below the measurement sensitivity of our semiconductor parameter analyzer (HP 4156B with noise level at $I \sim 10^{-13} \text{ A}$), we cannot obtain exact E_a near $V_{gs} = 0 \text{ V}$. An extrapolation of the linear fit curve yield $E_{a|V_{gs}=0} \approx 250 \text{ meV}$, which is slightly smaller than 300 meV , half of the estimated energy bandgap for our SWNTs. The difference could be caused the oxygen adsorption,⁴ which may not be eliminated at 0.03 mbar in our experiments.

Fig 5.12 Contour plots of I_{ds} in V_{ds} - V_{gs} plane for (a) SHC and (b) SEC condition, respectively. The Coulomb blockade region designates $I_{ds} < 1$ pA. The guidelines are inserted to delineate “diamond” shape. The color bars indicate different current levels.

In the nonlinear region, the quantum holes are supposed to tunnel into the memory nodes. Their effects could influence the conductance of the electrometer as discussed above. E_a starts to oscillate with its maximum (minimum) corresponding to the minimum (maximum) in I_{ds} . The peaks (valleys) labeled with A to G in Fig 5.14 (a) are corresponding to the current valleys (peaks) labeled by the solid lines with A to G in Fig 5.11 (a). This is understandable in the sense that when holes tunnel into the memory nodes, E_v bends away from E_F resulting in an increase in E_a , but a decrease in the channel conductance. The electron conduction current is unstable and the current peaks shift slightly from each other as shown in Fig 5.11 (b). Hence we cannot get well-defined E_a versus V_{gs} for positive V_{gs} .

In addition, we could estimate the energy barrier variation caused by holes charging the memory node. As shown in Fig 5.14 (a), the energy barrier height for hole to overcome initially is 20.21 meV at $V_{gs} = -2.448$ V. As V_{gs} is increased to -2.704 V, the barrier is decreased to 0.63 meV. However, it is increased to 2.01 meV at $V_{gs} = -2.872$ V probably due to the first hole charging the memory node. Next, it is decreased to 0.79 meV at $V_{gs} = -2.936$ V. Then, the second-hole charging is supposed to increase the barrier to 3.08 meV at $V_{gs} = -3.064$ V, and so on. One can see that the energy barrier variations due to the first and second quantum-hole-charging are about 1.38 and 2.29 meV, respectively.

Fig 5.13 (a) I_{ds} versus V_{gs} sweeping between -7.5 V and $+7.5\text{ V}$ in atmosphere environment and $V_{ds} = 250\text{ mV}$ for Device B. (b) I_{ds} - V_{gs} curves for Device B at 15 K . Inset: The AFM image of the device. The white scale bar is 500 nm .

Fig 5.14 (a) Thermal activation energy E_a as a function of V_{gs} for SHC condition. Inset: Arrhenius plot used to determine the activation energy at $V_{gs} = -3.38$ V. The labels A to G indicate the corresponding current peaks and valleys in Fig 5.11 (a). (b) Proposed circuit model for Device A. The memory node is the shortened-SWNT and electrometer represents the long SWNT channel.

Based on the above interpretations, we may set up a circuit model for Device A as shown in Fig 5.14 (b). C_{gd} , C_{ds} , C_{dc} and C_{gc} denote the equivalent capacitance between the gate electrode and memory node, the memory node and the source/drain electrode, the memory node and the electrometer, and the gate electrode and the electrometer, respectively. C_{gc} could be estimated using the geometric configuration of the gate as

$$C_{gc} \approx \frac{2\pi L \epsilon_{\text{SiO}_2} \epsilon_0}{\ln\left[\frac{2(t_{\text{ox}} + r)}{r}\right]},^{91}$$

where L is the length of the SWNT channel, ϵ_{SiO_2} the relative

dielectric constant of SiO_2 , ϵ_0 the permittivity in vacuum, t_{ox} the thickness of the gate oxide and r the radius of channel. With $L = 1500$ nm, $\epsilon_{\text{SiO}_2} = 3.9$, $t_{\text{ox}} = 200$ nm and $r = 1$ nm, $C_{gc} \approx 54$ aF. Assuming that the observed channel current relates to the memory node charging current by a constant factor, we may estimate the capacitances related to the memory node based on the theory for single-electron charging in an “island”.⁸⁸ As the Coulomb “diamonds” in Fig 5.12 (a) are better defined in shape compared to those in Fig 5.12 (b), we choose one of them for estimation. The gate modulation period is about 0.3 V, which is approximately e/C_{gd} , so $C_{gd} \approx 0.5$ aF. It is noted that C_{gc} is significantly deviated from C_{gd} . This could be due to constraints of the formula used, in which the CNTFET is modeled as a wire at a distance $t_{\text{ox}} + r$ over the back-gate plane.⁹¹ The slope of the left side boundary of the diamond is determined by C_{gd}/C_{ds} and that of the right side boundary by C_{gd}/C_{dc} . From the rhombus-shaped guidelines, we estimate $C_{gd}/C_{ds} \approx 0.2$ and $C_{gd}/C_{dc} \approx 0.4$, yields $C_{ds} \approx 2.7$ aF and $C_{dc} \approx 1.3$ aF. We give more weight to C_{ds} since the memory node should have larger overlap area on the electrode than that on the CNTFET channel. Assuming that the self-capacitance of the memory node is implicitly included in

C_{ds} and C_{dc} , the total memory node capacitance is therefore obtained as $C_{\Sigma} = C_{gd} + C_{ds} + C_{dc} = 4.5$ aF. The inequality $k_B T \ll E_c = \frac{e^2}{C_{\Sigma}}$ must be fulfilled in order to observe single-charge-charging phenomena. This estimation agrees reasonably with our observation of the Coulomb oscillations at $T < 70$ K. However, our model is very simple and rough, further study is necessary.

Both single electron and hole charging phenomena are observed in Device A that contains a long SWNT bundle bridging the source and drain electrodes and several short SWNTs attached to the electrodes. This type of devices is different from the conventional single electron devices¹²⁶ in the following two aspects: (1) the positions of the memory nodes are at the contacts instead of at the center of the electrometer channel, and (2) the reservoir of the charges is the source/drain instead of electrometer channel.

As a summary, this work provided following information:

- SWNT itself can be used as charge trapping centers in CNTFET. This implies that we can introduce stable trapping centers in CNTFET by controlled distribution of SWNT itself around the channel.
- By produced even shorter and thinner SWNT bundles ($L < 10$ nm and $D = 1.4$ nm), we may produce SED/SHD working at much higher temperatures.
- By using other coating method, we may improve the tunneling barrier between SWNTs. This may enable the devices to work as single electron/hole memories.

Chapter 6

Single-Electron Transport through Short-

Channel CNTFETs with Asymmetric Barriers

6.1 Introduction to Schottky diode effect in CNTFETs

Diode-like effects have been observed in CNTFETs with various fabrication and characterization methods.^{136,137,138,139,140,141} The methods are summarized as following: (1) creating a p-n junction by chemical doping of a CNT,¹³⁶ (2) making asymmetric barriers by local potential,¹³⁷ (3) patterning a pair of cross tubes consists of a metallic tube and a semiconducting tube,¹³⁸ (4) employing metals with different work functions as the drain and source electrodes,^{139,140} and (5) modifying the contacts by chemical molecules to achieve asymmetric contacts.¹⁴¹

The diode characteristics caused by work function difference of the source and drain electrodes¹⁴⁰ will be discussed in details since it will be employed in the following experiments. As shown in Fig 6.1 (a), the device is a common SB-CNTFET with Pd

(work function, $\Phi_{\text{Pd}} = 5.12$ eV) and Al ($\Phi_{\text{Al}} = 3.9 \sim 4.2$ eV) as the drain and source electrode, respectively. The I_d - V_{ds} curves at different V_{gs} are shown in Fig 6.1 (b) with linear scale and Fig 6.1 (c) with log scale. One can see that the I_d - V_{ds} curves are asymmetric and the asymmetry is determined by the direction of bias voltage. I_d is much larger under a positive V_{ds} than that under a negative V_{ds} .

Fig 6.1 (a) schematic of the CNT Schottky diode and direction dependent CNTFET using Pd and Al contacts. The diode characteristics are shown in linear (b) and logarithmic (c) scales.¹⁴⁰

Hence, the device could be viewed as a Schottky diode. One of the important parameters of a diode is the current rectification ratio (CRR), which is defined as the

relative change in I_{DS} when V_{DS} is reversed,¹⁴² i.e., $\frac{I_{\text{DS}}(|V_{\text{DS}}|)}{I_{\text{DS}}(|-V_{\text{DS}}|)}$. One can see from Fig 6.1

(c) that the CRR value could be as high as 300 at $V_{\text{gs}} = +10$ V. Moreover, the CRR is V_{gs} -dependent and becomes larger when V_{gs} is increased positively, i.e., the device is approaching “OFF” state. The working principle of this type of device is shown in Fig 6.2. Al/CNT ($\Phi_{\text{SWNT}} \sim 4.8$ eV) contact forms a higher Schottky barrier for holes than Pd/CNT contact because of $\Phi_{\text{Al}} < \Phi_{\text{Pd}}$. When the device is forward biased (Pd is positive),

holes feel the Schottky barriers at Pd side, which is estimated to be ~ 0.1 eV. In contrast, holes feel Schottky barrier of ~ 0.9 eV at Al side, theoretically, when the device is reverse biased. As a result, the hole current is much larger under forward bias. However, it is noted that the CRR is much smaller than the theoretical values. The reason remains an open question and will be discussed in details in the following experiments.

Fig 6.2 Band diagrams for the case of the CNT under forward (a) and reverse bias (b). The conduction mechanism is dominated by the barrier to holes at the Al/CNT contact. Under forward bias, holes can overcome the Al/CNT barrier. In contrast, under reverse bias, holes are blocked by the Al/CNT barrier which can be controlled by the applied gate voltages.

6.2 Unique characteristics of asymmetric contact short-channel carbon-nanotube field-effect transistors

We have discussed several types of SET devices in Chapter 5. However, all of the reported investigations have focused on SETs with similar capacitive couplings to the

drain (D) and source (S) electrodes, i.e., symmetric D-S contacts. In this work, we report SWNT-based FETs with asymmetric drain and source electrodes. A self-alignment technique (shadow electron-beam evaporation) was employed to define short channel lengths (< 100 nm). The devices exhibit remarkable current rectification characteristics at room temperature. In addition, the asymmetric barriers result in unequal conductance oscillations under positive and negative D-S bias at low temperatures.

A schematic structure of the short-channel CNTFETs is shown in Fig 6.3 (a). Firstly, interdigital electrodes (Au (90 nm)/Ti (10 nm)) were patterned on a heavily doped Si substrate capped by a layer of 500-nm-thick thermally grown SiO₂. Next, SWNTs (see Chapter 5 for the material properties) in solution of deionized water with 1% wt Triton X 100 were bridged between a pair of electrodes using AC DEP technique. Then, an AZ photoresist 5214 “window” ($\sim 20 \times 30 \mu\text{m}^2$) within the electrode region was opened by standard lithography technique. Afterward, a 50-nm Al layer was deposited using electron-beam evaporation at an angle, θ , with respect to the sample surface,¹⁴³ so that a ~ 90 -nm gap was created, as shown by the AFM image in Fig 6.3 (b). The left portion of the SWNT-channel is sandwiched between SiO₂ (bottom) and Al layer (top), and hence the electrical properties of the contact are determined by Al/SWNT coupling. In contrast, the right portion of the SWNT attaches to the sidewall of Au electrode. Thus the contact properties is dominated by Au/SWNT coupling.

Fig 6.3 (a) A schematic diagram of the device structure. (b) An AFM image of a ~ 90 -nm-channel CNTFET.

The results reported here were obtained using Al (low work function, Φ_{Al})¹³⁹ as the drain and Au (high work function, Φ_{Au}) as the source electrode. At 25 K, strong oscillations in the SWNT-channel current (I_{DS}) with positive D-S bias (V_{DS}) are observed as shown in Fig 6.4 (a). The temperature-dependent transfer curves at $V_{\text{DS}} = +30$ mV are shown in the inset. The linear scale plot of the oscillations with both positive and negative V_{DS} are presented in Fig 6.4 (b), where the curves having equal $|V_{\text{DS}}|$ are coded with the same color. Owing to a large $I_{\text{on}}/I_{\text{off}}$ ratio ($\sim 10^7$), some oscillation peaks could not be reflected in the linear plot, and we thus zoom in on the peak at $V_{\text{GS}} \sim -10$ V. These observations could be interpreted by single-electron tunneling with the Coulomb blockade effect in the classic regime (see inset of Fig 6.4 (b) for the equivalent SET circuit), in which the barriers at the metal/SWNT contacts⁵³ serve as the tunneling capacitors (C_1 and C_2). Due to its small volume, the SWNT-channel could be viewed as an “island” with discrete energy levels (E_i). With increasing temperature, the thermal energy ($k_{\text{B}}T$) becomes comparable to or even larger than the Coulomb charging energy (e^2/C_{Σ} , where C_{Σ} is the total capacitance of the “island”). As a result, the oscillation peaks broaden and fade out when T is increased beyond 100 K as shown in the inset of Fig 6.4 (a).

Fig 6.4 (a) I_{DS} - V_{GS} curves (log scale) at $T = 25$ K with V_{DS} ranging from $+20$ to $+100$ mV in step of 20 mV. Inset: I_{DS} - V_{GS} curves (log scale) at $V_{DS} = +30$ mV with temperature ranging from 25 up to 300 K. (b) I_{DS} - V_{GS} curves (linear scale) at $T = 25$ K for $V_{GS} = -20$ to 0 V with V_{DS} ranging from -100 to $+100$ mV in step of 20 mV (I_{DS} with equal $|V_{DS}|$ are plotted in the same color.). Inset: a schematic conduction band alignment and equivalent SET circuit. An extra barrier besides SB are inserted between metal and SWNT.

The observed Coulomb oscillations possess three notable characteristics. First of all, the peak-to-valley ratio can be as high as one order of magnitude and the peaks are situated at different I_{DS} levels. In other words, I_{DS} could be viewed as the Coulomb oscillations superimposed upon the transfer curve of an n-type transistor. Thus, the roles of V_{GS} could be twofold here: (1) to manipulate the position of discrete energy level, E_i , and (2) to control the carrier density in the SWNT-channel (through contact barrier or/and SWNT bulk modulation).^{35,53} Secondly, the oscillation peaks on different curves gradually shift toward negative V_{GS} . The peak shift could be caused by charge-trapping due to the electric field induced by V_{GS} .^{55,70} Lastly, the amplitude of the current oscillations under negative V_{DS} are larger than that under positive V_{DS} as shown in Fig 6.4 (b), where the dashed line indicates $V_{DS} = 0$. Thus, the “diamond”-shaped region confined by a pair of oscillation peaks (with equal $|V_{DS}|$) shift downwards as delineated by the dashed arrow. We attribute the asymmetric current oscillations to the difference between the Al/SWNT and Au/SWNT contacts ($C_1 < C_2$), which will be discussed later.

As pointed out in Ref 95, tunneling and thermionic emission compete to influence the channel conductance. The effective Schottky barrier (SB) height can be estimated from the thermionic emission current (above 100 K as shown in the inset of Fig 6.5 (a)).⁹⁵ From E_a - V_{GS} plot shown in Fig 6.5 (a), one may see that E_a increases drastically when $V_{GS} < -10$ V, implying that electrons are mainly thermionically injected into the channel when $V_{GS} < -10$ V, while mostly tunnel into the channel when $V_{GS} > -10$ V. It is noted that the extracted effective SB heights are very small. Chen *et al.* reported a similar observation and attributed it to the p-type chemical doping due to air.¹⁴⁴ However, their

explanations do not account for our case since our device shows strong n-type characteristics. We suggest the small E_a to be caused by imperfect contacts as CNTFETs fabricated with ac dielectrophoresis technique typically have weak contact coupling. Thus, an extra tunneling barrier (cyan regions in the inset of Fig 6.4 (b)) besides SB could be formed at the metal/SWNT interface, so that the effective SB is modulated in width and height.

Interestingly, one may see that E_a under positive V_{DS} (right branches) are larger than those under the corresponding negative V_{DS} (left branches), by a factor of at least 2, for all V_{GS} (see Fig 6.5 (b)). Since Al and Au are connected as the D and S electrodes, respectively, electrons feel the barrier at the Al/SWNT (Au/SWNT) contact when V_{DS} is negative (positive). Thus, the SB height is expected to be larger when V_{DS} is positive because Au ($\Phi_{Au} \sim 5.2$ eV for bare Au surface)¹⁴¹ is supposed to form a higher SB for electrons than Al/SWNT contact.¹³⁹ The consistency between our expectation and the experimental results indicates that Al and Au do form asymmetric barriers with SWNTs (We have fabricated 18 devices, of which 12 show significantly asymmetric contacts (strong current rectification characteristics)). Theoretically, electrons see a negative SB at SWNT/Al contact since the work function of Al is above the conduction band edge of SWNTs (~ 4.5 eV). However, low barriers are observed at the SWNT/Al contacts as shown in Fig 6.5 (b). We attribute the finite E_a to the extra barriers caused by imperfect contacts discussed previously.

Fig 6.5 (a) E_a versus V_{GS} at $V_{DS} = +30, +150$ and $+1000$ mV, respectively. Error bars are introduced due to linear fit of the Arrhenius plot for E_a estimation. Inset: $\log I_{DS}$ versus $1000/T$ plot at $V_{DS} = +150$ mV for $V_{GS} = -20, -10, 0, +10$ and $+20$ V, respectively. (b) E_a versus V_{DS} at $V_{GS} = -10, 0, +10$ and $+20$ V (from top to bottom), respectively. Inset: E_a versus V_{DS} at $V_{GS} = -20$ V (The large error bars are caused by the poor signal-to-noise ratio since the device is at “OFF” state with $V_{GS} = -20$ V.).

Fig 6.6 (a) I_{DS} - V_{GS} curves at $V_{DS} = \pm 20$ mV with V_{GS} ranging from -10 to -2 V. I_{tuS1} and I_{tuS2} mark the oscillation height (single-electron tunneling current) for positive and negative V_{DS} , respectively, and I_{thS2} labels the residual current (thermionic emission current). (b) Schematic band diagrams for (i) positive and (ii) negative V_{DS} . I_{th} and I_{tu} indicate thermionic emission and tunneling current components, respectively. Six energy levels (E_1 to E_6) are considered. Red color represents E_i involved in single-electron tunneling, gray color delineates E_i that are not involved in carrier transport, and green color indicates themionic emission current components (current paths above E_1 could also be involved). The cyan regions represent the extra barriers besides SB.

The transfer curve between $V_{GS} = -10$ and -2 V at $V_{DS} = \pm 20$ mV is selected from Fig 6.4 (b) and reported in Fig 6.6 (a). Single-electron tunneling (I_{tu}) and thermionic emission (I_{th}) are suggested to dominate electron transport in the devices at low temperatures. The energy band diagrams shown in Fig 6.6 (b) are proposed to illustrate the electron transport mechanisms. For simplicity, the discrete energy level E_i is assumed to be stationary with respect to E_{fAu} (common) when V_{GS} is fixed. For positive V_{DS} (case i), energy level E_4 and E_5 are situated in between E_{fAl} and E_{fAu} . Thus, electrons from S side (I_{tuS1}) could tunnel through E_4 or E_5 , to the D barrier (I_{tuD1}) as illustrated in Fig 6.6 (b) (i). Since the thermionic emission current (I_{thS1} in Fig 6.6 (a)) is negligible, $I_{DS} \sim I_{tuS1}$ could be obtained. In contrast, when V_{DS} is negatively biased (case ii), energy level E_2 and E_3 are situated in between E_{fAl} and E_{fAu} , so that electrons could tunnel through the D barrier (I_{tuD2}), E_2 or E_3 , to the S barrier (I_{tuS2}) in sequence. Moreover, since the barrier at D side (Al/SWNT) is small, some carriers could thermionically inject (I_{thD2} in Fig 6.6 (a)) over the S barrier. Thus, $I_{DS} \sim (I_{tuD2} + I_{thD2})$ is obtained in this case. One can see that the single-electron tunneling current in both cases are comparable ($I_{tuS1} \sim I_{tuD2}$ in Fig 6.6 (a)), and thermionic emission current for negative V_{DS} is much more significant than that for positive V_{DS} ($I_{thD2} \gg I_{thS1}$ in Fig 6.6 (a)). In other words, the unequal current amplitude is mainly caused by difference between thermionic emission current over the contact barriers, instead of single-electron tunneling current.

Fig 6.7 I_{DS} - V_{DS} curves at different V_{GS} (from -20 to +20 V in step of 10 V) in atmosphere environment and room temperature. Inset: current rectification ratio.

In atmosphere environment, striking current rectification characteristics^{140,141} are observed as shown in Fig 6.7 (a). The asymmetry of the I_{DS} - V_{DS} curves changes accordingly after swapping D with S (see Fig 6.7 (b)). As discussed above, I_{DS} is dominated by thermionic emission at $V_{GS} < -10$ V and room temperature. From the thermionic emission model, $CRR = \frac{I_{DS_{FB}}}{I_{DS_{RB}}} \sim \exp(-\frac{(E_{a_{FB}} - E_{a_{RB}})}{k_B T})$, where the subscript “FB” and “RB” stand for forward and reverse D-S bias, respectively. At 300 K and $V_{GS} = -10$ V, a maximum CRR is ~ 7000 at $V_{DS} \sim 0.5$ V (see green triangles in Fig 6.7 (a)), and hence the barrier height difference, $E_{a_{FB}} - E_{a_{RB}} \sim -k_B T \ln(\frac{I_{DS_{FB}}}{I_{DS_{RB}}}) \sim -230$ meV. For thermionic emission current, the barrier height is approximately $E_a = q(\phi_{\text{metal}} - \chi_{\text{SWNT}})$ for electrons under flat-band condition ($V_{GS} \sim -10$ V), where χ_{SWNT} is the electron affinity of SWNT. Thus, we have $E_{a_{FB}} - E_{a_{RB}} = q(\phi_{\text{Al}} - \phi_{\text{Au}})$. The estimated barrier height difference of 230 meV is much smaller than 900 meV, the theoretical work function difference between Au and Al. The underestimation may be caused by imperfect contacts as discussed previously. In spite of this reason, the SB theory for bulk materials may not fully explain the coupling between metal and one-dimensional SWNT because of the environmental influences,¹⁴⁴ dipole effects,¹⁴⁵ etc.

We attribute the n-type characteristics to the stronger coupling of Al/SWNT than that of Au/SWNT. The reasons are as following. (1) The metal work function plays an important role for contact barriers. For example, Javey *et al.* have experimentally

achieved air stable p-type and n-type near-ohmic contact using Pd¹⁹ and Al¹⁴⁶ as the metal electrode, respectively. (2) However, it is not true that higher-work-function metals form lower SBs for p-type CNTFETs. The interfacial structure of the nanoscale contact also plays an important role. For instance, Shan *et al.* theoretically showed that the Fermi level alignment at the metal/nanotube contact could depend on the interfacial distance.¹⁴⁷ Moreover, Moon *et al.* experimentally and theoretically observed n-type CNTFETs with large-work-function metal.¹⁴⁸ They attributed the conduction type of CNTFETs to the interface differences of contacts. (3) In our case, both Al/SWNT and Au/SWNT are Schottky contact. Our previous work showed that Triton X 100 (as surfactant) could change CNTFETs with Au electrodes from p-type to ambipolar, and the process is reversible.⁸⁶ The observation suggests that the Schottky barrier for hole at Au/SWNT is increased by Triton X 100. (4) The SWNT-channel is covered by the Al electrode, while attaches to the sidewall of Au electrode. Thus, it is reasonable to have a stronger Al/SWNT coupling. Stronger Al/SWNT coupling could lead to lower effective barriers to the conduction band. If electrons see a much smaller barrier than holes, n-type conduction is enhanced. If the barrier height for electrons is larger than that for holes, we have p-type conduction. In contrast, if the barrier height for holes is larger than that for electrons, the device is p-type.

The conclusions drawn from this work are list as following:

- Short-channel CNTFETs with asymmetric contacts are fabricated. The Coulomb oscillation peaks superimposed on the transfer curves of an n-type FET are observed up

to 100 K. The oscillation current amplitudes are found to be asymmetric under positive and negative V_{DS} . However, single-electron tunneling current component remains unchanged when V_{DS} is reversed.

- The asymmetric current amplitude could be mainly caused by unequal thermionic emission current over the different Schottky barrier heights at the source/drain contacts. The energy barrier at the Au/SWNT contact is larger than that at Al/SWNT contact, by a factor of > 2 for all V_{GS} , owing to the work function difference between Au and Al.
- In atmosphere environment, the devices show significant diode-like effects with a maximum current rectification ratio of $\sim 10^4$, implying this type of devices have great potential to be used as diodes.

Chapter 7

Single-Electron/Hole Transport in SWNT-Gated CNTFETs

As an ideal one-dimensional (1-D) material, CNTs may serve as a perfect platform for studying of electron/hole transport in 1-D systems.^{115, 149, 150} Single-electron/hole charging with Coulomb blockade effects are typically investigated in CNT-quantum dot (QD) defined by metallic electrodes.^{151, 152, 153} In the quantum regime ($k_B T \leq \Delta E$, where ΔE is the average energy-level separation in the QD), the transport of non-interacting electrons occurs due to single-electron tunneling. However, when the electrostatic energy required for adding a single electron/hole to the QD exceeds the thermal energy, the tunneling is suppressed (Coulomb blockade). In contrast, in the classic regime (at the temperatures above those expected for single-electron tunneling of non-interacting electrons), the discreteness of the energy spectrum can be neglected.¹⁵⁴ With advanced lithographic techniques, single-,¹¹³ double-¹⁵⁵ and multiple-QD¹⁵⁶ systems could be fabricated in a single CNT, which provide deep insights into physics of

single/few electrons/holes transport processes. A CNT-QD is usually formed by a pair of electrostatic potential barriers induced by top-gate electrodes. However, the thickness of the potential barrier depending on the width of gate electrode is constrained by the limitations of lithographic techniques. In this work, we use SWNTs bundles as the gate electrodes to define QDs in a SWNT-channel. The SWNT-electrode makes it easy to obtain very narrow gate electrodes in a readily controlled manner without complex lithography. The Coulomb oscillations and “diamonds” are modified by the SWNT-gate voltages at low temperatures.

7.1 Fabrication method

A pair of electrodes (5 nm Ti/20 nm Au) S and D were fabricated on top of heavily doped Si (boron as dopant, resistivity of 0.01-0.02 $\Omega\cdot\text{cm}$) capped by a 500-nm-thick thermally grown SiO_2 as the back-gate dielectric. SWNTs were dispersed in deionized water with Triton X 100 ($\text{C}_{14}\text{H}_{22}\text{O}(\text{C}_2\text{H}_4\text{O})_n$, where n is 9 or 10) as surfactants (1% by weight). The suspension was ultrasonicated for 30 mins (power ~ 27 Watt/L). Then, the ACDEP technique was employed by applying an ac signal (SIN wave with frequency $f = 6$ MHz, peak-to-peak voltage $V_{\text{p-p}} = 16$ V) between S and D. The SWNT suspension was dropped to cover the area of S and D using a micropipette. The electric field was stopped after 5 seconds, and then the device was rinsed with deionized water for several minutes. A multimeter was used to check the resistance across S and D. If the resistance fell into the range of 0.5 to 20 M Ω , the device was soaked in acetone for clean

purpose. Otherwise, the SWNT-bridge process was repeated. After the electric breakdown process (to achieve a current on/off ratio of $> 10^2$), the device was scanned using AFM to ensure that there was one SWNT-bundle and the device surface was clean. Afterwards, a Si_3N_4 layer was deposited to cover the SWNT-channel by using a plasma-enhance chemical vapor deposition system (Plasma-Therm 790) under the following conditions: a mixed flow gases of 100-sccm diluted 10% silane gas, 30-sccm ammonia gas and 1000-sccm nitrogen gas at 300 °C with 40 W RF power. Next, the other pair of electrodes G and G' were fabricated so that the underneath SWNT-bundle was situated between them. Next, the ACDEP technique was used again to bridge the SWNT-gate between G and G' (see Fig 7.1 (a)). By repeating the process, multiple SWNT-gates could be fabricated, as shown in Fig 7.1 (c).

Fig 7.1 AFM images of single-, double- and multiple-SWNT-gated CNTFETs. (a) AFM image of a single-SWNT-gated CNTFET. S and D represent the source and drain electrodes, respectively. G and G' represents the top-gate electrodes. (b) Enlarged view of the area in the dotted-square in (a). Inset: schematic cross-section view of the device. (c) AFM image of a double-SWNT-gated CNTFET. (d) AFM image of a multiple-SWNT-gated CNTFET.

7.2 Single-electron transport in double-SWNT-gated CNTFETs

Conventional CNTFETs (heavily doped Si as the back-gate and 500-nm-thick thermally grown SiO₂ as the back-gate dielectric) were fabricated with ACDEP techniques followed by an electric breakdown process. Then, a thin Si₃N₄ (~30 nm) layer was deposited on the CNTFETs to serve as the top-gate dielectric. The top-gate electrode pair (G-G') were fabricated. After that, the ACDEP technique was employed again to place the top SWNT-gate. In the following discussion, we present the low-temperature characteristics of a double-SWNT-gated CNTFET, whose AFM images are shown in Fig 7.2. The left and right SWNT-gate are 4 and 7 nm in height, respectively, and the distance between them is ~ 300 nm.

Fig 7.2 A double-SWNT-gated CNTFET. (a) AFM images of a double-SWNT-gated CNTFET. The scale bar is 1 μm . Inset: the schematic cross section of the device configuration. S, D are the source and drain electrodes, respectively. G_L and G_R are the left and right top SWNT-gates, respectively, and GBG is the global back-gate. (b) Enlarged view of the area in the dotted-square in (a) (the height of the left and right SWNT-gates are 4 and 7 nm, respectively. L and R mark the cross points between the channel and the left and right SWNT-gate, respectively. The distance between L and R is ~ 300 nm. (c) Equivalent energy band diagrams for the single-electron tunneling (left) and blockade (right).

At low temperatures, significant current (I_{DS}) oscillations in the transfer curves (I_{DS} versus the global back-gate voltage, V_{GBG}) are observed under a fixed SWNT-gate (V_{TG}) potential of +2 V. Fig 7.3 (a) shows the bias (drain-source voltage, V_{DS})- dependent current oscillations at 25 K. When V_{DS} is increased, the oscillation peaks broaden and then disappear gradually. The temperature dependence of the current oscillation is shown in Fig 7.3 (b). Oscillations vanish with increasing temperature up to 100 K. Fig 7.3 (c) presents the contour plot of $\log|I_{DS}|$ in the V_{GBG} - V_{DS} plane.¹²⁶ Clear “diamond”-shaped current suppression regions are seen. These observations could be caused by the Coulomb blockade effects in a SWNT-QD.¹¹³ Interestingly, the low-temperature characteristics of the device are tunable by V_{TG} . The “diamond”-shaped current suppression regions are shown in Fig 7.4 (a) and (b) for $V_{TGS} = 0$ and -2 V, respectively. The V_{DS} - and temperature-dependent Coulomb oscillations at $V_{TGS} = 0$ and -2 V are shown in Fig 7.5, respectively.

Fig 7.3 Low-temperature characteristics at $V_{TG} = +2$ V. (a) I_{DS} - V_{GBG} curves at 25 K and $V_{TG} = +2$ V with $V_{DS} = 20, 40, 60, 100$ and 150 mV, respectively. (b) I_{DS} - V_{GBG} curves with $V_{DS} = +30$ mV and $V_{TG} = +2$ V at 40, 50, 60, 75 and 100 K, respectively. Inset: the equivalent circuit of a SET. C_L and C_R represent the tunneling capacitances at L and R, respectively. C_G is the capacitance between the SWNT-quantum dot and global back-gate. (c) Contour lines of $\log|I_{DS}|$ in the V_{DS} - V_{GBG} plane. The innermost contour lines represent $|I_{DS}| \sim 10$ fA. The dashed-rhombi delineate diamond-shaped current suppression regions. “e” and “h” stand for single electron and hole, respectively.

The observations could be understood using the framework of the Coulomb blockade effect in a SWNT-QD. Within the extended Coulomb blockade model, the amplitude of the current peak should increase with decreasing T at low temperatures if the charge transport occurs in the quantum regime.¹¹² However, the observed amplitude of the current peak decreases with decreasing T , as shown in Fig 7.3 (b). We therefore consider the single-electron transport occurs in the classic regime ($\frac{e^2}{C_\Sigma} > k_B T > \Delta E$, where C_Σ is the total capacitance to the QD). Several discrete energy states in the QD may be involved in the tunneling process for one current peak. The current oscillations are interpreted as the Coulomb blockade oscillations in the short SWNT-segment (between L and R in Fig 7.2 (b)) as a quantum dot, which is formed by a pair of local potential V_L and V_R . The local potentials are induced by the voltage applied to the SWNT-gate (V_{TG}).¹⁵⁷ It is noted that the two SWNT-gates are not identical in height in the AFM image (4 and 7 nm for L and R, respectively). Thus, they are illustrated as asymmetric potential barriers in Fig 7.2 (c). Therefore, a single-electron/hole transistor (SET/SHT)¹¹⁶ (see inset of Fig 7.3 (b) for the equivalent circuits) is formed with the SWNT segment between L and R as the QD and the left and right portions of SWNT-channel as the “reservoirs”. Hence, a Coulomb oscillation peak occurs once there is one or more discrete energy states in the “island” enters the window, eV_{ds} , formed by the voltage drop across the SET (the left schematic of Fig 7.2 (c)). However, when V_{GBG} is negatively increased further, the discrete energy states in the quantum dots are lift; meanwhile the conduction band edge bends upward (the right schematic of Fig 7.2 (c)).

As a result, no energy state falls into the eV_{ds} window, blockade of tunneling occurs. The voltage drop across the QD increases as V_{DS} is increased, more discrete energy states contribute to the tunneling current, resulting in the broadening of the Coulomb oscillation peaks and vanishing of some peaks. In addition, as T increases, the Coulomb oscillations disappear gradually when the thermal energy ($k_B T$) is comparable to or greater than the charging energy.¹¹³

Fig 7.4 Current contour plot at 25 K. Contour lines of $\log|I_{DS}|$ in the V_{DS} - V_{GBG} plane at (a) $V_{TG} = 0$ V and (b) $V_{TG} = -2$ V. The dashed-rhombi delineate diamond-shaped current suppression regions. “e” stands for single electron.

When $V_{TG} = 0$ V, the device is ambipolar with stronger p-type, and the conduction changes to n-type at $V_{GBG} \approx -1$ V (see Fig 7.5). Fig 7.6 (a) shows the schematic energy band diagram of hole-conduction branch ($V_{GBG} < -1$ V) at $V_{TG} = +2$ V. At a slightly negative V_{GBG} (▲), the electrostatic potential at L and R are higher (for hole) than elsewhere of the channel, and hence holes could not be injected over the potential barriers. Thus, the channel conductance is dominated by single-hole tunneling through the barriers (I_h'). In contrast, the energy bands shift upwards significantly at a very negative V_{GBG} (■). In this case, holes could pass over the potential barriers without tunneling (I_h). The contribution of single-hole tunneling decreases significantly. Thus, the oscillations of I_{DS} become weak when V_{GBG} decreases. Similarly, the energy bands shift downwards for electron-conduction branch ($V_{GBG} > -1$ V), as shown in Fig 7.6 (c) and (d). Single-electron conduction dominates the channel conductance at a slightly positive V_{GBG} (●). The energy bands move downwards further as V_{GBG} is increased (◆). As a result, the single-electron tunneling becomes less significant, and thus the oscillation of I_{DS} becomes weak. This effect also explains the observation that the Coulomb diamonds disappear gradually when $|V_{GBG}|$ is increased, as shown in Fig 7.3 (c).

Assuming that the same amount of holes are involved in all tunneling events, we could give a quantitative description for the single-hole tunneling by considering the Coulomb diamonds (labeled by 1h and 2h) in Fig 7.3 (c). With the gate modulation period $\Delta V_G \approx 1$ V, the gate capacitance of the SWNT-QD is obtained as

$C_G = \frac{e}{\Delta V_G} \approx 0.16 \text{ aF}$.⁸⁸ The slopes of the left and right boundary lines of the Coulomb

diamonds are $S_L = \frac{C_G}{C_L + C_G} \approx 0.08$ and $S_R = \frac{C_G}{C_R} \approx 0.12$, respectively, where C_L and C_R

are the left and right tunneling capacitors, respectively. So, $C_L = (\frac{1}{S_L} - 1)C_G \approx 1.8 \text{ aF}$ and

$C_R = \frac{C_G}{S_R} \approx 1.3 \text{ aF}$. The total capacitance could be determined by $C_\Sigma = C_G + C_L + C_R \approx 3.3$

aF. Comparing this with a simple estimation of $C_\Sigma = \epsilon_0 \epsilon_r l$,¹¹⁸ where l is the length of the

SWNT-QD and $\epsilon_r = 4$ for SiO_2 , we obtain $l \sim 100 \text{ nm}$. l is underestimated in comparison

with the observed distance between L and R in Fig 7.2 (b) ($\sim 300 \text{ nm}$ from the AFM measurement). A smaller l is caused by underestimation of C_Σ , which is likely to be

caused by the S/D contacts that are connected in series with the tunneling barriers.

Therefore, the calculated capacitance, which is the equivalent capacitances of S/D contacts and tunneling barriers, is smaller than the actual tunneling capacitance. ΔE for electrons with the appropriate dispersion confined to a 1-D box of length l is

$\frac{dE}{dk} \frac{\Delta k}{2} = \hbar v_F \frac{\pi}{2l} \approx \frac{0.8}{l} \text{ meV}$, where l is in μm , and $v_F \approx 8.1 \times 10^5 \text{ m/s}$ is the Fermi velocity

of graphite and the factor $\frac{1}{2}$ accounts for the nondegeneracy of the two 1-D subbands.

$\Delta E \approx 2.8 \text{ meV}$ (for $l = 300 \text{ nm}$) is comparable to $k_B T \approx 2.6 \text{ meV}$ at 30 K. This estimation indicates that the Coulomb blockade effect occurs in the classic regime. Moreover, one can see that the significant Coulomb blockade is caused by the large charging energy

$E_C = \frac{e^2}{C_\Sigma} \approx 50 \text{ meV}$ ($\gg k_B T$ at 30 K). The conversion factor from the global back-gate

voltage to the electrostatic potential of the QD is estimated as $\frac{E_C}{e\Delta V_G} \approx 0.05$. The small

conversion factor is caused by poor back-gate coupling owing to the 500-nm-thick SiO_2 .

The observed Coulomb diamonds at $V_{TG} = 0$ and -2 V are shown in Fig 7.4 (a) and (b), respectively. As V_{TG} become more negative, the trends of Coulomb blockade characteristics are in three aspects: (1) the Coulomb oscillations of hole conduction are suppressed and those of electron conduction are enhanced; (2) the oscillation patterns change in terms of period and height (see supplementary materials), and (3) the slopes of the boundary lines of the Coulomb “diamonds” becomes different. At $V_{TG} = 0 \text{ V}$, four Coulomb diamonds for electron-conduction (1e to 4e in Fig 7.4 (a)) are clearly observed. In contrast, at $V_{TG} = -2 \text{ V}$, six Coulomb diamonds for electron-conduction are observed (1e to 6e in Fig 7.4 (b)). This is understandable from the energy band diagrams shown in Fig. 7.6 (e). A more negative V_{TG} shift energy band upwards locally and thus has higher impacts on electron conduction than on hole conduction. The slopes of the boundary lines of Coulomb “diamonds” are determined by the tunneling capacitors, which depend on the height and thickness of the potential barriers. With the aforementioned estimation, we can determine the electrical parameters for single-electron tunneling here. Considering the Coulomb “diamonds” (2e and 3e) in Fig 7.4 (b), the gate modulation period $\Delta V_G \approx 1.2 \text{ V}$ and the slopes of the boundary lines are $S_L \approx 0.03$ and $S_R \approx 0.04$. Therefore, the

capacitances are obtained as $C_G \approx 0.13$ aF, $C_L \approx 4.2$ aF and $C_R \approx 3.3$ aF. And then, the total capacitance is $C_\Sigma = C_G + C_L + C_R \approx 7.3$ aF. Higher capacitances mean stronger couplings, i.e., lower and/or thinner tunneling barriers, and hence SET here is not well defined as SHT at $V_{TG} = +2$ V.

The V_{DS} - and temperature-dependent Coulomb oscillations of the device at $V_{TG} = 0$ V are shown in Fig 7.5 (a) and (b), respectively. The Coulomb oscillations of hole-conduction are suppressed and those of electron-conduction are enhanced in comparison with the case of $V_{TG} = +2$ V (see Fig 7.3 (a) and (b)). As V_{TG} is decreased from +2 to 0 V, the energy bands at L and R shift upwards, and hence the barriers are decreased for holes, but increased for electrons. As a result, the single-electron tunneling is enhanced and single-hole tunneling is suppressed. However, the characteristics of the Coulomb oscillations are similar in comparison with those at $V_{TG} = +2$ V: (1) the oscillation peaks broaden and disappear when V_{DS} is increased, and (2) As temperature is increased, the oscillations vanish gradually. Moreover, the oscillation patterns are different in terms of peak spacing and shapes.

Fig 7.5 a, I_{DS} - V_{GBG} curves at 25 K and $V_{TG} = 0$ V with $V_{DS} = 20, 40, 60, 100$ and 150 mV, respectively. b, I_{DS} - V_{GBG} curves with $V_{DS} = +30$ mV and $V_{TG} = 0$ V at $40, 50, 60, 80$ and 100 K, respectively. c, I_{DS} - V_{GBG} curves at 25 K and $V_{TG} = -2$ V with $V_{DS} = 20, 40, 60, 100$ and 150 mV, respectively. d, I_{DS} - V_{GBG} curves with $V_{DS} = +30$ mV and $V_{TG} = -2$ V at $40, 50, 60, 70$ and 90 K, respectively.

Fig 7.6 Energy band diagrams at (a) a very negative V_{GBG} (■), (b) a slightly negative V_{GBG} (▲), (c) a slightly positive V_{GBG} (●), and (d) a very positive V_{GBG} (◆). The symbols are corresponding to those in Fig 7.3 (c). e, Schematic energy band diagrams at a very positive V_{GBG} , and the enlarged view of the energy band bending at different V_{TG} .

As stated above, the Coulomb blockade characteristics depend on the tunneling barriers, which are determined by both V_{TG} and V_{GBG} . The roles of V_{GBG} are twofold: (1) to manipulate the energy levels in the QD, and (2) to control the energy band bending over the entire channel. In contrast, the impact of V_{TG} is very local. The tunneling barriers depend on the effective electrostatic potentials superimposing the effects of V_{TG} and V_{GBG} .

The room-temperature transfer characteristics of the same device are shown in Fig 7.7. With floating V_{TG} , the device is ambipolar with stronger p-type conduction. As V_{TG} is increased from -2 to +2 V, the device continuously changes from p-type to n-type. The threshold voltage moves from greater than +8 V to -7.5 V (V_{th} in the case of $V_{TG} = -2$ V falls in the range $V_{GBG} > +8$ V). The observations are understood from the energy band diagram of the device. When $V_{TG} = +2$ V, a less positive V_{GBG} is necessary to start n-type conduction. Moreover, the subthreshold slope of p-type conduction increases drastically. A clear explanation of this observation is pending. A possible reason is related to band-to-band tunneling.⁵⁴ It is noted that the effect of V_{TG} is less significant at low temperatures. The reason could be the conductivity of the SWNT-gate decreases significantly at low temperatures.

Fig 7.7 Transfer curves in air at room temperature. I_{DS} - V_{GBG} curves in air with floating V_{TG} and $V_{TG} = -2, 0$ and $+2$ V, respectively.

7.3 Conclusions

The following conclusions could be drawn from the above works:

- A technique for fabricating SWNT-gated CNTFETs is developed, which makes it possible to fabricate sub-10-nm-wide top-gate electrodes without complex lithography.
- Significant Coulomb blockade characteristics are observed in the double-SWNT-gated CNTFETs. The SWNT-gates are 4 and 7 nm in height, respectively, and the distance between them is ~ 300 nm. A pair of potential barriers is induced by the double-SWNT-gates, and hence a single-electron/hole transistor working in the classic regime with Coulomb blockade effects is formed. The Coulomb oscillations show strong bias and temperature dependence. Coulomb “diamonds” are observed for both single-hole and -electron tunneling.
- Voltages applied to the SWNT-gates determine the tunneling barrier height, and thus modify the characteristics of Coulomb oscillations and diamonds. The unequal capacitances calculated from the Coulomb “diamonds” indicate that the tunneling barrier pair is asymmetric.

Chapter 8 Conclusions and Future Work

8.1 Conclusions

The findings and implications of this project are summarized as following.

8.1.1 Hysteresis and stability issues in CNTFETs

1. Hysteresis in our CNTFETs is caused by charge trapping around the SWNT-channel. Hysteresis window shifts when the metal-electrode and SWNT work function are affected by oxygen exposure. Hysteresis window size is reduced by more than 50% (~ 12 V) when temperature is decreased from 295 to 16 K because thermally activated charge hopping into and out of trapping centers are suppressed at low temperatures. However, the reduction of the hysteresis window is mainly ($\sim 67\%$) caused by shift of reverse sweeping curve. The observation suggests that electron trapping is easier to be affected by temperature variation than hole trapping.
2. The sources of trapping centers have been revealed in our CNTFETs. The major source is not from the water molecules adsorbed on the substrate and around the SWNT-channel. Because the hysteresis could only be reduced by 40% after annealing the device in dry air. The remaining hysteresis (60%) could be attributed to other trapping centers,

other than water molecules. The unknown trapping centers could be formed by the foreign species adsorbed on the device surface, such as surfactants (Triton X 100, $C_{14}H_{22}(C_2H_4O)_{10}$), impurities, and traps in bottom gate oxide (thermally grown SiO_2). Moreover, ammonia (NH_3) is also found to play a role of trapping centers, which are found to be closely related to surface water. It is found that water molecules help adsorption of NH_3 , and hence increase the amount of NH_3 as trapping centers.

3. A technique for eliminating hysteresis has been developed. An annealing process (300 °C) in vacuum followed by Si_3N_4 and SiO_2 passivation is found to be an efficient way. Since the surface water and surfactant molecules desorb at 300°C in vacuum in PECVD chamber, the trapping centers in passivated CNTFETs are mainly caused by interface and bulk traps in the passivation layer (Si_3N_4 and SiO_2). Owing to the interface traps at the dielectric/SWNT interface and the bulk traps in the low-density dielectrics (deposited by a PECVD), large gate voltage sweeping range still generates significant hysteresis. This observation suggests that energy levels associated with these trapping centers (Si_3N_4) are deeper than other traps (water-related), and then greater back-gate voltages (larger sweeping range) are necessary to activate the charging/discharge process.

4. The influences of globally and locally trapped charges on carrier transport in SWNTs have been investigated. Through applying voltage pulses to a global back-gate and a local top-gate, “globally” and “locally” distributed pre-trapped charges near the CNT-channel can be induced, respectively. For the back-gate voltage sweeping, the transfer curves are shifted due to the trapped charges. In addition, significant decreases in the field-effect mobility for both hole and electron transport are also found. Local

potential fluctuations caused by the trapped charges could be responsible for the observations. The locally pre-trapped holes and electrons keep the device at “ON” and “OFF” states for the top-gate sweeping, respectively. Therefore, the trapped charges at S/D contact regions and SWNT-body could both effectively influence the channel conductance through the “Schottky barrier modulation” and “bulk modulation”, respectively.

8.1.2 Single-electron/hole transport in SWNT

1. Single-electron/hole transports with the Coulomb blockade effects are studied in SWNTs. Significant Coulomb oscillations are found in specially constructed CNTFETs that consist of long SWNTs bridging the source/drain electrodes, and short SWNTs attached to the source/drain contacts. The oscillation peaks disappear gradually with increasing temperatures up to 70 K. Current contour plot in V_{ds} - V_{gs} plane shows “diamond”-shaped current forbidden regions at 15 K. The Coulomb oscillations could be interpreted as follows: (1) charges trapped in the short SWNTs could be quantized; and (2) the electrostatic potential at the long-tube/electrodes contacts could be influenced by the charges stored in the short SWNTs. As a result, the channel current could be modulated by the charged short SWNTs.

2. Short-channel (< 100 nm) CNTFETs with asymmetric drain and source contacts are fabricated with a self-alignment technique (shadow e-beam deposition). The Coulomb oscillation peaks superimposed on the transfer curves of an n-type CNTFET (on/off ratio

$\sim 10^7$) are observed up to 100 K. However, the oscillation current amplitudes are unequal under positive and negative V_{DS} . Single-electron tunneling current component remains unchanged when V_{DS} is reversed. The asymmetric current amplitude is mainly caused by unequal thermionic emission current over different barrier heights at the source/drain contacts. Above 100 K, thermionic emission dominates the current. The activation energy at the Al/SWNT contact should be larger than those at the Au/SWNT contact, by a factor of > 2 for all V_{GS} , owing to the work function differences between 3-D metal and 1-D SWNT. In atmosphere environment, the devices show significant diode-like effects with a maximum current rectification ratio $\sim 10^4$.

3. A technique for fabricating SWNT-gated CNTFETs has been developed. This success makes it possible to fabricate very narrow top-gate electrodes without complex lithography. Significant Coulomb blockade characteristic are observed in the double-SWNT-gated CNTFETs. A pair of potential barriers is induced by the double-SWNT-gates, and hence a single-electron/hole transistor working in the classic regime with the Coulomb blockade effects is formed. The Coulomb oscillations show strong bias and temperature dependence. The Coulomb “diamonds” are observed for both single-hole and -electron tunneling. Voltages applied to the SWNT-gates determine the tunneling barrier height, and thus modify the characteristics of the Coulomb oscillations and “diamonds”. The unequal capacitances calculated from the Coulomb “diamonds” indicate that the tunneling barriers are asymmetric.

8.2 Future work

1. Ohmic-contact CNTFETs

CNTFETs used in this work have the Schottky contacts. Ohmic-contact is indispensable for CNTFETs to be used in future nanoelectronics. In our case, ohmic contacts between SWNTs and metals might be achieved in three steps: (1) clean devices may be obtained by soaking the devices in acetone or other chemical solutions, followed by annealing in inert or high vacuum environment over 300 °C. (2) tube-under-metal structure could be achieved with a second lithography process with a pair of electrodes situated on top of the SWNT-channel. High-work-function metal Pd could be used to make the electrodes since it is reported to have the best contact with SWNTs due to “wet” interaction. (3) low-energy H plasma treatment that helps to reduce the contact barriers for hole could be implemented.

2. Coupling between 1-D SWNT and 3-D metal

When investigating the activation energy of thermionic emission current, we found some interesting points: (1) the extract activation energy is always very small (within 100 meV) for both p-type and n-type devices, (2) negative activation energy could be usually obtained if we use the SB theory as $\ln I = -\frac{qE_a}{kT} + 2 \ln T$. $2 \ln T$ is often omitted in the published works since its influence is negligible in some cases. However, it is not true in our devices. A tentative explanation is as following. The CNTFETs fabricated with ac dielectrophoresis technique usually have poor contacts. Hence, tunneling dominates the transport in the entire range of temperatures in some devices.

Therefore, the “thermionic emission current”, which is actually tunneling current, deviates much from the SB theory. However, further study is necessary for obtaining a quantitative description.

3. Memory devices based on CNTFETs

Reliable and reproducible memory operations may be achievable by introducing well-defined trapping centers, such as metal clusters, ONO layer, etc. CNTFET is a type of excellent charge-sensing devices owing to the 1-D properties of SWNTs. Metal cluster could be fabricated with a self-assembly method: A thin metallic film (<10 nm) is deposited on the surface of CNTFETs, followed by a rapid thermal annealing process to form metal nano particles. Charge trapped in the nano particles could be quantized even at room temperature. This type of devices could be promising to work as single-electron memory cells.

4. Ballistic carrier transport in SWNTs

SWNTs have a great advantage of observing ballistic carrier transport process over other nanoscale materials. The research on characteristics of ballistic transport is limited by the SWNT/metal interface and length of SWNT-channel. The self-alignment technique described in Chapter 6 could be employed to create sub-10 nm channel length. The channel length can be much smaller than the electron scattering mean free path with acoustic phonons, defects, and optical phonons in SWNTs, typically about ~ 1 μm , ~ 1 μm and ~ 15 nm, respectively. Therefore, the carrier transport through the short channel should show ballistic transport characteristics.

Author's Publications

1. **Hong Li** *et al.* "Carbon-Nanotube-Based Single-Electron/Hole Transistors", Appl. Phys. Lett. **88**, 013508 (2006)
2. **Hong Li** *et al.* "Charge Storage in Carbon Nanotube Field-Effect Transistors", International Journal of Nanoscience **5**, 553 (2006).
3. **Hong Li** *et al.* "Interpretation of Coulomb oscillations in carbon-nanotube-based field-effect transistors", Phys. Rev. B **73**, 235431 (2006).
4. **Hong Li** *et al.* "Charge-Trapping Effect Caused by Ammonia in Carbon Nanotubes", J. Nanosci. Nanotechnol. **7**, 335 (2007).
5. **Hong Li** *et al.* "Global and local charge trapping in carbon nanotube field-effect transistors", Nanotechnology **19**, 175203 (2008).
6. **Hong Li** *et al.* "Unique carbon nanotube field-effect transistors with asymmetric source and drain contacts", Nano Lett. **8**, 64 (2008).
7. Jingqi Li, Qing Zhang, and **Hong Li** and Mary B Chan-Park, "Influence of Triton X-100 on the Characteristics of Carbon Nanotube Transistors", Nanotechnology **17**, 668 (2006).

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