Design of CMOS broadband transimpedance amplifiers for 10Gbit/s optical communications

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Design of CMOS Broadband Transimpedance Amplifiers for 10Gbit/s Optical Communications

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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Lu Zhenghao

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ABSTRACT

The dramatic growth of data transportation volume and speed over Internet in recent years entails the development of low cost integrated optical communication systems with ever-increasing transmission bandwidth. Currently, the most successful commercial high-speed digital communication protocol is SONET (Synchronous Optical Network) OC-192 while the 10Gb/s Ethernet (IEEE802.3ae) is also emerging as an alternative for point-to-point applications. Therefore, optical communication systems operating at 10Gb/s are of great interest.

Transimpedance amplifiers are extensively exploited as the front-end of optical communication receivers. Traditionally, such front-end circuits and devices are heavily dependent on III-V technologies due to their speed and noise advantages. However, the demand for high volume, wide deployment of optical components in recent years makes silicon based integrated circuits the most economical solution. CMOS appears to be the best candidate for fully integrated Transimpedance Amplifier (TIA) design due to its cost, integration and manufacturability advantages and providing reasonable speed, noise performances at the same time.

This work examines the technical challenges and explores various broadband design techniques in implementing transimpedance amplifiers using cost effective CMOS technology. Based on these proposed and existing broadband design techniques, two prototypes of 10Gb/s transimpedance amplifiers are implemented using Chartered Semiconductor (CHRT) 0.18 μm CMOS process, which achieve comparable performance to those III-V and SiGe counterparts in most aspects while possessing the merits of CMOS technology.

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Chapter 1

Introduction

1.1 Background

Ever since the dream of transferring information over long distances with massive volumes was fulfilled in 1977 when AT&T (American Telephone & Telegraph) and GTE (General Telephone and Electronics) deployed the world's first fiber optic telephone system, the increasing volume and speed of data transportation over optical fibers have revolutionized the way people communicate and conduct business [1][2].

It is generally accepted that optical high speed signaling is not sensitive to electromagnetic interference (EMI) and virtually suffers no parasitic coupling as well as other problems faced by electrical signals. Moreover, optical signals enjoy unparalleled bandwidth. Therefore, fiber optic communications have experienced significant growth during the past three decades [3]. For the last 15 years, Synchronous Optical Network/Synchronous Digital Hierarchy (SONET/SDH) has been the main transport technology over optical fibers. SONET is a standard for optical communications, providing framing, as well as a rate hierarchy and optical parameters for interfaces. Initially developed by Bell Communications Research, it has been adopted as a standard by the American National Standards Institute (ANSI). A slightly different version, SDH, has been adopted by the International Telecommunication Union — Telecommunication Standardization Sector (ITU-T). The transmission bit rates offered by SONET or SDH standards are listed in Table 1.1. Currently, the most successful and commercially available optical

communication system is SONET OC-192 or SDH STM-64 operating at a data rate of about 10Gb/s while the 10Gb/s Ethernet (IEEE802.3ae) is also emerging as an alternative for point-to-point applications. Furthermore, with the fast development of optical transport infrastructures, the 40Gb/s OC-768 system is becoming commercially available and new techniques such as Wavelength Division Multiplex (WDM) have emerged to greatly increase the bandwidth capacity over optical fibers [4-8].

Table 1.1: SONET/SDH transmission data rates [9]

SONET	SDH	Bit Rate
OC-1	-	51.84Mb/s
OC-3	STM-1	155.52Mb/s
OC-12	STM-4	622.08Mb/s
OC-48	STM-16	2.4883Gb/s
OC-192	STM-64	9.9533Gb/s
OC-768	STM-196	39.8131Gb/s

1.2 Motivation

Based on the reach distances of the optical data-links, the global optical infrastructure can be categorized into the following individual networks [10]:

1. Ultra Long Haul Networks: >500km
2. Wide Area Networks (WAN): >100km
3. Metropolitan Area Networks (MAN): 2km~100km
4. Local Area Networks (LAN): <2km
5. Very Short Reach (VSR) Applications: <300m.

In long-haul optical transport systems that usually need to cover a distance of over

10km, transmission losses over long distances and optical sensitivity are of greater importance than the cost. The optical signal traveling over the fiber is usually amplified by expensive Erbium-doped Fiber-optical Amplifier (EDFA) before reaching the electrical receiver end. The optical communication wavelength is about 1300nm or 1550nm, where there is a minimum attenuation and high efficiency for EDFA while silicon exhibit very low absorption at these wavelengths. All these above-mentioned factors and concerns provide the reason why in high-speed optical front-end design, especially for WAN and MAN applications, III-V and SiGe devices and circuits dominate. The main drawbacks of such technologies are high cost and the incompatibility with the mainstream CMOS technology, leading to multi-chip solutions or hybrid-integration techniques, which increases the system cost further [11-17].

In short-reach optical transport systems (usually less than 1 kilometer, such as the LAN or VSR applications), CMOS technology is becoming popular due to the following reasons. First, the requirements of high volume and wide deployment of optical components in short-reach applications inevitably brings the cost factor to the top of all design considerations. The cost and integration advantages make CMOS technology the strongest candidate. Second, the 850nm wavelength has been widely used for short-reach applications because at the transmitter end low-cost 850nm vertical cavity surface emitting lasers (VCSEL) are readily available and at the receiver end silicon photodetectors exhibit reasonable absorption at this wavelength. CMOS monolithic integrated optical receiver appears to be a good low-cost match for the 850nm VCSEL transmitter [18-23]. Third, with the feature size scaling-down trend, deep-submicron CMOS transistors are well capable of high-frequency operations. With the help of carefully studied circuit design

techniques, CMOS optical preamplifiers are also able to achieve comparable performances to those III-V or SiGe counterparts yet maintain the merits of low-power, low-cost and high-manufacturability. Finally, short-reach 10Gb/s data communication standards (OC-192 VSR, 10Gb/s Ethernet) have been specified with relaxed optical sensitivity requirements comparing to those long-haul optical transmission standards, which subsequently alleviates the design challenges using CMOS technology [24-27].

Transimpedance amplifiers (TIAs) are widely exploited as the front-end circuits for optical communication receivers [28] [29]. Traditionally, such front-end circuits are implemented using III-V technologies due to their speed and noise advantages. There have been plenty of integrated circuits/devices implemented in III-V, Si Bipolar and SiGe technologies for 10Gb/s optical communication applications [30-36]. With these high-performance technologies, optical circuits/devices for even higher data rate operations (e.g. SONET OC-768) have been reported [37-42]. However, the recent rapidly increasing demand for high volume, wide deployment of optical components in LAN, fiber-to-home, VSR and inter/intra-chip applications requires low-cost and low-power devices. CMOS appears to be the best candidate for fully integrated TIA design due to its cost, power, integration and manufacturability advantages and provides reasonable speed, noise performances at the same time. Numerous CMOS TIAs for multi-gigabit/s, 10Gb/s or even higher data rate applications have been realized [43-50]. Fully integrated CMOS optical transceivers for high-speed optical communications have also been reported in recent years [51-53]. Among all the challenges in the design of fully integrated CMOS broadband TIAs, sufficient bandwidth with small gain ripple is of the first priority and low-noise is the second because the noise of

the preamplifier dominates that of the whole receiver. Due to the inferior parasitic, speed, noise characteristics of CMOS active/passive devices, many circuit techniques have been studied in CMOS TIA design to achieve comparable performances to those III-V or SiGe counterparts [54-58].

The main bandwidth restriction of a conventional TIA is usually at the input node due to the large parasitic photodiode capacitance. By modifying conventional common gate (CG) input stage [59-62] to regulated cascode [63-65] or common gate feed-forward topology [66] containing negative feedback, very small input impedance can be obtained to relax the gain-bandwidth trade-off at the input node. Capacitive degeneration or peaking utilizes capacitive elements to add an extra zero that compensates the dominant pole or an extra pole to implement a well-controlled frequency response respectively [28] [33] [55] [67-68]. Inductive peaking is found effective both in noise reduction and bandwidth enhancement. Shunt inductive peaking simply uses inductor in series with the load resistor to maintain a constant effective load over a wider frequency range. Series inductive peaking normally employs series inductors between gain stages or at input/output node so that the lumped parasitic capacitances at each node are split into LC networks. The whole TIA is turned into a low-pass filter with controllable pass-band characteristics [68-75].

The purpose of this thesis is to investigate various broadband design techniques in high performance TIA design and explore novel design techniques to implement low-noise, low-power 10Gb/s TIAs suitable for very-short-reach applications using cost effective CMOS technology.

1.3 Overview of optical transceivers

Optical interconnects have been used to circumvent the data transportation challenges arising from the physical limitations faced by electrical interconnects. Figure 1.1 shows a typical optical transceiver (transmitter and receiver) block diagram [76-77]. On the transmitter side, the multiplexer (MUX) combines the parallel data from the digital logic part into a single high speed serial data. The parallel data is selected via MUX and retimed by a bit-rate (or half-rate) clock synthesized from a clock multiplication unit (CMU). This high speed serial data stream is finally used to drive the corresponding optoelectronic device (usually a laser diode) by a laser driver or modulator driver. The current of a laser diode (LD) is modulated by the laser driver and the light intensity of the laser is therefore modulated [28] [55] [78-79]. In an OC-192 optical transport system, a 4:1 or 16:1 multiplexer (MUX) combines four parallel 2.488Gb/s electrical signals or 16 parallel 622-Mb/s electrical signals to 10Gb/s serial data, which is retimed by a clock synthesizer. The OC-192 system data rate is 9953.28Mb/s while the IEEE 802.3ae 10 Gigabit Ethernet standard operates at a data rate of about 10.3Gb/s [25] [26].

The light signal stream produced by the laser diode is mounted onto optical fibers for transmission. In long distance optical transmission systems, the light signal is usually amplified by expensive Erbium-doped Fiber-optical Amplifier (EDFA) before reaching the electrical receiver end to compensate the transmission loss [33]. The optical wavelength used for such long distance transmission is usually 1550nm where there is a minimum attenuation and high efficiency for EDFA. However, in cost-sensitive short-reach optical communication systems, EDFA is absent and low-cost 850nm optoelectronic devices are widely used.

Figure 1.1: A typical optical transceiver [76-77]

A typical optical receiver starts with a photodetector (PD), which converts the incoming optical signal to a small output current proportional to the input optical power. This small current is subsequently converted to voltage signal by a transimpedance amplifier (TIA) [28]. The transimpedance amplifier should have low-noise and wide-band characteristics to amplify the small current to voltage with a high signal to noise ratio (SNR) while introducing minimum intersymbol interference (ISI) [55]. In broadband circuit design, the transimpedance front-end usually cannot afford high gain and wide bandwidth at the same time. Therefore, high-speed TIA generally cannot provide enough gain to produce digitally detectable output voltage swing. The voltage signal from the output of the TIA is further amplified by either a limiting amplifier (LA) or an automatic gain control amplifier (AGC amplifier). The limiting amplifier and automatic gain control amplifier are collectively known as post amplifiers or main amplifiers [55]. The

resulting signal, which is typically several hundred mV strong, is fed into a clock-data-recovery (CDR) circuit, which reproduces the clock signal and extracts the data by means of retiming. A demultiplexer (DEMUX) then converts the fast serial data stream to low speed parallel data streams to be processed by the digital logic blocks [28].

The most commonly used modulation scheme in optical communication is the non-return-to-zero (NRZ) format. This modulation scheme is in a form of on-off keying (OOK), which means the signal is on to transmit a “one” bit and is off to transmit a “zero” bit. It is a more bandwidth efficient scheme compared with the return-to-zero (RZ) data [28] [55]. Figure 1.2 shows an example of the two data formats for the identical bit pattern. Though the RZ signal occupies a larger bandwidth compared with NRZ signal, it requires less signal-to-noise ratio for reliable detection [91]. In this work, only NRZ data scheme will be adopted.

Figure 1.2: NRZ and RZ bit streams with identical bit patterns [55]

1.4 Research contributions

The research of this thesis is mainly focused on the analysis and design of 10Gb/s transimpedance amplifiers (TIAs) using 0.18 μ m CMOS technology. Various technical challenges and broadband design techniques in designing CMOS high-speed TIAs are studied and explored. This thesis also provides detailed study of the noise characteristics of CMOS TIAs based on the van der Ziel noise model.

Two prototypes of 10Gb/s transimpedance amplifiers are proposed and implemented using Chartered (CHRT) 0.18 μm CMOS process, which are suitable for 10Gb/s short-reach optical communication systems such as 10G Ethernet VSR and OC-192C. An automatic gain control (AGC) mechanism has also been proposed and silicon verified.

1.5 Thesis organization

This thesis is organized into six chapters:

Chapter 1 provides an introduction to the problem addressed, and an outline of the thesis.

Chapter 2 is an overview of the transimpedance amplifier fundamentals including photodetectors, optical link budget calculations, and transimpedance amplifier specifications. Some existing design techniques for transimpedance amplifiers are reviewed in this chapter together with the basic noise analysis methods for TIAs. The analyses are based on the van der Ziel MOSFET noise model that includes the channel thermal noise, induced gate noise and their cross-correlation.

Chapter 3 introduces and analyzes a novel bandwidth enhancement technique based on the combination of capacitive degeneration, broadband matching network and the regulated cascode (RGC) input stage, which turns the transimpedance amplifier (TIA) design into a fifth order low-pass filter aiming for flat gain frequency response. This broadband design methodology for TIAs is presented with an example implemented in CHRT 0.18 μm 1.8V RFCMOS technology. Measurement data shows a -3dB bandwidth of about 8GHz for a 0.25pF photodiode capacitance (the total input parasitic capacitance is 0.35pF including

the photodiode capacitance). Comparing with the core RGC TIA without capacitive degeneration and broadband matching network, this design achieves an overall bandwidth enhancement ratio of 3.6 with very small gain ripple. The transimpedance gain is $53\text{dB}\Omega$ with a group delay of about $80\pm 20\text{ps}$. The whole chip size is $0.6 \times 0.6\text{mm}^2$ including pads while the core circuit occupies $0.45 \times 0.25\text{mm}^2$. The chip consumes 13.5mW DC power from a single 1.8V supply. The measured average input referred noise current spectral density is $18\text{ pA}/\sqrt{\text{Hz}}$ up to 10GHz . At the end of this chapter, an extended noise analysis of the regulated cascode input stage based on the van der Ziel MOSFET noise model that includes the effect of the induced gate noise is presented. This extended noise analysis of the RGC topology is original and has not been done before in any publications according to the author's knowledge.

Chapter 4 describes a novel CMOS broadband transimpedance amplifier design with common gate input stage and common source active feedback. The proposed input stage is able to achieve very low input impedance that is comparable to the well-known regulated cascode (RGC) input configuration. Therefore, the bandwidth limitation effect due to the large input parasitic capacitance including the photodetector capacitance can be greatly reduced. The proposed TIA design also employs series input inductive peaking to extend the bandwidth and a two-stage capacitive degeneration to boost the bandwidth as well as the gain. The proposed TIA design has been realized using CHRT $0.18\mu\text{m}$ RFCMOS technology. The measurement data shows a transimpedance gain of $54.6\text{dB}\Omega$ (540Ω) and a -3dB bandwidth of about 7GHz for a 0.2pF photodiode capacitance (the total input parasitic capacitance is 0.3pF including the photodiode capacitance). The noise measurement shows an average input referred noise current spectral density of

about $17.5 \text{ pA} / \sqrt{\text{Hz}}$ up to 7GHz. The measured group delay is within $65 \pm 10 \text{ ps}$ over the bandwidth of interest. The chip consumes 18.6mW DC power from a single 1.8V supply. The whole chip size is $0.55 \times 0.6 \text{ mm}^2$ including pads while the core circuit occupies $0.4 \times 0.25 \text{ mm}^2$. In this chapter, the noise performance of the proposed TIA is analyzed in detail based on the van der Ziel MOSFET noise model including the induced gate noise. The effect of the induced gate noise in a broadband transimpedance amplifier is also included.

Chapter 5 analyzes an automatic gain control (AGC) mechanism. A transimpedance amplifier with built-in AGC circuit is also presented. The core TIA design is based on the same TIA design presented in Chapter 3. The proposed AGC circuit is used to reduce the input overload induced distortion and timing jitter. The proposed TIA with AGC design has been realized using CHRT 0.18 μm RFCMOS technology. The proposed AGC mechanism is silicon verified.

Chapter 6 provides the conclusion of this thesis and proposes some recommendations for future work.

Chapter 2

Transimpedance Amplifier Fundamentals

The transimpedance amplifier (TIA), acting as the electrical front-end of an optical receiver, is an essential block in optical communication systems. Together with the photodetector (PD), it plays a very important role in optical link budget determination. Front-end circuits for high-speed applications usually require the characteristics of low-noise and broad-bandwidth. With no exception, the TIA design entails many trade-offs between noise, bandwidth, gain, dynamic range, supply-voltage and power dissipation, presenting difficult challenges especially when CMOS technology is used. At the beginning of this chapter, important performance characteristics of an optical receiver front-end will be identified and related to TIA design parameters. Next, the receiver front-end requirements for short distance OC-192/10G Ethernet standards will be reviewed, which lead to TIA design specifications for short-reach applications. This chapter concludes with a review of some existing TIA design techniques and basic noise analysis methods for TIAs based on van der Ziel MOSFET noise model.

2.1 General considerations

The most important performance characteristics that are used to measure an optical receiver are bandwidth (operation bit rate), sensitivity (bit error rate), and dynamic range (overload capabilities) [28] [55]. Figure 2.1 shows a basic receiver front-end model, which includes the photodetector and the transimpedance amplifier. The first element in an optical receiver is the photodetector (PD) [55].

The simplest photodetector in commercial optical communication systems is the p-i-n photodetector. In this thesis, we will use p-i-n photodetector as a simple example to understand the general principle of a photodetector. The equivalent input noise current source $i_{n,eq}$ is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actual noisy TIA does. This equivalent input noise current, also called the input referred noise current, is a significant figure of merit of TIA design in that it directly affects the receiver sensitivity. Although the photodetector also contributes to the total input noise, this part of noise will be neglected in the analysis of this thesis for simplicity, since the transimpedance amplifier noise dominates.

Figure 2.1: Basic receiver front-end model [55]

2.2 Photodetectors

Before processed by the electronic circuitry, the signal-carrying light-wave traveling through a fiber needs to be transformed to an electrical signal by means of a photodetector. The photodetector plays a key role in the optical preamplifier design. The physical features of the photodetector, such as the efficiency of converting the light energy to proportional current, switching speed and the parasitic capacitance load at the input node of the transimpedance amplifier, set limitations to and render difficulties for the TIA circuit design [28] [80-83].

Figure 2.2: p-i-n photodetector [28]

The p-i-n photodetector is the simplest photodetector, which is also called p-i-n photodiode. The schematic illustration of a p-i-n photodiode is shown in Figure 2.2 [55]. A p-i-n photodiode is composed of a p-n junction with an intrinsic (un-doped or lightly doped) semiconductor layer inserted between the p and n doped material layers. The junction must be reverse biased to create a strong electric field in the intrinsic layer and this layer is almost completely depleted, giving a depletion region width of L [28].

Generally, the principle of a photodetector is that it relies on the absorption of photons in the depleted intrinsic region, which generates electron-hole (E-H) pairs. The E-H pairs are then separated and collected to the edges of the depletion region by the built-in electric field and the external field due to the reverse biasing [28]. In an ideal photodiode, every photon entering the device generates an E-H pair. However, in reality some photons are reflected from the surface or absorbed by semiconductor materials to produce heat. The fraction of photons that generate E-H pairs is called the *quantum efficiency* and is designated by η . Based on the concept of *quantum efficiency*, the electrical current i_{pd} produced by the photodetector for a given amount of incident optical power P_{op} is given by

$$i_{pd} = \eta \frac{\lambda q}{hc} P_{op} \quad (2.1)$$

where λ is the incident light wave-length, q is the electron charge, h denotes the Planck constant and c is the light speed.

The constant relating i_{pd} and P_{op} is called the responsivity of the photodetector and is represented by the symbol $\mathfrak{R}$:

$$i_{pd} = \mathfrak{R} P_{op} \quad (2.2)$$

with

$$\mathfrak{R} = \eta \frac{\lambda q}{hc} \quad (2.3)$$

Based on (2.3) we obtain

$$\mathfrak{R} = \eta \frac{\lambda}{124.3} \quad (2.4)$$

where the responsivity $\mathfrak{R}$ is in terms of Ampere per Watt (A/W), η is in terms of percentage and λ is terms of μm .

The responsivity of a typical InGaAs p-i-n photodiode is in the range from 0.6 to 0.9A/W [55]. Recent research developments show that the best responsivity of 10Gb/s photodetectors fabricated in CMOS compatible processes is around 0.3A/W [84-86]. Although the responsivity of a CMOS compatible photodetector is much lower, its integration advantage can help to circumvent the extra cost and parasitic capacitance caused by packaging and bonding. Figure 2.3 shows the equivalent small signal circuit of a bare photodetector [55]. The current source represents the current generated by the incident light. The main parasitics are the photodiode junction capacitance C_{pd} and the combination of contact and spreading

resistance R_{pd} . The parasitic capacitance C_{pd} for a 10Gb/s photodetector is usually around 100fF to 200fF. The parasitic resistance is usually around 10 to 20 Ohms. Therefore, we neglect this resistive part in our analysis for simplicity.

Figure 2.3: Small signal equivalent circuit for a 10Gb/s bare photodiode [55]

2.3 Performance of TIAs

In the following, we discuss the main design parameters that characterize a transimpedance front-end: the input referred noise, the input overload current, the transimpedance gain, the bandwidth and the group delay.

Figure 2.4: Input and output signals of a single-ended TIA

2.3.1 Gain, bandwidth and group delay

The transimpedance amplifier converts the input current signal i_i into an output voltage v_o , which is illustrated in Figure 2.4. The transimpedance is defined as the output voltage change per input current change:

$$Z_T = \frac{\Delta v_o}{\Delta i_i} \quad (2.5)$$

In general, it is desirable to make the transimpedance gain of a TIA as high as possible since a high transimpedance gain relaxes the gain and noise requirements for the subsequent main amplifier. However, the trade-off between gain and bandwidth is well known and it is always a design challenge to increase the gain-bandwidth product without degrading other performances such as the noise and dynamic range. Therefore, a system with higher bit rate usually provides lower transimpedance gain. Typical gain for a single-ended 10Gb/s transimpedance amplifier is around 50dB Ω to 60dB Ω [55]. Additional gain is to be obtained by the subsequent main amplifier that is beyond the scope of this thesis.

The transimpedance amplifier bandwidth is defined as the upper frequency at which the frequency dependent transimpedance gain $|Z_T(f)|$ dropped by 3dB below its midband value. This bandwidth is also called the -3dB bandwidth. Obviously, we need to make the bandwidth wide enough to prevent the signal waveform from being distorted by the intersymbol interference (ISI). However, wider bandwidth also translates to more noise picked up, which may corrupt the signal [28] [55]. There must be an optimum bandwidth due to the trade-off between the noise and distortion. For NRZ data pattern, the 92% of the signal power is contained in the frequency of 0.7 times of the bit rate R_b [87]. As a rule of

thumb, for NRZ receivers, the optimum -3dB bandwidth of the whole receiver front-end is about

$$f_{-3dB} \approx \frac{2}{3} R_b \quad (2.6)$$

As for the transimpedance amplifier alone, the -3dB bandwidth is usually chosen to be from $0.6 R_b$ to $0.7 R_b$ if the whole receiver bandwidth is determined by the TIA part [55]. Table 2.1 lists the cumulative power of the NRZ signal.

The optimum bandwidth alone does not guarantee the overall performance of the TIA. Even if the gain frequency response $|Z_T(f)|$ is flat up to sufficiently high frequency, distortions in the form of data dependent jitter may occur if the phase linearity of $Z_T(f)$ is not enough [55]. Hence, the group delay τ is used to measure the phase linearity:

$$\tau(\omega) = -\frac{d\Phi}{d\omega} \quad (2.7)$$

Typically, a group delay variation $\Delta\tau$ of less than $\pm 10\%$ of the bit rate over the specified bandwidth is required to limit the generation of data dependent jitter [55].

Table 2.1: Cumulative power of the NRZ signal [78]

$\frac{f}{R_b}$	Cumulative power of the NRZ signal	$\frac{f}{R_b}$	Cumulative power of the NRZ signal
0.6	86.9%	1.0	95.1%
0.7	92.0%	1.2	95.5%
0.8	94.3%	1.4	97.1%
0.9	95%	1.6	98.9%

2.3.2 Bit error rate and input referred noise

Random data bits must be sampled at their midpoints so that maximum distance from the decision threshold could be achieved to correctly detect the “1/0” values of the sampled bits. During the transmission and signal processing, noise is inevitably added to the signal. Together with other distortion factors such as the intersymbol interference (ISI), group delay and jitter, noise degrades both the signal amplitude and the time resolution, closing the eye and increasing the bit error rate (BER).

Figure 2.5: Eye diagram example of NRZ random data

The bit error rate is defined as the ratio of the number of error bits to the total number of transmitted bits. Figure 2.5 shows an example of the eye diagram, where we can observe that the amplitude noise will close the eye vertically and the time variation caused by group delay and jitter will close the eye horizontally [88-

89]. Assuming we are using distortion free NRZ data and that the noise is Gaussian and signal independent, the root mean square (RMS) value of the total equivalent input noise current $i_{n,eq}^{rms}$ of the transimpedance amplifier directly determines the front-end bit error rate [55]:

$$BER = Q\left(\frac{i_{in,pp}}{2i_{n,eq}^{rms}}\right) \quad (2.8)$$

where $i_{in,pp}$ is the peak-to-peak input current signal amplitude and

$$Q(x) = \int_x^{\infty} \frac{1}{\sqrt{2}} \exp\left(-\frac{u^2}{2}\right) du .$$

Table 2.2 lists the numerical relationship between the

value of $\mu = \frac{i_{in,pp}}{2i_{n,eq}^{rms}}$ and the bit error rate [2]. For 10Gb/s Ethernet and OC-192

standard, the required bit error rate is 10^{-12} .

Table 2.2: Numerical relationship between μ and bit error rate

μ	BER	μ	BER
0.0	0.5	5.998	10^{-9}
3.090	10^{-3}	6.361	10^{-10}
3.719	10^{-4}	6.706	10^{-11}
4.265	10^{-5}	7.035	10^{-12}
4.753	10^{-6}	7.349	10^{-13}
5.199	10^{-7}	7.651	10^{-14}
5.612	10^{-8}	7.942	10^{-15}

The equivalent input noise current source $i_{n,eq}$ is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actual noisy TIA does [55]. This equivalent input noise current, also called input referred

noise current, is usually measured in terms of power spectral density $i_{n,eq}^2$. The relationship between the input referred RMS noise current and the input referred noise current spectral density is expressed as

$$i_{n,eq}^{rms} = \frac{1}{R_T} \sqrt{\int_0^{>2BW} |Z_T(f)|^2 i_{n,eq}^2(f) df} \quad (2.9)$$

where $|Z_T(f)|$ is the transimpedance gain frequency response and R_T is its midband value. The integration is usually up to about two times of the TIA bandwidth (BW).

2.3.3 Sensitivity and overload

The sensitivity is defined as the minimum input signal level that is required to achieve a given bit error rate. It is one of the key characteristics of an optical receiver that can tell the minimum detectable signal level after transmission attenuation and hence plays an important role in optical link budget determination. For an optical receiver front-end, sensitivity can be defined both in the electrical domain and optical domain [55].

The electrical receiver sensitivity $i_{sens,pp}$ is defined as the minimum peak-to-peak signal current at the input of the receiver necessary to obtain a given bit error rate. For a given bit error rate, there is a corresponding Q value which is listed in Table 2.2. According to (2.8) we have

$$i_{sens,pp} = 2i_{n,eq}^{rms} \mu \quad (2.10)$$

The optical receiver sensitivity $\bar{P}_{sens}$ is defined as the minimum average optical power incident into the photodetector necessary to achieve a given bit error rate.

For DC balanced signal, according to (2.2) and (2.10), we obtain [55]

$$\overline{P}_{sens} = \frac{i_{n,eq}^{rms} \mu}{\Re} \quad (2.11)$$

Table 2.3 summarizes the receiver sensitivity and overload specifications for SONET OC-192 and 10Gb/s Ethernet short distance standards. For 10Gb/s Ethernet and OC-192 standards, the required bit error rate is 10^{-12} [25-26]. For large input signal current levels, many transimpedance amplifiers produce severe pulse-width distortion and jitter. These undesirable distortions cause the bit error rate of the receiver to increase rapidly as the input power increases. When the input signal reaches a certain critical level, the BER will exceed the specified value and this critical signal current, measured in peak-to-peak, is called the input overload current $i_{ovl,pp}$. According to the preceding discussion, the relationship between the input overload current and the input overload power is

$$\overline{P}_{ovl} = \frac{i_{ovl,pp}^2}{2\Re} \quad (2.12)$$

Table 2.3: Optical sensitivity and overload specifications [25-26]

Standard	Sensitivity (dBm)	Overload (dBm)	Reach	Application
10Gb/s Ethernet	-9.9	-1	2~300m	VSR
	-14.4	1.5	2~10km	LAN
	-15.8	-1	2~40km	LAN and MAN
Very Short Reach (VSR) SONET OC-192C	-16	-3	0~300m	VSR in Central Office

2.4 TIA specifications

According to the previous discussion in Section 2.3, the electrical specifications of transimpedance amplifiers based on the standards listed in Table 2.3 are tabulated in Table 2.4. A CMOS compatible photodetector with a responsivity of 0.3A/W is assumed in calculation.

Table 2.4: Electrical specifications for 10Gb/s TIAs based on a 0.3A/W PD

Standard	Sensitivity (pA/sqrtHz)	Overload (mA)	RMS input referred noise current (μ A)	Bandwidth/ Power/ Gain	Reach
10Gb/s Ethernet	61.4	0.48	4.36		2~300m
	21.8	0.85	1.55		2~10km
	15.8	0.48	1.12		2~40km
Very Short Reach (VSR) SONET OC-192C	15.1	0.3	1.07	BW>6GHz Power<20mW Gain>50dB Ω	0~300m

2.5 TIA circuit concepts

In this section, we discuss some general TIA circuit concepts including basic preamplifier topologies, adaptive transimpedance, voltage mode TIA and current mode TIA.

2.5.1 Basic preamplifier topologies

The choice of preamplifier topologies has important impact on the receiver front-end performances. Different front-end topology entails different design challenges and trade-offs.

Figure 2.6: (a) Low impedance front-end, (b) high impedance front-end and (c) shunt feedback transimpedance front-end

Figure 2.6 shows the three commonly used optical receiver front-end topologies [90]. In the case of low impedance front-end illustrated in Figure 2.6 (a), which is the simplest optical receiver front-end realization and was once widely used, the photodetector current is converted to voltage at the input node by a small resistor R_l (typically 50Ω). The converted voltage signal $v_i = i_{pd} R_l$ is further amplified by a voltage amplifier. Due to this very small input resistance, the effect of the parasitic capacitance at the input node is negligible. Therefore, such topology is able to achieve respectable bandwidth. However, the drawbacks of the low impedance topology are also obvious. First, the converted voltage signal $v_i = i_{pd} R_l$ is very small. Second, it suffers from poor sensitivity due to the thermal resistor noise $i_{n,res} = \sqrt{4KT / R_l}$, which is about $18 pA / \sqrt{Hz}$ with $R_l = 50\Omega$.

In the case of high impedance front-end illustrated in Figure 2.6 (b), the gain and noise problem encountered by low impedance front-end is overcome by using an input resistor with a high resistance value. However, if the input resistance R_h is set to 500Ω , which is a reasonable value for the transimpedance gain of a 10Gb/s TIA, the parasitic capacitance at the input node cannot be neglected. The pole

determined at the receiver input node $R_h C_{parasitic}^{-1}$ is as low as 0.66GHz with a total input parasitic capacitance of 250fF, which is much lower than the necessary bandwidth of a 10Gb/s system. It is difficult to achieve the required bandwidth even with a following bandwidth extension amplifier [55].

Among the three topologies, the shunt feedback transimpedance front-end [43-45] [92-97] is by far the most popular circuit for converting the photodiode current into a voltage signal due to its ability to optimally solve the noise, gain and bandwidth trade-off problems at the receiver front-end. The circuit of the basic shunt-feed back TIA is shown in Figure 2.6 (c), which is essentially a negative current-voltage feedback (shunt-shunt) topology. Due to the negative feedback effect, the input resistance is expressed by

$$R_i = \frac{R_f}{1 + A} \quad (2.13)$$

The low frequency transimpedance gain (trans-resistance) is

$$R_T = \frac{A}{1 + A} R_f \quad (2.14)$$

Suppose the total parasitic capacitance at the input node is C_i and the dominant pole of the circuit is determined at the input node, which is expressed by

$$\omega_i = \frac{1}{R_i C_i} = \frac{1 + A}{R_f C_i} \quad (2.15)$$

Assuming the bandwidth of the core amplifier is infinite, which means the core amplifier gain $-A$ is frequency independent, we can express the frequency-dependent transimpedance (transfer function) as

$$Z_T(s) = -R_T \frac{1}{1 + s / \omega_i} \quad (2.16)$$

If the gain of the core amplifier $-A$ is large enough, then $R_T \approx R_f$. It is observable that by using shunt-shunt negative feedback, we can have a large transimpedance R_f (high gain and low noise) and maintain a low input resistance $R_i = \frac{R_f}{1+A}$ (wide bandwidth) at the same time.

However, the core amplifier that is assumed to have infinite bandwidth in the previous discussion could not be realized in reality. If we assume the core amplifier has a single dominant pole ω_0 . The transfer function is turned into a typical second order system expressed by

$$Z_T(s) = -R_T \frac{1}{1 + s/(\omega_n Q) + s^2/\omega_n^2} \quad (2.17)$$

where

$$\omega_n = \sqrt{\frac{1+A}{R_f C_i}} \omega_0 = \sqrt{\omega_i \omega_0} \quad (2.18)$$

$$Q = \frac{\sqrt{(1+A)R_f C_i \omega_0}}{1 + R_f C_i \omega_0} = \frac{\sqrt{\frac{R_f C_i}{1+A}} \omega_0}{\frac{1}{1+A} + \frac{R_f C_i}{1+A} \omega_0} \approx \sqrt{\frac{\omega_i}{\omega_0}} \quad (2.19)$$

According to (2.19), if ω_0 is much higher than ω_i , (2.17) can be simplified to (2.16). As ω_0 gets closer to ω_i , the transfer function characteristic exhibits peaking and ringing of a typical second-order system. Two values for Q (quality factor) are of particular interest. For $Q = 1/\sqrt{3}$, the transfer function exhibits *Bessel* response that provides maximally flat group delay and negligible overshoot in time domain. For $Q = 1/\sqrt{2}$, the transfer function exhibits *Butterworth* response, which provides maximally flat gain frequency response ($|Z_T(f)|$) without any peaking and some

overshoot in the time domain. For larger values of Q , peaking, overshoot and ringing become progressively worse.

In the case of a *Butterworth* response, where $\omega_0 \approx 2\omega_i$, the -3dB bandwidth of the TIA is given by

$$f_{-3dB} = \frac{1}{2\pi} \omega_n \approx \frac{1}{2\pi} \sqrt{2} \omega_i \quad (2.20)$$

By comparing (2.15) with (2.20), we find that the bandwidth is extended by 41%. From the analysis of the second order TIA model, we can see one way of bandwidth extension is to bring two poles in adjacent to each other and thereby an inductive behavior is created [28] [55]. More bandwidth extension methods will be studied in detail in the next chapter.

2.5.2 Automatic gain control

The upper end of the dynamic range of a TIA is defined by its overload current and the lower end is defined by its sensitivity. The concept of *adaptive transimpedance* or *Automatic Gain Control* (AGC) is raised as a counter-measurement to the optical overload [28] [55]. The idea is to ensure the TIA gain is adaptive in accordance to the input signal level. The signal amplitude is monitored at some stage and compared with a reference. The transimpedance gain is adjusted continuously in such a way that the output level remains relatively constant or increase very slowly when the input current level is high. However, for weak input signal levels, it is necessary to disable the adaptive transimpedance mechanism to ensure good sensitivity performance.

For the basic shunt-feedback TIA discussed previously, both overload and sensitivity are related to the shunt feedback resistor R_f . Therefore, the dynamic range can be extended by making this feedback resistor adaptive to the input signal strength, decreasing it continuously when the input power is high while maintaining a high resistance value when input power is low. Such an automatic gain control model is illustrated in Figure 2.7 (a) [55].

Figure 2.7: TIA with automatic gain control using a (a) variable feedback resistor and (b) variable input shunt resistor

An alternative to the above-mentioned TIA with adaptive feedback resistor is the TIA with adaptive (variable) input shunt resistor, which is shown in Figure 2.7 (b). Similar to the previous case, the shunt resistance is decreased continuously when the input signal level is high to divert some of the overloading photodetector current to ground. The resistor needs to maintain a high resistance value or even cut off when the input signal is weak in order not to affect the sensitivity performance. As a result of varying R_s , the trans-resistance is expressed as

$$R_T = \frac{A}{1 + A + (R_f / R_s)} R_f \quad (2.21)$$

In both cases, the variable shunt resistor can be implemented with an FET (field effect transistor) operating in the linear region.

2.5.3 Voltage mode TIAs

The shunt-feedback TIA illustrated in Figure 2.6(c) is a typical model of voltage mode amplifier in which the core amplifier is a pure voltage amplifier without input current buffer. The input current i_i is first converted to a voltage signal

$$v_i = i_i \frac{R_f}{1 + A} \text{ and then amplified by the voltage amplifier to } v_o = -\frac{A}{1 + A} i_i R_f.$$

In other words, if the TIA input stage is neither based on a current buffer nor configured as a current amplifier (mirror), such a TIA topology is called voltage mode.

Figure 2.8: Typical voltage mode TIA implementations: (a) Common source TIA and (b) common drain TIA

In reality, the voltage mode TIAs are commonly implemented using common source or common drain configurations with shunt-feedback at the input node. Their typical circuit implementations are shown in Figure 2.8 (a) and Figure 2.8 (b)

respectively [28] [98-99] and the analysis methods in Section 2.5.1 is readily applicable.

The voltage amplifier used in the voltage mode TIA usually has very high input impedance because of the gate of the input MOS transistor. The sizing of the input transistor is very critical with regard to the trade-offs between bandwidth, noise and gain. The sizing of this input transistor for optimum noise performance has been studied in detail in [90] [100-101]. In voltage mode low-noise high-speed preamplifier designs, three critical roles, i.e. the photodiode parasitic capacitance, the feedback resistance and the input transistor of the voltage amplifier are presented at the input node simultaneously. The trade-offs between bandwidth, gain and noise of the whole TIA circuit are brought together at the input node, presenting severe challenges while dealing with high-speed low-noise TIA designs based on the voltage mode topology especially when CMOS technology is used.

2.5.4 Current mode TIAs

According to the above discussion, the voltage mode transimpedance amplifier transforms current signal into voltage in the first step and proceed to voltage amplification in the second step. The size of the input transistor, feedback resistor and photodiode are three critical elements that decide the front-end performance. In such configuration, the core voltage amplifier presents high impedance at the input node, renders the bandwidth very sensitive to the input capacitive loading, gain of the core amplifier and the feedback resistor. On the other hand, current mode transimpedance amplifiers, which adopt the current buffer or current amplifier (current mirror) as the input stage, are able to provide very low input impedance. This low input impedance helps to isolate the relatively large input

capacitance from bandwidth determination and relax the design trade-offs at the input node. The design and performance of current mode TIAs have been studied extensively in [55] [62] [102-108]. Typical current mode TIA design implementations based on current buffer (common gate input stage) and current amplifier (current mirror) are illustrated in Figure 2.9 (a) and Figure 2.9 (b) respectively.

Figure 2.9: Current mode TIAs based on (a) common base input stage and (b) current mirror

In the case of common gate input transimpedance amplifier in Figure 2.9 (a), the input resistance is about $1/g_m$ that can be designed to be quite small. Moreover, the parasitic capacitance contributed by the photodetector is separated from the input capacitance of the voltage amplifier by the current buffer. Therefore, the determination power on the TIA bandwidth by the input node is greatly reduced. However, because the transimpedance gain is in large part determined by the effective impedance at node x , shunt-feedback is still necessary to achieve a relative high gain without affecting the bandwidth performance. In recent multi-gigabit/s applications, regulated cascode (RGC) input stage [63-65] and common gate feed-forward input stage [66] are used as more efficient low input impedance

configurations to replace the common gate topology as the input stage of current mode TIA circuits. Their characteristics and performances will be discussed in detail in the next section.

In the case of current mirror based transimpedance amplifier in Figure 2.9 (b), the small-signal low frequency input resistance turns out to be $\frac{1}{(1+A)g_m}$, which is advantageous over the common gate case. However, the large parasitic capacitance contributed by the photodetector and the gate capacitance of M_1 and M_2 are not separated. Hence, the parasitic capacitance is also larger with a higher current gain, which is a drawback compared to the common gate topology.

The primary drawback of current mode TIAs is that more noise sources are introduced at the input node than the voltage mode counterpart, which entails careful design optimizations on noise reduction [55]. The noise reduction techniques using series input inductors will be analyzed in detail in Chapter 3.

2.6 Broadband Design Techniques

2.6.1 Regulated cascode (RGC) input stage

The regulated cascode (RGC) input stage is a more suitable candidate for high-speed current-mode TIAs than the common gate (CG) input stage. The reason is that the RGC input stage incorporates strong local negative feedback to realized very low input impedance. Therefore, the influence on the TIA bandwidth by the relatively large input capacitance including the photodetector capacitance can be greatly reduced. The RGC input stage in Figure 2.10 (a) is well suited for

broadband TIA design by its very low input impedance [63-65], which could be derived from the small-signal circuit model in Figure 2.10 (b) as

$$Z_{in}(s) \approx \frac{\left(\frac{1}{R_2} + sC_j \right)}{\left(g_{m2} + \frac{1}{R_2} \right) \left(g_{m1} + sC_j \right) + \left(\frac{1}{R_2} + sC_j \right) \left(\frac{1}{R_s} + sC_i \right)} \quad (2.22)$$

where $C_i \approx C_{sb1} + C_{gs2}$ and $C_j \approx C_{gs1} + C_{gd2}$. The low-frequency small-signal input resistance is given by

$$r_i = Z_{in}(0) \approx \frac{1}{g_{m1}(1 + g_{m2}R_2)} \quad (2.23)$$

This very small input resistance in large part isolates the input parasitic capacitance from bandwidth determination. Therefore, unlike common gate or common source TIAs, the dominant pole of an RGC TIA is usually located within the amplifier rather than at the input node [63].

Figure 2.10: Regulated cascode stage: (a) its circuit schematic and (b) its small-signal model

2.6.2 Capacitive degeneration

Besides pushing the dominant pole to higher frequencies to increase the bandwidth, it is also possible to compensate the dominant pole with a zero. This

could be accomplished by capacitive degeneration. The capacitive degeneration, in essence, is to degenerate the transistor at the source so that when frequency increases, the effective transconductance also increases to counter the gain roll-off effect due to the pole. As shown in Figure 2.11, the voltage gain of a capacitive degeneration stage is given by [28] [55]

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}R_1}{1 + g_{m1}R_s} \frac{1 + sR_sC_s}{1 + s \frac{R_sC_s}{1 + g_{m1}R_s}} \quad (2.24)$$

According to (2.24), the capacitive degeneration stage contributes a zero at $(R_sC_s)^{-1}$ and a pole $\left(\frac{R_sC_s}{1 + g_{m1}R_s}\right)^{-1}$ at a higher frequency. The zero could be used to compensate the dominant pole of the circuit. The -3dB cut-off frequency is therefore determined by the second lowest pole of the circuit. Besides bandwidth extension, the noise contribution of the capacitive degeneration stage at high frequency is also small, which will be analyzed in Chapter 3. The drawback of this topology is also obvious that the gain of this stage is degenerated.

Figure 2.11: Gain stage with capacitive degeneration

2.6.3 Shunt inductive peaking

It is well known that inductors are widely used in narrow-band filters. With the advancement in high frequency communications, they are also found useful in wideband applications to enhance the bandwidth of a broadband amplifier. Inductive bandwidth peaking are extensively used in broadband circuits to obtain additional high-speed performance especially after the advent of monolithic inductors [69-71]. A simple schematic demonstrating the application of shunt inductive peaking in a common source gain stage is illustrated in Figure 2.12 [69]. The idea is to allow the capacitance that limits the bandwidth to resonate with the inductor, thereby improving the speed. The peaking inductor is usually used at the node where the dominant pole is located. Comparing to the capacitive peaking that brings one pole close to the dominant pole to generate a gain peak, inductive peaking also has tuning effect on high frequency noise while capacitive peaking degrades the high frequency noise performance.

Figure 2.122: (a) Common source amplifier with shunt inductive peaking and (b) its small-signal circuit [69]

The transfer function of this simple circuit is easily derived, which is given by

$$\frac{v_{out}}{v_{in}} = -g_m \frac{R + sL}{1 + sC(R + sL)} = -\frac{g_m R}{LC} \frac{1 + s\frac{L}{R}}{s^2 + s\frac{R}{L} + \frac{1}{LC}} = -\frac{g_m R}{LC} \frac{1 + s\frac{L}{R}}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.25)$$

where $\omega_n = (LC)^{-\frac{1}{2}}$ and $\xi = \frac{1}{2} \frac{RC}{\sqrt{LC}} = \frac{1}{2} \frac{\omega_n}{\omega_0}$ with $\omega_0 = (RC)^{-1}$. Assuming the zero

$\frac{R}{L}$ in (2.25) is negligible and let the damping ratio $\xi = \frac{1}{2} \frac{\omega_n}{\omega_0} = \frac{1}{\sqrt{2}}$, we

obtain $\omega_{-3dB} = \omega_n = \sqrt{2}\omega_0$. The bandwidth is therefore extended by 41%. However,

based on the above assumption the zero frequency $\frac{R}{L} = \frac{2}{RC} = 2\omega_0$, which is not

much higher than the -3dB bandwidth. Therefore, this zero shall be considered in the frequency analysis. For maximally-flat gain frequency response, the optimum value is $L = 0.4R^2C$. To achieve a flat group-delay response, the optimum value is $L = 0.32R^2C$. Table 2.5 shows the bandwidth enhancement and gain overshoot at different damping ratios when the effect of the zero is considered [28] [55] [69].

Table 2.5: Characteristics of shunt inductive peaking [28] [55]

Damping ratio	0.88	0.79	0.69	0.64	0.59
Gain overshoot	Flat group delay without overshoot	Maximum flat gain without overshoot	5%	7.5%	10%
Bandwidth enhancement	60%	70%	78%	82%	84%

2.6.4 Series inductive peaking

Besides the bandwidth enhancement method of “shunt inductive peaking,” it is also possible to utilize inductive peaking in series with the input of the TIA circuit or in between two stages. Besides bandwidth enhancement, the series inductor also helps to improve the noise performance. The series inductive peaking and noise reduction effects have been studied in details in [55] [71] [74]. The series inductive peaking with a single inductor can be regarded as the simplest broadband matching network. Figure 2.13 shows a typical TIA model with a single series input inductor. Assuming the core amplifier has an infinite bandwidth. The transfer function of this topology could be written as

$$Z_T(s) = -AR_{ff} \frac{1}{1 + s(C_1 + C_2)R_{ff} + s^2 LC_1 + s^3 LC_1 C_2 R_{ff}} \quad (2.26)$$

where $R_{ff} = \frac{R_f}{1+A}$. To avoid peaking and ringing, the maximally-flat gain frequency response is achieved when (2.26) satisfies the requirement of a third-order Butterworth transfer function:

$$(R_{ff} C_1)^{-1} = \frac{2}{3} \omega_0 \quad (2.27)$$

$$(R_{ff} C_2)^{-1} = 2 \omega_0 \quad (2.28)$$

$$(LC_1)^{-1} = \frac{1}{2} \omega_0^2 \quad (2.29)$$

The -3dB cut-off frequency of (2.26) is $f_{-3dB} = \omega_0 / 2\pi$. Without the series inductive peaking, the -3dB bandwidth of the TIA is $[2\pi R_{ff} (C_1 + C_2)]^{-1} = \omega_0 / 4\pi$. Therefore, the bandwidth is extended by 100% with a Butterworth frequency response. The inductor in Figure 2.13 can be replaced by a more general low pass L - C ladder matching network, which will be analyzed in detail in the next section.

Figure 2.13: TIA with a single series input inductor

2.6.5 Broadband matching networks

The simplest way that we increase the bandwidth of an existing amplifier topology is to increase the -3dB cut-off frequency of each gain stage, which is often accomplished by decreasing the respective resistive load. Smaller resistive load leads to lower gain and higher thermal noise current. Since the gain and sensitivity of a front-end amplifier counts to the communication distance directly, it is desirable to maintain a constant gain while pushing the cut-off frequency higher. Passive matching networks could be used to explore the gain-bandwidth limitation without degrading other performances of an existing amplifier [117]. The principle of increasing the gain-bandwidth product is to maintain a constant load over a wider frequency range. This can be realized by a *constant-k* filter, which means the pass-band gain of the filter is constant. The *L-C* ladder filter in Figure 2.14 is such a realization. Based on Bode-Fano Limit, it is proven [55] [70] [117] that the maximum obtainable gain-bandwidth product enhancement is four times by a two port passive matching network. In other words, the bandwidth could be at most extended to four times of the original amplifier with the gain unchanged. In fact, a more systematic analysis shows that the maximum bandwidth

enhancement ratio obtainable by a two-port broadband matching network is even greater than four, namely $\pi^2 / 2 = 4.93$ [55].

Figure 2.14: Small-signal model of an n -th order L - C ladder filter

It is notable that four times is the maximum obtainable enhancement. With finite sections of L - C ladders, the maximum bandwidth extension ratio is achievable with significant gain peaking/ripple at the same time. It is hence desirable to design the filter with sufficient bandwidth enhancement and maximum gain flatness (Butterworth-type response). In the case of the two port matching network in Figure 3.5, which is designed to exhibit an n -th order Butterworth characteristic, the power gain of this filter must satisfy [117]

$$|S_{21}(j\omega)|^2 = \frac{K_n}{1 + \left(\omega/\omega_c\right)^{2n}} \quad (2.30)$$

where K_n is the DC gain and ω_c is the cutoff frequency. It is derived that, to satisfy (2.30), the impedance matching condition is given by [117]

$$Z_{11}(s) = R_1 \frac{q(y) - \delta^n q(y/\delta)}{q(y) + \delta^n q(y/\delta)} \quad (2.31)$$

where $y = s/\omega_c$, $\delta = \sqrt[n]{\frac{R_1 - R_2}{R_1 + R_2}}$ and $q(y)$ is the Butterworth polynomial defined as

$$q(y) = \sum_{m=0}^n a_m y^m \quad (2.32)$$

where the coefficients a_m follow a recursion formula that is given by

$$\frac{a_{k+1}}{a_k} = \frac{\cos(k\pi/2n)}{\sin[(K+1)\pi/2n]}, k = 0, 1, 2, \dots, n-1. \quad (2.33)$$

Looking into node 1 in Figure 2.14, the input admittance of the two-port broadband matching network can be written as

$$\frac{1}{Z_{11}} = sC_1 + \frac{1}{sL_2 + \frac{1}{\dots sL_{n-1} + \frac{1}{sC_n + \frac{1}{R_2}}}} \quad (2.34)$$

Comparing (2.31) with (2.34) and following the recursion formula given by (2.33), the L - C elements can be computed. The detailed derivation can be found in [117].

2.6.6 Common gate feedforward input stage

With the geometric scaling down trend of the deep submicron CMOS devices, the supply voltage has also been reduced to prevent the transistor from breaking down and to save power in VLSI digital systems. However, the threshold voltage cannot be scaled down at the same ratio, which brings about severe design challenges in low power CMOS circuit design.

Conventional RGC topology (Figure 2.10) also suffers from the above-mentioned problem when it is used for low-power high-speed CMOS TIA design. The voltage swing headroom at the RGC input stage is quite stringent. A modified regulated cascode topology called common gate feedforward topology is introduced by [66] to circumvent the problem, which is shown in Figure 2.15. Comparing to the conventional RGC stage, transistor M_3 has been inserted as a pass transistor to shift the gate voltage of M_2 to a higher level. From another point

of view, M_3 is employed in the form of a common gate gain stage, and this gain-enhancing feedforward path boosts the local feedback to reduce the input impedance [66]. Therefore, this modified RGC stage is also called the common gate feedforward stage. The low frequency input resistance of the RGC circuit is given by

$$r_i = Z_{in}(0) \approx \frac{1}{g_{m1}(1 + g_{m2}g_{m3}R_2R_3)} \quad (2.35)$$

Figure 2.15: Common gate feedforward TIA input stage

Comparing (3.35) with (3.23), we can observe that the common gate feedforward configuration provides an even lower input resistance. The disadvantage is also obvious that this topology employs more devices in the signal path and hence more noise sources are added, which makes the noise optimization more complicated. Because this topology enables excellent high-speed performance while suffers from additional noise problem, it is quite suitable for

short-range optical links, where the optical incident power is usually high and the sensitivity requirement is not very stringent [66]. The transfer function of the TIA input stage could be roughly written as

$$Z_T(s) \approx \frac{g_{m1} \left[g_{m2} g_{m3} + \left(\frac{1}{R_2} + sC_2 \right) \left(\frac{1}{R_3} + sC_3 \right) \right]}{\left(\frac{1}{R_1} + sC_o \right) \left[\left(\frac{1}{R_2} + sC_2 \right) \left(\frac{1}{R_3} + sC_3 \right) \left(\frac{1}{R_s} + g_{m1} + g_{m3} + sC_1 \right) + g_{m2} g_{m3} (g_{m1} + sC_{gs1}) \right]} \quad (2.36)$$

where $C_o \approx C_{gd1} + C_L$, $C_1 \approx C_{pd} + C_{gs1} + C_{sb1} + C_{gs3} + C_{sb3}$, $C_2 \approx C_{gd2} + C_{db2} + C_{gs1}$ and $C_3 \approx C_{gd3} + C_{db3} + C_{gs2}$.

2.7 Noise analysis basics

According to the discussion and introduction in Section 2.3, the noise performance is extremely important for front-end circuits. This is because the equivalent input noise current of the optical preamplifier contributes to the total system noise without suppression and determines the input sensitivity of the optical receiver directly. In optical receivers, the preamplifier usually begins with a transimpedance stage, which transforms weak input current to voltage for further amplification by subsequent voltage gain stages. The noise performance of optical preamplifiers is usually measured by the equivalent input noise current. The equivalent input noise current source $i_{n,eq}$ is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actual noisy TIA does. This equivalent input noise current, also called input referred noise current, is usually measured in terms of power spectral density $i_{n,eq}^2$. Figure 2.16 (a) shows a typical transimpedance front-end noise model, where we have a noiseless TIA circuit with transimpedance gain of Z_T . For a certain output noise $v_{n,o}$ that is produced by the noise sources of the preceding stages, we obtain

$$\overline{i_{n,eq}^2} = \overline{v_{n,o}^2} \left| \frac{Z_s + Z_{in}}{Z_T Z_s} \right|^2 \quad (2.37)$$

Figure 2.16: (a) TIA noise model based on equivalent input noise current and (b) E_n - I_n pair

Although the TIA noise model can be conveniently represented by a noise current source only, the equivalent input noise current is dependent on the source impedance, which is mainly determined by the photodiode capacitance and the input matching network if there is one [55]. Therefore, standard noise analysis in terms of E_n - I_n noise pair (both noise voltage and noise current sources are present) [109] is necessary to evaluate the influence of the input matching network on noise. Figure 2.16 (b) shows the E_n - I_n noise model for the same TIA circuit in Figure 2.16 (a). E_n is a zero impedance noise voltage generator and I_n is an infinite impedance noise current generator [109]. Based on Figure 2.16 (b) and regarding these noise sources as linear voltage/current signals, we obtain

$$\frac{Z_T}{Z_s + Z_{in}}(E_n + Z_s I_n) = v_{n,o} \quad (2.38)$$

According to (2.38), E_n can be measured by setting $Z_s=0$ (short circuit) and I_n can be measured by setting $Z_s= \infty$ (open circuit). Therefore, for a given E_n - I_n noise model, E_n - I_n are independent on the source impedance characteristics. However, they are typically frequency dependent. For signals, linear voltage and current division and superposition principles can be applied. However, for noise calculation, each noise contribution must be summed up in mean square values.

Therefore, we obtain

$$\begin{aligned} \overline{v_{n,o}^2} &= \left| \frac{Z_T}{Z_s + Z_{in}} \right|^2 |E_n + Z_s I_n|^2 \\ &= \left| \frac{Z_T}{Z_s + Z_{in}} \right|^2 \left[\overline{E_n^2} + |Z_s|^2 \overline{I_n^2} + E_n (Z_s I_n)^* + (E_n)^* Z_s I_n \right] \\ &= \left| \frac{Z_T}{Z_s + Z_{in}} \right|^2 \left[\overline{E_n^2} + |Z_s|^2 \overline{I_n^2} + (c Z_s + c^* Z_s^*) \sqrt{\overline{E_n^2} \overline{I_n^2}} \right] \end{aligned} \quad (2.39)$$

where $c = \frac{\overline{I_n E_n^*}}{\sqrt{\overline{E_n^2} \overline{I_n^2}}}$ is the correlation coefficient. Usually we can assume c to be

zero with little error [109]. By this assumption and according to (2.38) and (2.39), we obtain

$$\overline{i_{n,eq}^2} = \overline{I_n^2} + \frac{\overline{E_n^2}}{|Z_s|^2} \quad (2.40)$$

where we can see that the equivalent input noise current is not constant and dependent on the input matching conditions and the source impedance.

2.7.1 Noise model of MOSFET

There are three principle noise sources in MOSFET identified as shot noise $\overline{i_{n,g}^2}$ that is due to the gate leakage current, flicker noise $\overline{i_f^2}$ and drain-source channel

thermal noise $\overline{i_{n,d}^2}$. These three noise components in the form of power spectral density could be expressed mathematically by [110-111]

$$\overline{i_{n,g}^2} = 2qI_g \quad (2.41)$$

$$\overline{i_f^2} = \frac{K_F}{C_{ox}WLf} \quad (2.42)$$

$$\overline{i_{n,d}^2} = 4KT\gamma g_{d0} = 4KT \frac{\gamma}{\alpha} g_m \quad (2.43)$$

where q stands for the electron charge, I_g is the gate leakage current, K_F is dependent on devices and can vary widely for different devices in the same process, $[W, L$ and $C_{ox}]$ represent the transistor's width, length and gate capacitance per unit area respectively, K is the Boltzmann constant, T is the absolute temperature, γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance and $\alpha = \frac{g_m}{g_{d0}}$. For long channel devices, $\gamma=2/3$ and $\alpha=1$. For short channel devices, γ can be much greater than 1 and $\alpha<1$ [110-113].

The dominant noise source for MOSFETs in wideband applications is the channel thermal noise. At radio frequencies, the channel thermal noise current will be coupled to the gate terminal through the gate-oxide capacitance and this coupled noise is called the induced gate noise. This induced noise source can not be neglected at very high frequencies. The van der Ziel MOSFET model [110] shown in Figure 2.17 is well accepted and the induced gate noise in the form of power spectral density is expressed as

$$\overline{i_g^2} = 4KT\delta g_g \quad (2.44)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (2.45)$$

Figure 2.17: The van der Ziel thermal noise model of a MOSFET

Typically, δ is 4/3 for long-channel devices and increases in short-channel devices. The induced gate noise is partially correlated with the drain thermal noise. The correlation coefficient c is expressed by

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \overline{i_d^2}}} \quad (2.46)$$

The value of the correlation coefficient is theoretically $c = -0.395j$ for long channel MOSFETs for noise current polarities shown in Figure 2.18, where the drain noise current flows from the drain to the source and the gate noise flows from the source to the gate. For short channel MOSFET, the magnitude of the correlation coefficient $|c|$ can take an abstract value of more than 0.75 [101].

According to recent research works, although the induced gate noise of the input transistors of CMOS TIAs adds directly to the total input referred noise current, the correlated noise cancels the equivalent input noise due to the channel thermal noise. This means the channel thermal noise is shorted out by the gate capacitance and hence the total noise at the input is reduced. According to numerical data, the input referred noise current reduction for *optimum* transistor size is about 10% to 20% [101].

Figure 2.18: The small-signal circuit thermal noise model of a MOSFET

2.7.2 Noise analysis of shunt-feedback common source TIA input stage

The first stage of an amplifier is, in most cases, responsible for the noise performance of the whole receiver. The shunt-feedback common source TIA input stage and its small-signal circuit for noise analysis is shown in Figure 2.19, where $C_i \approx C_{pd} + C_{sb}$, $C_o \approx C_L + C_{db}$.

Figure 2.19: Schematic of the shunt feedback common source TIA input stage and its small signal circuit

According to Figure 2.19, the induced gate noise adds directly to the input. The equivalent input noise current spectral density contributed by the feedback resistor R_f is roughly

$$N_{n,Rf} \approx \frac{4KT}{R_f} \left(1 + \frac{1}{g_m^2 |Z_{in}|^2} \right) \quad (2.47)$$

The equivalent input noise current spectral density contributed by R_I is given by

$$N_{n,R1} \approx \frac{4KT}{R_1} \frac{1}{g_m^2 |Z_{in}|^2} \quad (2.48)$$

The equivalent input noise current spectral density contributed by the transistor drain noise is roughly

$$N_{n,d} \approx 4KT \gamma g_{d0} \frac{1}{g_m^2 |Z_{in}|^2} \quad (2.49)$$

Because the gate noise and the drain noise are correlated, the equivalent input noise current spectral density contributed by the correlated noise is given by [110] [114]

$$N_{n,c} = \overline{i_g} \frac{\overline{i_d^*}}{g_m Z_{in}^*} + \overline{i_g^*} \frac{\overline{i_d}}{g_m Z_{in}} = \frac{c}{Z_{in}^*} \frac{\sqrt{\overline{i_g^2 i_d^2}}}{g_m} + \frac{c^*}{Z_{in}} \frac{\sqrt{\overline{i_g^2 i_d^2}}}{g_m} \quad (2.50)$$

where Z_{in} is the input impedance (the effect of R_f on the input impedance is neglected here for simplicity). The total equivalent input noise current spectral density based on (2.47) to (2.50) is about

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \frac{1}{R_f} \left(1 + \frac{\omega^2 C_{in}^2}{g_m^2} \right) + \frac{\omega^2 C_{in}^2}{g_m^2} \left[\frac{1}{R_1} + \gamma g_{d0} \left(1 - \frac{C_{gs}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] + \delta \frac{\omega^2 C_{gs}^2}{5g_{d0}} (1 - |c|^2) \right\} \quad (2.51)$$

where C_{in} is the sum of C_i , C_{gs} and the Miller capacitance of C_{gd} . According to (2.36), although the induced gate noise of the input transistor of CMOS TIAs adds directly to the total input referred noise, the correlated noise cancels the total equivalent noise. In deep submicron devices, the magnitude of the correlation

coefficient can take a value of more than 0.75, which can help to reduce the total input noise significantly for *optimum* transistor size according to (2.51) and [101].

2.7.3 Noise analysis of common gate TIA input stage

As discussed in Section 2.5.4, the primary drawback of current mode TIAs is that more noise sources are introduced at the input node than the voltage mode counterpart, which entails careful design considerations on noise reduction. In this section, we will derive the mathematical approximation of the equivalent input noise current spectral density of a typical common gate TIA input stage as an example of noise analysis. The common gate TIA input stage and its small-signal circuit for noise analysis is shown in Figure 2.20, where $C_1 \approx C_{gs} + C_{sb}$, $C_2 \approx C_{gd} + C_{db}$. According to Figure 2.20, the induced gate noise and the equivalent input noise current spectral density contributed by the feedback resistor R_s add directly to the input. The equivalent input noise current spectral density contributed by R_I is given by

$$N_{n,R1} \approx \frac{4KT}{R_1} \frac{1}{g_m^2 |Z_{in}|^2} \approx \frac{4KT}{R_1} \left(1 + \frac{\omega^2 C_{in}^2}{g_m^2} \right) \quad (2.52)$$

The equivalent input noise current spectral density contributed by the transistor drain noise is roughly given by

$$N_{n,d} \approx 4KT g_{d0} \left(\frac{1}{g_m^2 |Z_{in}|^2} - 1 \right) \approx 4KT g_{d0} \frac{\omega^2 C_{in}^2}{g_m^2} \quad (2.53)$$

Because the gate noise and the drain noise are correlated, the equivalent input noise current spectral density contributed by the correlated noise is given by

$$N_{n,c} = \overline{i_g} \frac{\overline{i_d^*}}{g_m Z_{in}^*} + \overline{i_g^*} \frac{\overline{i_d}}{g_m Z_{in}} = \frac{c}{Z_{in}^*} \frac{\sqrt{\overline{i_g^2 i_d^2}}}{g_m} + \frac{c^*}{Z_{in}} \frac{\sqrt{\overline{i_g^2 i_d^2}}}{g_m} \quad (2.54)$$

where Z_{in} is the input impedance. The total equivalent input noise current spectral density based on (2.52) to (2.54) is about

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \frac{1}{R_s} + \frac{1}{R_1} + \frac{\omega^2 C_{in}^2}{g_m^2} \left[\frac{1}{R_1} + \Gamma g_{d0} \left(1 - \frac{C_{gs}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] + \delta \frac{\omega^2 C_{gs}^2}{5g_{d0}} (1 - |c|^2) \right\} \quad (2.55)$$

where $C_{in} \approx C_{pd} + C_1$.

Figure 2.20: Schematic of the shunt feedback common source TIA input stage and its small signal circuit

(2.55) is very close to (2.51). Similarly, although the induced gate noise of the input transistor of CMOS TIAs adds directly to the total input referred noise, the correlated noise cancels the total equivalent input noise. In deep submicron devices, the abstract value $|c|$ of the correlation coefficient can be more than 0.75, which can help to reduce the total input noise significantly at *optimum* transistor size [101]. However, due to the technology limitation and the trade-offs between gain-bandwidth and noise. It is usually not possible to achieve the optimum noise

performance while maintaining the required gain-bandwidth. According to the analysis in Chapter 4, after meeting the gain-bandwidth requirement, there is nearly no design headroom for noise optimization. The noise reduction effect by the induced gate noise under such circumstances is not significant. The detailed method for finding the optimum transistor size for best noise performance could be found in [101].

2.8 Summary

In this chapter, the general design considerations of optical receivers and TIA performance metrics are introduced followed by TIA design specifications. Basic TIA topologies including current mode and voltage mode TIAs are reviewed with the pros and cons of different topologies. Various commonly used design techniques for transimpedance amplifiers are also reviewed. The idea of automatic gain control is also briefed in the middle of this chapter. In the section of noise analysis basics at the end of this chapter, noise analysis methodologies for transimpedance amplifier are introduced based on the van der Ziel MOSFET noise model. Noise analysis examples of shunt-feedback common source TIA input stage and current mode common gate TIA input stage are presented in this section. They reveal an important conclusion that though the induced gate noise of the input transistor of CMOS TIAs adds directly to the total input referred noise, the correlated noise cancels the total equivalent input noise. This means that the channel thermal noise is shorted out by the gate capacitance and hence the total noise at the input is reduced. According to numerical data, the input referred noise current reduction for *optimum* transistor size is about 10% to 20% [101].

Chapter 3

Design of a CMOS RGC TIA with Capacitive Degeneration and Broadband Matching

3.1 Introduction

Comparing with those state-of-the-art Heterojunction Bipolar Transistor/High Electron Mobility Transistor (HBT/ HEMT) technologies, CMOS transistors are less efficient for high-frequency applications. In the beginning of this chapter, several circuit design techniques are introduced with focus on the bandwidth enhancement of CMOS TIAs. Such techniques improve the bandwidth and relax the trade-offs between the bandwidth, gain and noise, thereby allow more design headroom to achieve an optimum overall performance. Based on these high performance design techniques, a novel bandwidth enhancement method based on the combination of broadband input matching *LC* network, RGC input stage and capacitive degeneration is introduced. This method turns the TIA design into a fifth order low-pass filter aiming for a frequency response with maximal gain flatness (*Butterworth response*). This topology is able to enhance the bandwidth and provide efficient noise reduction at the same time. The proposed broadband design methodology for transimpedance amplifiers is presented with an example implemented in CHRT 0.18 μ m-1.8V RF CMOS technology. Measurement data shows a -3dB bandwidth of about 8GHz with a 0.25pF photodiode capacitance. The total lumped input parasitic capacitance is about 0.35pF. Comparing with the core RGC TIA without capacitive degeneration and broadband matching network, this design achieves an overall bandwidth enhancement ratio of 3.6 with very small

gain ripple. The transimpedance gain is about 53dB Ω with a group delay of 80 $\pm$ 20ps. The chip consumes 13.5mW DC power from a single 1.8V supply. The measured average input referred noise current spectral density is 18pA/ $\sqrt{\text{Hz}}$ up to 10GHz.

Figure 3.1: (a) Schematic of the proposed TIA. (b) Small signal model of the matching network and the RGC stage. (c) Equivalent low-pass filter representation of the proposed TIA

3.2 Circuit design and analysis

The three broadband design techniques reviewed in Section 2.6, namely regulated cascode (RGC) input stage, capacitive degeneration and broadband matching network, are combined together to design a 10Gb/s CMOS TIA aiming for maximally-flat gain frequency response in this section. The L - C ladder filter employed in this design is used to enhance the bandwidth and reduce the equivalent input noise current as well, which will be analyzed in detail.

The proposed TIA design schematic is shown in Figure 3.1 (a). The circuit is composed of four parts, namely the matching network, the regulated cascode input stage, the gain stage with capacitive degeneration and the source follower output stage. The low frequency transimpedance gain is given by

$$Z_T(0) \approx R_1 \frac{g_{m3}R_3}{1 + g_{m3}R_b} \frac{g_{m4}R_4}{1 + g_{m4}R_4} \quad (3.1)$$

where we can infer that the transimpedance gain is mainly determined by R_1 . The RGC stage [63] presents a very small input resistance and therefore the lowest pole of the circuit is located within the TIA at node A, which is given by

$$f_{-3dB,0} = \frac{\omega_0}{2\pi} \approx \left\{ 2\pi R_1 [C_{gd1} + C_{db1} + C_{g3}] \right\}^{-1} \quad (3.2)$$

where C_{g3} is approximately the sum of the Miller capacitances of C_{gd3} and C_{gs3} . In this design, we choose a small R_2 resistance to avoid possible peaking due to the zero generated by the local feedback of the RGC stage [63] and a relatively large R_s resistance to minimize its noise current contribution and signal loss. The capacitive degeneration [28] gain stage consists of M_3 , R_3 , R_b and C_b contributes a zero $(R_b C_b)^{-1}$ that is used to compensate the lowest pole determined at node A, which means

$$f_{-3dB,0} \approx \left\{ 2\pi R_1 [C_{gd1} + C_{db1} + C_{g3}] \right\}^{-1} = (2\pi R_b C_b)^{-1} \quad (3.3)$$

Besides this zero, the capacitive degeneration also generates an additional pole $(1 + g_{m3}R_b)/R_b C_b$ at a higher frequency, which is the second lowest pole in this design. Therefore, the new -3dB bandwidth can be estimated by

$$f_{-3dB,1} = \frac{\omega_1}{2\pi} \approx \frac{1 + g_{m3}R_b}{2\pi R_b C_b} \quad (3.4)$$

M_4 , R_4 is the source follower output stage to drive the capacitance of the output pad. In this design, the lowest pole at node A is targeting at about 2.5GHz and the bandwidth after capacitive degeneration is chosen to be around 4.5GHz, which means $g_{m3}R_b \approx 0.8$. For a typical 10Gb/s TIA, the bandwidth is usually around 0.6B to 0.7B if the receiver bandwidth is set by the TIA, where B stands for the bit rate [55]. Therefore, the bandwidth of the core TIA is not enough and additional bandwidth extension is to be achieved by a broadband matching network (series inductive peaking) between the photodiode and the core TIA. Figure 3.1 (b) illustrates the small-signal model of the matching network and the RGC input stage. C_I is the lumped parasitic capacitance at node 1 including the photodiode parasitic capacitance C_{pd} . C_2 is the lumped parasitic capacitance at node 2. This matching network is not purely passive because it interacts with the RGC input stage. We need to convert it to an equivalent passive matching network for the convenience of mathematical analysis. Looking from into node 2 from the input in Figure 3.1 (b) and applying *Kirchhoff's Current Law* we obtain

$$Z_i \approx \frac{g_{m1} \left(1 + s \frac{C_{gs1}}{g_{m1}} \right) sL_2 + \left(1 + sC_{gs1}R_2 \right) \left(1 + s \frac{L_2}{R_s} \right)}{g_{m1} (1 + g_{m2}R_2) \left(1 + s \frac{C_{gs1}}{g_{m1}} \right) + \frac{1}{R_s} (1 + sC_{gs1}R_2)} \quad (3.5)$$

As mentioned previously, R_s is a relatively large resistance and R_2 is a small one in this design. Within the bandwidth of interest (below 10GHz), it is reasonable to make following simplifications

$$\begin{aligned}
 Z_i &\approx \frac{g_{m1} \left(1 + s \frac{C_{gs1}}{g_{m1}} \right) sL_2 + \left(1 + sC_{gs1}R_2 \right) \left(1 + s \frac{L_2}{R_s} \right)}{g_{m1} (1 + g_{m2}R_2) \left(1 + s \frac{C_{gs1}}{g_{m1}} \right) + \frac{1}{R_s} (1 + sC_{gs1}R_2)} \\
 &\approx \frac{sL_2}{1 + g_{m2}R_2} + \frac{1 + sC_{gs1}R_2}{g_{m1} (1 + g_{m2}R_2)} \frac{1 + s \frac{L_2}{R_s}}{1 + s \frac{C_{gs1}}{g_{m1}}} \\
 &\approx \frac{sL_2}{1 + g_{m2}R_2} + \frac{1}{g_{m1} (1 + g_{m2}R_2)}
 \end{aligned} \tag{3.6}$$

Therefore we have

$$Z_i \approx \frac{sL_2}{1 + g_{m2}R_2} + \frac{1}{g_{m1} (1 + g_{m2}R_2)} = sL_{2,eff} + r_i \tag{3.7}$$

where we define $L_{2,eff} = \frac{L_2}{1 + g_{m2}R_2}$ and $r_i = \frac{1}{g_{m1} (1 + g_{m2}R_2)}$. Based on this definition,

we can simplify the matching network in Figure 3.1 (b), which is not purely passive due to its interaction with the active devices of the RGC input stage, to a purely passive one. As shown in Figure 3.1 (c), the whole amplifier is simplified to a passive matching network with L_2 replaced by $L_{2,eff}$ followed by a core TIA with a dominant pole ω_1 expressed by (3.4) and an input resistance r_i defined in (3.7).

To simplify the analysis, we have neglected the effects of all other poles and zeros of the core-TIA circuit. The reasons are: Firstly there are two prominent zeros in the proposed design, one is used to compensate the lowest pole of the circuit and the other is due to the local feedback of the RGC stage and can be optimized to be beyond the bandwidth of interest. Secondly the poles at the drains of M_2 and M_3 are designed to be at much higher frequencies. Finally the pole at the output node

is also neglected due to the small output resistance of the source follower stage. Though these poles are neglected for analysis simplicity, their combinational effect will cause the actual -3dB bandwidth of the core TIA to be lower than that expressed in (3.4). The effective inductance $L_{2,eff}$ in the equivalent matching network is $(1 + g_{m2}R_2)$ times smaller than the actual value of L_2 by the effect of RGC stage. This equivalent matching network consists of C_1 , L_1 , C_2 and $L_{2,eff}$ is fourth order and considering the dominant pole ω_1 of the core TIA, the whole amplifier can be approximated to a fifth order low pass filter with a frequency independent gain $Z_T(0)$. From the small-signal circuit model in Figure 3.1 (c), the transfer function of the whole circuit can be derived as

$$Z_T(s) = \frac{Z_T(0)}{1 + s \left[(C_1 + C_2)Z_i + \frac{1}{\omega_1} \right] + s^2 \left[L_1 C_1 + \frac{(C_1 + C_2)Z_i}{\omega_1} \right] + s^3 L_1 C_1 \left[C_2 Z_i + \frac{1}{\omega_1} \right] + s^4 \frac{L_1 C_1 C_2 Z_i}{\omega_1}} \quad (3.8)$$

where ω_1 is the estimated -3dB bandwidth of the core TIA, which is given by (3.4), and Z_i is given by (3.7). To design this transfer function with maximally-flat gain response (Butterworth), the most convenient way is to map the coefficients of the denominator of (3.8) to the fifth-order Butterworth coefficients. As introduced in Section 2.6.5, the coefficients of a fifth-order Butterworth polynomial $q(y) = a_0 + a_1 y + a_2 y^2 + a_3 y^3 + a_4 y^4 + a_5 y^5$ can be computed as $a_0 = 1$, $a_1 = 3.2360$, $a_2 = 5.2360$, $a_3 = 5.2360$, $a_4 = 3.2360$, $a_5 = 1$ [117]. Therefore, we can write the coefficients of the denominator of (3.8) as

$$\omega_c \left[\frac{1}{\omega_1} + r_i (C_1 + C_2) \right] = a_1 \quad (3.9)$$

$$\omega_c^2 \left[L_1 C_1 + \left(L_{2,eff} + \frac{r_i}{\omega_1} \right) (C_1 + C_2) \right] = a_2 \quad (3.10)$$

$$\omega_c^3 \left[\frac{L_1 C_1 + L_{2,eff} (C_1 + C_2)}{\omega_1} + L_1 C_1 C_2 r_i \right] = a_3 \quad (3.11)$$

$$\omega_c^4 \left[\frac{L_1 C_1 C_2 r_i}{\omega_1} + L_1 L_{2,eff} C_1 C_2 \right] = a_4 \quad (3.12)$$

$$\omega_c^5 \frac{L_1 L_{2,eff} C_1 C_2}{\omega_1} = a_5 \quad (3.13)$$

where r_i and $L_{2,eff}$ are given in (3.5), ω_c is the cut-off frequency of the whole amplifier with matching network. Our design goal is to achieve $\omega_c = 2\omega_1$, i.e. $f_c = 2f_1 = 9GHz$. The design parameters can be computed from these equations to implement a maximally-flat gain response transimpedance amplifier. The simulation result in Figure 3.10 shows that, without any bandwidth enhancement technique employed, the RGC TIA exhibits only about 2.2GHz -3dB bandwidth. After the compensation by capacitive degeneration, the bandwidth is extended to about 4.5GHz. A bandwidth enhancement ratio of 2 is further achieved by the broadband matching network and the simulated bandwidth is extended to about 9.1GHz.

3.3 Noise analysis and reduction

As introduced in Section 2.3.2, the equivalent input noise current, also called the input referred noise current, is a significant figure of merit of TIA design. It directly affects the optical link budget. The bit error rate (BER) of an optical front-end can be expressed in terms of the RMS value of total equivalent input noise current by $BER = Q(i_{in,pp} / 2i_{n,eq}^{rms})$, where $i_{in,pp}$ is the peak to peak input current signal

amplitude and $Q(x) = \int_x^\infty \frac{1}{\sqrt{2}} \exp\left(-\frac{u^2}{2}\right) du$. The equivalent input noise current is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actually noisy TIA [55]. According to the discussion in Section 2.7, although the TIA noise model can be conveniently represented by a noise current source only, the equivalent input noise current is dependent on the source impedance, which is mainly determined by the photodiode capacitance and the matching network [55] [109]. Therefore, standard noise analysis in terms of E_n - I_n model (both noise voltage and noise current sources are present) is necessary to evaluate the influence of the input matching network on noise [109].

In this section, we will evaluate the noise reduction effect in our proposed TIA by expressing the equivalent input noise current in terms of the E_n - I_n pair. According to the schematics in Figures 3.1 (a) and (3.1), (3.23), only a portion of the input current that flows through the channel of M_1 to the following stages will produce the transimpedance gain, other portion of the input current will be lost through parasitic capacitances. The channel of M_1 can be viewed as a resistive element $r_i = \frac{1}{g_{m1}(1 + g_{m2}R_2)}$. Based on this concept, we represent the

transimpedance amplifier noise model in Figure 3.2 (a), where $i_{n,eq,0}$ is the portion of the total input referred noise current flowing through r_i to produce the output noise $v_{n,o}$ and $Z_T = \frac{v_{n,o}}{i_{n,eq,0}}$. Figure 3.2 (a) also represents a simple TIA model with

series inductive matching/peaking between the photodiode and the amplifier, which reduces the frequency dependent noise and improves the front-end sensitivity [115-116]. For a given output noise voltage spectral density $v_{n,o}$, the

equivalent input noise current spectral density, based on Figure 3.2 (a), can be derived as

$$\begin{aligned} \overline{i_{n,eq}}^2 &= \left| \left(1 - \omega^2 L C_{pd} \right) + j\omega (C_{pd} + C_x) r_i \left(1 - \omega^2 L \frac{C_{pd} C_x}{C_{pd} + C_x} \right) \right|^2 \frac{\overline{v_{n,o}}^2}{|Z_T|^2} \\ &= \left| \left(1 - \omega^2 L C_{pd} \right) + j\omega (C_{pd} + C_x) r_i \left(1 - \omega^2 L \frac{C_{pd} C_x}{C_{pd} + C_x} \right) \right|^2 \overline{i_{n,eq,0}}^2 \end{aligned} \quad (3.14)$$

where C_{pd} is for the photodiode parasitic capacitance and C_x is the total parasitic capacitance of the core TIA at the input node. The inductive noise reduction effect is straightforward from (3.14). However, $v_{n,o}$ and $i_{n,eq,0}$ are not constant for different matching networks. Figure 3.2 (b) shows the E_n - I_n noise model for the same TIA. E_n is a zero impedance noise voltage generator and I_n is an infinite impedance noise current generator [109]. Based on Figure 3.2 (b) and regarding these noise sources as linear voltage/current signals we obtain

$$\frac{Z_s I_n + E_n}{Z_s + Z_i} \frac{1}{1 + s r_i C_x} = \frac{v_{n,o}}{Z_T} = i_{n,eq,0} \quad (3.15)$$

where $Z_s = sL + 1/sC_{pd}$ is the impedance looking from E_n into the input matching network and $Z_{in} = r_i // (sC_x)^{-1}$ is the input impedance of the core TIA. According to (3.15), E_n can be measured by setting $Z_s = 0$ (short circuit) and I_n can be measured by setting $Z_s = \infty$ (open circuit). Therefore, for a given E_n - I_n noise model, E_n and I_n are independent of the input matching network and source impedance. However, they are typically frequency dependent [109]. For linear signals, linear voltage and current division and superposition principles can be applied. However, for noise calculation, each noise contribution must be summed up in mean square values [109]. Based on (3.14), (3.15) and assuming E_n and I_n are uncorrelated, the input referred noise current spectral density can be derived in terms of E_n and I_n as

$$\overline{|i_{n,eq}|^2} = (1 - \omega^2 LC_{pd}) I_n^2 + \omega^2 C_{pd}^2 E_n^2 \quad (3.16)$$

Figure 3.2: TIA noise model with series inductive noise reduction: (a) equivalent input noise current model, (b) E_n - I_n model.

It is also noteworthy that in microwave circuit design, noise representations are usually based on four noise parameters, i.e. minimum noise figure F_{min} , real and imaginary parts of optimum source admittance Y_{opt} and noise resistance R_n . It is proved in [118] that a general expression for the equivalent input current noise current spectral density of any transimpedance amplifier with arbitrary matching network can also be expressed in terms of the above-mentioned four noise parameters

$$\frac{\overline{|i_{n,eq}|^2}}{\Delta f} = 4KT_0 \frac{R_n}{Z_0^2} \left| \frac{1 - \Gamma_{opt}^2}{1 + \Gamma_{opt}^2} \right|^2 \quad (3.17)$$

where T_0 is the reference temperature, Z_0 is the characteristic impedance, Γ_{opt} is the optimum source reflection coefficient. According to (3.16), besides bandwidth

enhancement, the broadband matching network can also help to reduce the equivalent input noise current of the proposed TIA design. According to the discussion in Section 2.7, the dominant noise sources in a CMOS high frequency TIA are thermal noise. At radio frequencies, the channel thermal noise current will be coupled to the gate terminal through the gate-oxide capacitance and this coupled noise is called the induced gate noise [110]. Although the induced gate noise itself adds to the total input noise, it is correlated with the channel thermal noise. The correlated noise, when referring to the input, helps to reduce the total input referred noise [101]. We will now examine the input referred noise current due to the thermal noise sources but neglect the induced gate noise. At the end of this chapter, an extended noise analysis of the RGC TIA input stage based on the van der Ziel MOSFET noise model that includes the induced gate noise is presented. In Chapter 4, we will further discuss the effect of the induced gate noise in a broadband TIA in more detail. Without the matching network, the equivalent input noise current spectral density of the proposed TIA can be estimated using the analysis method introduced in Section 2.7 and [63] as

$$\begin{aligned}
 \overline{i_{n,eq}^2} \approx & \frac{4KT}{R_s} + \frac{4KT}{R_1} + \frac{4KT \left(\gamma g_{d0,1} + \frac{1}{R_1} \right)}{g_{m1}^2} \omega^2 \left(C_j + \frac{C_{pd}}{1 + g_{m2}R_2} \right)^2 \\
 & + \frac{4KT \left(\gamma g_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \left[\frac{1}{R_s^2} + \omega^2 (C_{pd} + C_i)^2 \right] \\
 & + \frac{4KT \omega^2 C_y^2}{1 + \omega^2 R_b^2 C_b^2} \left[\left(\gamma g_{d0,3} + \frac{1}{R_3} \right) \left(\frac{1 + g_{m3}R_b}{g_{m3}} \right)^2 + R_b \right]
 \end{aligned} \tag{3.18}$$

where K is the Boltzmann constant, T is the absolute temperature, γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, $C_i \approx C_{sb1} + C_{gs2}$,

$C_j \approx C_{gs1} + C_{gd2}$, C_y is the total parasitic capacitance at node A in Figure 3.1 (a) including C_{gd1} , C_{db1} and the Miller capacitance of C_{gd3} and C_{gs3} . The equivalent input noise current spectrum density expression of (3.18) can be divided into four components as follows

$$|i_{n,eq,R}|^2 \approx \frac{4KT}{R_s} + \frac{4KT}{R_1} + \frac{4KT \left(\mathcal{G}_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \frac{1}{R_s^2} \quad (3.19)$$

$$|i_{n,eq,1}|^2 \approx \frac{4KT \left(\mathcal{G}_{d0,1} + \frac{1}{R_1} \right)}{g_{m1}^2} \omega^2 \left(C_j + \frac{C_{pd}}{1 + g_{m2}R_2} \right) \quad (3.20)$$

$$|i_{n,eq,2}|^2 \approx \frac{4KT \left(\mathcal{G}_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \omega^2 (C_{pd} + C_i)^2 \quad (3.21)$$

$$|i_{n,eq,b}|^2 \approx \frac{4KT \omega^2 C_y^2}{1 + \omega^2 R_b^2 C_b^2} \left[\left(\mathcal{G}_{d0,3} + \frac{1}{R_3} \right) \left(\frac{1 + g_{m3}R_b}{g_{m3}} \right)^2 + R_b \right] \quad (3.22)$$

(3.19), (3.20) and (3.21) are due to the thermal noises of the RGC input stage including M_1 , R_1 , M_2 , R_2 and R_s . (3.19) is the frequency independent noise component contributed by the resistive elements. (3.20) and (3.21) are the major noise contributors and increase rapidly with frequency. (3.22) is contributed by the capacitive degeneration stage. Because $R_b C_b$ and $g_{m3} R_b$ are predetermined as mentioned in Section 3.1, if we choose a small R_b and a large C_b , this noise component can be reduced. Furthermore, the numerator and denominator of (3.22) both increase as frequency increases. Hence, at high frequencies, this noise

component can be simplified to $\frac{4KTC_y^2}{R_b^2 C_b^2} \left[\left(\mathcal{G}_{d0,3} + \frac{1}{R_3} \right) \left(\frac{1 + g_{m3}R_b}{g_{m3}} \right)^2 + R_b \right]$, which is

frequency independent. According to the above discussion, the capacitive degeneration stage not only boosts the bandwidth but also contributes low noise at high frequencies. Therefore, the major noise contribution is from the regulated cascode input stage including M_1 , R_1 , M_2 , R_2 and R_s . We will now recalculate the equivalent input noise current contributed by the RGC input stage based on the E_n - I_n model and discuss the noise reduction effect by the input matching network on the proposed TIA design. According to (3.1), the input admittance of the core TIA without the input matching network is

$$Y_{in}(s) = g_{m1}(1 + g_{m2}R_2) + \frac{1}{R_s} + sC_i + sC_j(1 + g_{m2}R_2) \quad (3.23)$$

$$= \frac{1}{r_i} + \frac{1}{R_s} + sC_x$$

Figure 3.3: (a) E_n - I_n noise model of the RGC TIA without input matching network and (b) its equivalent circuit for noise analysis

According to (3.23), the E_n - I_n noise model of the proposed TIA without the matching network can be represented in Figure 3.3 (a), where C_i and C_j are the same as those in (3.1) and (3.18), $C_x \approx C_i + (1 + g_{m2}R_2)C_j$ and r_i is defined in (3.7). Usually one can assume the E_n - I_n correlation to be zero with little error especially when they are only partially correlated [109]. Based on Figure 3.3 (a), we obtain

$$\overline{i_{n,eq}^2} = I_n^2 + \omega^2 C_{pd}^2 E_n^2 \quad (3.24)$$

where E_n can be evaluated by setting $C_{pd} = \infty$ (short circuit) and I_n can be evaluated by setting $C_{pd} = 0$ (open circuit). As introduced in the beginning of this section, $i_{n,eq,0}$ is the equivalent noise current flowing through the channel of M_1 to the following stages. When assuming the TIA is noiseless, this noise current produces the same output noise as the actual noisy TIA. Based on Figure 3.3 (a), we obtain

$$\left| i_{n,eq,0} \right|_{short}^2 = \left| \frac{E_n}{r_i} \right|^2 \quad (3.25)$$

$$\left| i_{n,eq,0} \right|_{open}^2 = \left| \frac{R_s}{R_s + r_i + sC_x R_s r_i} I_n \right|^2 \quad (3.26)$$

where $i_{n,eq,0}|_{short}$ stands for the equivalent noise current $i_{n,eq,0}$ when $C_{pd} = \infty$ (short circuit) and $i_{n,eq,0}|_{open}$ stands for the equivalent noise current $i_{n,eq,0}$ when $C_{pd} = 0$ (open circuit). By analyzing the noise sources in Figure 3.3 (b), we obtain

$$\left| i_{n,eq,0} \right|_{short}^2 = i_{n,R1}^2 + i_{n,M1}^2 + (i_{n,R2}^2 + i_{n,M2}^2) R_2^2 g_{m1}^2 \quad (3.27)$$

$$\begin{aligned} |i_{n,eq,0}|_{open}^2 &= i_{n,R1}^2 + i_{n,M1}^2 \left(1 - \left| \frac{R_s}{R_s + r_i + sC_x R_s r_i} \right|^2 \right) + i_{n,Rs}^2 \left| \frac{R_s}{R_s + r_i + sC_x R_s r_i} \right| \\ &+ \frac{i_{n,R2}^2 + i_{n,M2}^2}{\left(g_{m2} + \frac{1}{R_2} \right)} \left| \frac{1 + sC_i R_s}{R_s + r_i + sC_x R_s r_i} \right|^2 \end{aligned} \quad (3.28)$$

where $i_{n,R1}^2 = \frac{4KT}{R_1}$, $i_{n,R2}^2 = \frac{4KT}{R_2}$, $i_{n,Rs}^2 = \frac{4KT}{R_s}$, $i_{n,M1}^2 = 4KT\gamma_{d0,1}$ and $i_{n,M2}^2 = 4KT\gamma_{d0,2}$.

Substituting (3.25) into (3.27) and (3.26) into (3.28), we obtain

$$E_n^2 \approx \frac{4KT \left(\gamma_{d0,1} + \frac{1}{R_1} \right)}{g_{m1}^2 (1 + g_{m2} R_2)^2} + \frac{4KT \left(\gamma_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \quad (3.29)$$

$$\begin{aligned} I_n^2 &\approx \frac{4KT}{R_s} + \frac{4KT}{R_1} + \frac{4KT \left(\gamma_{d0,1} + \frac{1}{R_1} \right)}{g_{m1}^2} \omega^2 C_j^2 \\ &+ \frac{4KT \left(\gamma_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \left(\frac{1}{R_s^2} + \omega^2 C_i^2 \right) \end{aligned} \quad (3.30)$$

where C_i and C_j are the same as those in (3.1) and (3.18), $C_x \approx C_i + (1 + g_{m2} R_2) C_j$.

By substituting (3.29), (3.30) into (3.24) and disregarding the small difference that is due to the omission of the E_n - I_n correlation in our analysis, the derived equivalent input noise current spectral density contributed by the RGC input stage based on the E_n - I_n model is essentially the same as the sum of (3.19), (3.20) and (3.21). Figure 3.4 shows the noise model for the proposed TIA with the input matching network. Based on the preceding discussion, the correlated noise of E_{nI} and I_{nI} is only a small portion of the total noise. Therefore, we still assume E_{nI} and I_{nI} are uncorrelated for simplicity. According to (3.16), we obtain

$$\overline{i_{n,eq}^2} = (1 - \omega^2 L_1 C_{pd}) I_{n1}^2 + \omega^2 C_{pd}^2 E_{n1}^2 \quad (3.31)$$

Figure 3.4: *En-In* noise model of the RGC TIA with input matching network

The noise reduction effect of L_1 is clearly demonstrated by (3.31). The effect of L_2 is similar to that of L_1 . Based on Figure 3.4 and using the above analysis method based on Figure 3.3, we obtain

$$E_{n1}^2 \approx N_1^2 + N_2^2 \quad (3.32)$$

$$I_{n1}^2 \approx (1 - \omega^2 L_{2,eff} C_\alpha)^2 (\omega^2 C_\beta^2 N_1^2 + \omega^2 C_{sb1}^2 N_2^2 + N_R^2) + \omega^2 C_\alpha^2 N_1^2 + \omega^2 C_{gs2}^2 N_2^2 \quad (3.33)$$

where $C_\alpha \approx C_{gs2} + (1 + g_{m2} R_2) C_{gd2}$, $C_\beta \approx (1 + g_{m2} R_2) C_{gs1}$ and

$$N_1^2 = \frac{4KT \left(\gamma g_{d0,1} + \frac{1}{R_1} \right)}{g_{m1}^2 (1 + g_{m2} R_2)^2} \quad (3.34)$$

$$N_2^2 = \frac{4KT \left(\gamma g_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \quad (3.35)$$

$$N_R^2 \approx \frac{4KT}{R_s} + \frac{4KT}{R_l} + \frac{4KT \left(\gamma g_{d0,2} + \frac{1}{R_2} \right)}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \frac{1}{R_s^2} \quad (3.36)$$

Substituting (3.32) and (3.33) into (3.31), the equivalent input noise current spectral density of our proposed TIA with the input matching network is given by

$$\overline{|i_{n,eq}|^2} = \omega^2 C_{pd}^2 (N_1^2 + N_2^2) + (1 - \omega^2 L_1 C_{pd}) \cdot \left[(1 - \omega^2 L_{2,eff} C_\alpha)^2 (\omega^2 C_\beta^2 N_1^2 + \omega^2 C_{sb1}^2 N_2^2 + N_R^2) + \omega^2 C_\alpha^2 N_1^2 + \omega^2 C_{gs2}^2 N_2^2 \right] \quad (3.37)$$

Figure 3.5: Calculated equivalent input noise current spectral density of the proposed TIA input stage (Curve a: without noise reduction; curve b: noise reduction with L2 only; curve c: noise reduction with L1 only; curve d: noise reduction with L1 and L2)

Figure 3.5 shows the MATLAB calculated equivalent input noise current spectral density of the proposed TIA input stage. The calculation uses the device parameters in CHRT 0.18 μ m RFCMOS PDK. In Figure 3.5, curve “a” is based on (3.24), which is without any noise reduction effect; curve “b” is based on (3.37) with $L_l = 0$, which shows the noise reduction effect with L_2 only; curve “c” is

based on (3.16) with E_n and I_n expressed by (3.29) and (3.30) respectively, which shows the noise reduction effect with L_1 only; curve “d” is based on (3.37), which shows the noise reduction effect with L_1 and L_2 . Within the bandwidth of interest, the noise could be reduced significantly. Intuitively, such kind of noise reduction effect is two-fold. On one hand, the inductor splits the large capacitive load to two smaller parts. On the other hand, according to (3.37) and curve “d” of Figure 3.5, the noise decreases until it reaches a minimum level, after which it starts to increase. As illustrated by curve “a” of Figure 3.5, the noise increases monotonically without the input matching network.

3.4 Silicon implementation

To verify the merits of the proposed RGC TIA design with capacitive degeneration and broadband matching network, the proposed circuit is implemented using CHRT 0.18 μ m 2-poly 6-metal RFCMOS process. L_1 and L_2 are implemented using on-chip spiral inductors for the purpose of monolithic implementation and improving area efficiency. The on-chip spiral inductor is constructed based on the lithography, where the geometry of coils is well-controlled. Figure 3.6 shows a typical geometrical layout of a spiral inductor in CHRT foundry library, which uses the top metal layer and returns to outside through the underpass metal layer. Because they are used for series broadband matching/peaking, their quality factors are not the primary issue [73]. The lumped element model is widely used to simulate the performance of an inductor [119-120]. A typical π -equivalent model is shown in Figure 3.7. It consists of nine components, where L is the total inductance produced by the metal winding and mutual coupling, R_L is the total loss of the inductor, C_{ox} is the capacitance between

inductor and substrate, R_s and C_s are the parasitic resistance and capacitance of the substrate. The total inductance of the spiral inductor is the sum of the self-inductance and the mutual-inductance [121]. The mutual inductance is introduced by the magnetic coupling between the conductors. The same direction of the current flow results in a positive coupling, otherwise, a negative coupling is introduced. The detailed calculation of the mutual inductance is summarized in [122].

Figure 3.6: Geometry of a spiral inductor

Figure 3.7: The lumped element model of an on-chip inductor

Figure 3.8 shows the chip microphotograph of the proposed TIA. An on-chip MIM capacitor C_{pd} of 0.25pF is used to mimic the effect of the photodiode

parasitic capacitance, and together with the parasitic capacitance of the input pad, the total input parasitic capacitance is about 0.35pF.

Figure 3.8: Chip microphotograph of the proposed TIA

3.5 Simulation and measurement results

The simulations of the proposed TIA design are performed using the Cadence SpectreRF and CHRT 0.18 μ m RFCMOS design PDK. The noise simulation of the whole TIA circuit is shown in Figure 3.9 (a). For the purpose of comparison, the calculated noise in Figure 3.5 is also plotted together with the simulated noise in Figure 3.9 (b). The simulation confirms with our mathematical analysis. The simulated equivalent input noise current spectral density in Figure 3.9 is dominated by flicker noise at low frequencies and as frequency increases it exhibits similar characteristic to that MATLAB-calculated equivalent input noise current spectral density.

Figure 3.9: (a) SpectreRF post-layout simulated equivalent input noise current spectral density of the complete TIA circuit. (Curve a: without noise reduction; curve b: noise reduction with L2 only; curve c: noise reduction with L1 only; curve d: noise reduction with L1 and L2). (b) Calculated noise of the proposed TIA input stage/ simulated noise of the complete TIA design.

Disregarding the flicker noise, the discrepancy between the calculated and the simulated results is mainly due to three reasons. Firstly, in our calculation we only consider the noise of the input stage while the simulation is based on the whole

TIA circuit. Secondly, in our calculation we have neglected the correlated noise that is usually a very small portion as mentioned previously. Finally, the inductors used in calculation are ideal. The first reason explains why there is roughly $2\text{ pA}/\sqrt{\text{Hz}}$ difference between the calculated and the simulated results. According to curve “a” and curve “d” in Figure 3.9 (a), without noise reduction the simulated average input referred noise current spectral density is about $18\text{ pA}/\sqrt{\text{Hz}}$ and with noise reduction it is $12\text{ pA}/\sqrt{\text{Hz}}$ on average. According to (2.8), such kind of noise reduction can improve the input sensitivity by more than 30% at a given bit error rate requirement.

Figure 3.10: Post-layout simulated transimpedance response: -3dB bandwidth of 2.2GHz for core TIA, 4.5GHz for TIA with capacitive degeneration, 9.1GHz for TIA with capacitive degeneration and broadband matching network

The transimpedance gain frequency response simulation result is shown in Figure 3.10. The devices (MOSFETs, resistors, inductors and capacitors) used in theoretical calculation are ideal. However, they are non-ideal in reality. Furthermore, the CHRT RF MOSFETs and inductors used in the design are not

scalable. Therefore, calculation can only help to give a roughly estimated value. Small adjustments and fine optimizations on the device sizes with the help of the circuit simulator are necessary to meet the design objectives. The simulated -3dB bandwidth enhancement is from 2.2GHz to 4.5GHz by the capacitive degeneration and to 9.1GHz by the broadband matching network. Figure 3.11 shows the post-layout simulated eye-diagram with 10Gb/s $2^{31}-1$ pseudo random binary sequence (PRBS). Comparing Figure 3.11 (a) with Figure 3.11 (b), there is no clear distortion added when the signal level is increased from 50 μ A to 0.5mA. The chip is measured on wafer with Cascade Microtech Coplanar Ground-Signal Ground (GSG) probes. The frequency response is measured with HP8510C network analyzer. The measured transimpedance frequency response of the proposed design is shown in Figure 3.12. The transimpedance gain frequency response exhibits a -3dB bandwidth of about 8GHz and 53dB Ω transimpedance gain with very small gain ripple. Compared to the simulated result in Figure 3.10, the low frequency gain matches well while at higher frequencies the measured gain drops faster than simulated, which is possibly due to the non-ideality of the inductors, the EM radiation loss, the silicon substrate loss and process variations.

Good phase linearity is another important requirement for TIA design to limit the generation of data-dependent jitter [55]. The group delay is calculated from the measured phase response. The measured group delay frequency response of the proposed design is shown in Figure 3.13. According to Figure 3.13, the group delay is about 80 $\pm$ 20ps.

Figure 3.11: Post-layout simulated eye diagram with (a) 500 μ A peak-peak input current, (b) 50 μ A peak-peak input current, both with 10Gb/s $2^{31}-1$ pseudo random binary sequence (PRBS)

Figure 3.12: Measured transimpedance response of the proposed TIA

Figure 3.13: Measured group delay response of the proposed TIA

Figure 3.14: Measured noise response of the proposed TIA

The measured noise response is shown in Figure 3.14. The noise measurement is carried out using 8970B Noise Figure Meter, 8971C Noise Figure Test Set and NP5B Noise Parameter Test System. The average measured input referred noise current spectral density is about $18 \text{ pA}/\sqrt{\text{Hz}}$ up to 10GHz and the total input

referred noise current is $1.6\mu\text{A}$ integrated up to 8GHz. The measured input referred noise current spectral density is higher than the simulated one, possibly due to inaccurate noise model (BSIM3 model does not include the induced gate noise), additional parasitic elements and substrate noise/losses that are not considered in the simulation and process variations. However, the noise reduction effect is still noticeable from the measured data because over the bandwidth of interest the noise level is stable and does not increase with frequency.

The output transient response of the proposed TIA is also tested on wafer. The input signal is a 5GHz sine-wave, which is used to emulate the effect of a 10Gb/s 0101...0101... digital data. The input signal for the measurement is provided by an HP83731B 1-20GHz Synthesized Signal Generator. The output transient signals are captured by a LeCroy Wavemaster 8600A 6G oscilloscope. It is necessary to use a Hi-Z probe adapter for the oscilloscope to detect the actual output signal of the proposed TIA. However, our Hi-Z probe cannot provide sufficient bandwidth in this case. The probe adapter we use for the oscilloscope is a low-impedance (50Ω) one to detect the 5GHz high frequency signal. The magnitude of the TIA output impedance at 5GHz is about 100Ω according to the network analyzer measurement result. Therefore, the measured output transient voltage amplitude is about 1/3 of the actual one.

Figure 3.15 is the output transient response with -25dBm signal generator power. If we assume a 50Ω input matching and consider there is about 2dB loss through the RF cables. The actual available power to the TIA is about $-25 - 2 - 3 = -30\text{dBm}$, which means the corresponding peak amplitude of the sine-wave input current is about 0.2mA. The measured output voltage peak amplitude is about 23.6mV (peak-to-peak 47.17mV). This translates to an actual

output transient voltage peak amplitude of $23.6 \times 3 = 70.8 \text{ mV}$, which means the transimpedance gain at 5GHz is about 354Ω (50.9dB Ω). The above calculation is just a rough estimation since it is very difficult to precisely characterize the losses in the measurement. The whole chip size is $0.6 \times 0.6 \text{ mm}^2$ including pads while the core circuit occupies only $0.45 \times 0.25 \text{ mm}^2$ and dissipates 13.5mW DC power from a single 1.8V supply.

Figure 3.15: Measured output transient response of the proposed TIA with -25dBm signal generator power

In Summary, a novel bandwidth enhancement method for broadband transimpedance amplifier design is proposed, which is based on a unique combination of capacitive degeneration, regulated cascode input stage and broadband matching network. The noise performance of the proposed TIA is discussed based on the equivalent input noise current expressed in terms of the E_n -

I_n pair, which could be used to evaluate the input referred noise current of a given TIA with arbitrary input matching network. A prototype CMOS transimpedance amplifier is implemented based on the proposed broadband design technique, which turns the TIA design to a problem of solving a fifth-order low-pass filter with maximally-flat gain frequency response. The overall bandwidth extension, based on measured data, is from 2.2GHz to 8GHz, which translates to an enhancement ratio of 3.6. Table 3.1 lists the performance comparison of four 10Gb/s TIAs. In most aspects, this work achieves comparable performance to those III-V and SiGe counterparts while possessing the merits of the CMOS technology.

Table 3.1: Performance comparison of 10Gb/s TIAs

Design	[30]	[34]	[70]	This design
Technology	0.1 μ m pHEMT	0.25 μ m BiCMOS	0.18 μ m CMOS	0.18 μ m CMOS
Bandwidth (GHz)	8@0.25pF	9@0.1pF	9.2@0.5pF	8@0.25pF
Gain (dB Ω)	63.3	55	54	53
Power consumption (mW)	500@5V single-ended	140@5V differential	130@2.5V single-ended	13.5@1.8V single-ended
Input-referred noise (pA/sqrtHz)	6.5	14	17	18
Chip area (mm ²)	1.6x1.3	NA	0.8x0.8	0.45x0.25
Group delay (ps)	+/-40	+/-10	+/-25	+/-20

3.6 Extended noise analysis of the RGC input stage

In the noise analysis of the RGC input stage in Section 3.3, we have neglected the effect of the induced gate noise for the purpose of mathematical simplicity. Such simplification is made also because although the induced gate noise adds to

the total input referred input noise directly, its correlation with the channel thermal noise helps to reduce the total input noise [101]. As we will see from the analysis and discussion in Chapter 4, such simplification is reasonable if there is nearly no design headroom for noise optimization and the gain-bandwidth product is the first design priority. In this section, we will revisit the noise characteristics of the RGC TIA input stage based on the van der Ziel MOSFET noise model [110] that includes the channel thermal noise, the induced gate noise and their cross-correlation. The small signal circuit of the RGC TIA input stage for noise analysis based on the van der Ziel MOSFET noise model including the channel thermal noise, the induced gate noise and their cross-correlation is illustrated in Figure 3.16.

Figure 3.16: Small circuit model of RGC input stage for noise analysis based in van der Ziel MOSFET noise model

Based on Figure 3.16, the transfer function is given by

$$Z_T(s) \approx \frac{g_{m1} \left(g_{m2} + \frac{1}{R_2} \right)}{\left(\frac{1}{R_1} + sC_o \right) \left[\left(g_{m2} + \frac{1}{R_2} \right) (g_{m1} + sC_j) + \left(\frac{1}{R_2} + sC_j \right) \left(\frac{1}{R_s} + sC_{in} \right) \right]} \quad (3.38)$$

where $C_i \approx C_{sb1} + C_{gs2}$, $C_j \approx C_{gs1} + C_{gd2}$, $C_{in} \approx C_{pd} + C_i$ and $C_o \approx C_L + C_{gd1} + C_{db1}$.

According to Figure 3.16 and applying small signal analysis, we can obtain the equivalent input noise current components contributed by each noise sources illustrated in Figure 3.16. Starting from the left of Figure 3.16, the equivalent input noise current spectral density contributed by R_s is given by

$$N_{n,Rs} \approx \frac{4KT}{R_s} \quad (3.39)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_2 is given by

$$N_{n,g2} \approx 4KT\delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \quad (3.40)$$

The equivalent input noise current spectral density contributed by the channel thermal noise of M_1 is given by

$$N_{n,d1} \approx 4KT\gamma g_{d0,1} \left(\left| \frac{Z_o}{Z_T} \right|^2 - 1 \right) \approx 4KT\gamma g_{d0,1} \frac{\omega^2}{g_{m1}^2} \left(C_j + \frac{C_{pd}}{1 + g_{m2}R_2} \right)^2 \quad (3.41)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_1 is given by

$$N_{n,g1} \approx 4KT\delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} \left| 1 - j\omega \frac{C_{in}}{g_{m2} + \frac{1}{R_2}} \right|^2 = 4KT\delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} \left[1 + \frac{\omega^2 C_{in}^2}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \right] \quad (3.42)$$

The equivalent input noise current spectral density contributed by the thermal noise of R_2 is given by

$$N_{n,R2} \approx \frac{4KT}{R_2} \frac{\omega^2 (C_{pd} + C_i)^2}{\left(g_{m2} + \frac{1}{R_2} \right)^2} = \frac{4KT}{R_2} \frac{\omega^2 C_{in}^2}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \quad (3.43)$$

The equivalent input noise current spectral density contributed by the channel thermal noise of M_2 is given by

$$N_{n,d2} \approx 4KT\gamma g_{d0,2} \frac{\omega^2(C_{pd} + C_i)^2}{\left(g_{m2} + \frac{1}{R_2}\right)^2} = 4KT\gamma g_{d0,2} \frac{\omega^2 C_{in}^2}{\left(g_{m2} + \frac{1}{R_2}\right)^2} \quad (3.44)$$

The equivalent input noise current spectral density contributed by the thermal noise of R_l is given by

$$N_{n,R1} \approx \frac{4KT}{R_l} \left| \frac{Z_o}{Z_T} \right|^2 \approx \frac{4KT}{R_l} \left[1 + \frac{\omega^2}{g_{m1}^2} \left(C_j + \frac{C_{pd}}{1 + g_{m2}R_2} \right)^2 \right] \quad (3.45)$$

The channel thermal noise and the induced gate noise are cross-correlated. According to (3.41), (3.42) and the analysis in Section 2.7, the correlated noise of i_{g1} and $i_{n,d1}$ is

$$N_{n,c1} \approx -2|c| \frac{\omega}{g_{m1}} \left(C_j + \frac{C_{pd}}{1 + g_{m2}R_2} \right) \sqrt{i_{g1}^2 i_{n,d1}^2} \quad (3.46)$$

According to (3.40), (3.44) and the analysis in Section 2.7, the correlated noise of i_{g2} and $i_{n,d2}$ is given by

$$N_{n,c2} \approx -2|c| \frac{\omega C_{in}}{g_{m2} + \frac{1}{R_2}} \sqrt{i_{g2}^2 i_{n,d2}^2} \quad (3.47)$$

The total equivalent input noise current spectral density can be obtained by summing up the noise components from (3.39) to (3.47), which is given by

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \begin{aligned} & \frac{1}{R_s} + \frac{1}{R_1} + \delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} (1-|c|^2) + \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} (1-|c|^2) \\ & + \frac{\omega^2}{g_{m1}^2} \left(C_j + \frac{C_{pd}}{1+g_{m2}R_2} \right)^2 \left[\frac{1}{R_1} + \mathcal{R}_{d0,1} \left(1 - \frac{C_{gs1}}{C_j + \frac{C_{pd}}{1+g_{m2}R_2}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] \\ & + \frac{\omega^2 C_{in}^2}{\left(g_{m2} + \frac{1}{R_2} \right)^2} \left[\frac{1}{R_2} + \mathcal{R}_{d0,2} \left(1 - \frac{C_{gs2}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 + \delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} \right] \end{aligned} \right\} \quad (3.48)$$

In Equations (3.39) to (3.48), K is the Boltzmann constant, T is the absolute temperature, γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, $Z_o \approx R_1 // \frac{1}{s(C_L + C_{gd1} + C_{db1})}$, Z_T is given by (3.52) and $\alpha = \frac{g_m}{g_{d0}}$. For

long channel devices, $\gamma = 2/3$ and $\alpha = 1$. For short channel devices, γ can be much greater than 1 and $\alpha < 1$. Typically, δ is 4/3 for long-channel devices and increases in short-channel devices [101] [109-114]. According to (3.48), the correlated noise actually helps to reduce the total input referred noise. With a large magnitude of the correlation coefficient in deep submicron devices, the total input referred noise current can be reduced by a considerable amount for *optimum* transistor size [101].

3.7 Summary

In this chapter, a novel broadband transimpedance amplifier based on the combination of a regulated cascode input stage, capacitive degeneration and the broadband input matching network is proposed and silicon verified using CHRT 0.18 μ m RFCMOS technology. This design shows that, in most aspects, CMOS

TIAs are capable to achieve comparable performances to those HEMT/HBT counter parts with the help of circuit design techniques. An extended noise analysis based on the complete van der Ziel MOSFET noise model is also carried out for the well-known regulated cascode input stage for the purpose of a more precise understanding of the noise characteristics of the RGC stage, which is original and has not been done before in any publications to the author's knowledge. A part of this chapter has been published in the paper "Broad-Band design techniques for transimpedance amplifiers," *IEEE Transactions on Circuits and Systems —I: Regular papers*, Vol. 54, No. 3, March 2007, pp. 590 – 600.

Chapter 4

Design of a CMOS Broadband Transimpedance Amplifier with Active Feedback

4.1 Introduction

Traditional optical receiver front-end circuits and devices are usually dominated by HEMT, HBT or Si Bipolar technologies due to their speed and noise advantages. However, due to the following reasons CMOS technology is becoming popular in short range optical communications, such as the 10G Ethernet very-short-reach (VSR) application [18-20]. First, short-reach 10Gb/s data communication standards (OC-192c VSR, 10Gb/s Ethernet) have been specified with relaxed optical sensitivity requirements comparing to those long-haul optical transmission standards, which subsequently alleviate the design challenges using CMOS technology. Second, the requirement of high volume, wide deployment of optical components in short-reach communication applications inevitably brings the cost factor to the top of all design considerations. Third, low-cost 850nm vertical cavity surface emitting lasers (VCSEL) are widely used for optical transmitters in short-reach applications and 10Gb/s CMOS compatible silicon photodetectors demonstrating more than 0.3A/W responsivity in the 850nm wavelength range have been reported [84-85], making fully integrated CMOS optical receiver a good low-cost match for the 850nm VCSEL transmitter [18-23]. Finally, deep-submicron RFCMOS transistors are well capable of high-frequency operations.

With the help of carefully studied circuit design techniques, CMOS optical preamplifiers are also able to achieve comparable performances to those HBT, HEMT or Si Bipolar counterparts and maintain the merits of low-power, low-cost, high-integration and high-manufacturability [24] [66].

CMOS transimpedance amplifiers usually employ current-mode topology realized with common gate input stage to provide low input impedance [55] [104]. Regulated cascode input stage [63] [72] is essentially a common gate configuration with active feedback to provide even lower input impedance than a simple common gate input stage does. Therefore, better isolation of the input parasitic capacitance from bandwidth determination can be achieved. This chapter examines another type of current-mode TIA input topology based on the common gate input stage with common source active feedback, which provides as low input impedance as the RGC configuration does. Hence, the influence on the TIA bandwidth by the relatively large input capacitance including the photodetector capacitance can be greatly reduced. The proposed TIA design employs series inductive peaking to boost the bandwidth. A two-stage capacitive degeneration is used to further extend the bandwidth and boost the gain, which will be analyzed in detail in Section 4.2.

The proposed TIA design exploiting the common gate input stage with common source active feedback has been realized using CHRT 0.18 μ m RFCMOS technology. The proposed current-mode TIA input topology with active feedback is introduced in Section 4.2. The mathematical analysis of the proposed TIA design is presented in Sections 4.3. The detailed noise analysis of the proposed TIA is provided in Section 4.4, which includes the induced gate noise. The measurement shows a transimpedance gain of about 54.6dB Ω (540 Ω) and a -3dB bandwidth of

about 7GHz for a total input parasitic capacitance of 0.3pF. The measured average input referred noise current spectral density is about $17.5 \text{ pA}/\sqrt{\text{Hz}}$ up to 7GHz. The measured group delay is within $65 \pm 10 \text{ ps}$ over the bandwidth of interest. The chip consumes 18.6mW DC power from a single 1.8V supply. In Section 4.3, the noise performance of the proposed TIA is also analyzed in detail based on the van der Ziel MOSFET noise model [110] including the channel thermal noise, the induced gate noise and their cross-correlation. The effect of the induced gate noise in a broadband transimpedance amplifier is discussed.

4.2 Common gate input stage with common source active feedback

Figure 4.1: (a) The proposed common gate TIA input stage with common source active feedback. (b) RGC (regulated cascode) input stage.

Figure 4.1 (a) shows the proposed common gate TIA input stage with common source active feedback. Before our analysis on this topology, a brief review of the RGC input configuration is necessary for the purpose of comparison. It is well known that the regulated cascode (RGC) input stage [63] illustrated in Figure 4.1

(b) is able to provide very low input impedance. The low frequency input resistance of the RGC topology is given by

$$Z_{in,RGC}(0) \approx \frac{1}{g_{m1}(1 + g_{m2}R_2)} \quad (4.1)$$

The low frequency transimpedance gain of the RGC input stage is given by

$$R_{T,RGC} = Z_{T,RGC}(0) \approx R_1 \quad (4.2)$$

The transfer function of the RGC input stage is given by [63]

$$Z_{T,RGC}(s) = \frac{v_o}{i_{pd}} \approx \frac{R_1}{\left[1 + s \frac{C_{pd} + C_i}{g_{m1}(1 + g_{m2}R_2)}\right] [1 + sR_1(C_L + C_o)]} \quad (4.3)$$

where C_{pd} is the photodiode capacitance, $C_i \approx C_{sb1} + C_{gs2}$, $C_o \approx C_{gd1} + C_{db1}$ and C_L is the load capacitance due to the subsequent stage. From (4.3) we find that there are mainly two poles affecting the -3dB bandwidth,

namely $\omega_{i,RGC} = \frac{g_{m1}(1 + g_{m2}R_2)}{C_{pd} + C_i}$ and $\omega_{1,RGC} = \frac{1}{R_1(C_L + C_o)}$. $\omega_{i,RGC}$ is determined at

the input node and $\omega_{1,RGC}$ is determined at the drain of M_1 . Due to the very small input resistance, $\omega_{i,RGC} > \omega_{1,RGC}$ and the dominant pole is $\omega_{1,RGC}$. Nevertheless, $\omega_{i,RGC}$ also contributes to the total roll-off effect and the actual -3dB bandwidth is

$$f_{-3dB,RGC} < \frac{\omega_1}{2\pi} \quad (4.4)$$

There is one alternative to the RGC input configuration in the form of common gate input stage with common source active feedback, which is shown in Figure 4.1 (a). The NMOS transistor M_1 is the common gate input transistor and the PMOS transistor M_2 provides the active feedback.

Figure 4.2: Small-signal circuit model of the proposed common gate TIA input stage with common source active feedback

Figure 4.2 shows the small-signal circuit model of the active feedback input stage of Figure 4.1 (a) with a simple photodetector model included. Based on the small-signal circuit analysis we obtain

$$Z_{in,CGA}(s) = \frac{v_i}{i_i} \approx \frac{\frac{1}{R_1} + s(C_2 + C_{gd2} + C_L)}{\left[\frac{1}{R_s} + g_{m1} + s(C_1 + C_{gd2}) \right] \left(\frac{1}{R_1} + s(C_2 + C_{gd2} + C_L) \right) + (g_{m1} + sC_{gd2})(g_{m2} - sC_{gd2})} \quad (4.5)$$

where $C_1 \approx C_{gs1} + C_{sb1} + C_{db2}$, $C_2 \approx C_{gs2} + C_{gd1} + C_{db1}$. The low frequency input resistance is given by

$$Z_{in,CGA}(0) \approx \frac{1}{g_{m1}(1 + g_{m2}R_1)} \quad (4.6)$$

The transfer function of the proposed TIA input stage including the photodetector parasitic capacitance is given by

$$Z_{T,CGA}(s) = \frac{v_o}{i_{pd}} \approx \frac{(g_{m1} + sC_{gd2})}{\left[\frac{1}{R_s} + g_{m1} + s(C_{pd} + C_1 + C_{gd2}) \right] \left[\frac{1}{R_1} + s(C_L + C_2 + C_{gd2}) \right] + (g_{m1} + sC_{gd2})(g_{m2} - sC_{gd2})} \quad (4.7)$$

The low frequency transimpedance gain can be derived from (4.7) as

$$R_{T,CGA} = Z_{T,CGA}(0) \approx \frac{R_1}{1 + g_{m2}R_1} = R_1 // \frac{1}{g_{m2}} \quad (4.8)$$

Comparing (4.1) with (4.6) we can find that the input impedance of RGC topology and the proposed active feedback topology is quite similar. The RGC configuration employs an extra resistor R_2 that is absent in the proposed active feedback configuration. Therefore, the advantage of the proposed active feedback topology is with less noise sources. However, it can be inferred from (4.2) and (4.8) that the gain of the proposed active feedback topology is less than the RGC stage. In RGC topology, a large g_{m2} is required and R_2 needs to be small to maintain stability [63]. In the proposed active feedback configuration, as we can infer from (4.6) and (4.8), it is desirable to choose large R_1 and small g_{m2} to achieve low input resistance and maintain a relatively high gain. Moreover, the channel thermal noise $4KT\gamma g_{d0,2}$ of M_2 adds to the total input-referred noise current directly, where γ is the noise factor of the MOSFET, $g_{d0,2}$ is the zero-bias drain conductance of M_2 . Therefore, keeping the size of M_2 small is both desirable for gain and noise performances. By selecting an M_2 with small size (C_{gd2} very small) and assuming the value of R_s is relatively large, (4.7) can be simplified to

$$\begin{aligned}
 Z_{T,CGA}(s) &\approx \frac{R_1}{1 + g_{m2}R_1} \frac{1}{1 + s \left[\frac{R_1(C_L + C_2)}{1 + g_{m2}R_1} + \frac{C_{pd} + C_1}{g_{m1}(1 + g_{m2}R_1)} \right] + s^2 \frac{R_1(C_L + C_2)(C_{pd} + C_1)}{g_{m1}(1 + g_{m2}R_1)}} \\
 &= R_{T,CGA} \frac{1}{1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2}}
 \end{aligned} \tag{4.9}$$

where $R_{T,CGA}$ is given by (4.8), $\omega_n = \sqrt{\omega_i \omega_1}$, $Q = \frac{(1 + g_{m2}R_1)\sqrt{\omega_i \omega_1}}{\omega_i + (1 + g_{m2}R_1)\omega_1}$ with

$$\omega_i = \frac{g_{m1}(1 + g_{m2}R_1)}{C_{pd} + C_1} \tag{4.10}$$

$$\omega_1 = \frac{1}{R_1(C_L + C_2)} \tag{4.11}$$

where ω_i is determined at the input node and ω_1 is determined at the drain of M_1 .

Because of the small input resistance, the dominant pole is ω_1 and $\omega_i > \omega_1$. (4.9) is a typical second-order system with -3dB bandwidth higher than the dominant pole.

For Butterworth response, the -3dB cut-off frequency is $f_{-3dB} = \frac{\omega_n}{2\pi}$ and

$$Q = \frac{(1 + g_{m2}R_1)\sqrt{\omega_i \omega_1}}{\omega_i + (1 + g_{m2}R_1)\omega_1} = \frac{\sqrt{2}}{2} \tag{4.12}$$

The bandwidth extension ratio is

$$\mathfrak{R} = \frac{\omega_n}{\omega_1} = \sqrt{\frac{\omega_i}{\omega_1}} \tag{4.13}$$

If we design $\omega_i = 2\omega_1$. The -3dB cut-off frequency is

$$f_{-3dB, \text{butterworth}} = \frac{\omega_n}{2\pi} = \sqrt{2} \frac{\omega_1}{2\pi} \tag{4.14}$$

According to (4.12), we need to design $g_{m2}R_1 = 1$ if $\omega_i = 2\omega_1$. The -3dB cut-off frequency is about 41% higher than the dominant pole ω_1 in the above case.

Comparing (4.4) with (4.14), we can find that the proposed common gate TIA input stage with common source active feedback topology is advantageous over the RGC input configuration in terms of speed at the cost of lower gain. Suppose all other conditions to be the same, i.e. the noise contributed by R_1 , M_1 and R_s are roughly the same for both topologies. The input noise contributed by the proposed active feedback topology is about $4KT\gamma g_{d0,2}$. The input noise due to M_2/R_2 of the

RGC stage is roughly $\frac{4KT\left(\gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2} \left[\frac{1}{R_s^2} + \omega^2 (C_{pd} + C_i)^2 \right]$ [63]. The proposed

TIA input stage presents less noise than the RGC input stage does as frequency increases. However, because the gain of the proposed topology is less, the noise due to the subsequent stages will be higher. Therefore, the noise performance of the proposed topology and the RGC stage should be similar.

4.3 Design of a broadband TIA with proposed active feedback topology

In this section, a transimpedance amplifier incorporating the proposed TIA input stage in Figure 4.1 (a) is presented and analyzed. Figure 4.3 (a) shows the proposed TIA schematic consists of a simple photodetector model. The series input inductor L_I is used for bandwidth extension. The gate of M_I is biased using $[R_{b1}, R_{b2}, C_b]$. According to our discussion in Section 4.2, the proposed TIA input topology provides good bandwidth performance at the expense of gain. Therefore, a two-stage capacitive degeneration $[M_3, R_3, R_{s3}, C_{s3}]$ and $[M_4, R_4, R_{s4}, C_{s4}]$ is employed to provide extra gain and boost the bandwidth at the same time.

The output impedance of a discrete TIA typically needs to be matched to 50Ω to drive the transmission line. However, the trend is to integrate the TIA with the main amplifier on one chip [28], thereby avoiding the inter-stage 50Ω matching. Our design goal is to integrate the proposed TIA with the main amplifier in the future. Therefore, the output load is not matched to 50Ω to relax the gain and power dissipation trade-offs. The low-frequency transimpedance gain is given by

$$Z_T(0) = R_T \approx \frac{R_1}{1 + g_{m2}R_1} \frac{g_{m3}R_3}{1 + g_{m3}R_{s3}} \frac{g_{m4}R_4}{1 + g_{m4}R_{s4}} \quad (4.15)$$

Figure 4.3: (a) Circuit schematic of the proposed TIA design. (b) Its small-signal circuit model

Figure 4.3 (b) shows the small-signal circuit model of the proposed TIA. The two-stage capacitive degeneration part is simplified to a voltage amplifier model

with transfer function $Tx(s)$. The output load capacitor C_{Lo} is mainly due to the parasitic capacitance of the output pad, which is around $100fF$ in this design. According to Figure 4.3 (b), the complete transfer function of the TIA circuit is given by

$$Z_{T,TIA}(s) = \frac{v_{out}}{i_{pd}} \approx Z_{T,CGA}(s) \cdot Tx(s) \quad (4.16)$$

where $Z_{T,CGA}(s)$ is the transfer function of the proposed TIA input stage with series inductive peaking, which is given by

$$Z_{T,CGA}(s) = \frac{v_o}{i_{pd}} \approx \frac{g_{m1} + sC_{gd2}}{\left\{ (g_{m1} + sC_{gd2})(g_{m2} - sC_{gd2}) + \left(\frac{1}{R_s} + g_{m1} + sC_1 \right) \left[\frac{1}{R_1} + s(C_L + C_2 + C_{gd2}) \right] + \left[1 + sL_1 \left(\frac{1}{R_s} + g_{m1} + sC_1 \right) \right] \left[\frac{1}{R_1} + s(C_L + C_2 + C_{gd2}) \right] s(C_i + C_{gd2}) \right\}} \quad (4.17)$$

where $C_i \approx C_{pd} + C_{db2}$, $C_1 \approx C_{gs1} + C_{sb1}$, $C_2 \approx C_{gs2} + C_{gd1} + C_{db1}$ and C_L is the load capacitance due to the second stage, which is approximately the sum of the Miller capacitances of C_{gd3} and C_{gs3} . As mentioned in Section II, M_2 is designed with small size. Comparing to other parts, C_{gd2} is negligible. Assuming the resistance of R_s is relatively large, (4.17) can be simplified to

$$Z_{T,CGA}(s) = \frac{v_o}{i_{pd}} \approx \frac{R_1}{g_{m2}R_1 + \left(1 + s \frac{C_1}{g_{m1}} \right) [1 + sR_1(C_L + C_2)] + (1 + sg_{m1}L_1 + s^2L_1C_1)[1 + sR_1(C_L + C_2)]s \frac{C_i}{g_{m1}}} \quad (4.18)$$

In Figure 4.3, $Tx(s) = \frac{v_{out}}{v_o}$ is the transfer function of the two-stage capacitive degeneration part, where v_{out} is the small-signal output voltage and v_o is the small-signal voltage at the drain node of M_1 . The first capacitive degeneration gain stage $[M_3, R_3, R_{s3}, C_{s3}]$ contributes a zero $\omega_2 = (R_{s3}C_{s3})^{-1}$ that can be used to compensate part of the roll-off effect due to the input stage. Besides this zero, the capacitive degeneration also generates an additional pole $\omega_3 = (1 + g_{m3}R_{s3})/R_{s3}C_{s3}$ at a considerably higher frequency. Because we also need this stage to provide extra gain, the resistance of R_3 is designed to be relatively large. The frequency of the pole ω_3 is not high enough with a small R_{s3} . Similarly, the second capacitive degeneration stage $[M_4, R_4, R_{s4}, C_{s4}]$ generates a zero at $\omega_4 = (R_{s4}C_{s4})^{-1}$, which is used to cancel the pole determined at the drain node of M_3 . The second capacitive degeneration stage also creates a pole $\omega_5 = (1 + g_{m4}R_{s4})/R_{s4}C_{s4}$ at a considerably higher frequency. After the bandwidth extension by the two-stage capacitive degeneration, the -3dB bandwidth of the TIA is mainly determined by the pole located at the output node $\omega_0 = (R_4C_{LO})^{-1}$, which is at about $\frac{1}{2\pi \cdot 300\Omega \cdot 100fF} \approx 5.3GHz$ in this design. Nevertheless, the other poles at considerably higher frequencies such as ω_3 and ω_5 also contribute to the total roll-off effect. For the purpose of analysis simplicity, we neglect all other poles at higher frequencies. Based on the above discussion, the transfer function $Tx(s)$ in Figure 4.3 (b) is given by

$$Tx(s) = \frac{v_{out}}{v_o} \approx \frac{g_{m3}R_3}{1 + g_{m3}R_{s3}} \frac{g_{m4}R_4}{1 + g_{m4}R_{s4}} \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_0}} \quad (4.19)$$

The zero $\omega_2 = (R_{s3}C_{s3})^{-1}$ is used to compensate part of the roll-off effect due to the input stage. The pole $\omega_0 = (R_4C_{Lo})^{-1}$ is determined at the output node. The complete transfer function of the proposed TIA is therefore given by

$$Z_{T,TIA}(s) = \frac{v_{out}}{i_{pd}} \approx Z_{T,CGA}(s) \cdot Tx(s) \approx \frac{R_{TX}}{g_{m2}R_1 + \left(1 + s \frac{C_1}{g_{m1}}\right) \left(1 + \frac{s}{\omega_1}\right) + \left(1 + sg_{m1}L_1 + s^2L_1C_1\right) \left(1 + \frac{s}{\omega_1}\right) s \frac{C_i}{g_{m1}}} \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_0}} \quad (4.20)$$

where $C_i \approx C_{pd} + C_{db2}$, $C_1 \approx C_{gs1} + C_{sb1}$, $C_2 \approx C_{gs2} + C_{gd1} + C_{db1}$, C_L is the same as

that defined in (4.18), $R_{TX} = R_1 \frac{g_{m3}R_3}{1 + g_{m3}R_{s3}} \frac{g_{m4}R_4}{1 + g_{m4}R_{s4}}$, $\omega_1 \approx [R_1(C_L + C_2)]^{-1}$,

ω_0 and ω_2 is defined in (4.19). Equation (4.20) is a fourth order system. As mentioned previously, the zero ω_2 is used to compensate part of the roll-off effect due to the input stage. Because of this zero in the numerator of (4.20), the transfer function cannot be resolved to a standard Butterworth response. To investigate the frequency response of the proposed TIA regarding the bandwidth extension effect by the capacitive degeneration and the series inductive peaking, we reorganize (4.20) to

$$Z_{T,TIA}(s) \approx R_T \frac{1 + c_1x}{(1 + a_1x + a_2x^2 + a_3x^3 + a_4x^4)(1 + b_1x)} \quad (4.21)$$

where R_T is given by (4.15), $x = s/\omega_n = j\omega/\omega_n$ and

$$a_1 = \omega_n \left(\frac{1}{\omega_1} + \frac{C_1 + C_i}{g_{m1}} \right) / (1 + g_{m2}R_1) \quad (4.22)$$

$$a_2 = \omega_n^2 \left(\frac{C_1 + C_i}{\omega_1 g_{m1}} + L_1 C_i \right) / (1 + g_{m2} R_1) \quad (4.23)$$

$$a_3 = \omega_n^3 L_1 C_i \left(\frac{1}{\omega_1} + \frac{C_1}{g_{m1}} \right) / (1 + g_{m2} R_1) \quad (4.24)$$

$$a_4 = \omega_n^4 \frac{L_1 C_i C_1}{\omega_1 g_{m1}} / (1 + g_{m2} R_1) \quad (4.25)$$

$$b_1 = \frac{\omega_n}{\omega_0} \quad (4.26)$$

$$c_1 = \frac{\omega_n}{\omega_2} \quad (4.27)$$

When $|x| = 1$, which means $\omega = \omega_n$, Equation (4.21) becomes

$$Z_{T,TIA}(\omega_n) \approx R_T \frac{1 + jc_1}{[(1 + a_4 - a_2) + j(a_1 - a_3)](1 + jb_1)} \quad (4.28)$$

If we want $\omega_n / 2\pi$ to be the -3dB cut-off frequency $\omega_c / 2\pi$, we can write

$$a_1 = a_3 \quad (4.29)$$

$$\sqrt{\frac{1 + c_1^2}{1 + b_1^2}} \frac{1}{|1 + a_4 - a_2|} = \frac{\sqrt{2}}{2} \quad (4.30)$$

From (4.29) we obtain

$$\omega_n^2 = \frac{\left(\frac{1}{\omega_1} + \frac{C_1 + C_i}{g_{m1}} \right)}{L_1 C_i \left(\frac{1}{\omega_1} + \frac{C_1}{g_{m1}} \right)} \quad (4.31)$$

In this design, because of the gain and noise requirement, we set $g_{m2} R_1 = 1$ with $g_{m2} = 2mS$ and $R_1 = 500\Omega$. The dominant pole ω_1 at the drain of M_1 is at about 1.8GHz when $R_1 = 500\Omega$. According to (4.9), the -3dB bandwidth of the proposed TIA input stage without the subsequent capacitive degeneration and the input

inductive peaking should be somewhat higher than the dominant pole. As mentioned previously, after the bandwidth extension by the two-stage capacitive degeneration, the -3dB bandwidth is determined by ω_0 . According to (4.21) and (4.26), it is desirable to design ω_0 as high as possible. However, due to the gain-bandwidth trade-off, we can only make ω_0 as high as $2\pi \cdot 5.3\text{GHz}$ with about 55dB Ω transimpedance gain according to the calculation. For a typical 10Gb/s TIA, the bandwidth is usually around 0.6B to 0.7B if the receiver bandwidth is set by the TIA, where B stands for the bit rate. Therefore, the bandwidth of the core TIA is not enough and additional bandwidth extension is to be achieved by inductive peaking with the inductor L_I . The bandwidth extension using series inductor has been extensively studied in numerous publications such [55] [71] [74].

Now we start to solve Equations (4.22) to (4.31) on conditions that $g_{m2} = 2\text{mS}$, $R_1 = 500\Omega$, $\omega_1 \approx 2\pi \cdot 1.8\text{GHz}$, $\omega_0 \approx 2\pi \cdot 5.3\text{GHz}$ and $\frac{g_{m1}}{C_1} \approx 2\pi f_T \approx 2\pi \cdot 60\text{GHz}$. By numerical calculation and assuming the input parasitic capacitance C_i , which includes the photodiode capacitance, is 300fF, we obtain $L_1 \approx 1.4\text{nH}$, $\omega_n \approx 2\pi \cdot 8.6\text{GHz}$, $g_{m1} \approx 15\text{mS}$, $a_1 = a_3 \approx 3.01$, $a_2 \approx 3.601$, $a_4 \approx 0.521$, $b_1 \approx 1.62$ and $c_1 \approx 2.61$.

As mentioned previously, (4.21) cannot be resolved to standard Butterworth response due to the zero ω_2 . Equations (4.32), (4.33) and (4.34) are the normalized transfer function of the proposed TIA circuit, the transfer function with fourth-order Butterworth response and the transfer function with fourth-order Bessel response, respectively.

$$Z_{T,TIA,normalized}(s) \approx \frac{1 + c_1 x}{(1 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4)(1 + b_1 x)} \quad (4.32)$$

$$Z_{\text{Butterworth,normalized}}(s) = \frac{1}{1 + 2.613x + 3.414x^2 + 2.613x^3 + x^4} \quad (4.33)$$

$$Z_{\text{Bessel,normalized}}(s) = \frac{1}{1 + 3.240x + 4.5x^2 + 3.240x^3 + 1.050x^4} \quad (4.34)$$

Figure 4.4 shows the MATLAB calculated frequency response based on (4.32), (4.33) and (4.34) for the purpose of comparison. In Figure 4.4, the y-axis is the normalized gain and the x-axis is the normalized frequency $x = j\omega / \omega_n = s / \omega_n$. The frequency is normalized to $\omega_n / 2\pi \approx 8.6\text{GHz}$. With $c_1 \approx 2.61$, although a -3dB bandwidth of $\omega_c / 2\pi = \omega_n / 2\pi \approx 8.6\text{GHz}$ is achieved, the frequency response exhibits nearly 20% overshoot. By numerical analysis, we are able to obtain a very close to maximally-flat gain frequency response when $c_1 \approx 2.15$ with other polynomial coefficients unchanged. The -3dB cut-off frequency in this case is about $\omega_c / 2\pi \approx 0.93\omega_n / 2\pi \approx 8\text{GHz}$, which is calculated using MATLAB. Therefore, the finalized frequency response of our proposed TIA circuit is shown by curve “c” in Figure 4.4 with a -3dB bandwidth of 8GHz. As shown in Figure 4.4, the proposed frequency response is between the Butterworth response with maximally-flat gain and the Bessel response with maximally-flat group delay. The finalized transfer function is

$$Z_{T,TIA}(s) \approx R_T \frac{1 + 2.15x}{(1 + 3.01x + 3.601x^2 + 3.01x^3 + 0.521x^4)(1 + 1.62x)} \quad (4.35)$$

where R_T is given by (4.15) and $x = s / \omega_n = j\omega / \omega_n$. Based on the above analysis, all design parameters can be calculated.

Figure 4.4: MATLAB calculated normalized frequency response

Using the calculated design parameters and based on (4.32), Figure 4.5 shows the normalized frequency response of the proposed TIA under different conditions plotted by MATLAB. In Figure 4.5, curve “a” is without input inductive matching and capacitive degeneration, which has a -3dB bandwidth of about $\omega_c / 2\pi \approx 0.26\omega_n / 2\pi \approx 2.25GHz$. This bandwidth is higher than the dominant pole at 1.8GHz, which confirms our discussion based on Equations (4.9) to (4.14). Curve “b” of Figure 4.5 is with capacitive degeneration but without inductive peaking, which has a -3dB bandwidth of about $\omega_c / 2\pi \approx 0.55\omega_n / 2\pi \approx 4.7GHz$. After the bandwidth extension by capacitive degeneration and input inductive peaking, the -3dB bandwidth is $\omega_c / 2\pi \approx 0.93\omega_n / 2\pi \approx 8GHz$, which is shown by curve “c” in Figure 4.5. The bandwidth extension ratio by the series inductive peaking is about $8/4.7 \approx 1.7$.

Figure 4.5: MATLAB calculated frequency response of the propose TIA design under different conditions

4.4 Noise analysis of the proposed TIA

According to the discussion in Chapter 2, the noise characteristics of the transimpedance preamplifier in terms of the input referred noise current spectral density or the equivalent input noise current spectral density is of primary importance in the determination of the sensitivity performance of the whole optical receiver front-end.

In this section, we will first investigate the equivalent input noise current characteristics of the proposed common gate TIA input stage with common source active feedback shown in Figure 4.1 (a). Next, the noise characteristics of the proposed TIA with noise reduction effect provided by the series input inductor L_I shown in Figure 4.3 (a) will be analyzed. The noise analysis is based on the van der Ziel MOSFET noise model [110] including the channel thermal noise, induced

gate noise and their cross-correlation. According to the van der Ziel MOSFET noise model explained in Section 2.7, the dominant noise source of a MOSFET is the channel thermal noise while the induced gate noise and its correlation with the channel thermal noise are also considerable at very high frequencies. Although the equivalent input noise contributed by the induced gate noise adds directly to the equivalent input noise contributed by the channel thermal noise, their correlated noise helps to reduce the total equivalent input noise. According to our discussion in Section 2.7, the amplitude of the correlation coefficient in deep submicron CMOS devices can take a value of more than 0.75 [101], which can help to reduce the total input noise especially at very high frequencies. According to [101], such kind of noise reduction at optimum transistor size is considerable in short channel MOSFETs. However, the optimum transistor size for best noise performance might be too large to meet the bandwidth requirement at the same time. As we will see from the analysis and discussion in this section, the noise reduction effect due to the correlated noise is not significant if the gain-bandwidth product requirement is of first priority. The noise analysis only considering the channel thermal noise is usually sufficient for noise estimation of a broadband TIA.

Before we start to derive the total input referred noise current spectral density contributed by each of the noise sources of the proposed TIA input stage in Figure 4.1 (a), we will first derive the equivalent input noise current spectral density contributed by R_I as an example. The circuit schematic in Figure 4.6 is used to derive the equivalent input noise current spectral density contributed by R_I . According to Figure 4.6, the equivalent input noise current due to R_I is given by

$$i_{n,eq,R1} = \frac{v_{n,o}}{Z_T} \quad (4.36)$$

where $v_{n,o}$ is the output noise due to the thermal noise of R_I and Z_T is the transimpedance gain of the input stage that is expressed by (4.7).

Figure 4.6: Schematic used to derive the input referred noise current contributed by R_I

Based on Figure 4.6 and by regarding the noise sources as linear voltage/current signals, we obtain

$$v_{n,o} = Z_o (i_{n,R1} - i_1) \quad (4.37)$$

$$i_1 \approx i_2 \frac{g_{m1}}{\frac{1}{R_s} + g_{m1} + sC_{in}} = g_{m2} v_{n,o} \frac{g_{m1}}{\frac{1}{R_s} + g_{m1} + sC_{in}} \quad (4.38)$$

$$i_2 = g_{m2} v_{n,o} \quad (4.39)$$

where $i_{n,R1}$ is the thermal noise current of R_I , $Z_o \approx R_I // \frac{1}{sC_o}$ is the output

impedance with $C_o \approx C_L + C_{gd1} + C_{db1} + C_{gs2}$ and C_{in} is the lumped parasitic capacitance at the input node. Based on (4.36), (4.37), (4.38), (4.39) and by assuming that the resistance of R_s is relatively large, we obtain

$$i_{n,eq,R1} \approx A \cdot \frac{Z_o}{Z_T} \cdot i_{n,R1} \approx \left(1 + s \frac{C_{in}}{g_{m1}} \right) \cdot i_{n,R1} \quad (4.40)$$

$$A \approx \left(1 + s \frac{C_{in}}{g_{m1}}\right) / \left(1 + s \frac{C_{in}}{g_{m1}} + \frac{g_{m2}R_1}{1 + sR_1C_o}\right) \quad (4.41)$$

In the above analysis, we regard the noise sources as linear voltage/current signals. However, for noise calculation, each noise contribution must be expressed in mean square value. Therefore, the input referred noise current spectral density contributed by R_I is given by

$$N_{n,R1} \approx \overline{i_{n,R1}^2} \left| A \frac{Z_o}{Z_T} \right|^2 \approx \frac{4KT}{R_1} \left[1 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \right] \quad (4.42)$$

Figure 4.7 shows the small-signal circuit model for the purpose of noise analysis of the propose TIA input stage in Figure 4.1 (a) including the channel thermal noise, the induced gate noise and their cross-correlation.

Figure 4.7: Small-signal circuit model of the proposed TIA input stage for noise analysis

Based on Figure 4.7 and by applying small-signal analysis, we can first obtain the equivalent input noise current components contributed by each noise sources illustrated in Figure 4.6. Starting from the left side in Figure 4.7, the equivalent input noise current spectral density contributed by R_s is given by

$$N_{n,Rs} = \overline{i_{n,Rs}^2} = \frac{4KT}{R_s} \quad (4.43)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_I is given by

$$N_{n,g1} = \overline{i_{g1}^2} = 4KT\delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} \quad (4.44)$$

The equivalent input noise current spectral density contributed by the channel thermal noise of M_2 is given by

$$N_{n,d2} = \overline{i_{n,d2}^2} = 4KT\gamma g_{d0,2} \quad (4.45)$$

The equivalent input noise current spectral density contributed by the channel thermal noise of M_I is given by

$$N_{n,d1} \approx \overline{i_{n,d1}^2} \left(\left| A \frac{Z_o}{Z_T} \right|^2 - 1 \right) \approx 4KT\gamma g_{d0,1} \frac{\omega^2 C_{in}^2}{g_{m1}^2} \quad (4.46)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_2 is given by

$$\begin{aligned} N_{n,g2} &\approx \overline{i_{g2}^2} \left| A \frac{Z_o}{Z_T} \right|^2 \approx 4KT\delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \left| 1 - j\omega \frac{C_{in}}{g_{m1}} \right|^2 \\ &= 4KT\delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \left[1 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \right] \end{aligned} \quad (4.47)$$

The equivalent input noise current spectral density contributed by R_I is given by

$$N_{n,R1} \approx \overline{i_{n,R1}^2} \left| A \frac{Z_o}{Z_T} \right|^2 \approx \frac{4KT}{R_1} \left[1 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \right] \quad (4.48)$$

The channel thermal noise and the induced gate noise are cross-correlated and according to (4.44) and (4.46) and the analysis in Section 2.7, the correlated noise of i_{g1} and $i_{n,d1}$ is

$$\begin{aligned}
 N_{n,c1} &\approx \overline{i_{g1} i_{n,d1}^*} \left(1 + j\omega \frac{C_{in}}{g_{m1}} \right)^* + \overline{i_{g1}^* i_{n,d1}} \left(1 + j\omega \frac{C_{in}}{g_{m1}} \right) \\
 &= c \left(1 - j\omega \frac{C_{in}}{g_{m1}} \right) \sqrt{i_{g1}^2 i_{n,d1}^2} + c^* \left(1 + j\omega \frac{C_{in}}{g_{m1}} \right) \sqrt{i_{g1}^2 i_{n,d1}^2} = -2|c| \frac{\omega C_{in}}{g_{m1}} \sqrt{i_{g1}^2 i_{n,d1}^2}
 \end{aligned} \tag{4.49}$$

According to (4.45) and (4.47) and the analysis in Section 2.7, the correlated noise of i_{g2} and $i_{n,d2}$ is

$$\begin{aligned}
 N_{n,c2} &\approx \overline{i_{g2} \left(-1 - j\omega \frac{C_{in}}{g_{m1}} \right) i_{n,d2}^*} + \overline{i_{g2}^* \left(-1 - j\omega \frac{C_{in}}{g_{m1}} \right) i_{n,d2}} \\
 &= c \left(-1 - j\omega \frac{C_{in}}{g_{m1}} \right) \sqrt{i_{g2}^2 i_{n,d2}^2} + c^* \left(-1 + j\omega \frac{C_{in}}{g_{m1}} \right) \sqrt{i_{g2}^2 i_{n,d2}^2} = -2|c| \frac{\omega C_{in}}{g_{m1}} \sqrt{i_{g2}^2 i_{n,d2}^2}
 \end{aligned} \tag{4.50}$$

The total equivalent input noise current spectral density of the proposed TIA input stage can be obtained by summing up the noise components from (4.43) to (4.50), which is given by

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \begin{aligned} &\frac{1}{R_s} + \frac{1}{R_1} \left[1 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \right] \\ &+ \gamma g_{d0,1} \left[\frac{\omega^2 C_{in}^2}{g_{m1}^2} \left(1 - \frac{C_{gs1}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] + \delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} (1 - |c|^2) \\ &+ \gamma g_{d0,2} \left(1 - \frac{\omega C_{gs2} C_{in}}{g_{m1}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \\ &+ \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \left[1 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - |c|^2) \right] \end{aligned} \right\} \tag{4.51}$$

In Equations (4.43) to (4.51), K is the Boltzmann constant, T is the absolute temperature, γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, $C_1 \approx C_{sb1} + C_{gs1} + C_{db2}$, $C_2 \approx C_{gd1} + C_{db1} + C_{gs2}$, $C_{in} \approx C_{pd} + C_1$ is the total input parasitic capacitance, $C_o \approx C_L + C_2$, $Z_o \approx R_1 // \frac{1}{sC_o}$,

$$A \approx \left(1 + s \frac{C_{in}}{g_{m1}}\right) / \left(1 + s \frac{C_{in}}{g_{m1}} + \frac{g_{m2}R_1}{1 + sR_1C_o}\right), Z_T \text{ is given by (4.7) and } \alpha = \frac{g_m}{g_{d0}}. \text{ For long}$$

channel devices, $\gamma = 2/3$ and $\alpha = 1$. For short channel devices, γ can be much greater than 1 and $\alpha < 1$. Typically, δ is $4/3$ for long-channel devices and increases in short-channel devices. According to (4.51), the correlated noises of the induced gate noise and channel thermal noise of both M_1 and M_2 tend to reduce the total input referred noise [101] [109-114].

It is well-known that besides bandwidth extension, the input series inductor can also helps to reduce the equivalent input noise [115-116]. The small-signal circuit model for noise analysis including the input series inductor L_1 is shown in Figure 4.8, where C_{gd2} is absent for simplicity due to the small size of M_2 .

Figure 4.8: Small-signal circuit model of the proposed TIA input stage with series input inductor for noise analysis

The noise analysis procedure based on Figure 4.8 is similar to that based on Figure 4.6 and Figure 4.7. Starting from the left side in Figure 4.8, the equivalent input noise current spectral density attributed to the channel thermal noise of M_2 is given by

$$N_{n,d2} = \overline{i_{n,d2}^2} = 4KT\gamma g_{d0,2} \quad (4.52)$$

The equivalent input noise current spectral density due to R_s is given by

$$N_{n,Rs} \approx \frac{4KT}{R_s} (1 - \omega^2 L_1 C_i)^2 \quad (4.53)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_1 is given by

$$N_{n,g1} \approx 4KT\delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} (1 - \omega^2 L_1 C_i)^2 \quad (4.54)$$

The equivalent input noise current spectral density contributed by the channel thermal noise of M_1 can be derived using the same way that is used through Equations (4.36) to (4.42), which is given by

$$\begin{aligned} N_{n,d1} &\approx \overline{i_{n,d1}^2} \left(\left| B \frac{Z_o}{Z_T} \right|^2 - (1 - \omega^2 L_1 C_i)^2 \right) \\ &\approx 4KT\gamma g_{d0,1} \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \end{aligned} \quad (4.55)$$

where

$$B \approx \left(1 + s \frac{C_i}{g_{m1}} + s^2 L_1 C_i \right) / \left(1 + s \frac{C_i}{g_{m1}} + s^2 L_1 C_i + \frac{g_{m2} R_l}{1 + s R_l C_o} \right) \quad (4.56)$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_2 is given by

$$\begin{aligned} N_{n,g2} &\approx \overline{i_{g2}^2} \left| B \frac{Z_o}{Z_T} \right|^2 \\ &\approx 4KT\delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \left[(1 - \omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \right] \end{aligned} \quad (4.57)$$

The equivalent input noise current spectral density contributed by R_l is given by

$$\begin{aligned} N_{n,Rl} &\approx \overline{i_{n,Rs}^2} \left| B \frac{Z_o}{Z_T} \right|^2 \\ &\approx \frac{4KT}{R_l} \left[(1 - \omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \right] \end{aligned} \quad (4.58)$$

The channel thermal noise and the induced gate noise are cross-correlated and according to (4.54) and (4.55) and the analysis in Section 2.7, the correlated noise of i_{g1} and $i_{n,d1}$ is

$$N_{n,c1} \approx -2|c| \frac{\omega C_{in}}{g_{m1}} (1 - \omega^2 L_1 C_i) (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) \sqrt{i_{g1}^2 i_{n,d1}^2} \quad (4.59)$$

According to (4.52) and (4.57) and the analysis in Section 2.7, the correlated noise of i_{g2} and $i_{n,d2}$ is

$$N_{n,c2} \approx -2|c| \frac{\omega C_{in}}{g_{m1}} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) \sqrt{i_{g2}^2 i_{n,d2}^2} \quad (4.60)$$

The total equivalent input noise current spectral density of the proposed TIA input stage with inductive peaking can be obtained by summing up the noise components from (4.52) to (4.60), which is given by

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \begin{aligned} & (1 - \omega^2 L_1 C_i)^2 \frac{1}{R_s} + \frac{1}{R_1} \left[(1 - \omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \right] \\ & + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \mathcal{G}_{d0,1} \left[(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) - (1 - \omega^2 L_1 C_i) \frac{C_{gs1}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right]^2 \\ & + (1 - \omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs1}^2}{5g_{d0,1}} (1 - |c|^2) \\ & + (1 - \omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \\ & + \mathcal{G}_{d0,2} \left[1 - (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) \frac{\omega C_{gs2} C_{in}}{g_{m1}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right]^2 \\ & + (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - |c|^2) \end{aligned} \right\} \quad (4.61)$$

In Equations (4.52) to (4.61), K is the Boltzmann constant, T is the absolute temperature, γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, $C_i \approx C_{pd} + C_{db2}$, $C_1 \approx C_{sb1} + C_{gs1}$, $C_2 \approx C_{gd1} + C_{db1} + C_{gs2}$, $C_{in} \approx C_i + C_1$ is the

total input parasitic capacitance, $C_o \approx C_L + C_2$, $Z_o \approx R_1 // \frac{1}{sC_o}$,

$$B \approx \left(1 + s \frac{C_i}{g_{m1}} + s^2 L_1 C_i\right) / \left(1 + s \frac{C_i}{g_{m1}} + s^2 L_1 C_i + \frac{g_{m2} R_1}{1 + s R_1 C_o}\right), \quad Z_T \text{ is given by (4.18)}$$

and $\alpha = \frac{g_m}{g_{d0}}$. The equivalent input noise current spectral density expressed by

(4.61) can be divided into three parts. The part contributed by resistance thermal noise sources is given by

$$\overline{i_{n,eq,R}^2} \approx (1 - \omega^2 L_1 C_i)^2 \frac{1}{R_s} + \frac{1}{R_1} \left[(1 - \omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \right] \quad (4.62)$$

The part contributed by the input transistor M_1 is given by

$$\begin{aligned} \overline{i_{n,eq,M1}^2} &\approx \frac{\omega^2 C_{in}^2}{g_{m1}^2} \gamma g_{d0,1} \left[(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) - (1 - \omega^2 L_1 C_i) \frac{C_{gs1}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right]^2 \\ &+ (1 - \omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs1}^2}{5 g_{d0,1}} (1 - |c|^2) \end{aligned} \quad (4.63)$$

The part contributed by the active feedback transistor M_2 is given by

$$\begin{aligned} \overline{i_{n,eq,M2}^2} &\approx (1 - \omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs2}^2}{5 g_{d0,2}} \\ &+ \gamma g_{d0,2} \left[1 - (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}) \frac{\omega C_{gs2} C_{in}}{g_{m1}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right]^2 \\ &+ (1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i})^2 \delta \frac{\omega^2 C_{gs2}^2}{5 g_{d0,2}} \frac{\omega^2 C_{in}^2}{g_{m1}^2} (1 - |c|^2) \end{aligned} \quad (4.64)$$

Figure 4.9: MATLAB calculated equivalent input noise current spectra density of the propose TIA input stage in Figure 4.1 (a) with/without the induced gated noise

Figure 4.9 shows the MATLAB calculated input referred noise current spectral density of the proposed TIA input stage without the series inductive peaking based on (4.51), where we use $\gamma = 1.2$, $\alpha = 1$ and $\delta = 4/3$. For curve “a”, the induced gate noise and the correlated noise are absent. For curve “b”, we use $c = -0.7j$ in the calculation. As shown in Figure 4.9, the correlated noise helps to reduce the total input referred noise but the noise reduction effect is not significant in this case. According to (4.51), the size of M_I needs to be very large to achieve a significant noise reduction, which will also reduce the bandwidth by a considerable amount. Due to technology limitation, we cannot achieve the best noise performance without degrading other performances such as the bandwidth for this design. Therefore, neglecting the effect of the induced gate noise in a broadband TIA usually does not cause too much noise prediction error.

Figure 4.10: MATLAB calculated equivalent input noise current spectra density of the propose TIA input stage with/without series input inductor

Figure 4.10 shows the MATLAB calculated input referred noise current spectral density of the proposed TIA input stage with and without the series inductive peaking based on (4.61), where we assume $\gamma = 1.2$, $\alpha = 1$, $\delta = 4/3$ and $c = -0.7j$. In Figure 4.10, curve “c” is with the series input inductor $L_I = 1.4\text{nH}$ and curve “b” is without the series input inductor, which is the same one as the curve “b” in Figure 4.9. If we choose $L_I = 0$, (4.61) becomes same as (4.51). According to Figure 4.10, the series input inductor can help to reduce the input referred noise significantly.

According to the discussion in Section 4.2, the gain of our proposed common gate TIA input stage with common source active feedback is not high enough to suppress the noise of the second stage to a negligible level. Therefore, it is more accurate to include the noise contribution by the second stage in our noise estimation for the whole TIA circuit. Nevertheless, the effect of the noise due to the second stage is not as important as the input stage. We therefore neglect the

induced gate noise of the second stage for mathematical simplicity. Based on the schematic shown in Figure 4.3, the input referred noise current spectral density contributed by the capacitive degeneration second stage is approximately given by

$$N_{n,M3} \approx \left| \frac{1}{Z_T} \right|^2 \frac{4KT}{1 + \omega^2 R_{s3}^2 C_{s3}^2} \left[\left(g_{d0,3} + \frac{1}{R_3} \right) \left(\frac{1 + g_{m3} R_{s3}}{g_{m3}} \right)^2 + R_{s3} \right] \quad (4.65)$$

where Z_T is given by (4.18). As we can see from the denominator of (4.65), the capacitive degeneration topology has a counter-effect to noise increment as frequency increases.

Figure 4.11 shows the MATLAB calculated input referred noise current spectral density based on the sum of (4.61) and (4.65), which includes the noise contribution of the input stage and the second stage of our new TIA circuit illustrated in Figure 4.3 (a). This result is also used in Figure 4.16 to estimate the noise performance of the whole TIA circuit.

Figure 4.11: MATLAB calculated equivalent input noise current spectra density of the propose TIA input stage and second stage

4.5 Simulation and measurement results

As for the frequency response of the proposed TIA design of Figure 4.3, besides the mathematical analysis in Section 4.3, it is also double-checked using the circuit simulator. The frequency response simulation is carried out using the Cadence SpectreRF with CHRT 0.18 μm RFCMOS process including all parasitics (post-layout simulation). The devices (MOSFETs, resistors, inductors and capacitors) used in our calculation in Section 4.3 are ideal. However, they are non-ideal in reality. Therefore, some small adjustments on the device sizes with the help of the circuit simulator are necessary to meet the design objectives. The finalized device sizes are illustrated in Figure 4.3. The transimpedance response simulation result is shown in Figure 4.12. The simulated transimpedance gain is about 54.5dB Ω . In Figure 4.12, curve “a” is the simulated transimpedance frequency response without input inductive matching and capacitive degeneration, which has a -3dB bandwidth of about 2.2GHz. Curve “b” of Figure 4.12 is the simulated result with capacitive degeneration but without inductive matching, which has a -3dB bandwidth of about 4.6GHz. After the bandwidth extension by capacitive degeneration and input inductive peaking, the simulated -3dB bandwidth is about 8GHz, which is shown by curve “c” in Figure 4.12.

When comparing the simulated results in Figure 4.12 with the calculated results in Figure 4.5, we can see that the simulation results agree with the mathematical calculation very well, which confirms our circuit analysis and design procedure discussed in Section 4.3. Figure 4.13 shows the post-layout simulated output eye-diagram with $2^{31}-1$ PRBS (Pseudo-Random-Binary-Sequence) and with 0.1mA (Figure 4.13(a)) and 0.5mA (Figure 4.13(b)) input current respectively.

Figure 4.12: Post-layout simulated transimpedance frequency response of the proposed TIA

Figure 4.13: Post-layout simulated output eye-diagram of the proposed TIA: (a) 0.1mA input current and (b) 0.5mA input current

To test the feasibility of the proposed common gate transimpedance amplifier input stage with active feedback and to verify the proposed TIA design in Figure 4.3, the proposed transimpedance amplifier design is implemented using CHRT 0.18 μm 2-poly 6-metal RFCMOS process. L_I is implemented using on-chip spiral inductors for the purpose of monolithic implementation and improving area efficiency. The on-chip spiral inductor is constructed based on the lithography, which is discussed in Chapter 3. Figure 4.14 shows the chip microphotograph of the proposed circuit design. An on-chip MIM capacitor C_{pd} of 0.2pF is used to mimic the effect of the photodiode parasitic capacitance, and together with the parasitic capacitance of the input pad that is around 0.1pF, the total input parasitic capacitance is about 0.3pF.

Figure 4.14: The chip microphotograph of the proposed TIA design

The chip is measured on wafer with Cascade Microtech Coplanar Ground-Signal-Ground (GSG) probes. The frequency response is measured using HP8510C network analyzer. Figure 4.15 shows the measured transimpedance frequency response. For a typical 10Gb/s TIA, the bandwidth is usually around 0.6B to 0.7B for NRZ data if the receiver bandwidth is set by the TIA, where B

stands for the bit rate [55]. As shown in Figure 4.15, the transimpedance frequency response is tested from 500MHz to 10GHz and the data is captured using Agilent IC-CAP. The measured low-frequency transimpedance gain is around 54.6dB Ω and the -3dB bandwidth is about 7GHz (0.7B). When compared to the calculated and simulated results in Figure 4.5 and Figure 4.12, the measured gain matches the predicted gain very well at low frequencies. However, the measured gain drops faster as frequency increases. The measured -3dB bandwidth is somewhat lower than the predicted. This is most possibly due to the non-ideality of the inductors. The EM radiation loss, the silicon substrate loss and process variations may also contribute to such bandwidth degradation.

Figure 4.15: Measured transimpedance frequency response of the proposed TIA

Figure 4.16 shows the measured input referred noise current spectral density from 800MHz to 10GHz. The noise measurement is carried out using 8970B Noise Figure Meter, 8971C Noise Figure Test Set and NP5B Noise Parameter Test System. The calculated equivalent input noise current spectral density based on Figure 4.11 is also illustrated in the Figure 4.16 for comparison. The measured

input referred noise current spectral density is about $17.5 \text{ pA}/\sqrt{\text{Hz}}$ in average up to 7GHz. The calculated input referred noise current spectral density is about $15.8 \text{ pA}/\sqrt{\text{Hz}}$ in average up to 7GHz. According to the measured and the predicted noise illustrated in Figure 4.16, the predicted noise is much closer to the measured noise at low frequencies than at high frequencies. The difference between the measured and the predicted noise is most probably due to additional parasitic elements and substrate noise/losses that are not considered in the mathematical prediction. Nevertheless, the calculated input referred noise current spectral density is quite close to the measured one, which confirms the validity of our mathematical analysis in Section 4.4. The predicted average noise is about 10% less than the measured average noise, which is sufficient for noise evaluation [109]. The measured total input referred RMS noise current is about $1.8\mu\text{A}$ integrated up to 10GHz.

Figure: 4.16: Measured and predicted equivalent input noise current spectral density of the proposed TIA

According to our discussion in Section 2.3, the optimum bandwidth alone does not guarantee the performance of the TIA. Even if the frequency response $|Z_T(f)|$ is flat up to sufficient high frequency, distortions in the form of data dependent jitter may occur if the phase linearity of $Z_T(f)$ is not sufficient. The group delay is used to measure the phase linearity. Typically, a group delay variation of less than $\pm 10\%$ of the bit rate over the specified bandwidth is required to limit the generation of data dependent jitter [55]. The group delay is calculated from the measured phase response. The measured group delay frequency response of the proposed TIA is shown in Figure 4.17. According to Figure 4.17, the group delay is about 65 ± 10 ps, which is within the requirement of $\pm 10\%$ of the bit rate over the specified bandwidth for 10Gb/s applications.

Figure 4.17: Measured group delay response of the proposed TIA

Figure 4.18: Measured output transient response of the proposed TIA with -25dBm signal generator power

The output transient response of the proposed TIA is also tested on wafer. The test setup is the same as that in Chapter 3. The magnitude of the TIA output impedance at 5GHz is about 150Ω according to the network analyzer measurement result. Therefore, the measured output transient voltage amplitude is about 25% of the actual one.

Figure 4.18 is the output transient response with -25dBm signal generator power. If we assume a 50Ω input matching and consider there is about 2dB loss through the RF cables. The actual available power to the TIA is about $-25 - 2 - 3 = -30\text{dBm}$, which means the corresponding peak amplitude of the sine-wave input current is about 0.2mA. The measured output voltage peak amplitude is about 23.2mV (peak-to-peak 46.43mV). This translates to an actual output transient voltage peak amplitude of $23.2 \times 4 = 92.8\text{mV}$, which means the transimpedance gain at 5GHz is about 460Ω (53dB Ω). The above calculation is just a rough estimation since it is very difficult to precisely characterize the losses

in the measurement. The transimpedance gain obtained from the transient measurement result is very close to that obtained by the network analyzer measurement shown in Figure 4.15.

4.6 Summary

In this chapter, a current-mode TIA topology based on common gate input stage with common source active feedback is presented, which provides as low input impedance as the RGC configuration. Thus, the influence on the TIA bandwidth by the large input capacitance including the photodetector capacitance can be greatly reduced. The characteristics of this proposed TIA input stage is analyzed and its pros and cons are discussed.

Based on this TIA input topology, a prototype TIA design is proposed, which also employs series inductive peaking to extend the bandwidth. Furthermore, a two-stage capacitive degeneration is used to boost the bandwidth as well as the gain. The design procedure of the proposed transimpedance amplifier is addressed in detail in this chapter by mathematical calculation. The proposed TIA is designed to exhibit a transimpedance frequency response between the Butterworth response and the Bessel response.

In this chapter, the effect of the induced gate noise in a broadband transimpedance amplifier is also discussed with a detailed noise analysis based on the van der Ziel noise model. The noise reduction effects due to the series input inductor and the correlated noise of the channel thermal noise and the induced gate noise are discussed via mathematical calculation. Due to technology limitation, the noise reduction effect by the correlated noise is not significant if the gain-bandwidth product requirement is of first priority. The noise analysis only

considering the channel thermal noise is usually sufficient for noise estimation of a broadband TIA. The proposed TIA design has been realized using CHRT 0.18 μm RFCMOS technology. The measurement data confirms our circuit design procedure and noise analysis method.

The measurement data shows a transimpedance gain of about 54.6dB Ω (540 Ω) and a -3dB bandwidth of about 7GHz for a total input parasitic capacitance of 0.3pF. The noise measurement shows an average input referred noise current spectral density of about 17.5 pA/ $\sqrt{\text{Hz}}$ up to 7GHz. The measured total input referred RMS noise current is about 1.8 μA integrated up to 10GHz. The measured group delay response is within $\pm 10\text{ps}$ over the bandwidth of interest. The chip consumes 18.6mW DC power from a single 1.8V supply. The whole chip size is 0.55 $\times$ 0.6mm² including pads while the core circuit occupies only 0.4 $\times$ 0.25mm². According to the TIA specifications discussed in Section 2.4, the proposed TIA circuit is suitable for very-short-reach 10Gb/s Ethernet applications and possesses the merits of CMOS technology such as high integration, low cost, high manufacturability and very low power consumption.

Chapter 5

Transimpedance Amplifier with Automatic Gain Control

As introduced in Section 2.5.2, the concept of *adaptive transimpedance* or *Automatic Gain Control* (AGC) is raised as a counter-measurement to the optical overload. The idea is to ensure the TIA gain is adaptive in accordance to the input signal level. The signal amplitude is monitored at some stage and compared with a reference. The transimpedance gain is adjusted continuously in such a way that the output level remains relatively constant or increase very slowly when input current increases to high levels. However, at weak input signal levels, it is necessary to disable the adaptive transimpedance mechanism to ensure the sensitivity performance.

In this chapter, a broadband transimpedance amplifier (TIA) with automatic gain control (AGC) is designed with CHRT 0.18 μ m 1.8V RFCMOS technology for the application in 10Gb/s fiber-optical data links. The core TIA circuit is based on the same design presented in Chapter 3. Post-layout simulation of the proposed design shows a -3dB bandwidth of about 9GHz with an adaptive transimpedance gain of about 53dB Ω in the weak-input case and about 43dB Ω under input overload condition. The design is also silicon verified and the transient response measurement shows validity of the automatic gain control mechanism.

5.1 Introduction

Besides low-noise and broadband requirements, in short-haul optical systems

where expensive erbium doped fiber amplifier is not present or in systems with burst-mode operation, transimpedance amplifiers are also required to work under input overload condition [30], [55]. To meet such a requirement, TIA with build-in AGC to adjust the conversion gain needs to be employed, reducing the input overload induced distortion and timing jitter [55] [65]. This chapter presents a 10Gb/s CMOS transimpedance amplifier with automatic gain control, which is suitable for monolithic integration and low cost, low power applications. The core TIA design is based on the same TIA circuit presented in Chapter 3.

5.2 Circuit design and analysis

The circuit diagram of the proposed TIA with AGC is shown in Figure 5.1. The circuit is composed of five parts, namely the input matching network, the regulated cascode input stage, the capacitive degeneration stage, the source follower output stage and the parallel shunt feedback automatic gain control loop. The core-TIA circuit is based on the same TIA design proposed in Chapter 3, which is illustrated in Figure 3.7 (a). M_1 and M_2 is part of the regulated cascode input stage, which presents very small input impedance [63] [72]. The lumped capacitive load at the input stage (including the photodiode capacitance) was split by L_1 and L_2 and absorbed into the LC input matching network. Therefore, in this design, the input stage is isolated from the bandwidth determination. In conventional TIAs, the bandwidth is usually restricted by the large input capacitance. However, in this design the dominant pole is located at node “A” within the core TIA circuit. The capacitive degeneration [28] stage $M_3/C_b/R_b$ generates a zero at $(R_b C_b)^{-1}$, which is designed to compensate the dominant pole at node “A” and extend the bandwidth of the core TIA circuit to the second lowest pole. Besides this zero, the capacitive

degeneration also creates an additional pole at $(I + g_{m3}R_b)/R_bC_b$ at a higher frequency, which is the second lowest pole of the core TIA circuit. This second lowest pole now determines the -3dB bandwidth of the core TIA without the input matching network. The input matching network and the capacitive degeneration together are used to enhance the bandwidth of the TIA circuit. The detailed analysis of the core-TIA circuit can be found in Section 3.1.

Figure 5.1: The proposed TIA with Automatic Gain Control (AGC) function

In addition to the core TIA circuit introduced in Section 3.1, the feedback pMOS transistor acts as an adaptive feedback resistor. The output voltage is not taken directly at the source of M_4 , an extra output stage consists of M_5/R_5 is used to improve the stability [28].

The automatic gain control mechanism is explained as follows: Basically, the transimpedance amplifier sees on-off (1/0) current signals from the photodetector, which means the electrical signals in the TIA circuit swings only in one direction.

In this design, the voltage signal at node “A” swings in the positive direction and the voltage signal at node “B” swings in the negative direction. Therefore, under high input current condition, transistor M_3 may be driven into deep triode region, which results in output waveform distortion and overload induced data jitter. The dynamic range is therefore decreased. To improve the dynamic range, an automatic gain control circuit is employed in parallel with the TIA by means of shunt feedback. The pMOS transistor P_1 is connected in a shunt feedback manner, acting as an adaptive feedback resistor. The first stage of the AGC block $M_6/R_6/C_{agc}$ is a peak detector. The automatic gain control circuit is shown on top of the TIA in Figure 5.1. The signal strength at node “B” is sensed by the peak detector and stored on capacitor C_{agc} . The second stage M_7/R_7 is a level shifter. The output buffer P_2/M_8 amplifies the detected signal strength and generates the gain control signal, which is applied to the gate of P_1 and controls its channel resistance. In the weak input current state, P_2 of the AGC output buffer is on and M_8 is off, the feedback transistor P_1 is therefore completely cut off. As the input current increases, the voltage swing at node “B” that goes in the negative direction also increases. The peak detector circuit senses this negative swing and charges up C_{agc} . Once M_8 is turned on after its threshold voltage is exceeded, the gain control voltage V_{agc} is gradually pulled down as the TIA input power increases. The feedback transistor P_1 starts to turn on gradually by V_{agc} and its channel resistance is reduced gradually, resulting in a continuously decreasing transimpedance gain.

5.3 Post-layout simulation

The circuit is implemented using CHRT 0.18 μ m 1.8V RFCMOS technology. The circuit layout is shown in Figure 5.1. Same as that in Chapter 3, C_{pd} is a

0.25pF on-chip MIM capacitor, which is used to mimic the effect of the photodiode parasitic capacitance.

Figure 5.2: Layout of the proposed TIA with AGC in Figure 5.1

The post-layout simulation with extracted parasitic R/C components is carried out using Cadence SpectreRF. The simulated transimpedance gain with AGC circuit in the off-state is shown by the dotted line in Figure 5.2, which is about 53dB Ω with a -3dB bandwidth of about 9GHz. As mentioned previously, the core TIA circuit in the proposed TIA with AGC design is the same as the TIA design presented in Chapter 3. Therefore, the measured transimpedance response of the core TIA part (without AGC) in Chapter 3 is also shown in Figure 5.2 by the solid line for comparison. The measurement data shows that the gain of the core TIA part is about 53dB Ω with a -3dB bandwidth of 8GHz. As discussed in Chapter 3, the difference between the simulated and measured data is probably due to the process variation, the non-ideality of the inductors, the EM radiation loss and the silicon substrate loss especially at high frequencies.

Figure 5.3: Simulated transimpedance response of the proposed TIA with AGC in the off-state vs. measured transimpedance response of the core TIA in Chapter 3

Figure 5.4 shows the post-layout simulated output transient response with 10Gb/s random input current signal of 2mA strength (on/off square wave input). According to Figure 5.4, the output amplitude is quite large at the first instance. However, the active gain control mechanism is turned on instantly and the output amplitude decreases and stabilizes very fast within 1.5ns.

Figure 5.4: Post-layout simulated output transient response with random input data with 2mA current signal strength

Figure 5.5: Post-layout simulated output peak-to-peak voltage swing and transimpedance gain versus input current signal strength (with on/off square wave input)

Figure 5.5 shows the post-layout simulated output voltage peak-to-peak swing amplitude and the associated transimpedance gain versus the input current signal level (on/off square wave input). The input current is a 5GHz square wave that is equivalent to 10Gb/s “010101...010101...” digital data. According to the simulated result, when the input signal strength is lower than 0.4mA, the output voltage swing increases linearly as the input current increases and the associated transimpedance gain remains relatively stable at about 53dBΩ. However, when the input current increases further, the automatic gain control circuit is activated and the transimpedance gain begins to drop. As discussed previously, the automatic gain control mechanism is used to alleviate overload induced data jitter and reduce the output waveform distortion. The dynamic range is therefore improved.

Figure 5.6: Post-layout simulated output eye-diagram with 2mA input current and 10Gb/s $2^{31}-1$ PRBS: (a) without AGC and (b) with AGC

Figure 5.6 shows the post-layout simulated output eye-diagram with/without automatic gain control mechanism, both with 2mA input current and 10Gb/s $2^{31}-1$ pseudo random binary sequence (PRBS). Figure 5.6 (a) is the simulated output eye-diagram without automatic gain control and Figure 5.6 (b) is the simulated output eye-diagram with automatic gain control. Although without automatic gain control the output signal swing is much higher, the distortion is also significant. According to Figure 5.6 (b), the output eye-diagram can be greatly improved with the automatic gain control mechanism.

5.4 Measurement results

The proposed TIA with automatic gain control is implemented using CHRT 0.18 μm 2-poly 6-metal RFCMOS process. L_1 and L_2 are implemented using on-chip spiral inductors for the purpose of monolithic implementation and improving area efficiency. The on-chip spiral inductor is constructed based on the lithography, which is introduced in Chapter 3. Figure 5.7 shows the chip microphotograph of the proposed circuit design. The core TIA design is the same as the transimpedance amplifier design presented in Chapter 3.

Figure 5.7: Chip microphotograph of the proposed TIA with AGC

The measured DC power dissipation of the proposed TIA with AGC is about 27mW from a single 1.8V power supply. The output transient response of the proposed TIA is tested on wafer. The test setup is the same as that in Chapter 3. The probe adapter we use for the oscilloscope is a low-impedance (50 Ω) one to detect the 5GHz high frequency signal. The magnitude of the TIA output impedance at 5GHz is about 100 Ω according to the network analyzer measurement

result. Therefore, the measured output transient voltage amplitude is about 1/3 of the actual one.

Figure 5.7(a) is the output transient response with -25dBm signal generator power. If we assume a 50Ω input matching and consider there is about 2dB loss through the RF cables. The actual available power to the TIA is about $-25 - 2 - 3 = -30\text{dBm}$, which means the corresponding peak amplitude of the sine-wave input current is about 0.2mA. The measured output voltage peak amplitude is about 22.7mV (peak-to-peak 45.52mV). This translates to an actual output transient voltage peak amplitude of $22.7 \times 3 = 68.1\text{mV}$, which means the transimpedance gain at 5GHz is about 341Ω (50.6dB Ω). Figure 5.7(b) is the output transient response with -15dBm signal generator power. The corresponding peak amplitude of the sine-wave input current is about 0.6mA, which means the transimpedance gain at 5GHz is about 281Ω (48.9dB Ω). Figure 5.7(c) is the output transient response with -5dBm signal generator power. The corresponding peak amplitude of the sine-wave input current is about 2mA, which means the transimpedance gain at 5GHz is about 138Ω (43.7dB Ω).

The transimpedance gain decreases as the input power increases. The automatic gain control mechanism is clearly effective. However, due to the difficulty in precisely characterizing the losses during the measurement, the above calculation is just a rough estimation to testify the AGC mechanism.

(a)

(b)

(c)

Figure 5.8: Measured output transient response of the proposed AGC-TIA with (a) -25dBm, (b) -15dBm and (c) -5dBm signal generator power

5.5 Summary

In this chapter, a 10Gb/s wideband transimpedance amplifier with built-in automatic gain control (AGC) is designed and analyzed. The core TIA circuit is based on the same TIA design discussed in Chapter 3. The automatic gain control circuit is employed in parallel with the TIA by means of a peak-detector and an adaptive shunt feedback to reduce the input overload induced distortion and timing jitter. To verify the proposed automatic gain control mechanism, the proposed TIA with AGC circuit is implemented using CHRT 0.18 μ m 2-poly 6-metal RFCMOS process.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, the challenges and difficulties for high-speed transimpedance amplifier design with CMOS technology have been studied. Various broadband design techniques for high performance TIA design have been analyzed and explored to implement novel low-noise, low-power 10Gb/s TIAs suitable for very-short-reach (VSR) applications using cost effective CMOS technology.

The noise characteristics of broadband CMOS transimpedance amplifiers have also been studied in detail based on the van der Ziel MOSFET noise model, which includes the channel thermal noise, the induced gate noise and their cross-correlation. The effect of the induced gate noise in a high-speed TIA has been analyzed mathematically.

Based on the various broadband design techniques explored and proposed, two novel CMOS TIA prototypes have been designed and implemented using CHRT 0.18 μ m 2-poly 6-metal RFCMOS process. The measurement results confirm the feasibility of designing high performance TIA circuits with CMOS technology. The proposed CMOS TIA designs are able to achieve comparable performances to those SiGe and III-V counterparts in most aspects yet maintaining the merits of CMOS technology such as low power, low cost, high integration level and high manufacturability. Moreover, an automatic gain control (AGC) circuit that helps to reduce the overload induced distortion and jitter has also been proposed and silicon verified.

On-wafer measurements of the above circuits are carried out using HP8510C Network Analyzer, 4142B Modular DC Source/Monitor, 8970B Noise Figure Meter, 8971C Noise Figure Test Set, NP5B Noise Parameter Test System, 8517B S-Parameter Test Set, HP83731B 1-20GHz Synthesized Signal Generator, and Cascade Microtech Coplanar Ground-Signal Ground (GSG) probes. The measurement data is captured using Agilent IC-CAP. The transient response is captured by the LeCroy Wavemaster 6 GHz oscilloscope.

Table 6.1 summarizes the performances of the proposed TIA design 1 introduced in Chapter 3 and design 2 in Chapter 4. A detailed comparison to other high-speed TIAs implemented in various technologies is also presented in Table 6.1. The figure-of-merit of wide-band amplifiers in terms of gain-bandwidth-product (GBP) per DC power (P_{dc}) is also shown in this table.

Table 6.1: Performance comparison of high-speed TIAs

Ref.	Techno.	BW (GHz)	Gain (dB Ω)	Power (mW)	Input Noise (pA/sqrtHz)	Chip Area (mm ²)	Group Delay (ps)	GBP/ P_{dc} (GHz Ω /mW)
[30]	0.1 μ m pHEMT	8@ 0.25pF	63.3	500 @5V	6.5	1.6 $\times$ 1.3	$\pm$ 40	23.4
[34]	0.25 μ m BiCMOS	9@ 0.1pF	55	140 @5V	14	NA	$\pm$ 10	36.2
[125]	0.2 μ m HEMT	8.3@ NA	57	NA	8.8	NA	NA	NA
[126]	2 μ m DHBT	12@ NA	55	12.2@ 3.4V	NA	0.41 $\times$ 0.47	NA	553.1
[66]	80nm CMOS	13.4@ 0.1pF	52	2.2@ 1V	28	0.01	$\pm$ 20	2425
[123]	0.18 μ m CMOS	15@ NA	58	200@ 1.8V	12	NA	NA	60
[124]	0.18 μ m CMOS	30.5@ 0.05pF	51	60.1@ 1.8V	34.3	0.17 $\times$ 0.46	NA	180.1
[70]	0.18 μ m CMOS	9.2@ 0.5pF	54	130@ 2.5V	17	0.8 $\times$ 0.8	$\pm$ 25	33.5
Proposed Design 1	0.18 μ m CMOS	8@ 0.25pF	53	13.5@ 1.8V	18	0.45 $\times$ 0.25	$\pm$ 20	266.7
Proposed Design 2	0.18 μ m CMOS	7@ 0.2pF	55	18.6@ 1.8V	17.5	0.4 $\times$ 0.25	$\pm$ 10	206.9

From Table 6.1, the proposed TIA design 1 and design 2 achieve comparable performance to those 10Gbit/s TIAs implemented in III/V technologies such as

[30], [125] and [126] in most aspects. The proposed design 2 presents similar performance to the proposed design 1. The gain-bandwidth-product of the proposed design 2 is less than the proposed design 1 mostly because the proposed design 1 employs a 5th-order input matching and that of the proposed design 2 is a 3rd-order one. However, the proposed design 2 shows improved phase-linearity since its frequency response is designed to be closer to the Bessel response. Comparing to other 0.18 μ m CMOS TIAs such as [123], [124] and [70], the figure-of-merits in terms of GBP/P_{dc} of the proposed TIAs in this thesis are among the highest ones.

According to the comparison table in Table 6.1, CMOS technology enjoys significant advantage in terms of GBP/P_{dc} figure-of-merit due to its low power characteristic. This advantage increases tremendously with the down-scaling trend. For example, the current-mode common-gate feed-forward transimpedance amplifier in [66] implemented in 80nm CMOS shows the highest GBP/P_{dc} in favor of the very low power and excellent cut-off frequency characteristics of sub-100nm CMOS technology. Today's state-of-the-art 65nm CMOS technology shows an nMOSFET cut-off frequency of about 210GHz with microwave low-noise and high-gain properties [127]. With the down-scaling trend, the improving performance in terms of cut-off frequency, high-frequency noise of sub-100nm CMOS technology makes it an excellent candidate for 40Gbit/s beyond low-noise ultra-low-power TIAs. Meanwhile, the current-mode broadband design techniques introduced in this thesis such as the regulated cascode topology, common-gate feed-forward and common-gate input-stage with active-feedback can be easily employed in sub-100nm CMOS TIA designs such as in reference [66]. TIA designs fabricated the 65nm CMOS technology enjoy the advantages of very-high-

speed, ultra-low-power and improved high-frequency-noise. However, several design challenges also exist. First, the voltage headroom and the input overload current are reduced. Second, the maximum cut-off frequency is usually measured when device is biased under maximum supply voltage, which is not practical in analog design. Third, the increased leakage current of sub-100nm MOSFET leads to reduced gain [66]. All these problems need to be taken care of when transistors are cascaded in current-mode TIA designs.

6.2 Future work

The way people exchange simple information and transmit short message using light can be traced back to ancient times when beacon and torch signals were widely used for simple instant communications. Ever since then, the effort toward faster, more accurate and more powerful communications is continuous and incessant especially after modern optical communications came into reality in last century. Although today's mainstream optical communication systems operating at 10Gbit/s have been mature and widely spread and optical communication systems of much higher speed such as 40GHz are gradually becoming commercially available, the demand for higher speed and lower cost will never be satisfied.

The transimpedance amplifier, acting as the front-end of an optical receiver system, set limitations and render difficulties to the whole system design. Being one of the bottlenecks of the optical communication system, the future challenges and directions of TIA design will be higher speed, lower noise, higher integration and lower cost. For higher integration and lower cost purpose, CMOS technology is without any saying the best candidate. However, SiGe or III-V technologies are definitely superior over CMOS when speed and noise are concerned.

In this thesis, broadband design techniques that can be used to boost the bandwidth of amplifiers have been studied in detail while the study on noise reduction techniques for a high-speed front-end amplifier has been mainly focused on inductive tuning. In relatively lower speed TIA designs, noise reduction techniques such as noise-free optical feedback, noise-free capacitive feedback as well as integration and dump have been studied and effectively employed [55]. However, in higher speed TIA designs, the study on noise optimization is far behind the study on speed improvement and therefore needs more attention. Nevertheless, current circuit design techniques can only compensate part but not all of the disadvantages of CMOS technology in terms of speed and noise performances. Therefore, the future TIA and optical communication system design improvement is preferably to be focused on novel circuit design techniques that will be ubiquitously helpful in any technology as well as novel/improved CMOS compatible technologies that possess the merits of both CMOS and compound semiconductor technologies.

The Author's Publications:

Z. Lu, K. S. Yeo, J. G. Ma, M. A. Do, W. M. Lim and X. Chen, "Broad-Band design techniques for transimpedance amplifiers," *IEEE Transactions on Circuits and Systems —I: Regular papers*, Vol. 54, No. 3, March 2007, pp. 590 – 600.

Z. Lu, K.S. Yeo, J. Ma and M.A. Do, "Low power CMOS transimpedance amplifier for 10Gbit/s optical receivers," *Proceeding of 10th International Symposium on Integrated Circuits, Devices & Systems (ISIC'04)*, Singapore, Sep. 2004.

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X. Shi, **Z. Lu**, J. Ma, E. Li, K.S. Yeo, M. A. Do, "Investigation of interconnect effects in a transimpedance amplifier," *Proceeding of 17th International Zurich Symposium on Electromagnetic Compatibility, 2006 (EMC-Zurich 2006)*, pp. 586-589, Feb. 2006.

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