Class D Amplifiers (CDAs) : PWM-in-PWM-out CDA, Filterless Bang-Bang CDA, and high-frequency high-efficiency CDA for Envelope Tracking

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**Class D Amplifiers (CDAs):
PWM-In PWM-Out CDA,
Filterless Bang-Bang CDA, and
High-Frequency High-Efficiency CDA
for Envelope Tracking**

KANG YANG

School of Electrical & Electronic Engineering

**A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy**

2018

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

22 Aug 2019

Date

KANG Yang

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

2/9/19

Date

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Authorship Attribution Statement

This thesis contains material from 3 paper published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 3 is largely extracted from the author's publication [99], L. Guo, T. Ge, Y. Kang, H. He and J. S. Chang "Analysis and design of PWM-in-PWM-out Class D Amplifiers" published in the proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), 2014.

The contributions of the co-authors are as follows:

- (i) Dr. Ge provided the initial project direction and revised the manuscript;
- (ii) Dr. Guo prepared the manuscript drafts, proposed the prototype CDA structure, verified the design and mathematical formulas;
- (iii) I co-designed the proposed PIPO CDA, performed the simulation and co-derived the mathematical expressions of THD and PSRR. I also assisted to analyze data and revise the manuscript.
- (iv) Dr. He assisted the design, derivation and verification;
- (v) Prof. Chang suggested the research area and edited the manuscript drafts.

Chapter 4 is largely extracted from the author's publication [102], H. He, Y. Kang, J. Yu, L. Guo, T. Ge and J. Chang "A novel low-power high-efficiency 3-state filterless Bang-Bang class D amplifier" published in the proceedings of the IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2015.

The contributions of the co-authors are as follows:

- (i) Dr. He prepared the manuscript draft, co-design the proposed filterless Bang-Bang CDA, performed simulations, and co-verified the mathematical expressions;
- (ii) I co-designed the proposed filterless Bang-Bang CDA, co-verified the mathematical expressions, evaluated the simulation, and revised the manuscript;
- (iii) Mr. Yu assisted with the simulation and mathematical verifications;
- (iv) Dr. Guo proposed the initial project direction and preliminary structures;
- (v) Dr. Ge evaluated the design and derivations, and revised the manuscript draft;
- (vi) Prof. Chang suggested the research area and edited the manuscript drafts.

Chapter 5 is largely extracted from the author's publication [105], H. He, Y. Kang, T. Ge, L. Guo, and J. S. Chang, "A 2.5W 40MHz-Bandwidth Hybrid Supply Modulator with 91% Peak Efficiency, 3V Output Swing and 4mV Output Ripple at 3.6V Supply" published in the IEEE Transactions on Power Electronics. The contributions of the co-authors are as follows:

- (i) Dr. He prepared the manuscript draft, designed the Class AB part of the proposed supply modulator, co-derived the mathematical expressions, co-performed the measurement;
- (ii) I analyzed and designed of the Class D part of the proposed supply modulator, performed pre-/post-layout system simulation verifications,

co-derived the mathematical derivations, co-performed the measurement;
and revised the manuscript draft;

- (iii) Dr. Ge assisted with the measurement and revised the mathematical derivations;
- (iv) Dr. Guo assisted with the simulation verifications;
- (v) Prof. Chang suggested the research area and edited the manuscript drafts

22 Aug 2019

Date

KANG YANG

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Table of Contents

STATEMENT OF ORIGINALITY	I
SUPERVISOR DECLARATION STATEMENT.....	II
AUTHORSHIP ATTRIBUTION STATEMENT	III
ACKNOWLEDGEMENT	VI
TABLE OF CONTENTS	VII
SUMMARY... ..	XI
LIST OF FIGURES	XIV
LIST OF TABLES	XIX
CHAPTER 1 INTRODUCTION.....	1
1.1. MOTIVATIONS.....	1
1.2. OBJECTIVES	9
1.3. MAJOR CONTRIBUTIONS.....	10
1.4. ORGANIZATION OF THIS THESIS.....	12
CHAPTER 2 LITERATURE REVIEW	13
2.1. REVIEW OF LINEAR POWER AMPLIFIERS	13
2.1.1. Class A Power Amplifier	14
2.1.2. Class B Power Amplifier	15

2.1.3.	Class AB Power Amplifier	16
2.2.	REVIEW OF CLASS D AMPLIFIERS	17
2.2.1.	Modulation Schemes for Analog Class D Amplifiers	18
2.2.1.1.	Pulse-Width-Modulation	19
2.2.1.2.	Delta-Sigma Modulation	22
2.2.1.3.	Bang-Bang Control.....	25
2.2.1.4.	Self-Oscillating.....	26
2.2.2.	Class D Amplifier Output Stage	27
2.2.2.1.	Output Power Transistors and Drivers	28
2.2.2.2.	Control Logic.....	30
2.2.2.3.	Feedback Model	32
2.2.3.	Filterless Class D Amplifier.....	34
2.3.	CONCLUSIONS.....	36
 CHAPTER 3 NON-LINEARITIES OF PWM-IN PWM-OUT CLASS D		
	AMPLIFIERS	40
3.1.	INTRODUCTION	40
3.2.	ANALYSIS OF PIPO CLASS D AMPLIFIERS	44
3.2.1.	Derivation of Distortions	45
3.2.2.	Derivation of PSRR	52
3.3.	DESIGN AND VERIFICATION OF A PIPO CDA	57
3.4.	SIMULATION RESULTS	58
3.5.	CONCLUSIONS.....	61

CHAPTER 4 LOW-POWER HIGH-EFFICIENCY FILTERLESS BANG-	
BANG CLASS D AMPLIFIER	62
4.1. INTRODUCTION	62
4.2. CONVENTIONAL BANG-BANG CONTROL CDA.....	63
4.3. PROPOSED 3-STATE FILTERLESS BANG-BANG CONTROL CDA	66
4.4. RESULT AND VERIFICATION	72
4.5. CONCLUSIONS.....	76
CHAPTER 5 ANALYSIS AND DESIGN OF CLASS D AMPLIFIERS FOR	
SUPPLY MODULATORS.....	77
5.1. INTRODUCTION	77
5.2. OPTIMIZATION OF THE SUPPLY MODULATOR FOR WIDEBAND APPLICATIONS	80
5.2.1. Effect of Threshold Current and Propagation Delay on Hysteresis	83
5.2.2. Optimization of Hysteresis and External Inductor.....	86
5.3. PROPOSED SUPPLY MODULATOR.....	91
5.3.1. System Architecture	91
5.3.2. Proposed High-speed Current Comparator in the Hysteresis Controller	94
5.3.3. Proposed Class AB Amplifier.....	95
5.3.4. Analysis of Class D Output Stage*	100
5.3.4.1. Power Dissipation Due to On-Resistance.....	107

5.3.4.2.	Power Dissipation Due to Parasitic Capacitance.....	108
5.4.	MEASUREMENT RESULTS.....	113
5.5.	CONCLUSIONS.....	125
CHAPTER 6 CONCLUSIONS & RECOMMENDATIONS.....		126
6.1.	CONCLUSIONS.....	126
6.2.	RECOMMENDATIONS AND FUTURE WORK	127
AUTHOR’S PUBLICATIONS		129
BIBLIOGRAPHY		132

Summary

This Ph.D. program pertains to investigations into the mechanisms and parameters affecting the non-idealities and power-efficiency of Class D Amplifiers (CDAs), and our ensuing novel circuit designs (and proposal of novel architectures) to mitigate the aforesaid. There are three specific CDA architectures. The first is the PWM-In PWM-Out (PIPO) CDA, an emerging CDA whose input is PWM, hence highly compatible with digital signal processing. Our effort pertains to addressing its relatively high inherent non-linearities. The second is the Bang-Bang CDA, arguably the simplest CDA architecture, hence the CDA with the lowest hardware, and potentially the most power-efficient CDA. Our effort pertains to the design of a 3-state Bang-Bang CDA – to our knowledge the first 3-state (filterless) Bang-Bang CDA reported in literature – where we ascertain its fidelity and power-efficiency. The third is the high-frequency high-efficient CDA for the supply modulator of the Envelop Tracking (ET) Power Amplifier (PA) which serves as the power supply to a radio frequency (RF) PA. Our effort pertains to addressing the power-efficiency of the wideband PA.

The PIPO CDA is advantageous over conventional CDAs because the cumbersome Digital-to-Analog Converter is not required – the PIPO CDA innately provides for ‘data conversion’. Interestingly despite the apparent advantages of the PIPO CDAs, the reported PIPO CDAs hitherto suffer from relatively high non-linearities and low power-efficiency. We analytically investigate the fidelity (qualified by Total Harmonic Distortion, THD) and the noise immunity (qualified by Power Supply

Rejection Ratio, PSRR) and derive the mechanisms thereto. On the basis of our investigations, we propose a PIPO CDA whose THD and PSRR parameters are notably superior over its conventional counterparts, on average by 50-75% and 6dB, respectively; in terms of absolute values over the entire modulation index, the THD and PSRR ranges from 0.01% - 0.014% and from 78dB - 38dB, respectively.

For the Bang-Bang CDA, heretofore, only single-ended and 2-state Bang-Bang control CDAs have been reported. These topologies are disadvantageous because their outputs require a bulky output lowpass filter, hence expensive and incongruous with present-day need for small form-factor. We propose the first-ever 3-state Bang-Bang CDA, i.e., a filterless Bang-Bang CDA. Compared to the conventional first-order filterless 3-state CDAs, our proposed filterless 3-state Bang-Bang control CDA features the simplest hardware and high power-efficiency, 93%-95% for modulation indexes above 0.2, but with somewhat compromised fidelity. Nevertheless, the fidelity thereto is sufficient for typical ultra-low-power applications such as low-to-mid performance wearable devices.

For the high-frequency high-efficient CDA for the ET RF PA, we investigate its power dissipation on optimization of the supply modulator taking into consideration the propagation delay, and show that a controller with zero threshold current not only improves the bandwidth but also reduces the power dissipation. On the basis of our investigations, we propose improved circuits for a conventional CDA architecture but with significantly improved power dissipation. This CDA in part

provides for a supply modulator for ET PAs for 40MHz LTE-A protocols, featuring high output power (2.5W), high peak efficiency (91%), high output voltage swing (3V) and low output ripple noise (4mVrms) at 3.6V supply. The ET PA embodying our proposed supply modulator achieves a high power-efficiency of 41.4% at 28.5dBm peak output power and 34.4% at 3dB backoff – a significant >1.6x improvement over the RF PA without the supply modulator.

From an overall perspective, the contributions in this PhD program are interesting and pertinent as they provide valuable insights to the design of CDAs.

List of Figures

Figure 1-1: Block diagram of a closed-loop CDA.....	3
Figure 1-2: An audio system of (a) conventional PWM CDA with a preceding DAC, and (b) PIPO CDA with a preceding digital-like PWM modulator.....	4
Figure 1-3: Block diagram of a Bang-Bang control CDA.....	6
Figure 1-4: Block diagram of an ET PA with a hybrid supply modulator	8
Figure 2-1: Class A amplifier schematic and waveform	14
Figure 2-2: Class B amplifier schematic and waveform.....	15
Figure 2-3: Class AB amplifier schematic and waveform.....	16
Figure 2-4: Block Diagram of a typical (a) digital CDA, and (b) analog CDA	17
Figure 2-5: Schematic of an open-loop PWM CDA.....	20
Figure 2-6: Generated PWM Signal	20
Figure 2-7: Schematic of a single-feedback 2 nd order PWM closed-loop CDA.....	22
Figure 2-8: Schematic of a 1 st order synchronous $\Delta\Sigma$ CDA	24
Figure 2-9: Schematic of a 1 st -order asynchronous $\Delta\Sigma$ CDA	25

Figure 2-10: Block diagram of a Bang-Bang control CDA	25
Figure 2-11: Block diagram of a self-oscillating CDA.....	26
Figure 2-12: Schematic of CDA output stages and their drivers in (a) PMOS-NMOS configuration, and (b) NMOS-NMOS configuration.....	29
Figure 2-13: (a) Output transistors with separate drivers, and (b) output waveforms for high and low drivers	31
Figure 2-14: Schematic of a deadtime circuit using the non-over lapping logic	32
Figure 2-15: Linear model of open-loop CDA	33
Figure 2-16: Linear model of closed-loop CDA.....	33
Figure 2-17: Block diagram of a filterless CDA.....	35
Figure 2-18: Waveforms of a filterless CDA with a sinusoidal input signal.....	36
Figure 2-19: Block diagram of (a) a conventional PA, and (b) an ET PA	37
Figure 2-20: Comparison of power dissipations in ET PA and linear PA.....	38
Figure 3-1: Block diagrams of (a) a conventional PWM CDA with a preceding DAC, and (b) a PIPO CDA with a preceding digital PWM modulator	42
Figure 3-2: Schematic of a PIPO CDA.....	45

Figure 3-3: Signal waveforms of a PIPO CDA in a one period (for illustration and not in scale)	47
Figure 3-4: Block diagram of the (a) the PIPO CDA, and (b) equivalent gain model of the PWM modulator	53
Figure 3-5: THD (%) versus modulation index for a PIPO CDA and a conventional CDA	60
Figure 3-6: PSRR (dB) versus Supply noise frequency (Hz) for the PIPO CDA (both simulated and calculated) and a conventional CDA	61
Figure 4-1: (a) Single-ended Bang-Bang CDA, and (b) its waveforms; (c) 2-state BTL Bang-Bang CDA, and (d) its waveforms	65
Figure 4-2: (a) The proposed 3-state filterless Bang-Bang control CDA, and (b) its waveforms.....	67
Figure 4-3: Waveforms of Bang-Bang controller upper branch	68
Figure 4-4: Output signal waveform V_{out_p} - V_{out_n}	73
Figure 4-5: THD versus modulation index M	74
Figure 4-6: Power-efficiency plot against modulation index M for Case 1	75
Figure 5-1: Block diagram of an ET PA with a hybrid supply modulator	80

Figure 5-2: Simulated frequency response of i_{AB} and i_D	81
Figure 5-3: Typical current waveforms of the supply modulator tracking (a) low-frequency input signals, and (b) high-frequency input signals	82
Figure 5-4: Simulated power-efficiency with various external inductors	90
Figure 5-5: Schematic of the supply modulator embodying a proposed delay-based hysteresis controller, a proposed wideband Class AB amplifier, and a high power-efficiency CDA	92
Figure 5-6: The proposed wideband Class AB amplifier: (a) simplified schematic, and (b) model	96
Figure 5-7: Simulated results of the proposed Class AB amplifier: (a) frequency response, and (b) closed-loop output impedance	99
Figure 5-8: The model of CDA output stage including driver and parasitics.....	100
Figure 5-9: Driving and modulated signals of CDA output stage with (a) current flows into load, and (b) current flows out of load.....	101
Figure 5-10: Current flow in CDA output stage during state transitions where (a) from state (i) to (ii), (b) from state (ii) to (iii), (c) from state (iii) to (iv), (d) from state (iv) to (i), (e) from state (v) to (vi), (f) from state (vi) to (vii), (g) from state (vii) to (viii), and (h) from state (viii) to (v)	106

Figure 5-11: Microphotograph of the prototype supply modulator.	114
Figure 5-12: (a)The measured static power-efficiency; The comparison of the static power-efficiency with the state-of-the-art designs at (b) different output power, and (c) different normalized output power	116
Figure 5-13: 35MHz measured waveforms (a) switching frequency, and (b) output ripple	118
Figure 5-14: Dynamic power-efficiency	119
Figure 5-15: Time domain response of our supply modulator tracking a 60MHz 1.4V _{pp} sinusoidal signal (from 1.1V to 2.5V)	120
Figure 5-16: Time domain response of our supply modulator tracking a 40MHz LTE-A envelope signal	121
Figure 5-17: Measured RF PA output spectrum for 20MHz LTE signal at 27dBm RF PA output power	122
Figure 5-18: PAE of the ET PA and the stand-alone RF PA	123

List of Tables

Table I: Circuit Parameters of the designed 3-State Bang-Bang CDA.....72

Table II: Benchmark of the state-of-the-art filterless CDAs75

Table III: Results of corner simulations for quiescent current98

Table IV: Benchmark of state-of-the-art supply modulators124

Chapter 1 Introduction

1.1. Motivations

The demand for increasingly power-efficient electronic devices with high quality audio output, particularly portable audio devices and smartphones, remains unabated. For example, in some audio devices, e.g., hearing instruments (hearing aids [1, 2]) and MP3 players, the power amplifier therein is often the most power-dissipative block. In smartphones, on the other hand, its limited battery lifetime the most often complaint and in most applications, the most power-dissipative block is the radio-frequency (RF) power amplifier (PA) [3]. Interestingly, the Class D Amplifier (CDA) is a common circuit block as an audio amplifier and an amplifier to provide the varying supply voltage to the RF PA [2, 4-11]. In addition to power-efficiency considerations [12-14], contemporary audio-related electronic devices are also expected to feature high quality audio, if possible to high-fidelity standards [15] (e.g., qualified by Total Harmonic Distortion, THD [14, 16-22]), and in the presence of circuit noise (qualified by Power Supply Rejection Ratio, PSRR [19, 21, 23-27]).

The CDA was probably first proposed in 1958 [28], and its primary motivation is high power-efficiency, theoretically 100% power-efficient. Interestingly, in practice, by means of careful design, the power-efficiency of many practical CDAs at full modulation index (equivalent to maximum output power) is high – typically higher than 90%. Not unexpectedly, CDAs, at this juncture, are the audio amplifiers of

choice, and are increasingly replacing their linear counterparts [29-33] (Class A, Class B and Class AB amplifiers) largely for their superior power-efficiency [3].

In general, in the perspective of CDA output stages [12, 13, 34], there are two amplifier configurations/topologies – single-ended (SE) and fully-differential (bridge-tied-load, BTL). The former is widely used in earphones/headsets due to the sharing of the common ground between the left and right channels (of the stereo amplifiers). The fully-differential, on the other hand, is usually preferred for general speakers due to the availability of individual grounds and to the 4x output power for the same V_{DD} (supply rail).

Despite the power-efficiency advantage of CDAs over their linear counterparts, CDAs nevertheless, in general, suffer from lower fidelity largely due to switching distortions [3, 16, 23, 35-40]. The non-linearities generally include THD, Inter-Modulation Distortion (IMD), Power Supply Induced Inter-Modulation (PS-IMD) and PSRR, where the distortions are desired to be low and the PSRR high.

Of the various non-linearities, THD [14, 17-22] is arguably of the greatest interest because THD is typically quoted and generally easily perceived psycho-acoustically. In general, the design for high power-efficiency and low distortion are somewhat a trade-off, i.e., they are contradictory parameters. For example, high fidelity often stipulates the need for high switching frequency [14, 17, 19, 41], but high switching frequency compromises the power-efficiency. The need for these contradictory attributes renders the design for high fidelity CDAs, yet with high power-efficiency,

a somewhat formidable design exercise but necessary in view of the demands and expectations of contemporary audio-related electronic devices.

Consider the basic design of an analog CDA in view of the aforesaid imperative attributes. Fig. 1-1 depicts the block diagram of a prevalent closed-loop analog CDA consisting of a modulator, an output stage, a low-pass filter [42-46] (for non-filterless CDAs) and a load. The modulator modulates the analog input signal to a digital-like pulse train, and serves as switch control signal to the output stage. The output stage is largely a power buffer which provides sufficient power to drive the low-pass filter and the load.

Figure 1-1: Block diagram of a closed-loop CDA

At this technical juncture of the design of CDAs, there are three motivations of interest in this Ph.D. Program. These three motivations will now be delineated in turn.

The first motivation pertains a CDA amplifier whose input is PWM vis-à-vis the more conventional analog signal. There are a number of reported modulation techniques for CDAs [17, 40, 41, 47-53]. Of these modulation techniques, the Pulse-Width-Modulation (PWM) is the most prevalent due to its high power-efficiency,

hardware simplicity and superior performance [15, 19, 20, 37, 54-56]. In a typical audio output system as depicted in Fig. 1-2(a), the input of the conventional PWM CDA is an analog signal provided by a Digital-to-Analog Converter (DAC) embodied in the codec connected to the preceding Digital Signal Processor (DSP). This architecture requires the DAC to feature high-fidelity (which is usually power-consuming), as any noise or distortion introduced by the DAC will be amplified by the CDA without any suppression. Furthermore, for a mobile device where many modules are integrated in a System-on-Chip (SoC), noise can be easily coupled to the DAC via the substrate and/or supply rails, hence degrading the performance of the DAC. Put simply, in view of the desire to obtain ever-increasing integration, lower power dissipation (hence higher power-efficiency) and high fidelity, it is desirable to consider an approach where the DAC is unnecessary.

Figure 1-2: An audio system of (a) conventional PWM CDA with a preceding DAC, and (b) PIPO CDA with a preceding digital-like PWM modulator

Such an audio system architecture has been reported [57] and is depicted in Fig. 1-2(b), where the said DAC is not employed – specifically, a PWM-in PWM-out (PIPO) CDA that directly receives the digital-like input signal from the preceding digital PWM modulator embodied in the DSP. As most of the computation is now computed by digital means (thereby compatible with technology scaling, i.e., smaller transistor feature size and lower supply voltage), this PIPO architecture potentially features smaller form-factor and higher power-efficiency than its conventional CDA counterpart. This particularly interesting and pertinent in view of the ever-increasing demands of wearability and portable mobile devices with extended battery life. Nevertheless, the digital PWM may suffer some drawbacks arising from the fixed sampling moments, while digital PWM need not to be sampled at fixed intervals. [58, 59]

At this juncture, the design art [15, 19, 20, 37, 38, 54-56, 60] for conventional PWM CDAs is relatively mature where the methodologies to mitigate their inherent relatively high non-linearities are well established. However, for the PIPO CDA where the input is a PWM signal, the investigations into its inherent non-linearities, including THD and PSRR, and methodologies to mitigate the said non-linearities remain largely unreported. In short, there are imperative motivations to investigate and to design PIPO CDAs, particularly to obtain higher noise immunity, smaller form-factor and yet higher power-efficiency than conventional PWM CDAs.

The second motivation pertains to a somewhat esoteric CDA whose hardware is arguably the simplest, thereby providing the opportunity for the most power-efficient design. Amongst the aforesaid modulation techniques, the Bang-Bang

control CDAs [38, 40, 61-63] are arguably the most advantageous for low-power power-critical applications. A typical block diagram of a Bang-Bang control CDA is depicted in Fig. 1-3 below. This is due to their significantly higher power-efficiency (in part due to their hardware simplicity), comparable fidelity (qualified by THD) and higher noise immunity (qualified by PSRR) for the same hardware. Specifically, it was reported [38] that for some micro-power applications, the power-efficiency of the Bang-Bang control CDA is a high 53% whilst that of the competing and conventional PWM CDA is substantially lower at 35%, at the nominal operating condition of Modulation Index $M = 0.15$ (15dB below the maximum due to the crest factor of audio/speech signal). Furthermore, in said reported design, the THD and PSRR of Bang-Bang Control CDAs are respectively 0.08% and 70dB, whilst the THD and PSRR of the competing PWM CDA are respectively 0.09% and 45dB. In short, the Bang-Bang control CDA is arguably the most power-efficient architecture for low-power power-critical applications, yet featuring comparable or better fidelity than the more common PWM CDAs of compatible hardware.

Figure 1-3: Block diagram of a Bang-Bang control CDA

The reported Bang-Bang control CDAs [38, 61] embody either the single-ended or the 2-state Bridge-Tide-Load (BTL) architecture/topology. The major drawback of the single-ended and 2-state BTL Bang-Bang control CDAs is that an output lowpass filter is required to filter the high frequency carrier components, i.e., it is not a filterless CDA. The output lowpass filter is highly undesirable as it typically occupies >70% of the PCB area and adds 30% further cost, thereby undesirably substantially increases the overall form factor and the cost. The 3-state (filterless) CDA, on the other hand, mitigates the aforesaid shortcomings associated with the output lowpass filter, by eliminating the need of the output lowpass filter. However, hitherto the filterless Bang-Bang control CDA remains unreported. Put simply, there are imperative motivations to investigate and to design the 3-state Bang-Bang CDAs, particularly for lower power dissipation and yet higher power-efficiency than conventional PWM CDAs.

The third motivation pertains to a CDA employed as part of a supply modulator for an RF PA. The advanced communication protocols, e.g. LTE and LTE-A, impose stringent requirements on the linearity of the RF PA, yet requiring high Peak-to-Average-Power-Ratio [64] – translating to low power-efficiency in conventional RF PAs [65], hence reduced battery-life. Of the various reported methods to improve the power-efficiency of RF PAs, the Envelope Tracking (ET) has been reported to be one of the most effective means [5, 66-85]. The supply modulator in the ET PA is essentially a power management circuit for the RF PA. The mechanism thereto is the supply modulator constantly providing a dynamically changing supply to the RF PA based on the time-varying envelope of the RF signals. In this fashion, the RF

PA is kept nearly always in compression, where its power-efficiency is high and avoiding operation in the back-off condition.

Fig. 1-4 depicts the block diagram of a supply modulator, comprising a wideband Class AB amplifier, a high-efficiency CDA and a hysteresis controller. The supply modulator provides a variable power supply to the RF PA. Many supply modulators in ET PAs employ a hybrid topology (Class AB amplifier-cum-CDA) [5, 66-68, 70, 72-74, 78-83]. This is because the hybrid topology features higher power-efficiency compared to the Class AB amplifier-only topology [75], higher bandwidth and lower output ripple compared to the CDA-only topology [69, 71, 76, 77, 84, 85]. Nevertheless, at this juncture, the major shortcoming of the state-of-the-art supply modulators [5, 66-72, 75-85] is their limited bandwidth of $\leq 20\text{MHz}$, which is insufficient for LTE-A applications whose bandwidth is 40MHz-100MHz.

Figure 1-4: Block diagram of an ET PA with a hybrid supply modulator

Another shortcoming is the low output power. For instance, the designs reported in [67, 70, 79] operate at a low supply voltage of 1.2V supply, hence resulting a low output voltage of <1V and low maximum output power of <0.2W. This low output power is, however, generally unacceptable for contemporary communication protocols including LTE and LTE-A. The limited bandwidth and/or output power is in part due to the inevitable trade-off between bandwidth, output power, output noise and power-efficiency. Put simply, there are imperative motivations to investigate the power dissipation mechanisms of CDAs, particularly a wideband high-efficiency CDA for supply modulator for ET PAs.

1.2. Objectives

The overall objectives of this Ph.D. program pertain to the three motivations delineated in Section 1.1. particularly they are to analyse and investigate the mechanisms and parameters affecting the non-idealities of CDAs, including the proposal of novel architecture and/or new design methodologies to improve their fidelity and their power-efficiency. The specific objectives are:

- (i) For the PIPO CDA,
 - (a) An investigation into the mechanisms of and parameters affecting its non-idealities; and
 - (b) To propose a novel architecture(s) and/or new design methodologies to mitigate the said non-linearities.

- (ii) For the Bang-Bang CDA,
 - (a) An investigation into the parameters affecting its power-efficiency; and
 - (b) To propose a 3-state Bang-Bang control CDA where the output lowpass filter is not required.

- (iii) For the CDA in the supply modulator (comprising CDA and class AB amplifier) for ET PAs,
 - (a) An investigation into the mechanisms of its power dissipation; and
 - (b) To propose a supply modulator that simultaneously features the wide bandwidth, high output power, high peak efficiency, and low output noise.

1.3. Major Contributions

The contributions in this Ph.D. program pertain objectives (i), (ii) and (iii) in Section 1.2 earlier. Specifically,

- (i) For the PIPO CDA,
 - (a) The THD is analytically investigated, and its expressions derived, thereby depicting the mechanisms thereto. The derived expressions are verified by means of computer simulations based on a commercial 65nm CMOS process; and

- (b) The PSRR is similarly analytically investigated, and its expression derived, thereby depicting the mechanisms thereto. The derived expressions are also similarly verified by computer simulations based on the same commercial 65nm CMOS process. It is shown that the PIPO CDA advantageously featured superior performance (THD and PSRR) compared to the conventional CDA that embodies the same integrator and output stage.
- (ii) For the Bang-Bang CDA,
 - (a) The first-ever 3-state filterless Bang-Bang control CDA is proposed to the best of our knowledge; and
 - (b) Its filterless attribute eliminates the undesirable bulky and expensive output lowpass filter. The proposed 3-state Bang-Bang control CDA featured a simple hardware and high power-efficiency of ~95%. Nevertheless, the proposed 3-state Bang-Bang control CDA somewhat compromises the fidelity (in terms of THD) but sufficient for many low-power power-critical audio applications.
- (iii) For the CDA in supply modulator (composing CDA and Class AB amplifier) for ET PAs,
 - (a) The mechanisms of power dissipation are investigated; and
 - (b) A supply modulator is proposed featuring simultaneously the wide bandwidth (40MHz), high output power (2.5W), high peak efficiency (91%), high output voltage swing (3V) and low output ripple noise

(4mVrms) at 3.6V supply. The ET PA embodying our proposed supply modulator achieves a high power-efficiency of 41.4% at 28.5dBm peak output power and 34.4% at 3dB backoff – a significant >1.6x improvement over the RF PA without the supply modulator.

1.4. Organization of this Thesis

This thesis is organized in following manner.

Chapter 1 presents the introduction and overview of this Ph.D. program, including the motivations, objectives and contributions.

Chapter 2 provides a comprehensive and critical literature review. The CDA modulation techniques and output stage design of CDAs are reviewed in some detail.

In Chapter 3 – Chapter 5, the candidate's research contributions are delineated, including the analysis and design of PIPO CDA, low-power high-efficiency 3-state filterless Bang-Bang control CDA, and the analysis and design of the CDA for a supply modulator.

In Chapter 6, conclusions are drawn and recommendations for future work are delineated.

Chapter 2 Literature Review

In this chapter, we provide a comprehensive and critical literature review of the various CDA architectures and designs. The review commences with a succinct overview of CDAs and their linear counterparts. As the analog CDA is the CDA of interest in this research program, a comprehensive review of modulation schemes for analog CDAs is thereafter presented. The CDA output stage and the filterless CDA are also reviewed as well as a brief review of the supply modulator.

This literature review serves as a preamble to the contributions delineated in Chapter 3, 4 and 5.

2.1. Review of Linear Power Amplifiers

The design art of classical amplifiers is very mature [3]. These classical amplifiers are typically linear amplifiers and classified by their output stage biasing conditions [86]. As expected, power amplifiers with different output stages will exhibit different levels of power-efficiency and performance even when they have identical input and gain stages.

The most common linear power amplifiers are Class A, Class B and Class AB. Operation principle of these linear power amplifier will now be reviewed, including the infidelity and power-efficiency. For sake of simplicity, all amplifiers illustrated herein will be based on the bipolar junction transistor (BJT).

2.1.1. Class A Power Amplifier

In the Class A amplifier, the conduction angle is 360° , i.e., the transistor conducts for the entire cycle. Its output is typically an emitter follower stage. The output power transistors are biased at fixed current I_{bias} and is continuously turned on. Consequently, the two transistors in the Class A output stage will conduct current and operate in active region regardless of input or output signals. The output waveform of an emitter follower stage (using n-type devices) is depicted in Fig. 2-1 below.

Figure 2-1: Class A amplifier schematic and waveform

As the transistors are always in active region, the Class A amplifier presents a better linearity compared to other classes of linear amplifiers, but at the cost of higher power consumption, even if there is no input signal. It has been shown in literature [86] [87] that the maximum power-efficiency occurs at maximum output signal swing (maximum output), and is theoretically 25% and 50% for single-end stage and

push-pull stage, respectively, under the assumption that the devices are ideal. At expected, the power-efficiency is considerably lower when the signal swing is lower.

2.1.2. Class B Power Amplifier

Compared with the Class A amplifier, the Class B amplifier features higher power-efficiency but at the expense of signal fidelity [3]. The class B output stage has two transistors which will not be turned on at same time. As shown in Fig.2-2 below, each transistor will conduct half cycle thus the conduction angle is 180° .

Figure 2-2: Class B amplifier schematic and waveform

Theoretically, the Class B power amplifier has a maximum power-efficiency of 78.5% [86, 87]. One advantage of the Class B amplifier is that there is no power consumption when there is no input signal. However, both transistors will be turned off when the signal is low ($< \text{threshold voltage } V_{th}, 0.7\text{V}$), which results non-

conduction, rendering a severe crossover distortion. To avoid this kind of distortion and the ensuing non-linearity, this theoretical maximum power-efficiency is never achieved in a practical design [3].

2.1.3. Class AB Power Amplifier

The Class AB amplifier is a compromise on a hybrid between the Class A amplifier and the Class B amplifier. The topology involves adding a biasing circuit to the Class B amplifier, such that at least one output transistor is on within the range of negative and positive threshold voltages ($-0.7\text{V} \sim 0.7\text{V}$). As depicted in Fig. 2-3, each transistor has a conduction angle of larger than 180° but much less than 360° [86].

Figure 2-3: Class AB amplifier schematic and waveform

In view of the hybrid configuration, the Class AB amplifier expectedly has a trade-off between the power-efficiency and linearity. The power-efficiency will be

reduced when both of the output transistors are simultaneously turned on, but the signal fidelity will in turn be improved. This trade-off of efficiency-linearity, which is between the Class A amplifier and the Class B amplifier, makes Class AB very popular in industry.

2.2. Review of Class D Amplifiers

As depicted in Fig. 1-1 earlier, a typical CDA consists of a modulator, an output stage and a load with a preceding low-pass filter (for non-filterless CDAs) or sometimes a band-pass filter. The CDA can be generally classified into two classes, digital CDA and analog CDA as depicted in Fig. 2-4, and this is reflected by the modality of its input signal [3, 49]. The difference between digital and analog CDAs is largely the representation of the signal in their modulators, where the former is digitally computed and the latter, analog processed.

Figure 2-4: Block Diagram of a typical (a) digital CDA, and (b) analog CDA

The digital CDA employs a digital modulator to process a digital signal, e.g., the Pulse-Coded-Modulation signal. The preceding circuit to a digital CDA is typically a microprocessor. The analog CDA, on the other hand, employs an analog modulator to amplify an input analog signal. There are several considerations in the design of the digital CDA, and arguably, the key challenge is to reduce the clock rate, which is usually the requirement for accurate timing. At this juncture, the design-art of digital CDAs is relatively mature [36, 88].

Of the two CDAs, the analog CDA is more prevalent, in part due to the industry practice of having an analog output from the DAC, i.e., the analog input to the analog CDA. Although the digital CDA features smaller IC area and lower power-dissipation because of the elimination of DAC, the digital CDA is susceptible to supply noise largely due to its open-loop structure; although the digital CDA can embody negative feedback, the hardware overheads are considerable [14, 36]. This is unlike the analog CDA which typically embodies negative feedback, - and hence reduced non-linearities.

2.2.1. Modulation Schemes for Analog Class D Amplifiers

It was earlier shown in Fig. 2-4(b), that the modulator in the analog CDA takes analog signal as the input and modulates it into a digital-like output signal. In general, the analog CDAs can be classified into four general types based on their different modulation schemes - Pulse Width Modulation (PWM) [15, 19, 20, 24, 54,

55], Sigma-Delta Modulation [48, 62, 89], Bang-Bang Control [38, 40, 49, 61, 63] and Self-Oscillating [39, 41, 47, 87, 90, 91]. They will now be reviewed in turn.

2.2.1.1. Pulse-Width-Modulation

Amongst these modulation topologies, the PWM is the most prevalent adopted technique in CDA design due to its relatively simple circuitry and low power dissipation. A pulse train is generated from a PWM modulator where the pulse width is modulated. The PWM CDA can be designed as either open-loop or closed loop [15, 54].

The open-loop CDA, as depicted in Fig. 2-5 as expectedly, has a simple hardware structure and often used in low-fidelity applications. The PWM signal is basically generated from a comparator by comparing the input signal V_{in} (sinusoidal in this case) with a referencing signal V_C (usually a higher frequency triangular wave), hence producing the output pulse train V_M depicted in Fig. 2-6. In the PWM pulses, the voltage level of V_M is high when input signal is larger than the reference signal and low when the input signal is smaller.

Figure 2-5: Schematic of an open-loop PWM CDA

Figure 2-6: Generated PWM Signal

For a sinusoidal input signal V_{in} , the mathematical expression of output PWM signal V_M is expressed as [51]:

$$\frac{V_M}{V_{in}} = M \cos(2\pi f_{in} t) + 4 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(4m\pi f_c t + 4n\pi f_{in} t) * \sin\left(\frac{m+n}{2}\pi\right) \quad (2.1)$$

where M is the modulation index (ratio of maximum input signal amplitude over maximum carrier amplitude), f_{in} and f_c are input signal and carrier frequencies respectively, and $J_n(\cdot)$ is the n -order Bessel function of the first kind.

According to this equation, the ideal open loop PWM amplifier has no harmonic distortion components, the THD = 0. For completeness, THD [17] is defined as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \dots + V_\infty^2}}{V_1} \quad (2.2)$$

where V_1 is the magnitude at fundamental frequency, and $V_2, V_3 \dots V_\infty$ are the 2nd, 3rd ... ∞^{th} harmonic components at 2, 3 ... ∞ times of fundamental frequency respectively.

Although the output has theoretically zero THD, an open-loop PWM is practically unacceptable due to high non-linearities from a number of mechanisms, including non-ideal carrier, dead time and output stage [16]. At this juncture, these non-linearities are well understood and can be mitigated by means of negative feedback [42]. Put differently, a practical PWM amplifier is designed with feedback to overcome the non-linearities of open-loop structure, i.e., a closed-loop architecture [14]. A block diagram of a single-feedback 2nd order PWM closed loop CDA is shown in Fig. 2-7 below.

Figure 2-7: Schematic of a single-feedback 2nd order PWM closed-loop CDA

In terms of THD, it has been shown in literature that by means negative feedback, the open-loop THD is suppressed by a factor of $(A\beta + 1)$, where $A\beta$ is the loop gain [17]. A detailed analysis on the THD due to the phase and duty cycle errors from negative feedback was reported in [17].

2.2.1.2. Delta-Sigma Modulation

The Delta-Sigma ($\Delta\Sigma$) CDA is another well-known CDA modulation [3, 48, 51] for its lower output noise and lower non-linearities compared with other CDA modulation techniques. The modus operandi of $\Delta\Sigma$ CDA is similar to $\Delta\Sigma$ data converters, and in general a high order ($> 3^{\text{rd}}$ order) modulation is used to significantly suppress the out-of-band noise. Nevertheless, the drawbacks of $\Delta\Sigma$ CDA include increased hardware complexity and high clock frequency.

The $\Delta\Sigma$ CDAs can be categorized into: (i) synchronous $\Delta\Sigma$ CDA, and (ii) asynchronous $\Delta\Sigma$ CDA based on different quantizer designs. The quantizer of synchronous $\Delta\Sigma$ CDA synchronizes the switching with the clock. The quantizer for asynchronous $\Delta\Sigma$ CDA, on the other hand, is time-continuous without clock, and the switching is dependent on the input signals.

The synchronous $\Delta\Sigma$ CDA as depicted in Fig. 2-8 comprises an integrator, a quantizer realized using a comparator followed by a D flip-flop with fixed clock frequency, an output stage with feedback network and a load. The integrator integrates the difference between the input and the output signals, and feeds its output to a comparator with pre-determined reference. The D flip-flop thereafter samples the comparator output at a high sampling frequency to generate a Pulse Density Modulated (PDM) signal. This digitalized PDM signal drives the output stage and finally the desired analog signal will be recovered on the load.

It is well established in literature [48] that the non-linearities, especially in-band quantization noise, can be reduced by using a higher order modulator or increasing the sampling frequency. However, these techniques are costly from a practical perspective, where both the hardware complexity and the power dissipation are increased.

Figure 2-8: Schematic of a 1st order synchronous $\Delta\Sigma$ CDA

The asynchronous $\Delta\Sigma$ CDA as shown in Fig. 2-9 has a similar architecture as the synchronous counterpart. Instead of using comparator and D flip-flop, the quantizer of an asynchronous $\Delta\Sigma$ CDA employ a hysteresis comparator. The quantization error of the asynchronous $\Delta\Sigma$ CDA is zero theoretically [52] and this that is the advantage over its synchronous counterpart. It is because the switching is time-continuous and depend the input, instead of fixed by clock as in the synchronous $\Delta\Sigma$ CDA. The drawbacks of asynchronous $\Delta\Sigma$ CDA is that the switching frequency is varying, and undesired coupling for multiple channel designs on a single IC.

Figure 2-9: Schematic of a 1st-order asynchronous $\Delta\Sigma$ CDA

2.2.1.3. Bang-Bang Control

The Bang-Bang control CDA is less popular than the PWM and $\Delta\Sigma$ CDAs largely because of the lower linearities offered by its modulation scheme. Nevertheless, the Bang-Bang CDA features the simplest hardware and it is more power-efficient than the PWM and $\Delta\Sigma$ CDAs (and the self-oscillation CDA; see later). The block diagram of a Bang-Bang CDA is depicted in Fig. 2-10.

Figure 2-10: Block diagram of a Bang-Bang control CDA

The structure of a Bang-Bang CDA is very simple. It comprises a hysteresis comparator that serves as the Bang-Bang controller, an output stage, a feedback network and a load with a preceding low-pass filter. The Bang-Bang controller compares the error signal with its hysteresis and generates the digitalized PDM signal. This signal is thereafter driven by the output stage and recovered by the low-pass filter. It can be seen from Fig. 2-10 that the only quiescent power dissipating block of Bang-Bang CDA is the hysteresis comparator. Compared with the PWM and $\Delta\Sigma$ CDAs, both of which have a power consuming integrator, the Bang-Bang CDA features higher power-efficiency. Furthermore, the switching frequency of a typical Bang-Bang controller is lower than the PWM and $\Delta\Sigma$ CDAs, thereby leading to a lower switching power dissipation.

2.2.1.4. Self-Oscillating

The block diagram of a self-oscillating CDA is depicted in Fig. 2-11, consisting of a modulator, an output stage, a load and a feedback network. The feedback signal may be taken at either the output stage or after the low-pass filter [41].

Figure 2-11: Block diagram of a self-oscillating CDA

The modus operandi of the self-oscillating CDA is similar to a normal oscillator. Oscillation occurs when the total phase shift within the modulator and feedback network is $\geq 180^\circ$. As the oscillating mode is inherently unstable, there is no stability issues for the self-oscillating CDA.

The advantage of the self-oscillating CDA is that the feedback signal can be taken from the load after the low-pass filter (where other CDAs take their feedback input from the output of the output stage). Consequently, the non-linearities of the low-pass filter will be mitigated as the filter is within the feedback loop. Nevertheless, the drawback of the self-oscillating CDA is its relatively complex hardware as an additional I/O pin required.

2.2.2. Class D Amplifier Output Stage

As the output stage in CDA is required to feature low output impedance, its realization usually occupies the largest area ($>50\%$) and dissipates the most power ($\sim 90\%$) in a CDA [12, 13, 34]. The primary design parameter of the output stage is to achieve high power-efficiency. There are a number of function blocks within the output stage, including the power transistors with their driving circuit, control logic, etc. These blocks will now be described in turn.

2.2.2.1. Output Power Transistors and Drivers

The output power transistors are typically designed as a PMOS-NMOS inverter [91] or as a totem-pole inverter with two NMOS transistors [34, 92]. The schematics of these two configurations are shown in Fig. 2-12(a) and (b) respectively. As both configurations serve as a low impedance stage to drive the load, the last inverter size has to be large enough to provide sufficient current. As the large gate capacitance cannot be driven by a single stage, each inverter in the high-side and low-side drivers is used to drive the next inverter with high aspect ratio. The tapering ratio, which is the ratio of aspect ratio, is usually a fixed number [12].

Of the two configurations, the PMOS-NMOS output stage features simpler configuration as no external components is required. Nevertheless, the drawbacks of this configurations are a higher switching loss and a larger IC area. This is because the high-side PMOS has a lower carrier mobility which leads a three times larger area than its low-side NMOS counterpart of the same output impedance.

Figure 2-12: Schematic of CDA output stages and their drivers in
 (a) PMOS-NMOS configuration, and (b) NMOS-NMOS configuration

The advantage of the NMOS-NMOS output stage is its requirement of a much smaller IC area due to the NMOS for both high-side and low-side. However, this design needs an off-chip large bootstrap capacitor and a power diode to boost the supply of the high-side driver. This increases the component cost and enlarges the form factor undesirably.

2.2.2.2. Control Logic

The control logic of a CDA output stage [34, 92-95] is to prevent the high-side and low-side power transistors both turn on simultaneously. This transient short circuit current directly flows from V_{DD} to ground and dissipates huge power. This decreases the overall power-efficiency, and possibly damage the device, particularly when the supply voltage V_{DD} is high.

The driving topology for the power transistors to prevent this potential short current [12] is shown in Fig. 2-13(a). By means of a dead-time circuit introducing a small dead-time (~ 50 ns), these two power transistors now have different driving signals, to ensure that the high-side and low-side transistor will not turn on simultaneously. Fig. 2-13(b) depicts an example of the control signals for high-side and low-side drivers embodying the dead-time.

Figure 2-13: (a) Output transistors with separate drivers, and
(b) output waveforms for high and low drivers

There are other reported approaches including skewing [90], offset [50] and non-overlapping logic [96] etc. to prevent the short circuit current. A typical deadtime circuit using non-overlapping [96] is depicted in Fig. 2-14, which is implemented by simple combinational logic with low hardware overheads.

Figure 2-14: Schematic of a deadtime circuit using the non-overlapping logic

In the perspective of non-linearities, a small time interval introduced by the deadtime circuit will induce some undesirable distortion into the output signal when both the high-side and low-side transistor are off. This non-linearity problem is well recognized with considerable reported effort [34, 97] to minimize the distortion. The effort typically involves the cost of increasing circuit complexity [34] and the mitigation is generally very effective. The typical approach [97] involves having the deadtime to be short (in duration) to a few nano-seconds to prevent short-circuit current.

2.2.2.3. Feedback Model

A reported linear model of the open-loop CDA [24], consisting of a constant gain stage, G_{PWM} , and a noise source, N_D , is depicted in Fig. 2-15.

Figure 2-15: Linear model of open-loop CDA

According to the linear model, the output V_{OL} can then be expressed as:

$$V_{OL} = G_{PWM}V_{in} + N_D$$

It can be shown in literature that in this equation, the noise N_D directly appears at the output and manifests as distortions. There is no option available to the designer to reduce these nonlinearities of an open-loop CDA.

Figure 2-16: Linear model of closed-loop CDA

Fig. 2-16 depicts the generic closed-loop CDA linear model based on the closed-loop structure [24], where G is feedforward open-loop gain, G_{PWM} , and H is the feedback factor. The noise source N_D is the same as the one in open-loop model.

The closed-loop architecture output can be easily expressed from the linear model as:

$$V_{CL} = \frac{G}{1 + GH} V_{in} + \frac{1}{1 + GH} N_D$$

The first term in this output signal equation is the amplified input signal, while the second term is the noise source N_D but reduced by a factor of $(1+GH)$. In other words, a high loop gain GH is required to suppress noise, thereby mitigating the non-linearities, including the PSRR and the IMD (in the closed-loop CDA).

2.2.3. Filterless Class D Amplifier

The filterless CDA, is an extension of the four CDA architectures described in Section 2.2.1, where a low-pass filter (between the output power transistors and load) is rendered unnecessary, i.e., Filterless. The primary reason for the increasing acceptance of the filterless CDA [98-100] is that the elimination of the bulky output low-pass filter saves component cost as well as PCB area. Further, it has been claimed [42], perhaps somewhat contentious, that the filterless CDA features lower non-linearities than its with-filter CDA counterparts.

The modulation techniques of a filterless CDA is similar as the traditional CDA and the typical architecture of a filterless CDA is the 3-state architecture depicted in Fig. 2-17. V_{out1} and V_{out2} are the two outputs of the BTL output stage (whose supply rails are V_{DD} and $-V_{DD}$) and I_{out} is the current in the (loudspeaker) load. The filterless

CDA is feasible since the impedance presented by a typical loudspeaker is similar to the low-pass filter in the frequency range of a few hundred kHz to several MHz, i.e., the load is used as a filter.

Figure 2-17: Block diagram of a filterless CDA

The filterless CDA output waveforms for a sinusoidal input signal is depicted in Fig. 2-18. Note that this waveform is 3-state, i.e., V_{DD} , 0 and $-V_{DD}$, whereas the with-filter CDAs are 2-state. The effective switching on the load is twice the conventional with-filter CDAs although they have same switching frequency. Consequently, the power-efficiency is not affected as the switching at output stage is not increased.

Figure 2-18: Waveforms of a filterless CDA with a sinusoidal input signal

2.3. Review of Supply Modulator for Envelope Tracking Power Amplifiers

Of the various reported methods to improve the power-efficiency of RF PAs, the Envelope Tracking (ET) has been reported to be one of the most effective means [5, 66-85]. The supply modulator in the ET PA is essentially a power management circuit for the RF PA as shown in Fig. 2-19(b) comparing to its conventional counterpart in Fig. 2-19(a).

(a)

(b)

Figure 2-19: Block diagram of (a) a conventional PA, and (b) an ET PA

As depicted in the comparison in Fig. 2-20, the mechanism thereto is the supply modulator constantly providing a dynamically changing supply to the RF PA based

on the time-varying envelope of the RF signals, comparing with the conventional PA. In this fashion, the RF PA is kept nearly always in compression, where its power-efficiency is high, hence avoiding operation in the back-off condition.

Figure 2-20: Comparison of power dissipations in ET PA and linear PA

Many supply modulators in ET PAs employ a hybrid topology (Class AB amplifier-cum-CDA) [5, 66-68, 70, 72-74, 78-83]. This is because the hybrid topology features higher power-efficiency compared to the Class AB amplifier-only topology [75], higher bandwidth and lower output ripple compared to the CDA-only topology [69, 71, 76, 77, 84, 85]. Nevertheless, at this juncture, the major shortcoming of the state-of-the-art supply modulators [5, 66-74, 76-85] is their limited bandwidth of $\leq 20\text{MHz}$, which is insufficient for LTE-A applications whose bandwidth is 40MHz-100MHz. Another shortcoming is the low output power. For instance, the reported designs in [67, 78, 79] operate at a low supply voltage of 1.2V supply, hence

resulting a low output voltage of $<1\text{V}$ and low maximum output power of $<0.2\text{W}$. This low output power is, however, generally unacceptable for the recent communication protocols including LTE and LTE-A. The typical output power of an LTE/LTE-A RF PA is $\sim 27\text{dBm}$ (0.5W) taking into account the duplexer and antenna losses. Hence, the output power of the supply modulator would need to be $>1\text{W}$ for the III/V-based RF PA (with $\sim 45\%$ power-efficiency) and $>2\text{W}$ for CMOS-based RF PA (with $\sim 25\%$ power-efficiency). The limited bandwidth and/or output power is in part due to the inevitable trade-off between bandwidth, output power, output noise and power-efficiency.

2.4. Conclusions

This chapter has reviewed the architecture of CDAs and a brief review of the supply modulators. The review commenced with a succinct overview of analog and digital CDAs. A comprehensive review of modulation schemes for analog CDAs was thereafter presented and designs provided. The merits and drawbacks of different kinds of CDA modulation techniques have been discussed.

The CDA output stage and the filterless CDA have also been reviewed. Critical circuits such as the deadtime circuitry and filter designs within the output stage have also been discussed.

Chapter 3 Non-Linearities of PWM-in PWM-out Class D Amplifiers

This chapter is largely extracted from the author's publication [101], "Analysis and design of PWM-in-PWM-out Class D Amplifiers" published in the proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), 2014.

Following Chapter 1 and Chapter 2, we will delineate in this chapter our research pertaining to the PWM-in PWM-out (PIPO) CDAs to feature improved performance. Specifically, we analytically investigate the fidelity (qualified by THD) and the noise immunity (qualified by PSRR) of the PIPO CDA and derive their mechanisms. On the basis of our investigations, we design a PIPO CDA whose THD and PSRR parameters are notably superior over its conventional counterparts. Computer simulations of the designed CDA are thereafter presented to corroborate the analytical results and to demonstrate/verify the performance of the proposed PIPO CDA.

3.1. Introduction

As mentioned in Chapters 1 and 2, PWM CDAs are presently the most prevalent largely due to their hardware simplicity and low quiescent current (hence high power-efficiency) amongst the various modulation techniques. The design art for

the conventional PWM CDAs whose input is a continuous-time analog signal, is very mature [15, 51, 54]. However, for the ‘unconventional’ PWM CDAs where both the input and output are PWM signals, the design art is relatively nascent. Of particular note, that the methodologies to mitigate their inherent relatively high non-idealities remain largely unreported.

The block diagram of a typical audio output subsystem within a largely digital system whose signal processing is digital, e.g., a mobile device, is depicted in Fig. 3-1(a). The Digital Signal Processor (DSP) in the largely digital system processes audio signals in the digital domain. An audio Digital-to-Analog Converter (DAC) embodied in audio codec converts the digital audio signal into its analog form, which is subsequently received by an audio amplifier (possibly with a pre-amplifier in between as a buffer with gain) to drive a loudspeaker load.

This well-established architecture, although straightforward, requires the DAC therein to feature high-fidelity – any noise or distortion introduced by the DAC will directly be amplified by the CDA without suppression. This approach is disadvantageous for several reasons. First, said high-fidelity DACs are not only complex but also often power-consuming [102]. Second, in a mobile device where many modules are likely to be integrated into an SoC, noise (include ground-bounce noise or power supply noise induced by both audio power amplifiers and radio frequency power amplifiers) can easily couple to the DAC via the substrate and/or the supply rails. This drastically undermining the performance of the DAC [18]. Third, the DAC has a hardware cost. Put simply, it is hence highly desirable that the said DAC can be avoided.

Figure 3-1: Block diagrams of (a) a conventional PWM CDA with a preceding DAC, and (b) a PIPO CDA with a preceding digital PWM modulator

To this end, an alternative reported architecture [57] is depicted in Fig. 3-1(b) where said DAC is not employed as the ‘interface’ to the preceding digital processing circuits. The CDA therein directly receives the digital signal as its input signal. Specially, a PIPO CDA is employed to directly receive the digital PWM signal (as its input signal) from the preceding digital PWM modulator circuit within the DSP. The operation of the PIPO CDA will be discussed in detail in the next section.

We envision that this reported PIPO CDA approach could be increasingly prevalent as most of the signal processing in digital devices is computed digitally (in the preceding DSP in the electronic device embodying the CDA). This is congruous with the technological trend of having most of the computation by digital means and signal conditional by analog means, thereby, in part, exploiting CMOS technology scaling. Put simply, the PIPO CDA potentially offers increased power-efficiency,

lower non-linearities, and yet lower cost due to reduced IC area than conventional PWM CDAs. In short, PIPO CDAs is an emerging class of CDAs.

In this chapter, the distortion fidelity (qualified by THD) and the noise immunity (qualified by the PSRR) of the PIPO CDA will be analytically investigated to depict their mechanisms. On the basis of our analytical analyses, we find that, somewhat unexpectedly, the PIPO CDA features theoretical zero distortion; conventional PWM CDAs conversely incur intrinsic systematic distortions [17]. Furthermore, we show that the PSRR of the PIPO CDA is largely independent of the gain of the integrator therein, but is instead dependent on the switching frequency of the CDA. This is again somewhat unexpected because the PSRR of conventional PWM CDAs is directly affected by the integrator gain [23].

Based on our analytical results, we design a PIPO CDA, and simulations of the designed CDA are afterwards presented to corroborate our analytical results and to demonstrate the performance of the designed PIPO CDA. In addition, the performance (THD and PSRR) of the PIPO CDA is juxtaposed with that of a competing conventional CDA embodying the same integrator and output stage as that embodied in said PIPO CDA. The comparison unambiguously depicts that the PIPO CDA is superior to the conventional CDA both in terms of THD and PSRR.

The chapter is organized as follows. The operation of the PIPO CDA and our analytical investigation into the distortion are presented in Section 3.2, followed by our analysis into the PSRR of the PIPO CDA. Section 3.3 discusses the design of a

PIPO CDA. Simulation results are presented in Section 3.4 and finally conclusions are drawn in Section 3.5.

3.2. Analysis of PIPO Class D Amplifiers

Fig. 3-2 depicts the schematic design of a PIPO CDA, which consists of a 1st-order integrator, a PWM modulator, an output stage, a loudspeaker load with a preceding low-pass filter, and a feedback network. As described earlier, the input of this PIPO CDA is a digital PWM signal obtained from the preceding DSP.

The modus operandi of the PIPO CDA is as follows. The integrator therein integrates the digital input PWM signal V_{PWM_In} together with the feedback signal from the output of the output stage. The integrator output V_{int} is then compared by a PWM modulator (essentially a comparator with the inverting input port connected to AC ground) and generates a PWM output signal V_{PWM_Out} which is the input to the output stage. The output stage thereafter drives the load (with or without a preceding low-pass filter).

Figure 3-2: Schematic of a PIPO CDA

For sake of analysis, we will assume that the input signal is an ideal PWM signal and it is generated by comparing an input signal (analog) against an ideal triangular wave. In other words, the signal is assumed to be generated by analog means. This assumption is largely valid because the Audio Codec (or audio signal processing unit) in the audio output subsystem is a digital circuit whose transistors' W/L is small (hence a negligible switching time from 'on' to 'off', and vice versa), and the ensuing digital PWM signal is approximately the PWM signal with ideal 'on' and 'off' times.

3.2.1. Derivation of Distortions

The PWM signal is a series of square wave pulses in the time domain, and the PWM signal is described by three parameters – amplitude, duty cycle and phase. The

PWM signal amplitude is determined by the supply rails and its variation is due to the power supply ripples. The duty cycle and the phase of a PWM signal are varying with time and will be reflected in the output signal. Consequently, the duty cycle error and/or phase error is expected to affect the overall THD of the CDA.

As per our literature review in Chapter 2, we will derive the phase-error and show that there is zero phase-error in the PIPO CDA, i.e., the PIPO CDA has negligible duty-cycle-error and zero phase-error – in principle, highly advantageous over its conventional analog PWM counterparts. The THD of an ideal open-loop CDA is theoretically 0% as the PWM signal is sampled by comparing input signal and ideal triangular waveform [51]. In the case of a closed-loop CDA, the PWM signal is sampled between the reference triangular signal and a combined signal of the amplified input and the attenuated feedback signals. The generated PWM output signal of the closed-loop CDA may suffer from some THD [14, 17, 41] due to the duty cycle error and phase error within the combined signal (instead of the input of the open-loop CDA).

It has been shown in literature [17, 24] that distortions due to duty-cycle-error is negligible compared to the phase-error in first-order closed loop PWM CDA. Hence, only the distortions due to phase-error will be analysed. For completeness, the phase-error arises from the delay between the final (output) PWM signal and the ideal PWM signal, and is varying and signal-dependent.

Figure 3-3: Signal waveforms of a PIPO CDA in a one period
(for illustration and not in scale)

Fig. 3-3 depicts the pertinent waveforms in the PIPO CDA depicted in earlier Fig.

3-2. The analog input V_{in} is expressed as:

$$V_{in} = MV_C(0) \sin \omega t \quad (3.1)$$

where M the signal modulation index (the average for V_{PWM_In} is M),

$V_C(0)$ is the maximum signal magnitude, and

ω is the angular switching frequency.

As described earlier, V_{PWM_In} is the ideal PWM signal from the digital input by comparing the V_{in} with a triangular carrier signal V_C . V_{PWM_Out} is the output PWM signal of the PIPO CDA before the low-pass filter, and V_{int} is the output signal of the 1st-order integrator. On the basis of Fig. 3-2, it is easy to show that

$$\frac{V_{PWM_{In}}}{R_1} + \frac{V_{PWM_{Out}}}{R_3} = -C \frac{dV_{int}}{dt} \quad (3.2)$$

By re-arranging and simplification, the gradient of the integrator output V_{int} is

$$\frac{dV_{int}}{dt} = - \frac{kV_{PWM_{In}} + V_{PWM_{Out}}}{\tau} \quad (3.3)$$

$$k = \frac{R_2}{R_1} \quad (3.4)$$

$$\tau = R_2 C_1 \quad (3.5)$$

where T is the switching period,

k the closed-loop gain of the PIPO CDA, and

τ is the time constant.

The gradient of V_{int} in Fig. 3-3 can then be calculated according the value to $V_{PMM_{Out}}$

and $V_{PWM_{In}}$ on different time intervals from t_1 to t_5 .

$$\text{During } t_1: \quad \left. \begin{array}{l} V_{M1} = -V_{DD} \\ V_{M2} = V_{DD} \end{array} \right\} \Rightarrow \quad \frac{dV_{int}}{dt} = - \frac{-kV_{DD} + V_{DD}}{\tau}$$

$$\Rightarrow V_1 - V_3 = -\frac{(k-1)}{\tau} V_{DD} \cdot t_1 \quad (3.6)$$

Similarly,

$$\text{During } t_2: V_1 = \frac{(k+1)}{\tau} V_{DD} \cdot t_2 \quad (3.7)$$

$$\text{During } t_3: V_2 = -\frac{(k-1)}{\tau} V_{DD} \cdot t_3 \quad (3.8)$$

$$\text{During } t_4: V_2 = -\frac{(k+1)}{\tau} V_{DD} \cdot t_4 \quad (3.9)$$

$$\text{During } t_5: V_3 = \frac{(k-1)}{\tau} V_{DD} \cdot t_5 \quad (3.10)$$

According to the waveform and Eqns. (3.6 - 3.10), the value for V_1 and V_2 and the relation between the time intervals are derived as follows:

$$V_1 = V_{DD} \frac{(k-1)}{\tau} (t_1 + t_5) = V_{DD} \frac{(k+1)}{\tau} t_2 \quad (3.11)$$

$$V_2 = -V_{DD} \frac{(k-1)}{\tau} t_3 = -V_{DD} \frac{(k+1)}{\tau} t_4 \quad (3.12)$$

For V_{PWM_In} , we denote t_{on1} as the ‘on’ time duration when $V_{M1} = V_{DD}$, and t_{off1} as the ‘off’ time duration when $V_{PWM_In} = -V_{DD}$. Similarly, for V_{M2} , we denote t_{on2} as the ‘on’ time duration when $V_{PWM_Out} = V_{DD}$, and t_{off2} as the ‘off’ time duration when $V_{PWM_Out} = -V_{DD}$. According to the waveforms in Fig. 3-3, the ‘on’ and ‘off’ time of V_{PWM_In} can be expressed as:

$$\begin{cases} t_{on1} = t_2 + t_3 = \frac{T}{2}(1+M) \\ t_{off1} = t_1 + t_4 + t_5 = \frac{T}{2}(1-M) \end{cases} \quad (3.13)$$

$$\begin{cases} t_{on2} = t_1 + t_2 + t_5 \\ t_{off2} = t_3 + t_4 \end{cases} \quad (3.14)$$

From Eqns. (3.11 - 3.14) and the waveforms from Fig. 3-3, and with some algebraic manipulation, we can derive t_{on2} and t_{off2} for V_{PWM_Out} in terms of the switching period T , closed-loop gain k and modulation index M . The average of V_{PWM_Out} is therefore $-km$.

$$t_{on2} = \frac{(k+1)t_{on1} - (k-1)t_{off1}}{2} = \frac{T(1+kM)}{2} \quad (3.15)$$

$$t_{\text{off}2} = T - t_{\text{on}2} = \frac{T(1 - kM)}{2} \quad (3.16)$$

The phase error arises if the delay time Δt between V_{PWM_In} and V_{PWM_Out} is dependent on the input signals, i.e., the time delay between the output PWM signal and the ideal input PWM signal is dependent on the input signal [23]. Assuming V_{int} is piecewise linear, we can easily derive:

$$\Delta t = \frac{t_1 + t_2 - t_5}{2} = -\frac{k(-t_{\text{on}1} + t_{\text{off}1}) + T}{4k} = \frac{T}{4} \left(1 - \frac{1}{k}\right) \quad (3.17)$$

It can be seen from Eqn. (3.17) that, compared to V_{PWM_In} , V_{PWM_Out} is delayed by Δt . As Δt is independent of the magnitude and frequency of the input signal, the PIPO CDA does not introduce phase error. Hence, the PIPO CDA is intrinsically distortion-free. It is because it has no phase-error and, as mentioned earlier, the first-order PIPO CDA does not suffer from duty-cycle-error. Interestingly, this is somewhat unexpected because conventional closed-loop CDAs typically incur intrinsic system errors, i.e. conventional CDAs incur distortions, even if all the building blocks therein are ideal.

Nevertheless, it would be overly optimistic to expect a distortion-free PIPO CDA, as distortions would arise from other mechanisms, including the non-ideal output stage and non-ideal active circuits, such as operational amplifiers. We will show later that, despite the distortions introduced into PIPO CDAs by other non-idealities,

the PIPO CDA still features favourable THD over the conventional closed-loop CDA; see Fig. 3-5 later.

3.2.2. Derivation of PSRR

The PIPO CDA schematic shown in Fig. 3-2 consists of five functional blocks: digital signal processing block, 1st order integrator, open-loop CDA, feedback network (R_1 and R_2) and load (low-pass filter and the loudspeaker).

As the CDA is essentially a switching mode amplifier, PSRR is one of its major drawbacks compared to their linear counterparts. The modelling of PSRR in analog PWM CDAs has been reported in [24]. Where, three important parameters that affect PSRR are the integrator gain, PWM stage gain and the feedback factor. Interestingly, the PSRR of PIPO CDAs remain unreported. We will now derive this PSRR.

Fig. 3-4 (a) depicts the block diagram model of the PIPO CDA depicted earlier in Fig. 3-2, where G_1 is the transfer function of the pre-processing block, G_{int} represents the transfer function of the 1st-order integrator, H_1 is the feedback factor and N_D is the added noise due to the supply noise N_S .

Figure 3-4: Block diagram of the (a) the PIPO CDA, and
(b) equivalent gain model of the PWM modulator

To derive the PSRR of the PIPO CDA, we first derive the expression of the added noise N_D according the supply noise N_S .

$$N_S = N \cos(2\pi f_n t) \quad (3.18)$$

$$N_D = 0.5N \cos(2\pi f_n t) + 0.25MN \cos(2\pi f_{in} t \pm 2\pi f_n t) \quad (3.19)$$

where M is the modulation index of the input signal,

f_n is the supply noise frequency, and

f_{in} is the input frequency.

The first term in Eqn. (3.19) is the output distortion due to supply noise at f_n , and the second term is the intermodulation distortion at $f_{in} \pm f_n$.

Secondly, we ascertain the equivalent gain of the PWM modulation, G_{PWM} , which equals to the ratio of supply voltage V_{DD} and carrier signal $V_{Carrier}$:

$$G_{PWM} = \frac{V_{DD}}{V_{Carrier}} \quad (3.20)$$

Fig. 3-4b depicts the equivalent gain model of the PWM modulator, where $V_{Carrier}$ is the equivalent carrier signal of the PWM modulator, and its maximum signal swing V_{C_Max} can be derived from the current analysis within a half switching cycle $T/2$:

$$I = C_1 \frac{dV_{Carrier}}{dt} = \frac{V_{DD}}{2R_1} \quad (3.21)$$

$$\Rightarrow V_{Carrier} \left(\frac{T}{2} \right) - V_{Carrier}(0) = \frac{V_{DD}}{2C_1R_1} \cdot \frac{T}{2} \quad (3.22)$$

$$\Rightarrow V_{C_Max} = \frac{V_{DD}}{4R_1C_1f_c} \quad (3.23)$$

where f_c is the switching frequency for input PWM signal.

The ensuing PWM gain G_{PWM} of the equivalent model can be easily derived as:

$$G_{PWM} = \frac{V_{DD}}{V_{C_{Max}}} = 4R_1C_1f_c \quad (3.24)$$

The integrator gain G_{int} , input digital signal processing block gain, G_1 and the feedback factor H_1 of the feedback network can be easily derived respectively as:

$$G_{int} = \frac{V_{int}}{V_{M1}} = -\frac{1}{sC_1 \left(\frac{R_1}{R_2} \right)} \quad (3.25)$$

$$G_1 = \frac{R_2}{R_1 + R_2} \quad (3.26)$$

$$H_1 = \frac{R_1}{R_1 + R_2} \quad (3.27)$$

The complete linear model can be obtained by substituting Eqns. (3.15 - 3.18) into the block diagram in Fig. 3-4(a). The system transfer function V_{out}/V_{in} and the noise transfer function V_{out}/N_D can then be derived on the basis of negative feedback analysis, i.e.,

$$\left. \frac{V_{out}}{V_{in}} \right|_{N_S=0} = \frac{G_1 G_{int} G_{PWM}}{1 + G_1 |G_{int}| G_{PWM} H_1} \quad (3.28)$$

$$\left. \frac{V_{out}}{N_s} \right|_{V_{in}=0} = \frac{1}{1 + G_1 |G_{int}| G_{PWM} H_1} * \frac{N_D}{N_s} \quad (3.29)$$

According to Eqns. (3.25 - 3.28), the attenuation of the supply noise, N_s , (i.e., by PSRR) can then be derived as:

$$\begin{aligned} \text{PSRR} &= 20 \log \left(\left. \frac{V_{out}}{N_s} \right|_{V_{in}=0} \right) = 6 + 20 \log(2 |G_{int}| H_1 G_{PWM}) \\ &= 6 + 20 \log \left(\frac{4 R_1 f_c}{R_2 s} \right) \end{aligned} \quad (3.30)$$

Eqn. (3.30) is particularly interesting. Surprisingly, it can be seen from Eqn. (3.30) that the PSRR of the PIPO CDA is independent of C_1 and is largely determined by the carrier frequency f_c . It is somewhat unexpected as the PSRR of conventional CDAs is largely dependent on the integrator gain, hence dependent on the capacitor value therein. It can be seen from Eqn. (3.30) that the imperative parameters affecting the PSRR are R_1/R_2 and f_c .

Intuitively, R_1/R_2 , the closed-loop gain k of the amplifier, should be designed to be as large as possible, and f_c as high as possible. However, these ‘intuitive’ design decisions would incur undesirable penalties – a R_1/R_2 larger than one would reduce the dynamic range of the CDA, hence reduced maximum output power. Conversely, a very high f_c would require the digital signal processing circuit to operate at an even higher clock rate, hence increasing the overall system power dissipation. In view of

said potential penalties, we will now discuss the design of a practical PIPO CDA and the considerations thereto in the following section.

3.3. Design and Verification of a PIPO CDA

On the basis of our derived distortion and the PSRR of PIPO CDAs, we will now delineate the design of a (practical) PIPO CDA.

The first practical design consideration is the need for the closed-loop gain, $k=R_2/R_1$, of the amplifier to be greater than 1. In view of the PSRR of the PIPO CDA derived in Eqn. (3.30), which is inversely proportional to k , a good compromise is that k equals to 2.

Furthermore, signal-clipping at the integrator output should be avoided in the case of maximum signal swing, for example, when the modulation index $M = 0.9$. In this case, according to Fig. 3-3, the instantaneous switching output voltage of the integrator V_1 should still be smaller than the supply rail voltage V_{DD} . The expression of V_1 in terms of closed-loop gain k , modulation index M , time constant τ and switching period T can be derived according to the analysis in Section 3.2.1. Specifically,

$$V_1 = V_{DD} \frac{(k+1)}{\tau} t_2 = \frac{(k+1)V_{DD}}{\tau} \left(-\frac{kTM}{4} + \frac{T(1+M)}{4} - \frac{T}{4k} \right) \quad (3.31)$$

Based on the expression of V_1 , with $k = 2$, we have the following inequality:

$$V_1 = \frac{3V_{DD}}{\tau} \left(-\frac{2Tm}{4} + \frac{T(1+M)}{4} - \frac{T}{8} \right) < V_{DD} \quad (3.32)$$

For $M = 0.45$ (with $k = 2$, the modulation index of the output signal is at 0.9 and is inverted), we can derive the following design requirement for time constant τ :

$$\tau > 0.7125T \quad (3.33)$$

On this basis, a practical design involves a design whose switching frequency $f_c = 200$ kHz (10 times of the maximum audio frequency 20 kHz) where the carrier signal period $T = 5\mu s$. Further, we design $R_2 = 200$ k Ω (hence $R_1 = 100$ k Ω) and $C_2 = 20$ pF can satisfy Eqn. (3,33), to avoid signal clipping. Note that the values of the RC components are practical for the 65 nm CMOS process without excessive IC area.

For completeness, note that the switching frequency of the PWM signal is a low 200 kHz, and it is much lower than typical clocking frequency [103] of the preceding digital processing circuits.

3.4. Simulation Results

In this section, we verify our derivations of the THD and PSRR by comparing our theoretical derivations against simulations for a conventional CDA and our designed PIPO CDA.

A commercial 65 nm CMOS process is adopted for the design and simulations of the PIPO CDA. A supply voltage of 3.6V and a resistive loudspeaker load of 8Ω are used, unless specified otherwise. For ascertaining the PSRR, a noise signal, $V_{ripple} = 200 \text{ mV}_{pp}$, is injected to the 3.6V supply voltage.

Fig. 3-5 depicts the THD (%) versus the modulation index, M , for the PIPO CDA. For comparison, the THD of a conventional single-feedback 1st-order integrator PWM CDA is also depicted therein. For fair comparison, this conventional CDA embodies the same integrator and output stage as the PIPO CDA.

It can be seen from Fig. 3-5 that the THD of the PIPO CDA is relatively independent of the modulation index and the THD is a low $\sim 0.01\%$. Based on our earlier analysis earlier, this THD is largely caused by the non-idealities of the output stage (with a $>5 \text{ ns}$ dead-time and approximately $150 \text{ m}\Omega$ on-resistance). On the other hand, the conventional CDA suffers from a worse THD (almost 4 times larger) and is dependent on the signal level where the THD is expected more pronounced at low modulation indexes.

Figure 3-5: THD (%) versus modulation index for
a PIPO CDA and a conventional CDA

Fig. 3-6 depicts the PSRR (dB) of the PIPO CDA versus the supply noise frequency f_n (Hz) obtained both from simulations and analytically from Eqn. (3.16). The PSRR of the same abovementioned conventional CDA is also plotted therein.

It can be seen that the simulation results agree very well with our analytical results, hence corroborating the derived analytical equations. Furthermore, the PSRR of the PIPO CDA is advantageously at least 6 dB higher than the conventional CDA over a wide range of frequencies.

Figure 3-6: PSRR (dB) versus Supply noise frequency (Hz) for the PIPO CDA (both simulated and calculated) and a conventional CDA

3.5. Conclusions

The THD distortion and PSRR of PIPO CDAs have been analytically investigated. Based on our derived analytical expressions, a (practical) design using a commercial 65 nm CMOS process has been designed. On the basis of simulations, we have verified the validity of our derived analytical expressions. We have further shown that the PIPO CDA advantageously featured superior performance (THD and PSRR) compared to the conventional CDA that embodies the same integrator and output stage.

Chapter 4 Low-Power High-Efficiency

Filterless Bang-Bang

Class D Amplifier

This chapter is largely extracted from the author's publication [104], "A novel low-power high-efficiency 3-state filterless Bang-Bang class D amplifier" published in the proceedings of the IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2015.

4.1. Introduction

It was earlier reviewed that CDAs are increasingly ubiquitous over their linear counterparts due to their higher power-efficiency [105] where the modulation techniques commonly used in CDAs include the Pulse-Width-Modulation (PWM), Sigma-Delta Modulation [48], Bang-Bang control modulation [49], and Self-Oscillation [91]. Amongst these modulation techniques, Bang-Bang control CDAs are arguably the most advantageous for low-power power-critical applications. This is due to their significantly higher power-efficiency (in part due to their hardware simplicity), comparable fidelity (qualified by THD) and higher noise immunity (qualified by PSRR) when benchmarked against the PWM CDA with equal hardware.

We earlier explained in Chapter 1 and 2 that Bang-Bang CDAs hitherto remain filter-on designs, i.e., they required the bulky extended LC filter. To this end, in this chapter, we propose, to the best of our knowledge, the first-ever 3-state Bang-Bang control filterless CDA applicable to regular-power and ultra-low-power applications. Compared to other filterless 3-state CDAs, the proposed filterless 3-state Bang-Bang control CDA features the simplest hardware and highest power-efficiency, but with somewhat compromised fidelity. Nevertheless, the fidelity is sufficient for typical ultra-low-power applications such as low-to-mid performance wearable devices.

This chapter is organized as follows. In Section 4.2, the single-ended and 2-state Bang-Bang control CDAs are reviewed, and our proposed 3-state filterless CDA is delineated in Section 4.3. The analysis and benchmarking of our CDA are given in Section 4.4, and the conclusions drawn in Section 4.5.

4.2. Conventional Bang-Bang control CDA

The schematics of the conventional single-ended CDA [3] and 2-state BTL Bang-Bang control CDAs [24] are depicted in Fig. 4-1(a) and (c), respectively. Their respective waveforms are depicted in Fig. 4-1(b) and (d). Each CDA comprises a Bang-Bang controller (realized by a hysteresis comparator), an output stage, a RC feedback network, a lowpass filter and a loudspeaker load (modelled resistively).

The modus operandi of the two CDAs is similar. The RC feedback network feeds back the output signal. The Bang-Bang controller controls the error signal (V_{err})

between the input signal and the output signal (ideally a replica of the input signal for Gain=1), and generates the digital-like switching signal(s) by comparing the V_{err} with the hysteresis band. The output stage provides current to drive the loudspeaker load. The lowpass filter filters the high frequency switching components and recovers the desired output signal at the loudspeaker load.

It can be seen from Fig. 4-1(b) and (d) that the output switching signal of both CDAs is effectively ‘2-state’. Specifically, for the case of the single-ended CDA, the output switching signal, V_{SE} , alternates between the two supply rails (V_{DD} and 0). On the other hand, for the 2-state BTL CDA, the output switching signal, V_{2State_p} - V_{2State_n} , alternates between V_{DD} and $-V_{DD}$ as the two output signals (V_{2State_p} and V_{2State_n}) are always 180° out of phase. It is well established [106] that in 2-state output signals, the carrier components are large, and hence an output lowpass LC filter is required to filter these components.

(a)

(b)

(c)

(d)

Figure 4-1: (a) Single-ended Bang-Bang CDA, and (b) its waveforms;
(c) 2-state BTL Bang-Bang CDA, and (d) its waveforms

4.3. Proposed 3-state Filterless Bang-Bang Control CDA

The schematics of the proposed 3-state filterless Bang-Bang control CDA and its waveforms are depicted in Fig. 4-2. It comprises a Bang-Bang controller (comprising two comparators and 4 feedback resistors, R_{h11} , R_{h21} , R_{h12} and R_{h22}), two output stages, a synchronization block (R_{h31} and R_{h32}), a feedback network (R_{in1} , R_{in2} , R_{fb1} , R_{fb2} , C_{fb1} and C_{fb2}) and the loudspeaker load.

In the proposed CDA, the hysteresis (V_h) of the Bang-Bang controller is generated by the feedback resistors and the synchronization block. The synchronization block feeds back the signal of the opposing branch to the Bang-Bang controller, and synchronizes the carrier components of the two branches, thereby generating the 3-state output switching signal by comparing the error signal (V_{err1} and V_{err2}) with the hysteresis band (V_{h1}^- , V_{h1}^+ , V_{h2}^- , V_{h2}^+ ; on Fig. 4-3) of the two comparators. The nomenclatures V_{h1}^- and V_{h1}^+ are the hysteresis bands of comparator at the upper branch; V_{h1}^- is the lower limit and V_{h1}^+ is the upper limit; and V_{h2}^- and V_{h2}^+ are the hysteresis bands of comparator at the lower branch. The waveforms are presented in Fig. 4-3. For sake of completeness, it is worthwhile to note that in reported single-ended and 2-state BTL Bang-Bang control CDAs [38], there is no synchronization block.

Consequent to the function of the synchronization block, the high frequency carrier components of the two output signals, V_{out_p} and V_{out_n} , are in-phase whilst the low

frequency audio components are out of phase. Put simply, the resultant output switching signal is 3-state (see Fig. 4-2(b)).

(a)

(b)

Figure 4-2: (a) The proposed 3-state filterless Bang-Bang control CDA,
and (b) its waveforms

Figure 4-3: Waveforms of Bang-Bang controller upper branch

On the basis of Fig. 4-2(a) and a reported derived analytical methodology [61], the ‘on’ and ‘off’ period, t_{on} and t_{off} , can be derived; t_{on} is the period when $V_M = V_{DD}$ and t_{off} is the period when $V_M = -V_{DD}$. By straight forward analysis, we can show that t_{on1} and t_{off1} respectively, the ‘on’ and ‘off’ periods for the upper branch shown in Fig. 4-3, can be derived as follows:

By application of Kirchhoff’s Current Law,

$$\frac{V_{in} - V_{err1}}{R_{in1}} + \frac{V_{out_p} - V_{err1}}{R_{fb1}} = C_{fb1} \frac{dV_{err1}}{dt} \quad (4.1)$$

By re-arranging and integration,

$$\int \frac{dt}{R_{e1}C_{fb1}} = \int \frac{dV_{err1}}{\frac{R_{in1}}{R_{in1} + R_{fb1}} V_{out_p} + \frac{R_{fb1}}{R_{in1} + R_{fb1}} V_{in} - V_{err1}} \quad (4.2)$$

where $R_{e1} = R_{in1} // R_{fb1}$ is the equivalent resistance of R_{in1} and R_{fb1} in parallel.

Hence,

$$e^{-\frac{t}{R_{e1}C_{fb1}}} * const = mV_{outp} + (1 - m)V_{in} - V_{err1} \quad (4.3)$$

where $m = \frac{R_{in1}}{R_{in1} + R_{fb1}}$ is the resistance ratio.

During $t_1 \rightarrow t_2$, which is the ‘on’ period t_{on1} based on the waveform in Fig. 4-3, the error signal V_{err1} can be derived as follows:

At $t = t_1$,

$$V_{err1} = V_{h1}^-$$

At $t = t_2$,

$$V_{err1} = V_{h1}^+$$

Hence, $const$ in Eqn. (4.3) and t_{on1} and t_{off1} can be derived:

$$const = mV_{DD} + (1 - m)V_{in} - V_{h1}^- \quad (4.4)$$

$$t_{on1} = R_{e1}C_{fb1} \ln \left[\frac{mV_{DD} + (1 - m)V_{in} - V_{h1}^-}{mV_{DD} + (1 - m)V_{in} - V_{h1}^+} \right] \quad (4.5)$$

$$t_{off1} = R_{e1}C_{fb1} \ln \left[\frac{mV_{DD} - (1 - m)V_{in} + V_{h1}^+}{mV_{DD} - (1 - m)V_{in} + V_{h1}^-} \right] \quad (4.6)$$

Similarly, t_{on2} and t_{off2} , the ‘on’ and ‘off’ period of the lower branch, can be derived as:

$$t_{on2} = R_{e2}C_{fb2} \ln \left[\frac{mV_{DD} + (1 - m)V_{ip} - V_{h2}^-}{mV_{DD} + (1 - m)V_{ip} - V_{h2}^+} \right] \quad (4.7)$$

$$t_{off2} = R_{e2}C_{fb2} \ln \left[\frac{mV_{DD} - (1 - m)V_{ip} + V_{h2}^+}{mV_{DD} - (1 - m)V_{ip} + V_{h2}^-} \right] \quad (4.8)$$

Where $R_{e2} = R_{in2} // R_{fb2}$,

$$V_{h1}^+ = \frac{R_{h11}}{R_{h11} + R_{h21}} V_{DD} + \frac{R_{h11}}{R_{h11} + R_{h31}} V_{M2} \quad (4.9)$$

$$V_{h1}^{-} = -\frac{R_{h11}}{R_{h11} + R_{h21}}V_{DD} + \frac{R_{h11}}{R_{h11} + R_{h31}}V_{M2} \quad (4.10)$$

$$V_{h2}^{+} = \frac{R_{h12}}{R_{h12} + R_{h22}}V_{DD} + \frac{R_{h12}}{R_{h12} + R_{h32}}V_{M1} \quad (4.11)$$

$$V_{h2}^{-} = -\frac{R_{h12}}{R_{h12} + R_{h22}}V_{DD} + \frac{R_{h12}}{R_{h12} + R_{h32}}V_{M1} \quad (4.12)$$

From Eqn. (4.9) – (4.12), it can be noted that the hysteresis band of the Bang-Bang controller is determined by the feedback resistors and the synchronization block. The synchronization block synchronizes the high frequency carrier components by feeding back the signal of the opposing branch to the Bang-Bang controller. Hence, this feedback mechanism forces the synchronization of the signals at the two branches.

Based on the Eqn. (4.5) – (4.8) and by using Taylor Series, when the input signal is 0, the idle switching frequency, f_{sw} can be easily derived as:

$$f_{sw} = \frac{mV_{DD}}{2R_e C_{fb} V_h} \quad (4.13)$$

where R_e and C_{fb} are the designed values of R_{e1} (or R_{e2}), C_{fb1} (or C_{fb2}), respectively. V_h is the average value of V_{h1}^{+} and V_{h2}^{+} (or $-V_{h1}^{-}$ and $-V_{h2}^{-}$).

4.4. Result and verification

The proposed filterless 3-state Bang-Bang control CDA is simulated using Cadence based on a commercial 65nm CMOS process. The circuit parameters of the designed 3-state Bang-Bang CDAs for four cases of feedback and synchronization block designs are tabulated in Table I – the intention here is to ascertain the important parameters thereto. The input frequency f_{in} is 2 kHz and supply voltage V_{DD} is 3.6V.

Table I: Circuit Parameters of the designed 3-State Bang-Bang CDA

Parameters	Values			
	Case 1	Case 2	Case3	Case4
R_{h11}, R_{h12}	500 Ω	1 k Ω	500 Ω	1 k Ω
R_{h21}, R_{h22}	100 k Ω	100 k Ω	100 k Ω	100 k Ω
R_{h31}, R_{h32}	300 k Ω	300 k Ω	300 k Ω	300 k Ω
$R_{in1}, R_{in2}, R_{fb1}, R_{fb2}$	120 k Ω	120 k Ω	120 k Ω	120 k Ω
C_{fb1}, C_{fb2}	100 pF	100 pF	300 pF	300 pF
R_{load}	8 Ω (for all cases)			

Fig. 4-4 depicts the waveform of the output signal (for Case 1, $m=0.7$) expected, the output is that of a filterless 3-state Bang-Bang control CDA.

Figure 4-4: Output signal waveform $V_{out_p} - V_{out_n}$

Fig. 4-5 depicts the THD versus the modulation index, M , for the four cases of circuit parameters tabulated in Table I. It can be seen from Fig. 4-5 that unlike the conventional PWM and Sigma-Delta CDAs, the THD of the proposed filterless Bang-Bang CDAs increases with decreasing M . The comparison between Case 1 and Case 2 (or Case 3 and Case 4) shows that a lower hysteresis band results a lower THD. The comparison between Case 1 and Case 3 (or Case 2 and Case 4) shows that a smaller value of C_{fb1} and C_{fb2} results in reduced THD. This is somewhat expected, because with a lower hysteresis band and a smaller value of C_{fb1} and C_{fb2} , the Bang-Bang control CDA switches at a higher frequency (refer to Eqn. (4.13)), but at the cost of higher switching power loss at the output stage.

Figure 4-5: THD versus modulation index M

Although the THD is somewhat compromised in all four cases – the best being Case 1, this THD is usually sufficient for a number of low-power power-critical applications. For example, as the signal-to-noise ratio/dynamic range of the sub-miniature loudspeaker in many wearable devices is $\leq 40\text{dB}$, a THD of $\sim 1\%$ is generally acceptable – particularly in view of the much-desired hardware simplicity (and accompanying high power-efficiency as depicted in the power-efficiency vs modulation index plot shown in Fig. 4-6 below). The output power of Case 1 at full modulation index is about 1.54 watts. The comparison for this work with state-of-the-art filterless CDAs are given in Table II.

Figure 4-6: Power-efficiency plot against modulation index M for Case 1

Table II: Benchmark of the state-of-the-art filterless CDAs

	This Work	[21]	[98]	[99]	[19]
VDD	3.6V	3.6V	5.5V	3.6V	3.7V
Min THD+N	0.2%	0.0027%	0.1%	0.2%	0.018%
Max Power Efficiency	95%	94%	90%	79%	85.5%
Process	65nm	65nm	250nm	500nm	180nm

4.5. Conclusions

We have proposed, to the best of our knowledge, the first-ever filterless 3-state Bang-Bang control CDA where the output lowpass filter is not required. The proposed 3-state Bang-Bang control CDA featured the simplest hardware (and high power-efficiency of ~95%), but with somewhat compromised fidelity. Nevertheless, the fidelity is sufficient for typical low-power power-critical applications such as wearable devices.

Chapter 5 Analysis and Design of Class D

Amplifiers for Supply Modulators

A large part of this chapter is extracted from the author's publication [107], "A 2.5W 40MHz-Bandwidth Hybrid Supply Modulator with 91% Peak Efficiency, 3V Output Swing and 4mV Output Ripple at 3.6V Supply" published in the IEEE Transactions on Power Electronics, 2019. The author's role is the analysis and design of the CDA within the supply modulator and a collaboration on the system architecture of this supply modulator. The part of Class AB amplifier is the work of another Ph.D. candidate. Of particular note, in this Chapter, an extended description of the Class D output stage is provided in Section 5.3.4, i.e., this section is not provided in our publication [107].

5.1. Introduction

Short battery lifespan is one of the challenges of mobile communication devices and is exacerbated with the demand for ever-increasing speed and data. This is in part due to the adopted communication protocols, e.g. LTE and LTE-A, that employ spectrally efficient modulation schemes and wide bandwidth. These advanced communication protocols impose stringent requirements on the linearity of the Radio Frequency (RF) Power Amplifier (PA), yet requiring high Peak-to-Average-Power-Ratio [64] – translating to low power-efficiency in conventional RF PAs [65], hence reduced battery-life.

Of the various reported methods to improve the power-efficiency of RF PAs, the Envelope Tracking (ET) has been reported to be one of the most effective means [5, 66-85]. The supply modulator in the ET PA is essentially a power management circuit for the RF PA. The mechanism thereto is the supply modulator constantly providing a dynamically changing supply to the RF PA based on the time-varying envelope of the RF signals. In this fashion, the RF PA is kept nearly always in compression, where its power-efficiency is high, hence avoiding operation in the back-off condition.

Many supply modulators in ET PAs employ a hybrid topology (Class AB amplifier-cum-CDA) [5, 66-68, 70, 72-74, 78-83]. This is because the hybrid topology features higher power-efficiency compared to the Class AB amplifier-only topology [75], higher bandwidth and lower output ripple compared to the CDA-only topology [69, 71, 76, 77, 84, 85]. Nevertheless, at this juncture, the major shortcoming of the state-of-the-art supply modulators [5, 66-74, 76-85] is their limited bandwidth of $\leq 20\text{MHz}$, which is insufficient for LTE-A applications whose bandwidth is 40MHz-100MHz. Another shortcoming is the low output power. For instance, the reported designs in [67, 78, 79] operate at a low supply voltage of 1.2V supply, hence resulting a low output voltage of $<1\text{V}$ and low maximum output power of $<0.2\text{W}$. This low output power is, however, generally unacceptable for the recent communication protocols including LTE and LTE-A. The typical output power of an LTE/LTE-A RF PA is $\sim 27\text{dBm}$ (0.5W) taking into account the duplexer and antenna losses. Hence, the output power of the supply modulator would need to be $>1\text{W}$ for the III/V-based RF PA (with $\sim 45\%$ power-efficiency) and $>2\text{W}$ for CMOS-based RF PA (with $\sim 25\%$ power-efficiency). The limited bandwidth and/or

output power is in part due to the inevitable trade-off between bandwidth, output power, output noise and power-efficiency.

In this paper, we propose a supply modulator for ET PAs to provide wide bandwidth and sufficient output power for 40MHz LTE-A protocols, yet with high power-efficiency, high output voltage swing and low ripple noise. We achieve this by the following. First, we investigate the power dissipation and optimization method of the supply modulator for wideband applications taking into consideration the effect of the propagation delay (a previously unexploited but imperative parameter).

We show that the threshold current is unnecessary – in fact a controller with zero threshold current results not only high bandwidth but also high power-efficiency for wideband supply modulators. Second, based on the first, we propose a delay-based hysteresis controller for the supply modulator. The proposed controller embodies a novel high-speed current comparator to compare the ripple current with zero current, instead of the conventional approach [5, 67, 72, 82] embodying a hysteresis comparator with a threshold current. By this means, higher power-efficiency and simpler hardware are achieved. Third, a wideband Class AB amplifier with an accurate quiescent current control and sufficient driving capability is proposed.

Collectively, the proposed supply modulator features the highest bandwidth (40MHz), yet with high output power (2.5W), high peak efficiency (91%), high output voltage swing (3V) and low output noise (4mV_{rms}) at 3.6V supply, compared to the reported designs [5, 66-85]. When the prototype supply modulator is embodied in an ET PA for tracking 20MHz LTE envelope signals, the ET PA

achieves a high power-efficiency of 41.4% at peak output power of 28.5dBm and 34.4% at 3dB backoff – a significant >1.6x improvement over the RF PA without the supply modulator. The prototype supply modulator is fabricated in a commercial 180nm CMOS process.

5.2. Optimization of the Supply Modulator for Wideband Applications

Fig. 5-1 depicts the block diagram of a supply modulator, comprising a wideband Class AB amplifier, a high-efficiency CDA and a hysteresis controller. The inductor, L_O , filters out the high frequency component from the output of the preceding CDA. The supply modulator provides a variable power supply to the RF PA. The output current, i_O , of the supply modulator is the sum of the output current, i_{AB} , of the Class AB amplifier and the output current, i_D , of the CDA, i.e., $i_O = i_{AB} + i_D$.

Figure 5-1: Block diagram of an ET PA with a hybrid supply modulator

Fig. 5-2 depicts the simulated frequency response of i_{AB} and i_D , where the DC voltage of the input signal is 1.8V and the AC amplitude is 1.4V_{pp}. In the low-frequency range (<5MHz), i_D is much higher than i_{AB} , and both i_D and i_{AB} remain largely unchanged. In this frequency range, i_D provides most of the output current whilst i_{AB} provides the ripple current due to switching of the CDA; see Fig. 5-3(a). In the high-frequency range (>5MHz), i_{AB} increases with the frequency whilst i_D reduces with the frequency. This is because in the high-frequency range, the CDA is unable to provide sufficient high-frequency current and the Class AB amplifier needs to provide not only the ripple current (due to the switching of the CDA) but also the high-frequency components of the output signal; see Fig. 5-3(b).

Figure 5-2: Simulated frequency response of i_{AB} and i_D

(a)

(b)

Figure 5-3: Typical current waveforms of the supply modulator tracking

(a) low-frequency input signals, and (b) high-frequency input signals

The hysteresis controller controls i_D by means of sensing i_{AB} and comparing i_{AB} against the hysteresis current of the controller, shown in Fig. 5-1. Conventionally [67, 72], it is assumed that the threshold currents, $\pm I_T$, of the hysteresis comparator

are the actual upper limit, I_U , and lower limit, I_L , of the hysteresis current, and the effect of the propagation delay, t_D , is ignored. However, this is only true for narrowband applications (i.e., low-frequency signals, such as EDGE, CDMA envelope signals) whose switching frequency is low (hence the switching period is much longer than t_D). We will now show that due to t_D , this is not the case of the supply modulator for wideband applications (i.e., high-frequency signals, such as LTE, LTE-A envelope signals). The optimization of the supply modulator for wideband applications, taking into consideration t_D , will be delineated thereafter.

5.2.1. Effect of Threshold Current and Propagation Delay on Hysteresis

The threshold currents of the hysteresis comparator, $\pm I_T$, are ideally the upper and lower limits of the hysteresis current of the supply modulator. However, due to t_D , the actual upper and lower limits of hysteresis current are conversely I_U and I_L , shown in Figs. 3(a) and 3(b). Based on Figs. 5-1, 5-3(a) and 5-3(b), I_U and I_L are derived as Eqns. (5.1a) and (5.1b) respectively, which are a reasonable approximation of I_U and I_L for both narrowband applications and wideband applications.

$$I_U = +I_T + \frac{V_{DD} - v_O}{L_O} \times t_D \quad (5.1a)$$

$$I_L = -I_T - \frac{v_O}{L_O} \times t_D \quad (5.1b)$$

where v_O is output voltage,
 V_{DD} is the supply, and
 L_O is the external inductor in Fig. 5-1.

We define the hysteresis current I_{HYS} as the difference between the upper and lower limits, i.e., $I_{HYS} = I_U - I_L$. It is straightforward to derive I_{HYS} as expressed in Eqn. (5.2a). I_{HYS} comprises two times of the threshold current, $2I_T$, of the hysteresis comparator, and the intrinsic hysteresis, I_{HYS_int} , expressed in Eqn. (5.2b). I_{HYS_int} arises from the propagation delay, t_D , and also is affected by the external inductor, L_O , and supply voltage, V_{DD} .

$$I_{HYS} = I_U - I_L = 2I_T + I_{HYS_int} \quad (5.2a)$$

$$\text{where } I_{HYS_int} = V_{DD} \times \frac{t_D}{L_O} \quad (5.2b)$$

In the reported supply modulator designs [72, 75], I_{HYS_int} is typically assumed to be negligible, i.e., $I_{HYS} = 2I_T$. This is true for supply modulators with narrow bandwidth whose switching frequency is low, but it is not the case for wideband supply modulators.

Compared to the supply modulator optimized for narrowband applications, smaller L_O is normally used for wideband applications. This is because in wideband supply modulators, the switching frequency of the CDA is normally designed to be high ($>10\text{MHz}$) [68, 70, 72, 75, 78, 79] to extend the bandwidth of the CDA and to reduce the current burden of the power-inefficient Class AB amplifier, hence featuring high power-efficiency. This high switching frequency is facilitated by employing a relatively small external inductor L_O [72], e.g. $1\mu\text{H}$ in our design (see subsection 5.2.2 for the optimization of the external inductor).

On the other hand, t_D in Eqn. (5.2b) is relatively long in supply modulators with high output power ($>1\text{W}$) because t_D from the output stage of the CDA is relatively long for the following reasons. First, to provide high output power, $V_{DD} > 3\text{V}$ is typically adopted in the supply modulators [5, 66, 68-77, 80-85]. Consequently, to prevent simultaneously turning on both the high-side and low-side power transistors in the Class D output stage (i.e., to reduce the short-circuit current), an anti-shoot-driver with a relatively long dead time (several ns) [5, 21, 72, 82] is generally employed. Second, the size of the power transistors in the output stage of the CDA is large to realize small output impedance, hence low conduction loss. These large power transistors have relatively large parasitic capacitance, which undesirably results in a long propagation delay [21, 40].

Put simply, as evident in Eqn. (5.2b), L_O is relatively small and t_D is relatively long for wideband supply modulators with high output power, resulting in an undesirably high I_{HYS_int} , vis-à-vis I_{HYS_int} assumed to be negligible. I_T is generally several mA to several tens of mA [72, 75, 78]. As a case in point, in our proposed supply

modulator (see Fig. 5-5 later), with $t_D = 7\text{ns}$, $L_O = 1\mu\text{H}$, and $V_{DD} = 3.6\text{V}$, the intrinsic hysteresis I_{HYS_int} is 25mA. Hence, the delay in wideband supply modulators has a significant (not-negligible) effect on the hysteresis current.

5.2.2. Optimization of Hysteresis and External Inductor

We will now describe the design tradeoffs and optimization means that takes into account the propagation delay t_D .

The power dissipation of the supply modulator comprises three parts – P_{loss_AB} due to the Class AB amplifier, P_{loss_D} due to the CDA, and P_{loss_Ind} due to the external inductor.

P_{loss_AB} is different for narrowband and wideband applications. For narrowband applications, the CDA can follow the signals closely (refer to Fig. 5-3(a)), and the Class AB amplifier provides ripple current swinging between I_U and I_L . P_{loss_AB} , expressed in Eqn. (5.3), is mainly due to the ripple current and the quiescent current. In this case, the switching frequency f_{sw} can be estimated by Eqn. (5.4). Due to the trade-off between f_{sw} and I_{HYS} (i.e., the trade-off between the switching loss of the CDA and the ripple current of the Class AB amplifier), f_{sw} and I_{HYS} can be optimized [4], [9].

$$P_{loss_AB} = \frac{1}{4} I_{HYS} V_{DD} + I_Q V_{DD} \quad (5.3)$$

$$f_{sw} \approx \frac{(\alpha - \alpha^2) V_{DD}}{L_O I_{HYS}} \quad (5.4)$$

where I_Q is the quiescent current of the Class AB amplifier, and $\alpha = v_O/V_{DD}$ is the ratio of the output voltage over the supply.

For wideband applications, the optimization method is different from the case for narrowband envelope signals. In this case, the switching frequency reduces and depends on the input frequency only as observed in Fig. 5-3(b). In other words, f_{sw} is independent of I_{HYS} and fixed for a specific envelope signal; and P_{loss_D} is relatively small. P_{loss_AB} in this case is determined by (i) the bandwidth of the CDA, (ii) the delay between the CDA and the Class AB amplifier, and (iii) the quiescent power loss of the Class AB amplifier. For (i), the current swing (peak-to-peak value) of i_D in Fig. 5-3(b) is determined by L_O . A small L_O is preferred to achieve a large bandwidth of CDA; hence more AC current will be delivered by the power-efficient CDA and less current is needed from the Class AB amplifier. For (ii), the delay between the CDA and the Class AB amplifier increases the distortion at the output of the CDA, hence resulting in increased current flow in the Class AB amplifier to compensate for the distortion. Therefore, to reduce the power dissipation, the delay should be as low as possible. The delay of the CDA is contributed by I_{HYS} , and it includes the delay due to the Class D output stage, t_D , and the threshold currents of

hysteresis comparator, $\pm I_T$. In view of this, $I_T=0$ is recommended, consequently reducing I_{HYS} to I_{HYS_int} . For (iii), by reducing the current burden of the Class AB amplifier, the Class AB amplifier can be designed with a small quiescent current I_Q and wider bandwidth, hence further improving the power-efficiency and extending the bandwidth of the supply modulator.

P_{loss_D} , expressed in Eqn. (5.5), consists of the switching loss and conduction loss, which are due to the parasitic capacitance, C_{eq} , and the parasitic resistance, R_{eq} , of the drivers and power transistors, respectively.

$$P_{loss_D} = f_{sw} C_{eq} V_{DD}^2 + R_{eq} i_o^2 \quad (5.5)$$

P_{loss_Ind} , expressed in Eqn. (5.6), is due to the parasitic resistance, R_L , of the inductor. The power-efficiency optimization of the supply modulator involves the trade-offs for selecting external inductor L_O – a small L_O is preferred for wide bandwidth of the CDA and a large L_O is preferred to reduce I_{HYS_int} (as expressed in Eqn. (5.2b)). In addition, the parasitic resistance of L_O contributes P_{loss_Ind} (expressed in Eqn. (5.6)), and a small L_O is preferred for its relatively small parasitic resistance.

$$P_{loss_Ind} = R_L i_o^2 \quad (5.6)$$

In this work, our design (see Fig. 5-5 later) is optimized for tracking wideband envelope signals, particularly for tracking 40MHz LTE-A envelope signals. The

optimization procedure is delineated now. First, we begin the design with the estimation of the overall performance based on our experience and the optimization presented above. Specifically, for 40MHz LTE-A envelope signals, we recommend that the average switching frequency of the supply modulator is ~20MHz, and the bandwidth of the Class AB amplifier is >200MHz with >200mA driving capability. Second, the design is simulated for tracking dynamic envelope signals extracted from 40MHz LTE-A RF signals (1.2W output power) with various inductors. The parasitic resistance of the external inductor is approximated by $R_L \approx 0.05\Omega + 0.01\Omega/\mu\text{H} * L_O$ – this is typical for commercial surface mount inductors with sufficient current rating. Third, based on the simulation results, the power losses P_{loss_D} , P_{loss_AB} , and P_{loss_Ind} can be ascertained and the inductor can be selected to achieve the minimum total power loss. As explained earlier, the supply modulator involves many tradeoffs between P_{loss_D} , P_{loss_AB} , and P_{loss_Ind} , several iterations may be conducted to optimize the design of the supply modulator. Following the optimization procedure, Fig. 5-4 shows the simulated power-efficiency for tracking 40MHz LTE-A envelope signals (1.2W output power) with various inductors. As shown in Fig. 5-4, the maximum power-efficiency of ~86.5% is achieved with 1 μ H inductor. Considering all the abovementioned trade-offs, L_O is chosen to be 1 μ H.

Figure 5-4: Simulated power-efficiency with various external inductors

In short, for wideband supply modulators, I_{HYS} is primarily bounded by the intrinsic hysteresis, I_{HYS_int} , due to the propagation delay t_D – not the threshold current, I_T , of the hysteresis comparator as generally perceived. For wideband supply modulators, I_T is, in fact, unnecessary due to the propagation delay of the CDA. By reducing I_T , the output power of the Class AB amplifier is reduced, which in turn extends the bandwidth and improves the power-efficiency of the supply modulator. The external inductor, L_O , can be selected considering the trade-offs between the bandwidth of the CDA, the intrinsic hysteresis, I_{HYS_int} , and the parasitic resistance of the inductor, R_L , to optimize the power-efficiency of the wideband supply modulator.

5.3. Proposed Supply Modulator

5.3.1. System Architecture

We have shown in section 5.2 that to obtain maximum power-efficiency, I_T should be 0. In other words, the hysteresis comparator should be delay-based. We will now discuss the design of our supply modulator embodying a delay-based hysteresis controller.

The schematic diagram of the proposed supply modulator is depicted in Fig. 5-5, which embodies a delay-based hysteresis controller, a wideband Class AB amplifier, and a high-efficiency CDA. As the sensing transistors, M_{PS} and M_{NS} (top left of Fig. 5-5) of the delay-based hysteresis controller are designed to match the output power transistors of the Class AB amplifier, M_{PA} and M_{NA} (middle bottom of Fig. 5-5), i_{SEN} in the controller is a scaled version of i_{AB} . i_{SEN} is compared with zero current ($I_T = 0$) by means of the proposed current comparator (see sub-section B below). The output voltage of the controller, v_C , controls the output of the CDA, v_D , via the anti-shoot-through driver to prevent large shoot-through current. The power transistors, M_{PD} and M_{ND} , of the CDA are sized accordingly to obtain minimum switching loss and conduction loss [5, 67], thereby obtaining high power-efficiency. The external inductor, L_O , is chosen to be 1 μ H in view of our preceding discussions in section 5.2.2.

Figure 5-5: Schematic of the supply modulator embodying a proposed delay-based hysteresis controller, a proposed wideband Class AB amplifier, and a high power-efficiency CDA

With $I_T = 0$ in the proposed controller, the intrinsic hysteresis, I_{HYS_int} , arising from the propagation delay, t_D , determines I_U and I_L as given in Eqns. (5.1a) and (5.1b). The ensuing output of the CDA, v_D , will ‘on’ (i.e., $v_D = V_{DD}$) when $i_{SEN} > I_U$, and v_D will ‘off’ (i.e., $v_D = 0$) when $i_{SEN} < I_L$. By this means, the proposed supply modulator embodies a large-signal negative feedback loop. According to the large-signal stability criterion [78], the stability of the hybrid supply modulator is assured by controlling the ripple current from the CDA to be within the driving capability of the Class AB amplifier. This is different from the small-signal feedback loop (e.g. the feedback loop in the Class AB amplifier) whose location of its poles and zeros is critical to the stability. In other words, despite the hysteresis, I_{HYS} , depending on the propagation delay, t_D , which may vary with the process variations, the supply modulator with delay-based hysteresis controller is stable if the Class AB amplifier has sufficient output current.

By circumventing the need for the conventional hysteresis comparator, the propagation delay of the comparator is significantly reduced, thereby further improving the power-efficiency and the ensuing hardware is simplified. Furthermore, by adopting a current comparator instead of the more prevalent voltage comparator, wider bandwidth is facilitated.

5.3.2. Proposed High-speed Current Comparator in the Hysteresis Controller

The major issue of the conventional current-mode comparator embodied in the supply modulators, e.g. [67], is that the upper and low limits of i_{AB} , I_U and I_L , are both positive (i.e., $I_U > 0$ and $I_L > 0$ vis-à-vis $I_U > 0$ and $I_L < 0$ in our proposed design). In the supply modulators with a conventional current-mode comparator, the Class AB amplifier therein is designed to always provide positive current. This results in an undesirably larger portion of i_O sourced from the Class AB amplifier, which in turn reduces the power-efficiency [78].

To circumvent this, a proposed high-speed current comparator (top left of Fig. 5-5) is embodied in the proposed delay-based hysteresis controller. The current mirror, M_{PC1} and M_{PC2} , serves to compare the currents, i_{PC1} and i_{PC2} , flowing through these transistors. The output of the comparator, v_C , is ‘on’ (i.e., $v_C = V_{DD}$) when $i_{PC2} > i_{PC1}$, and vice versa. By appropriate matching, transistors $M_{NC3} \sim M_{NC6}$ are biased at I_{BIAS} , and the current flowing through M_{NC7} and M_{NC8} is i_{SEN} . Consequently, $i_{PC1} = I_{BIAS}$ and $i_{PC2} = i_{SEN} + I_{BIAS}$. Instead of comparing i_{SEN} and I_{BIAS} in the conventional designs [67], $(i_{SEN} + I_{BIAS})$ is conversely compared with I_{BIAS} in the proposed current comparator. Consequently, the reference current (i.e., I_T) in our proposed current comparator is zero. By eliminating the need for a positive reference current, the supply modulator would feature higher power-efficiency.

5.3.3. Proposed Class AB Amplifier

In the proposed supply modulator in Fig. 5-5, a three-stage Class AB amplifier featuring wide bandwidth and high output power embodies a proposed accurate quiescent current control is designed. For sake of illustration, the three stages of the Class AB amplifier, input, buffer, and output stages, are identified in Fig. 5-6(a), and the model of the three-stage Class AB amplifier is depicted in Fig. 5-6(b). The input stage features rail-to-rail input embodying the well-known constant- g_m technique, and embodies a folded-cascode amplifier to achieve stable and relatively high open-loop gain. The buffer stage embodies two source followers. The output stage is designed as a common-source amplifier to provide high current driving capability with rail-to-rail output swing.

(a)

Figure 5-6: The proposed wideband Class AB amplifier:

(a) simplified schematic, and (b) model

In the Class AB amplifier, the largest parasitic capacitances therein are the gate-source and gate-drain capacitances, C_{GS3} and C_{GD3} , of the power transistors, M_{PA} and M_{NA} , in the output stage. These large power transistors, occupying $\sim 50\%$ of the chip area of the Class AB amplifier, are designed for low open-loop output impedance and to provide high output current to track the high-frequency input signals. The poles and zeros due to these large parasitic capacitances are critical and are sensitive to process variations. Moreover, the slew rate and the output swing of the Class AB amplifier are primarily limited by the driving signals to these power transistors. To accommodate them, a buffer stage is embodied in the Class AB amplifier. The source followers in the buffer stage extend the bandwidth of the supply modulator by means of its small C_1 (input capacitance of the source follower) at the output of the input stage and a small R_2 (output impedance of the source follower) at the input of the output stage, shown in Fig. 5-6(b). This subsequently pushes the non-dominant poles due to parasitic capacitances, i.e., $1/R_1C_1$ and $1/R_2C_2$, to high frequencies. The driving signals, v_{PS} and v_{NS} , are the output of the buffer stage. This

is advantageous because the biasing current of the folded-cascode amplifier in the input stage can be designed freely without the limitation of the slew rate and the output swing, and the biasing current of the source followers is designed to be relatively large for high slewing.

Although the three-stage amplifier with a buffer stage has many advantages, this structure is not commonly used in the designs of Class AB amplifier. This is because the quiescent current of power transistors, M_{PA} and M_{NA} , in this structure are sensitive to process variations and supply. To address this issue, an accurate quiescent current control, M_{P3} - M_{P5} and M_{N3} - M_{N5} shown in the shaded area in Fig. 6(a), is proposed. Two translinear circuit loops are formed: (1) M_{P4} , M_{N4} , M_{P5} and M_{N5} (2) M_{PA} , M_{NA} , M_{P1} and M_{N1} . Through the current mirrors (M_{P2} and M_{P3} , M_{N2} and M_{N3}), the biasing current of transistors M_{P1} and M_{N1} in loop (2) is controlled by the current of transistors M_{N4} and M_{P4} in loop (1). Due to the abovementioned circuit loops, the quiescent current of M_{PA} and M_{NA} is determined by I_B in M_{P5} and M_{N5} . By appropriately matching the transistors, the quiescent current of M_{PA} and M_{NA} is set to be $r \times I_B$ (r is 250 in the design). To check the sensitivity of the quiescent current, corner simulations for our proposed design have been conducted, and the results are presented in Table III. The bolded values in red color and in blue color indicate the worst cases and the nominal values, respectively. We can clearly see that without the accurate quiescent current control, the conventional structure is sensitive – the variations of the quiescent current can be unacceptable 300% bigger. With the proposed accurate quiescent current control, the quiescent current is significantly improved – the variations are controlled within 20%.

Table III: Results of corner simulations for quiescent current

	Quiescent current (mA) without quiescent current control			Quiescent current (mA) with proposed quiescent current control		
	3.5V	3.6V	3.7V	3.5V	3.6V	3.7V
Supply						
typical	21.62	30.03	39.71	29.95	30.06	30.11
ss*	0.73	1.62	3.24	27.20	28.20	29.07
ff*	91.59	107.64	124.55	33.59	34.64	35.91
sf*	18.58	26.38	34.71	30.44	30.78	31.02
fs*	23.84	32.63	42.67	30.30	30.36	30.38

*ss=slow NMOS & slow PMOS; ff=fast NMOS & PMOS; sf=slow NMOS & fast PMOS; fs=fast NMOS & slow PMOS

The Class AB amplifier features high output swing, from 0.3V to 3.3V, and can drive 600mA at mid-rail, and 200mA at 0.3V and 3.3V. It also features a high slew rate of $\sim 250\text{V}/\mu\text{s}$. The simulated frequency response of the Class AB amplifier and its closed-loop output impedance are depicted in Figs. 5-7(a) and 5-7(b), respectively. It features a DC gain of 65dB, and GBW of $\sim 230\text{MHz}$ (with 64° phase margin and 6.5dB gain margin) for $6.7\Omega//100\text{pF}$ load. In the quiescent condition ($i_{AB} = 0$), the output impedance is small ($\sim 4\text{m}\Omega$) at frequencies below the dominant pole ($\sim 250\text{kHz}$), and the output impedance is $< 0.45\Omega$ at the maximum switching frequency of 35MHz. Under the worst-case operating conditions, i.e., the Class AB amplifier sourcing 200mA at 3.3V and sinking 200mA at 0.3V, the performance of the amplifier remains adequate. Specifically, when sourcing 200mA at 3.3V, the output impedance is $78\text{m}\Omega$ at low frequencies, and 1.08Ω at 35MHz; and when

sinking 200mA at 0.3V, the output impedance is $19\text{m}\Omega$ and 0.96Ω at low frequencies and at 35MHz, respectively.

(a)

(b)

Figure 5-7: Simulated results of the proposed Class AB amplifier:

(a) frequency response, and (b) closed-loop output impedance

5.3.4. Analysis of Class D Output Stage*

In view of the implementation of power-efficiency, we provide herein an extended investigation of the power dissipation mechanisms. The three main mechanisms of power loss are that due to parasitic capacitance, on-resistance and short circuit current. As describe in Chapter 2 earlier, a dead-time circuit is incorporated in the output stage to eliminate the short-circuit current. We will henceforth assure that the power due to short circuit current negligible.

Figure 5-8: The model of CDA output stage including driver and parasitics

* This section is an augmentation to our publication [107] to delineate the part of the contributions of the author of this Ph.D. thesis.

The model for the output stage is shown in Fig. 5-8. The main parasitic capacitances of the MOSFET transistor is assumed to be three fixed capacitors C_{GS} , C_{GD} and C_{DS} . The timing graph for the driving PWM signals V_{MH} , V_{ML} and output signal V_{MO} are shown in Fig. 5-9. There are four kinds of stable states (i), (ii), (iii), (iv) when current flows into load resistance as shown in Fig. 5-9(a), and four kinds of stable states (v), (vi), (vii), (viii) when current flows out of load as shown in Fig. 5-9(b).

Figure 5-9: Driving and modulated signals of CDA output stage with
(a) current flows into load, and (b) current flows out of load

In state (i) and state (v), the high side power transistor M_{NH} is on and the low side power transistor M_{NL} is off. The load current is drawn from supply in state (i) and flows into supply in state (v). State (ii), (iv), (vi) and (viii) are the dead-time states where both power transistors M_{NH} and M_{NL} are off to avoid short circuit current. As the load current is held by the inductor during the dead-time thus the transistor diode will be forward biased. The load current is drawn from ground through the diode across M_{NL} in states (ii), (iv) and flows into supply through the diode across M_{NH} in states (vi), (viii). State (iii) and state (vii) are the states where M_{NH} is off and M_{NL} is on. The load current is drawn from ground in state (iii) and flows into ground in state (vii). The current flows in the CDA output stage for the transition of states are depicted in Fig. 5-10 (a)-(h).

As there is always current flowing through the load resistance, the output power P_{out} dissipated on load resistance R_L is:

$$P_{out} = \frac{1}{T_s} \int_0^{T_s} i_o^2 R_L dt = \frac{1}{2} M^2 I_0^2 R_L \quad (5.7)$$

where M is the modulation index, and

I_0 is the maximum output current.

Consider now the power dissipation due to the on-resistance and the parasitic capacitance in turn.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

Figure 5-10: Current flow in CDA output stage during state transitions where
 (a) from state (i) to (ii), (b) from state (ii) to (iii), (c) from state (iii) to (iv),
 (d) from state (iv) to (i), (e) from state (v) to (vi), (f) from state (vi) to (vii),
 (g) from state (vii) to (viii), and (h) from state (viii) to (v)

5.3.4.1. Power Dissipation Due to On-Resistance

As the NMOS power transistors are working in linear region when they are turned on, the on-resistance is mainly the channel resistance be estimated as:

$$R_{on} = \frac{V_{DS}}{I_{DS}} = \frac{L}{W} \frac{1}{\mu C_{OX}(V_{GS} - V_{TH})} \quad (5.8)$$

Hence, the total power dissipation P_R due to the power transistor on-resistance is:

$$P_R = \frac{1}{T_S} \int_0^{T_S} i_0^2 R_{on} dt = \frac{1}{2} m^2 I_0^2 R_{on} \quad (5.9)$$

where T_S is the input signal period.

The power dissipation is expected to be increased quadratically with modulation index M and output current I_0 , and linearly with load resistance R_{on} . However, the only parameter available to the designer's control is the on-resistance. Hence a lower R_{on} is desired to achieve a low power loss P_R due to the on-resistance, but at the cost of larger chip area, A .

5.3.4.2. Power Dissipation Due to Parasitic Capacitance

The power dissipation due to capacitance occurs only during charging and discharging, or the transition between states in another sense because the stored charges will be consumed by the connected resistance. The power loss due to charging and discharging are the same for a capacitor C with voltage swing V at switching frequency f . With the assumption that the current flows into and out of the load, both occupying half switching cycles, the power loss P_{cap} is then:

$$P_{cap} = \frac{0.5f}{2} CV^2 = \frac{f}{4} CV^2 \quad (5.10)$$

(a) State (i) to (ii)

During this transition shown in Fig. 5-10(a), the high side power transistor M_{NH} is turned off while M_{NL} remains off. As the NMOS of high side driver is turned on, the charges stored on gate capacitors C_{GSH} and C_{GDH} will be discharged. With assumption that high side driver has negligible on-resistance compared to the load, these charges will be mostly consumed by the load resistance. All the charges stored on C_{DSH} , C_{GDL} , C_{DSL} and C_{BOOT} will also be discharged by the load. Hence there is no power loss in these parasitic capacitances during this transition period, i.e.,

$$P_{(i) \rightarrow (ii)} = 0 \quad (5.11)$$

(b) State (ii) to (iii)

During this transition shown in Fig. 5-10(b), the low side power transistor M_{NL} is turned on while M_{NH} remains off. As the PMOS of the low side driver is turned on, the gate capacitances C_{GSL} and C_{GDL} will be charged by low side driver power supply, LV_{DD} . The power loss during this charging states is:

$$P_{(ii) \rightarrow (iii)} = \frac{f}{4} (C_{GDL} + C_{GSL}) LV_{DD}^2 \quad (5.12)$$

(c) State (iii) to (iv)

During this transition shown in Fig. 5-10(c), the low side power transistor M_{NL} is turned off while M_{NH} remains off. As the NMOS of low side driver is turned on, the charges stored on the gate capacitances C_{GDL} and C_{GSL} will be discharged to ground. This discharge power loss can be expressed as:

$$P_{(iii) \rightarrow (iv)} = \frac{f}{4} (C_{GDL} + C_{GSL}) LV_{DD}^2 \quad (5.13)$$

(d) State (iv) to (i)

During this transition shown in Fig. 5-10(d), the high side power transistor M_{NH} is turned on while M_{NL} remains off. As the PMOS for high side driver is turned on hence the gate capacitors C_{GDH} and C_{GSH} will be charged by the boosted high side

driver power supply of $HV_{DD} + V_{REF}$ and V_{REF} respectively. The other affected capacitors C_{DSH} , C_{DSL} and C_{GDL} will be charged by the power transistor supply, HV_{DD} . The power loss due to charging the above-mentioned capacitances is:

$$P_{(iv) \rightarrow (i)} = \frac{f}{4} (C_{DSH} + C_{DSL} + C_{GDL}) HV_{DD}^2 + \frac{f}{4} C_{GDH} (HV_{DD} + V_{REF})^2 + \frac{f}{4} C_{GSH} V_{REF}^2 \quad (5.14)$$

(e) State (v) to (vi)

During this transition shown in Fig. 5-10(e), the high side power transistor M_{NH} is turned off while M_{NL} remains off. The NMOS of the high side driver is turned on in this transition. As the output V_{MO} is still HV_{DD} , the gate capacitor C_{GSH} and C_{GDH} will be discharged from $HV_{DD} + V_{REF}$ to HV_{DD} . The charges will be consumed by on-resistance of M_{NH} and the dissipated power in this discharging process is:

$$P_{(v) \rightarrow (vi)} = \frac{f}{4} (C_{GDH} + C_{GSH}) V_{REF}^2 \quad (5.15)$$

(f) State (vi) to (vii)

During this transition shown in Fig. 5-10(f), the low side power transistor M_{NL} is turned on while M_{NH} remains off. As the NMOS of high side driver remains on, C_{GDH} will be discharged from HV_{DD} to 0. The same applies to C_{DSH} , C_{DSL} and C_{GDL} .

As the PMOS of low side driver is turned on, the gate capacitors C_{GDL} and C_{GSL} will be charged from 0 to LV_{DD} . The power loss in this transition period is:

$$P_{(vi) \rightarrow (vii)} = \frac{f}{4} (C_{GDH} + C_{DSH} + C_{GDL} + C_{DSL}) HV_{DD}^2 \quad (5.16)$$

$$+ \frac{f}{4} (C_{GDL} + C_{GSL}) LV_{DD}^2$$

(g) State (vii) to (viii)

During this transition shown in Fig. 5-10(g), the low side power transistor M_{NL} is turned off while M_{NH} remains off. As the NMOS of high side driver remains on, C_{GDH} will be charged from 0 to HV_{DD} so does C_{DSH} , C_{DSL} and C_{GDL} . Similarly, as the NMOS of low side driver is turned on, the gate capacitors C_{GDL} and C_{GSL} will be discharged from LV_{DD} to 0. The power loss in this transition period is:

$$P_{(vii) \rightarrow (viii)} = \frac{f}{4} (C_{GDH} + C_{DSH} + C_{GDL} + C_{DSL}) HV_{DD}^2 \quad (5.17)$$

$$+ \frac{f}{4} (C_{GDL} + C_{GSL}) LV_{DD}^2$$

(h) State (viii) to (v)

During this transition shown in Fig. 5-10(h), the high side power transistor M_{NH} is turned on while M_{NL} remains off. The NMOS of the high side driver is turned on in

this transition. As the output V_{MO} is still HV_{DD} , the gate capacitor C_{GDH} and C_{GSH} will be charged from $HV_{DD}+V_{REF}$. The dissipated power in this charging process is:

$$P_{(viii) \rightarrow (v)} = \frac{f}{4} (C_{GDH} + C_{GSH}) V_{REF}^2 \quad (5.18)$$

The overall power loss P_C due to parasitic capacitances is the summation of $P_{(i) \rightarrow (ii)}$, $P_{(ii) \rightarrow (iii)}$, $P_{(iii) \rightarrow (iv)}$, $P_{(iv) \rightarrow (i)}$, $P_{(v) \rightarrow (vi)}$, $P_{(vi) \rightarrow (vii)}$, $P_{(vii) \rightarrow (viii)}$ and $P_{(viii) \rightarrow (v)}$, where V_{REF} is set to LV_{DD} for ease of analysis but without loss of generality.

$$\begin{aligned} P_C &= P_{i \rightarrow ii} + P_{ii \rightarrow iii} + P_{iii \rightarrow vi} + P_{iv \rightarrow i} + P_{v \rightarrow vi} + P_{vi \rightarrow vii} + P_{vii \rightarrow viii} \\ &\quad + P_{viii \rightarrow v} \\ &= f(C_{GDL} + C_{GSL}) LV_{DD}^2 \\ &\quad + \frac{f}{4} (2C_{GDH} + 3C_{DSH} + 3C_{GDL} + 3C_{DSL}) HV_{DD}^2 \\ &\quad + \frac{f}{4} (2C_{GDH} + 3C_{GSH}) V_{REF}^2 + \frac{f}{4} C_{GDH}^2 (HV_{DD} + V_{REF})^2 \\ &= C_{GDH} \left[\frac{f}{2} HV_{DD}^2 + \frac{f}{4} (HV_{DD} + V_{REF})^2 + \frac{f}{2} V_{REF}^2 \right] + C_{GSH} \left[\frac{f}{2} V_{REF}^2 \right] \\ &\quad + C_{DSH} \left[\frac{3f}{4} HV_{DD}^2 \right] + C_{GDL} [f LV_{DD}^2] + C_{GSL} [f LV_{DD}^2] + C_{DSL} \left[\frac{3f}{4} HV_{DD}^2 \right] \end{aligned} \quad (5.19)$$

It can be seen from Eqn. (5.19) that the power loss due to the high side power transistor parasitic capacitance is lower than the power loss due to the low side. This is because the discharging of M_{NH} gate capacitance does not dissipate power.

Nevertheless, as there is additional loss in C_{BOOT} , the value of this boost capacitor should be chosen to be comparable to the parasitic capacitances. This is the approach adopted in our design.

5.4. Measurement Results

Fig. 5-11 depicts the die micrograph of the prototype supply modulator fabricated in 180nm CMOS process where the core area is 0.6mm^2 in the 2.25mm^2 die. The prototype supply modulator is packaged in a $4\text{mm}\times 4\text{mm}$ QFN package. Congruous with the aforesaid trade-off, a small $1\mu\text{H}$ off-chip inductor, whose DC resistance and self-resonance frequency are 0.06Ω and 490MHz , respectively, is selected. A 100pF load capacitance is added at the output of the supply modulator to filter the high-frequency noise. On-chip decoupling capacitors ($\sim 100\text{pF}$) are employed to suppress the noises in the supply rails due to the switching of the CDA. In Fig. 5-12 – Fig. 5-16, a resistive load is employed to ascertain the performance of the supply modulator. For completeness, in Fig. 5-17 and Fig. 5-18, the tests include an evaluation of the overall performance of the ET PA embodying our supply modulator as the supply of a commercial RF PA. The RF signals and the envelope signals were generated from the vector signal generator and the measurements of the output power spectrum were obtained using the signal analyser. In all measurements, $V_{DD} = 3.6\text{V}$ was used for our supply modulator.

Figure 5-11: Microphotograph of the prototype supply modulator.

Fig. 5-12(a) depicts a plot of the measured power-efficiency of the supply modulator when tracking different DC output voltages, i.e., static power-efficiency. Three resistive loads, 4Ω , 6.7Ω and 10Ω , were used. The 4Ω load serves to ascertain the driving capability of the supply modulator, where the supply modulator provides a maximum output power of 2.5W at $v_o = 3.2\text{V}$, with $\sim 88\%$ power-efficiency. With the nominal 6.7Ω load, the output voltage swing ranges from 0.3V to 3.3V , and a peak efficiency of 91% is achieved at $v_o = 3.3\text{V}$, i.e., the output power is 1.63W . It can be observed from Fig. 5-12(a) that the power-efficiency of the supply modulator, as expected, reduces for higher resistive loads at low output voltages. For example, at $v_o = 1.8\text{V}$ ($\sim 5\text{dB}$ backoff), the power-efficiency of the supply modulator for 4Ω , 6.7Ω , 10Ω is 70.6% , 67.2% and 61.7% , respectively. The decrease of the power-efficiency is mainly due to the largely constant and relatively large quiescent power dissipation of the Class AB amplifier. Figs. 5-12(b) and 5-12(c) compare the static power-efficiency with the state-of-the-art designs at different output power and

different normalized output power (with respect to their maximum output power), respectively. The reported supply modulators are optimized for different output-power levels and different bandwidth, which inevitably affects the design of the Class AB amplifier therein and the quiescent power dissipation of the Class AB amplifier. The proposed supply modulator shows comparable power-efficiency for low- to mid-power applications, and achieves the highest peak efficiency of 91%. The output voltage range and power-efficiency parameters will be benchmarked against the state-of-the-art supply modulators in Table III later.

(a)

(b)

(c)

Figure 5-12: (a)The measured static power-efficiency; The comparison of the static power-efficiency with the state-of-the-art designs at (b) different output power, and (c) different normalized output power

Fig. 5-13 – Fig. 5-16 are measured with the nominal 6.7Ω load, as it corresponds to our testing of the commercial RF PA whose $V_{DD} = 3.2V$ (i.e., $v_O = 3.2V$ for the supply modulator) and 28.5dBm output power. Fig. 5-13(a) depicts the output waveform, v_D , of the CDA at the maximum switching frequency of 35MHz, where the propagation delay is $\sim 7ns$. As expected, there is ground-bounce noise, i.e., voltage spikes on the otherwise clean supply rails. This is largely due to the switching operation of the CDA and the inductance of the bonding wires. In the prototype supply modulator, the CDA is powered separately from the other analog circuits (including the Class AB amplifier and the hysteresis controller). In the packaging of the prototype supply modulator, multiple power pins and multiple bonding wires were employed to reduce the bonding wire inductance (hence reducing the ground-bounce). Fig. 5-13(b) depicts the output waveform, v_O , of the supply modulator, at $v_O = \frac{1}{2}V_{DD}$. The ripple noise is $\sim 4mV_{rms}$ (i.e., $16mV_{pp}$) at 35MHz switching frequency, and this complies with the stipulated spectrum mask of the 20MHz LTE signals; see Fig. 5-17 later. Different from the noise mechanism of CDAs [24, 40, 108], the ripple noise due to high switching frequency is the main source of noise in the supply modulator. The ripple voltage of our supply modulator is relatively small – suppressed by the wideband Class AB amplifier with small output impedance at the switching frequencies (refer to Fig. 5-10(b)) and the $1\mu H$ external inductor.

(a)

(b)

Figure 5-13: 35MHz measured waveforms

(a) switching frequency, and (b) output ripple

Fig. 5-14 depicts a plot of the measured dynamic power-efficiency of the supply modulator when tracking sinusoidal signals with different frequencies, ranging from 15kHz to 60MHz. Four sinusoidal signals with a DC voltage of 1.8V and with different peak-to-peak values, 1V_{pp}, 1.4V_{pp}, 2V_{pp}, and 2.5V_{pp}, were used. With 1V_{pp} and 1.4V_{pp}, the supply modulator is able to track sinusoidal inputs to ~60MHz (i.e., ~60MHz bandwidth), while at 2V_{pp} and 2.5V_{pp}, the bandwidth of the supply modulator is ~40MHz and ~30MHz respectively. The prototype supply modulator features high dynamic power-efficiency over a wide range of input frequencies, and of particular interest, its power-efficiency is 68.9% and 71.9% for the 60MHz 1.4V_{pp} and 30MHz 2.5V_{pp} sinusoidal inputs respectively. The power-efficiency is almost

constant when tracking low-frequency input signals because the switching frequency and the ripple current from the Class AB amplifier are almost constant. When the frequency of the input sinusoidal signal increases from ~1MHz to 2-4MHz, the power-efficiency of the supply modulator increases. This is due to the low switching frequency (equals to the signal frequency), hence low switching losses. Beyond 2-4MHz, the power-efficiency decreases due to the increased output power from the relatively power-inefficient Class AB amplifier.

Figure 5-14: Dynamic power-efficiency

To ascertain the bandwidth of the supply modulator, a 60MHz 1.4V_{pp} sinusoidal signal (from 1.1V to 2.5V) is applied separately to the supply modulator. Fig. 5-15 depicts the ensuing output waveform of the supply modulator where the respective output signal closely tracks the input signal.

Figure 5-15: Time domain response of our supply modulator tracking a 60MHz
1.4V_{pp} sinusoidal signal (from 1.1V to 2.5V)

The waveforms of the input signal and the time domain response of our supply modulator tracking an envelope signal extracted from a 40MHz LTE-A RF signal are depicted in Fig. 5-16. To the best of our knowledge, there is no commercially available 40MHz LTE-A RF PA for ET PA at this stage. In the measurements, the 6.7 Ω resistor is connected as the load to the supply modulator. The 40MHz LTE-A RF signal consists of two component carriers, and each component carrier is a 20MHz LTE (100RB, QPSK) RF signal. The supply modulator is able to track the envelope signals closely. The proposed supply modulator can provide a maximum power of 1.2W with a maximum efficiency of 85%.

Figure 5-16: Time domain response of our supply modulator
tracking a 40MHz LTE-A envelope signal

To ascertain the overall performance of the ET PA embodying the prototype supply modulator and a commercial RF PA, Band VIII 20MHz LTE (100RB, QPSK) RF signals and their extracted envelope signals are applied to the ET PA. Fig. 5-17 depicts the measured output spectrum at 27dBm RF PA output power, which meets the spectrum mask of 20MHz LTE signals.

Figure 5-17: Measured RF PA output spectrum for 20MHz LTE signal
 at 27dBm RF PA output power

Fig. 5-18 depicts the measured power added efficiency (PAE) of the ET PA and the stand-alone RF PA against the RF PA output power. The measured overall PAE of the ET PA is 41.1% @28.5dBm – a significant 11% power-efficiency improvement compared to the stand-alone PA. Of particular interest, the improved power-efficiency is even more significant around 3dB backoff where the improvement is ~13% – a significant >1.6x improvement compared to the RF PA without the supply modulator.

Figure 5-18: PAE of the ET PA and the stand-alone RF PA

The measurements of the prototype supply modulator are consolidated in Table IV and are benchmarked against pertinent state-of-the-art designs. It can be seen that the prototype supply modulator features the highest performance for three imperative parameters – 40MHz bandwidth, 2.5W maximum output power and 91% peak power-efficiency. In short, the proposed supply modulator is highly competitive.

Table IV: Benchmark of state-of-the-art supply modulators

Design	This work	JSSC'16	JSSC'17	ISSCC'16	PE'16	PE'16
Control	Delay-based hysteresis control	SCCI	Ripple-current-based PWM	Hysteresis with AC-coupling	SIDO	SAVT
Topology	Hybrid	Hybrid	Hybrid	Hybrid	Class D	Class D
Bandwidth	40MHz	-	-	40MHz	10MHz	10MHz
	LTE-A	-	-	LTE-A	LTE	LTE
Bandwidth	60MHz 1.4V _{pp} sine wave	10MHz 0.8V _{pp} sine wave	13MHz 0.8V _{pp} sine wave	-	-	-
Maximum output power	2.5W	0.2W	0.2W	1W	1W	2W
Maximum static power-efficiency	91%	88%	88%	-	-	87%
Maximum dynamic power-efficiency	85%	81%	81%	83%	87%	86%
Output voltage	3V	0.8V	0.8V	-	4V	1.7V
	0.3-3.3V	0.2-1V	0.2-1V	-	0.5-4.5V	0.5-2.3V
Ripple noise	16mV _{pp}	8mV _{pp}	8mV _{pp}	-136dBm/Hz	-	-
Supply voltage	3.6V	1.2V	1.2V	4V	3.3V	3.3V
Process	180nm	130nm	130nm	130nm	180nm	180nm

5.5. Conclusions

We have described a supply modulator comprising a proposed delay-based hysteresis controller, proposed wideband Class AB amplifier, and CDA for an ET PA. We have shown that to achieve maximum power-efficiency for wideband supply modulators, the hysteresis should be controlled by the propagation delay of the supply modulator – not the threshold current of the hysteresis controller. The prototype supply modulator was shown to be the most competitive design when benchmarked against reported supply modulators – it featured the widest bandwidth, highest output power and highest static power-efficiency, yet with high dynamic power-efficiency, high output swing and low ripple noise at 3.6V supply. The ET PA embodying our supply modulator achieved 41.4% power-efficiency at 28.5dBm peak output power and 34.4% at 3dB backoff – a significant 1.6x improvement over the standard-alone RF PA.

Chapter 6 Conclusions & Recommendations

6.1. Conclusions

We have presented the motivations and detailed objectives of this Ph.D. program in Chapter 1. A comprehensive review on CDA architectures has been provided in Chapter 2.

In Chapter 3, we have analytically investigated the THD and PSRR of a PIPO CDA and have derived their expressions. The derived expressions have been verified by means of computer simulations based on a commercial 65nm process. Based on the derived analytical expressions, a practical design using a 65nm CMOS process was presented. We have shown that the PIPO CDA featured superior performance (in terms of THD and PSRR) compared to a conventional CDA that embodied the same integrator and output stage.

In Chapter 4, we have proposed, to the best of our knowledge, the first-ever 3-state filterless Bang-Bang control CDA; the filterless attribute is eliminated the undesirable bulky and expensive output lowpass filter. The proposed 3-state Bang-Bang control CDA featured the simplest hardware and high power-efficiencies of ~95% but with somewhat compromised fidelity). Nevertheless, the fidelity is sufficient for many low-power power-critical audio applications.

In Chapter 5, we have investigated the mechanisms of power dissipation of CDA for an ET PA for RF applications. The proposed supply modulator simultaneously

featured the wide bandwidth (40MHz), high output power (2.5W), high peak efficiency (91%), high output voltage swing (3V) and low output ripple noise (4mVrms) at 3.6V supply. The ET PA embodying our proposed supply modulator achieved a high power-efficiency of 41.4% at 28.5dBm peak output power and 34.4% at 3dB backoff – a significant >1.6x improvement over the RF PA without the supply modulator.

6.2. Recommendations and Future Work

We recommend the following as future work:

- (i) To investigate, propose and implement architectures and design methods of a high-speed high-power PIPO CDA for cellular applications (4G-LTE-A, 4G LTE-A Pro, 5G NR, etc.) The intention is the proposal of a novel CDA architecture for RF PA and exploits the advantages offered by PIPO CDA.
- (ii) We further propose an investigation to exploit the unique advantages offered by III-V semiconductors over CMOS process, e.g. Gallium Nitride on CMOS (GaN-CMOS) and/or Indium Gallium Arsenide on CMOS (InGaAs-CMOS).
- (iii) To investigate the mechanisms of non-linearities, especially THD, of the proposed 3-state Bang-Bang control CDA. We note that the current

design somewhat compromises the fidelity but is sufficient for many low-power power-critical audio applications. It will be particularly interesting if the fidelity could be improved for mid-power and high-power applications.

- (iv) To investigate a novel method that improve the system bandwidth of the supply modulator used for the ET PA. The intention is to extend the scope of envelope tracking to include the 5G New Radio where the maximum channel bandwidth is 100MHz for Frequency Range 1 (sub 6GHz) and 1GHz for Frequency Range 2 (above 6GHz).

Author's Publications

Journal Publication

- [1] H. He, **Y. Kang**, T. Ge, L. Guo, and J. S. Chang
“A 2.5W 40MHz-Bandwidth Hybrid Supply Modulator with 91% Peak Efficiency, 3V Output Swing and 4mV Output Ripple at 3.6V Supply”
IEEE Transactions on Power Electronics, volume 34, issue 1, pp. 712-723,
Jan. 2019
- [2] H. He, T. Ge, **Y. Kang**, L. Guo, and J. S. Chang
“A 40MHz Bandwidth, 91% Peak Efficiency, 2.5W Output Power Supply Modulator with Dual-mode Sigma-Delta Control and Adaptive Biasing Amplifier for Multi-standard Communications”
IEEE Transactions on Power Electronics, submitted in May 2019,
(conditional accepted and revised in Nov 2019)

Conference Publications

- [3] **Y. Kang**, T. Ge, H. He, and J. S. Chang
“A review of audio Class D amplifiers”
International Symposium on Integrated Circuits (ISIC), Singapore, pp. 1-4,
2016.
- [4] H. He, **Y. Kang**, J. Yu, L. Guo, T. Ge, and J. S. Chang
“A novel low-power high-efficiency 3-state filterless Bang-Bang class D amplifier”

IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, Egypt, pp. 93-96, 2015.

- [5] Q. Yong, W. Shu, **Y. Kang**, and J. S. Chang
“A 30V 2A Real-Time Programmable Solid-State Circuit Breaker with Improved Detection-Speed and Enhanced Power-Efficiency”
European Solid-State Circuits Conference (ESSCIRC), Kraków, Poland, pp.1-4, 2019.

- [6] T. Ge, J. Zhou, **Y. Kang**, and J. S. Chang
“Review: A fully-additive printed electronics process with very-low process variations (Bent and unbent substrates) and PDK”
IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, Maryland, United States, pp. 1-4, 2017.

- [7] T. Ge, H. He, J. Zhou, **Y. Kang**, and J. S. Chang
“An Investigation of THD of a BTL Class D Amplifier”
IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, pp. 1-4, 2016.

- [8] T. Ge, L. Guo, H. He, **Y. Kang**, J. Yu, and J. S. Chang,
“Envelope Tracking RF Power Amplifiers: Fundamentals, Design Challenges, and Unique opportunities offered by LEES-SMART InGaAs-on-CMOS process”
8th International Conference on Materials for Advanced Technologies, Singapore, 2015.

- [9] T. Ge, L. Guo, **Y. Kang**, J. Zhou, H. HE, P. J. E. Ng, E. Fitzgerald, K. E. K. Lee, and J. S. Chang
“A driver circuit based on the emerging GaN-on-CMOS process for the emerging Electroluminescent panels”
IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, Colorado, United States, pp. 1-4, 2015.
- [10] L. Guo, T. Ge, **Y. Kang**, H. He, and J. S. Chang
“Analysis and design of PWM-in-PWM-out Class D Amplifiers”
IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, Texas, United States, pp. 254-257, 2014.
- [11] J. S. Chang, K. S. Chong, W. Shu, T. Lin, J. Jiang, K. Z. L. Ne, and **Y. Kang**
“Radiation-hardened library cell template and its total ionizing dose (TID) delay characterization in 65nm CMOS process”
IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, Texas, United States, pp. 821-824, 2014.

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