An approach for circuit design optimization based on complexity considerations

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**AN APPROACH FOR CIRCUIT DESIGN OPTIMIZATION
BASED ON COMPLEXITY CONSIDERATIONS**

TAN ZHI QUAN AARON

School of Electrical & Electronic Engineering

2019

**AN APPROACH FOR CIRCUIT DESIGN OPTIMIZATION
BASED ON COMPLEXITY CONSIDERATIONS**

TAN ZHI QUAN AARON

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

in partial fulfillment of the requirement for the degree of

Doctor of Philosophy

2019

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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SUPERVISOR DECLARATION STATEMENT

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Goh Wang Ling

AUTHORSHIP ATTRIBUTION STATEMENT

This thesis contains material from 6 papers published or pending publication in the following peer-reviewed journal(s) and conferences where I was the first and/or corresponding author.

Chapter 2 is published as Aaron Tan, Rui Tze Toh, Alfred Lim, Yongfu Li, Zhi Hui Kong, "A Simplified Methodology To Evaluate Circuit Complexity: Doherty Power Amplifier As A Case Study," *in Electronics 2019, 8, 313*

The contributions of the co-authors are as follows:

- Aaron Tan prepared the manuscript drafts, constructed and derived the formulas and edited the drafts based on inputs of co-authors
- Dr Rui Tze Toh provided his insights on industry's direction and gave his suggestions on the improvements over time
- A/Prof. Yongfu Li discussed and gave opinions on the complexity of circuits and helped to interpret some of the data collected
- Alfred Lim provided his layout design expertise in doing the floor planning of the circuits for simulate complexity
- Dr Zhi Hui Kong provided valuable feedbacks on the drafts and helped to proof-read the manuscripts. She also fine-tuned the selling points of this work.

Chapter 3 is published as Alfred Lim, Aaron Tan, Zhi Hui Kong, Kaixue Ma, “A Design Methodology And Analysis for Transformer-Based Class-E Power Amplifier,” in *Electronics* 2019, 8, 494

The contributions of the co-authors are as follows:

- Alfred Lim conceptualized, designed the parameters, interpreted some results and prepared the manuscript
- Aaron Tan verified some of the results and aided in designing the parameters of the Class-E PA design
- Dr Zhi Hui Kong advised and proof-read the manuscript
- Prof. Kaixue Ma provided the simulation resources

And pending internal review as Rui Tze Toh, Shyam Parthasarathy, Aaron Tan, Amit Kumar Sahoo, Jen Shuang Wong, Shaoqiang Zhang, Madabusi Govindarajan, Kok Wai Chew, "Power Amplifier Topologies Using EDNMOS On CMOS-SOI For Sub-6 GHz Wireless Applications," and pending submission as Aaron Tan, Rui Tze Toh, Alfred Lim and Wang Ling Goh, “S-Band HRSOI Process Cascode Amplifier with High Gain and PAE”

The contributions of the co-authors are as follows:

- Dr Rui Tze Toh did the consolidation of data, comparison and manuscript drafts
- Shyam Parthasarathy is the technical lead for the work done
- Aaron Tan did the design and layout floor-planning of the proposed 4-stacked resistor-ladder SGNFETs simulations and analyses
- Dr Amit Kumar Sahoo did the load-pull measurement

- Jen Shuang Wong did the S-Parameters measurement and the layout designer for 2-stacked cascode
- Dr Shaoqiang Zhang is the technical advisor for issues regarding the design and fabrication
- Dr Madabusi Govindarajan designed the cascode EDNFET and SGNFET test topology
- Dr Kok Wai Chew is the technical advisor for the overall direction and provided the usage of the measurement tool
- Alfred Lim did the layout floor planning of the design and troubleshoot design rule checks
- A/Prof Wang Ling Goh advised and provided feedback on the improvements of the manuscript

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- Aaron Tan designed, ran the experiments and did the floor-planning of the circuits
- Aaron Tan prepared the manuscripts and they were proof-read by both Dr Zhi Hui Kong and Prof. Kaixue Ma
- Prof. Kaixue Ma lent his technical expertise on the DPA designs

- Dr Zhi Hui Kong advised on the technical manuscripts style. She also helped to fine-tune the selling points of the manuscripts
- Prof. Kai Seng Yeo gave his insights and fine-tuned the DPA designs based on his experience with general RF circuits

01/11/2019

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Date

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Tan Zhi Quan Aaron

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LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
CF	Complexity Factor
CMOS	Complementary Metal Oxide Semiconductor
DPA	Doherty Power Amplifier
EDNFET	Extended Drain N-Doped Field Effect Transistor
EER	Envelope Elimination and Restoration
EHF	Extremely High Frequency
EM	Electro-Magnetic
ET	Envelope Tracking
ETPA	Envelope-Tracking Power Amplifier
FET	Field Effect Transistor
FoM	Figure-of-Merit
GaAs	Gallium Arsenide
GSG	Ground-Source-Ground
HVFET	High-Voltage Field Effect Transistor
IMD3	Inter-Modulation Distortion (IMD3)

IP3	Third-Order Intercept Point
ITRS	International Roadmap for Devices and Systems
LINC	Linear Amplification with Nonlinear Components
M/N	Matching Network
NCF	Normalized Complexity Factor
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-To-Average-Power-Ratio
RF	Radio-Frequency
RFSOI	Radio-Frequency Silicon-On-Insulator
SCPA	Switched-Capacitor Radio-Frequency Power Amplifier
SGNFET	Single-Gate N-Doped Field Effect Transistor
SHF	Super High Frequency
SiGe	Silicon Germanium
TTM	Time-To-Market
UHF	Ultra-High Frequency

ABSTRACT

Optimizing circuit trade-offs is a highly challenging task for any design team. This challenge is further exacerbated with the additional design complexity of integrating multiple circuits. Today, with the increasing demand for newer wireless communication products, design teams face a shorter time-to-market (TTM) for every generation of their new products and each product requires major improvement in wireless capability. Hence, it is important for the design teams to design circuits with complexity in mind. A design approach divided into architecture complexity, component complexity and discretional complexity are proposed. A novel benchmarking figure-of-merit, complexity factor (CF), was formulated and proposed for the architecture complexity. A simulated application of a goal, gain optimization, demonstrated and revealed that a reduction of up to 400% in the normalized complexity factor (NCF) could enhance the gain performance by approximately up to 40% for ultra-high frequency (UHF) applications. As the number of variables to be permuted is very high for the power amplifier (PA) blocks from circuit down to the process level, it is treated as a black box in the analysis but the next topology complexity step addressed this. A topology comparison was proposed between a 2-stacked EDNFET and SGNFET and a 4-stacked resistor-ladder SGNFET PA. Both of them achieved a near 20dBm output power and approximately 60% efficiency on the test-chips measurements, which demonstrated that the 2-stacked EDNFET and SGNFET topology with a reduction in stack height is a potential candidate for a reduced difficulty and complexity Doherty power amplifier (DPA) design. In the discretional complexity step, we explored the linearization of the DPA and proposed a DPA with a gm3 cancellation bias scheme tapping on its intrinsic linearization property, without adding external circuitry to

increase the complexity of the overall circuit but at the same time, improve its linearity by 6-8dB compared to a DPA optimized for power and more than 9dB compared with a balance PA with a similar structure.

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CHAPTER 1

Introduction and Motivation

1.1 Background

With the increasing appetite of the market for more functionality and performance of RF products, semiconductor and circuit design companies are racing to implement better performing circuits on integrated circuit chips, which result in higher complexity designs. This caused the organizations in the industry to be in a game of overtaking where they would always do everything to increase the standards on time-to-market (TTM) and product performance. Many companies shroud the pressures of TTM and design complexity by increasing headcounts until someone puts a stop to the increasing operating cost or layoff occurs.

With the process technology differentiation out of the equation, this puts the circuit design competitiveness and productivity at the forefront. From a circuit designer's point of view, designing, optimizing and analyzing circuits is not an easy task to be done simultaneously. This is because the complexity of circuit designs increases

with the scaling of technology. This is even more so for RF circuits, where parameters do change with frequency and even signal levels for components such as power amplifiers. Design approaches for optimizing circuit performance such as targeting reliability at the circuit level [1] or for performance improvements at the component level [2, 3] are focusing on best practices for achieving better design outcomes. On the other hand, there are also design approaches that are coming in from a digital and analog system design perspective [4, 5] that deal with the complexity of design planning to circuit verification and the implementation. The design approaches for optimization are often not targeting at the circuit level to address its complexity specifically. However in the recent years, RF circuits at the system level are receiving attention in reducing their complexity [6, 7]. For complexity issues to be addressed, it has to be from the ground up to reduce unnecessary manpower, cost and time wastage, starting from the component level as seen in Figure 1.1. The final complexity at C4 would be an exponential increment over the different stages of development and it would not be an easy feat to trace the earlier tasks to resolve complexity issues. Hence, it is important for the design teams to have a design approach at the component level for optimizing circuit performance involving complexities to come up with the final product.

Figure 1.1: Simplified Flow Diagram Of Product Development

PA is one of the most power consuming components in a RF sub-system and the complete system with other digital and analog integrated components. With recent news and spotlights on Huawei, the proliferation of 5G technology is gaining media attention. 5G would be tapping on the sub-6GHz and also in millimeter-wave (mm-wave) range of 24 to 86GHz, with the sub-6GHz PA having to achieve close to 25dBm or more [8].

A good candidate for PA is the DPA [9] which enhances efficiency at back-off as shown in Figure 1.2. It will be used as the core example circuit in this thesis. There are some of the emerging DPA architecture introduced in the recent years, such as harmonic matching [10, 11], inverted DPA [12], impedance combining [13] and addition of offset lines [14, 15], which are implemented to improve the performance and to overcome the disadvantages of silicon processes such as inherent low gain, silicon substrate losses and low drain source breakdown voltages of transistors.

Figure 1.2: Ideal Block Diagram Of Doherty Power Amplifier

The new circuit architecture come with design trade-offs. Degradation of RF circuits such as hot carrier injection, oxide breakdown [16] and electromigration [17] are some examples. Before any design team or designer decides to incorporate new architecture in the circuit design, it is also important to understand the complexity

for these because the integration of new techniques requires an additional effort to optimize the circuit performance. These can be characterized and managed under complexity considerations and the hierarchy of the proposed approach and the role this fits in can be seen from Figure 1.3.

The architecture complexity first deals with the big picture of the component, which is DPA in this thesis as an example. Choosing architecture with low complexity before diving into the topology helps to reduce unnecessary time in optimization. The next step of the approach involves the topology complexity. The PA as a sub-block in the DPA has different topologies such as differential PA [18, 19], cascade PA [20, 21] and cascode PA [22, 23] to name a few. For PA in general, the output power is required to be high as the conventional component before the antenna in a transmitter.

Figure 1.3: Hierarchy And Flow Of Complexity Considerations

After the first two considerations have been addressed, the discretional complexity involves the optional parameter to optimize the circuit and for the sake of discussion

in this thesis, linearity. Some PAs are to be used in the non-linear region. However, there are PAs which are required to operate with high linearity but due to the intrinsic non-linear characteristics of the PAs used, they display non-linear properties after circuit design. Linearization techniques can add additional complexity to the entire DPA, which will be discussed in Chapter 4. In this aspect, discretionary complexity can be exercised.

Following this flow of design considerations shown in Figure 1.3 using DPA as an example, starting from the architecture complexity down to the discretionary complexity, the complexity issue at the component level can be addressed.

1.2 Challenges and Limitations

In addressing the complexity considerations of circuits using DPA as an example, the area of the circuit is not explicitly included in the analysis using the proposed approach. However, it is indirectly tied to the architecture complexity as by reducing the number of passive elements in the architecture using DPA as an example, the area of the chip will be reduced. As the proposed complexity analysis needs data to calculate, new frequency of applications or tech nodes will have some difficulty in analyzing as there would not be enough data to provide a meaningful result. This would limit the implementation of the architecture complexity step but the topology and discretionary complexity considerations can still be carried out.

For researchers who wish to tap on the proposed architecture complexity analysis, time has to be spent on collecting the relevant data needed for their designs. This might add a time overhead to their design cycle. However, it needs to be only done once. It would be more appropriate for the foundries to collect the data using

customers' designs as black-boxes to get the data as process design kits are available to designers from the foundries and the data could be stored by the foundries and disseminated to designers instead.

The topology complexity analyses the PA topology which can be implemented into the DPA. However, the results of the PA could depend on the process technology nodes as well. With advancement of the semiconductor industry and different technologies ranging from gallium arsenide to silicon, silicon-on-insulator and silicon germanium, a comparison of a similar topology across different processes should not be made as it would render the results inaccurate. The topologies have to be compared between or among the same process for example, 65nm silicon process. In the topology complexity, there is no metric to quantify the step. As such, it has to be based on the users' judgement. A general rule of thumb is that when the number of active components is being reduced, the complexity will be reduced as well. For the example of PA topologies introduced in Chapter 3, this thesis only did a study of comparison between two stacked topologies out of the many research works that had been done. Furthermore, if the results from Chapter 3 need to be replicated, the devices are from 0.13 μ m RFSOI process which others may not have access to get the same results. The works are to demonstrate that it is possible to have a lower complexity topology to achieve comparable or even better performance out there for the industry and academia.

Discretional complexity in this thesis only examines one optional parameter of enhancement and as an example of using the DPA, the linearity. It will be difficult to gauge the complexity if multitude of enhancements were chosen to be made to the circuits. Furthermore, this thesis does not quantify the discretional complexity

but showing the possibility of achieving better performance in the chosen parameter without increasing the complexity of the circuit by doing an internal optimization. A designer or researcher may not choose to perform this complexity consideration if the basic performance is being met at the topology complexity consideration.

1.3 Contributions

This thesis focuses on the complexity considerations of circuit using DPA as an example. The approach first focuses on the architecture complexity. Analysis uses S-Parameters and parameters of matching network to quantify a metric for benchmarking of DPAs. This tool can be further extended to other circuit components, where design time is a primary concern. After which, a topology complexity consideration is given to the PA blocks, demonstrating the potential that a lower complexity topology can show comparable performance to a higher complexity one. Moreover, the discretionary complexity step allows us to propose gm3 cancellation DPA with no added complexity to the circuitry. The following detailed contributions have been achieved:

- An approach and flow are proposed for circuit design using DPA as an example.
- A proposed figure-of-merit (FoM), complexity factor (CF) and hence, normalized complexity factor (NCF), is introduced with formulation to tackle the architecture complexity issue.
- The topology complexity issue addresses the PA blocks in DPA. We proposed a comparison between stacked extended-drain N-doped field effect transistor (EDNFET) and single gate N-doped field effect transistor (SGNFET) and a 4-stacked SGNFET topology implemented on 0.13 μm

radio frequency silicon-on-insulator (RFSOI) process as potential candidates for a reduced complexity DPA design, demonstrating a lower complexity topology has the potential to yield comparable performance to a higher complexity topology.

- A gm3 cancellation bias was proposed to demonstrate linearity enhancement to DPA without adding additional circuitry to increase its complexity based on the discretional complexity. Its results were compared with a DPA optimized for power and a balance PA and it is in good agreement with the operation of a DPA at higher output power levels with improved linearity.

1.4 Organization

This thesis is organized as follows. Chapter 1 introduces the background knowledge of complexity-aware DPA limitations and challenges. It also includes the background and motivation for research of this area and lists the major contributions of this thesis.

Chapter 2 first introduces the DPA and the different architecture to improve the performance of the DPA. Based on some of the architecture, a study has been conducted on the complexity of the DPA designs. A methodology to quantify a metric to evaluate the circuit complexity with DPA as an example was proposed. It is shown that a reduction in the complexity can potentially increase the gain performance. A detailed discussion on an example objective, which is gain optimization, is carried out in the subsequent subchapter.

Chapter 3 presents the aspect on topology complexity. As the proposed approach to evaluate the complexity of the architecture assumes the PA blocks as black-boxes due to the limitations of this research work, there is a need to simplify the PA topology as much as possible. The experimental results for the 2-stacked EDNFET and SGNFET and the 4-stacked SGNFET are discussed in the subchapters.

Chapter 4 discusses the discretional complexity, using linearity of the DPA as an example. This chapter begins with a more specific review of various linearization techniques of PA block for the DPA. A gm3 cancellation bias DPA is then proposed with no additional circuitry to improve its linearity and experimental results are discussed in the subchapter.

Finally, Chapter 5 draws the conclusion of this research and gives the area that merits future works.

CHAPTER 2

Architecture Complexity

2.1 Background

The DPA is one of the most popular techniques to enhance the efficiency of a PA, particularly at the back-off region where a PA would be favored to operate in as it would allow the PA to be in the linear operation. Its simplicity and potential are reviving the research of DPA in the recent years for sub 6GHz [24-27] as well as into the 60GHz region [28-30]. The DPA employs two PAs in different classes, typically class A, B and AB, combining the output power of the two PAs to increase the power range of the DPA and thus extends the efficiency range of the PA block. The main PA amplifies the signals when the input power is low while the auxiliary PA will turn on at the peak output power, depending on the condition the designer sets. This will result in two peaks for its efficiency; one at full output power and the other at a usually 6 dB back-off for a conventional design. Figure 2.1 shows a more practical block diagram of the DPA [31].

Figure 2.1: Practical Block Diagram Of Doherty Power Amplifier

If the transistors were to be ideal, the DPA architecture would have been easy to realize. However, parasitic resistance, inductance and capacitance complicate the design effort as the optimal output impedance of the power amplifiers become complex numbers instead of real numbers. As the load modulation at the output of the main PA works for real impedances, conventional output matching networks need to be combined with offset lines at the output of the PAs before the quarter-wave length impedance inverter and impedance transformer. Research works have been conducted to improve the efficiency and linearity, enhancing the bandwidth, and allowing the DPA to operate in multi-bands. Jangheon Kim et. al. [32] optimized the transistors biasing and sizes so as to focus on compensating the amplitude and phase distortions at high power level as shown in Figure 2.2. The other blocks of the DPA are not modified. This would reduce the complexity of the pre-distorters that would be needed to enhance the overall system's performance such as linearity.

Figure 2.2: Schematic Of Uneven Transistors' Sizing And Biasing [32]

As mentioned earlier, two efficiency peaks can be demonstrated with a conventional DPA. However, high peak to average power ratio (PAPR) applications require higher efficiency at back-off, which can be achieved with a 3-way DPA as demonstrated in [33-35].

The concept of 3-way DPA as shown in Figure 2.3 is used to maintain the efficiency at the back-off region that extends beyond the conventional design which is typically at 3dB back-off. Three branches of PAs are being used instead of two and they are turned on at different output power levels, thus extending the efficiency range.

Figure 2.3: Schematic Of Three-Way DPA With Adaptive Gate Biasing [35]

Modifying the output matching network (M/N) as demonstrated by S. Chen and Q. Xue [36] is another technique to improve the efficiency at back-off. This is done to rectify the unbalance contribution of currents by the main and auxiliary PA branches in a two-way DPA.

Even with these architecture to enhance the linearity and efficiency of DPA, the quarter wavelength lines are intrinsically the bottle-neck of the narrow-band DPA designs. Research works have shown that optimizing the output block of the DPA [37-39] allow high back-off efficiency over a larger bandwidth. This can be achieved by integrating the matching, offset lines and impedance transformer into a network that combines all these functions or cancellation of reactive components of devices at the band of interest together with harmonic tuning for the higher frequencies. These works have focused on improving the different aspects of DPA to enable it to compete with the standard class AB or other classes of PA that are widely adopted in the industry by design companies but they did not address the complexity of the DPA architecture, which is a concern for market-driven works as time and cost are of paramount importance. The works explored the possibilities of

implementing certain architecture but we may find that often, their results could be comparable. Therefore, it is important to analyze the complexity of DPA architecture.

2.2 Motivation

It has been observed that if circuit enhancement architecture are implemented at the expense of increased complexity, the circuit performance improvement could be marginal and it would result in a diminishing return for an investment of time into the optimization. For example, X. Fang et al. [40] employed 33 matching network (M/N) elements to achieve a saturation output power (P_{sat}) of 42dBm, power added efficiency (PAE) of 50.3% and a gain of 11dB at around 2GHz. However, C. H. Kim et al. [41] achieved slightly higher overall performance based on only 16 M/N elements with both of them utilizing GaN technology. As such, there is a need to analyze the complexity of DPA architecture to benchmark against published designs so that it can be decided whether to continue with the work or to adopt the published design for a targeted parameter to enhance. An extensive overview of the different solutions to enhancing DPA has been presented by Vittorio et al. [42]. The work in this chapter aims to provide an alternative view to DPA designs from the perspective of architecture complexity but not the details of the DPA designs such as performance of the passive components or the area of the inductors for example. Complexity factor (CF), which is a function of the number of parameters of the individual blocks of circuits as a figure of merit is proposed. With this exemplary model, designers will be able to extend this concept, quantify a metric and evaluate the complexity before committing to any circuit design.

2.3 Contributions

The complexity of circuits affects the design time and consequently the TTM for products. The CF of a DPA architecture was demonstrated and analyzed by studying the number of S-parameters of the power divider and PA which consist of transistors as shown in Figures 2.4 and 2.5, and the number of parameters of the M/N. The numbers of parameters for the M/N are the key parameters in these analyses and some of these blocks can be characterized through S-parameter models.

Figure 2.4: Complexity Paths for Two-Way DPA

The proposed CF is a function of complexity numbers of the individual blocks defined as

$$CF = f(C_{PD}, C_{PA}, C_{M/N}) \quad (2.1)$$

C_{PD} is the complexity number for the power divider

C_{PA} is the complexity number for the power amplifier

$C_{M/N}$ is the complexity number for the matching network

Figure 2.5: Complexity Paths For Three-Way DPA

As shown in Figures 2.4 and 2.5, C_M and C_A are the aggregate complexity numbers for the paths of the carrier or main PA and auxiliary PA respectively. The fundamental building blocks for DPA are the power divider, the carrier and auxiliary PA branches and the output quarter-wavelength line from the carrier to the auxiliary branches which can also be considered as the power combiner. The quarter-wavelength and delay lines are represented by Φ and δ respectively. These blocks can be designed to terminate with 50Ω ports but co-designing some of them can reduce circuit complexity and improve performance such as PAE [43]. This could be done by tuning the variables with computer aided design tools. The paths for analyses are shown with the individual branches in series while the power divider is a parallel block. The following sections briefly introduce the individual blocks and the simplified models used for the complexity analysis.

2.3.1 Complexity Models of DPA Blocks

The M/N are to minimize standing waves and to increase the transfer of power from input to the output of the DPA. It is also one of the sources of the complexity. Figure 2.6 shows the possible variations in the M/N for the building blocks. In any conventional M/N, it can be represented by discrete components, T-line or a hybrid approach. For a LC network, there are two parameters to vary but for a full transmission line network, we have four parameters to optimize. The hybrid approach reduces area of the chip as a capacitor can replace the second transmission line. The complexity number $C_{M/N}$ depends on the total number of variables for the matching network.

Figure 2.6: (a) Discrete Model M/N, (b) T-Line Model M/N, (c) Hybrid Model M/N

For the purpose of the model, we will only consider the input port and the ports connected to branches of the carrier and auxiliary PAs. The ports with resistors are not involved in the calculations as they have predefined resistances to attenuate reflections. Examples of passive ports used in our analyses of two-way and three-way DPAs are illustrated in Figures 2.7 and 2.8 respectively. For example, a six-port power divider is used but we classify it as a four-port network to analyze. We model the complexity number by the number of S-Parameters. The different types of transistors and the different designs of PA architecture in the DPA are chosen by designers to fulfill the output power, PAE, linearity and gain. With the variety of parameters for transistors such as process, technology, sizes, types, operating voltages and current density, we simplify the complexity analysis and adopt the traditional two-port network S-Parameters. This provides a degree of freedom to choose a PA before analyzing the complexity of the DPA architecture in our case study.

Figure 2.7: Four-Port Power Splitter for Two-Way DPA

Figure 2.8: Six-Port Power Splitter for Three-Way DPA

2.3.2 Proposed Complexity Factor For DPA Architecture

For a design with higher complexity, a deduction can be made that the optimization time will be longer whether done manually or by optimization software. Consider a two-way conventional DPA, it is observed that it could be broken down into three sub-blocks which are the power divider, the main and auxiliary PA branches. As the power divider and the PAs can be designed as standalones before the integration, complexities with their S-Parameters can be quantified. For a two-way DPA, two output and one input ports are utilized for the power divider. Extending to a three-way DPA, three output and one input ports will be used. A conventional two-port PA would have four S-parameters and an equation can be derived to extend to multi-port PA. Therefore, the complexity numbers for the power divider and PA are

$$C_{PD} = (n + 1)^2 \quad (2.2)$$

$$C_{PA} = (n^2)^\gamma \quad (2.3)$$

where n is the number of ports in use for the power divider and the PAs in (2.2) and (2.3) respectively and γ is the number of stages of PA cascaded in the branch. For a conventional T-line, two parameters which are the width and length can be optimized for the required impedance and phase shift. A discrete passive element would have only its inductance or capacitance. The complexity numbers of input and output matching networks and delay lines shown in (2.4) and (2.5) respectively for a path can thus be represented by

$$C_{M/N,i/o} = (2n_{tl} + n_{de}) \quad (2.4)$$

$$C_{\sigma} = \alpha\sigma \quad (2.5)$$

$\alpha = 2$ for T-line model

$\alpha = 3$ for discrete model

where σ is the number of delay lines and phase shifters, n_{tl} is the number of T-line elements and n_{de} is the number of discrete elements in the matching circuit blocks. For the main and auxiliary branches, where the number of auxiliary branches can be increased up till the $(n - 1)^{th}$ branch depending on design and application, the complexity number for each of the branch can be represented by a product of the building blocks' complexity numbers as calculated by

$$C_{M,A} = C_{PA} C_{M/N,i} C_{M/N,o} C_{\sigma} \quad (2.6)$$

For a given N-way DPA, the complexity numbers of the individual parallel branches are summed up and then multiplied by the complexity number of the power divider in series. As the 50 Ω impedance transformer is common for most DPA designs, it was excluded from the formulation. If a DPA is designed in a way that allows it to

omit the impedance transformer at the output, the equation would still apply. The CF of an N-way DPA is then formulated to be

$$CF = C_{PD}(\alpha^{n-2}C_M + \sum_{i=2}^n \alpha^{n-i} C_{A_{i-1}}), n \geq 2 \quad (2.7)$$

Equation (2.7) can be applied on designs of DPA to quantify their complexities. After which, the values would be normalized by a figure depending on the type of passive components of the DPA design. By designing the basic DPA with the simplest L-type matching network together with a one stage two-ports PA in each branch, the CF of two-way DPA for the different types of passive components used in the circuits can be deduced. The numbers have been calculated and shown in Table I and Table II. For example, if a reported two-way DPA design with passive discrete components has a CF of 3556, it would have a NCF of 2. The NCF can be applied to an N-way DPA depending on the applications and designs but the prevalent designs currently are limited to mostly 3-way DPA.

Table I Base Figures For Normalization

DPA Blocks	Complexity Variables	Complexity Number		
		Discrete Passives	T-Line Passives	Hybrid Passives
Power Divider	C_{PD}	9	9	9
Main Branch	C_{PA}	4	4	4
	$C_{M/N,i}$	2	4	3
	$C_{M/N,o}$	2	4	3
	C_{δ}	6	4	4
	C_M	96	256	144
Auxiliary Branch	C_{PA}	4	4	4
	$C_{M/N,i}$	2	4	3
	$C_{M/N,o}$	2	4	3
	C_{δ}	6	4	4
	C_A	96	256	144
	CF	1728	4608	2592

Table II Complexity Factor For Conventional DPA Designs

Types of Passive Components	Complexity Factor
Discrete	1728
T-Line	4608
Hybrid	2592

2.3.3 Experimental Results And Discussions

In this case study of DPA, one of the ways performance is quantified is by the PA FoM, which was developed in 2005 by the International Roadmap for Devices and Systems (ITRS) for PA design. It includes the critical aspects of its performance and considers the gain roll-off at high frequency of operation.

The PA FoM is calculated by

$$PA\ FoM = P_{out} * G * PAE * f^2 \quad (2.8)$$

where the P_{out} is output power or saturated power, G is gain, PAE is power added efficiency and f is frequency of operation in GHz. The NCF together with the PA

Table III Reported DPAs With PA FoM And Normalized Complexity Factor

Freq [GHz]	P _{sat} [dBm]	PAE [%]	G [dB]	NCF	PA FoM	Ref
1.55	42	58.4	14	8.4	558.9	[44]
1.95	33	48.5	12.2	1.3	61.1	[45]
2.0	43	55.8	12	4.4	705.6	[46]
2.0	42	50.3	11*	6.4	401.2	[40]
2.14	33*	74	10.5*	1.0	76	[36]
2.14	41.2	56.2	19.7	1.0	3166.4	[47]
2.14	42	58.3	16.5	0.4	1890.2	[41]
2.14	46	72.5	12	6.0	2094.9	[48]
2.14	50.5	40*	10	2.3	2055.4	[49]
2.4	25	61.3*	25	10	353.3	[50]
2.6	44	61.2*	18*	0.9	6555.6	[51]
2.65	42*	46.3	16*	0.5	1629.0	[52]
3.3	43	45.0*	12.5*	16.7	1739.1	[38]
4.9	44.5	60*	11*	9.2	5111.4	[53]
5.5	20	34.2*	10	1.17	10.3	[54]
7.65	35	43*	9*	0.8	632.1	[55]
25.8	25.1	16.5	7	2.0	178.1	[56]
29.5	27.8	38	10.5	6.1	2235.8	[57]
45	18	21	8	3.0	169.3	[58]

*Values are estimated from graphs or calculated from gain and drain efficiencies

FoM provide a quick assessment on the performance limitation of DPA, which can also be extended to other circuit components applying this complexity analysis. The NCF itself is a FoM that can be complemented with the PA FoM but not to replace it. It is a function of parameters such as number of passive elements, topology of circuits and circuit design techniques as opposed to PA FoM, which are parameters of the PA results such as power, gain and PAE.

Figure 2.9: PA FoM and Normalised Complexity Factor Plot. Designs with High PA FoM and Low NCF are Preferred

Applying the formulas of the proposed NCF and PA FoM on reported DPAs as shown in Table III, the scatter plot of PA FoM against NCF as shown in Figure 2.9 was derived. A design which ideally has low NCF and high PA FoM is what designers would need to achieve to work towards to and it should warrant a higher tendency of adoption as the design cycle time would be reduced as well as achieving good performances overall. A general diagram of such a matrix can be seen in

Figure 2.10, where the dividing lines for the four sections are arbitrary and are not shown. They can be trained and determined as the mean after collecting hundreds to thousands of data.

Figure 2.10: Classification of Regions for Complexity-Aware Circuit Design

The plot in Figure 2.9 could be used as a benchmarking tool for designers to decide whether the design is comparable to the state-of-the-art DPA and whether to adopt a higher PA FoM design based on the calculated NCF or to continue to develop the current design.

With about 19 data from DPA designs due to limited published works with transparent circuit designs and the difficulty in designing and fabricating circuits at the millimeter-wave spectrum, the model was simulated by classifying the frequencies of operations into three frequency bands which are ultra-high frequency

Figure 2.11: Plot of Average Gain Against Normalized CF For Different Applications. One-Way ANOVA At 90% Confidence Level With Statistical Significant Difference

(UHF), super high frequency (SHF) and extremely high frequency (EHF) meant for mobile phones, satellite links or wireless communication and remote sensing applications respectively. However, due to insufficient data for EHF DPA designs and for the sake of discussion, they are omitted from the graphs. The data of average gain, peak PAE and P_{sat} are plotted against the NCF in Figures 2.11, 2.12 and 2.13, with Figure 2.11 suggesting that decreasing the NCF by about 400% from 8 to 2 could possibly increase the average gain of the DPA designed by up to 40%. This further suggests that designs which are targeting for gain should have their DPA NCF to be below 2. Designs which fall into the group of $0 < \text{NCF} < 2$ are using techniques which are mostly employing merged passive components to reduce the area as well as number of passive elements in the circuit. This could possibly lead to the reduction of cost of production and design time due to the smaller area. Substituting Equation (2.4) into (2.6) with the other parameters as constants would

result in complexity number of the branches directly proportional to the number of passive elements. It could be deduced that the complexity number would decrease with the decrease in the number of passive elements. The reduced number of passive elements could also be one of the reasons that the average gain could be higher compared to published DPA designs with $2 \leq \text{NCF} < 8$ as they have inherent insertion losses which could reduce the overall gain of the DPA.

For SHF applications, the increased in NCF does not contribute to a significant drop in average gain as suggested in Figure 2.11. This shows that for SHF applications, to design DPA for gain, designs should target the region of $0 < \text{NCF} < 2$. The separate groups of specific designs circled for UHF and SHF are not feasible if design time and hence complexity, is an important factor for the designers who are designing for gain enhancement. Employing multiple harmonic tunings done by Steffen et al. [53] could reach a gain of 11dB for SHF applications but at the expense of a high NCF. On the other hand, a cascading design as demonstrated by J. Kang et al. [50] might enhance the gain significantly but the designer has to weigh the trade-off with an NCF of about 10.

Figure 2.12: Plot of Average P_{sat} Against Normalized CF For Different Applications

Figure 2.13: Plot of Average PAE Against Normalized CF For Different Applications

A few stages of PAs could be cascaded but it would lead to an exponential increase in complexity of the main and auxiliary branches as shown in Equations (2.3) and (2.6), leading to possibly larger area of the chip and longer time to design and optimize. Designing with multiple harmonic tunings could lead to a high PAE and gain for SHF applications. However, this results in a very high NCF of more than 8. It might increase the cost of manufacturing as the number of passive components used in the design increases due to the increase in the NCF.

By comparing the initial gain of the designs for UHF or SHF applications with a plot such as in Figure 2.11, if the gain of the design is more than the average gain, designers could choose to continue with the development. However, if it is lower, the designers could instead, adopt published designs and reduce the overall design time to meet the TTM. Designers designing for gain and targeting UHF applications utilizing silicon processes for example could opt for designs which rely on merging passive components to reduce the complexity and the insertion losses due to the reduction in the number of passive network elements. A similar approach and

analysis can be applied by designers who are targeting for other parameters such as PAE and P_{sat} , which have their average values plotted against NCF for the different applications in Figures 2.12 and 2.13. As a quick initial observation, the average PAE for example, does not differ by more than 5% for UHF applications. This probably suggests that a designer is able to choose the DPA design with the lowest complexity in the $0 < x < 2$ range if he or she is targeting for PAE. This model and methodology could be implemented by foundries, which could potentially allow a scalable benchmarking database for circuit designers to differentiate their designs with current state-of-the-art, allowing quick evaluation of the efforts required to adopt new circuit design techniques. One other current potential application could be to couple with algorithm to design DPA such as one demonstrated by Chenyu Liang et al. [59]. It could possibly improve the 95 seconds of production time for a functional DPA prototype with a Linux workstation and pave ways for new applications.

2.4 Summary

In this chapter, a methodology to characterize and analyze architecture complexity of circuits is proposed. Design teams could leverage on the presented methodology to identify and differentiate architecture which would thereafter be adopted to meet overall design targets such as RF circuit performance. As an illustration, the presented methodology was used to analyze the architecture complexity of DPA circuits, in which an example objective, that is, gain optimization, was chosen. The relationship of NCF versus gain was discussed and practical design implications of this relationship were explored in detail. The use of this methodology could potentially be adopted for any circuit design and any aspect of circuit performance.

The adoption of such a methodology may open up novel design approaches contributing to improvements to future circuit design.

CHAPTER 3

Topology Complexity

3.1 Background

In the previous chapter, complexity analysis was introduced for the consideration of architecture complexity. However, the details of the PA blocks are treated as a black box due to the many parameters involved and this chapter will address the design intricacies involved with the PA block design from the point of view of topology complexity. As one of the few active components in the DPA, the classes of PA have often been exploited in the PA blocks to improve the performance of the DPA [10, 60, 61], particularly the PAE. The efficiency of the DPA, being one of the matrices for PA performance, largely depends on the efficiency capabilities of the individual main and auxiliary PA [62]. As such, switching PAs such as Class D onwards are often explored as a single transistor implementation with harmonic tunings to enhance the efficiency. Chaoyi Huang et al. [10] presented a Class-J DPA with an integrated second harmonic tuning networks at both the outputs of the main and auxiliary PAs as shown in Figure 3.1. The second harmonic matching was done on top of the fundamental frequency tuning as it had been determined that second

harmonic termination significantly affects the performance of their design more than the third harmonic matching based on their simulation results as seen in Figure 3.2. The deltas for a step of 5% for efficiency and 0.5dBm are significant for the PA.

Figure 3.1: Block Diagram Of Second Harmonic Tunings of DPA [10]

Figure 3.2: Simulated Load-Pull Contours of Efficiency (Red) and Output Power (Green) For Second Harmonic (Left) And Third Harmonic (Right) [10]

In terms of switching PAs, which are also known as the non-linear PAs, there are the Classes D, E and F. Envelope tracking power amplifiers (ETPA) such as Class G for example, will also be discussed and investigated in the subsequent sub-chapters

3.1.1 Single Transistor PA Topology

For a single transistor PA as seen in Figure 3.3, the variables of the PA design are reduced. However, employing harmonic tunings by using more passive components and demonstrated in the previous chapter, the CF of the DPA will increase due to the number of passive components involved in the M/N, resulting in a more complex design.

Figure 3.3: A Conventional Single Transistor PA

By using single transistor in its most basic form as a PA, one of the ways topology can be classified is by classes of PA. The common ones are Classes A, B, AB, C, D, E and F. Those with variation of power supply rails such as Class G will be treated in the next section as ETPA.

Classes A to C PAs have similar architecture such as that shown in Figure 3.3 in general and they can be distinguished by their biasing conditions or by their conduction angle; time in which they are switched on in a period. Class A is the most linear of them as the output signal follows that of the input signal with the least distortion, which is obtained at the expense of power losses. However, as it is turned on 100% of the time, it results in low efficiency. To improve the efficiency with a trade-off in linearity, the conduction angle is reduced by biasing the FET with a lower quiescent current so that the input RF signal will aid in turning on the FET for a smaller part of the duty cycle.

As technology scales, for a single transistor, the supply voltage is gradually scaled from 2.4V to 1.2V and even 1V. By using Equations 3.1 and 3.2

$$P_{out} = \frac{V_{DD}^2}{2R_L} \quad (3.1)$$

$$P_{dBm} = 10 \log_{10} \left(\frac{P_{mW}}{1mW} \right) \quad (3.2)$$

We can calculate that the ideal maximum output powers that can be delivered to a 50Ω load are 17dBm, 11.6dbM and 10dBm respectively. Most applications are looking close to 20dBm and even watt-level of 30dBm. As such, impedance transformation or power combining techniques will definitely be needed for a single transistor PA topology. In practical cases, due to parasitic losses, this will pose even a greater challenge to designers to design the PA block for the DPA in this example. Table IV shows the summary of Class A to C PAs.

Table IV Summary Of Conduction Angle And Maximum Drain Efficiency For PA

PA Class	Conduction Angle	Maximum Drain Efficiency
A	$\theta = 2\pi$	50%
B	$\theta = \pi$	78%
AB	$\pi < \theta < 2\pi$	$50\% < \eta < 78\%$
C	$\theta < \pi$	100%

Class A to C PA employed the devices as current controlled sources while Class D, E and F are using the devices as PA switches instead. Ideal switch has no power dissipation during the off-state as zero current flows through it and it has no potential difference across it when it is being turned on. This would result in the current and voltage-time signals not overlapping, which ideally would enable it to achieve 100% efficiency. Class D PA as shown in Figure 3.4, cannot be used by itself if the designer wants a linear PA. Due to the finite switching speed of practical transistor, it causes the FET to stay in the active regions when current is conducting. Class D PA acts as a voltage controlled switch and a series filter tank made up of L_1 and C_1 are chosen which follows Equation 3.3

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (3.3)$$

where the values of L_1 and C_1 are chosen so that at resonance, there is negligible impedance and fundamental signal will see it as a ‘short’.

Figure 3.4: Conventional Class D PA Architecture

On the other hand, Class E and F PA shown in Figure 3.5 and 3.6 utilize harmonic tuning to resonate out the parasitic drain-source capacitance so as to minimize the overlapping of the current and voltage waveforms which would result in output power loss. It is worth to note that a trend to design the auxiliary PA of the DPA using Class E [63-65] is arising but there are still on-going research works [66].

As Class E PA incorporates the parasitic capacitance into the design of the load network and still utilizes a single transistor topology to reduce complexity without more than one resonant LC tank, a 2.4 GHz transformer Class E PA shown in Figure 3.7 was investigated, designed and implemented on GLOBALFOUNDRIES 65nm CMOS process for the feasibility of a low complexity topology to be implemented for DPA.

Figure 3.5: A Conventional Class E PA

Figure 3.6: A Conventional Class F PA

Figure 3.7: 2.4GHz Transformer Class E PA Design

A conventional Class E uses RF choke as the DC_{Feed} for L_{DC} shown in Figure 3.7. However, this will bring the voltage swing across the FET to be about 4 times that of V_{DD} as shown in Equation 3.4 [67] given by

$$V_{DSmax} = 2\pi \left[\frac{\pi}{2} - \arctan\left(\frac{\pi}{2}\right) \right] V_{DD} \approx 3.6V_{DD} \quad (3.4)$$

By designing with a finite inductor, the peak voltage can be brought down to $2.5V_{DD}$ [68]. The benefits are multiple folds as it not only helps to reduce the peak voltage swing but also by simplifying the design of the matching network.

The values of C_1 , L_x and R_L can be derived from Equations 3.5 to 3.7 [69]

$$C_1 = \frac{0.1836}{\omega R_L} \quad (3.5)$$

$$R_L = 0.5768 \frac{V_{DD}^2}{P_{out}} \quad (3.6)$$

$$L_x = 1.152 \frac{R_L}{\omega} \quad (3.7)$$

where $\omega = 2\pi f$ and $f = 2.4 \text{ GHz}$. P_{out} is the output power and V_{DD} is the supply voltage. C_2 and L_2 are selected to be 12.88 pF and 0.34 nH respectively to design the series harmonic tuner at 2.4 GHz . The microphotograph of the PA is as shown in Figure 3.8.

Figure 3.8: Microphotograph of Implemented 2.4 GHz Class E PA

The chip measures an area of $0.49 \times 0.43 \text{ mm}^2$ including bondpads. The results of the simulated and measured Class E PA are as shown in Figure 3.9.

Figure 3.9: Simulation And Measurement Results Of Class E PA

Keysight spectrum analyzer and Cascade Microtech probe station were used for the measurement. At 1.2V of supply voltage, the DE and PAE are approximately 60 to 70%, which could be a good candidate to replace Class C PA in a DPA. However, considering that the output power achieved with a single transistor topology shown in this investigation is around 10dBm, a cascode or stacked PA topology could be a better candidate to raise the output power by a few folds. This is needed to achieve a near watt-level PA design for 2.4GHz while keeping the complexity at a manageable level. The difference in efficiency is largely due to parasitic effects mismatched during simulation and measurement [70]. The bondpads could also have been accounted for in the EM modelling using HFSS.

3.1.2 Envelope Tracking PA Topology

As DPA is known for improving the PAE at back-off power levels, the topology for the main and auxiliary PA can be improved and further implemented with ETPA. This could come in the form of Class G or H PA for discrete level ET or continuous level ET respectively. Class G PA employs discrete power supply switching to decrease the PA power consumption and hence increase its efficiency whereas Class H PA uses the input signal to modulate the power supply to provide just sufficient voltage supply for optimizing of efficiency. Switching or non-linear PA's efficiency is dependent on the correlation of the output power and the maximum output power [71]. The closer they are, the higher the efficiency of the PA.

It has been demonstrated that a general Class G PA in Figure 3.10 using dual supply rails can enhance the efficiency at back-off power levels seen in Figure 3.11.

Figure 3.10: Block Diagram Of Class G PA

Figure 3.11: Efficiency Vs Normalized Vout for Single Supply PA and Class G Dual Supply PA [71]

However, due to the discrete switching, it causes the abrupt discontinuity in efficiency as observed in Figure 3.11. However, linearity is degraded due to the dependency of gain and phase with the supply voltages. Hence, digital predistortion could be needed [72]. Yoo et al. [73, 74] proposed a digitally-controlled switched-capacitor RF PA (SCPA) with Class G architecture to further increase linearity and efficiency as shown in Figure 3.12. However, their output matching network, which could be a source of power losses, parasitics and complexity of design, was done off-chip to reduce the die area.

Figure 3.12: Efficiency Vs Normalized For SCPA Class G and Conventional Class G PA

As mentioned earlier that DPA could be used to improved back-off power level efficiency due to load modulation and since Class G PA demonstrated improved efficiency due to multiple supply voltages switching, DPA implementing Class G research works had been done [75-77]. Hu et al. [77] demonstrated that the hybrid Class G Doherty had a drain efficiency improvement of about 1.5x to 2x for 6dB and 12dB power back-off respectively compared to a static supply Doherty at 3.7GHz. However, the daunting complexity of the mixed-signal CMOS PA has a way to go to reduce complexity as their work is at the proof-of-concept stage.

3.1.3 Cascode/Stacking PA Topology

A contender for PA topology for DPA is the cascode structure as seen in Figure 3.13. The low drain-to-source breakdown voltage of a SGNFET reduces the maximum output power swing and the overall efficiency of RF PAs. Hence, to increase the output power of the PAs, a cascode topology PA can be employed as

the output power delivered to the load. A cascode topology differs from stacking in which the FETs at the top are common ground while stacking FETs have supply voltages biased to the gates.

Figure 3.13: A Conventional PA Cascode Topology [68]

The SGNFETs are arranged in a cascode arrangement such that the DC voltage drop can be distributed equally or in a ratio across the two transistors, depending on the circuit designer. This would enable a higher V_{DD} to be supplied to this PA topology and thus, allowing a higher output power to be achieved theoretically. However, a PA needs to be operated under a large signal operation and the voltage swing across the drain-source of M2 would be larger than across the drain-source of M1 [78]. This prompted the research community to optimize the cascode PA such that M1 can be selected as a SGNFET with better RF performance while M2 is typically a thick-gate FET to absorb the higher voltage swing. As the latter does not have the RF performance standard as M1, the overall performance of the PA would be

limited by the thick-gate FET. However, a self-biasing scheme [79] could allow both the transistors to experience the same maximum drain to gate voltage swings, thus enabling SGNFET to be used as the two transistors, providing better RF performance.

As technology scaling also scales down the supply voltage and increasing the unity current gain of the transistors (f_T), research works have been challenged to employ the cascode design topology at higher frequency bands of DPA designs which typically increase the output power to meet their specifications as shown in [28, 80], both of which achieved a P_{sat} of 13.2dBm and 7.8dBm respectively, with differences owing to their designs as well as the technology of the transistors among many other factors such as the foundries' process recipes et cetera. However, there are also designs which pushed to the limits of 4-stacked FETs [81] to improve the performance but at the same time, increased the complexity of the PA design.

In recent years, there has been an increased in adoption of CMOS silicon-on-insulator (SOI) for PAs [82-84]. As mentioned in Chapter 1, disadvantages of silicon processes such as inherent low gain, silicon substrate losses and low drain source breakdown voltages of transistors have allowed most of the PA designs today based on gallium arsenide (GaAs) MESFET or silicon germanium (SiGe) HBT processes shown in Figure 3.14 and 3.15 respectively. However, with innovations happening at a rapid pace and for ease of integration, CMOS SOI PA is a viable alternative due to a simplified process shown in Figure 3.16, with better device isolation and lower parasitic capacitance, enabling the design and integration of PA modules for SOI processes to be an attractive solution.

Figure 3.14: Simplified Cross-Sectional View Of GaAs MESFET Process

Figure 3.15: Simplified Cross-Sectional View Of SiGe HBT Process

Figure 3.16: Simplified Cross-Sectional View Of SOI CMOS Process

3.2 Motivation

For the consideration of topology complexity, a PA with low complexity coupled with a good balance of linearity and efficiency need to be maintained and the conventional operation of Class AB as the main PA and Class C as the auxiliary PA would sometimes be preferred due to its simplicity. In the previous subchapter, it has been shown that a 4-stacked PA topology or its simple counterpart as a 2-stacked can boost the output power of the PA and hence, the DPA. To potentially reach high output power at higher frequency of operations for high power applications, a stacking design can be chosen. With the CF analysis, a cascade structure shown in [85] will increase the complexity due to interstage matching

networks. Hence a cascode or stacking design would be preferred for the works of a reduced complexity DPA to reach higher output power. However, among the different N-stacked topologies, there is a need to select the lowest number of stacked topology to improve the circuit design cycle. A comparison of two designs utilizing the same process technology of a 2-stacked HVFET+SGNFET and a 4-stacked SGNFET topologies in SOI process with both of them having comparable performance could suggest that designing using a 2-stacked HVFET+SGNFET reduces the complexity of the PA block itself and hence reduces the design time, chip area and cost of manufacturing for the DPA.

3.3 Contributions

Kink effects in SOI devices shown in Figure 3.17 have been well studied by research works and one of the reasons is mainly due to high R_{body} of the body contacts on conventional SOI processes. However, research work had been done by R. T. Toh et al. [86] to optimize and mitigate this issue. Further discussion of the kink effects is beyond the scope of this thesis.

Figure 3.17: Typical Issue Of Kinks Observed In Id-Vd Of SOI Device

Figure 3.18: I_d - V_d Of SOI SGNFET With Onset Of Parasitic NPN Breakdown In Red Circle

Even with the kink effects eliminated from the process point of view, the parasitic NPN breakdown of the FETs is still present and inherent for the SGNFETs. An I_d - V_d characteristics plot in Figure 3.18 shows the performance of a SGNFET for PA biasing points. Further-more, pulse width was varied from DC to 100ns as shown in Figure 3.19 with the gate voltage biased slightly above the threshold voltage [87]. This shows that the kink regions are prominent for the different pulses and even DC voltages. We also measured the dynamic load lines as shown in Figure 3.20. There is a shift of approximately 20-40% of the dynamic load line when biased near the kink region of V_d 1.4V and it can be demonstrated that the degradation of efficiency would be more detrimental beyond this region as seen in Figure 3.21.

Figure 3.19: Id-Vd Of SGNFET With Different Pulse Widths At $V_g=0.75V$ [87]

Figure 3.20: Dynamic Load Lines Of PA Designed With SGNFET. Large Shift In Dynamic Load Line For $V_d=1.4V$

Figure 3.21: PAE Curves Of Various Vd Biasing Of SGNFET. Drops In PAE Are Visible

3.3.1 Adopted Stacked Topology

As mentioned in Chapter 3.1, a cascode or stacked topology could increase the output power of the PA as it allows the increase of the supply voltage V_{dd} of the PA. A 4-stacked resistor-ladder SGNFET topology as illustrated in Figure 3.22 was investigated and adopted. During operation, the voltage swings are not proportional across the 4 FETs with the top most FET absorbing most of the voltage swing across the entire PA. Since from the previous subchapter, the nominal biasing voltage across the drain-source has to be kept within 1.4V to 1.5V, the V_{dd} of the entire 4-stacked resistor-ladder PA has to be determined to be 3V to take into account the voltage swings during AC operation. The biasing circuits are designed in a way so as to reduce the chip size with lesser number of bond pads involved. They are also necessary to improve the stability of the circuit by adding some resistive losses to the input of the SGNFETs and to act as potential divider to allow the SGNFETs to be in saturation during operation.

Figure 3.22: Adopted Resistor-Ladder 4-Stacked SGNFET Topology

The drain inductor and gate resistor R_G are part of the components of the external tee-bias circuit. The stacked resistor-ladder biasing adopted for this topology is as shown in Figure 3.22. Common source input SGNFET M_T is stacked with 3 SGNFETs M_1 to M_3 . The gates of the stacked FETs are not grounded but instead, biased with external capacitors of C_1 to C_3 to result in a capacitive potential divider to allow in-phase voltage swing at the drain and gate of each SGNFET, which would reduce the V_{gd} and V_{ds} swings under large signal operations [88]. As shown in Figure 3.23, the source input impedance $Z_{s,n}$ of each SGNFET is affected by the value of the external capacitor according to Equation 3.8

Figure 3.23: Simplified Small Signal Model of SGNFET

$$\begin{aligned}
 Z_{s,n} &= \left(1 + \frac{C_{gs}}{C_n}\right) \left(\frac{1}{g_m} \parallel \frac{1}{sC_{gs}}\right) \\
 &\approx \left(\frac{C_{gs} + C_n}{C_n}\right) \left(\frac{1}{g_m + sC_{gs}}\right)
 \end{aligned} \tag{3.8}$$

Stacking the 4 SGNFETs will yield an overall small-signal voltage gain that can be derived to be shown in Equation 3.9

$$A_v = \frac{g_{mt} R_{load}}{\left(1 + \frac{sC_{gs1}}{g_{m1}}\right) \left(1 + \frac{sC_{gs2}}{g_{m2}}\right) \left(1 + \frac{sC_{gs3}}{g_{m3}}\right)} \tag{3.9}$$

Each SGNFET is designed with a total gatewidth of $800\mu m$ with a fingerwidth of $8\mu m$. Capacitors C_1 to C_3 are set to obtain the highest PAE and gain of the stacked PA. Resistors R_1 to R_3 are 400, 200 and 200Ω respectively. To allow flexible biasing of the gate voltages of the stacked SGNFETs, the voltage is not tapped from the drain supply voltage. The gate voltage of M_T is not incorporated with the

resistor ladder potential divider and it was adjusted separately to improve the performance. Furthermore, there are 3 DC probes from the measurement tool that can be used. The load-pull is done from the measurement tool to obtain the performance results which are to be elaborated in the next sub-section.

3.3.2 Experimental Results And Discussions

The simulated output impedance of optimal output power for the adopted resistor-ladder 4-stacked SGNFETs topology is approximately $43.4+j124.1 \, \Omega$ as seen in the smith chart from Figure 3.24 as a purple cross. The power contours for the other power levels are shown but they are not of interest for this design. The higher Z_{opt} is owing to the stacked configuration where the Z_{opt} at the drain of the top 3 FETs follows the equation of

$$Z_{opt,drain} = \sum_{i=1}^n Z_{opt,i}, n = 3 \quad (3.10)$$

Figure 3.24: Smith Chart Of Z_{opt} for Output Power

Based on the smith chart, as the purpose is to simply have high output power but at the same time, reduce the complexity of the circuits, a simple L-type M/N is chosen and designed for the output and input M/N respectively for maximum power transfer from the input to the output of the PA. By varying the input power to the PA, the simulated results of gain and PAE against output power sweep can be seen from Figure 3.25.

Figure 3.25: Simulated Power Sweep Of Cascode Resistor-Ladder 4-Stacked Topology

The saturated output power is approximately 19dBm with a stable 35dB of gain over a range of 15dB of output power and a peak PAE of about 67%. At the peak PAE, the gain dropped to about 20dB as the P_{1dB} point has been reached at around 15dBm, where the gain starts to compress after that point and any increase in input power will cause a smaller increase in output power until it saturates. We designed the chip on a 0.13 μ m radio frequency silicon-on-insulator (RFSOI) process with the layout as seen in Figure 3.26. The layout was designed to be as compact as possible to reduce the parasitic losses as much as possible from the routing of the devices

and pads. Spacing in the GSG pads are kept at $40\mu\text{m}$ for the tool to be able to probe during measurement.

Figure 3.26: Layout Of Proposed Design With GSG Pads and 1 Bond Pad

We set up the load-pull system for measurement with hardware and software from Focus Microwave as shown in Figure 3.27.

Figure 3.27: Focus Microwave Loadpull System Setup For Measurement

Figure 3.28: Measured Power Sweep Of Cascode Resistor-Ladder 4-Stacked Topology

Figure 3.29: Measured Gain And PAE Versus Input Power Plot

Figure 3.30: Measured Gain And Output Power Versus Input Power Plot

Tuners are multi-purpose tuner for adjusting 2nd and 3rd harmonics. The nonlinear vector network analyzer is for the large signals' waveforms and DC parametric for the DC signals. The tool sweeps varying loads to get the optimal output impedance followed by an input matching before recording the results which can be seen from Figures 3.28 and 3.29 for two variations of plots. The recorded P_{sat} is about 19dBm with 34dB stable power gain over 14dB and a peak PAE of approximately 60%. The recorded gain at peak PAE is approximately 29dB and the OP_{1dB} is approximately 14dBm shown in Figure 3.30. The small deltas in measurement and simulation results are most likely attributed to the parasitic inductance that could have been compensated for the routing between the FETs and especially from M3 to the V_{DD} supply pad shown in the microphotograph is Figure 3.31.

Figure 3.31: Microphotograph Of 4-Stacked PA

This effect will be more pronounced at higher frequency and should be taken into consideration.

As seen from the results, with SGNFETs forming the 4-stacked resistor-ladder, choosing of parameters for the impedance of each of the 4 FETs is further complicated by the characterization of devices needed to be done by the PA circuit designer for use in DPA. However, this stacked PA suffers a drawback of uneven voltage swings across the transistors due to the different impedance of each transistor at their inputs and for the 4-stacked PA, the drain-source voltage swing is the largest at the top-most FET as seen in Figure 3.32 reaching close to 1.2V and

precaution has to be taken to ensure that the DC and AC signals will not allow it to reach the parasitic NPN junction diode breakdown of the SGNFET.

Figure 3.32: Drain-Source Voltage Swings Of All 4 SGNFETs

If a designer wants to improve the output power handling of this 4-stacked PA, they can modify the design and substitute the SGNFETs with thick gate FETs as demonstrated by S.pornpromlikit et al. [89]

3.3.3 Proposed Comparison With Reduced Complexity Stacked Topology

In the previous subchapter, the 4-stacked SGNFET topology was investigated and adopted to deliver a high output power PA for the DPA block. However, we further compared it with another topology of a reduced complexity to deliver the approximate PA performance for the DPA block. This circuit was designed with load-pull measurement results and tapped on the performance of the industry available EDNFET on SOI process. The effects of EDNFET have been well studied and illustrated in [86, 87]. The excellent linear I-V characteristic until a DC supply voltage of 5V allows it to be a good candidate to replace the thick gate FET. The I_d - V_d graph of the standalone EDNFET optimized for PA applications is shown in Figure 3.33. The EDNFET to be used for the design does not have the presence of the kink effect as seen. The breakdown voltage ranges from approximately 8V at the on-state to 15V at the off-state, which allows the supply V_{dd} to be higher for the 2-stacked topology seen in Figure 3.34. As the EDNFET is to be used in a PA, the f_T/f_{max} performance is also measured as shown in Figure 3.35. The f_T of about 39GHz shown in Figure 3.35 theoretically allows the EDNFET to operate up to 3.9GHz as a rule of thumb for a standalone PA.

Figure 3.33: Id-Vd Sweep Of EDNFET Device Optimized For PA

Figure 3.34: 2-Stacked EDNFET And SGNFET Topology

Figure 3.35: f_T/f_{max} Sweep Of EDNFET Device

The ideal PAE of a PA factoring in the knee voltage is as shown in the equation:

$$\eta_{knee} = \left(\frac{V_{DC} - V_{knee}}{V_{DC}} \right) * \eta_{ideal} \quad (3.11)$$

For conventional silicon or SOI processes, stacking PA architecture allows the supply voltage to increase and hence increasing the output power. However, increasing the height leads to higher knee voltage which will reduce the PAE and at the same time increases the complexity of the PA architecture design. The EDNFET and SGNFET are sized to allow a quiescent current of approximately 30mA to reach the optimum f_i of the EDNFET. At the same time, the dynamic load line of the EDNFET is measured and shown in Figure 3.36.

Figure 3.36: Dynamic Load Line Of EDNFET at P_{1dB}

The dynamic load line of the EDNFET gave us a better understanding of how it should be biased before being stacked together with the SGNFET. At the P_{1dB} level, the output voltage can swing from about 1V to 9V with a gate biasing voltage of about 0.7V. Since the harmonics are still relatively small, the trajectories are almost shaped like an oval compared to higher output power levels, the shape will be much more distorted, depicting square-like waveform [90].

Since the dynamic load-line is inclined toward the vertical position rather than horizontal, it is consistent with a PA operation that is matched for gain instead for efficiency [91].

The voltage drop allowed across the EDNFET should be around three times lesser than the breakdown voltage of about 8V and the current swinging to the negative regime is due to parasitic effects in the transistor under AC signals. The width ratio of the EDNFET and SGNFET should be optimized for allowing the proper AC voltage swings at the respective drains of the two different devices. Proper biasing was done to ensure the V_{ds} of the SGNFET also does not reach the breakdown voltage during operation.

3.3.4 Experimental Results And Discussions

The PA is biased at 4V and the EDNFET of 1mm is first biased at 3.5V and 4.2V for safe operations by considering the breakdown voltage. The results demonstrate no negative effects at high V_{dd} operation for EDNFET. As the standalone EDNFET has a lower f_t compared to SGNFET, stacking it can improve the range of frequency and power of the PA overall. With the optimized width of the EDNFET and SGNFET, bulk of the voltage swing during saturation can be appeared across the EDNFET, which has a larger breakdown voltage. With a quiescent current of 30mA, the measurement results are shown in Figure 3.37. A P_{sat} of about 22dBm and OP_{1dB} is approximately 20.5dBm with a peak PAE of approximately 59% are recorded. The PAE is comparable to the 4-stacked cascode PA resistor-ladder designed.

Figure 3.37: Measured Power Sweep Of Cascode EDNFET And SGNFET

By employing this recommended 2-stacked EDNFET and SGNFET topology in a DPA design, the complexity of the DPA can be further reduced with enhanced output power of theoretically up to 25dBm with the DPA architecture. Table V compares the measured performance of both the adopted 4-stacked resistor-ladder SGNFET and 2-stacked EDNFET/SGNFET.

Table V Performance Summary Of Proposed Two Cascode Topologies

Topology	Gain (dB)	PAE @ P_{1dB} (%)	P_{sat} (dBm)	OP_{1dB} (dBm)
4-Stacked Resistor-Ladder SGNFET	34	50	19	14
2-Stacked EDNFET And SGNFET	17	55	22	20.5

As the EDNFET has inherently lower f_T , the overall gain would be lower for the 2-stacked cascode topology. However, the complexity is clearly reduced with the use of lesser devices in the 2-stacked EDNFET and SGNFET with comparable PAE and delivering almost twice the saturated output power at 22dBm. Ultimately, the EDNFET is supposed to absorb bulk of the voltage swing across the PA to enable it to handle higher output power. Compared to the 4-stacked resistor-ladder SGNFET, the gain of the 4-stacked would be amplified due to the use of 4 SGNFETs, delivering 19dBm of saturated output power, with a much higher number of devices and parameters to optimize before implementation.

3.4 Summary

In this chapter addressing the topology complexity issue, we first investigated and adopted a 4-stacked resistor-ladder SGNFET cascode topology for a high gain PA to be implemented in DPA architecture. The measured results are P_{sat} of 19dBm and peak PAE of 60%. A comparison is then made between the 4-stacked topology and a 2-stacked EDNFET and SGNFET topology with the latter achieving a comparable peak PAE of 59% and twice the P_{sat} at 22dBm. The PA block for the DPA needs to have a higher power handling capability and the EDNFET and SGNFET topology is able to let the DPA achieve a theoretical 25dBm of output power from the design, which is closer to 1W at 30dBm. With the 2-stacked topology delivering high output power and excellent PAE, it should be the preferred topology for PA implementation in DPA to reduce the overall complexity of the DPA from the topology complexity point of view.

CHAPTER 4

Discretional Complexity

4.1 Background

In the previous chapters, architecture complexity has been addressed and the topology complexity which detailed performance of the PA block in terms of gain, PAE and P_{sat} have been reviewed with the proposed 2-stacked EDNFET and SGNFET topology for reduced complexity compared to the 4-stacked SGNFETs with almost comparable PAE and better output power handling. In this chapter, the linearity aspect will be addressed for the discretional complexity to finish the DPA design flow with complexity considerations. DPA is again an architecture that has its performance limited by its individual sub-blocks. The linearity of the conventional DPA suffers due to the needed Class C PA at the auxiliary branch for turning on at the required power level for the DPA to operate. Certain PAs may not need to be linearized but if there is a need to, this discretionary complexity step is necessary for circuit designers. Linearization techniques have been employed on PA throughout the years to preserve the time-varying envelope of the signals due to modulation techniques that result in a high level of PAPR such as Orthogonal

Frequency Division Multiplexing (OFDM) [92, 93]. One big challenge facing circuit designers is the need to tackle the perennial trade-off between linearity and efficiency. An investigation on a typical Class A PA and a Class C PA illustrates this trade-off. Conventional Class A turns on all the time and the output will be able to follow its input, hence categorized as a linear power amplifier. However, the current is constantly flowing through the transistor, which reduces its efficiency. On the other hand, a conventional Class C PA only turns on when the input signal goes beyond the threshold voltage, which limits its linearity yet avoiding unnecessary power consumption as it turns off when input signal goes below the threshold level.

Some of the techniques for linearizing the PA blocks done by the research community suitable for PAs at the component level, involve feedforward [94-97], predistortion [98, 99], linear amplification with nonlinear components (LINC) [100, 101], envelope elimination and restoration [102-104] and third order intermodulation distortion cancellation [65, 105, 106] to enhance the linearity of the PA, which can be measured by parameters such as the output compression point (P_{1dB}) and the third-order intercept point (IP3) at the device or component level, error vector magnitude and adjacent channel power ratio (ACPR) at the system level. One of the simplest and straight-forward ways to achieve a highly linear operation is to operate the PA at the back-off region. However, this is not suitable for the DPA even though it does not add any complexity to the design as the DPA is designed in such a way that it operates at full output power load with enhanced back-off efficiency. In the next subsections, a quick overview of each linearization technique with its relevance to complexity and implementation for the PA block in the DPA will be given.

4.1.1 Feedforward Technique

In a typical feedforward system involving two loops, the distortion in red lines, is cancelled as shown in Figure 4.1. Minimal IP3 of 4dB improvement for a feedforward linearization can be achieved at 2.6GHz [107]. Their reported ACPR was also improved by about 12dB under 15MHz offset and -10dBm input power. At a higher frequency of operation, Alfonso et al [96] had demonstrated the effectiveness of feedforward linearization schemes near mm-wave frequencies. With phase mismatch of 10° to 100° between the two paths, the results could vary from ACPR improvement of 6dB to 25dB. Although feedforward linearization method improves the linearity of the power amplifier by employing phase delay circuits and an error amplifier, a very strict requirement is needed for an accurate cancellation. One of the limits for the system's efficiency will be the power consumed by the delay components [108, 109]. Designers have to minimize the delay insertion loss of the main path to enable higher efficiency performance. Phase mismatches between the two paths also have to be addressed in order to have better improvement. The complexity of the PA and hence, the DPA is also increased with the delay elements and the error amplifier.

Figure 4.1 Two Loops Feedforward System

Heungjae Choi et al had done work to truncate the use of a delay element to provide the efficiency enhancement [95]. They proposed their negative group-delay circuit to remove the necessary delay components required for the feedforward linearization. Yamauchi et al [110] also proposed an earlier work of the negative group-delay circuit to improve the efficiency of the system by 3%. However, the inherent complexity of the circuit remains as well as the usage of the very linear error amplifier which consumes a lot of power. An attenuator may be needed after the main PA to reduce the signal from the output. This attenuator will further increase the complexity of the PA blocks and the entire DPA

4.1.2 Predistortion Technique

A simple diode circuit can be used in front of a PA and with the right size and bias, the nonlinearity of the PA can be compensated. However, the linearity improvement is limited and does not work well at higher output power levels [111, 112]. Figure 4.2 shows the diode linearizer schematic [112]

Figure 4.2 Diode Linearizer

The non-linear resistor R_p is in parallel with the parasitic capacitance C . A forward biased diode will form a nonlinear RC phase shift circuit which initially will be biased to set both points to a starting small signal operation value. As input power increases, R_p decreases as the operating point is moving up the I/V characteristic curve. Since the change is non-linear, the resulting phase shift with increasing input power is non-linear as well. The S_{21} of the RC network is given as

$$S_{21} = \frac{2Z_0 Y}{1+2Z_0 Y} \quad (4.1)$$

where $Y = j\omega C + \frac{1}{R_p}$

Typical PAs exhibit a gain compression and upon looking at the S_{21} of the RC network, the gain expansion contributed by the diode circuit due to the decrease in R_p will compensate the nonlinear characteristics of the PA. The drawback is that the drive level has to be determined to overcome the small-signal insertion loss of the diode and the efficiency requirements. More complicated design and usage of a predistortion circuit can be seen in Figure 4.3.

Figure 4.3 Schematic Of Mirror Predistorter [113]

They claimed that by employing the low power PA in front of the main high-power PA, with its same distortion characteristics, the nonlinearities of the main PA can be replicated and cancelled at the output. They demonstrated an improvement of 23dB in third order inter-modulation distortion (IMD3) at a back off value of 7.5dB. However, this defeats the purpose of the general consensus that the predistortion circuits are easy to implement and simple. The mirror predistorter is a moderately complex circuit as it requires delay components, resulting in efforts needed to match the phase delay as well as the efficiency degradation seen in similar structure for feedforward schemes. At 60GHz, a built-in pre-distortion linearizer presented by Jeng-Han Tsai et al [99] demonstrated an improvement of 25dB for the IMD3 and the P_{1dB} and PAE have been doubled. It works by providing a gain expansion characteristic to the input of the stage which will counteract the gain compression. The effect will be cancelled and the linear region of the gain will be extended. This resulted in the reason that the 1dB gain expansion of the linearizer has to be equal to the 1dB gain compression point of the PA. As a linearization circuitry for the DPA, it is an addition of complexity to the circuit by adding of components.

4.1.3 Linear Amplification With Nonlinear Components

Cox introduced the linear amplification with LINC in 1974 [114]. The structure of LINC can be seen in Figure 4.4. LINC has the potential for applications with very high power efficiency without sacrificing its linearity [100]. The signal separator is the place where the concepts of LINC start.

Figure 4.4 Block Diagram Of LINC Linearizer

The principle of LINC is to resolve the amplitude modulation signal $S(t)$ into two constant envelopes with phase modulated signals $S1(t)$ and $S2(t)$ as shown

$$S(t) = r(t)[e^{i\phi(t)}] \quad (4.2)$$

$$r(t) = r_{max} \cos(\theta(t)) \quad (4.3)$$

$$S1(t) = \frac{r_{max}}{2} [e^{i(\phi(t) + \theta(t))}] \quad (4.4)$$

$$S2(t) = \frac{r_{max}}{2} [e^{i(\phi(t) - \theta(t))}] \quad (4.5)$$

$$\theta(t) = \arccos\left(\frac{r(t)}{r_{max}}\right) \quad (4.6)$$

where r_{max} is the maximum of $r(t)$, $\phi(t)$ is the phase of the baseband signal, $\theta(t)$ is the phase modulation angle given by equation 4.6. Assuming the gain of the two amplifiers are identical and represented by G , the outputs of the top and bottom PAs are $GS1(t)$ and $GS2(t)$ respectively.

Summing them up is given by

$$\text{Output} = G[S1(t) + S2(t)] = GS(t) \quad (4.7)$$

The constant envelopes or amplitudes seen in equations 4.4 and 4.5 means that these two signals can be amplified by non-linear amplifiers near their saturation points to provide the highest obtainable efficiency theoretically. After amplification, the signals can then be summed with a combiner to provide the output. Because the two input signals before the PA have constant amplitudes, no IMD will be created due to the non-linearity of the PAs, which demonstrates that LINC can be insensitive to PAs non-linearity [115]. Jingshi Yao et al [101] reiterated that in practical cases, the properties of the combiner is correlated to the efficiency of LINC and supported by Charles Baylis et al [116]. The combiner also plays an important role in determining the linearity of the LINC PAs depending on the output impedance matching [100]. Current designs are complex and they call for simpler LINC architectures, which are needed to overcome the flaws in linearization performance [117].

4.1.4 Envelope Elimination And Restoration

Kahn's technique or Envelope Elimination and Restoration (EER) technique [118] linearizes high efficiency but non-linear PA such as Class D or E suitable for the auxiliary PA of the DPA by modulating its supply voltage. The supply voltage is modulated by the envelope PA to reconstruct the waveform to be sent to the output as shown in Figure 4.5.

Figure 4.5 EER General Schematic

Modern techniques enabled the replacement of the envelope detector and limiter by a digital signal processor which generates the amplitude and phase waveforms from the in-phase and quadrature (I/Q) signals. The I and Q signals can be derived into the envelope and phase waveforms as follow

$$Env(t) = \sqrt{I(t)^2 + Q(t)^2} \quad (4.8)$$

$$\phi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \quad (4.9)$$

The envelope signal which consists of the amplitude is being pushed into the envelope PA whereas the constant amplitude phase signal is fed into the non-linear PA at the bottom branch. The non-linear PA only needs to amplify the phase signal and thus, it can be of very high efficiency. The envelope signal is used to modulate the drain node of the non-linear PA and hence, reconstruct the original input signal. It demonstrates the use of non-linear component for linear amplification. In theory, it can achieve 100% efficiency and the total system efficiency is calculated by [119]

$$\eta_{total} = \eta_{envelope\ PA} \cdot \eta_{non-linear\ PA} \quad (4.10)$$

Feipeng et al [119] compared their EER work with a class AB PA and the improvement of PAE is approximately doubled from 12.3% to 28%.

The phase matching between the two paths is also critical. Jeffrey et al [120] mentioned the delay mismatches between the envelope and phase paths is tolerable of only up to 4% of the symbol period while meeting some of the specifications for IEEE 802.11a. However, in view that the total system's efficiency is the product of the two PAs, any degradation of the envelope PA efficiency can offset any improvements in the efficiency contributed by the non-linear PA. Also, to further implement an efficient envelope PA that is able to track the entire envelope bandwidth is challenging. This increases the complexity of the whole design by a notch.

4.2 Motivation

Integrated RF/millimeter-wave transceivers have been designed in the recent years with the latest state of the art offering a maximum supported throughput of 4.6Gbps using SiGe 0.18 μ m BiCMOS process. The total power consumption for transmission mode is 718mW and that of the receiving mode is 939mW [121], which are unfortunately high. Hence, this necessitates additional research effort to reduce its power consumption by enhancing its efficiency and at the same time, the trade-off in linearity must also be addressed. DPA has been used for both efficiency-enhancement operation and to improve the linear range of the power amplifier [122]. The GaAs based DPA's simpler circuitry compared to other techniques also makes it a viable option. However, the DPA implemented using GaAs process does not

have a cost-efficiency advantage over silicon-based CMOS SoC design as mentioned in Chapter 1 of the thesis. It is due to efforts in overcoming the disadvantages of DPA designs in silicon-based processes that increase the complexity of the overall circuit. Linearization issues have been addressed in [123] but small signal gain achieved was only 7dB. It may not be a good idea to apply a post-distortion linearization technique as too much gain is sacrificed for the improvement in linearity as demonstrated in this work. In [124], a pre-distortion linearization technique utilizing diode linearizer is implemented. However, the drive level of the entire DPA has to be pre-determined to compensate for the loss due to the diode linearizer. The linearity improvement is also limited and does not work well at higher output power levels. These linearization techniques also added the unwanted hardware complexity for the DPA design. A proposed solution that can address the discretionary complexity is to enhance the linearity but at the same time, not adding more elements into the design to have the best of both worlds.

4.3 Contributions

The non-linearity of the power amplifiers produces third-order harmonics which distort output signals. Works have been done to cancel the gm3 to enhance linearity [125-127]. Instead of implementing an additional circuit to cancel the gm3 signal, we proposed a gm3 cancellation bias DPA scheme with a wideband 60GHz broadside coupler. The matching network was done with transmission lines and capacitors and a phase shifter was implemented to compensate the phase shift that some designs had not given much attention to but the phase difference is one of the most crucial parameters in a DPA design for the Doherty operation.

4.3.1 Proposed Broadside Coupler For DPA

In the proposed methodology to analyze the complexity of the DPA, the power divider at the input of the DPA has been treated with the S-Parameters as well. This subsection explores two types of power divider for the DPA as potential candidates. A Wilkinson power divider shown in Figure 4.6 consists of two quarter-wavelength lines and a resistor between the two output ports for isolation was being implemented in [37, 128, 129]. However, the area is one of the concerns for such a 90 degree power split. Works had also been done to enhance the bandwidth of the Wilkinson power divider by implementing an additional transmission line and a stub, effectively another section [130], and another which is designed with tapered transmission lines [131]. Thereafter, a 90-degree phase shifter can be used at the input of the peaking power amplifier. Directly implementing a 90-degree phase shift quadrature hybrid branch coupler was done [97, 132, 133]. The power split is achieved at the two output ports with one of the ports having a 90-degree phase lag as compared to the other port. These techniques increase the complexity involved with designing of the entire DPA.

Figure 4.6 Wilkinson Power Divider

We proposed using a broad-side coupler [134] shown in Figure 4.7 that allows a broader bandwidth design for a DPA. The very small gap of $0.6\mu\text{m}$ between the two different layers of metal use in the design enables an S21 and S31 to be about -4dB. For the use of a wideband 90-degree phase shift, the two metal layers used have to be of quarter-wavelength initially and they were then optimized. This technique taps on the technology of multi-layer IC design and can be proven to reduce the area [135], which will also help decrease the chip area of the final DPA.

Figure 4.7 Cross Section View of Designed Broadside Coupler

The broadside coupler is implemented using metal layers 7 and 8 of the 65nm CMOS process and the design was further optimized to ensure about 0.4dB of over-coupling shown in Figure 4.8 to compensate for any process deviation that will cause a shift in the results. The spread of the phase difference is also less than 2.2° from 57GHz to 66GHz which is only a 2.4% margin deviation.

Figure 4.8 S-Parameters And Phase Difference Plot Of Proposed Broadside Coupler

4.3.2 Proposed Gm3 Cancellation Bias For DPA

The block diagram of the DPA is shown in Figure 4.9. It consists of two branches of PAs with the main and auxiliary PAs biased to cancel the gm3 coefficient [136] by biasing in Class AB and Class C respectively at the specific voltages. The $\lambda/4$ line after the main PA is to enable the load modulation. The matching networks and the non-linearity of the transistors result in the phase shift of both branches. In order for the two branches to be 90 degrees out of phase, a phase shifter is designed and added to it. This results in an improved gain and PAE of the overall DPA with enhanced linearity.

Figure 4.9 Intrinsic Transconductance Cancellation Of DPA Design

The crux of the operation of DPA is at the output of the main PA, which is the $\lambda/4$ line to enable the load modulation. The equivalent circuit is shown in Figure 4.10.

From a two-dimension time and position perspective, the voltage and current waveforms along the lossless transmission line at any point in time is given by,

$$V(t, x) = V^+ \cos(\omega_0 t - \beta x) + V^- \cos(\omega_0 t + \beta x) \quad (4.11)$$

$$I(t, x) = \frac{V^+}{Z_0} \cos(\omega_0 t - \beta x) - \frac{V^-}{Z_0} \cos(\omega_0 t + \beta x) \quad (4.12)$$

The first terms represent a wave propagating in the positive x axis and the second terms represent a wave propagating in the negative x direction, phase constant β and Z_0 is the transmission line's characteristic impedance. With I_2 delayed by $\lambda/4$,

$$I_1 = I_0 \cos(\omega_0 t) \quad (4.13)$$

$$I_2 = -\alpha I_0 \sin(\omega_0 t) \quad (4.14)$$

where α is the relative fraction or ratio of the current in the peaking amplifier stage.

At a given time at position $x = 0$, equations 4.11 and 4.12 will be reduced to

$$V(t, 0) = (V^+ + V^-) \cos(\omega_0 t) = V_1 \quad (4.15)$$

$$I(t, 0) = \left(\frac{V^+}{Z_0} - \frac{V^-}{Z_0} \right) \cos(\omega_0 t) = -I_1 \quad (4.16)$$

and at $x = \lambda/4$,

$$V(t, \lambda/4) = (-V^+ + V^-) \sin(\omega_0 t) = V_{out} \quad (4.17)$$

$$I(t, \lambda/4) = \left(-\frac{V^+}{Z_0} - \frac{V^-}{Z_0} \right) \sin(\omega_0 t) \quad (4.18)$$

Figure 4.10 Output Network Equivalent Model

Applying Kirchhoff's Current Law at the output,

$$\frac{V_{out}}{R} + I_2 = I(t, \lambda/4) \quad (4.19)$$

Substituting equations 4.14, 4.17 and 4.15 into 4.19, we derived,

$$\frac{V^+ - V^-}{R} + \alpha I_0 = \frac{V^+ + V^-}{Z_0} \quad (4.20)$$

From Figure 4.12, we also observed that $Z_1 = -V_1/I_1$

Using equations 4.15 and 4.16 to substitute into 4.20, we get

$$Z_1 = Z_0 \left(\frac{Z_0}{R} - \alpha \right) \quad (4.21)$$

As the peaking amplifier starts to turn on, the increasing current causes an increase in α . This results in the load impedance seen by the main PA to drop. This prevents the voltage swings at the main PA to increase for larger input levels, enabling a relative constant drain voltage.

From equation 4.21, when the peaking power amplifier is off, $\alpha=0$, the designed carrier PA sees an impedance of 100Ω for a fixed output resistor of 25Ω . When the peaking PA starts to turn on and the relative ratio of current is 1, the impedance seen

by the main PA will be reduced to 50Ω . This explains that the main and peaking PA will be designed to match to 50Ω output for the DPA and the impedance transformer of characteristic impedance of 35.35Ω at the end of the DPA to transform 25Ω to 50Ω .

To optimize the matching network to ensure maximum power is delivered to the load, the output of the carrier and peaking amplifiers' transistors are modeled as shown in Figure 4.11.

Figure 4.11 Output Impedance Model Of The Transistor For Matching

The load-pull optimum impedances are $(21.43+j24.74)\Omega$ for carrier PA and $(20.4+j37.7)\Omega$ for the peaking PA. The values of R_c , R_p , C_c and C_p can be derived to be 50Ω , 90Ω , 0.61pF and 0.54pF respectively from

$$X_c = -\frac{1}{2\pi f} \quad (4.22)$$

$$Z = \frac{R \cdot X_c^2}{R^2 + X_c^2} - j \frac{R^2 \cdot X_c}{R^2 + X_c^2} \quad (4.23)$$

This will allow the matching network to be carefully designed to be matched to 50Ω for both the main and auxiliary PAs.

The overall non-linearity of the DPA is a result from the aggregate of the main PA and peaking PA non-linear characteristics [137].

Considering a two-tone signal given by

$$v_{in}(t) = A[\cos(2\pi f_1 t) + \cos(2\pi f_2 t)] \quad (4.24)$$

The power series expansion of the output current of a PA in terms of its input voltage is

$$I_{out}(v_{in}(t)) = gm_1 v_{in}(t) + gm_2 v_{in}^2(t) + gm_3 v_{in}^3(t) + \dots \quad (4.25)$$

where gm_1 is the linear transconductance, gm_2 and gm_3 are the non-linear transconductances. Substituting equation 4.24 into 4.25 and extracting the upper sideband third order terms of the main and peaking PAs, we get

$$I_{out,main}(2\omega_2 - \omega_1) = \frac{3}{4} A^3 gm_{3,main} \cdot e^{j\phi_{main}} \quad (4.26)$$

$$I_{out,peaking}(2\omega_2 - \omega_1) = \frac{3}{4} A^3 gm_{3,peaking} \cdot e^{j\phi_{peaking}} \quad (4.27)$$

The summation of the third order main and peaking PAs currents

$$I_{out,summation}(2\omega_2 - \omega_1) = \frac{3}{4} A^3 (gm_{3,main} \cdot e^{j\phi_{main}} + gm_{3,peaking} \cdot e^{j\phi_{peaking}}) \quad (4.28)$$

The practical components in the circuit will result in a phase off-set in the two paths.

Adding them into consideration,

$$I_{out,summation}(2\omega_2 - \omega_1) = \frac{3}{4}A^3(gm_{3,main} \cdot e^{j(\phi_{main} + \phi_{offset,main\_path})} + gm_{3,peaking} \cdot e^{j(\phi_{peaking} + \phi_{offset,peaking\_path})}) \quad (4.29)$$

From Figure 4.9, the gm3 of the Class C and Class AB PAs have negative correlation in their gm3 values. Assuming the phase shifts between the two paths are negligible or in the case, off-set by the phase shifter, the third order IM term can be suppressed.

The carrier PA is biased at 0.3mA/ μ m for the highest f_{max} with voltage supply of 1.2V based on simulation results. The gate voltage is approximately 0.9V and using that as a starting point, the auxiliary PA is biased below threshold voltage to serve two purposes; turn on after the input power reaches a favorable condition and act as a gm3 cancellation source for the carrier PA. The majority of the harmonic distortion comes from the third-order transconductance and the non-linear current can be seen from equation 4.25. At such a high frequency, as the gain rolled off, pre-amplifiers have to be designed to provide the maximum stable gain before cascading them with the respective driver stages in each path. Contrary to increasing the CF of the entire DPA, this is necessary to allow the DPA to function at 60GHz using this process technology of 65nm.

To design the last block of the phase shifter shown in the schematic in Figure 4.9, the quarter wavelength lines are decoupled from the circuit to determine the phase differences between the two output ports as shown in Figure 4.12. This phase has to be adjusted to ensure the signals are constructively combined.

Figure 4.12 Output Block Decoupled From Architecture

Figure 4.13 Phase Difference and Phases Of S21 and S31

The phase difference to be offset is approximately 49° at 60GHz shown in Figure 4.13. The lumped components following 2 parallel capacitors with a series inductor with the expressions below to determine their values were considered.

$$L = \frac{Z_0}{\omega \tan(\frac{\theta}{2})} \quad (4.30)$$

$$C = \frac{1}{\omega Z_0 \sin \theta} \quad (4.31)$$

The transmission line which acts as the phase shifter was later modelled to replace these components with a Z_0 of 50Ω .

To verify the linearity performance of the gm3 cancellation bias DPA and its performance, another DPA optimized for output power was also designed.

4.3.3 Experimental Results And Discussions

The microstrip lines were modelled to take into account the parasitic capacitances and resistances. For two DPA designs, one with the proposed gm3 linearization and the other optimized just for output power, the DPA with gm3 cancellation achieves a gain of 8.5dB seen in Figure 4.14 as compared to the DPA that is optimized for output power with a gain of 6.2dB seen in Figure 4.15.

Figure 4.14 S-Parameters Plot Of DPA With Gm3 Cancellation

Figure 4.15 S-Parameters Plot Of DPA Without Gm3 Cancellation And Optimized For Output Power

The transistor has a fundamental limit at 60GHz, which does not provide enough gain when biased at Class C, a voltage point below its turn on voltage. Adding more gain stages to boost the gain of the auxiliary PA branch will only result in higher power dissipation which may further reduce the overall PAE the DPA can possibly achieve. The peak PAE of 11% is reached when P_{in} reaches 7dBm as shown in Figure 4.16 compared with a DPA with no gm3 cancellation scheme having a peak PAE of 7.3% as shown in Figure 4.17.

The active load modulation trait of the DPA maximizes the P_{sat} that is approximately 14.5dBm and the output referred compression point is above 10.8dBm as seen from Figure 4.18. The power consumption of the entire circuit is 89.2mW. The DPA with no gm3 cancellation scheme has a P_{sat} of 14.1dBm and P_{1dB} of 9.5dBm shown in Figure 4.19.

Figure 4.16 Power Gain And PAE Plot Of DPA With Gm3 Cancellation

Figure 4.17 Power Gain And PAE Plot Of DPA Without Gm3 Cancellation And Optimized For Output Power

Figure 4.18 Output Power And Compression Point Of DPA With $Gm3$ Cancellation

Figure 4.19 Output Power And Compression Point Of DPA Without $Gm3$ Cancellation And Optimized For Output Power

The IMD3, a FoM for linearity, is improved by about 9dB for the DPA as compared to the balance PA at higher output power level as shown in Figure 4.20 with a two-tone spacing of 100MHz. At higher output power, the auxiliary PA turned on with linearizing effect to the overall DPA due to the gm3 cancellation biasing and extension of its output compression point. As we had to sacrifice the right turning on voltage for the gm3 cancellation effect, the Class C PA is turned on slightly later. The initial higher IMD3 for the DPA with gm3 cancellation was attributed to the additional phase offset lines and possibly slight mismatched in the matching networks. However, the gm3 cancellation effect or the improvement in linearity could be observed at higher output power level once the auxiliary PA is in full operation. When the auxiliary PA turns on, the saturation operation allows the main PA to enter the under-saturation regime due to the active load modulation, which can be seen in the dips. With increasing power level from there, the main PA will start to enter the saturation region similar to the auxiliary PA, which explains the increasing non-linearity trend afterwards. This is in agreement with some of the DPA linearization works [138, 139] in the recent years after the proposed work at 60GHz which shows the non-monotonic increase of IMD3 during the operation of the DPA.

Figure 4.20 IMD3 Of Balance PA, DPA With And Without Gm3 Cancellation Biasing

The IMD3 at higher output power level is improved by approximately 10dB compared with a balance PA structure due to the linearizing effects of gm3 cancellation with proper biasing and the operation of DPA. At the higher output power levels from approximately 5dBm onwards, we can also observe that the linearity is improved compared to the DPA designed without considering the gm3 cancellation biasing by about 6dB.

At the time of publication, this work is compared with the published 60GHz DPA design optimized for output power and the work by [80] as shown in Table VI. The small improvement rather than a significant jump is due to power and gain limitations because of the high gain roll-off at 60GHz. The f_T of the device is lesser

than 60GHz, which explains the low gain and output power at this designed frequency if power combining techniques are not employed.

Table VI Performance Summary Of 60GHz CMOS DPA

References	<i>This Work</i>	[140]	[80]	[141]	[28]
Process	65nm DPA	65nm DPA	0.13μm DPA	45nm SOI DPA	65nm DPA
Supply(V)	1.2	1.2	1.6	2	1.8
Gain(dB)	8.5	6.2	13.5	12.9	16
P_{sat}(dBm)	14.5	14.1	7.8	20.1	13
Peak PAE(%)	11	7.3	3	26	17*
P_{1dB}(dBm)	10.8	9.5	7	19.3	9**
FoM	19	14.5	12	32.7	27^

FoM (ITRS) = P_{sat}+Gain+20log(fc[GHz])+10log(PAE)-30dm

* Drain efficiency of the design

** Estimated from the graph

^ Calculated from drain efficiency

4.4 Summary

In this chapter, some of the linearization techniques that could be applicable to the PA blocks of the DPA were introduced to consider the discretonal complexity. Designers can choose to, or not to perform this optional step but using linearity of DPA as an example, we then proposed a gm3 cancellation bias scheme to improve the linearity of the DPA to demonstrate linearity can be improved for circuit without looking at external circuitry to increase the complexity. Two designs of the power divider were introduced and discussed briefly to cover all aspects of the DPA design in which a broadside coupler was proposed and introduced to be used in the DPA. The wide phase offset allows the results to be improved and the DPA achieves a gain of 8.5dB with a peak PAE of 11%. The demonstrated P_{sat} is 14.5dBm and output referred compression point $P_{1\text{dB}}$ is above 10.8dBm. The total power consumption of the chip is 89.2mW. In terms of the modified FoM, PAE and $P_{1\text{dB}}$, it achieved one of the highest during the time of publication of this work. This work demonstrated that linearity sometimes as an optional parameter in research works, can be enhanced without increasing the complexity of DPA.

CHAPTER 5

Conclusion and Future Work

5.1 Conclusion

Circuit optimization is a daunting task for any circuit designer due to many circuit-level designs trade-offs. This is further complicated with additional complexity involved with the design. A higher complexity circuit will increase the design cycle time and hence lengthen the TTM of wireless products and also increasing the manufacturing cost and operation cost. This thesis focused on the complexity considerations of circuit design using DPA as an example.

To start off with the design flow using DPA as an example, the architecture complexity was addressed first by utilizing the proposed methodology to quantify a metric to select the DPA architecture with low CF. This will be the first pass in reducing the design cycle time of a DPA. The methodology simplified the process by tapping on the parameters of the passive networks and S-Parameters of the power divider and PA blocks. In doing so, the following contributions were achieved:

- An approach and flow to circuit design for a complexity-aware DPA is proposed
- A proposed FoM for circuits using DPA as an example, CF, and hence, NCF, is introduced to tackle the architecture complexity issue.

To address the next step of topology complexity, the PA blocks are explored. A comparison between 2-stacked EDNFET and SGNFET and an adopted 4-stacked SGNFET on SOI process, both of which would potentially provide more than 20dBm of output power in a DPA and approximately 60% PAE was made. This would allow designers to consider exploring the SOI process 2-stacked PA to be implemented in the DPA instead of higher order number of stacked PA for high output power applications, which certainly would decrease the complexity of the circuit. This allowed us to achieve the following:

- A topology complexity consideration of stacked EDNFET and SGNFET and an adopted 4-stacked SGNFET implemented on 0.13 μ m RFSOI process was proposed as potential candidates for a reduced complexity DPA design, demonstrating a lower complexity topology can possibly yield comparable, or even better performance compared with a higher complexity topology.

In the last step of the design flow for discretional complexity in which we chose linearity of the DPA as an example, a gm3 cancellation bias DPA was proposed to enhance the linearity of the DPA without increasing the number of components from external circuitry. The proposed scheme makes use of the biasing point of the main PA and the auxiliary PA in the DPA to carry out the linearization. This helps to maintain its complexity and at the same time, potentially improving its performance. It demonstrated an IMD3 improvement of 6-8dB compared to a DPA

designed for optimized output power and more than 9dB improvement compared to a balance PA which has a similar structure at 60GHz. The contribution by this work is as follows:

- A gm3 cancellation bias was proposed to demonstrate linearity enhancement to DPA at 60GHz without adding additional circuitry to increase its complexity much to address discrecional complexity. Its linearity is improved compared to a DPA optimized for power.

5.2 Recommendations for Future Work

The ever-evolving RF wireless products seen from the explosive growth of technological products and the welcoming of 5G standard will create new opportunities for many design companies. The tight demand for shorter TTM by companies and industry which are profit driven may create opportunities for low complexity designs and methodology to be a research focus so as to meet the market demands.

The conventional solution to design circuits, DPA as an example, is to set out a target technical specification and work towards it. However, there have been plenty of research works done to optimize certain parameters of the DPA and none of them addresses the complexity issue explicitly. The proposed methodology in Chapter 1 could be applicable to choosing a design architecture before committing. The current proposed methodology requires building up a database of CF and FoM manually so as to gather useful data to determine the sweet-spot for gain, PAE or output power. One effective way is that foundries are able to compile the data by treating customers' designs as black-boxes, thus protecting the intellectual

properties of the customers but at the same time, increasing the database exponentially since designers go through foundries for the process design kits and tapeouts, which will also allow designers to tap on a real-time complexity analysis on the circuits.

With 5G standard still in the works, designers and companies would be looking at ease of integration and cheaper manufacturing cost for circuits. In future works, the topology complexity could be formulated and a more comprehensive study of topologies could be conducted. A look-up table can be compiled to input data such as frequency of design, processes, output parameters such as gain, PAE, output power to allow some form of data to be collected and computed. This would allow the best of each component to be chosen, yet not compromise the complexity of the circuit design process.

The discretionary complexity only addresses the linearity concern in this thesis using DPA as an example. For different circuits, there could be different optional factors. This can be further explored in the future as well.

With this thesis as a stepping stone for future research works on the complexity considerations for circuit design, it can be part of a larger hierarchical framework forming a two-pronged approach from the circuit and manufacturing point of view as seen in Figure 5.1 to reduce the cost at the start.

Figure 5.1 Two-Pronged Hierarchical Framework

Higher frequency designs are still dominated by MESFET, HBT and P-HEMT processes due to their ability to deliver higher output power and efficiency. However, it reduces the capability and ease of co-design and integration with components from CMOS or SOI processes. By pushing the gain stage of the DPA for example into SOI process could save the cost significantly. However, as there are limitations to overcome due to cost and performance trade-off, complexity considerations have to be explored now more than ever as increasing performance for DPA as an example could come with a higher complexity design. However, performance and complexity can still reach a compromise as shown throughout this thesis. In the pursue of circuit performance, many research works had not undertaken the task to address the complexity issue which is of paramount importance to design companies as it will lead to issues in TTM and profit margin for example.

As a result, from Figure 5.1, it can be seen from the proposal that process and circuit design complexity analyses are to be done at the start during the design phase. By formulating a complexity FoM for processes, it can be integrated with the circuit's complexity FoM to allow designers and companies to optimize circuit performance, TTM and profit margin.

The author believes that research in methodology to design circuits involving reducing the complexity will be one of the hottest topics for the industry in the coming years. It allows companies to drive up revenues by reducing their TTM and potentially pioneering new research and development frontiers. One way to achieve that is to develop a complexity analysis suite for designers to anticipate the complexity for circuit design as well as manufacturing process before optimizing or even designing their circuits.

AUTHOR'S PUBLICATIONS

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1. **Aaron Tan**, Rui Tze Toh, Alfred Lim, Yongfu Li, Zhi Hui Kong, “A Methodology To Evaluate Circuit Complexity: Doherty Power Amplifier As A Case Study,” *Electronics*, 2019, 8, 313
2. Alfred Lim, **Aaron Tan**, Zhi Hui Kong, Kaixue Ma, “A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier” *Electronics*, 2019, 8, 494
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4. Alfred Lim, **Aaron Tan**, Zhi Hui Kong, Kaixue Ma, Kiat Seng Yeo, “A 2.4-GHz Transformer-Based Class-E Power Amplifier” *Pending submission*
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