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Balancing Average Capacitor Voltages in Neutral-Point-Clamped Converters Using Band-Limited Three-Level Modulation

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Abstract—In this paper, a band-limited three-level modulation scheme is presented which aims to balance the average capacitor voltages in neutral-point-clamped converters under all load operating conditions. Compared to previous three-level modulation schemes, the proposed scheme provides a trade-off between voltage balancing performance and switching losses. Consequently, helping in optimizing the system's footprint and its operating cost. A variable current band is calculated in order to provide the necessary control action for balancing the average (as opposed to instantaneous) capacitor voltages. The proposed modulation scheme is tested under both linear and nonlinear loads. A comparison is also performed between the proposed band-limited three-level modulation and other modulation schemes presented in the literature.

Index Terms—Capacitor voltage balancing, neutral-point-clamped converter, pulsewidth modulation, three-level modulation.

I. INTRODUCTION

Fig. 1 shows the neutral-point-clamped (NPC) converter [1]. This converter topology is commonly used in medium-voltage applications [2]. However, it faces some important control challenges, which limit its application. One of the most crucial challenges is balancing the dc-link capacitor voltages, especially when feeding nonlinear loads enriched in even harmonics [3], [4]. Another issue is the presence of low-frequency neutral point (NP) voltage ripples, especially when operating with large modulation indices and low load power factors [5].

The NPC converter has natural voltage balancing capability when feeding balanced linear loads, which implies there is a tendency for the average dc-link capacitor voltages to balance without any explicitly imposed control action or external balancing circuitry [6]. However, due to the weak nature of this natural balancing capability, many control and hardware solutions have been proposed in the literature to deal with the voltage balancing issue in NPC converters.

In [7], the authors proposed a carrier-based pulse-width modulation (CBPWM) technique with zero-sequence signal injection for achieving better voltage balancing performance and larger output voltage amplitudes compared to sinu-

soidal PWM. A standard CBPWM technique with maximum-minimum based zero-sequence addition [8] is considered for reference in this work and is referred as CBPWM in the rest of this paper. In CBPWM, with steady state operation, all the phases of the converter switch between two consecutive voltage levels, i.e., within a sampling period either they switch between the positive rail and the NP or between the negative rail and the NP [9]. This, in turn, leads to low switching losses. However, the ability to balance capacitor voltages is limited when using CBPWM with unbalanced / nonlinear loading conditions [4], [10].

Lopez *et al.* [8] proposed a three-level modulation scheme, which completely eliminates the low-frequency ripples in the capacitor voltages. In this technique, two phases of the NPC converter switch in two levels, while one phase switches in three voltage levels, i.e., one phase switches among the positive rail, the NP and the negative rail during one sampling period. However, switching a phase in three levels leads to higher switching losses, which reduces the efficiency of the converter.

In this paper, a band-limited three-level modulation scheme

Fig. 1. Three-phase NPC converter feeding a linear and a nonlinear load.

is proposed, which aims to achieve lower switching losses compared to the three-level modulation [8], and better capacitor voltage controllability than CBPWM. For achieving this, in the proposed scheme, the oscillatory NP voltage fluctuations are allowed to remain while the target is to balance the average capacitor voltages. Thus, the reference NP current is calculated using the average voltage difference of the two capacitor voltages. Depending on the values of the reference NP current and the NP current, the band-limited three-level modulation scheme decides whether all the phases will switch in two levels or one of the three phases will switch in three levels. Moreover, a variable current band is calculated which ensures that the three-level modulation is limited only to sampling instants where the absolute value of the corresponding phase current is low, i.e., the phase current resides within the band. The main features of the proposed scheme are as follows,

- No external circuit is employed, thereby, there is no increase in the system's footprint and cost.
- A variable current band is calculated online in order to provide only the necessary control action for balancing the average capacitor voltages depending upon the operating requirements.
- The average capacitor voltages are maintained equal under linear as well as nonlinear loads such as half-wave rectifiers.

The rest of this paper is organized as follows. Section II introduces the proposed band-limited three-level modulation scheme. Section III presents simulation results for a three-phase NPC converter feeding a linear and a nonlinear load. The main conclusions of the paper are summarized in Section IV.

II. PROPOSED MODULATION TECHNIQUE

The proposed band-limited three-level modulation scheme aims to balance the average capacitor voltages by eliminating the dc component of the NP current. The various steps involved are as follows:

1) Computation of normalized modulation signals

The three phase reference voltages ($v_{a_REF}, v_{b_REF}, v_{c_REF}$) obtained from the controller are normalized as:

$$v_{in} = \frac{v_{i_REF}}{V_{dc}/2} \quad \text{for } i = \{a, b, c\} \quad (1)$$

A zero-sequence signal (v_{off}) is added to the obtained normalized signals so as to enhance the utilization of the dc-link voltage.

$$v_i = v_{in} + v_{off} \quad \text{with } i = \{a, b, c\}. \quad (2)$$

where,

$$v_{off} = -\frac{\max(v_{an}, v_{bn}, v_{cn}) + \min(v_{an}, v_{bn}, v_{cn})}{2} \quad (3)$$

The obtained v_i represents the normalized modulation signals with zero-sequence addition.

2) Estimation of NP current

Under CBPWM, all the three phases switch in two voltage levels, i.e., either they switch between positive dc-rail and NP, or between negative dc-rail and NP. From [9], the duty cycle for phase i connected to the NP (d_{NPi}) is calculated as:

$$d_{NPi} = 1 - |v_i|. \quad (4)$$

Assuming that all phases are switching in two consecutive levels, the average NP current in a switching cycle is calculated as:

$$i_{NP} = d_{NPa}i_a + d_{NPb}i_b + d_{NPc}i_c. \quad (5)$$

3) Calculation of NP current reference

The band-limited three-level modulation aims to balance the average capacitor voltages. For achieving this, the NP current reference is calculated by using the average difference of the two capacitor voltages (v_{C1} and v_{C2}) as shown below:

$$i_{NP}^* = C \frac{\overline{v_{C1} - v_{C2}}}{T_s} \quad (6)$$

where T_s represents the switching period and C is the capacitance of each dc-link capacitor.

4) Calculation of the variable current band limit

Based on the NP current value (i_{NP}) and NP current reference (i_{NP}^*), the band-limited three-level modulation scheme decides if one phase will switch in three levels. A current band is chosen such that a phase switching in three levels is limited only to sampling instants in which its phase current resides within the band. This will help to reduce the switching losses. The variable current band limit is calculated as shown in Fig. 2 and is dependent on two controller feedback loops.

In the first controller feedback loop, the difference between the two capacitor voltages is fed to a low pass filter (LPF) to obtain the average difference. Larger average voltage differences result in a larger band limit. As a result, the chances of a phase switching in three levels increases, which helps in balancing the average capacitor voltages. In addition, using the absolute value of the average capacitor voltages precludes the use of an integral component to eliminate steady state errors. Therefore, a second controller feedback loop is required to remove this steady state error by eliminating the dc component of the NP current, which results in average capacitor voltage shifts. For this, the difference between the average NP current which would flow if all the phases switched in two levels (i_{NP}), and the average of the NP current which no longer flows to the NP when three-level modulation is applied (i_{NPp}), is regulated to zero. The phase switching in three levels is decided using the NP current reference and the NP current (as discussed in the next step). If the average of i_{NP} equals the average of i_{NPp} (the current that is no longer injected into the NP), then there is no average current that unbalances the NP.

Fig. 2. Calculation of the variable current band limit.

5) Calculation of duty cycles

- a) Case I. If $(0 < i_{NP} < i_{NP}^*)$ or $(0 > i_{NP} > i_{NP}^*)$
This implies that the direction of i_{NP} is the same as the required direction of i_{NP}^* , and also the magnitude of i_{NP} is not larger than the required reference NP current. Therefore, there is no need for any leg to switch in three levels. The NP duty cycles for all the three phases are calculated using (4).
- b) Case II. If $(i_{NP} * i_{NP}^*) < 0$
In this case, as the direction of the NP current and the reference NP current is the opposite, it is important to switch a phase in three levels. However, all the phases are first tested if their absolute phase current values are within the variable current band. The phases within the band are then tested if they have the tendency to shift the NP current in the required direction of i_{NP}^* . Let's take a case where phase 'p' has phase current within the current band, take $d_{NPp} = 0$, and calculate the new i'_{NP} using (5). If $(i'_{NP} * i_{NP}^*) > 0$, then phase 'p' is allowed to switch in three levels. If there are two phases that can switch in three levels and their currents are within the band, then the phase with less absolute phase current value is chosen to switch in three levels. The phase selected to switch in three levels is entered as a feedback for the calculation of variable current band limit as phase 'p'. Let's assume phase 'p' is chosen to switch in three levels, while phases 'l' and 'm' switch in two levels. The NP duty cycles for phases 'l' and 'm' are calculated using (4), while the NP duty cycle for phase 'p' connected to the NP is given by [10]:

$$d_{NPp} = \frac{i_{NP}^* - d_{NPl}i_l - d_{Npm}i_m}{i_p} \quad (7)$$

- c) Case III. If $(i_{NP} * i_{NP}^*) > 0$ and $|i_{NP}| > |i_{NP}^*|$
As the magnitude of the required reference NP current is less than the NP current, one phase

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Carrier frequency, f_s	4 kHz
DC-link capacitors (each), C	168 μ F
DC-link voltage, V_{dc}	400 V
AC-side frequency, f	50 Hz
AC-side load (per-phase), RL	6 Ω , 36.8 mH

is required to switch in three levels. Similar to the previous case, herein, the phases which are below the variable current band are selected. Let's assume the current of phase 'p' is within the band, then taking $d_{NPp} = 0$, the new i'_{NP} is calculated using (5). If $|i'_{NP}| < |i_{NP}^*|$, then phase 'p' is chosen to switch in three levels. If there are more than one phase that meets these conditions, the phase with the lowest phase current is chosen to switch in three levels. The phase switching in three levels is continuously updated for the variable band calculation. The NP duty cycle for phase 'p' switching in three levels is calculated using (7).

The duty cycle for phase i connecting to the negative dc-rail (d_{li}) and the duty cycle for phase i connecting to the positive dc-rail (d_{hi}), irrespective of the phase is switching in two or three levels, are given by:

$$d_{li} = \frac{1 - d_{NPi} - v_i}{2}, \quad (8)$$

$$d_{hi} = 1 - d_{NPi} - d_{li} \quad \text{with } i = \{a, b, c\}. \quad (9)$$

The obtained duty cycles are then compared to the carrier waveform to generate the required switching pulses. Finally, it is noted that a phase is only chosen to switch in three levels if the phase has the tendency to compensate the NP current in the appropriate direction to reduce the average voltage difference (and also has a current within the defined band limit).

Fig. 3. Performance of the proposed band-limited three-level modulation with initial voltage imbalance at (a) $m=1$ and (b) $m=0.5$.

III. SIMULATION RESULTS

For validating the proposed modulation scheme, various simulation tests are performed in MATLAB/Simulink environment using a three-phase NPC converter feeding a linear and a nonlinear load. The simulation parameters employed are given in Table I.

A. Linear Load Condition

The switch ‘S’ in Fig. 1 is open such that the three-phase NPC converter feeds a linear load. The dc-link capacitors are forced to have an initial voltage imbalance, $V_{C1} = 250V$ and $V_{C2} = 150V$. Fig. 3 shows the line-to-line voltage (v_{ab}), capacitor voltages (v_{C1} and v_{C2}) and load currents (i_a , i_b and i_c) at different modulation indices (m) under the proposed band-limited three-level modulation. In Fig. 4, a performance comparison among the proposed scheme, CBPWM and three-level modulation [8] is shown. From these figures, it is clear that even with an initial imbalance, the proposed band-limited three-level modulation balances the average capacitor voltages faster as compared to CBPWM which utilizes only the natural capacitor voltage balancing capability.

B. Nonlinear Load Condition

For implementing the nonlinear load, switch ‘S’ is closed in Fig. 1. Fig. 5 shows the performance of the proposed band-limited three-level modulation feeding a nonlinear load at $m=1$ and $m=0.5$. Fig. 6 depicts a comparison among CBPWM, three-level modulation and the proposed scheme under the same test conditions. The challenge of the diverging nature of capacitor voltages in the presence of nonlinear loads enriched with even harmonics is resolved using the proposed scheme. The average capacitor voltages are balanced, unlike the case of applying CBPWM.

C. Efficiency Analysis

Using the characteristic curves from the manufacturer’s datasheet of an insulated-gate bipolar transistor (IGBT), a loss model is implemented for the NPC converter. DIM1200SM17-E000 IGBT are considered for the loss analysis with $V_{dc} = 1500V$ and $f_s = 2.5kHz$. Fig. 7 shows the ratio of losses of the proposed band-limited three-level modulation to three-level modulation [8] at different load phase angles and modulation indices. It is clear that the switching losses of the proposed technique are lower than the case of three-level modulation under all operating conditions. The conduction losses for the two modulation schemes are almost the same as the only difference is the device conducting during the conduction period in the two schemes. Fig. 7(c) shows that the band-limited three-level modulation scheme produces lower switching losses than the three-level modulation.

IV. CONCLUSION

In this paper, a trade-off modulation scheme between CBPWM and three-level modulation has been introduced. The performance of the proposed band-limited three-level modulation scheme is tested under linear as well as nonlinear loads. The average capacitor voltages are balanced under all the tested operating conditions unlike CBPWM. Moreover, the obtained switching losses of the proposed scheme are lower than three-level modulation at all modulation indices and load phase angles.

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Fig. 4. Comparison among the proposed scheme, CBPWM and three-level modulation under same initial voltage imbalance at $m=1$.

Fig. 5. Performance of the proposed scheme feeding a nonlinear load at (a) $m=1$ and (b) $m=0.5$.

Fig. 6. Comparison among the proposed band-limited three-level modulation, CBPWM and three-level modulation feeding a nonlinear load at $m=1$.

Ratio of switching losses (Band-limited three-level modulation/Three-level modulation)

(a)

Ratio of conduction losses (Band-limited three-level modulation/Three-level modulation)

(b)

Ratio of total losses (Band-limited three-level modulation/Three-level modulation)

(c)

Fig. 7. Ratio of losses between the proposed modulation scheme and three-level modulation, (a) switching losses, (b) conduction losses, and (c) total losses.

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