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Feedforward Modulation for the Neutral-Point-Clamped Converter with Confined Capacitor Voltage Ripples and Reduced Switching Power Losses

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Abstract—This paper presents a new modulation technique with feedforward compensation for the three-phase three-level neutral-point-clamped converter. With the proposed technique, the capacitor voltage ripples are allowed to vary within certain limits. This enables an optimised design of the converter since the maximum capacitor voltages are predefined. Furthermore, the proposed modulation technique is able to reduce switching power losses compared to modulation techniques that eliminate capacitor voltage ripples completely. The proposed technique is therefore a trade-off solution between aforementioned techniques and traditional modulation techniques where the capacitor voltage ripples are not limited. In the proposed technique, if the capacitor voltages are within the tolerable specified range, all the phases switch in two consecutive voltage levels in steady state. When the capacitor voltages go beyond the specified limits, one of the three phases is chosen to switch in three levels to inject an appropriate neutral point current for capacitor voltage balance. As the capacitor voltages are allowed to oscillate, the modulation technique is provided with feedforward compensation to avoid producing low frequency distortion on the output voltages of the converter. Experimental results are presented operating under different loading conditions.

Index Terms—Neutral-point-clamped converter, carrier-based PWM, voltage imbalance, feedforward compensation.

I. INTRODUCTION

The neutral-point-clamped (NPC) converter, shown in Fig. 1, has gained wide popularity since its first introduction in 1981 [1]. The major advantages of using an NPC converter over traditional two-level voltage source converters are fewer harmonics in the ac side voltages, lower device ratings for the same power rating of the converter and less switching losses. With these merits, the NPC converter has been widely used in applications like wind and solar energy conversion, static compensator (StatCom) devices, ac drives, etc. [2]–[7].

There are many challenges associated with operation of the NPC converter. The major issue is to divide the dc-link voltage equally among the dc-link capacitors. A first attempt to achieve capacitor voltage balance was implemented by Newton and Sumner in [8]. Additionally, when operating the converter with high modulation indices and low power factor loads, a low-frequency voltage ripple appears at the neutral point [9], [10], which in turn leads to distortion in the ac side voltages. Pou *et al.* [11] have discussed the effect of nonlinear loads fed by an NPC converter on the

dc-link capacitor voltages. The odd-order harmonics result in additional low-frequency NP voltage ripples, while the even-order harmonics from the nonlinear load can shift the NP voltage, leading to instability. Another issue is the complexity of the modulation and control involved for the NPC converter. Several modulation techniques have been proposed in the literature [12], [13]. One of the commonly employed modulation techniques is space-vector pulsewidth modulation (SVPWM) [14]–[17]. In [14], a feedforward modulation approach was proposed for compensating the capacitor voltage imbalances on the space vector diagram, and successfully eliminating low frequency distortion on the output voltages. However, the low-frequency capacitor voltage ripples are not limited and depend on the operational condition. In [15], a modulation technique based on nearest three vector virtual SVPWM was presented. Though the technique achieves capacitor voltage balancing for all modulation indices and power factors, the switching frequency of the power devices increases significantly and additional high frequency distortion is observed in the output voltages. An improved version of virtual SVPWM using feedforward compensation is presented in [16] which shows lower switching distortion in the output voltages, however, the subdivisions of the sectors increase the control complexity. An SVPWM technique for high modulation indices along with neutral point (NP) balancing is presented in [17]. The duty cycles are calculated for different ranges of modulation indices, expanding the control algorithm and therefore making its implementation more difficult.

Another commonly employed modulation technique is carrier-based pulsewidth modulation (CBPWM) [18]–[22]. Dordevic *et al.* [23] presented a comparison among two SVPWM and three CBPWM based techniques. The results show superior performance of CBPWM techniques on account of execution time, implementation complexity and capability to be extended to multilevel and multiphase converters. In [18], a zero sequence was added to the modulation signals, obtained from the duality between nearest-three-vector space-vector modulation [10] and CBPWM. It provides better capacitor voltage balancing performance compared to standard sinusoidal PWM (without zero sequence injection), besides achieving 15% larger output voltage amplitudes. Another approach for calculating the zero sequence was introduced

Fig. 1. Three-phase NPC converter feeding a linear and a nonlinear load.

in [19], wherein the authors used an interpolation method to calculate the zero sequence voltage. In [20], a general modulation technique for multiphase NPC converters was proposed. Similarly to [18], it is based on clamping one phase either to the positive dc rail, negative dc rail, or to the NP, depending on the modulation index and the error between the reference NP current and the actual NP current. In all these modulation techniques, a low-frequency capacitor voltage ripple appears, where the ripple amplitude depends on the operating conditions of the converter. This fact challenges converter design because of uncertainties when estimating the maximum voltages on the dc-link capacitors. In [21], a CBPWM technique able to completely remove the low-frequency ripples in the capacitor voltages was proposed. A different approach that achieves similar results, but with improved voltage balancing performance, was presented in [22].

All the modulation techniques that eliminate low-frequency capacitor voltage ripples in the three-phase NPC converter [15], [21], [22], need to switch one of the phases in three voltage levels (using positive, NP, and negative voltage rails denoted as 1, 0, and -1 in Fig. 1, respectively) within each switching cycle, while the rest of the phases switch in two consecutive levels (using +1 and 0, or 0 and -1 voltage rails shown in Fig. 1). Consequently, the switching losses of the converter increase significantly because of the additional switching transitions. As a trade-off between these techniques and traditional modulation techniques, this paper proposes a new CBPWM approach based on [22]. However, here certain deviations of the capacitor voltages are tolerated but constrained within predefined limits. If the capacitor voltages reach the selected limits, one phase switches in three levels for one or more switching periods, to prevent the capacitor voltages exceeding the limits. Since the capacitor voltages are allowed to oscillate with this technique, a novel feedforward compensation is proposed to avoid low frequency distortion in the ac voltages due to capacitor voltage imbalances. Such a feedforward compensation is introduced in this paper for the first time, and it is able to compensate the output voltage during the switching periods where one phase is switching

in three levels. The proposed modulation technique produces less switching losses than [15], [21], [22], while the maximum voltages on the dc-link capacitors and switching devices are limited, unlike traditional modulation techniques. It is therefore a trade-off solution between the two cases.

In most of the previously presented modulation techniques in the literature, the NP voltage ripple is dependent on the converter's operating conditions, thus, there are uncertainties in estimating the maximum voltage across the dc-link capacitors and the semiconductors of the converter. With the proposed modulation scheme, as the capacitor voltage limits are predefined, the maximum voltage that the power semiconductors and dc-link capacitors have to withstand is also known. This fact is important to optimally design the NPC converter beforehand. As mentioned earlier, the various applications of NPC converter includes grid-connected NPC converter, medium-voltage drives, grid interfacing of renewable energy resources such as wind and solar, etc. [2]-[7]. Whenever an unbalanced voltage sag occurs in such systems, a large voltage ripple is observed on the dc-link capacitors. As a result, generally, large bulky dc-link capacitors are employed to limit these ripples. However, with the proposed modulation scheme, the capacitor voltage ripples can be limited to predefined values even under unbalanced loading conditions. This helps in employing less bulky capacitors at the dc-link, thereby, reducing the system's size and cost. Moreover, the switching losses obtained under the proposed modulation scheme are lower than the case of applying three-level modulation all the time. This further helps in reducing the operating cost of the converter.

The major advantages of the proposed modulation technique are:

- As the maximum voltage across the capacitors is predefined, the converter can be optimally designed beforehand.
- There is no need for tuning gains or adjusting parameters because there are no controllers involved.
- When the capacitor voltages are within the specified limits, traditional CBPWM is applied, implying low switching losses and high quality output voltages.
- For the short intervals where one phase has to switch in three levels, the phase with additional transitions is carefully selected to reduce switching losses.
- No low-frequency distortion is produced in the output voltages thanks to the feedforward compensation implemented.

The paper is organized as follows. Section II presents details of the proposed modulation technique. Section III provides experimental results for a three-phase three-level NPC converter under balanced, unbalanced and nonlinear loads. Finally, Section IV summarizes the main conclusions of this work.

II. PROPOSED MODULATION TECHNIQUE

The proposed modulation technique is based on a CBPWM approach, wherein modulation signals are used to control the phases. In [22], the authors showed that in the case of a three-phase three-level NPC converter, switching just one phase

Fig. 2. Flow diagram of the proposed feedforward modulation.

in three levels and the rest in two levels at each switching period results in complete removal of NP voltage oscillations. However, switching in three levels produces additional power losses as compared to switching in two levels. The proposed modulation technique is a trade-off between switching losses and capacitor voltage controllability. With this technique, the capacitor voltages, v_{C1} and v_{C2} , are free to vary within a range $[0.5V_{dc} \pm \Delta V]$, wherein V_{dc} is the total dc-link voltage and ΔV represents the specified tolerance band for the capacitor voltages. However, the variation of capacitor voltages causes distortion in the ac side voltages. A feedforward compensation is required to compensate for such voltage imbalances.

Figs. 2 and 3 show the various steps involved in the proposed modulation technique. Firstly, the NP current and the NP current reference are estimated using the steps shown in Fig. 2. Depending on the obtained values of these currents, it is decided whether a phase will switch in two levels or three levels (Fig. 3). The various steps involved are described next.

1) Calculation of normalized modulation signals.

The original normalized modulation signals are given by:

$$v_{in} = \frac{v_{iREF}}{V_{dc}/2} \quad \text{for } i = \{a, b, c\} \quad (1)$$

where v_{iREF} is the reference voltage for phase i given by the controller.

A zero sequence is added to the modulation signals:

$$v_{off} = v_{off1} + v_{off2} \quad (2)$$

in which,

$$v_{off1} = -\frac{\max(v_{an}, v_{bn}, v_{cn}) + \min(v_{an}, v_{bn}, v_{cn})}{2} \quad (3)$$

and,

$$v_{off2} = \pm \frac{v_{C2} - v_{C1}}{v_{C2} + v_{C1}}, \quad (4)$$

where v_{an} , v_{bn} and v_{cn} are the original normalized modulation signals for phases a , b and c , respectively, and v_{C1} and v_{C2} are the voltages of the lower and upper capacitors, respectively. v_{off1} represents the offset to achieve full utilization of the dc-link voltage, while v_{off2} is needed to balance the average voltages of the dc-link capacitors. The sign in (4) for v_{off2} is taken as positive when the converter operates as an inverter and negative when it operates as a rectifier. The normalized modulation signal with the added zero sequence is indicated as v_i :

$$v_i = v_{in} + v_{off} \quad \text{with } i = \{a, b, c\}. \quad (5)$$

2) Calculation of duty cycles without feedforward compensation.

If a phase is switching in two consecutive voltage levels, and the normalized modulation signal is positive, the phase will be switching between the positive rail and the NP [24]. The duty cycles can be calculated as:

$$d_{hi} = v_i, \quad d_{li} = 0 \quad \text{and} \quad d_{NPi} = 1 - v_i, \quad (6)$$

where d_{hi} , d_{li} and d_{NPi} are the duty cycles for connecting phase i to the high, low and NP dc rails, respectively. If the modulation signal v_i is negative and the phase is switching in two levels, the corresponding phase will switch between the negative rail and the NP. The duty cycles are given by:

$$d_{hi} = 0, \quad d_{li} = -v_i \quad \text{and} \quad d_{NPi} = 1 + v_i. \quad (7)$$

In general terms, the duty cycle connecting to the NP can be calculated as [24]:

$$d_{NPi} = 1 - |v_i|. \quad (8)$$

3) Calculation of duty cycles incorporating feedforward compensation.

For mitigating the effect of capacitor voltage imbalance on the ac side voltages, a feedforward compensation is incorporated. A detailed formulation of the duty cycles with feedforward compensation is provided in the Appendix. The modified duty cycles for a phase that is switching in two consecutive levels are obtained as:

$$d'_{hi} = d_{hi} \frac{V_{dc}}{2v_{C2}} \quad (9)$$

$$d'_{li} = d_{li} \frac{V_{dc}}{2v_{C1}} \quad (10)$$

$$d'_{NPi} = 1 - d'_{hi} - d'_{li} \quad (11)$$

where d'_{hi} , d'_{li} and d'_{NPi} are the feedforward compensated duty cycles.

4) Calculation of NP current.

Fig. 3. Proposed modulation technique.

The locally-averaged NP current over a switching cycle is computed as:

$$i_{NP} = d'_{NP_a} i_a + d'_{NP_b} i_b + d'_{NP_c} i_c. \quad (12)$$

5) Calculation of reference NP current.

If the capacitor voltages are outside the interval $[V_{Cmin}, V_{Cmax}]$, the locally-averaged NP current needs to be regulated to achieve capacitor voltage balance. Here, V_{Cmin} represents $[0.5V_{dc} - \Delta V]$ and V_{Cmax} represents $[0.5V_{dc} + \Delta V]$.

The reference NP current is calculated as follows [22]:

$$i_{NP}^* = 2C \frac{\Delta v_{NP}}{T_s} \quad (13)$$

where T_s is the switching period, C is the value of each dc-link capacitor, and Δv_{NP} is the deviation of the NP voltage from its reference value:

$$\Delta v_{NP} = v_{C1} - \frac{V_{dc}}{2}. \quad (14)$$

In order to produce an appropriate NP current, one phase may be required to switch in three voltage levels during the next switching period.

6) Determination of phases switching in two or three levels and calculation of duty cycles.

It is expected that all the phases will switch in two consecutive voltage levels most of the time. However, a phase may be required to switch in three levels depending on the operating conditions of the converter. This will be determined at each switching period from

v_{C1} , V_{Cmin} , V_{Cmax} and i_{NP} . The different cases are given in the following.

a) Case-I. If $V_{Cmin} \leq v_{C1} \leq V_{Cmax}$

In this case, all the phases are switched in two consecutive voltage levels as the capacitor voltages are within the tolerable limits. The duty cycles for all the phases remain the same as calculated in (9)-(11).

b) Case-II. If $v_{C1} < V_{Cmin}$ and $i_{NP} \leq 0$

In this case, the voltage of the lower capacitor needs to increase. As the NP current goes in the direction to charge this capacitor, no special action is required and all the phases switch in two consecutive voltage levels. The duty cycles remain unchanged and are the same as in (9)-(11).

c) Case-III. If $v_{C1} > V_{Cmax}$ and $i_{NP} \geq 0$

Since a positive NP current will decrease the capacitor voltage v_{C1} , no further action is required. Therefore, all phases switch in two levels and the duty cycles remain the same as in (9)-(11).

d) Case-IV. If $v_{C1} < V_{Cmin}$ and $i_{NP} > 0$

As $v_{C1} < V_{Cmin}$ and the NP current goes in the discharging direction, a phase switches in three levels to change the direction of the NP current. First of all, it is necessary to check what is the phase or phases that can change the direction of the NP current. For this, contribution of phase i to the NP current is eliminated by imposing $d'_{NP_i} = 0$, and checking if i_{NP} using (12) changes its sign,

i.e., $i_{NP} < 0$. The phases that meet this condition can be chosen to switch in three levels. In a three-phase system, there will be one or two phases that meet this requirement.

If only one phase can change the direction of the NP current, then that phase will be chosen to switch in three levels. In the case that two phases have the capacity to change the direction of the NP current, the phase with minimum absolute value of the current is chosen to switch in three levels. This will minimize the switching power losses.

It is assumed that phase k is chosen to switch in three levels, and the other two phases are indicated as phases l and m . The duty cycles for phases l and m will remain unchanged, i.e., those calculated using (9)-(11), as both phases will be switching in two levels.

Calculation of the duty cycles for the phase that is switching in three levels, including feedforward compensation, is provided in the Appendix. The duty cycles for phase k :

$$d'_{NP_k} = \frac{i_{NP}^* - d'_{NP_l} i_l - d'_{NP_m} i_m}{i_k} \quad (15)$$

$$d'_{h_k} = \frac{v_k}{2} + \frac{(1 - d'_{NP_k}) v_{C1}}{V_{dc}} \quad (16)$$

$$d'_{l_k} = 1 - d'_{NP_k} - d'_{h_k} \quad (17)$$

If the duty cycle calculated for d'_{NP_k} using (15) is negative, then d'_{NP_k} is imposed to be zero and d'_{h_k} and d'_{l_k} are calculated with this assumption from (16) and (17), respectively. Under this condition, phase k will be switching between the upper and lower dc-link rails. The sign of the NP current will be such that it helps capacitor voltage balance, although the reference current (13) will not be achieved.

- e) Case-V. If $v_{C1} > V_{Cmax}$ and $i_{NP} < 0$

In this case, the NP current will charge the lower dc-link capacitor further, which is already charged above the maximum voltage limit (V_{Cmax}). The NP current (i_{NP}) and the reference NP current (i_{NP}^*) have opposite signs, similar to Case-IV, though the directions of the currents are opposite between these two cases. Again, in this case, one phase has to switch in three levels to be able to change the direction of the NP current. The process of determining the phase that switches in three levels and the corresponding duty cycles will be the same as in Case IV.

The calculated duty cycles are then compared with a carrier signal in order to produce the switching pulses for all the power devices of the NPC converter. CB1 PWM technique mentioned in [25] has been utilized in this paper for generating the switching pulses. Fig. 4 shows the waveforms of carrier and reference feedforward compensated duty cycles for phase 'a'. The same carrier is employed for generating the switching pulses for phase 'b' and 'c'.

Fig. 4. Waveforms of carrier and reference feedforward compensated duty cycles.

TABLE I
EXPERIMENTAL PARAMETERS

Parameter	Value
DC-link voltage, V_{dc}	300 V
DC-link capacitors (each), C	130 μ F
Carrier frequency, f_s	2 kHz
AC-side frequency, f	5 Hz

III. EXPERIMENTAL RESULTS

The proposed modulation technique is tested on a laboratory hardware prototype, constituted by a three-phase three-level NPC converter feeding a star-connected R-L load. The experimental parameters of the system are provided in Table I. The ac-side frequency is chosen 5Hz so as to obtain noticeable capacitor voltage ripples with the corresponding value of dc-link capacitor. Several tests are carried out on the prototype to validate the proposed technique.

A. Balanced Load Conditions

Fig. 5(a) shows the waveforms of capacitor voltages (v_{C1} and v_{C2}), line-to-line voltage (v_{ab}) and load currents (i_a , i_b and i_c) at modulation index $m=1$ using CBPWM [18], while Fig. 5(b) shows the waveforms using three-level modulation [22]. A balanced R-L load with the parameters $R=25\Omega$ and $L=6.3\text{mH}$ is star-connected to the converter, with switch S open. As it can be seen from these figures, using CBPWM, the capacitor voltages have large low-frequency ripples, while using three-level modulation, the low-frequency ripples are eliminated.

Figs. 6 and 7 show waveforms for the proposed technique for different modulation indices (m) under the same loading conditions. Fig. 6 shows the results when the limits of the capacitor voltages are defined as $[0.5V_{dc} \pm 5\%]$, i.e., [142.5V, 157.5V], for modulation indices $m=1$, $m=0.7$ and $m=0.4$. In Figs. 6(a) and 6(b), the proposed modulation technique changes between CBPWM and three-level modulation, while in Fig. 6(c) the modulation operates only in CBPWM as the capacitor voltages are within the specified limits even though all the phases switch in two levels.

The waveforms in Fig. 7 are obtained by applying the proposed modulation technique with voltage range $[0.5V_{dc} \pm 10\%]$, i.e., [135V, 165V]. Similar to the previous case, for

Fig. 5. Balanced load with $m=1$ using: (a) CBPWM and (b) three-level modulation.

Fig. 6. Balanced load using proposed technique with capacitor voltage range $[0.5V_{dc} \pm 5\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

Fig. 7. Balanced load using proposed technique with capacitor voltage range $[0.5V_{dc} \pm 10\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

$m=1$ and $m=0.7$, the proposed modulation switches between CBPWM and three-level modulation and for $m=0.4$, it operates with CBPWM all the time. As it can be observed from Figs. 6 and 7, for most of the cases the capacitor voltages are maintained within the specified range and the load currents are sinusoidal despite capacitor voltage imbalances, which is achieved thanks to the implemented feedforward compensation. However, in Figs. 6(a) and 7(a), the capacitor voltages go a bit beyond the predefined band. This is due to the presence of switching ripples, which can be easily eliminated by increasing the switching frequency.

B. Unbalanced Load Conditions

Fig. 8(a) shows the same waveforms with an unbalanced load ($R_{a,b}=25\ \Omega$, $R_c=50\ \Omega$ and $L_{a,b,c}=6.3\text{mH}$) and switch **S** open at $m=1$ using CBPWM [18], while Fig. 8(b) shows the

waveforms using three-level modulation [22]. The capacitor voltage ripples are almost double with this unbalanced load than with the balanced load (Fig. 8(a)). Using three-level modulation, the capacitor voltages are balanced though at the price of more switching in three levels, thereby, increased switching losses.

Figs. 9 and 10 show waveforms for the proposed technique operating with the same unbalanced load. These results demonstrate that the proposed modulation can operate under unbalanced conditions, while maintaining the capacitor voltages within V_{Cmax} and V_{Cmin} and generating sinusoidal output currents.

C. Initial Capacitor Voltage Imbalances

An initial voltage imbalance is forced on the dc-link capacitors, such that $V_{C1}=200\text{V}$ and $V_{C2}=100\text{V}$ under balanced

Fig. 8. Unbalanced load with $m=1$ using: (a) CBPWM and (b) three-level modulation.

Fig. 9. Unbalanced load using proposed technique with capacitor voltage range $[0.5V_{dc} \pm 5\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

Fig. 10. Unbalanced load using proposed technique with capacitor voltage range $[0.5V_{dc} \pm 10\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

R-L load condition with switch S open. Figs. 11 and 12 show capacitor voltages (v_{C1} and v_{C2}), line-to-line voltage (v_{ab}) and load currents (i_a , i_b and i_c) for different modulation indices (m). The capacitor voltages are quickly regulated within the interval $[V_{Cmin}, V_{Cmax}]$. Therefore, the proposed modulation technique has the capability to regulate the capacitor voltages irrespective of the initial voltage imbalance.

D. Nonlinear Load Conditions

The switch S in Fig. 1 is closed to connect the half-bridge diode rectifier feeding a resistive load ($R_s=104\Omega$) to the NPC converter in addition to the star-connected R-L load ($R=25\Omega$ and $L=11.3\text{mH}$). The added nonlinear load is highly enriched in second-harmonic currents which tends to cause capacitor voltage instability [11]. Figs. 13 and 14 show waveforms for the proposed technique for different modulation

indices (m). Fig. 13 shows the results when the limits of the capacitor voltages are defined as $[0.5V_{dc} \pm 5\%]$ for modulation indices $m=1$, $m=0.7$ and $m=0.4$. The proposed modulation technique applies three-level modulation for some intervals with $m=1$ and $m=0.7$, while for $m=0.4$ the modulation operates only in CBPWM as the capacitor voltages are within the specified limits therefore all the phases switch in two levels. Fig. 14 shows the same waveforms with the capacitor voltage limits as $[0.5V_{dc} \pm 10\%]$. From these figures, it is clear that the proposed modulation scheme is able to limit the capacitor voltages within the predefined voltage limits even when operating with nonlinear loads that inject second-harmonic currents.

E. Distortion Analysis

Fig. 15 shows the harmonic spectra of a line-to-line voltage with CBPWM, three-level modulation and the proposed mod-

Fig. 11. Initial voltage imbalance operating with capacitor voltage range $[0.5V_{dc} \pm 5\%]$: (a) $m=1$ and (b) $m=0.7$.

Fig. 12. Initial voltage imbalance operating with capacitor voltage range $[0.5V_{dc} \pm 10\%]$: (a) $m=1$ and (b) $m=0.7$.

Fig. 13. Nonlinear load using the proposed technique with capacitor voltage range $[0.5V_{dc} \pm 5\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

Fig. 14. Nonlinear load using the proposed technique with capacitor voltage range $[0.5V_{dc} \pm 10\%]$: (a) $m=1$, (b) $m=0.7$, and (c) $m=0.4$.

Fig. 15. Harmonic spectra of v_{ab} at $m=0.7$ with (a) CBPWM, (b) three-level modulation, (c) proposed modulation technique with capacitor voltage range $[0.5V_{dc} \pm 5\%]$ and (d) proposed modulation technique with capacitor voltage range $[0.5V_{dc} \pm 10\%]$.

ulation technique with two different capacitor voltage limits (V_{Cmax} and V_{Cmin}). In Fig. 15(a), low-frequency harmonics are present near the fundamental component of v_{ab} , i.e. between 0 Hz to 100 Hz, due to capacitor voltage imbalances. As a result, the weighted total harmonic distortion (WTHD) obtained under CBPWM is higher. Such low-frequency harmonics do not exist under the proposed modulation scheme as feedforward compensation is employed. The three-level modulation technique produces voltages with larger total harmonic distortion (THD) compared to CBPWM, as it requires a phase to switch in three-levels within a switching period all the time [22]. The proposed modulation technique is a combination of CBPWM and three-level modulation and thereby, shows THD and WTHD between them. When defining a wide tolerant band, the technique operates with CBPWM all the time because the capacitor voltages fit within the band, resulting in lower THD values. If $V_{Cmax}=V_{Cmin}=V_{dc}/2$, i.e. the tolerance band is zero, the proposed modulation technique operates in three-level mode all the time, as in [22].

Fig. 16 shows the variation of weighted THD (WTHD) values with different modulation indices operating with a balanced linear load. For low modulation indices the capacitor voltage ripples are small and CBPWM is applied all the time. This is why the curves overlap each other. On the other hand, when the modulation index is larger, a small tolerance band produces higher WTHD values because of the larger intervals operating in three levels. In any case, the increase of WTHD is relatively small because the harmonics that cause additional distortion are at relatively high frequencies (around

Fig. 16. WTHD of the line-to-line voltage waveform at different modulation indices for a balanced load with proposed modulation technique.

the switching frequency and beyond).

F. Power Losses Analysis

When a phase switches in three-levels, the switching losses increase because there are more transitions involved in a switching period. The proposed modulation technique reduces the intervals where one phase switches in three levels as compared to [15], [21], [22]. It is hence a trade-off solution between switching power losses and capacitor voltage ripples. A power loss analysis is performed considering the insulated-gate bipolar transistor (IGBT) DIM1200SM17-E000, having a maximum collector-emitter voltage of 1700V and a continuous collector current of 1200A. The manufacturer's datasheet provides a curve to calculate the energy dissipated in every turn-on (E_{on}) and turn-off (E_{off}) of the semiconductor as a function of the current and for a given collector-emitter voltage

Fig. 17. Equivalent switching frequency under: (a) CBPWM, (b) three-level modulation and (c) proposed modulation scheme with capacitor voltage range $[0.5V_{dc} \pm 6.67\%]$.

(V_{CE}). The authors used the least square method (implemented in a toolbox supplied by MATLAB) to find equations that fit the curves. The switching pulses generated by comparing the carrier and reference duty cycles helps in identifying the switching instants and conduction times of IGBTs and diodes. Using this data and the loss equations, the switching and conduction losses are calculated under different modulation schemes. The switching frequency is 2.5kHz, rated power is 1.5MW, dc-link voltage is 1500V, and the limits of the capacitor voltages are defined as $[0.5V_{dc} \pm 6.67\%]$, i.e., [700V, 800V].

Fig. 17 shows the equivalent switching frequency for CBPWM, three-level modulation and proposed modulation technique under different modulation indices and load phase angles. From these figures, it is clear that the equivalent switching frequency of the proposed modulation lies between CBPWM and three-level modulation. Fig. 18 shows the power losses of the proposed modulation technique and CBPWM [18] under different modulation indices and load phase angles. Fig. 18(a) shows that the conduction losses are similar for both cases. The small differences between these modulation techniques are due to the kind of device that is conducting (IGBT or diode). In Fig. 18(b) the switching losses of the two techniques are equal when the proposed modulation technique operates with CBPWM predominantly. When the proposed modulation applies three-level modulation during some intervals, the obtained switching losses, and hence total losses, are higher with the proposed modulation technique.

In Fig. 19, the proposed modulation technique is compared with the three-level modulation [22]. Figs. 19(b) and (c) show that the switching and total power losses, respectively, produced with the proposed modulation technique are less than when three-level modulation is applied. This is due to the fact that the proposed modulation technique does not operate solely in three-level mode, and only for some intervals if required. From Figs. 18 and 19, it is demonstrated that the switching and total losses with the proposed modulation technique are, in general terms, higher and lower than those produced with CBPWM and three-level modulation, respectively.

IV. CONCLUSION

In this paper, a new modulation technique with feedforward compensation has been proposed. With this technique, a maximum variation of the dc-link capacitor voltages is defined. If the capacitor voltages go beyond the limits, one phase of the converter switches in three levels to lead the capacitor voltages

within the tolerance band again. A feedforward compensation is also implemented in order to compensate for the negative effect of capacitor voltage imbalances on the output voltages. With the proposed modulation technique, the power losses are the same as those produced with CBPWM when the capacitor voltages are within the limits, and a bit higher if the capacitor voltages tend to go beyond the limits. In any case the losses are always lower than those produced by modulation strategies where one phase is switching in three levels all the time. Hence, the proposed modulation technique represents a trade-off solution between voltage controllability and switching power losses. Experimental results operating with balanced, unbalanced and nonlinear loads have been obtained to verify the capability of the modulation technique in regulating the capacitor voltages within the specified limits. The modulation technique has also been tested under strong initial capacitor voltage imbalances. Limiting the capacitor voltage ripples helps in the design of the NPC converter, since the maximum voltage that the dc-link capacitors and the power semiconductors have to withstand is predefined.

APPENDIX

FEEDFORWARD COMPENSATED DUTY CYCLES

The locally-averaged output voltage of one phase of the converter (phase i) respect to the NP is given by:

$$v_{i0} = d_{hi}v_{C2} - d_{li}v_{C1} \quad \text{for } i = \{a, b, c\}. \quad (18)$$

If phase i is switching in two levels and the reference signal is positive, phase i will be switching between the positive rail and the NP [24], such that,

$$d_{li} = 0 \quad \text{and} \quad v_{i0} = d_{hi}v_{C2}. \quad (19)$$

Assuming the capacitor voltages are balanced, i.e., $v_{C1}=v_{C2}=V_{dc}/2$:

$$v_{i0} = d_{hi} \frac{V_{dc}}{2}. \quad (20)$$

However, if the capacitor voltages are unbalanced, the duty cycle needs to be compensated to produce the same reference voltage at the output, as follows:

$$v_{i0} = d'_{hi}v_{C2}. \quad (21)$$

The compensated duty cycle can be obtained from equating (20) and (21):

$$d'_{hi} = d_{hi} \frac{V_{dc}}{2v_{C2}} \quad (22)$$

Fig. 18. Power losses comparison between the proposed modulation technique and CBPWM [18]. (a) Conduction, (b) switching, and (c) total power losses.

Fig. 19. Power losses comparison between the proposed modulation technique and the three-level modulation [22]. (a) Conduction, (b) switching, and (c) total power losses.

The other duty cycles for phase i are calculated as follows:

$$d'_{l_i} = d_{l_i} = 0 \quad \text{and} \quad (23)$$

$$d'_{NP_i} = 1 - d'_{h_i}. \quad (24)$$

The duty cycles (22)-(24) are feedforward compensated; therefore, they produce the reference output voltage even under capacitor voltage imbalances.

Similarly, if the reference signal is negative and phase i is switching in two levels, the corresponding phase will switch between the negative rail and the NP, such that:

$$d_{h_i} = 0 \quad \text{and} \quad v_{i0} = d_{l_i} v_{C1}. \quad (25)$$

Again, assuming that the capacitor voltages are balanced, i.e., $v_{C1} = v_{C2} = V_{dc}/2$:

$$v_{i0} = d_{l_i} \frac{V_{dc}}{2}. \quad (26)$$

However, for producing the same reference voltage when the capacitor voltages are imbalanced, the duty cycle needs to be compensated as:

$$v_{i0} = d'_{l_i} v_{C1}. \quad (27)$$

From (26) and (27), the feedforward compensated duty cycles are calculated as follows:

$$d'_{l_i} = d_{l_i} \frac{V_{dc}}{2v_{C1}} \quad (28)$$

$$d'_{h_i} = d_{h_i} = 0 \quad (29)$$

$$d'_{NP_i} = 1 - d'_{l_i}. \quad (30)$$

For the phase that is switching in three levels, calculation of the compensated duty cycles requires more elaboration, and it is proposed in this paper for the first time.

Let's suppose the phase that is switching in three levels is phase c , while phases a and b are switching in two levels.

Phase c has to produce the desired locally-averaged output voltage for that phase, i.e.:

$$v_{c0} = d'_{h_c} v_{C2} - d'_{l_c} v_{C1}. \quad (31)$$

Simultaneously, the NP current has to meet the NP current reference:

$$i_{NP} = d'_{NP_a} i_a + d'_{NP_b} i_b + d'_{NP_c} i_c = i_{NP}^* \quad (32)$$

Since phases a and b are switching in two levels, their duty cycles are calculated using (22)-(24) and (28)-(30). From (32), the NP duty cycle for phase c can be obtained as follows:

$$d'_{NP_c} = \frac{i_{NP}^* - d'_{NP_a} i_a - d'_{NP_b} i_b}{i_c} \quad (33)$$

Equation (33) provides the NP duty cycle for phase c to achieve the desired NP current. The other duty cycles for phase c (i.e., d'_{h_c} and d'_{l_c}) need to be calculated with the objective of generating the reference voltage for that phase, even under unbalanced dc-link capacitor voltages.

Since the sum of the three duty cycles has to be one at all times, the duty cycle for connecting phase c to the lower voltage level is:

$$d'_{l_c} = 1 - d'_{h_c} - d'_{NP_c}. \quad (34)$$

Substituting (34) in (31), and taking into account that $v_{C1} + v_{C2} = V_{dc}$:

$$d'_{h_c} = \frac{v_{c0} + (1 - d'_{NP_c}) v_{C1}}{V_{dc}} \quad (35)$$

The output voltage for phase c is related to its normalized magnitude as follows:

$$v_{c0} = v_c \frac{V_{dc}}{2} \quad (36)$$

Therefore, substituting (36) in (35):

$$d'_{h_c} = \frac{v_c}{2} + \frac{(1 - d'_{NP_c}) v_{C1}}{V_{dc}}. \quad (37)$$

The feedforward compensated duty cycles for the phase that is switching in three levels (phase c in this example) are given by (33), (34) and (37).

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