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Enhancing the Natural Voltage Balancing Capability of Neutral-Point-Clamped Converters under Carrier-Based Pulsewidth Modulation

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Abstract—In this paper, a new modulation technique is presented which aims to enhance the natural voltage balancing capability of neutral-point-clamped converters. The traditional carrier-based pulsewidth modulation technique with zero-sequence injection faces many drawbacks, namely, its inability to balance initial capacitor voltage imbalances quickly and the divergence of the capacitor voltages in the presence of nonlinear loads with even harmonics. This paper aims to find a trade-off between voltage balance performance and switching losses by reducing the difference between the average capacitor voltages without incorporating any external circuitry. A reference NP current is generated using the average difference between the capacitor voltages. Depending on the reference NP current and predicted NP current, appropriate duty cycles are applied to switch the three phases. These duty cycles are directly linked to the voltage unbalance between the capacitor voltages and thus provides the necessary push to mitigate deviations in natural balancing characteristics. To validate the proposed modulation technique, simulation results are presented for linear loads as well as for nonlinear loads with even harmonics.

Index Terms—Neutral-point-clamped converter, natural balancing, carrier-based pulsewidth modulation, three-level modulation, moving average filter.

I. INTRODUCTION

In the last decades there has been a drastic increase in the popularity of the neutral-point-clamped (NPC) converter (Fig. 1) due to its inherent advantages over the conventional two-level voltage source converter [1], [2]. Nowadays, NPC converters are widely employed for various applications like static compensator (StatCom) devices, ac drives, solar and wind conversion systems, etc.

However, there are many issues which need to be addressed while operating the NPC converter [3], [4]. The biggest challenge is to maintain equal voltages among the dc-link capacitors. Low frequency neutral point (NP) ripples are also prominent at high modulation indices and low power factor loads which further escalates the voltage unbalance among the dc-link capacitors. Moreover, the capacitor voltages tend to diverge in the presence of nonlinear loads with even harmonics. Therefore, in order to handle these voltage unbalances, the power devices and the dc-link capacitors are generally oversized. Many attempts have been made in the literature to address this issue. In [5], a compensation loop is incorporated with double-width pulsewidth modulation so as to provide natural balancing to the system. Natural balancing refers to the capability of the NP voltage to settle to half of the

dc link voltage naturally [6]. However, finding an optimal compensation signal with the system's intrinsic limitations is a cumbersome task. Other natural voltage balancing techniques using external circuits have also been proposed in the literature [7], [8], however the addition of extra circuit components increases the system's footprint and cost.

In [9], a space-vector pulsewidth modulation technique based upon virtual vectors is used to balance the capacitor voltages for all operating conditions. However, the obtained output voltages show higher frequency distortions along with higher switching losses. Pou *et al.* [10] proposed a carrier-based pulsewidth modulation (CBPWM) strategy incorporating a zero sequence signal with improved voltage balancing performance and 15% larger output voltage amplitudes than sinusoidal PWM. In this paper, the modulation strategy proposed in [10] has been referred to as CBPWM for reference. In [11], the authors presented a carrier-based three-level modulation technique with the ability to completely eliminate the low frequency ripples at the NP by switching one phase in three levels, that is, the phase switches among the positive rail, negative rail and the NP. However, switching one phase always in three levels results in increased switching losses.

In this paper, a new method to enhance the natural voltage balancing of NPC converters under CBPWM [10] is proposed. The proposed technique aims to balance the average capacitor voltages, thus resulting in lower switching losses as compared to [11] which focuses on balancing the instantaneous capacitor voltages equal to half of the dc link voltage. This technique is basically a trade-off between voltage balance performance and switching losses. A zero sequence voltage is added to the modulation signals in order to balance the capacitor voltages and reduce the voltage ripples at NP. The difference between the average voltages of the two capacitors is utilized to measure the voltage imbalance and to calculate the reference NP current. The required NP current is imposed by switching one phase of the converter in three levels.

Since one leg will be switching in three levels when needed, the proposed technique produces more switching losses to the converter as compared to CBPWM. Some of the major advantages of the proposed technique are:

- No external circuitry is used to enhance the natural voltage balancing capability of the NPC.
- The instantaneous value of the capacitor voltages are not forced to be equal, therefore, the resulting switching

Fig. 1. Three-phase three-level NPC converter feeding a linear and a nonlinear load.

losses are less as compared to the three-level modulation technique.

- The average capacitor voltages are regulated and they do not diverge even operating with nonlinear loads producing unbalancing even harmonics.

The paper is organized as follows. Section II provides the details of the proposed modulation technique. Section III presents simulation results for a three-phase three-level NPC converter. Finally, Section IV summarizes the main conclusions of this work.

II. PROPOSED MODULATION TECHNIQUE

The proposed modulation strategy aims to enhance the natural voltage balancing capability of the NPC converter by balancing the average voltages of the two capacitors. The steps involved in the proposed modulation technique are as follows:

- 1) Calculation of normalized modulation signals.

The original normalized modulation signals are given by:

$$v_{in} = \frac{v_{iREF}}{V_{dc}/2} \quad \text{for } i = \{a, b, c\} \quad (1)$$

where v_{iREF} is the reference voltage for phase i given by the current controller and V_{dc} is the total dc-link voltage.

To fully utilize the dc-link voltage, a zero sequence voltage is added to the modulation signals:

$$v_{off} = -\frac{\max(v_{an}, v_{bn}, v_{cn}) + \min(v_{an}, v_{bn}, v_{cn})}{2} \quad (2)$$

where v_{an} , v_{bn} and v_{cn} are the original normalized modulation signals for phases a , b and c , respectively. The normalized modulation signal with the added zero sequence is indicated as v_i :

$$v_i = v_{in} + v_{off} \quad \text{with } i = \{a, b, c\}. \quad (3)$$

- 2) Calculation of duty cycles under CBPWM.

If a phase is only switching between two consecutive voltage levels in the switching cycle, and the normalized modulation signal is positive, the phase will be switching

between the positive rail and the NP [11]. The duty cycles can be calculated as:

$$d_{hi} = v_i, \quad d_{li} = 0 \quad \text{and} \quad d_{NPi} = 1 - v_i, \quad (4)$$

where d_{hi} , d_{li} and d_{NPi} are the duty cycles for connecting phase i to the high, low and NP dc rails, respectively. If the modulation signal v_i is negative and the phase is switching in two levels, the corresponding phase will switch between the negative rail and the NP. The duty cycles are given by:

$$d_{hi} = 0, \quad d_{li} = -v_i \quad \text{and} \quad d_{NPi} = 1 + v_i. \quad (5)$$

In general terms, the duty cycle connecting to the NP can be calculated as:

$$d_{NPi} = 1 - |v_i|. \quad (6)$$

- 3) Calculation of NP current.

The locally-averaged NP current over a switching cycle is computed as:

$$i_{NP} = d_{NP_a} i_a + d_{NP_b} i_b + d_{NP_c} i_c. \quad (7)$$

- 4) Estimation of average capacitor voltages and reference NP current.

For estimating the average value of the two capacitor voltages, a moving average filter (MAF), with a window length of $T_w = 1/(3f)$ is applied, f being the fundamental output frequency of the converter. As the frequency of capacitor voltage ripples is three times the fundamental frequency, the output of MAF will only have the average difference of the two capacitor voltages, without any ripple content. However, if unbalanced loads were connected to the converter, the window width of the MAF should be increased to $T_w = 1/(f)$, since the capacitor voltages would also include a fundamental output frequency.

Using the difference between the average capacitor voltages, the reference NP current is calculated as follows:

$$i_{NP}^* = C \frac{\Delta v_C}{T_s} \quad (8)$$

where T_s is the switching period, C is the capacitance of each dc-link capacitor, and Δv_C is the locally averaged difference between the two capacitor voltages over a sampling period:

$$\Delta v_C = \overline{v_{C1}} - \overline{v_{C2}}. \quad (9)$$

The calculated reference NP current is then fed to a proportional-integral (PI) controller with K_p as proportional gain and K_i as integral gain to obtain the final reference current i_{NP}^{**} .

- 5) Determination of phases switching in two or three levels and calculation of duty cycles.

Assume that one phase is required to switch in three levels for balancing the two capacitors and the remaining phases switch in two levels as per [11]. For $i_{NP} \geq 0$, choose the phase contributing maximum to the NP current in (7) to switch in three levels, while for $i_{NP} < 0$, choose the phase which has minimum contribution to the

NP current. Suppose phase k is chosen to switch in three levels while phase l and m switch in two levels. Then, imposing $d_{NPk}=0$, the new NP current (i_{NP}') can be calculated using (7). The following ratio z is calculated:

$$z = \frac{i_{NP}^{**}}{i_{NP}'} \quad (10)$$

Depending on the value of z , the different modulation cases are summarized as:

a) Case-I. If $z \geq 0$

In this case, phase k switches in three levels and the NP duty cycle is dependent on the value of i_{NP}^{**} . Using (6), the NP duty cycle when phase k switches in two levels is given as,

$$d_{NPk} = 1 - |v_k|. \quad (11)$$

When phase k switches in all three levels, that is, it is connected to the positive dc rail, negative dc rail and also to the NP and phase l and m switch in two levels, the NP duty cycle for phase k is given by,

$$d_{NPk}' = \frac{i_{NP}^{**} - d_{NPk} i_l - d_{NPk} i_m}{i_k} \quad (12)$$

The difference between the NP duty cycles calculated in (11) and (12) represents the necessary push required to balance the average capacitor voltages. The saturation limits for d_{NPk}' is defined between 0 and 1. The new value of d_{NPk} is evaluated as,

$$d_{NPk} = d_{NPk} - \frac{d_{NPk} - d_{NPk}'}{h} \quad (13)$$

Here, 'h' represents a tuneable gain that determines how aggressive the control action (push) is. Higher values of 'h' leads to the generation of a smaller push, therefore, the average capacitor voltage takes more time to balance equally. On the other hand, smaller values of 'h' produce a larger push.

When the voltage unbalance is large, the difference between d_{NPk} and d_{NPk}' will also be large and the new value of d_{NPk} will be less than its originally calculated value. For smaller voltage unbalances, d_{NPk} and d_{NPk}' will not deviate as significantly therefore the new d_{NPk} will not differ significantly from its originally calculated value.

The new duty cycles for high rail and low rail for phase k are calculated as,

$$d_{lk} = \frac{(1 - d_{NPk} - v_k)}{2} \quad (14)$$

$$d_{hk} = 1 - d_{NPk} - d_{lk} \quad (15)$$

Phase l and m will switch in two levels and will have duty cycles given by (4)-(6).

b) Case-II. If $z < 0$

In this case, the natural balancing tendency of the system is utilized, no external push is given to the system. All the phases switch in two levels and have duty cycles given by (4)-(6). As no phase

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Simulation sampling time, T_s	10 μ s
Carrier frequency, f_s	4 kHz
DC-link voltage, V_{dc}	400 V
DC-link capacitors (each), C	168 μ F
AC-side frequency, f	50 Hz
AC-side load (per-phase), RL	17.5 Ω , 0.25 H
Proportional gain, K_p	1
Integral gain, K_i	5
Gain, h	50

switches in three levels here, the switching losses are the same as CBPWM.

The obtained duty cycles are then compared with a carrier signal in order to generate the switching pulses for all the switches within the NPC converter.

III. SIMULATION RESULTS

The proposed modulation technique is tested in the MATLAB/Simulink environment by using a three-phase three-level NPC converter and a combination of a star-connected R-L load and a nonlinear load constituted by a half-bridge diode rectifier. The simulation parameters of the system are provided in Table I. Several tests are carried out on the prototype to validate the proposed technique.

A. Balanced Linear Load

This test is carried out with switch 'S' open in Fig. 1. Fig. 2 shows line-to-line voltage (v_{ab}), capacitor voltages (v_{C1} and v_{C2}) and load currents (i_a , i_b and i_c) for different modulation indices (m) when an initial voltage imbalance is forced on the dc-link capacitors, such that $V_{C1} = 150$ V and $V_{C2} = 250$ V. It is seen from these figures that the proposed modulation technique has the capability to regulate the capacitor voltages irrespective of the initial voltage imbalance. Moreover, Fig. 3 shows the comparison between the proposed modulation technique and CBPWM. When CBPWM is employed, the natural voltage balancing capability of the capacitors is not sufficient to regulate the voltage at the NP, which results in distortions at the ac side.

B. Combination of Nonlinear Load and Linear Load

The presence of asymmetrical loads like arc furnaces, half-wave rectifiers, electrical discharge devices lead to the distortion of load currents. Such loads when connected to a NPC converter results in high capacitor voltage unbalance under CBPWM. Fig. 4 shows the performance of the proposed technique feeding a combination of nonlinear load with even harmonics with $R_s = 50\Omega$ and a linear load. For this test, the switch 'S' is closed in Fig. 1. It is observed that the capacitor voltages are still regulated and do not diverge. Fig. 5 shows the comparison between CBPWM and the proposed technique feeding the same combination of load. The proposed technique shows better performance than CBPWM in this case.

Fig. 2. Performance of the proposed technique with initial voltage imbalance: (a) $m=0.5$ and (b) $m=1$.

Fig. 3. Comparison between CBPWM and proposed technique with initial voltage imbalance: (a) $m=0.5$ and (b) $m=1$.

Fig. 4. Performance of the proposed technique feeding a nonlinear and linear load: (a) $m=0.5$ and (b) $m=1$.

Fig. 5. Comparison between CBPWM and proposed technique feeding a nonlinear and linear load: (a) $m=0.5$ and (b) $m=1$.

IV. CONCLUSION

In this paper, a new modulation technique is proposed which aims on achieving the same average voltages in each of the dc-link capacitors and, therefore, enhancing the natural voltage balancing capability of the NPC converter. Appropriate duty cycles are given to switch one phase in three levels depending on the capacitor voltage unbalance. The proposed technique is tested on linear load as well as on second harmonic load in the MATLAB/Simulink environment at different modulation indices. The average capacitor voltages obtained do not diverge under any loading conditions. Moreover, a comparison has been presented between the proposed modulation technique and CBPWM which shows that the proposed technique has much better voltage balancing performance.

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