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2019

Rodriguez, E., Farivar, G. G., Pou, J., Tafti, H. D., Townsend, C. D., & Vazquez, S. (2019). A generalized voltage balancing algorithm for modular multilevel cascaded converters. IEEE Energy Conversion Congress and Exposition (ECCE) 2019. doi:10.1109/ECCE.2019.8912648

<https://hdl.handle.net/10356/136973>

<https://doi.org/10.1109/ECCE.2019.8912648>

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A Generalized Voltage Balancing Algorithm for Modular Multilevel Cascaded Converters

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Abstract—The use of an inter-cell voltage balancing scheme to evenly distribute the total dc-link voltage among the multiple floating capacitors is crucial in modular multilevel cascaded converters (MMCs). This paper presents an intuitively simple and computationally efficient sorting-based modulation algorithm for capacitor voltage balancing applicable to any MMC. The proposed modulation stage is inherently decoupled from the upper-level control scheme and it is able to both generate the required converter output voltage and balance the capacitor voltages suitably. Furthermore, it maintains a constant harmonic performance even as the number of switching transitions is varied to achieve voltage balance under different loading conditions with minimum incurred switching losses. The effectiveness of the proposed algorithm is validated on an experimental seven-level 350-VA single-phase cascaded H-bridge working as a static compensator. In addition, a simulated 350-VA system is used to obtain complimentary results.

Index Terms—Capacitor voltage balancing, cascaded H-bridge (CHB), multilevel converters, static synchronous compensator (STATCOM), virtual voltages

I. INTRODUCTION

Modular multilevel converters represent the leading technology for medium/high power industrial applications due to their high efficiency and harmonic performance [1], [2]. Particularly, modular multilevel cascaded converters (MMCs) [3] offer several salient features which make them potential candidates for various industrial applications, including high-voltage direct-current transmission systems, flexible-alternating-current transmission systems, integration of renewable energy sources, and variable-speed drives. The most attractive property of MMCs in comparison with other multilevel converters is their modular configuration, which allows scalability to different power and voltage levels without having to necessarily increase the submodule (SM) voltage rating or utilise a step-up transformer.

Another important feature of the MMCs is the possibility of employing floating capacitors as dc-sources. The task of balancing the capacitor voltages within the string of SMs, which is subsequently referred to as an “arm”, is relatively simple in MMCs. Nevertheless, recent research studies [4], [5] show that there is still room for improvements, especially in relation to achieving secondary control objectives such as minimizing losses, avoiding harmonic deterioration and incurring low computational times. For instance, model predictive control-based algorithms are well suited to accommodate the above-mentioned multiple control objectives in detriment of a

relatively high number of computations required to find the optimal control inputs [6]–[8].

Phase-shifted carrier pulse-width modulation (PSC-PWM) is a popular scheme employed by industry due to its inherent capacity to distribute both conduction and switching losses evenly among the semiconductor devices. However, harmonic performance degradation and control interactions represent the main drawbacks of this modulation strategy [9]. This is because multiple individual control loops are needed for voltage balancing purposes [10]. On the other hand, sorting-based modulation schemes [7] do not suffer from control interactions and harmonic degradation, but they require an additional algorithm in order to achieve loss equalisation [11].

Reducing per-device switching frequencies is important in order to reduce associated switching losses. As presented in [12], utilising a standard sorting algorithm in which capacitor voltages are fictitiously separated within the sorting stage by adding a voltage offset ΔK to the voltages of those SMs that are inserted in the arm, achieves a significant reduction in the average switching frequency.

In this paper, a general modulation technique and an inter-cell voltage balancing scheme for the MMC is presented. In the proposed scheme, there is a base switching frequency determined by the carrier frequency, which fixes the harmonic spectrum of the total PWM output voltage from the converter. Similar to [12], the number of transitions incurred each execution step, which requires a change of the output voltage, depends on the feedback gain ΔK . The novelty of the proposed voltage balancing scheme is to extend the original idea proposed in [12] to the case of H-bridge/bipolar SMs. In contrast to [13], which also utilises the feedback gain ΔK , the proposed scheme does not limit the subset of available switching redundancies that exist for each discrete output voltage vector. In other words, cell inversion capability [14] is not constrained in the proposed scheme (i.e., all the SMs can generate ‘-1’, ‘0’ or ‘+1’ state at any time during the fundamental period), which provides greater flexibility to balance the capacitor voltages. The benefits of cell inversion have been demonstrated to extend the operating region, especially during unbalanced load conditions [15]. Therefore, superior voltage balancing capability is expected. Furthermore, the gain ΔK will be shown to be an effective mechanism to trade-off between cell inversion capability and switching losses.

Although the proposed balancing scheme is applicable to any converter based on the series connection of multiple half-

Fig. 1. (a) Circuit diagram of a CHB power converter arm, and (b) proposed voltage balancing algorithm with restricted number of commutations and cell inversion capability.

bridges or H-bridges, this paper will focus on the cascaded H-bridge (CHB) converter for static synchronous compensator (StatCom) applications, which represents a challenging case due to the absence of an external voltage source to regulate each SM capacitor voltage. The proposed voltage balancing scheme is validated via simulations and experiments on a seven-level 350-VA single-phase CHB-based StatCom prototype.

II. APPLICATION OF THE CHB CONVERTER TO A STATCOM SYSTEM

Due to the symmetry among phases of the converter, only a single phase is considered in this paper without loss of generality. Fig. 1(a) shows a CHB power converter arm composed of \$n\$ series-connected SMs. Each of them consists of a floating capacitor with the voltage \$v_{Cj}\$ for \$j \in \{1, 2, \dots, n\}\$, and four conventional power switches that form an H-bridge structure with three possible output voltage levels. The converter is connected to the grid voltage \$v_g\$ through an inductor \$L\$ and its parasitic resistance \$R_L\$.

Assuming capacitor voltage balance (i.e., \$v_{Cj} = v_{clus}/n \ \forall j \in \{1, 2, \dots, n\}\$, where \$v_{clus}\$ denotes the sum of capacitor voltages in the converter arm, i.e., \$v_{clus} = \sum_{j=1}^n v_{Cj}\$) and averaging the converter behavior over a switching period, the following bilinear time-varying system model with continuous state variables is obtained for the inductor current dynamic:

$$L \frac{di_L}{dt} = -R_L i_L + v_{clus} \delta - v_g, \quad (1)$$

where the variable \$\delta\$ denotes the averaged control input of the modulator, and it is given by:

$$\delta(t) = \frac{1}{n} \frac{1}{T_{sw}} \sum_{j=1}^n \int_{t-T_{sw}}^t S_j(\tau) d\tau \in [-1, 1]. \quad (2)$$

This parameter is adjusted by a suitable current controller in order to regulate the converter output current \$i_L\$.

The switching period \$T_{sw}\$ is assumed much lower than the converter system time-constants. The discontinuous function \$S_j = (S_{Aj} + S_{Bj} - 1)\$ represents the instantaneous switching state of the \$j^{th}\$ SM, and it belongs to the set \$\{-1, 0, 1\}\$, being the state of each complementary-operation pair of switches as follows:

$$S_{lj} = \begin{cases} 0 & \text{if the corresponding switch is off} \\ 1 & \text{if the corresponding switch is on} \end{cases}, \quad (3)$$

where \$\forall l \in \{A, B\}\$ and \$\forall j \in \{1, 2, \dots, n\}\$.

III. CAPACITOR VOLTAGE BALANCING ALGORITHM

The proposed sorting-based modulation algorithm for capacitor voltage balancing is depicted in Fig. 1(b), where the thicker arrows represent vectors. To simplify the proposed balancing algorithm, the \$n\$ series-connected SMs are visualized as a collection of 'Type A' and 'Type B' legs, as depicted in Fig. 1(a). The discontinuous control variables \$S_{Aj}\$ and \$S_{Bj}\$ associated with each leg are such that a transition from '0' to '1' always increases the SM PWM output voltage in one step in the positive direction, and vice versa. Thanks to this distinction, the balancing controller is independent of the sign of the converter output voltage. That is, in order to generate the converter top voltage level, all the \$2n\$ legs need to be inserted in the arm, i.e., \$S_{lj} = 1\$ for all \$l \in \{A, B\}\$ and \$j \in \{1, 2, \dots, n\}\$; whereas to create the converter bottom voltage level, all the legs need to be not inserted, i.e., \$S_{lj} = 0 \ \forall l, j\$. Then, the original problem of finding the unknown control input vector \$\mathbf{u} = [S_1 \ S_2 \ \dots \ S_n]^T \in \mathbb{R}^n\$, with \$3^n\$ possible cases, is reformulated as finding the augmented vector \$\mathbf{u}_a = [S_{A1} \ S_{B1} \ S_{A2} \ S_{B2} \ \dots \ S_{An} \ S_{Bn}]^T \in \mathbb{R}^{2n}\$, with \$2^{2n} = 4^n\$ possible cases. The reformulated problem is different from solving the voltage balancing problem in [12] since the H-bridge circuit with two independent legs seen from the sorting stage is not electrically equivalent to two series-connected half-bridges.

The first part of the modulation scheme is not directly associated with how specifically the different capacitors are being used to create the output voltage waveform. It only provides the (integer) number of switching legs to be inserted into the arm, which belongs to the set $\{0, 2n\}$, by the sorting-based voltage balancing algorithm. The two discrete voltage levels that reproduce the given reference $\eta = \frac{\delta+1}{2}2n \in [0, 2n]$ on average over a switching period are obtained comparing η with a carrier waveform. Phase-disposition PWM (PD-PWM) technique with $2n$ carriers is used due to its inherent ability to concentrate energy at triplen harmonics that cancel between phases, thus leading to a better trade-off between harmonic performance and losses compared to PSC-PWM [16], [17].

The operation of the proposed balancing controller is described next.

- First, the vector comprising the n capacitor voltages of the arm, $\mathbf{v}_C = [v_{C1} \ v_{C2} \ \dots \ v_{Cn}]^T \in \mathbb{R}^n$, is multiplied by the sign of the arm current (i_L) under the convention that a positive sign denotes an arm current that is suitable to charge capacitors in ‘Type B’ legs and discharge capacitors in ‘Type A’ legs.

- The n -dimensional virtual voltage vector

$$\mathbf{v}'_C = \text{sgn}(i_L) \mathbf{v}_C, \quad (4)$$

is split into two equal vectors as there are two legs sharing the same capacitor voltage per SM. The sorting algorithm has to deal with $2n$ voltages, which makes sense because there are $2n$ legs in the converter arm. The legs sharing a common capacitor are sorted out according to the capacitor voltage of the SM, but with a very small epsilon ε added to one of them to distinguish between the two legs. The value of epsilon must be very small ($\varepsilon \rightarrow 0$) to avoid interfering with the priorities given to the other SMs of the converter arm. More importantly, ε should be constant to ensure a sequential utilization of the legs over a fundamental period, which leads to a natural switching loss equalisation among the semiconductor devices in the proposed technique.

- A fictitious separation between the voltages of those inserted legs and the voltages of those not inserted is used. For that purpose, the switching state of each leg S_{lj} multiplied by the gain ΔK (with volt as unit) is used as a feedback signal and added to the respective voltage (see Fig. 1(b)). Indeed, this simple yet effective fictitious separation allows a noteworthy reduction in the number of switching events, hence reducing the per-switch average switching frequency. The virtual voltage in the l^{th} leg of the j^{th} SM seen by the sorting stage is equal to

$$v''_{C,lj} = v'_{C,lj} + S_{lj} \Delta K. \quad (5)$$

- Finally, the $2n$ virtual voltages are processed by two cascaded index sorting structures. Those legs with an activation order below or equal to the number of required legs indicated by the modulator are the legs that are scheduled to be inserted in the next control/sampling period.

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Symbol	Definition	Value
$\hat{V}_g$	Grid Voltage Nominal Amplitude	$110\sqrt{2}$ V (1 p.u.)
S_g	Nominal Power	350 VA (1 p.u.)
n	Number of H-Bridges per Arm	3
f_g	Grid Frequency	50 Hz
$V_{C,\max}^*$	Peak Capacitor Voltage Reference	57 V
C	Capacitance per H-Bridge	0.26 mF
L	Interface Filter Inductance	5 mH
f_c	Carrier Frequency	500 Hz
$2nf_c$	Equivalent Switching Frequency	3 kHz
f_s	Control/Sampling Frequency	6 kHz

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, some simulation and experimental results are presented. The parameters of the scaled-down StatCom prototype are given in Table I. The control scheme implemented is the same than that used in [18], which consists of a cascade control structure based on the instantaneous power theory [19]. A performance comparison between the standard individual capacitors’ voltage controller based on PSC-PWM [20] and the proposed sorting-based modulation algorithm has been conducted. The carrier frequency in the proposed scheme is $2n$ -times higher than that used in the PSC-PWM strategy in order to obtain the same equivalent switching frequency in the synthesized PWM converter output voltage [17]. To compare switching loss performance, the instantaneous values of capacitor voltages and arm current at the time of each switching event are accounted for [21], rather than just the number of switching transitions incurred. For this purpose, the following normalized metric is used:

$$L_{sw} = \frac{1}{4nT_e} \sum_{k=1}^{T_e f_s} \sum_{l \in \{A, B\}} \sum_{j=1}^n 2\Delta S_{lj}[k] |i_L[k]| v_{Cj}[k], \quad (6)$$

with

$$\Delta S_{lj}[k] = |S_{lj}[k] - S_{lj}[k-1]|, \quad (7)$$

where T_e is the evaluation time and f_s is the control/sampling frequency. The term $\Delta S_{lj}[k]$ is equal to ‘1’ if a switching event is detected at the start of the k^{th} control period in the switch S_{lj} belonging to the l^{th} leg of the j^{th} SM, and it is multiplied by ‘2’ in order to account for the complementary transition of its pair $\bar{S}_{lj}$. The division by ‘ $4n$ ’ in (6) is to normalise the metric to the total number of switches in the converter arm. Similarly, the average switching frequency of the semiconductor devices is defined as

Fig. 2. Simulated capacitor voltages: (a) proposed PD-PWM without restricted commutations ($\Delta K = 0$ V) and $2n \cdot 500$ Hz carrier frequency, (b) proposed PD-PWM with restricted commutations ($\Delta K = 1000$ V) and $2n \cdot 500$ Hz carrier frequency, and (c) PSC-PWM with 500 Hz carrier frequency [20].

Fig. 3. Simulated loss performance using (6): (a) proposed PD-PWM without restricted commutations ($\Delta K = 0$ V) and $2n \cdot 500$ Hz carrier frequency, (b) proposed PD-PWM with restricted commutations ($\Delta K = 1000$ V) and $2n \cdot 500$ Hz carrier frequency, and (c) PSC-PWM with 500 Hz carrier frequency [20].

TABLE II
SUMMARIES OF SIMULATION RESULTS IN A SINGLE-PHASE CHB INVERTER

Modulation Technique	Switching Frequency $\bar{f}_{sw}$ (Hz)	%WTHD Inverter Voltage	%THD Arm Current	Loss (L_{sw})
Proposed nonrestrictive PD-PWM	1270	0.33	7.35	2.77e5
Proposed restrictive PD-PWM	580	0.33	7.39	1.25e5
PSC-PWM [20]	609	0.36	7.52	1.33e5

$$\bar{f}_{sw} = \frac{1}{4nT_e} \underbrace{\sum_{k=1}^{T_e f_s} \sum_{l \in \{A, B\}} \sum_{j=1}^n 2\Delta S_{lj}[k]}_{\text{Total number of switching transitions}}. \quad (8)$$

The capacitor voltages and the power loss performance are illustrated in Figs. 2 and 3, respectively. A capacitance value to obtain 60% peak-to-peak voltage ripple has been adopted, which represents a low-capacitance type StatCom (LC-StatCom) [18]. It is worth noting that due to the feedback gain value utilised in the proposed PD-PWM with restricted commutations ($\Delta K = 1000$ V), a trade-off is effectively enforced between the voltage balancing capability and semiconductor losses, as desired. In Fig. 3, the thickest line represents the normalised metric defined in (6), whilst the other lines represent the switching losses incurred by each individual leg. It should be noted that a switching loss equalisation among the $2n$ legs is achieved in the proposed technique.

Table II shows relevant performance indicators for each modulation technique when using a single-phase CHB. It can be deduced that the proposed modulation technique with restricted number of switching commutations presents a superior performance to the proposed nonrestrictive case (similar

Fig. 4. General performance of the StatCom during a sudden reactive power change at time $t = t_0$ when the restricted PD-PWM scheme is used.

to [12] for the half-bridge case) and a similar performance to that obtained with the industry standard PSC-PWM [20]. However, in the three-phase case, the trade-off between losses and harmonic performance of the proposed scheme can be further improved due to the possible triplen harmonic can-

cellation between phases when using PD-PWM. Furthermore, the proposed restricted PD-PWM, in contrast to many PSC-PWM based schemes, provides inherent decoupling between the modulation and current control stage and better stability margins, as there is no need for individual control loops to balance the capacitor voltages.

The transient performance of an LC-StatCom prototype under a sudden step change in the capacitive reactive power level is illustrated in Fig. 4. As it can be seen, the proposed scheme was able to balance the capacitor voltages effectively even during such a highly dynamic transient event.

V. CONCLUSION

This paper has proposed and experimentally validated a general voltage balancing scheme for MMC configurations. The major advantages of the proposed balancing controller are:

- Individual voltage loops based on proportional plus integral controllers, typically utilised in conjunction with PSC-PWM, are not needed. Therefore, the proposed scheme exhibits better stability margins as it uses the switching redundancies directly instead of relying in feedback loops.
- It is general, easy to implement and expand, it is intuitively simpler than previous works [15], and it exhibits low computational complexity.
- It can deal with multiple steps in the converter output voltage step-size for transient operation. Moreover, as confirmed in this paper, the gain ΔK controls the switching losses while not limiting either the dynamic or harmonic performances of the converter.
- Unlike [13], [15], the proposed scheme does not constrain the subset of available switching redundancies that exist for each discrete output voltage vector.

VI. ACKNOWLEDGMENT

This work was supported by the Singapore Ministry of Education Academic Research Fund Tier 1 under Grant No: 2017-T1-001-213 (RG 90/17).

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