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A 10-bit 300MS/s 5.8mW SAR ADC With Two-Stage Interpolation for PET Imaging

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***Abstract*— In this paper, a high speed low power 2b/cycle successive approximation register (SAR) analog-to-digital converter (ADC) is proposed for medical imaging. The ADC adopts a two-stage differential pair based interpolation technique that can reduce resolution of the capacitive DAC and avoid usage of smaller unit capacitor. A meta-stability immunity technique is proposed to enhance the asynchronous conversion. A design example of 10-bit 2b/cycle SAR ADC with sampling rate up to 300MS/s is fabricated. Dissipating 5.8mW with 1.2V supply and occupying an active area of 0.082mm^2, the measured SFDR and SNDR at Nyquist input are 59dB and 51.5dB respectively. It achieves an effective resolution bandwidth (ERBW) of 360MHz and a figure-of-merit (FoM) of 61fJ/conversion-step.**

***Index Terms*— 2b/cycle, background offset calibration, interpolation, SAR ADCs, medical imaging.**

I. Introduction

Analog-to-digital converter plays an important role in the systems of medical imaging, such as ultrasound imaging [1] , positron emission tomography (PET) imaging and X-ray computed tomography (CT). A block diagram of PET system is shown in Fig. 1. The analog signal is acquired by sensing cell array, amplified by low noise amplifier (LNA) and variable gain amplifier (VGA) and filtered before sampling and digitizing. The ADCs with ultra-low power and compact silicon area facilitate portable applications and large array sensing applications.

It has been proven that high speed successive approximation register (SAR) ADCs have better power efficiency at low and medium resolution [1]-[9], [23]. To achieve higher sampling rate in SAR ADCs, 2-bit/cycle structure is widely used [10]-[15], [24]. However, the 2-bit/cycle structure suffers from heavily increased hardware overhead, including at least 2x DAC array size increasing. Compared to capacitor-DAC based SAR ADC, the resistor-DAC based 2b/cycle SAR ADC [11] consumes static current, which degrades the power efficiency. A non-binary 2b/cycle solution is reported in [13], resulting in a 1GS/s 7-bit single-channel ADC without interleaving. However, the mismatch between input DAC and reference DAC may introduce certain gain mismatch, which needs further calibration.

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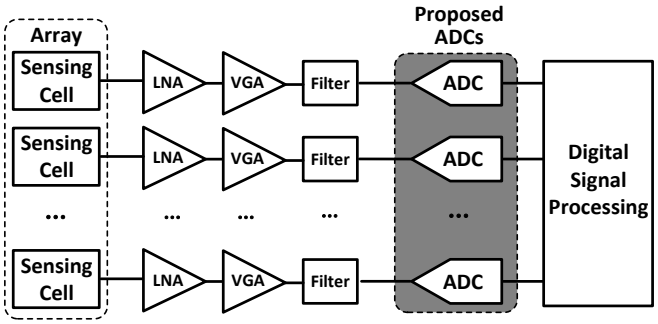

Fig. 1. The block diagram of PET sensing system.

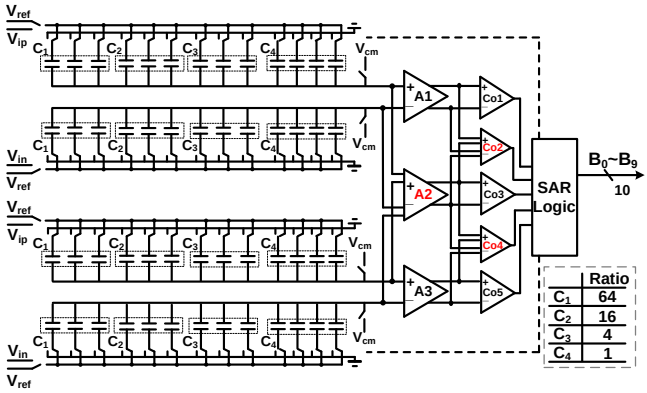

Fig. 2. The architecture of the 2b/cycle SAR ADC, including binary DAC array, interpolated pre-amplifier and comparators.

This work proposes a 300MS/s 10-bit 2b/cycle SAR ADC without interleaving and pipelining. By employing the two-stage interpolation structure that could solve 2 additional bits in last cycle, only two 8-bit capacitive DAC arrays are required to achieve 10-bit resolution. A meta-stability immunity technique is proposed to enhance the robustness of asynchronous conversion. The remainder of the paper is divided into five sections. Section II briefly introduces the proposed SAR ADC architecture. In Section III, the two-stage interpolation for 2b/cycle SAR ADC and the meta-stability immunity technique are described. In Section IV, some building blocks of the ADC are described. The measurement results are given in Section V. Finally, the conclusion is drawn in Section VI.

II. Proposed SAR-ADC Architecture

The block diagram of the proposed 2b/cycle SAR ADC with binary DAC array is shown in Fig. 2. The ADC mainly consists

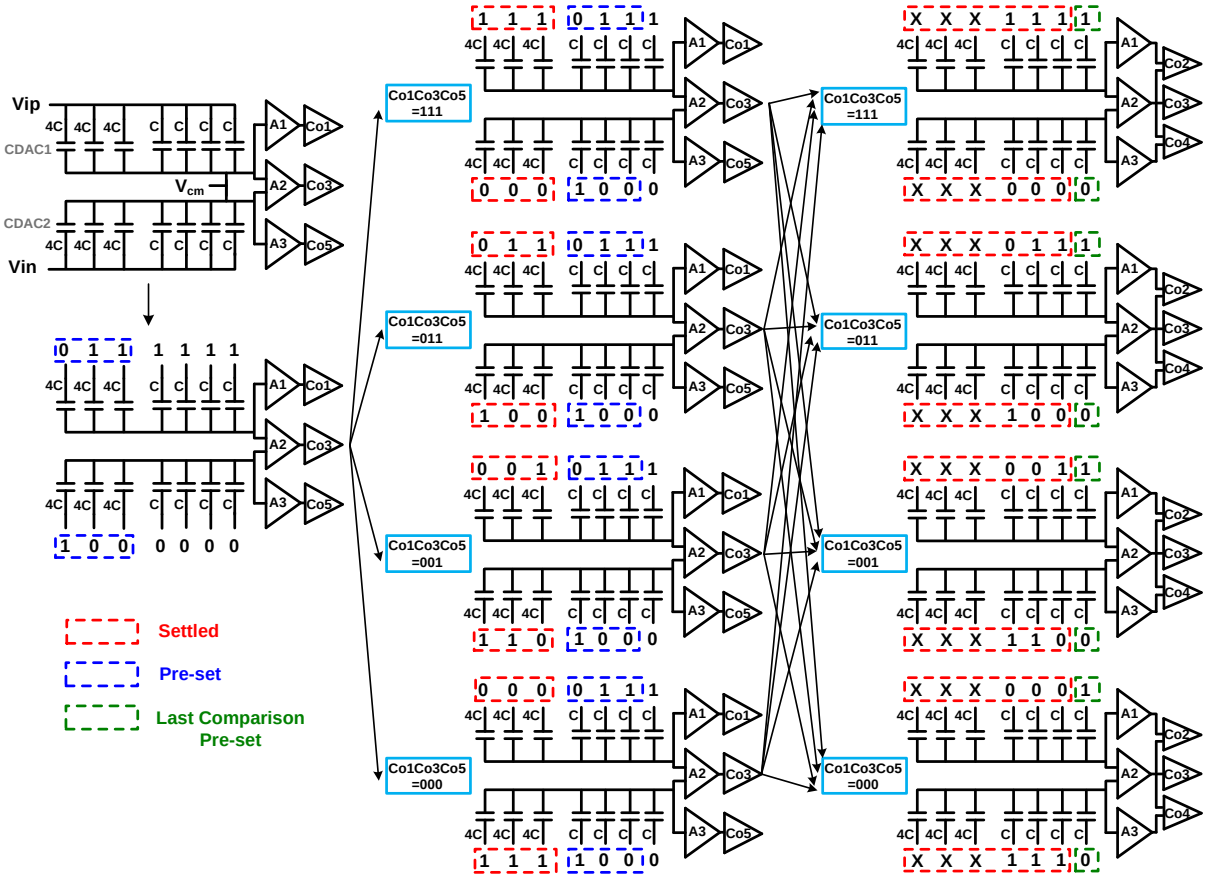

Fig. 3. Proposed switching procedure of a 4-bit DAC array.

of two differential 8-bit DAC arrays, three pre-amplifiers, five parallel comparators and SAR logic. The overall architecture is completely symmetric about the differential input signal. Only two differential capacitive DACs (CDAC1 and CDAC2) array are adopted due to the first-stage interpolation of pre-amplifier A2. Further, two second-stage interpolations of comparators (Co2 and Co4) are presented to reduce the DAC resolution. The two-stage interpolation reduces the resolution of the CDACs by 2 bits. During the initial conversion cycles, the dynamic comparators Co2 and Co4 are in reset phase and only activated in the last cycle. Similarly, the comparators Co1, Co3, Co5 are in reset phase in the last cycle. Therefore, only three dynamic comparators are activated in each cycle without extra power wasted. The three comparators generate 3-bit thermometer code and drive the DAC array directly without binary encoding. The offsets of pre-amplifiers and comparators are calibrated separately in the background to prevent the deterioration of system linearity. Asynchronous timing proved in [18] is applied to further reduce the conversion time and also to avoid high frequency conversion clock generator. A meta-stability immunity technique is proposed to enhance the conversion robustness by avoiding meta-stability caused long cycle scenario. The feedback delay from comparator output to DAC array is not negligible for high speed SAR ADC. The dynamic control logic is adopted in this work to shorten the feedback delay. All the blocks are implemented in a fully differential structure, so that the common mode noise from input, power supply and ground can be well suppressed. To prevent charge injection effect, the bottom plate sampling technique is used.

III. Proposed Techniques for 2b/cycle SAR ADCs

A. DAC Switching for 2b/cycle Conversion

In Fig. 2, the branch ratio of the DAC array is C_1: C_2: C_3: C_4: =64: 16: 4: 1. Basically, one of C_i (i=1, 2, 3, 4) is used for threshold pre-setting. To describe the operation of 2b/cycle DAC switching, one example with 4-bit DAC arrays is illustrated in Fig. 3. It shows the single-ended switching procedure of one conversion. The sampling phase is illustrated in Fig. 3. All the bottom plates of CDACs are connected to input during the sampling. Before the MSB comparison, the threshold of CDAC1 is set to $3/4V_{FS}$ (by connecting one 4C to 0 with others reset to 1), while the threshold of CDAC2 is set to $1/4V_{FS}$ (by connecting one 4C to 1 with others reset to 0). Briefly, the CDAC1 searches from "16" $LSB_{4\text{-bit}}$, while the CDAC2 searches from "0" $LSB_{4\text{-bit}}$. Both CDACs approximate the targeted input. With the different MSB comparison results "Co1Co3Co5", the connections of 4C are different. While the pre-settings of C are the same, which generate the thresholds for next comparison. For the LSB comparisons, where the last two bits are generated by interpolated comparators (Co2, Co3 and Co4), the voltage difference settled between CDAC1 and CDAC2 is one $LSB_{4\text{-bit}}$ ($1/16V_{FS}$). At the outputs of pre-amplifiers, the thresholds of interpolated dynamic

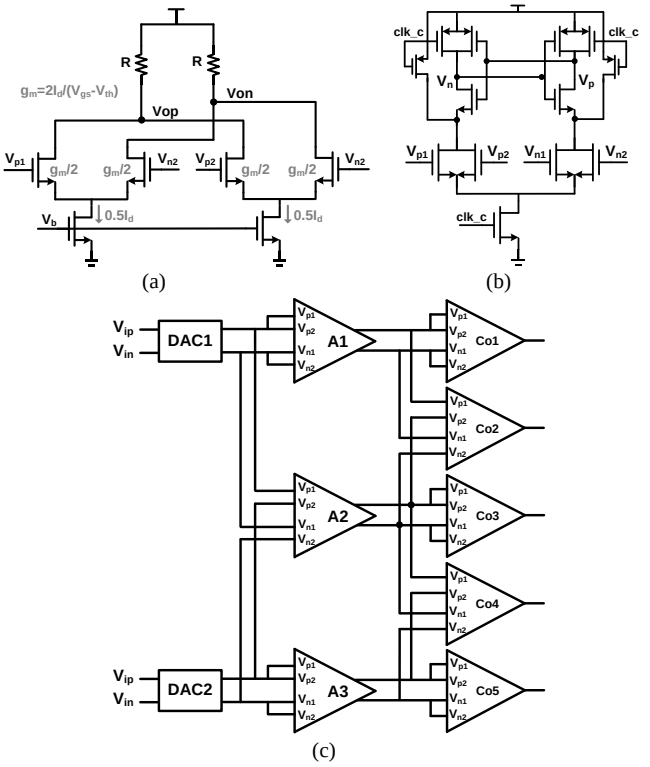

Fig. 4. Illustration of two-stage interpolation. (a) Schematic of pre-amplifier (b) Schematic of dynamic comparator. (c) Schematic of two-stage interpolation.

comparators Co2 and Co4 are $3/64V_{FS}$ and $1/64V_{FS}$ within one $LSB_{4\text{-bit}}$, respectively.

B. 2bit/cycle Architecture with Two-stage Interpolation

The commonly used interpolations are resistive [22] and capacitive [21]. However, the resistive interpolation will introduce crosstalk between pre-amplifier outputs. More switching connections will be present if capacitive interpolation is employed, which cause longer regeneration time thus not suitable for high speed operation. To avoid crosstalk and achieve short regeneration time, the interpolations are realized by split input differential pairs of pre-amplifiers and comparators. The cascades of comparators and SR latches are applied for Flash ADCs with resolution of 6~7 bits [25]-[27]. The first-stage interpolation is placed between two DAC arrays with pre-amplifier A2 as shown in Fig. 2, which reduces one DAC array compared with [10]. The schematic of interpolated pre-amplifier is shown in Fig. 4(a). The interpolated differential amplifier (A2) adopts the same bias current I_d as the non-interpolated amplifier A1 (A3). Therefore, the single-ended gain of A2 is $g_mR/2$. The output of A2 is

$$V_{op}-V_{on}=\frac{(V_{p1}-V_{n1})+(V_{p2}-V_{n2})}{2}\cdot g_mR. \tag{1}$$

After implementing the interpolation, the voltage gain of A1, A2 and A3 are the same, which is g_mR. Since the differential input full scale is 2.4V, the corresponding LSB is 2.34mV (0.68mV *rms*). The desired input referred noise of comparator V_{noise_comp} is less than 1mV *rms*. In this work, the gain of pre-amplifier is designed to satisfy

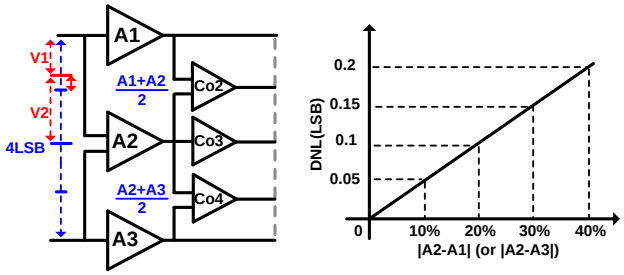

Fig. 5. Illustration of gain mismatch effect on DNL.

TABLE I
DAC COMPARISON WITH THE STATE-OF-THE-ART 2B/CYCLE SAR ADCS.

	Resolution (B)	No. of unit capacitor N_c (Single-ended)	No. of unit capacitors per conversion step (N_c/2^B)
[10]	6	192*	3
[13]	7	192	1.5
[14]	9	512	1
This work	10	512	0.5

*Equivalent number of unit capacitors without split capacitive structure.

$$V_{LSB,rms}\cdot g_mR \geq V_{noise\_comp,rms} \tag{2}$$

Therefore, the gain of pre-amplifier is set around 3.5dB (1.5). The time constant of output bandwidth of pre-amplifier is set around 10ps. Since the comparators Co1, Co3 and Co5 are independent with each other, the gain variation will not affect their decisions. For the interpolated comparators Co2 and Co4, the effect of gain variation is illustrated in Fig. 5. Assuming that the threshold between V1 and V2 is caused by mismatch between A1 and A2. Therefore, the following relation can be obtained, which is

$$\begin{cases} V1\cdot \mathrm{A1}=V2\cdot \mathrm{A2} \\ DNL=\dfrac{|V1-V2|}{V1+V2} \end{cases}. \tag{3}$$

Then, the relation between DNL and |A2-A1| (or |A3-A2|) can be represented as

$$DNL=\frac{|\mathrm{A2}-\mathrm{A1}|}{\mathrm{A2}+\mathrm{A1}}. \tag{4}$$

For instance, 10% gain mismatch will cause 0.05 LSB DNL penalty, which means the effect of gain mismatch is negligible. The second-stage interpolation is realized by dynamic comparator Co2 and Co4 (Fig. 2), the schematic of the interpolated dynamic comparator is shown in Fig. 4(b). Fig. 4(c) depicts the overall schematic of the proposed two-stage interpolation. All the pre-amplifiers and dynamic comparators are identical to achieve good matching. The pre-amplifier and dynamic comparator work in non-interpolated mode with positive inputs and negative inputs shared, respectively. In this work, the thresholds of first 8 bits are generated by the DAC arrays. The interpolated pre-amplifiers and comparators produce the thresholds of the least 2 bits. Table I lists the

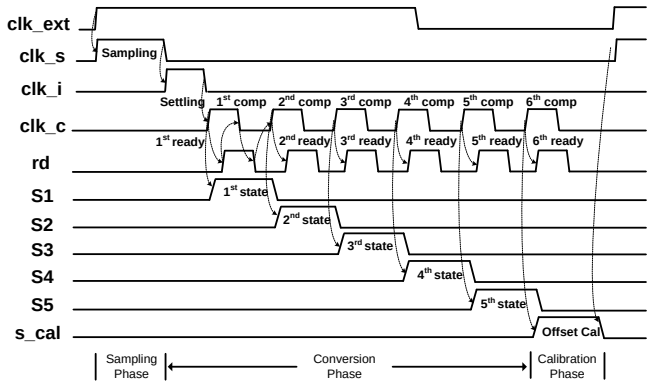

Fig. 6. Asynchronous timing diagram, including sampling phase, conversion phase and offset calibration phase.

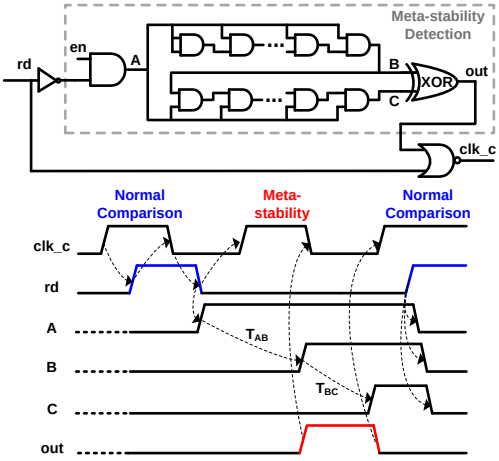

Fig. 7. Proposed meta-stability immunity technique.

comparison of DAC of 2b/cycle SAR ADCs. The number of unit capacitors per conversion step is only 0.5 in this work.

C. Meta-stability Immunity Technique for Asynchronous Conversions

The asynchronous processing makes the average conversion time shorter than that of synchronous processing, which is suitable for high speed applications. The asynchronous timing is depicted in Fig. 6, consisting of sampling phase, conversion phase and background offset calibration phase. With the presence of external clock signal *clk_ext*, the pulse duration of signal *clk_s* and *clk_i* are created by delay of inverter chain. The duration of *clk_s* defines the sampling phase. The falling edge of *clk_i* triggers the MSB comparison, and the comparators are activated from reset state (*clk_c*=0 to 1). After the completion of the comparison phase, the ready signal becomes 1 (*rd*=1) to indicate that the comparison results are ready. The state signals S_i (*i*=1, 2, 3, 4, 5), which gate the corresponding control logics for DAC array, are generated from shift register.

The well-known meta-stability effect [18] brings a risk for asynchronous operation. If the meta-stability happens, the whole conversion phase may be interrupted and an unexpected code may be produced, significantly degrading the bit error rate (BER). A meta-stability cancellation technique was presented

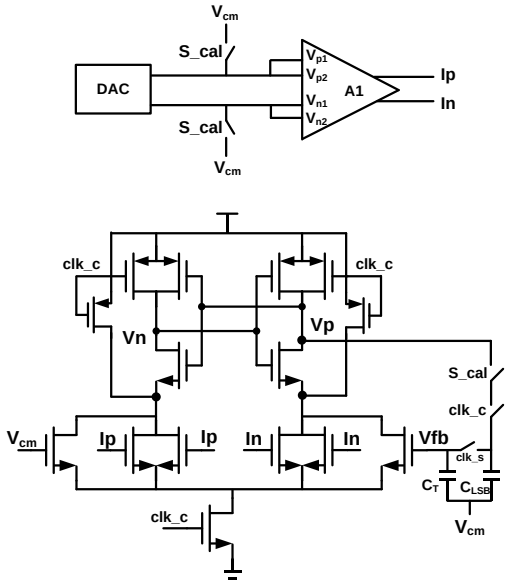

Fig. 8. Schematic of interpolated comparator.

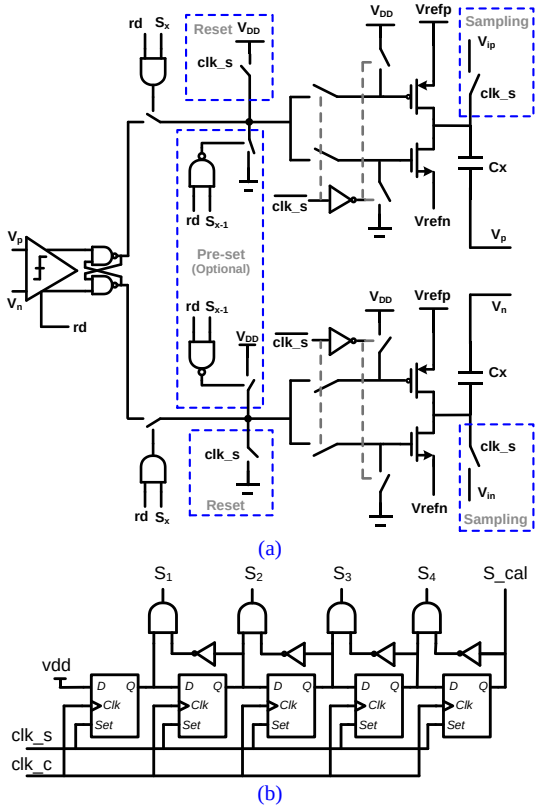

Fig. 9. (a) Schematic of control logic for DAC array. (b) Schematic of shifter register.

in [28] with different asynchronous feedback loop. The ready signal has no control on the time out signal, which may result in the triggered time out signal in each cycle. In this work, the meta-stability immunity technique is illustrated in Fig. 7. *en* is the enable signal. Normally, the signal *rd* will be triggered to be high after comparison starts (*clk_c*=1). While the meta-stability detection block is in reset phase when *rd*=1. The meta-stability detection is activated with *A* rising to be 1. Once signal *rd* keeps 0 beyond certain period (T_{AB} in Fig. 7), meta-stability occurs as

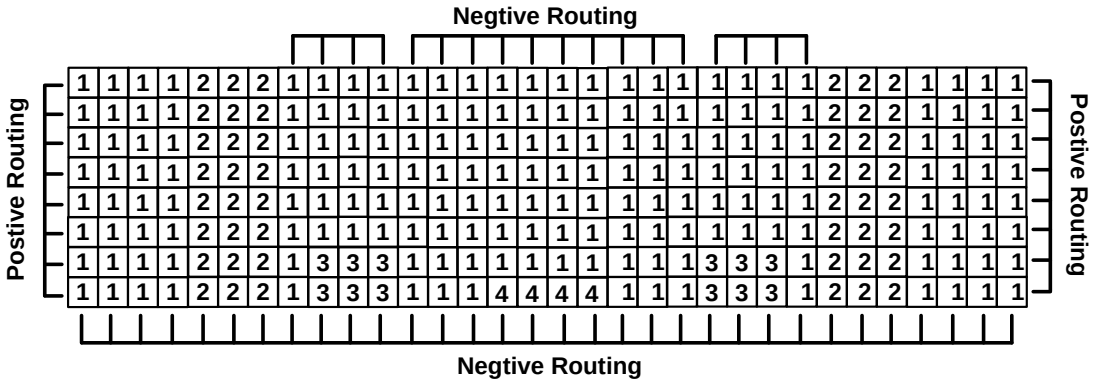

Fig. 10. Floor plan of the DAC capacitor array.

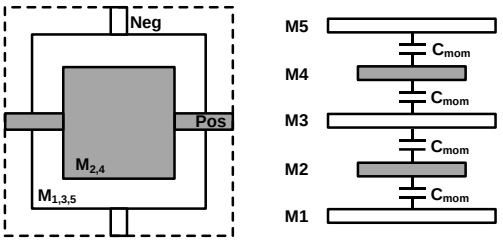

Fig. 11. Top (left) and cross-section (right) views of the unit capacitor.

TABLE II
EXTRACTED CAPACITANCE OF EACH BRANCH.

	Ratio	Total (fF)	Normalized value
C1	64	75.778	63.74
C2	16	18.934	15.92
C3	4	4.745	3.99
C4	1	1.189	1

shown in Fig. 7. The delay of T_{AB} equals the tolerable longest regeneration time of comparison. After a delay of T_{AB}, the *B* also becomes 1 to generate a high *out* through a XOR gate. Since both *out* and *rd* are the inputs of the NOR gate to trigger *clk_c*, the signal *out* plays the triggering role of *rd* when *rd* is absent. After one more delay of T_{BC} for comparator resetting, the *C* is triggered to be high to reset *out*, therefore, *clk_c* is activated for next comparison. All the signals in meta-stability detection block will be in reset phase when *rd* becomes high. Once the meta-stability occurs, a wrong bit could be generated due to interruption feature of the proposed meta-stability immunity technique. Fortunately, since the differential input of pre-amplifier should be much small, the caused error for DNL E_{DNL} is much smaller than one LSB. Therefore, the small error is negligible.

IV. CIRCUITS DESIGN

A. Comparators

The schematic of dynamic comparator with offset calibration is shown in Fig. 8. When *clk_c* is low, the

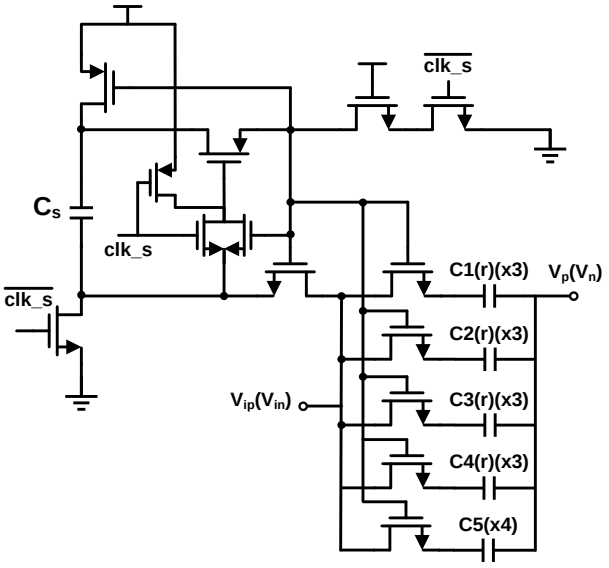

Fig. 12. Schematic of bootstrapped switches.

comparator is in reset phase. Comparator is in conversion phase when *clk_c* is high. The pre-amplifier is placed prior to comparator to suppress the kick back noise. The background offset calibration is realized by placing an auxiliary differential pair with the gate voltage of one fixed and other one adjusted by negative feedback loop. To decouple the switching noise on the *Vcm*, the bottom plate of C_T is connected to *Vcm*. Additionally, a latch follows the *Vop* and *Von* to store the results of comparison. After the last comparison, the residues at differential input of pre-amplifiers are less than 1 $LSB_{8\text{-bit}}$. It is easier to conduct the background offset calibration, for which shorting the differential inputs are required. Therefore, the calibration phase is placed following the last comparison. After the LSB conversion, the calibration control signal *S_cal* equals 1. C_{LSB} is employed to store the comparison result. During the next sampling phase, the C_T and C_{LSB} share the charges with *clk_s*=1. The size of C_T is determined by the required calibration resolution. The changing of voltage on C_T for each charge and discharge V_{step} is

$$V_{step} = \frac{\Delta Q}{C_T} = \frac{C_{LSB} \cdot V_{DD} / 2}{C_T}. \quad (5)$$

To make the resolution of calibration sufficient accurate, the following condition should be satisfied.

$$\frac{V_{\text{step}}}{g_m R} \le \frac{1}{2} LSB_{\text{10-bit}}, \tag{6}$$

where $g_m R$ is the gain of pre-amplifier. Therefore, the C_T should satisfy

$$C_T \ge \frac{V_{DD}}{g_m R \cdot LSB_{\text{10-bit}}} C_{\text{LSB}}. \tag{7}$$

B. Control Logics

Unlike the traditional SAR logic [19], the proposed control logic is designed as dynamic to eliminate the delay of DFF and the equivalent delay is equal to propagation delay of just two inverters. The schematic of DAC control logic is shown in Fig. 9(a). During the sampling phase with *clk_s*=0, the bottom plate of DAC array is disconnected from the control logic and connected to the input signal, while the outputs of control logic are reset. The output of comparator is driven by a latch. During conversion phase, the C_x (x=1, 2, 3, 4) will be settled in state S_x (x=1, 2, 3, 4) with a ready signal *rd* from comparator. For the pre-settled branches, the C_x could be pre-settled in state S_{x-1}. The schematic of the shifter register is shown in Fig. 9(b), which generates the state signals S_x (x=1, 2, 3, 4).

C. DAC array

Fig. 10 shows the floor plan of capacitor DAC array. The positive (top plate) of all unit capacitors are connected horizontally and the negative (bottom plate) are connected vertically. Unlike the previous placement of unit capacitors [19], in which the extra wiring is necessary in between the DAC array, the DAC in this work introduces no wiring caused parasitic capacitance. According to [6], the variation of unit capacitor should satisfy

$$3\sigma_{DNL} < \frac{1}{2} LSB_{10b} = \frac{1}{8} LSB_{8b} \tag{8}$$

The nominal value and standard deviation of 8-bit unit capacitor are C_u and σ_u, respectively. The switching of branch C_1 is considered as the worst case. For differential implementation, total $254C_u$ (2· (64+63)) unit capacitors are switched with the LSB of $2C_u$. Therefore, by considering with (8) the σ_{DNL} becomes

$$\sigma_{DNL} = \frac{\sqrt{254}\,\sigma_u}{2C_u} < \frac{1}{24} LSB_{8b} \tag{9}$$

Hence,

$$\frac{\sigma_u}{C_u} < 0.5\% \tag{10}$$

The required process variation of unit capacitor needs to be less than 0.5%. The mismatch of capacitor could be described as

$$\frac{\sigma_u}{C_u} = \frac{A}{\sqrt{W \cdot L}}, \tag{11}$$

where A is the mismatch coefficient. W and L are the width and length of unit capacitor, respectively. The simulated parameter A in 40nm CMOS technology is 0.56% [μm]. The W and L of unit capacitor are both set to 1.2μm, resulting in a capacitance of 1.2fF. The customized unit capacitor is composed of 5 layers metal (M1, M3, M5 for negative and M2, M4 for positive) as shown in Fig. 11. The extracted capacitance of each branch is listed in Table II.

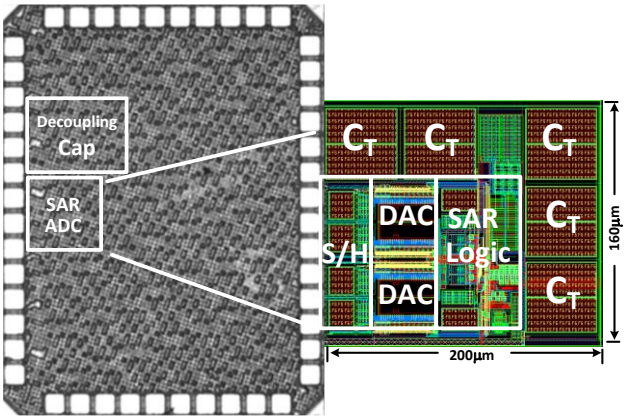

Fig. 13. Die photo and layout of the proposed SAR ADC.

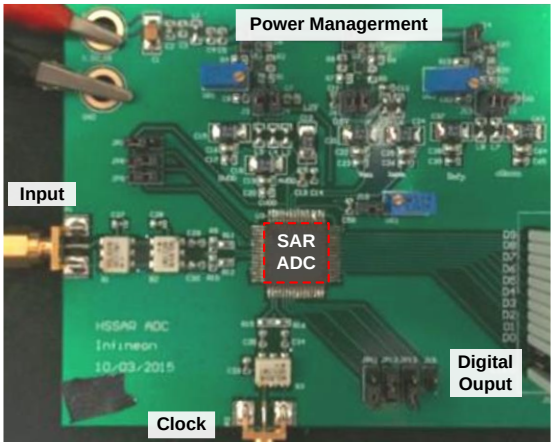

Fig. 14. Testing board of the proposed SAR ADC.

D. Sample and Hold

Fig. 12 shows the schematic of bootstrapped switch. The bootstrapped switch has multiple outputs. The bottom plate sampling is applied in this work. One potential issue is that the bandwidth mismatch may degrade the linearity of sampled signal. However, by benefiting from advanced CMOS process with large transition frequency f_T (exceeding 200GHz) and matching layout, the sampling time constant can be easily set as 20ps. Therefore, the bandwidth mismatch is negligible. The differential input range $V_{p\text{-}p}$ is around $2V_{dd}$ with a common voltage of $V_{dd}/2$.

V. Measurement Results

The ADC chip is fabricated in 40nm CMOS Low-Power technology. The die photo and layout are shown in Fig. 13, and ADC core occupied 160μm x 200μm. The testing board is shown in Fig. 14. The performance is measured at 1.2V power supply and normal temperature. To supply a clean reference voltage, one solution is putting a large decoupling capacitor between the positive and negative reference voltage, which can decouple the large transient voltage drop and ringing caused by

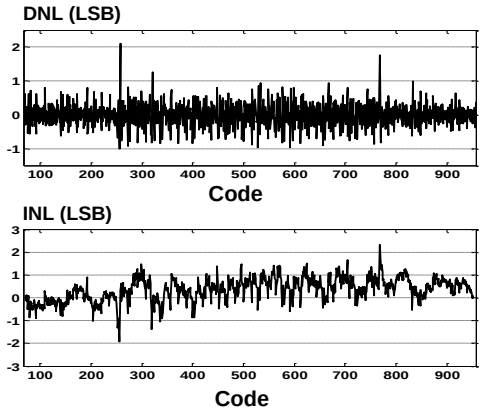

Fig. 15. Measured DNL and INL results.

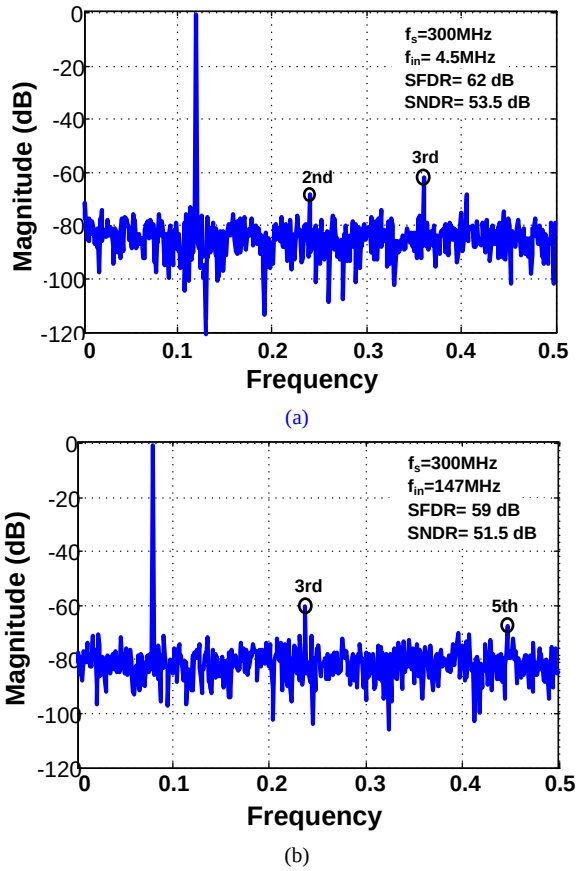

Fig. 16. Measured SFDR and SNDR (digital output is decimated by 8) with (a) f_{in}=4.5MHz and (b) f_{in}=147MHz.

bonding wire during switching. In this work, the value of decoupling capacitance is 300pF, occupying an area of 250μm x 200μm. The differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 15. The measured peak DNL and INL of binary approximation are -1.0/2.1 and -1.9/2.3 respectively. The peak values of DNL are located at code 1011111111 (767) and 0100000000 (256). It could be concluded that the settling time allocated for MSB comparison is not sufficient.

The sampled output is decimated by a factor of 8. With a 300MHz sampling frequency, Fig. 16 (a) shows the measured SFDR and SNDR at 4.5MHz input are 62dB and 53.5dB,

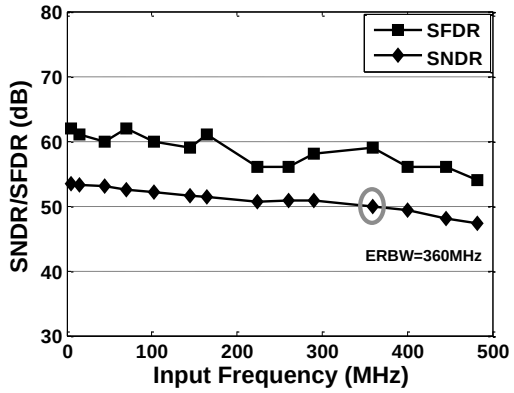

Fig. 17. SFDR and SNDR versus input frequency at f_s=300MHz and V_{dd}=1.2V.

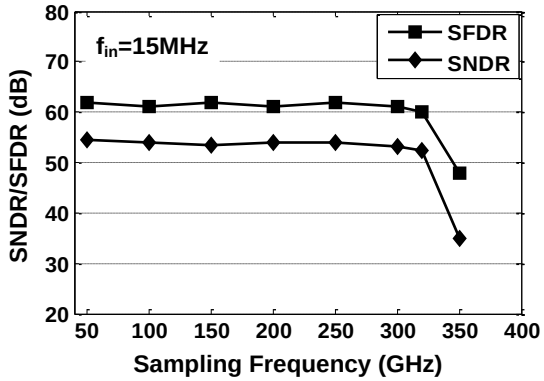

Fig. 18. SFDR and SNDR versus sampling frequency at f_{in}=15MHz and V_{dd}=1.2V.

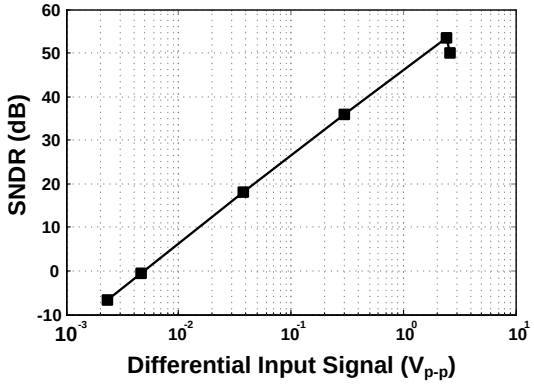

Fig. 19. SNDR versus input signal magnitude at f_{in}=15MHz, f_s=300MHz and V_{dd}=1.2V.

respectively. The measured SFDR and SNDR at 147MHz are 59dB and 51.5dB respectively as shown in Fig. 16 (b). The corresponding effective number of bit (ENOB) is 8.3 bits at Nyquist input. The calculated jitter performance is around 1.53ps rms. The SFDR and SNDR versus input frequency is shown in Fig. 17, where the effective resolution bandwidth (ERBW) is up to 360MHz. Fig. 18 illustrates the measured SFDR and SNDR versus sampling frequency at 15MHz input. The SNDR versus input signal magnitude is shown in Fig. 19. When the differential input peak-to-peak voltage (V_{p-p}) is 2.4V, the maximum SNDR of 53.5dB is achieved. The power

TABLE III
PERFORMANCE SUMMARY

Technology		**40nm LP CMOS**
Supply Voltage (V)		**1.2**
Input Common Mode (V_{cm})		**0.6**
Differential Input Range (V_{p-p})		**2.4**
Input Capacitive Load (pF)		**0.6**
Sampling Rate (MS/s)		**300**
Active Area (mm^2)		**0.082**
DNL		**-1.0/2.1**
INL		**-1.9/2.3**
SFDR(dB) @Nyquist-freq		**59**
SNDR(dB) @Nyquist-freq		**51.5**
ENOB @Nyquist-freq		**8.3**
Power	**Preamp+Comparator**	**2.5mW**
	DAC array	**0.3mW**
	Digital logic	**3.0mW**
	Total	**5.8mW**
Figure of Merit (fJ/conv-step)		**61**

TABLE IV
COMPARISON OF 2B/CYCLE SAR ADCS AND 300MS/S 10-BIT PIPELINE ADCS

	[13]	[24]	[16]	[17]	This Work
Amplifier Architecture	2b/cyc. SAR	2b/cyc. SAR	Pipeline	Pipeline	2b/cycle SAR
No. of Channel	1	1	1	1	1
Technology (nm)	45	40	90	65	40
Supply voltage (V)	1.1	1.2	-	1	1.2
Power (mW)	7.2	2.1	40	26.6	5.8
Sampling Rate (MS/s)	800	300	320	300	300
Resolution	7	10	10	10	10
SNDR(dB) **@Nyquist**	39.4	47	51.2	52.9	51.5
FOM @Nyquist (fJ/conv-step)	73	38.4	396	245	61
Area (mm^2)	0.016	0.008	0.46	0.36	0.082

consumption of the ADC core is 5.8mW (pre-amplifier 2.5mW, digital logic 3.0mW, DAC array 0.3mW). Since the size of unit capacitor utilized in this work is only 1.2fF, the power contribution of DAC array is only 5%. The performance summary is listed in Table III. The ADC shows a better power efficiency than 300MS/s 10-bit pipelined ADCs. Compared to another 2b/cycle 300MS/s SAR ADC [24], this work has a better ENOB. The proposed ADC achieves a FoM value of 61fJ/conversion-step and a core size of $0.082mm^2$. The performance comparison with the state-of-the-art 2b/cycle SAR ADCs and pipeline ADCs with sampling rates up to 300MS/s is listed in Table IV.

VI. CONCLUSION

A test chip of a single channel 10-bit 2b/cycle SAR ADC with sampling rate of 300MS/s, which extends the speed limitation of single-channel SAR ADC, is proposed. The proposed two-stage interpolation based 2b/cycle architecture relaxes the resolution of capacitive DAC array and reduces the trade-off between input bandwidth and resolution. Moreover, the proposed meta-stability immunity technique enhances the asynchronous processing for high-speed SAR ADCs.

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