Investigation and design of low power circuit blocks for medical implant SOCs

Arjun, Ramaswami Palaniappan

2020

Arjun, R. P. (2020). Investigation and design of low power circuit blocks for medical implant SOCs. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/137142>

<https://doi.org/10.32657/10356/137142>

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**INVESTIGATION AND DESIGN
OF
LOW POWER CIRCUIT BLOCKS FOR MEDICAL IMPLANT SOCs**

**RAMASWAMI PALANIAPPAN ARJUN
SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING
2020**

**Investigation and Design
of
Low Power Circuit Blocks for Medical Implant SOCs**

Ramaswami Palaniappan Arjun

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

03 Aug 2019

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

03 Aug 2019

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Assoc Prof Liter Siek

Authorship Attribution Statement

This thesis contains material from 5 papers submitted to or published in the following peer-reviewed journals or conferences in which I am listed as an author and 1 PhD thesis submitted by one of my co-author to School of Electrical and Electronic Engineering, Nanyang Technological University.

Chapter 3 is published as Arjun Ramaswami Palaniappan and Liter Siek, “Wide-input dynamic range 1 MHz clock ultra-low supply flip-flop,” *Electronics Letters*, vol. 54, no. 15, pp. 938–939, Jun. 2018.

The contributions of the co-authors are as follows:

- Assoc Prof Siek provided the initial project direction, guidance during the project implementation and reviewed the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and analyzed the proposed sense-amplifier flip-flop.
- I also simulated the design and analyzed the collected results.

Chapter 4 is published as Arjun Ramaswami Palaniappan and Liter Siek, “A 0.6 V, 1.74 ps Resolution Capacitively Boosted Time-to-Digital Converter in 180 nm CMOS,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019

The contributions of the co-authors are as follows:

- Assoc Prof Siek provided the initial project direction, guidance during the project implementation and reviewed the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and analyzed the proposed time-to-digital converter (TDC) architecture. I also designed a PCB for measuring the performance of this TDC test chip.
- I will be measuring the fabricated TDC test chip and will be analyzing the collected results.

Chapter 5 is published as Arjun Ramaswami Palaniappan and Liter Siek, “A TDC-less All-Digital Phase Locked Loop for Medical Implant Applications,” *Elsevier Microprocessors and Microsystems*, vol. 69, pp. 168–178, 2019 and published as Arjun Ramaswami Palaniappan and Liter Siek, “A 0.0186 mm², 0.65 V Supply, 9.53 ps RMS Jitter All-Digital PLL for Medical Implants,” in *IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, 2018.

The contributions of the co-authors are as follows:

- Assoc Prof Siek provided the initial project direction, guidance during the project implementation and reviewed the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and analyzed the proposed all-digital phase locked loop (ADPLL) architecture. I also designed a PCB for measuring the performance of this ADPLL test chip.
- I measured the fabricated ADPLL test chip and analyzed the collected results.

Chapter 6 is submitted as Section 3.2 of Chapter 3, Jian Sen Teh, “Design of a Time-Mode Analog-to-Digital Converter Utilizing a Time-to-Digital Converter That Is Scalable with CMOS Technology,” PhD Thesis, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, 2019 and submitted as Jian Sen Teh, Arjun Ramaswami Palaniappan, and Liter Siek, “Analysis of Negative Skewed Delay Scheme for Ring Oscillator With Multi-Phase Outputs,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2019.

The contributions of the co-authors are as follows:

- Assoc Prof Siek provided the initial project direction, guidance during the project implementation and reviewed the manuscript drafts.
- Mr. J.S. Teh analyzed the negative skewed ring oscillator and designed a test chip for validating this analysis.
- I assisted in simulation of SE NSRO in 180 nm CMOS.

- Mr. J.S. Teh prepared the manuscript drafts and I assisted in revising the manuscripts.
- Mr. J.S. Teh measured the test chips and analyzed the collected results.
- I also measured the test chips, assisted in phase noise analysis, collected output frequency, phase noise and jitter data from the test chips and analyzed the results.

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Acknowledgements

First of all, I would like to express my heartfelt thanks and gratitude to my supervisor, Assoc Prof. Siek Liter for his guidance, supervision, encouragement and advice both before and during this PhD journey. His fresh and inspiring ideas even at the most difficult times propelled me to successfully complete this PhD journey. I have strongly admired his approaches to solve difficult problems, friendliness and care towards students, easy approachability even during his busiest times, cheerfulness and passion towards the work. Without his encouragement, guidance and inspiring words, this PhD thesis would have not been possible. I will always be indebted to him for his support and guidance.

Next, I would like to thank EDB, Singapore and NXP Semiconductors, Singapore for funding my PhD studies. I would also like to thank Mediatek, Singapore and NTU-A*STAR Silicon Technologies Centre of Excellence for sponsoring the test chip fabrication in 40 nm and 180 nm CMOS technologies. I would like to thank my colleagues and seniors in VIRTUS for their knowledge sharing and support whenever needed. In addition, I would also like to thank all the lab staffs of VIRTUS IC Design Centre for providing the technical supports as and when needed.

Ultimately, I would like to thank all my family members for their constant motivational support, encouragement, financial support and understanding throughout this PhD journey.

Abstract

Biomedical implant devices are growing in recent years due to advancements in microelectronics, increase in chronic diseases and rising aging population. Since biomedical implants have stringent constraints on area and power consumption, majority of its electronic circuitry is realized using application specific system-on-chips (SoC). These SoCs contain various sub-blocks, intellectual property cores and standard cells in it for providing the intended functionality of the medical implant under consideration. In order to reduce the overall power and area consumption of the medical implant SoC, novel circuit architectures without compromise on performance for all individual SoC sub-blocks is necessary. This PhD research investigates 4 of the important sub-blocks of the medical implant SoC and proposes novel circuit architectures for these sub-blocks towards achieving a low power medical implant SoC without compromise on individual sub-block performance.

Firstly, a novel ultra-low supply voltage and wide-input dynamic range flip-flop (FF) standard cell capable of operating at 0.16 V is designed in CMOS 40 nm. When compared with other FF topologies, the proposed capacitively boosted sense-amplifier FF topology achieves the least clock-to-output propagation delay and power-delay product. The proposed FF is also the only one capable of sampling low swing data signals from 0.2 V to 1 V. Thus, the proposed FF standard cell can be used to build the processor and logic unit of the implant SoC for achieving a better performance at ultra-low supply voltages.

Secondly, a low power, low supply voltage and high time resolution time-to-digital converter (TDC) is designed and fabricated in 180 nm CMOS. While most of the current TDC architectures are designed to operate at a supply voltage of 1 V and above, the proposed TDC architecture utilizes capacitive boosting differential buffers for enabling the TDC to operate at a supply of 0.6 V even when using standard 1.8 V transistors in the design. The proposed TDC achieves a resolution of 1.74 ps and is suitable for use in the biosensor unit of implant SoC for time-of-flight measurements.

Thirdly, a TDC-less low area all-digital phase locked loop (ADPLL) is designed and fabricated in 40 nm CMOS. Various circuit design techniques such as fractional capacitor tuning, capacitive boosting ring oscillator and frequency control mechanism is incorporated in the design to reduce silicon area and power consumption. The ADPLL operates at 0.68 V, covers the MedRadio frequency band, occupies a silicon area of 0.0186 mm² and exhibits an rms jitter of 11.88 ps. The ADPLL is suitable for use in the transceiver unit of the implant SoC.

Finally, negative skewed ring oscillators (NSRO) are analyzed and a sequence tree based time-domain approach that is able to determine the optimum oscillation behavior of an NSRO is proposed and validated using test chips fabricated in 180 nm CMOS. The scheme is also extended to differential ring oscillators. Such NSROs can be used in various applications inside the implant SoC, such as to design the TDC (ring oscillator based TDCs), VCO of PLL and pulse generators.

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List of Abbreviations

PMU	Power management unit
ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
DSP	Digital signal processor
AS-SoC	Application specific system on chip
SoC	System on chip
FF	Flip-flop
PLL	Phase locked loop
VCO	Voltage controlled oscillator
APLL	Analog PLL
ADPLL	All-digital phase locked loop
SAFF	Sense amplifier flip-flop
TDC	Time-to-digital converter
HLFF	Hybrid latch flip-flop
SDFF	Semi dynamic flip-flop
CB-SAFF	Capacitively boosted sense-amplifier flip-flop
INL	Integral non-linearity
DNL	Differential non-linearity
FOM	Figure of merit
GRO	Gated ring oscillator
FCW	Frequency command word
DCO	Digitally controlled oscillator
DLPF	Digital loop filter

MICS	Medical implant communication service
PFD	Phase frequency detector
MedRadio	Medical device radio communication service
CB-VDL	Capacitively boosted vernier delay line
RO	Ring oscillator
SE	Single-ended
NSRO	Negative skewed ring oscillator
SCL	Source-coupled logic
SD	Saturated delay
TRx	Transceiver
IP	Intellectual property
PDP	Power-delay product
OTW	Oscillator tuning word
SDM	Sigma delta modulator
MOM	Metal oxide metal

Chapter 1

Introduction

1.1 Overview

Technological innovations in microelectronics and materials science has propelled the growth of biomedical implant devices in the current years [1]. An increasing incidence of chronic illnesses and growing older population are few of the key reasons accelerating the growth of the market for biomedical implants. As older people are more vulnerable to chronic disorders and illnesses relevant to orthopedics, cardiovascular, dental and endovascular systems, medical implants are commonly used in solving various diseases, such as heart disease, epilepsy, repair of fractures, hearing and vision problems etc... In latest years, the global annual market for medical devices has surpassed \$200 billion.

Biomedical implant is a device which is partly or completely inserted in the human body to monitor, control and manipulate the functions of the human body [2]. Usually these devices are implanted into the body through various ways depending on the type of implant. Some of the common ways for implanting medical devices are performing an open surgery, swallowing pill type implants, injecting the device through injections etc... After implanting the medical device, it stays at the placement site to either substitute a faulty body part, assist the body part to function properly or augment the body part to function efficiently.

There are two types of medical implant devices: passive and active. Passive medical implants do not require an energy source to function. Some examples of passive implants are artificial valves, artificial leg, artificial knees, vascular grafts etc... On the other hand, active medical implants do more than what a passive implant can do and hence it requires a power source for functioning. There are numerous type of active biomedical implant devices ranging from neural implants [3], cochlear implants [4], retinal implants [5], pacemakers [6] [7], drug delivery implants [8], diabetic insulin pumps [9] etc... with each focused on a specific application to treat specific disease conditions in the human body, thereby enhancing the patient's quality of life. Some of other emerging active medical implant devices are shown in Figure 1.1.

Figure 1.1 – Various active biomedical implant devices [10]

1.2 System Description

While there are different kinds of biomedical implants for different application, each medical implant device comprises mainly of the electronic unit and battery. Given the implant device's size limitations, most of the electronics circuit in the implant is accommodated by a system on chip (SoC) which is application specific as depicted in Figure 1.2. The implant device's electronics system has one or several of the below mentioned functionalities [2], (1) observing and measuring the body's essential physiological signals (2) replacing the body part or organ which is defective or malfunctioning (3) supplying the medicines needed exactly when necessary (4) stimulating the body organ when it does not work correctly (5) transmits diagnostic data and receives external commands.

Figure 1.2 – Biomedical implant system on chip

The system on chip (SoC) unit of the implant has various sub systems and intellectual property (IP) cells in it like the power management unit (PMU), transceiver (TRx), phase locked loop (PLL), digital signal processor (DSP), data converters, logic circuits, analog front-end, bio sensors, stimulators and pulse generators, with each one performing a specific task.

The power management unit of the implant device consists of energy harvesting circuits and voltage regulators to provide a stable supply to the implant device [11][12]. Since, different sub systems of the implant SoC operates at different supply voltages for reducing power consumption, the PMU unit contains level shifters and voltage regulators for providing different supply voltages. Biosensors are used to sense various vital signals from the human body and they are processed with an analog front-end which has amplifiers and filters. The signals are then digitized using an analog-to-digital converter (ADC) which are then processed by a digital signal processor (DSP) unit. The DSP unit consists of logic and memory blocks to perform complex algorithms in the signal to check whether the body organ is functioning as intended or not. Based on the results, the DSP unit issues signals to the digital-to-analog converter (DAC) which drives the stimulator unit to stimulate the body organ to function properly. These results are also transmitted to the outside world using a transceiver system for continuous monitoring and diagnostic purposes.

It can be observed that one of the vital component of the biomedical implant system is the communication system or transceiver. Many standard implants have short-range magnetic communications that require a close connection between the implanted inside and outside units [13][14]. These magnetic based communication link systems are easily affected by electromagnetic interference, have danger of patient safety and are inaccurate in transmission due to the overwhelming amount of electric-power radiating devices worldwide, such as wireless routers and cellular phones [15][16].

Thus, the FCC has allotted a 401 MHz – 457 MHz frequency band called as medical device radio communications service (MedRadio), for the application of medical implants and medical transceivers in order to overcome the above mentioned constraints and security concerns [17] [18].

1.3 Design Challenges for Medical Implants

Even though there are various low power systems available today like the internet of things (IoT), medical implants require specialized architectures to achieve low power consumption without compromising the performance metrics. As technology progresses, medical implants demand both speed and low power consumption all while operating at a low supply voltage. This is primarily because, the number of implant applications is increasing globally which leads to emerging markets and business opportunities. Today, implants are not only used to just treat disease conditions, but it is also used to monitor the patient's health round the clock and transmit patient data to cloud which enables the doctors to be informed of their patient's health. This is evident from the Carelink Smartsync Device Manager software platform that Medtronic recently introduced [19]. Thus, today's and future medical implants need high performance systems while consuming low power and this imposes multiple challenges in designing medical implants when compared with other low power systems like IoT systems.

Even though there are various specifications available for different sub-blocks of a medical implant, power consumption is one of the critical specification of any medical implant device. Unlike IoT systems, it is practically impossible to

replace the batteries of medical implants once the device is implanted inside the body, unless another surgery is done to replace the batteries. Considering a battery capacity of 2.5 Ah that is typically present in medical implants, the overall electronics needs to consume a power of less than 50 μ W in order for the device to last for 5-6 years (if the device is turned on continuously for 5-6 years). In order to mitigate this, all medical implant devices operate with a sleep-wake pattern where they sleep for most of the time and wake-up if need arises. When the medical implant wakes up and if all the sub-blocks of the implant is turned on, the overall implant consumes a power of 50-100 mW [20]. This means if the implant is continuously turned on, the battery would be discharged in less than 50 hrs when the current consumption is 50 mA. Most of the existing low power, high performance circuit sub-blocks are optimized for IoT applications and they work at a range of 1-2 mW. But medical implants require μ W sub-systems in order to maximize battery life. This explains the need for low power architectures for every single sub-block of the implant to increase battery life so that surgeries to replace batteries can be avoided.

1.4 Motivation

With the emergence of increased clinical needs for various biomedical implant applications for treating various disease conditions, multiple challenges in metrics such as power consumption, area, size, weight and performance of the implant device needs to be addressed. Since the SoC is one the most vital block of any implant device and moreover it is not convenient to have discrete components or replace batteries of the implant once it is inside the human body, ultra-low power consumption and good performance of the SoC is essential to

increase the life time of the implanted devices. Since the SoC itself is divided into numerous subsystems and IP blocks, low power / low supply voltage design and good performance of all the subsystems and IP blocks is essential to develop an ultra-low power SoC that is highly suitable for biomedical implants applications [21].

This PhD thesis investigates and focuses on 4 of such important circuit blocks namely the flip-flop (FF), time-to-digital converter (TDC), all-digital phase locked loop (ADPLL) and ring oscillator. These four blocks are chosen because they find multiple applications inside the medical implant SoC as shown in Figure 1.3. Hence, designing novel architectures for these four circuit blocks would aid in achieving a good performance SoC at a low V_{DD} and low power consumption.

Figure 1.3 – Medical implant SoC and important circuit blocks

One of the power hungry and time critical block of the implant SoC is the processor and logic unit which comprises of thousands to ten thousands of flip-flops as standard cells [22]. FFs are also used in data converters. Hence the FF block is one of the important circuits in the SoC. Time-to-digital converters are

widely used for time of flight measurement in biosensors of the implant SoC [23] and are also used in data converters. Phase locked loops are the heart of transceiver and occupy a major portion of the transceiver both in terms of power and area consumption [18] [24]. PLLs are used for frequency synthesis and clock generation in the implant SoC. Ring oscillators are widely used as voltage controlled oscillators (VCO) of the PLL and pulse generators in the implant SoC due to its lower area consumption compared with LC oscillators [25]. Since the overall medical implant device itself operates at a lower V_{DD} and needs to consume lower power, special architectures for these circuit blocks are essential in order to design a low power implant SoC without compromise on performance metrics. The important performance metrics of these four circuit blocks are a) FF – power-delay product and propagation delay (clock-to-output, C-Q) b) TDC – time resolution c) PLL – jitter and phase noise d) ring oscillator – frequency.

1.5 Research Objectives

This PhD research work investigates four of the above-mentioned important circuit blocks of the medical implant SoC and proposes novel circuit architectures for these blocks for achieving a low supply voltage and low power medical implant SoC without compromising the performance metrics. The four circuit blocks are flip-flop standard cell, time-to-digital converter, ring oscillator and phase locked loop. The primary research objectives are listed below,

- 1) To design an ultra-low supply voltage and power-delay product (PDP) efficient flip-flop standard cell capable of sampling low swing data signals for the processor and logic unit of the implant SoC.

- 2) To design a low supply voltage, low power and high resolution time-to-digital converter (TDC) for biosensors of implant SoC which is required to perform time-of-flight measurements.
- 3) To design an all-digital phase locked loop (ADPLL) which can operate at low power, low silicon chip area and low supply voltage for the transceiver unit of implant SoC.
- 4) To analyze and design single ended and differential negative skewed ring oscillators (NSRO) for VCOs and pulse generators of the implant SoC. To propose a time-domain analysis featuring sequence tree for the negative skewed delay scheme that will efficiently determine the optimum configuration and optimum oscillation behavior of a NSRO.

1.6 Research Contributions

The research contributions from this PhD thesis are listed below,

- 1) Investigation of various flip-flop architectures and design of flip-flop that is capable of operating at a clock frequency of 1 MHz at a very low V_{DD} of 0.16 V. The proposed FF cell achieves the lowest propagation delay (clock-to-output, C-Q) and a balanced power-delay product (PDP) when compared with other state-of-the-art flip-flop designs. The flip-flop is designed in 40 nm CMOS technology, has a wide-input dynamic range and is able to sample data signals having low voltage swing that can go down till 0.2 V, all while operating at an very low V_{DD} of 0.16 V [26].

- 2) Investigation of various time-to-digital converter architectures and design of capacitively boosted vernier time-to-digital converter that can operate at a low V_{DD} of 0.6 V even when the TDC system is designed using 1.8 V transistors (standard threshold) available in 180 nm channel length CMOS process. The proposed 6-bit TDC achieves a time resolution of 1.74 ps and has a power consumption of 217 μ W while operating at 0.6 V supply. Even though the proposed TDC prototype is fabricated in 180 nm CMOS for low cost, the proposed technique can be extended to design TDCs in shorter CMOS nodes thereby having the potential to reduce both power and area consumption further [27].
- 3) Investigation of various ADPLL architectures and design of 0.68 V supply, 0.0186 mm² silicon area and 11.88 ps rms jitter all-digital phase locked loop that covers the MedRadio frequency band. For achieving very less silicon area consumption and easy portability that are very much desired for biomedical implant devices, the usage of TDCs and LC oscillators are avoided in the proposed ADPLL. Thus, a TDC-less ADPLL design architecture which covers the MedRadio frequency band, incorporates techniques such as fractional capacitor tuning, frequency controller mechanism, shunt capacitor tuning and differential ring oscillator system using capacitively boosted buffer cells is designed in 40 nm CMOS for achieving good jitter performance capabilities, low power and ultra-low area consumption [28] [29].

- 4) Design and analysis of single ended and differential negative skewed ring oscillators. A ring oscillator employing the negative skewed delay scheme can increase its oscillation frequency by up to 2 or 3 times, making it a suitable architecture for multi-phase outputs generation. However, the original analysis of this scheme does not adequately explain the frequency increment. Thus, an alternative time-domain analysis featuring a sequence tree graph is proposed and validated which shows that the frequency increment is due to the presence of multiple oscillating edges. It also describes the phase sequence of the resulting oscillation. The impact of this scheme to phase noise is also briefly investigated. The proposed analysis is validated with simulation and measurement results from test chip fabricated in 180 nm CMOS [30].

1.7 Thesis Organization

This PhD thesis consists of seven chapters and their brief outline is given below.

Chapter 2 – An extensive literature survey and investigation on flip-flops, sense-amplifier flip-flops, time-to-digital converter architectures, ring oscillator architectures and all-digital phase locked loop architectures is presented.

Chapter 3 – Presents the proposed sense-amplifier flip-flop topology that can operate at a very low supply voltage and can sample wide-input data signals.

Chapter 4 – Presents the proposed capacitively boosted time-to-digital converter that operates at low supply voltages and achieves high resolution.

Chapter 5 – Presents the proposed ADPLL architecture that consumes low power and silicon area and covers the MedRadio frequency band.

Chapter 6 – Presents and discusses the proposed sequence tree analysis for designing negative skewed ring oscillators. The analysis is also validated with simulation and measurement results.

Chapter 7 – Concludes the thesis and provides recommendations and suggestions for the future work.

Chapter 2

Literature Review

One of the main aim of this thesis work is to investigate different state-of-the art architectures of flip-flop, time-to-digital converter, ring oscillator and all-digital phase locked loop for its suitability to be used in designing a low power medical implant SoC. Hence this chapter will review the various available architectures of these 4 circuit blocks.

2.1 Flip-Flop and Sense Amplifier Flip-Flop

The most conventional FF topology consisting of tristate inverters and transmission gates was presented in 1994 as shown in Figure 2.1. By eliminating short circuit power dissipation using tristate inverters, it achieved good speed and reduced power consumption. But its large clock load still influenced its overall total power consumption [31].

Another type of FF namely the flow-through latch or hybrid-latch FF (HLFF) which utilized a short transparent sampling window for data flow was then reported as shown in Figure 2.2. Due to its flow-through property, the latch exhibited a negative setup time and was robust to clock skew issues. But the circuit had a constraint on the transparency window which determined its hold time. Larger transparency window increased its hold time and a shorter window affected the switching of the latch leading to reliability issues [32].

Figure 2.1 – FF design using tristate inverter and transmission gate [31]

Figure 2.2 – Flow-through latch [32]

In order to attain high speeds and eliminate the drawbacks of previous topologies, a semi-dynamic FF (SDFF) was then introduced as shown in Figure 2.3. But it still suffered from a large clock load and pre-charge capacitance which increased its overall power consumption [33].

Figure 2.3 – Semi-dynamic FF [33]

Even though, the power consumption and the propagation delay of a FF is inversely proportional, the demand for FFs achieving very low power-delay products (PDP) are growing. The power-delay product is defined as the product of power consumption and the longest clock-to-output propagation delay (C-Q) of the flip-flop [34]. This shows that even when a FF is designed to achieve very low propagation delay, the asymmetrical rise and fall propagation delays in which either one is usually less and the other is more due to different charging and discharging structures, weakens the advantages of the design done to achieve low propagation delays. This is because of the longest clock-to-output propagation delay that determines the PDP of the FF.

Meanwhile, a new class of FF namely the sense amplifier FF (SAFF) having a sense-amplifier (SA) stage as master stage and latch stage as slave stage was introduced as shown in Figure 2.4. Sense amplifiers (SA) were conventionally used in memory designs to detect small voltage swings applied at its differential inputs and amplify the voltage difference to full rail swing [35].

The SAFF achieved better performance characteristics in terms of speed and power dissipation compared with previous conventional FF topologies. It also operated effectively with reduced clock swings. However the slave latch stage which consisted of a NAND based S-R latch led to a longer clock-to-output propagation delay with asymmetrical timing [36]. This asymmetric property makes one output to depend on other leading to highly imbalanced rise / fall output propagation delays. This imbalance increases the PDP and causes glitches in the subsequent digital logic which eventually give rise to reliability issues and shoot-up in overall power consumption.

Figure 2.4 – Conventional sense amplifier FF [36]

In order to overcome the above issue, a SAFF with a symmetrical slave S-R latch stage was later presented [37] as shown in Figure 2.5. In this design, the critical pull-up and pull-down paths were constructed using single transistor to speed up the transition. However, the slave latch consists of transistor stacking of up to 4 devices which increases the effective output resistance imposing a limit on the minimum achievable propagation delay.

Moreover, even though the slave latch has been designed to achieve symmetrical outputs there is still an asymmetry having a time delay closer to a gate delay between the rise and fall propagation delays.

Figure 2.5 – Nikolic SAFF [37]

Another SAFF topology which achieved low propagation delay than [28] also suffered from larger asymmetrical delays at ultra-low supply voltages due to poor drive strength [38] as shown in Figure 2.6.

Figure 2.6 – Strollo SAFF [38]

Recently, other improved performance SAFF topologies such as the boost-bulk SAFF (BBSAFF) [39] as shown in Figure 2.7 and the transition completion detection SAFF (TCD-SAFF) [40] as shown in Figure 2.8 were proposed and they also suffer from larger asymmetrical delays due to a greater imbalance between their output charging and discharging paths.

Figure 2.7 – Boost-bulk SAFF [39]

Figure 2.8 – Transition completion detection SAFF [40]

2.2 Time-to-Digital Converters

TDCs have been traditionally widely used before for accurate time interval measurements in the area of high-energy and particle physics [41][42][43]. With the current advances in technology, today TDCs are widely used in applications such as ADPLL [44], jitter measurements, time mode analog to digital converters [45] and biomedical applications [23][46].

2.2.1 Performance Metrics of TDC

A TDC works similarly like a analog-to-digital converter (ADC). It digitizes the time interval between two input signals to generate a output code depending upon the time difference. The important specifications that determine the performance of the TDC are summarized below,

- ❖ **Measurement Range** - The TDC measurement range or dynamic range (DR) denotes maximum time difference the TDC can measure before overflowing. Larger measurement ranges are required for time of flight measurements in particle physics experiments and shorter measurement range is required for time of flight measurement of digital systems such as jitter measurement and ADPLL. Dynamic range is usually denoted by number of bits (n) and resolution of the TDC (T_{LSB}),

$$\text{Measurement Range, } DR = 2^n \cdot T_{LSB} \quad (2.1)$$

- ❖ **Resolution** - The TDC resolution (T_{LSB}) denotes the degree of fineness the TDC can quantize an input time interval. The resolution of the TDC can also be called as least significant bit (LSB). Higher the resolution better the TDC performance.
- ❖ **Sampling Rate** - The sampling rate (F_s) of a TDC describes how fast the TDC can convert the given input time difference into a digital code. Dead-time or latency is the time the TDC does not perform any conversion after the current time conversion is finished.

If the TDC is a single stage TDC without any pipelining, the maximum conversion speed or the sampling rate is given by,

$$\text{Maximum Sampling Rate, } F_{Smax} = \frac{1}{DR} \quad (2.2)$$

- ❖ **TDC Non-Linearity** - Non-linear imperfections are all deviations of a TDC characteristic from its expected shape that lead to non-linear distortion. The deviation in the step position from its ideal digital code is called as integral non-linearity (INL). The deviation of each step from its ideal value T_{LSB} is called as differential non-linearity (DNL). Both the DNL and INL are generally normalized to one T_{LSB} .
- ❖ **Power Consumption** - This describes the operational power consumption of a TDC. It is desirable to have lower power consumption. The TDC power consumption usually depends directly upon the resolution, measurement range and sampling rate.
- ❖ **Figure of Merit** - The TDC figure of merit (*FOM*) denotes a standardized approach to compare the performance of the TDC across different technology nodes and process. The *FOM* takes into account the non-linear effects of TDC, number of bits of TDC, TDC power consumption and the sampling rate of the TDC. The *FOM* is given by the unit pJ/conversion step [47],

$$\text{Effective number of linear bits, } N_{linear} = Bits - \log_2(INL + 1) \quad (2.3)$$

$$FOM = Power / (2^{N_{linear}} \cdot FS) \quad (2.4)$$

2.2.2 TDC Architectures

This section provides an overview of basic and advanced techniques used for accurate measurement of time intervals. The time interval which is to be digitized by the TDC is usually assumed to be the interval between two asynchronous timing events namely START and STOP pulses.

2.2.2.1 Counter based TDC

Counter based time measurement has a free running reference clock having time period of T_{REF} and a counter structure [48]. The counter counts the number of reference clock cycles between the START and STOP pulses to give the digital code. The frequency and stability of the reference clock determine the resolution and accuracy of this scheme. This method offers a very large dynamic range, in a highly integrated digital design. However, to obtain high resolution a reference clock frequency on the GHz range is required and thus, this architecture consumes very high power when high frequency clocks are used. Due to the asynchronous nature of both the START and STOP events, there is a quantization associated with both starting and stopping the counting process, resulting in the maximum quantization error to be $2 * T_{REF}$. The resolution of the counter based TDC is usually limited to few hundred ps.

2.2.2.2 Delay Line TDC

To overcome the limitations of counter based TDC namely the poor resolution, delay line based TDCs were introduced [44] [49]. In this technique, several delay elements usually inverters or buffers are connected in series to make up a delay line through which a signal event is propagated as shown in Figure 2.9. The progression of the pulse along the delay line reflects the time interval being measured as shown in Figure 2.10. The other signal pulse is used to sample the delay elements using arbiters or flip-flops to get a thermometer digital code equivalent to the time interval to be measured as shown in Figure 2.10. The delay line TDC offers resolution which is limited by the delay of a single inverter for the given technology node which is usually around 50 ps. To cover a large measurement range, long delay chain is required which gives rise to non-linearities and higher power consumption. Another drawback is that the delay line is susceptible to PVT variations and the resolution is directly dependent on the unit delay of the buffer present in the line which can also vary due to PVT variations.

Figure 2.9 – Delay Line TDC [44]

Figure 2.10 – Working principle of the delay line TDC [44]

2.2.2.3 Vernier Architecture TDC

The Vernier delay line TDC has two parallel delay lines with delay elements having different delays [50]. One delay line has delay elements having a delay of τ_1 per delay element in which the START signal is given into. Another delay line has delay elements having a delay of τ_2 per delay element in which the STOP signal is given into as shown in Figure 2.11. In the Vernier TDC $\tau_2 < \tau_1$ and this makes the STOP signal to catch up with START signal in a vernier fashion as shown in Figure 2.12. The vernier delay line TDC offers resolution which is the difference between two delays of the two delay elements and hence it can be made very smaller. But practically, it is limited by the noises in the

delayed START and STOP signals, such as jitters and mismatches between the delay elements in the individual delay lines. To cover a large measurement range, long delay chains are required which gives rise to non-linearities and higher power consumption. Hence, the vernier delay line TDC has a large latency, or low conversion rate, for the resolution and measurement range that it can offer. The vernier delay line TDC has also been extended to 2-dimensional version [51] to reduce the conversion time, number of delay elements, and increasing overall efficiency. The vernier TDC also provides a 1st order immunity against variations in PVT since the resolution depends upon the time difference of the delay elements.

Figure 2.11 – Vernier delay line TDC [50]

Figure 2.12 – Working principle of vernier delay line TDC [50]

2.2.2.4 Ring Oscillator TDC

All the TDCs discussed above has its range limited by the length of its delay line. A straightforward way to extend the range of the TDCs is to use ring oscillators or cyclic structures [52] as shown in Figure 2.13. A ring oscillator is a delay line where the end is fed back to the input to form a loop structure. Because of this feedback, the delay line is re-used again after it reaches its limit. The range of the TDC can be extended by adding a counter to the ring oscillator where the counter counts the number of cycles completed by the ring oscillator within an input time interval. Therefore, the input time interval is quantized in terms of the number of completed cycles and the phase change of the ring oscillator. The major drawback of the ring oscillator TDC comes in the form of the free running nature of the ring oscillator. This leads to higher power consumption. Another drawback is that the ring oscillator as like the delay line is susceptible to PVT variations and the resolution is directly dependent on the unit delay of single inverter which can vary due to PVT variations.

Figure 2.13 – Ring Oscillator TDC [52]

2.2.2.5 Vernier Ring Oscillator TDC

The vernier ring oscillator TDC is a merger of ring oscillator TDC and vernier delay line TDC by which two ring oscillators running at different frequencies are used [53][54]. Due to difference in frequencies, the delays of the delay elements of the fast ring oscillator and slow ring oscillator is different, by which the fast ring oscillator catches up with the slow ring oscillator in a vernier fashion to give a vernier resolution and at the same time a higher measurement range as shown in Figure 2.14. Similar to the ring oscillator TDC, counters are used to extend the range of the TDC. The major disadvantage of the Vernier ring oscillator TDC comes in the form of the free running nature of both the ring oscillators. This leads to higher power consumption than the ring oscillator TDC which has only one free running ring oscillator. The vernier ring oscillator TDC also provides a first order immunity against PVT variations since the resolution depends upon the time difference of the delay elements.

Figure 2.14 – Vernier ring oscillator TDC [54]

2.2.2.6 Gated Ring Oscillator TDC

In order to control the free running nature of the ring oscillators used in ring oscillator based TDCs, the oscillator is enabled or disabled depending upon the input time difference between the START and the STOP signals in the gated ring oscillator (GRO) TDC [55][56]. The START and STOP signals are feeded into pulse generator logic, which produces a pulse width proportional to input time interval. The pulse enables and disables the GRO from oscillating as shown in Figure 2.15. Before the START signal arrives, the GRO is reset to a known state and when the STOP signal comes, the phase of GRO is sampled. Thus, between two consecutive measurements, the status of ring oscillators is freezed by the GRO, and the time residue obtained is moved to the time interval of next conversion. Thus a differential operation is made on the residue of each conversion by continuing the next time quantization from the previous results. This represents a 1st order noise shaping of quantization error in frequency domain. Consequently, the in-band phase noise is filtered out and the effective resolution of the TDC is improved.

Figure 2.15 – Gated ring oscillator TDC [55]

2.2.2.7 Passive Interpolation TDC

Sub-gate delay resolution can be achieved by the passive interpolation TDC, in which the coarse time interval given by an inverter buffer is subdivided or interpolated [57]. The basic principle of the passive interpolation TDC as illustrated in Figure 2.16 is similar to the voltage interpolation that takes place in folding ADCs or interpolating flash. Let us assume two signals having rising transitions with a delay of one inverter delay. A simple CMOS inverter provides a signal transition time that is equal to the gate delay. If the rise time of the CMOS inverter is larger than its gate delay, the second signal starts rising while the first signal still increases. When these signals are given to a comparator latch, the latch detects the midlevel crossing and produces a new signal which can be used to quantize the time interval in between V_A and V_B . A passive resistive voltage divider as shown in Figure 2.17 can be connected between to generate the interpolated signals. Thus, the parallel sampling technique gives a high-resolution thermometer code at the same dead time and low latency like the delay line based TDC. When compared with the vernier TDC, this technique does not increase the measurement time while still achieving higher resolution.

Figure 2.16 – Time step interpolation [57]

Figure 2.17 – Resistive interpolator [57]

2.2.2.8 Time Amplification TDC

Most of the previously discussed TDCs creates narrowly spaced time events to achieve a higher resolution by using either by a delay line or vernier delay line. Time amplifier based TDCs are different, in which a time interval which is the coarse quantization residue is taken and stretched along the time axis [58]. The time amplifier enlarged time interval can then be digitized with a fine TDC approach as shown in Figure 2.18.

Figure 2.18 – Time amplification TDC [45]

2.2.2.9 Stochastic Interpolation TDC

The stochastic interpolation TDC (STDC) [59][60] is similar to the statistical ADC [61] which can achieve sub-gate resolution by using the inherent mismatches and variations of the comparators or arbiters to create fine interpolation of signals. Two different types of stochastic based TDCs have been previously proposed, namely using arbiter's offset and using phase interpolation [62].

The operation of the arbiter offset based STDC relies on the finite voltage offset between the two inputs of a set of arbiters. The STDC uses the stochastic properties of a set of arbiters or flip-flops for achieving a high time resolution. To illustrate the STDC working, consider a 1-bit TDC that is built with 1 arbiter. The two inputs of the arbiter are feeded with START and STOP signal. If STOP signal arrives after START crosses the midpoint V_{TH} of arbiter, the TDC will give an output "1", otherwise the TDC will give an output "0". Thus, the 1-bit TDC works similarly to a bang-bang phase detector.

Similarly, if an array of latches or arbiters are used as shown in Figure 2.19 and if the arbiters are assumed to be ideal with $offset = 0$, the output of all the arbiters will be the same for a given time comparison. However, in the presence of inherent mismatches, each of the arbiters will possess an input voltage offset which translates into a time offset T_{offset} that is slightly different from another arbiter. For a time comparison where ΔT is small, only those arbiters where $\Delta T > T_{offset}$ will output high, whereas the rest of the arbiters will output low. Since all the arbiters are identical, the input time offsets of these arbiters will have an identical distribution. Hence, according to the central limit theorem, the cumulative distribution of the input voltage offsets of these arbiters will approximately be normal or Gaussian. Hence, by summing the outputs of all the arbiters measuring the same ΔT , the digital output of this stochastic based TDC can be obtained.

Figure 2.19 – Arbiter based stochastic TDC [60]

2.2.2.10 Pulse Shrinking TDC

Apart from the TDC architectures discussed above, the pulse shrinking TDC [63] accepts a pulse signal as its input where the pulse width is proportional to the time interval to be measured. The pulse is fed through a chain of pulse shrinking delay elements that shrinks the pulse by a certain amount each time it passes through a pulse shrinking element. As the input pulse propagates through this chain, the pulse width slowly decreases and eventually vanishes. As the pulse propagates through the pulse shrinking chain, it will drive the arbiters to high. At the point where the pulse vanishes, the corresponding register and the other registers after this will have its output remaining at low. This results in a thermometer code, which can be decoded to form a binary output.

2.3 All-Digital Phase Locked Loop

This section discusses and reviews the key performance metrics of the PLL, the basic operation of analog PLL, all-digital phase locked loop (ADPLL) and existing ADPLL architectures. The drawbacks of analog PLL and the need for moving towards all-digital PLL architectures is also briefly summarized.

2.3.1 Performance Metrics of PLL

An analog PLL or ADPLL is normally used as a local oscillator (LO) or frequency synthesizer in the transceiver. The PLL generates an output clock with a frequency that is programmable for use in clock generators or for use in up-conversion and down-conversion in a wireless transceiver as it can provide a range of frequency signals with good spectral purity.

Figure 2.20 shows the frequency synthesizer block diagram which is designed using a PLL.

Figure 2.20 – Frequency synthesizer

A frequency synthesizer gets a clean reference signal as an input from a crystal oscillator which has a low frequency and produces an output signal whose frequency is determined by the frequency command word (FCW). Some of the commonly used metrics that is used to assess the frequency synthesizer performance are discussed below,

- ❖ **Frequency Tuning Range** - The frequency tuning range represents the range of signal frequencies which can be produced by the synthesizer can generate with acceptable resolution and signal quality.
- ❖ **Switching Time** – The time the frequency synthesizer takes to change from one signal frequency to other with a specific accuracy. This is very critical for applications that require fast switching performance like Bluetooth.

❖ **Phase Noise** – In time domain, the frequency synthesizer output can be shown by (2.5), where A is the amplitude of the generated signal having frequency ω_c and $\varphi(t)$ refers to phase variations. Phase variations are divided into periodic variations and random variations and as shown in (2.6).

$$v(t) = A \sin(\omega_c t + \varphi(t)) \quad (2.5)$$

$$\varphi(t) = \Delta\varphi \sin(\omega_m t) + \emptyset(t) \quad (2.6)$$

The spurious tone which appear at a frequency ω_m from the carrier is denoted as the first term. The random fluctuations $\emptyset(t)$, appear as a noise-skirt around the desired frequency as shown in Figure 2.21. Both the noise skirt and spurious tones deteriorates the transceiver performance as shown in Figure 2.22.

The transceiver performance is further impaired by the spot value of the phase noise spectrum at a particular frequency and the integral of phase spectral density over a frequency range. On the transmit side, the noise-skirt present on the LO signal can make it a potential interferer (blocker) to a near-by receiver which is trying to detect a signal in the nearby adjacent frequency channel as shown in Figure 2.23.

Figure 2.21 – Output spectrum of oscillators [64]

Figure 2.22 – Phase noise and spurious tones [65]

Figure 2.23 – LO phase noise effect in transmitter [64]

Figure 2.24 depicts the frequency synthesizer phase noise impact on the receiver in the presence of a large blocker in the near-by frequency channel.

Figure 2.24 – LO phase noise effect in receiver [64]

2.3.2 Analog PLL

Phase Locked Loops are widely used in transceiver systems and SoC chips for frequency synthesis and clock generation. Implementation of conventional analog PLLs (APLL) requires bulky charge pump, passive RC low pass loop filter and LC voltage controlled oscillator (VCO) circuits as shown in Figure 2.25. These analog intensive circuits also occupy large chip area and its performance is prone to process, voltage and temperature (PVT) variations. With current advances in CMOS technology scaling, conventional APLLs are not easily compatible and portable to other technology nodes. Hence the need arises to move towards digital intensive design methodologies for implementing PLL circuits that uses lesser analog circuits, is portable easily to other CMOS technology processes and occupy less silicon area.

Figure 2.25 – Analog phase locked loop

2.3.3 ADPLL Architectures

All analog PLL sub-blocks are substituted by corresponding mixed signal circuits or digital circuits in an ADPLL and these equivalent circuits have digital input and output interfaces. A time-to-digital converter (TDC) is used in place of phase frequency detector (PFD) and charge pump. The TDC converts the time and phase difference between the output and reference clock into digital codes. The passive RC filter of the APLL is substituted by a digital loop filter (DLPF) because the phase error is digitized. The APLL's voltage controlled oscillator which is controlled using an analog voltage is changed to digitally controlled oscillator (DCO) which is controlled by the digital loop filter using digital control words. Thus, the DCO produces an output frequency that is proportional to the input digital control word. There are two architecture types of ADPLL namely the divider-less and divider-based ADPLLs which are explained as follows.

2.3.3.1 Divider-Less ADPLL

The block-level architecture of the divider-less ADPLL or counter based ADPLL is shown in Figure 2.26 [66][67][68]. This type of ADPLL does not have a divider in the feedback path as opposed to the conventional analog PLL. The output variable clock (CKV) is set by the frequency command word (FCW) where FCW is the number of variable clock cycles within one reference clock (FREF). The FCW is accumulated at the rate of reference frequency using an accumulator (ACC) to provide the output period normalized reference phase. The TDC performs both the fractional conversion of phase error and integer conversion of phase error. The integer part of the output phase is generated by counting the number of output clock cycles. The fractional part of phase error is generated by fractional phase error quantizer.

With this, the variable phase is digitized to a digital word using the TDC and the reference phase is digitized to a digital word using the FCW accumulator. The digital logic subtracts the reference phase and the variable phase digital words to produce the phase error. This phase error is then provided to the digital filter which then generates the oscillator tuning control word (OTW). The DCO frequency is controlled by the OTW in a negative feedback configuration. The ADPLL loop works in a way such that the CKV and reference clock phases either have a constant phase difference or become equal in the steady state, which depends on the loop type employed in the ADPLL. The output signal frequency is therefore equal to $FCW * \text{reference frequency}$.

Figure 2.26 – Divider-less ADPLL

2.3.3.2 Divider-Based ADPLL

The top-level architecture of divider-based ADPLL [69] [70] shown in Figure 2.27 is the digital equivalent of the analog PLL. The phase frequency detector and charge pump of the analog PLL is replaced by a TDC. The RC low pass filter is replaced by a digital loop filter. The VCO is replaced by a DCO. The output variable clock is passed through a fractional divider and then to the TDC for digitizing the phase error. The output clock frequency is set by the divider ratio and a sigma delta modulator (SDM) is used to dither the divider ratio between two integer values to achieve a fractional division ratio.

Figure 2.27 – Divider-based ADPLL

2.3.3.3 Architecture Comparison

Table 2.1 gives the main performance metrics comparison between divider-less ADPLL and divider-based ADPLL architecture.

Table 2.1 – ADPLL architecture comparison

	Divider based	Counter based
TDC range requirement	Large – due to coverage requirement of 1 reference clock cycle	Small – due to coverage requirement of 1 output clock cycle
TDC power	Small – due to operating at reference clock frequency which is usually lower	Large – due to operating at output clock frequency which is higher
Flexibility	Better – due to the presence of divider and SDM	Best – due to the presence of accumulator based architecture

2.3.4 Biomedical Implant ADPLL Designs

Since biomedical implants are one of the emerging research topics, there are only quite a few analog PLL and ADPLL designs reported for biomedical implant applications. A controller based ADPLL for MICS transceivers was proposed as depicted in Figure 2.28 [71]. The phase difference is indicated with their pulse widths as output signals DN and UP from the PFD. The controller digitizes the phase difference by measuring the DN and UP signals.

The phase error is counted by the accumulator in the controller with a time resolution in the order of output clock signal period. The controller adjusts the digital control words, based on the frequency and phase errors. The LC based DCO generates the output signal with a frequency which is controlled by the digital control words from controller. Based on the phase control word, one of the multi-phase signals is selected by phase selector with least phase error.

Figure 2.28 – Controller based ADPLL [71]

Another ADPLL designed for transceiver SoC utilizes a LC oscillator and digital-to-time (DTC) converter based TDC range reduction technique to reduce power consumption of the ADPLL as shown in Figure 2.29 [24]. The DTC narrows aligns the reference clock edge closely with the output clock edge in order to narrow down the measurement range of the TDC. This architecture resembles a two stage TDC architecture, where the DTC takes care of the longer measurement range with a coarse resolution and the TDC takes care of the shorter measurement range with fine resolution. But since the TDC measurement range is reduced, the power consumption of the TDC is reduced.

Figure 2.29 – Medical implant ADPLL [24]

Figure 2.30 shows a proposed master-slave ADPLL architecture [72] for reducing power consumption. The proposed architecture consists of a master PLL producing a low frequency which is followed by a high output frequency slave injection-locked oscillator. The master PLL contains a fractional-N coarse-lock unit and the slave oscillator contains a fine frequency initialization unit. Two fast-lock modes are supported in the PLL and they are: 1) start-up locking from power-down mode and 2) instantaneous relocking from standby mode. To remove drifts in free running frequency, a frequency error compensation circuit is built in the slave oscillator.

Figure 2.30 – Master slave ADPLL architecture [72]

Figure 2.31 shows a proposed ADPLL with embedded cyclic TDC [73]. The ADPLL consists of a PFD, controller, frequency finder, digital loop filter and an embedded cyclic TDC. The frequency finder computes the initial DCO control code after which the frequency divider, PFD and DCO are started at the next rising edge of the reference clock. This eliminates the phase error when the ADPLL returns to the normal frequency and phase acquisition process. But, since the frequency finder has a limited resolution, frequency errors are caused. The embedded cyclic TDC has an interpolation stage with fine resolution to reduce the frequency errors. The frequency estimation algorithm used in the design enables to achieve a faster settling time for the ADPLL.

Figure 2.31 – Embedded TDC based ADPLL [73]

2.4 Ring Oscillators

LC oscillators and ring oscillators (RO) are widely used as voltage controlled oscillators and pulse generators in SoC applications. The LC oscillator utilizes a passive on-chip monolithic inductor together with a resonating capacitor structure in the form of MOS varactors for tuning the output frequency. The presence of inductor makes the LC oscillator to relatively exhibit low phase noise, low timing jitter and high linearity when compared with ring oscillators [74]. At the same, the LC oscillator also exhibits several drawbacks in CMOS process, which are described as follows,

- ❖ The LC oscillator do not possess a wider tuning range as like a RO [75].
- ❖ The inductor occupies a large silicon area and also possess substrate loss which is due to the silicon substrate's high conductivity [74].
- ❖ At high frequencies, the ohmic losses of the inductor leads to a low Q factor and this worsens the Q factor of overall resonant circuit [76].

Thus, in order to overcome these issues and challenges, RO is widely used in recent years. Unlike the LC oscillator, RO does not an inductor and it is built only using delay cells without any resonant tank circuit. The RO also satisfies the Barkhausen's oscillation criteria which states that, at a frequency, the phase shift around the feedback loop must be an even multiple of 360° or 0° and the loop gain magnitude at that frequency must be unity.

Odd or even number of delay cells (N) coupled in a positive feedback loop can be used to build a ring oscillator as shown in Figure 2.32 [77]. The RO delay cells can be arranged in either single-ended or differential configuration. The single-ended RO is built by a chain of CMOS inverters where the number of inverters must be odd in order to achieve oscillation. Each inverter consists of a NMOS and PMOS transistor. The differential RO (DRO) is built by a chain of delay cells which can be either even or odd depending upon the feedback connection.

The fundamental limitation of the ring oscillator is that its propagation delay time resolution is determined by the time delay of single stage buffer. More delay cells can be added to create more output phases at the expense of degradation in the maximum output oscillation frequency. This type of architecture where only the primary set of inputs are used to construct the RO is called as single-loop or single-path architecture and its oscillation frequency is determined by the single stage propagation delay.

Figure 2.32 – Ring oscillator with N delay cells [77]

There are also other types of RO architectures which uses secondary inputs in addition to the primary inputs where the secondary inputs are switched before the primary inputs to increase the maximum oscillation frequency of the RO. This architecture is called as multi-loop RO architecture. Some of the widely used ring oscillator architectures for increasing the output frequency are reviewed as follows,

One of the earliest reported architecture is the array oscillator structure shown in Figure 2.33 which is based on the coupled ring oscillator [78]. A series of coupled ring oscillators are used to build an array oscillator. By coupling a number of ring oscillator together, the dependency of output frequency on number of delay buffers is eliminated. By adding more rings, the delay resolution can be increased without affecting the oscillation frequency.

Several ring oscillators running at constant frequencies are forced to be uniformly offset in phase and this uniform spacing is generated by the coupling between the rings. This divides the buffer delay into many time intervals by using the outputs from each ring. The array oscillator buffer cell is designed using an NMOS source-coupled pair. The pair is constructed using a NMOS current source which is dynamically-biased and symmetric load elements as depicted in Figure 2.34. A source-coupled pair which shares the same current source and load is used to form the coupling input. The load of the delay cell is symmetric and utilizes a diode connected PMOS which is connected in parallel with a biased PMOS transistor. The bias voltage of NMOS current source is provided by the control voltage, which is also used to tune the delay of the buffer.

Figure 2.33 – Array oscillator structure [78]

Figure 2.34 – Dual-input differential buffer [78]

Another technique, namely self-timed ring oscillators (STRO) which utilizes additional asynchronous logic to enable multiple oscillating edges to propagate simultaneously was proposed as shown in Figure 2.35 [79][80]. The architecture of a STR shown above consists of a ring of L stages. Each stage consists of an inverter and Muller gate. The muller gate is shown in Figure 2.36. There are two propagation delays associated with each stage which are the forward and reverse static propagation delays associated to inputs F and R . There are several ways to tune the oscillation frequency of the STRO. One way is to set the number of tokens and bubbles at the ring initialization. Another way is that the token propagation rules can be modified to tune the oscillation frequency.

Figure 2.35 – STRO architecture [80]

Figure 2.36 – Muller gate [79]

The circuit of the delay cell employing the negative skewed delay scheme is shown in Figure 2.37. This ring oscillator is called as negative skewed ring oscillator (NSRO). Proposed in [81], the NSRO oscillation frequency increases as the weaker PMOS is compensated by turning it on earlier during the low-to-high transition. In addition, the high-to-low transition time is shortened by turning the PMOS off prematurely before the NMOS turns on, reducing the amount of short-circuit current as shown in Figure 2.38.

Figure 2.37 – Negative skewed delay cell [81]

Figure 2.38 – Transient operation of negative skewed delay cell [81]

To achieve multi-path implementation, the inverter delay cell must be modified to allow multiple inputs. There are many ways to do this. One way is to connect the NMOS and PMOS inputs asymmetrically to different delay stage outputs. For the slow PMOS transistor, this enables the early arrival of input transitions which speeds up the delay stage. Another way is to have multiple connections to all inverter stages. The third way is to combine these two ways. The combination of coupled ring oscillators and negative skewed delay scheme led to the multi-path or sub-feedback loop ring oscillators [55].

The multi-path technique feeds multiple output taps of a ring oscillator back into its each stage using additional input transistors. The multiple feedback paths are also uniform for all ring oscillator stages as depicted in Figure 2.39.

Figure 2.39 – Multi-path structure [55]

2.5 Observations from Literature Review

After investigating various circuit architectures and performing extensive literature survey on the 4 circuit blocks mentioned before, the following observations have been made.

Ultra-low area circuit topologies and low power circuit blocks are required to ensure miniaturization and longer battery life for medical implantable devices. An aggressive supply voltage scaling is one of the main widespread approaches used to decrease circuit power consumption, because the circuit's dynamic power consumption is proportional to the voltage square. However, this aggressive decrease in supply voltage causes poor driving ability and a deterioration in speed due to a larger transistor threshold voltage. Another technique to lower the circuit power consumption is to use near-threshold computing, in which the V_{DD} of the circuits is kept at a range of the transistor threshold voltage to achieve a balanced performance [82]. Nonetheless, digital circuits having supply voltage at the near-threshold voltage region still show poor drive capability and switching speed performance.

Flip-flops are one of the most regularly and vitally used circuit block in any integrated circuit. Digital intensive and mixed-signal based circuit architectures such as processor unit and controller unit contain complex circuits such as pipelining elements, logic blocks, memory, frequency dividers and counters which need a good flip-flop design for reliable working. Also, for ultra-low voltage applications, the emphasis on good flip-flop design is even more critical.

Thus, flip-flops capable of operating reliably at V_{DD} which is lesser than the transistor threshold voltage and providing performance metrics such as low propagation delay (clock-to-output, C-Q), good drive strength and low power-delay product is crucial. The present flip-flop topologies suffer from poor driving capability leading to poor PDP performance and speed degradation at ultra-low V_{DD} . Also, the existing FF topologies cannot sample data signals which has low voltage swings directly without the need of intermediate level shifting. Thus, a wide-input dynamic range FF capable of sampling data signals having low voltage swings at low supply voltages is essentially required for biomedical implants to save the additional power and area overhead that arises because of the use of level shifters and buffers.

Even though, the present TDC architectures are capable of achieving time resolutions in the order of sub-gate delay, all of the existing TDCs work at a V_{DD} of 1 V and above. The TDC performance metrics such as linearity and resolution is severely affected when the operating V_{DD} is reduced. At ultra-low V_{DD} , the TDC's capability to drive the time arbiter array is also affected which results in larger non-linearity and unreliable sampling.

Phase locked loops are widely used to provide a clean reference signal having a steady output frequency. Nevertheless, traditional analog PLLs are constructed using analog intensive circuit blocks such as RC low pass filters, LC oscillators and charge pump. These analog intensive circuits are not easily portable from one process to other process and they also occupy a large silicon area due to the presence of passive components.

As the CMOS transistor channel length decreases and the V_{DD} is aggressively reduced to 1 V and less than that, much importance is given towards moving to circuit design techniques that are digitally intensive. All these have favored the growth and rise of all-digital phase locked loops (ADPLL). These ADPLLs use circuit blocks such as digital loop filter, time-to-digital converter and digitally controlled oscillator which are all highly digitally intensive.

Even though the currently available ADPLL architectures offers many advantages when compared with a conventional analog PLL in performance metrics such as phase noise and jitter, portability, low power and silicon area consumption, there is still a big space available for improving their performances for using in medical implants. The radio transceivers present in medical implant devices use the frequency band having a range from 401 MHz - 457 MHz named as medical device radio communications service (MedRadio) [83][17]. Moreover, the present biomedical implant ADPLLs available in literature utilizes TDC and LC oscillator which is not easily portable across CMOS technology nodes and consumes more silicon area. Thus, the use of TDCs and LC oscillators can be avoided in the ADPLL design in order to ensure low silicon area consumption and easy portability required for medical implants.

All the existing ring oscillator design techniques increase the oscillation frequency by more than two-fold while generating multi-phase outputs. However, since the negative skewed delay scheme only reconfigures the input connections, it is the only technique that uses the same number of transistors as compared to the conventional ring oscillator.

Hence, this scheme is the simplest, adds least noise sources and area overhead which are attractive metrics for use in medical implant SoCs. Therefore, even though this scheme is two decades old, it is still being actively employed in recently published ADC [84] and TDC [85] designs. Moreover, the optimum skew suggested by the original literature [81] is 2 inverters delay, but in reality it is not the case. This discrepancy has resulted in insufficient emphasis being placed on the negative skewed delay scheme where the scheme has only been applied to single-ended (SE) ring oscillators, limiting its usefulness where differential ring oscillators mainly only employ the multi-path technique and do not use the negative skew technique.

Moreover, the original literature [81] states that the increase in oscillation frequency is due to the reduction of short circuit current during the high-to-low transition and the compensation of a normally weaker PMOS in the low-to-high transition. While the analysis for the high-to-low transition is reasonable, the counterpart for the low-to-high transition is debatable. The PMOS can be sized appropriately such that it can have approximately the same or even stronger driving strength as compared to the NMOS. Moreover, if the same analysis from the high-to-low transition is applied to the low-to-high transition, such that the PMOS turns on prematurely before the NMOS turns off, there will be an increase in short circuit current during the low-to-high transition.

This leads to a large discrepancy between calculated and simulated oscillation frequencies of the negative skewed ring oscillator. Hence, the original analysis [81] does not adequately explain the large increase in oscillation frequency.

Chapter 3

Wide-Input Dynamic Range Flip-Flop

This section discusses and presents a wide-input dynamic range flip-flop that is designed in CMOS 40 nm and capable of operating at 0.16 V while still achieving least power-delay product (PDP) performance metric [26]. The section starts with a basic introduction about sense-amplifier flip-flop (SAFF) architecture which the proposed FF is based on.

3.1 Sense-Amplifier Flip-Flop

In general, a flip-flop contains a master pulse generator stage and a slave latch stage. Similarly, the SAFF consists of a sense amplifying stage as master stage followed by an S-R latch stage as slave stage as shown in Figure 3.1. Sense-amplifiers (SA) were conventionally used in memory designs to detect small voltage swings applied at its differentials inputs and amplify the voltage difference to full rail swing [35]. In a SAFF, the sense amplifier acts as a pulse generator which produces a pulse with duration depending upon the changes in the data D , $\bar{D}$ and clock CLK signals. This pulse triggers the slave S-R latch stage to either update with new value or hold back the previous value.

The operation of the circuit can be explained as follows. When the clock signal CLK is '0' or low, the sense amplifier output $\bar{S}$ and $\bar{R}$ is pre-charged to high or V_{DD} using P1 and P4 transistors, which turns on the transistors N4 and N5. This also enables the slave S-R latch to use its P6-N8 and P7-N9 cross coupled

inverter stage for holding the previous value. While at this state, the changes happening to the data signals will not be affecting the SA output, since the transistor N1 is turned off due to low clock signal. When the CLK switches to '1' or high, the sense amplifier detects the differential inputs which are applied at D , $\bar{D}$ and discharges one of its output node $\bar{S}$ or $\bar{R}$ either through N4 or N5 to ground or low, forcing the other output to stay at V_{DD} . The new values at $\bar{S}$ and $\bar{R}$ drives the S-R latch stage accordingly to update its output Q and $\bar{Q}$ depending on the data inputs, thus making the whole structure to efficiently work as a flip-flop. The interesting thing to note here is once the SA switches its state, either N4 or N5 is turned off and the SA stage is not affected by subsequent immediate changes in its data inputs. This short transparency window assures negative or zero setup time and a very short hold time leading to accurate timing characteristics.

Figure 3.1 – Conventional sense-amplifier flip-flop [36]

However, there is an inherent drawback with this conventional SAFF topology which leads to very high asymmetrical clock-to-output delays. The problem lies in the slave S-R latch stage which does not update its outputs Q and $\bar{Q}$ independently due to its structure. To illustrate this, if suppose D is high and $\bar{D}$ is low when CLK is high, $\bar{S}$ is discharged to ground through N4-N2-N1 while $\bar{R}$ remains high at V_{DD} . After $\bar{S}$ is discharged to ground, P5 is turned on to charge up the output node Q to high. Meanwhile, the high value at $\bar{R}$ turns on N7. Only after Q is pulled-up to high, N9 is turned on to pull down $\bar{Q}$ to low.

This asymmetric property makes one output to depend on other, leading to highly imbalanced rise / fall output propagation delays and increased power-delay product (PDP) which causes glitches in the subsequent digital logic. This eventually creates reliability issues and shoot-up in overall power consumption. This imbalance and the drive strength capability of SAFF becomes even worse when the supply voltage of the flip-flop is reduced, leading to speed degradation, poor PDP performance and unreliable operation.

Moreover, the currently available SAFF topologies cannot sample data signals with low signal swing. Thus, flip-flops that can operate at V_{DD} lower than the transistor threshold voltage and provide performance metrics such as low clock-to-output propagation delay (C-Q), good drive strength, low PDP and wide-input dynamic range is essential for medical implant SoCs.

3.2 Proposed Flip-Flop Design

The proposed capacitively boosted SAFF (CB-SAFF) design shown in Figure 3.2 utilizes a sense-amplifier as master and a SR latch as slave. The body connection of all the NMOS transistors used in the design is connected to GND and body connection of all the PMOS transistor used in the design is connected to V_{DD} , except for the PMOS transistor PT1 whose body connection is connected to its drain terminal to prevent the parasitic junction diodes from forward biasing. The sense-amplifier stage shown in Figure 3.2 a, uses two metal-oxide semiconductor (MOS) capacitors MC1 and MC2 to introduce capacitive boosting based detection of data signals [86]. This makes the SA stage to detect the data signals and amplifies them towards generating a large voltage signal swing from $-\beta.V_{DD}$ to $\beta.2V_{DD}$. This large swing drives the SR latch shown in Figure 3.2b with improved strength. Since the node A and node B has parasitic capacitance associated with it, β which is the boosting efficiency is always < 1 . The transistor sizes used to design the CB-SAFF is given in Table 3.1.

Table 3.1 – Design parameters of proposed CB-SAFF

Device	W (μm) / L (nm)	Device	W (μm) / L (nm)
PT1	1 / 40	PT2,N1	0.2 / 40
P1,P4	1 / 40	N2-N3	1.5 / 40
P2-P3, P6-P7	0.2 / 40	N4,N5,N6,N7,N8	0.2 / 40
P5, P8	2 / 40	N9-N10,N12-N13	0.4 / 40
MC1-MC2	5 / 1	N11,N14	2 / 40

Figure 3.2 – Proposed capacitively boosted SAFF [26]

a) Master stage - Capacitively boosted sense-amplifier

b) Slave stage - SR latch

The proposed CB-SAFF works as described below. When the clock signal CLK is '0' or low, one of the terminal of the MC1 boost capacitor is connected to GND by the buffer B1. The PT1 pre-charge transistor is turned on by buffer B2 to charge the boost capacitor MC1 to V_{DD} , making V_{DD} to also get connected with the node A. The buffer is essential to help in boosting the node A to $\beta.2V_{DD}$ when the CLK turns '1' and to prevent the clock signal loading with capacitor.

Similarly, the pre-charge transistor PT2 is turned on by inverter INV1 to charge MC2 to V_{DD} . The transistors P1 and P4 are turned on to pre-charge the sense amplifier stage outputs $\bar{S}$ and $\bar{R}$ to V_{DD} . Since $\bar{S}$ and $\bar{R}$ are '1', the transistors P5 and P8 are turned off. This enables the slave SR latch cross coupled inverter stage P7-N8 and P6-N7 to hold the previous value. Since the transistor N1 is also turned off, the output of SA is not affected due to changes in the data signals when the CLK is '0'.

When the CLK switches to '1' or high, the differential inputs applied at D , $\bar{D}$ is sensed by the SA stage and for example, if D is '1' or high and $\bar{D}$ is '0' or low, the signal $\bar{S}$ is discharged to node Z through transistors N4-N2. Paralelly, the transistor N1 is turned on to provide the boosted voltage of $-\beta.V_{DD}$ to node Z. Therefore, $\bar{S}$ is discharged to a boosted voltage of $-\beta.V_{DD}$, instead of GND . At the same time, the PT1 pre-charge transistor is turned off and this makes the node A to be connected to the boosted voltage of $\beta.2V_{DD}$ instead of V_{DD} through B1-MC1, thereby delivering the boosted voltage of $\beta.2V_{DD}$ to $\bar{R}$. At the slave latch side, the transistor P5 is turned on with increased strength due to the discharge boosted $\bar{S}$ which pulls up Q to V_{DD} . The transistor N14 is turned on with increased strength due to charge boosted $\bar{R}$ which pulls down $\bar{Q}$ to GND .

The operation is vice-versa and similar when $\bar{D}$ is high and D is low. The transistor N6 which is turned on always due to its gate terminal directly connected to V_{DD} provides a static operation. This is to ensure that, even when the data input signals changes during a high CLK , either $\bar{S}$ or $\bar{R}$ can be discharged to GND .

3.3 Simulation Results

The proposed capacitively boosted SAFF is designed using 40 nm / 1.1 V CMOS technology. Other SAFF topologies such as the recently published BB-SAFF [39] and TCD-SAFF [40], Nikolic SAFF [37] and conventional SAFF [36] are also designed in 40 nm CMOS for evaluating the performance metrics of all the SAFFs in a same environment. In order to have a fair comparison, all the designed SAFFs are optimized individually, have a load capacitance of 15 fF and use same W/L size for the input/output transistors. All the designed SAFFs are simulated using a supply voltage range from 0.16 V to 0.7 V at clock signal *CLK* frequencies of both 1 MHz and 50 MHz as shown in Figure 3.3, Figure 3.4, Figure 3.5 and Figure 3.6. A data switching activity of 50% ($\alpha = 50\%$) is chosen.

From the simulation results, it can be observed that the proposed CB-SAFF achieves the lowest power-delay product among all the other SAFF topologies for a V_{DD} of 0.16 V to 0.6 V. The proposed FF is also the only flip-flop which can work at a V_{DD} of 0.16 V at a *CLK* of 1 MHz as shown in Figure 3.3. The supply voltage is kept below 0.7 V, to prevent the parasitic junction diodes from forward biasing which will increase the overall power consumption. This phenomenon can also be observed in Figure 3.3. The setup time and hold time of the proposed FF at a V_{DD} of 0.5 V, *CLK* of 1 MHz is -10.94 ps and 25.18 ps. The proposed CB-SAFF achieves the lowest clock-to-output (C-Q) propagation delay at both *CLK* frequencies of 1 MHz and 50 MHz as shown in Figure 3.4 and Figure 3.5. At *CLK* frequencies of both 1 MHz and 50 MHz, the rise and fall clock-to-output propagation delay of the proposed CB-SAFF also shows good symmetry as shown in Figure 3.6.

Power-delay product versus supply voltage @ CLK 1 MHz

Power-delay product versus supply voltage @ CLK 50 MHz

Figure 3.3 – Variation of PDP with supply voltage at different CLK frequencies

Figure 3.4 – C-Q delay versus supply voltage, CLK = 1 MHz

CLK and $D = 1$ V swing

Figure 3.5 – C-Q delay versus supply voltage, CLK = 50 MHz

CLK and $D = 1$ V swing

Figure 3.6 - Variation of C-Q delay of proposed CB-SAFF

D and $CLK = 1$ V swing

From simulation results, it can be observed that, the proposed CB-SAFF is the only FF design which is capable of sampling low swing data signals from a low voltage of 0.2 V to 1 V at a V_{DD} of 0.5 V and 50 MHz CLK frequency. The proposed flip-flop is also the only design that accurately sampled data signals from a low voltage of 0.2 V to 1 V even while working at a V_{DD} of 0.16 V and 1 MHz CLK frequency as shown in Figure 3.7. This proves the proposed design's capability of ultra-low V_{DD} operation and wide-input dynamic range.

Figure 3.7 - Output waveform at $CLK = 1$ MHz, $D = 0.2$ V, $V_{DD} = 0.16$ V

From the monte-carlo simulation results, it can be seen that the proposed FF design is robust across process variations and mismatches as shown in Figure 3.8 and Figure 3.9. For Figure 3.8, the mean of C-Q delay (rise) is 86.82 ps with $\pm 3\sigma$ variation of 14.46 ps and mean of C-Q delay (fall) is 86.08 ps with $\pm 3\sigma$ variation of 12.30 ps. For Figure 3.9, the mean of C-Q delay (rise) is 20.06 ns with $\pm 3\sigma$ variation of 1.04 ns and mean of C-Q delay (fall) is 5.71 ns with $\pm 3\sigma$ variation of 0.74 ns. The total number of runs selected is 200.

Figure 3.8 – Monte-carlo simulation at $CLK = 50$ MHz and $V_{DD} = 0.5$ V

Figure 3.9 – Monte-carlo simulation at $CLK = 1$ MHz and $V_{DD} = 0.2$ V

From Table 3.2, it can be seen that the proposed CB-SAFF design attains better performance at a low V_{DD} than existing SAFF designs. The proposed CB-SAFF is also the only FF design that can work reliably at a V_{DD} of 0.16 V. Using its capacitive boosting feature, the proposed FF can sample data signals having low voltage swing even while operating at CLK frequencies of both 1 MHz and 50 MHz at a low V_{DD} , where other flip-flop designs could not operate reliably.

Table 3.2 – Performance comparison of SAFF designs

Performance Metrics	Proposed CB-SAFF	[40] TCD-SAFF	[39] BB-SAFF	[37] Nikolic-SAFF
$CLK = 1$ MHz, Min V_{DD}	0.16	0.2	0.2	0.2
$CLK = 50$ MHz, Min V_{DD}	0.35	0.4	0.45	0.35
Sum of widths (μm)	35.1	22	30.4	24.2
Samples low-swing data	Yes	No	No	No
CLK of 50 MHz and V_{DD} of 0.5 V				
Rise C-Q delay (ps)	86.4	520.7	481.5	492.3
Fall C-Q delay (ps)	86.2	929.4	958.7	396.2
Supply (V)	0.5	0.5	0.5	0.5
Power (nW)	605.5	213.7	190.4	206.8
PDP (aJ) @ $\alpha = 50$ %	52.3	198.6	182.6	101.8
CLK of 1 MHz and V_{DD} of 0.2 V				
C-Q delay (rise) (ns)	20.007	84.477	81.374	81.207
C-Q delay (fall) (ns)	5.743	165.037	109.732	49.638
Supply (V)	0.2	0.2	0.2	0.2
Power (nW)	1.73	0.705	0.631	0.761
PDP (aJ) @ $\alpha = 50$ %	34.72	116.42	69.33	61.82

Table 3.3 summarizes the performance metrics of the proposed CB-SAFF at a V_{DD} of 0.16 V. The metrics are not compared with others, because other SAFF topologies were not able to operate at such an ultra-low V_{DD} .

Table 3.3 – Performance metrics of proposed CB-SAFF at 0.16 V supply

Performance Metrics	Proposed CB-SAFF
Rise C-Q delay (ps)	199207
Fall C-Q delay (ps)	26429
Power (nW)	0.901
PDP (aJ) @ $\alpha = 50\%$	181.07
Clock frequency (MHz)	1
Supply voltage (V)	0.16

3.4 Summary and Discussions

A novel FF design capable of working at an ultra-low V_{DD} of 0.16 V and having a wide-input dynamic range is proposed and designed in CMOS 40 nm process. The proposed capacitively boosted sense-amplifier flip-flop (CB-SAFF) uses a master stage which is constructed using a capacitive boosting sense-amplifier. The master stage detects the data signals and amplifies them to provide an output which has a voltage swing range from below GND to above V_{DD} . This capacitively boosted voltage is used to drive the slave latch stage with greater strength, thus achieving an overall low V_{DD} operation. The proposed CB-SAFF design outperforms the existing SAFF topologies in terms of performance metrics such as power-delay product and clock-to-output propagation delay while working at a low V_{DD} from 0.16 V to 0.6 V.

The proposed CB-SAFF and its capacitive boosting feature has the ability to detect and sample data signals having low voltage swing from 0.2 V to 1 V even while operating at a CLK of 1 MHz (V_{DD} of 0.16 V) and CLK of 50 MHz (V_{DD} of 0.5 V). The power consumption is one of the the most important metric for biomedical implant applications. However, with increase in number of clinical needs and increase in implant applications, other metrics such as output propagation delay and wide-input dynamic range are also becoming increasingly important. Hence, even though the proposed FF design consumes a bit more power than existing flip-flop topologies, its other advantages such as ultra-low V_{DD} operation, capability to have a wide-input dynamic range, low clock-to-output propagation delay and low PDP are still attractive for future biomedical implant applications.

Chapter 4

Capacitively Boosted TDC

This section proposes and discusses a capacitively boosted TDC which adopts a vernier architecture. Using the proposed capacitive boosting differential buffer, the V_{DD} of the TDC is scaled down to 0.6 V. This enables the proposed TDC to achieve high resolution, reliable sampling and good drive strength even when the proposed TDC is designed using 1.8 V transistors (standard threshold) available in the given 180 nm CMOS process development kit [27].

4.1 Proposed Capacitively Boosted TDC Architecture

The top-level architecture of the proposed capacitively boosted vernier delay line (CB-VDL) TDC is shown in Figure 4.1. It is a 6-bit vernier based TDC architecture which works on the vernier TDC principle reviewed in 2.2.2.3. When the supply voltage of the conventional vernier delay line TDC is reduced, the unit delay of each of the buffer increases. The buffer drive strength is also affected, since each buffer is loaded with a flip-flop. This poor drive strength leads to larger non-linearity, missing codes and false sampling in the final output code. Therefore, the proposed TDC is not designed using slow and fast delay lines which uses conventional inverter buffer. Rather, the proposed capacitive boosting differential buffer delay cell shown in Figure 4.2 is used to build the delay lines of the proposed TDC. This technique improves the driving capability of the buffer and allows to attain a fine time resolution while still operating at low supply voltage and consuming lower power.

The capacitive boosting function of buffer is indicated by double headed arrow.

Figure 4.1 – Proposed capacitive boosting TDC [27]

4.1.1 Proposed Capacitive Boosting Differential Buffer

The proposed capacitive boosting buffer boosts the swing of the output signal from $-\beta \cdot V_{DD}$ to $+\beta \cdot 2V_{DD}$ by utilizing a capacitive boosting technique [86] [87]. Four capacitors C1-C4 which are metal-oxide metal (MOM) capacitors are used as shown in Figure 4.2, where $\beta = Cap_C / (Cap_C + C_{parasitic})$. Since the nodes GN1, GN2, VD1 and VD2 has parasitic capacitance associated with it, β which is the boosting efficiency is always < 1 . The body connection of all the NMOS transistors used in the design is connected to *GND* and body connection of all the PMOS transistor used in the design is connected to the supply, except for the PMOS transistors whose body connection is shown which is done to avoid the parasitic junction diodes from forward biasing.

The transistor and capacitor size utilized for designing the capacitive boosting differential buffer is provided in Table 4.1.

Figure 4.2 – Proposed capacitive boosting differential buffer

Table 4.1 – Device size of capacitive boosting differential buffer

Device	W (μm) / L (nm)	Device	Capacitance (fF)
P1-P2	1.6 / 180	C1-C4	50
PP1-PP2	0.6 / 180	W (μm) / L (nm) - INV1-INV4 transistors, PMOS: 1.8 / 180 NMOS: 0.8 / 180	
LP1-LP2	1.2 / 180		
PN1-PN2	0.6 / 180		
N1-N2	0.7 / 180		
LN1-LN2	0.4 / 180		

The operation of the capacitive boosting buffer is described below. When the input signal $IN+$ turns '0' or low and $IN-$ turns '1' or high, the inverters INV1 and INV2 provide an output of '1' which connects one of the terminal of capacitors C1 and C2 to V_{DD} . The inverter INV3 and INV4 outputs are '0' which connect one terminal of the capacitors C3 and C4 to GND . The boosted voltage of $+\beta \cdot 2V_{DD}$ is delivered to the $OUT-$ output signal by turning off the transistor N1 and by turning on the transistor P1. The PN1 pre-charge transistor is turned on to charge the C2 capacitor to V_{DD} and the PP1 pre-charge transistor is turned off. The boosted voltage of $-\beta \cdot V_{DD}$ is delivered to the $OUT+$ output signal by turning off the P2 transistor and turning on the N2 transistor. This switches on the PP2 pre-charge transistor for charging the C3 capacitor to V_{DD} and the PN2 pre-charge transistor is switched off.

The operation is vice-versa and similar when the $IN+$ input signal is '1' or high and $IN-$ input signal is '0' or low. The INV1 and INV2 inverter outputs are low which connect one terminal of C1 and C2 capacitor to ground. The inverter INV3 and INV4 outputs are high which connect one terminal of capacitor C3 and C4 to V_{DD} . The boosted voltage of $-\beta \cdot V_{DD}$ is provided to the $OUT-$ output signal by turning off transistor P1 and turning on transistor N1. This also turns on PP1 pre-charge transistor to charge the C1 capacitor to V_{DD} and the PN1 pre-charge transistor is switched off. Similarly, the boosted voltage of $+\beta \cdot 2V_{DD}$ is provided to the $OUT+$ output signal by turning off transistor N2 and turning on transistor P2. Thus, the PN2 pre-charge transistor is switched on to charge the C4 capacitor to V_{DD} and the PP2 pre-charge transistor is switched off.

The source terminals of latch transistors LP1, LP2, LN1, LN2 are connected to the boost voltage nodes VD2, VD1, GN2 and GN1 for providing a cross-coupled boosted latching of $OUT+$ and $OUT-$ output signals. The boosted cross-coupled latching and the differential topology adopted in the proposed TDC enables the output signals to have sharp transition times, better common-mode rejection and noise immunity and low jitter when compared with the design in [87] which uses a single ended delay cell. The W/L of transistors P2-N2 and P1-N1 are sized differently in both the fast and slow delay lines for achieving a vernier time resolution of $\tau_1 - \tau_2$.

4.1.2 Delay Line Calibration

In order to tune or calibrate the vernier time resolution after the chip is fabricated, a delay line calibration circuitry should be incorporated inside the chip. The block-level architecture of calibration circuitry is presented in Figure 4.3. It uses a shunted-MOS capacitor bank with 4-bit resolution that is loaded at each capacitively boosted differential buffer output terminals $OUT+$ and $OUT-$. The control pins $CTW_0 - CTW_3$ is switched or tuned accordingly to vary the load capacitance which will in turn tune the time delay of the signal going through it. Since the proposed TDC adopts a vernier architecture, its time resolution is obtained by the delay difference between the fast and slow delay line elements. Thus, the vernier architecture offers 1st order immunity for PVT variations.

4.1.3 Time Arbiter

The time arbiter of the proposed TDC samples the START signal on the STOP signal rising edge along the delay chain using a bank of sense-amplifier flip-

flops (SAFF) [37] to produce a thermometer coded output. The main reason for using SAFF as time arbiter is, it has a very low metastability window. Metastability occurs when the data signal and clock signal has rising edges which are very close to each other.

Figure 4.3 – Delay line calibration unit using shunt-MOS capacitors

4.1.4 Digital Processor

The sampling time arbiter array indicates the position of signal catch-up with a 0 and provides 64-bit thermometer code output. The digital processor converts the thermometer code into a binary code using two steps as shown in Figure 4.4 [88]. Using a thermometer to one-hot (TM2OH) circuit, the 64-bit thermometer code is converted into a one-hot code (OH) as the first step by detecting the 1 to 0 transition point in the thermometer code output. Fat-tree encoder is then used to convert the 64-bit one hot code into a 6-bit binary code. The digital processing system also contains a bubble error correction circuit in order to eliminate the bubble errors that occurs during the conversion.

Figure 4.4 – Thermometer to binary conversion of proposed TDC

4.2 Post-Layout Simulation Results

To demonstrate the efficiency of proposed TDC design technique and for low cost prototype fabrication, the proposed capacitively boosted TDC has been designed in CMOS 180 nm process using 1.8 V transistors (standard threshold). The test chip is sent to fabrication and hence the results mentioned below are post-layout simulation results. Since the proposed TDC is designed using capacitive boosting buffers, the minimum V_{DD} required for the TDC is only 0.6 V. The proposed CB- VDL TDC operates at a sampling frequency (F_S) of 50 MHz, consume a power of 217.43 μ W and achieves a time resolution of 1.74 ps. The layout of the TDC that includes the I/O pad-ring is shown in Figure 4.5 and the TDC consumes an active area of 1.225 mm² which also includes the on-chip delay line calibration circuitry. The overall TDC core chip dimensions are 1276 μ m x 960 μ m. In order to generate an input time difference ramp that is increasing, for measuring the performance of the TDC, two clock signals START and STOP with a minor variation in running frequency id used. The resolution of the time ramp is formed by the difference in frequencies [89]. The START and STOP signals utilises a base time period of 20 ns or frequency of 50 MHz.

Figure 4.5 – Proposed TDC chip layout with pad-ring

The proposed TDC exhibits a LSB resolution of 1.74 ps and a measurement range of 6-bits. The layout mismatches, cross talks and PVT variations translate as TDC integral and differential non-linearity (INL and DNL). The proposed TDC shows a maximum INL of 1.45 LSB and DNL of 1.31 LSB as plotted in Figure 4.7 and Figure 4.8. The TDC figure-of-merit (FoM) is calculated using (4.1) [90], and the proposed TDC has a figure-of-merit of 166 fJ / conversion step.

$$FoM = Power / (2^{N_{linear}} . F_S) \quad (4.1)$$

Where N_{linear} (effective number of linear bits) = $Total\ bits - \log_2 (INL+1)$

Figure 4.6 – Input time versus output digital code of proposed TDC

Figure 4.7 – INL of proposed TDC

Figure 4.8 – DNL of proposed TDC

Figure 4.9 – Monte-carlo simulation results of proposed TDC

Figure 4.9 shows the monte-carlo simulations results of the proposed TDC with process variations and mismatch. Single shot precision (SSP) experiment is employed for the monte-carlo simulations. The proposed TDC achieves an SSP of 1.76 ps to 2.24 ps for different input time intervals (T_{in}) which demonstrates

its robustness against process variations and mismatches. From Table 4.2, it can be seen that the proposed CB-VDL TDC attains low power consumption and good resolution when compared with other TDC architectures. The proposed TDC can work at a low V_{DD} of 0.6 V even when designed using 1.8 V transistors (standard threshold) available in the 180 nm CMOS process. Since the chip is currently under fabrication, the results presented below are post-layout simulation results.

Table 4.2 – Performance metrics comparison of recent TDCs

TDC	Proposed^a [27]	[91]	[62]	[90]	[92]	[93] ^b
TDC type	Cap Boost VDL	Time Amp	Stoch	Pipeline	Cyclic	Time Amp
Tech Node	180 nm	65 nm	14 nm	65 nm	0.35 μ m	180 nm
V_{DD} (V)	0.6	1.2	0.6	1.2	3.3	1.2
Power (mW)	0.217	2	0.78	15.4	80	1.1
Range (bits)	6	8	10	9	13	8
Resolution (ps)	1.74	2.6	1.17	1.12	0.61	5.3
INL (LSB)	1.45	2.36	2.3	1.7	7.38	2.8
F_s (MHz)	50	80	100	250	0.8	30
FOM (pJ/con.step)	0.166	0.328	0.025	0.325	102.3	0.54
Area (mm ²)	1.225 ^c	0.07	0.036	0.14	0.61 ^d	0.05

^a Post layout simulated results – chip currently in fabrication

^b Post layout simulation results

^c Calibration – on-chip

^d Calibration – of-chip

Table 4.3 shows the performance comparison of the proposed TDC between the pre-layout simulations results and post-layout simulation results.

Table 4.3 – Performance of proposed TDC

Proposed TDC	Pre-layout	Post-layout
Power (mW)	0.181	0.217
INL	1.26	1.45
FOM (pJ/conv.step)	0.127	0.166

4.3 Summary and Discussions

A novel low supply voltage TDC is designed and fabricated in 180 nm / 1.8 V CMOS process. The proposed TDC is designed using capacitive boosting differential buffer based vernier delay lines. It exhibits a dynamic measurement range of 6 bits and can work at a low V_{DD} of 0.6 V even when designed using 1.8 V transistors (standard threshold) available in CMOS 180 nm technology. The TDC design consumes a core area of 1.225 mm² and this also includes the on-chip calibration circuitry also. The TDC attains a fine time resolution of 1.74 ps. At a sampling rate of 50 MS/s, the TDC consumes a power of 217.43 μ W and exhibits a *FoM* of 166 fJ / conv.step.

Even though, the prototype TDC has been designed based on the vernier delay line principle, the proposed technique of using capacitive boosting for designing TDCs can be extended to a wide range of TDC architectures making it an attractive method for designing ultra-low V_{DD} TDCs. Since, the proposed TDC can operate at 0.6 V, the proposed technique can be extended to design various

TDC architectures in short channel CMOS technologies for further reducing the required silicon area, operating supply voltage and power consumption, thus making the proposed TDC design technique ideally attractive for use in biosensor time-of-flight measurements applications.

Chapter 5

TDC-Less ADPLL

This section proposes and discusses a TDC-less MedRadio ADPLL which uses fractional capacitor tuning, shunt capacitor tuning, frequency controller mechanism and capacitive boosting differential ring oscillator system for accomplishing good jitter performance capabilities, low area and low power consumption at an operating V_{DD} of 0.68 V in 40 nm CMOS [28][29].

5.1 Proposed Biomedical Implant ADPLL

5.1.1 Top Level System Architecture

The block-level architecture of the proposed MedRadio ADPLL is shown in Figure 5.1. It comprises of circuit blocks such as frequency controller, DCO system consisting of tuning block and capacitive boosting differential ring oscillator, phase frequency detector (PFD) and programmable frequency divider. The ADPLL DCO system contains a coarse and fine tuning block. The proposed ADPLL system works as explained below. The difference in phase and frequency between the *REF* reference and the *DIV* divided output signals is detected by the PFD to provide the phase error signal *DN and UP*. The frequency controller block uses these phase error signals to produce a fine oscillator tuning word *FTW* and coarse oscillator tuning word *CTW*. These tuning words control the DCO and tunes it to obtain the desired *CLK* frequency. The ADPLL output frequency is programmed using frequency divider block to

attain the desired reference frequency multiplication factor N . While previously reported ADPLL topologies use a digital loop filter, the proposed ADPLL uses a proposed frequency controller to attain good miniaturization and low power consumption that is required for medical implant devices and applications. The operation and overview of all other ADPLL sub-blocks are explained below,

Figure 5.1 – Proposed biomedical implant ADPLL [28][29]

5.1.2 Phase Frequency Detector

Two true-single-phase clock D-flip-flops (TSPC-DFF) and fundamental logic gates are used to build the ADPLL's PFD [94] as shown in Figure 5.2. The TSPC D-flip-flop circuit diagram is illustrated in Figure 5.3 and in Table 5.1 the transistor size of the flip-flops are shown. The PFD senses phase errors between the output signal and reference signal for producing the phase error signals DN and UP which are used as control signals of frequency controller. When the frequency of DCO lags, the signal DN is produced as shown in Figure 5.4, and when the frequency of DCO leads the reference frequency, the

UP signal is produced. This type of PFD uses less transistors, quickly secures a lock-in for the PLL, demonstrates a low propagation delay and power, all of which are necessary for medical implants. Also, they provide better jitter performance and are not susceptible to duty cycles [95][89].

Figure 5.2 – Phase frequency detector

Figure 5.3 – TSPC D-flip-flop

Table 5.1 –TSPC D-flip-flop transistor sizes

Device	W (μm) / L (nm)
N1	0.2 / 40
P3	0.9 / 40
P1-P2	1.1 / 40
N2-N3	0.4 / 40

Figure 5.4 – Simulation waveform of PFD operation

5.1.3 Capacitively Boosted Differential Ring Oscillator

The proposed ADPLL's DCO system is built using 8-stage capacitive boosting differential ring oscillator, fine and coarse tuning block. The proposed capacitive boosting differential buffer which is used to construct the DCO ring oscillator is shown in Figure 5.5 and its operation is described previously in Chapter 4 . It utilizes four C1-C4 MOM capacitors for capacitively boosting the output signal swing from $-\beta \cdot V_{DD}$ to $+\beta \cdot 2V_{DD}$ [86] [87], where β is the boosting efficiency, which is given by the expression $Cap_C / (Cap_C + C_{parasitic})$. Since the nodes GN1, GN2, VD1 and VD2 has parasitic capacitance associated with it, β which is the boosting efficiency is always < 1 . The body connection of all the NMOS transistors used in the design is connected to *GND* and body connection of all the PMOS transistor used in the design is connected to V_{DD} , except for the PMOS devices whose body connection is shown which is done to avoid the parasitic junction diodes from forward biasing. The transistor and capacitor sizes utilized to design the capacitive boosting buffer is shown in Table 5.2.

Table 5.2 – Device size of capacitive boosting differential buffer

Device	W (μm) / L (nm)	Device	Capacitance (fF)
P1-P2	1.2 / 40	C1-C4	50
PP1-PP2	0.4 / 40	W (μm) / L (nm) - transistors of INV1-INV4, PMOS: 1.1 / 40 NMOS: 0.4 / 40	
LN1-LN2	0.3 / 40		
LP1-LP2	0.9 / 40		
PN1-PN2	0.2 / 40		
N1-N2	0.45 / 40

Figure 5.5 – Proposed capacitive boosting differential buffer

Since there are P1-N1 and P2-N2 inverter pairs in the proposed capacitive boosting differential buffer, the inverter's drain current expression I_D can estimate the inverter propagation delay. The NMOS drain current for an inverter is given by,

$$I_{D,INV} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (5.1)$$

where, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_{TH} is the threshold voltage, C_{ox} is the gate oxide capacitance, μ_n is the mobility of electrons, W is the transistor width and L is the transistor length.

When the input signal to the proposed capacitive boosting differential buffer is high, the V_{GS} of NMOS will be $+ \beta.2V_{DD}$ and the V_{DS} will be the V_{OUT} of the inverter. Hence the inverter's drain current (5.1) can be modified for the capacitive boosting inverter as $I_{D,CB\ INV}$,

$$I_{D,CB\ INV} = \mu_n C_{ox} \frac{W}{L} \left[(\beta.2V_{DD} - V_{TH})V_{OUT} - \frac{1}{2}V_{OUT}^2 \right] \quad (5.2)$$

The inverter's propagation delay is determined by [96]

$$t_{PHL,INV} = \frac{C_{LOAD} \frac{V_{DD}}{2}}{I_{D,INV}} \quad (5.3)$$

By substituting (5.2) in (5.3), capacitively boosted inverter's propagation delay $t_{PHL,CB\ INV}$ can be obtained as below, where C_{LOAD} is the load capacitance.

$$t_{PHL,CB\ INV} = \frac{C_{LOAD} \frac{V_{DD}}{2}}{\mu_n C_{ox} \frac{W}{L} \left[(\beta.2V_{DD} - V_{TH})V_{OUT} - \frac{1}{2}V_{OUT}^2 \right]} \quad (5.4)$$

For a single stage capacitively boosted inverter, its average propagation delay can be represented as,

$$t_{P,CB\ INV} = \frac{t_{PHL,CB\ INV} + t_{PLH,CB\ INV}}{2} \quad (5.5)$$

Capacitive boosting differential buffers are used to construct the proposed ADPLL's differential ring oscillator (8-stage) as presented in Figure 5.6. The buffer's capacitive boosting function is indicated by a double headed arrow. The simulation waveforms of a single stage capacitive boosting differential cell running at 500 MHz while functioning at a V_{DD} of 0.68 V is shown in Figure 5.7.

The DCO ring oscillator's capacitive boosting functionality while providing a output frequency of 450 MHz and working at a supply of 0.68 V is illustrated in Figure 5.8.

Figure 5.6 – Capacitive boosting differential ring oscillator

With above discussions, the running frequency of the 8-stage differential ring oscillator shown in Figure 5.6 can be obtained from the propagation delay expression (5.4) and (5.5). The capacitive boosting differential ring oscillator's frequency is given by,

$$F_{CB\ RO} = \frac{1}{N \cdot (t_{PHL,CB\ INV} + t_{PLH,CB\ INV})} \quad (5.6)$$

where the number of stages is denoted by N .

Figure 5.7 – IO signals of capacitively boosted differential buffer

Figure 5.8 – Waveform of capacitively boosted differential RO

5.1.4 Tuning Block of DCO

The DCO tuning system of the ADPLL contains 2 sub-systems which are the fine and coarse tuning block. The coarse tuning word (*CTW*) and fine tuning word (*FTW*) controls the tuning blocks of the DCO, where the control words are produced by the frequency controller. The DCO coarse tuning sub-system architecture is shown in Figure 5.9. The coarse tuning block is constructed using a 14-bit shunted-NMOS capacitor array. The MOS capacitor array is connected at both the *OUT+* and *OUT-* terminals of each capacitive boosting differential buffer as its load. The control word *CTW* which is produced by the frequency controller switches the control pins $CTW_0 - CTW_{13}$ to control the coarse tuning bank. The ring oscillator frequency is increased or decreased coarsely by the *CTW* word, which depends on the number of 0's and 1's available in the *CTW* word. The oscillator frequency will reduce if more '1' is available on the *CTW* word, due to which more NMOS transistors will be switched on. The oscillator frequency will increase if more '0' is available on the *CTW* word, due to which more NMOS transistors will be switched off.

Figure 5.9 – Coarse tuning block using shunt-MOS capacitor array

To attain good jitter performance capability for the ADPLL without utilizing a TDC, the DCO of the ADPLL must have ultra-fine frequency tuning capability for reducing quantization noise of DCO. The minimum capacitance achievable by using the smallest MOM capacitor present in the 40 nm process is not enough to realize DCO tuning with high resolution. Hence, the DCO fine frequency tuning system of the proposed ADPLL uses a capacitor bank with fractional MOM capacitors [97][98]. The DCO fine tuning block architecture is presented in Figure 5.10. It contains an 8-bit fractional MOM capacitor bank loaded between the $OUT+$ and $OUT-$ terminals of each capacitive boosting differential buffer. The FTW control word which is produced by the frequency controller switches the control pins $FTW_0 - FTW_7$ to achieve fine tuning. The equivalent circuit when FTW_n is logic '0' and logic '1' is used to derive the capacitance step accomplished for an single fractional capacitor cell [98].

From the *FTW* switching, the realized capacitance step ΔC is approximated by,

$$\Delta C = \frac{1}{2} \frac{C^2}{C + 2C_{Fn}} \quad (5.7)$$

A minimum available capacitance C in the used 40 nm process and a larger C_{Fn} capacitor is utilized to achieve fractional capacitance [97][98]. Thus in order to obtain a fine capacitance step that tunes the DCO finely, a larger C_{Fn} is utilized.

Figure 5.10 – Fine tuning block using fractional capacitor array

5.1.5 Frequency Controller of ADPLL

The proposed ADPLL frequency controller system has 4 sub-systems in it which are the coarse and fine register, frequency error generator and register clock generator as shown in Figure 5.11. The signals *REF* and *DIV* are compared by the frequency error generator to produce an output error signal *FE*. The phase lock status of the ADPLL is indicated by this error signal. The register clock generator produces a register clock signal *CK* by using the *FE* signal and PFD outputs.

The *CK* signal is utilized by the fine and coarse registers for issuing the fine and coarse tuning words to the DCO tuning block for changing the output frequency.

Figure 5.11 – Frequency controller

The coarse and fine register is built using the register unit cell illustrated in Figure 5.12. Basic logic gates and D-flip-flop are used to build the register unit cell. The coarse register is built using 14 register unit cells and the fine register is built using 8 register unit cells. The phase frequency detector provides the signals *DN* and *UP*. The output from previous register's unit cell is connected to the signal *PS* and the output of next register's unit cell is connected to the signal *NS*.

When the ADPLL output signal is running faster than required, the PFD produces a high *UP*. This enables the register to generate more logic 1's to reduce the ADPLL output frequency by turning on more NMOS transistors in the tuning block. When the ADPLL output signal is running slower than required, the PFD produces a high *DN*. This enables the register to generate more logic 0's to increase the ADPLL output frequency by turning off more NMOS transistors in the tuning block.

Figure 5.12 – Register unit cell

The *FE* error signal drops to low or '0' when the required ADPLL frequency multiplication is attained, as shown in Figure 5.13 and this disables the register clock generator, making the register to store and hold the fine and coarse tuning word so that the words do not change after desired frequency locking is achieved. From Figure 5.13, it can be observed that the error signal *FE* drops to '0' when frequency locking is achieved and output frequency becomes stable.

The ADPLL simulation waveforms across different temperatures for a frequency selection of 401 MHz and while functioning at a supply of 0.68 V is presented in Figure 5.14. It can be observed that the proposed ADPLL operates robustly across temperatures. The ADPLL simulation waveforms across various process corners for a frequency selection of 401 MHz and while functioning at a supply of 0.68 V is presented in Figure 5.15. It can be observed that the proposed ADPLL operation is robust across process corners namely slow-fast (SF), fast-slow (FS), slow-slow (SS), fast-fast (FF) and typical-typical (TT).

Figure 5.13 – Transient simulation of proposed ADPLL

Figure 5.14 – Proposed ADPLL transient simulation across different temperatures

Figure 5.15 – Transient simulation across different process corners

The ADPLL frequency divider aids to multiply the reference frequency to the desired output frequency. It divides the output signal frequency which is then used by the PFD to perform a comparison with reference frequency and for producing the phase error signals *DN* and *UP*. The frequency controller system also uses this divided signal to compare with the reference signal to produce the frequency error signal *FE*. Divide-by-2/3 cells are used to build a 3-bit frequency divider block, to accomplish a balance between performance, power and area consumption of ADPLL. D-flip-flops and logic gates are used to build the divide-by-2/3 cell as shown in Figure 5.16. Based on the division control signal *DC*, the cell divides the *CLK* frequency by either 2 or 3. The input and output of DFF1 becomes '0', when *DC* is '1'. The inverted output of DFF2 becomes the input of DFF2 which enables the DFF2 to be reconfigured as a divide-by-2 cell. Hence divide-by-2 operation of the *CLK* signal is achieved by the whole divide-by-2/3 cell. The outputs of both the FF change at the *CLK* rising edge, when *DC* is '0', and divide-by-3 operation on *CLK* signal is performed by the entire divide-by-2/3 cell.

5.2 Measurement Results

The proposed ADPLL is designed and fabricated in 40 nm / 1.1 V CMOS process. The minimum V_{DD} needed for the ADPLL to operate is reduced to 0.68 V using the proposed capacitive boosting differential buffers. The ADPLL has a power consumption of 248.62 μ W when running at 401 MHz. The ADPLL provides an output tuning range of 330 MHz – 470 MHz and covers the entire MedRadio frequency band. The chip layout and microphotograph of the ADPLL is shown in Figure 5.17. The chip layout consists of decoupling capacitor and dummy filling and pad-ring.

Figure 5.17 – Chip layout and microphotograph of proposed ADPLL

The chip pad-ring comprises of analog I/O pads which works at a V_{DD} of 2.5 V and the ADPLL core functions at a V_{DD} of 0.68 V. Therefore, the test chip inputs and outputs should be able to drive the 2.5 V analog I/O pads. Hence multi-stage inverter buffers are placed inside the chip to deliver the ADPLL core's input and output signals. The analog I/O pad is also driven after the ADPLL output is level shifted to 2.5 V.

Since the proposed ADPLL uses fractional capacitor tuning bank, frequency controller and capacitive boosting differential ring oscillator in place of a TDC, digital low pass filter and LC oscillator respectively, it consumes an active core area of 0.0186 mm² only. The ADPLL dimensions are 140 μ m x 133 μ m, making it highly desirable for integrating into medical implant SoCs. The proposed ADPLL is easily portable from one process to other since it is constructed using logic gates and flip-flops except the ring oscillator DCO system, which also saves redesigning time. A FR4 PCB board is designed for measuring the performance of the ADPLL chip using a Loranger socket. The reference frequency of the ADPLL is inputted through a Keysight 33600A Series waveform generator. The ADPLL output waveforms and jitter is observed through the Agilent DSO91304A oscilloscope and the DC current consumption is measured through a Keysight 34461A digit multimeter.

Figure 5.18, Figure 5.19 and Figure 5.20 shows the measured ADPLL output waveforms while operating at 330 MHz, 401 MHz and 470 MHz respectively. The ADPLL jitter performance is shown in Figure 5.21 and it can be observed that the ADPLL demonstrates an 11.88 ps rms jitter and 95.56 ps peak-to-peak jitter while running at a frequency of 401 MHz. Since the ADPLL output is buffered to drive the 50 Ω coaxial cable and analog I/O pads for performing measurements, the measured jitter possess jitter from I/O pads and buffers also. But, when used inside a SoC, the ADPLL will not be driving a 50 Ω line and therefore, the ADPLL jitter will be lower than the measurement results provided here.

Figure 5.18 – Measured ADPLL output at 330 MHz

Figure 5.19 – Measured ADPLL output at 401 MHz

Figure 5.20 - Measured ADPLL output at 470 MHz

Figure 5.21 – Measured ADPLL jitter at 401 MHz

The ADPLL spectrum and phase noise is measured using an R&S signal analyzer. The measured ADPLL spectrum and phase noise graphs are shown in Figure 5.22 and Figure 5.23. The reference frequency provided to the ADPLL is 17.45 MHz. The maximum power exhibited by the measured reference spur tone is -40.76 dBc. The measured ADPLL phase noise when running at 401 MHz at 1-MHz frequency offset is -98.76 dBc/Hz and at 10-MHz frequency offset is -111.26 dBc/Hz. The phase noise contribution from different sub-blocks of the ADPLL is simulated as shown in Figure 5.24. The loop bandwidth selected was 100 KHz since the MedRadio frequency band has a phase noise requirement of -70 dBc/Hz at 200-KHz frequency offset [99]. The PFD contributes most noise at lower frequency offsets and the DCO contributes most noise at higher frequency offsets. An Agilent 11612VK68 bias tee is used to inject a peak-to-peak sinusoidal signal of 50 mV amplitude into the supply for measuring the ADPLL performance under supply noise. Figure 5.25 shows the ADPLL jitter versus supply noise frequency.

Figure 5.22 – Measured ADPLL spectrum at 401 MHz

Figure 5.23 – Measured ADPLL phase noise at 401 MHz

Figure 5.24 – Simulated phase noise contribution of ADPLL sub-blocks

Figure 5.25 – Measured ADPLL jitter versus supply noise frequency

The below mentioned figure-of-merits (*FOM*) [100] are used to benchmark the performance specifications of the proposed ADPLL design when compared with existing medical implant MedRadio and low power PLL architectures,

$$FOM_{area} = \frac{area (mm^2) \times 1(\mu m^2)}{(channel length^2)(\mu m^2) \times 1(mm^2)} \quad (5.8)$$

$$FOM_{power} = \frac{power (\mu W)}{Frequency (MHz)} \text{ energy per cycle} \quad (5.9)$$

$$FOM_{pn} = L\{\Delta f\} - 20 \log\left(\frac{f_o}{\Delta f}\right) + 10 \log\left(\frac{P_{diss}}{1 mW}\right) \quad (5.10)$$

where $L\{\Delta f\}$ is phase noise, P_{diss} is the power dissipation, f_o is center frequency and Δf is certain frequency offset.

From Table 5.4 it can be seen that the proposed ADPLL attains good performance at a very low silicon area, on comparison with existing medical implant MedRadio and low power PLL designs. On comparison with ADPLL architectures presented in [24] and [68] which uses both TDC and LC oscillator in 40 nm CMOS, the proposed ADPLL design accomplishes a silicon area reduction of 15 times and 10 times respectively. Even though by using LC oscillators, the other reported PLLs attain good phase noise performance, their larger area consumption outweighs the benefit of having good FOM_{pn} metrics. For biomedical implant applications, the phase noise requirements of the MedRadio frequency band is not stringent and hence consuming low power and low silicon area is more important.

Since the chip was not designed accordingly to measure the power consumption of the individual sub-blocks, the average power consumption of sub-blocks from post-layout simulation is provided below in Table 5.3. The DCO consumes the most power of the overall ADPLL.

Table 5.3 – Power consumption of ADPLL sub-blocks

Sub-block	Power (μ W)
PFD	0.62
Frequency Controller	19.38
Frequency Divider	44.17
DCO	193.52

Table 5.4 – Comparison of medical implant and low power PLL designs

PLL	Prop [28][29]	[73]	[99]	[25]	[71]	[24]	[68]	[101]
Process (nm)	40	90	65	130	130	40	40	65
PLL	ADPLL	ADPLL	Analog	Analog	ADPLL	ADPLL	ADPLL	ADPLL
TDC Present	No	Yes	No	No	No	Yes	Yes	Yes
DCO	Ring	Ring	LC	Ring	LC	LC	LC	Ring
V_{DD} (V)	0.68	1	1	0.5	0.7	1	1	1
Power (μ W)	248.62	920	430	440	840	852	860	2400
Freq (MHz)	330 – 470	60 – 600	400 – 405	400 – 433	382 – 412	315 – 450	2100 – 2700	1300 - 2650
RMS Jitter (ps)	11.88	13.7	NA	5.5	NA	NA	1.71	12
PN (dBc/Hz) @ Offset	-98.76 @ 1-MHz	NA	-102.1 @ 200-KHz	-91.5 @ 1-MHz	-114 @ 200-KHz	NA	-109 @ 1-MHz	-105 @ 3.5-MHz
Ref.Spur (dBc)	-40.76	NA	-45	-38.3	NA	NA	-70	-59.8
Area (mm ²)	0.0186	0.065	0.54	0.0736	0.64	0.28	0.2	0.12
FOM_{area}	11.62	8.02	127.81	4.35	37.86	175	125	28.4
FOM_{power} (pJ)	0.620	1.53	1.07	1.015	2.07	1.89	0.409	0.90
FOM_{pn}	-156.86	NA	-171.9	-147.8	-181.4	NA	-177.4	-148.1

5.3 Summary and Discussions

An ultra-low silicon area TDC-less ADPLL for medical implant transceivers is proposed, designed and fabricated in CMOS 40 nm process. The ADPLL has a frequency tuning range that covers MedRadio frequency band. Instead of using a LC oscillator, the proposed ADPLL uses capacitive boosting differential ring oscillator DCO to minimize chip area consumption. The functionality of the digital loop filter is achieved by a frequency controller block. Instead of using a TDC, fractional capacitor tuning is utilized to achieve DCO fine frequency tuning for reducing power and silicon area. The ADPLL provides a frequency tuning range of 330 MHz – 470 MHz, exhibits a power consumption of 248.62 μ W at 0.68 V, and demonstrates 11.88 ps rms jitter and -98.76 dBc/Hz phase noise at 1-MHz offset when generating a frequency of 401 MHz. The ADPLL design consumes a core area of 0.0186 mm² only. The proposed ADPLL can be easily redesigned in other CMOS technology nodes ensuring higher degree of portability, accomplishes a balanced performance in terms of silicon area, jitter, phase noise and power consumption, thus making it very attractive for usage in medical implant SoCs and applications.

Chapter 6

Negative Skewed Ring Oscillators

This section discusses and analyses the negative skewed ring oscillator (NSRO) to bridge the gap of the discrepancy found in the original analysis. The section proposes and validates a time-domain approach that is able to determine the optimum oscillation behavior of an NSRO. This time-domain approach uses a proposed graph termed as the sequence tree and the proposed approach is able to more accurately account for the frequency increment. As compared to the small signal analysis, the proposed approach is more efficient and explains the mechanism of the NSRO propagating edges that causes the increase of frequency. The scheme has also been extended to differential ring oscillators and the impact of negative skewed delay scheme to phase noise is also briefly investigated [30][102].

6.1 Original Analysis and Discrepancy

The oscillation frequency f_c of a conventional ring oscillator can be obtained by using the following equation,

$$f_c = \frac{1}{N(t_{HL} + t_{LH})} \quad (6.1)$$

where N is the total number of stages in the ring oscillator, t_{HL} and t_{LH} are the 100% to 50% high-to-low and 0% to 50% low-to-high edge transition times [103].

The total number of stages present in the smaller loop of the NSRO is defined as L . Hence a negative skew of 2 inverter stages is given as, $L = N - 2$ and moreover, the negative skew is applied to the PMOS transistor. The circuit schematic of an $N = 11$, $L = 9$ NSRO is shown in Figure 6.1. The simulation waveforms of the NSRO and a conventional ring oscillator (i.e. $N = 11$, $L = 11$) is shown in Figure 6.2. The oscillation frequency and edge transition times of the NSRO is given by f_s , t_{HLS} and t_{LHS} . Other NSRO configuration examples such as of $N = 5$, $L = 3$ and $N = 10$, $L = 3$ NSROs can be seen in [81].

Figure 6.1 – Circuit of $N = 11$, $L = 9$ NSRO

Figure 6.2 – Simulation waveforms of conventional RO and NSRO

From Figure 6.2 it can be seen that the f_s of NSRO is 89% faster than the conventional RO. As discussed previously in 2.5, it is originally explained that is the reduction of short circuit current during the high-to-low transition and compensation of a normally weaker PMOS in the low-to-high transition the causes the increase in f_s [81]. While the analysis for the high-to-low transition is reasonable, the counterpart for the low-to-high transition is debatable. If the same analysis from the high-to-low transition is applied to the low-to-high transition, such that the PMOS turns on prematurely before the NMOS turns off, there will be an increase in short circuit current and t_{LHS} should increase. From simulations it can be seen that both t_{LHS} and t_{HLS} are increased by 28.7% and 15.6% respectively, as compared to the conventional RO. The increase in both t_{LHS} and t_{HLS} is due to other higher order effects such as the mutual dependency of t_{LHS} and t_{HLS} . The larger t_{LHS}/t_{HLS} ratio of 1.14 ($N = 11, L = 9$) as compared to t_{LH}/t_{HL} ratio of 1.02 ($N = L = 11$) is in line with the above discussion. When t_{HLS} and t_{LHS} are applied to (6.1), it predicts that f_s should decrease by 18.2%. Instead, simulation results shows that f_s has increased by 89% and therefore there is a large error of 107.2% which proves that the original analysis [81] does not adequately explain the f_s frequency improvement of NSRO.

6.2 Proposed Analysis

A time-domain approach is proposed in this section to characterize the optimum oscillation behaviour of NSRO. It is desirable to have the NSRO outputs to be spaced evenly apart with a phase difference of $2\pi/N$ for multi-phase outputs operation. Hence, the optimum oscillation operation or oscillation mode is defined as the case where this condition is satisfied, while achieving largest f_s .

In an NSRO, the inputs to its NMOS and PMOS transistors are decoupled and since the output of each stage is connected to two different following stages, a transition at one stage will cause two different stages to respond, i.e. due to the NMOS in one stage and the PMOS in the other as shown in Figure 6.1. The truth table of a negative skewed delay stage is described by Table 6.1. For State 2 and State 3, the stage output will be in a high impedance and contention state respectively. These states inhibit an oscillating edge from propagating. Hence, the delay stage does not stay in State 2 or State 3 for a long period of time during optimum oscillation operation and it will rapidly change to State 1 or State 4.

This behaviour enables the largest f_s and during optimum operation, the stage output will always be high or low except during transition, meaning that State 2 and State 3 can be interpreted as storing the previous output and the start of a transition respectively. Therefore, during optimum operation, the NSRO at any point in time can be described by the following set of pseudo-digital relationships.

$$V_{o,i}(t) = \bar{V}_n \bar{V}_p + \bar{V}_n V_p V_{o,i}(t), \text{ for } i = 1 \text{ to } N \quad (6.2)$$

$$\text{Transition} = V_n \bar{V}_p, \text{ for } i = 1 \text{ to } N \quad (6.3)$$

Table 6.1 – Truth table of negative skewed delay stage

State	V_n	V_p	General V_o	Optimum V_o
1	0	0	1	1
2	0	1	Z	V_o
3	1	0	$\approx V_{DD}/2$	$V_o \rightarrow \overline{V_o}$
4	1	1	0	0

where each stage is defined by its output node and indexed by i , $V_n = V_{o,i-1}(t)$ and $V_p = V_{o,i-(N-L)-1}(t)$. The looping effect of ring oscillators can be accounted for by adding or subtracting N to i whenever $i \leq 0$ or $i > N$, ensuring that $1 \leq i \leq N$. Note that this looping effect will be applied throughout the rest of the chapter even if it is not stated explicitly. The t parameter shows that all N stages of the NSRO continuously interact with one another through events of rising and falling edges to satisfy the equations in (6.2) and (6.3) simultaneously. In other words, the NSRO is a complicated dynamic system where its stages are inter-related. In addition, there are also multiple solutions to (6.2) and (6.3). Hence, it is possible for the NSRO to have multiple modes of oscillation at steady state. The chosen mode at steady state depends on the NSRO configuration (N & L) and initial conditions applied. For the rest of the chapter, the stages will be referred to by their indexes, e.g. Stage $V_{o,i}$ as Stage i .

Each stage in an NSRO is related to four other stages where two stages are related due to its input connections and the other two stages due to its output connections. In order to see the propagation relationship between all stages in a graphical manner, a sequence tree is proposed as shown in Figure 6.3.

Figure 6.3 – Proposed sequence tree

Every node in the tree represents a stage in the NSRO. The next stage of NMOS and PMOS connections are represented by the left and right branches from a node. Since the negative skew is applied to the PMOS, it can be generalized that from Stage i , its NMOS connection is always at Stage $i+1$, whereas its PMOS connection is always at Stage $i+(N-L)+1$. Since an oscillating edge propagates forward in a ring oscillator, the tracking of the stages is also counted upwards from 1 to N . The looping effect is shown by the brackets in Figure 6.4. In addition, within the same level in the tree and counting upwards in the ring, it can be derived that the difference between a node from its left or right neighbour is $N-L$ or L , as shown in Figure 6.4. Hence, for the sequence tree to form fully without repetition in the same level, L and $N-L$ have to be relatively prime to N . The sequence tree for the example in Figure 6.1 is shown in Figure 6.4. Figure 6.5 shows an example where the sequence tree is unable to form fully when $N=9$, $L=3$.

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Hence, the NSRO supports the propagation of multiple oscillating edges, such that the system of (6.2) and (6.3) can be satisfied with minimum contention conditions in order to achieve an optimum operation. The multiple oscillating edges increase f_s by the factor of the number of oscillating edges. This phenomenon is similar to self-timed ring oscillators and hence (6.1) can be modified as below,

$$f_s = \frac{k}{N(t_{HLS} + t_{LHS})} \quad (6.4)$$

where k is the number of oscillating edges within the NSRO. The derivations of t_{HLS} and t_{LHS} are non-trivial. Hence, as a quick estimation, assuming that the reduction of short circuit current during the high-to-low transition can be approximately compensated by the increase during the low-to-high transition, the original t_{HL} and t_{LH} of a conventional N stages ring oscillator can be used. However, for this work, t_{HLS} and t_{LHS} will be extracted directly from the results.

One way of understanding the presence of multiple oscillating edges is to study an $N = 10, L = 5$ NSRO. The simulated Stage 1 and Stage 6 outputs oscillation waveforms of this NSRO and a conventional $N = L = 5$ ring oscillator are shown in Figure 6.6. It can be observed that they are oscillating with the same frequency and are in-phase. Thus, this NSRO can be viewed as two 5-stage conventional ring oscillators connected in series that produces two oscillating edges within this 10-stage NSRO. These two oscillating edges double f_s and therefore, f_s is not limited by the NSRO unit stage delay.

Figure 6.6 – Simulation waveforms of conventional RO and NSRO

6.2.1 Single Edge Sequence

The multiple oscillating edges have to be differentiated from one another in order to identify the number of oscillating edges k within a configuration of NSRO. Each oscillating edge can be identified by understanding the rising edges phase sequence from a single edge. For the rest of this chapter, one cycle of this repeating rising edges phase sequence of a single edge is defined as the single edge sequence. In a conventional ring oscillator, its single edge sequence (CQ_N) can be expressed as,

$$\{cq_i\}_{i=2}^N = \{cq_{i-1} + 2\}, \quad cq_1 = 1 \quad (6.5)$$

For example, the single edge sequence of a 5-stage conventional ring oscillator is $CQ_5 = \{1, 3, 5, 2, 4\}$. For an NSRO, using the sequence tree shown in Figure 6.3 as a reference, consider a rising edge at Stage i .

This rising edge results in two separate falling edges to occur at Stage $i + 1$ and Stage $i + (N - L) + 1$ as Stage i is connected to the NMOS input of Stage $i + 1$ and the PMOS input of Stage $i + (N - L) + 1$. Then, these two falling edges will converge back and cause the next rising edge to occur at Stage $i + (N - L) + 2$. This convergence occurs as both Stage $i + 1$ and Stage $i + (N - L) + 1$ are connected to the PMOS and NMOS inputs of Stage $i + (N - L) + 2$, respectively. This convergence event is the single edge sequence of NSRO (SQ_N^L). In other words, SQ_N^L can be derived from any straight column in the sequence tree and can be expressed as,

$$\{sq_i\}_{i=2}^N = \{sq_{i-1} + (N - L) + 2\}, \quad sq_1 = 1 \quad (6.6)$$

For example, for an $N = 11$, $L = 5$ NSRO, $SQ_{11}^5 = \{1, 9, 6, \dots\}$. This SQ_{11}^5 can be seen from the sequence tree and the simulated oscillation waveform of this NSRO as depicted in Figure 6.7 and Figure 6.8.

This NSRO supports only a single oscillating edge. For cases involving multiple oscillating edges, they can be categorized into two groups. Namely, when N is odd or even. In the following analyses, only the oscillation behaviours of NSROs operating in the optimum mode are discussed, as only this mode has the smallest tap-to-tap delay.

Figure 6.7 – Sequence tree of $N = 11$, $L = 5$ NSRO

Figure 6.8 – Simulation waveforms of $N = 11$, $L = 5$ NSRO

6.2.2 Total Number of Stage, N is Odd

When N is odd, a phase shift of 2π is provided by two different lengths of loops in the NSRO for sustained oscillation. They are of lengths N and L . The NSROs where N is odd behave as follows in the optimum oscillation mode. Due to the decoupling of the NMOS and PMOS, a rising edge occurring at Stage i will cause a falling edge to first occur at Stage $i + 1$, followed by another at Stage $i + (N - L) + 1$.

For $L = N - 2$, using Stage i as reference for phase 0, these falling edges occur at phase $2\pi/N$ and phase $2(2\pi/N)$, respectively. They are termed the early and late edges, respectively. Then, the single edge sequence rising edge occurs at Stage $i + (N - L) + 2$ at approximately the same phase as the late falling edge (i.e. $\approx 2(2\pi/N)$). These transition events are exemplified by the timing diagram of an $N = 11$, $L = 9$ NSRO shown in Figure 6.9. They are part of single edge sequence A where $i = 3$. The sequence tree shown in Figure 6.4 can be used as a guide to trace these transition events.

Figure 6.9 – Timing diagram of $N = 11$, $L = 9$ NSRO

In order to have stability and uniformity in the symmetrical NSRO, another rising edge should also occur at Stage x with approximately the same phase as the early falling edge. This rising edge originates from an even earlier rising edge at Stage q that occurs before phase 0. In other words, the rising edge at Stage x is another single edge sequence following Stage q .

$$x = q + (N - L) + 2 \quad (6.7)$$

Therefore, the early falling edge due to Stage i is the same late falling edge due to Stage q . Together with (6.7),

$$\begin{aligned} i + 1 &= q + (N - L) + 1 \\ x &= i + 2 \end{aligned} \quad (6.8)$$

This second single edge sequence is shown by sequence B in Figure 6.9. In this example, using (6.7) and (6.8), $x = 5$ and $q = 1$. In fact, using (6.8), it can be shown that the rising edge at Stage $i + (N - L) + 2$ following single edge sequence A has the relationship of $i + (N - L) + 2 = x + 2 = i + 4$. Hence, the overall phase sequence of this NSRO is the same as the conventional case, i.e. 2 stages apart as described by (6.5).

Overall, as shown by Figure 6.9, there are two separate single edge sequences occurring simultaneously, meaning that two separate oscillating edges are propagating in this configuration of NSRO. The two oscillating edges increase f_S by a factor of 2 ($k = 2$). However, the larger contention during the rising edge results in a final frequency increment of less than 2 times. Note that if the analysis starts from a falling edge instead of a rising edge at Stage i , the subsequent rising edges at Stage $i + 1$ and Stage $i + (N - L) + 1$ and the single edge sequence falling edge at Stage $i + (N - L) + 2$ occur at approximately phase 0, phase $2\pi/N$, and phase $2(2\pi/N)$ respectively. The same conclusion can be derived. In addition, if the negative skew is applied to the NMOS instead

of the PMOS, the above analysis is still applicable. In this case, the behaviour of the rising and falling edges is reversed and the contention occurs during the falling edge transition.

For $L = N - 4$, the falling edges at Stage $i + 1$ and Stage $i + (N - L) + 1$ due to a rising edge at Stage i occur at phase $2\pi/N$ and phase $3(2\pi/N)$ respectively. The single edge sequence rising edge at Stage $i + (N - L) + 2$ occurs at approximately the same phase as the late falling edge (i.e. $\approx 3(2\pi/N)$). Similarly, for uniformity and stability, another falling edge should occur at phase $2(2\pi/N)$ and two separate rising edges should occur at phase $2\pi/N$ and phase $2(2\pi/N)$. These two rising edges occur at Stage v and Stage y respectively. All of these transition events are exemplified by the timing diagram of a general odd N , $L = N - 4$ NSRO as shown in Figure 6.10.

Figure 6.10 – Timing diagram of Odd N , $L = N - 4$ NSRO

Using the same analysis as before,

$$v = i + 2 \quad (6.9)$$

$$y = v + 2 \quad (6.10)$$

From (6.9) and (6.10), the overall phase sequence for this configuration of NSRO is also the same as the conventional case as described by (6.5). However, there are three oscillating edges coexisting, i.e. $k = 3$. In this case, there is larger contention during the rising edge transition since it arises from falling edges that have a larger phase difference of $2(2\pi/N)$. Hence, the final increase in frequency is much lesser than 3 times.

For smaller values of L , such as the example in Figure 6.7 there are only one oscillating edge within these NSROs. Hence, these configurations are undesirable. In contrast to [81], the optimum skew for largest f_s is $L = N - 4$. However, it will be shown later that the power-delay product (PDP) for $L = N - 2$ cases are lower than that for $L = N - 4$ cases.

6.2.3 Total Number of Stage, N is Even

When N is even, only the loop of length L provides the required phase shift of 2π to sustain oscillation. For these NSROs, there is only one optimum L configuration for each length of N that achieves the optimum operation. In optimum operation, following the single edge sequence, a rising edge at Stage i causes an early and a late falling edge to occur at phase $2\pi/N$ and phase $2(2\pi/N)$ respectively. After which, the single edge sequence rising edge at

Stage $i + (N - L) + 2$ occurs at phase $3(2\pi/N)$. Similarly, uniformity and stability of the symmetrical NSRO can be achieved by having two other single edge sequences in the NSRO. Separately, they produce rising edges at Stage w and Stage u that are in phase with the early and late falling edges due to Stage i , i.e. at phase $2\pi/N$ and phase $2(2\pi/N)$ respectively. All of these transition events are also exemplified by the timing diagram of a general even N NSRO as shown in Figure 6.11.

Figure 6.11 – Timing diagram of Even N NSRO

If Stage $i + 1$ and Stage $i + (N - L) + 1$ are the early and late falling edges respectively, Stage w and Stage u can be derived by applying the same analysis as before,

$$w = i + (N - L) \quad (6.11)$$

$$u = i + 2 (N - L) \quad (6.12)$$

In addition, continuing the analysis where the early falling edge due to Stage $i + (N - L) + 2$ is the same late falling edge due to Stage u , the following condition to determine the optimum L for a length of N can be derived,

$$\begin{aligned} i + (N - L) + 3 &= u + (N - L) + 1 \\ (N - L) + 2 &= 3 (N - L) \end{aligned} \quad (6.13)$$

From (6.11) and (6.12), the overall phase sequence (EQ_N^L) for this configuration of NSRO can be described by,

$$\{eq_i\}_{i=2}^N = \{eq_{i-1} + (N - L)\}, \quad eq_1 = 1 \quad (6.14)$$

However, if Stage $i + (N - L) + 1$ and Stage $i + 1$ are the early and late falling edges respectively, another set of relationships for Stage w and Stage u , optimum L condition and EQ_N^L can be derived as shown below,

$$w = i + L \quad (6.15)$$

$$u = i + 2L \quad (6.16)$$

$$2L = 2 (N - L) + 2 \quad (6.17)$$

$$\{eq_i\}_{i=2}^N = \{eq_{i-1} + L\}, \quad eq_1 = 1 \quad (6.18)$$

Do note that the looping effect is applied throughout all of the analysis. Overall, when N is even, optimum oscillation operation can be achieved with integer L chosen such that either (6.13) or (6.17) is satisfied. In such cases, there are three single edge sequences occurring simultaneously in these NSROs, increasing f_s by 3 times (i.e. $k = 3$). The overall phase sequences of these oscillations can be described by (6.14) or (6.18), respectively. The contention between the NMOS and PMOS occurs during the rising edge for the former and during the falling edge for the latter. As compared to when N is odd and $L = N - 4$, the contention is less severe since the phase difference between the early and late edges is smaller at $2\pi/N$. Hence, f_s increment is less degraded from the factor of 3.

Moreover, further inspection of (6.14) and (6.18) reveals that the nodes sequence in level N of the sequence tree is able to predict the overall phase sequence of an NSRO with even N and optimum L . As discussed in 6.2, the differences between a node from its left and right neighbour are $N - L$ and L , respectively. These differences correspond to (6.14) and (6.18) respectively. This relationship also means that the sequence tree must be able to form fully for optimum oscillation operation (i.e. L and $N - L$ relatively prime to N).

As an example, an $N = 10$, $L = 3$ NSRO satisfies (6.17), leading to its overall phase sequence being described by (6.18), i.e. $EQ_{10}^3 = \{1, 4, 7, \dots\}$. EQ_{10}^3 can be seen from the sequence tree and simulated oscillation waveform of this NSRO as depicted in Figure 6.12 and Figure 6.13.

optimum cases where the NSROs have the smallest tap-to-tap delays. Nevertheless, as compared to the small signal analysis using Eigenvalues which is mathematically complex and needs to be repeatedly applied for each configurations of L to find the optimum L , the proposed sequence tree approach is simple and reveals the multiple oscillating edges mechanism. It can also efficiently determine the optimum L and describe the resulting oscillation behaviour.

6.3 Extension to Differential Ring Oscillators

Even though, the analysis so far was focused on single-ended (SE) NSROs, the negative skewed delay scheme can be also extended to differential ring oscillators enabling their oscillation frequencies to be increased without any additional transistors. Two architectures of differential ring oscillators are considered in this work namely built with source-coupled logic (SCL) and with saturated delay (SD) single stages. Their single stage delay elements are shown in Figure 6.14 and Figure 6.15. An example of an $N = 5$, $L = 3$ differential NSRO is shown in Figure 6.16. The analyses in 6.2 can also be extended to SCL differential NSRO. The SCL stage differential input transistors can be treated as the NMOS and PMOS of a SE stage. Hence, similar to the SE case, f_S is increased by the coexistence of multiple oscillating edges. The final oscillation mode at steady state depends on the interactions between the transconductances during transient. However, for SD differential NSRO, its analysis is not straightforward as the cross-coupled feedback PMOS transistors serve as another set of inputs to each stage of the SD differential NSRO.

Figure 6.14 – Source-coupled logic delay stage

Figure 6.15 – Saturated delay type delay stage

Figure 6.16 – Schematic of $N = 5$, $L = 3$ differential NSRO

6.4 Phase Noise Analysis

Phase noise is an important consideration for any oscillator design. However, a full phase noise analysis is non-trivial and is highly dependent on the architecture of the oscillator. Hence, the aim of this section is not to give full phase noise analyses for the 3 architectures of NSROs presented. Instead, the general impact to phase noise due to the application of the negative skewed delay scheme is briefly investigated.

6.4.1 Phase Noise from White Noise Sources

For a general oscillator and hence a conventional ring oscillator, its period τ may be defined as the interval between successive crossings of a reference point by the rising edges of its oscillation. Due to phase noise, $\{\tau\}$ is a set of discrete random variables. Its standard deviation σ_τ is defined as the periodical jitter. Using the general link between jitter and phase noise, assuming that all sources contributing to phase noise arise from white noise only, [103] derives the following general equation. This general equation can be applied to a conventional ring oscillator.

$$\mathcal{L}(f) = \sigma_\tau^2 \frac{f_C^3}{f^2} \quad (6.19)$$

where $\mathcal{L}(f)$ is the power spectral density (PSD) of single-sideband (SSB) phase noise at moderate frequency offsets of f .

When the negative skewed delay scheme is applied using (6.19), the SSB phase noise PSD of an NSRO $\mathcal{L}_S(f)$ will be affected by the changes of f_c to f_s and σ_τ to $\sigma_{\tau S}$, where $\sigma_{\tau S}$ is the periodical jitter of the NSRO. Hence, as compared to $\mathcal{L}(f)$, $\mathcal{L}_S(f)$ will be increased by $(f_s/f_c)^3$. Note that $f_s/f_c < k$. However, the change of σ_τ to $\sigma_{\tau S}$ is not as simple.

Firstly, it is assumed that all white noise sources are uncorrelated. As discussed, there are k oscillating edges propagating within an NSRO. As these oscillating edges propagate through the NSRO, they are independently sped up or slowed down by identical white noise sources in the NSRO. Hence, the k oscillating edges have individual periodical jitter but are identically distributed. A second assumption is made here whereby the periodical jitter of an oscillating edge in an NSRO $\sigma_{\tau e}$ is equal to that of a conventional ring oscillator, i.e. $\sigma_{\tau e} = \sigma_\tau$. In the NSRO, the k oscillating edges are spaced approximately $2\pi/k$ phase apart from each other. In other words, the k oscillating edges will alternatively pass through a stage of the NSRO in repeated sequence.

Using the NSRO in Figure 6.9 as an example, Stage 3 will see edge A, edge B, edge A, edge B and so on. Therefore, the jitter of the rising edges at that stage is an average of the jitters of the k oscillating rising edges. Since these oscillating edges are independent and identically distributed, $\sigma_{\tau S}^2$ will be k times smaller than $\sigma_{\tau e}^2$ ($= \sigma_\tau^2$). However, the second assumption is a poor assumption, i.e. $\sigma_{\tau e} \neq \sigma_\tau$ as the difference between $\sigma_{\tau e}$ and σ_τ is highly dependent on the ring oscillator architecture.

In summary, the phase noise of an NSRO as compared to its conventional ring oscillator will be increased by $(f_s/f_c)^3$, decreased by k due to the averaging effect and affected by the difference between σ_{te} and σ_t .

6.4.2 Phase Noise from Flicker Noise

Considering only flicker noise, the impact to phase noise due to the negative skewed delay scheme can be estimated using the impulse sensitivity function (ISF) analysis [104]. For a ring oscillator, [104] shows that the $1/f^3$ corner frequency of its phase noise spectrum f_{1/f^3} is related to the $1/f$ noise corner $f_{1/f}$ through the following equation,

$$f_{1/f^3} = f_{1/f} \cdot \frac{3}{2\eta N} \cdot \frac{(1-A)^2}{(1-A+A^2)} \quad (6.20)$$

where η is a proportionality constant, $A \equiv f_{LH}'/f_{HL}'$, f_{LH}' and f_{HL}' are the maximum slopes during the rising and falling edges respectively. Hence, from (6.20), the amount of $1/f$ noise upconversion is minimized when the rising and falling edges are perfectly symmetrical [104]. For an NSRO, as discussed, there are more contention during the rising edge and less during the falling edge (or vice versa). In other words, the NSRO transition edges are more asymmetrical as compared to the conventional case. An example of this asymmetry is shown in Figure 6.2. Hence, there will be more upconversion of $1/f$ noise for the NSRO that degrades its close-in phase noise.

6.5 Measurement Results

Both single-ended and differential NSROs with varying N and L configurations are simulated and measured to validate the proposed analysis. The test chip is fabricated in the 180 nm / 1.8 V CMOS technology due to its lower cost. The test chip contains 28 different configurations of NSROs, including conventional cases ($N = L$) for fair comparison. Since the main objective is to validate the proposed analysis, the fabricated NSROs have aggressive startup transistors and larger transistor sizes. Therefore, oscillation frequencies of the fabricated NSROs are generally low. The micrograph of test chip is shown in Figure 6.17.

When N is odd, both cases of $L = N - 2$ and $N - 4$ (i.e. $k = 2$ and 3) are validated. When N is even, optimum L such that $k = 3$ is chosen by satisfying either (6.13) or (6.17). Multiple chips are measured through probing. However, only 1 set of results is presented to avoid cluttering the figures as the measured results are similar across all chips.

Figure 6.17 – NSRO test chip micrograph

For SE NSROs, using the rising (t_{LHS}) and falling (t_{HLS}) edge transition times from simulations together with (6.4), the calculated and simulated f_s are plotted in Figure 6.18 for $N = 7$ to 22. These plots are categorized by N being odd or even and for $k = 2$ or 3. It can be seen from Figure 6.18 that the calculated and simulated f_s are in good agreement. This validates that there are 2 or 3 oscillating edges coexisting within these NSROs. In addition, the phase sequences of these NSROs are as predicted by 6.2.

The multiple oscillating edges are further validated by the measurement results. The measured f_s/f_c are plotted in Figure 6.19 for $N = 9, 10, 13$ and 16. Note that f_c for $N = 10$ and 16 ring oscillators are extrapolated using f_c of $N = 9$ and 13 ring oscillators respectively. It can be seen that the f_s/f_c for N being odd or even are around 1.21–1.69 or 1.96–2.16 respectively. These frequency increments are much lower than the ideal values of $k = 2$ or 3 due to the larger t_{HLS} and t_{LHS} values as compared to the t_{HL} and t_{LH} values. A contributing factor to the increase in edge transition times is the additional routings required to apply the negative skewed delay scheme. These routings add significant parasitic loadings to the NSROs, thus slowing down f_s .

The power-delay products of the fabricated SE NSROs are plotted in Figure 6.20 where the tap-to-tap delays are used for the PDP calculations. From Figure 6.18, Figure 6.19 and Figure 6.20, comparing between odd N configurations, it can be seen that although $L = N - 4$ (i.e. $k = 3$) configurations have lower tap-to-tap delays as compared to $L = N - 2$ (i.e. $k = 2$) configurations, it comes at a trade-off of higher power consumption.

$L = N - 4$ configurations consume more power due to the larger contentions between their NMOS and PMOS as discussed in 6.2.2.

Figure 6.18 – Calculated and simulated f_s of SE NSRO

Figure 6.19 – Measured f_s / f_c of SE NSROs

In addition, comparing between $k = 3$ configurations, it can be seen that even N configurations have higher f_s with lower PDPs as compared to odd N , $L = N - 4$ configurations. The better performance of even N configurations is attributed to their comparatively smaller contentions between their NMOS and PMOS as discussed in 6.2.3. Overall, the results show that even N SE NSROs outperform their odd N counterparts, making them more suitable for multi-phase outputs generation.

Figure 6.20 – Measured PDPs of SE conventional and NSROs

Similarly, the extension of the negative skewed delay scheme to differential ring oscillators is verified by the measurement results. The measured f_s/f_c of differential NSROs are plotted in Figure 6.21 for $N = 11$ to 20. For $N = 11, 12, 14$ and 15, the NSROs are built using source-coupled logic (SCL) stages, whereas $N = 17-20$ NSROs are built using saturated delay (SD) stages. As can be seen, the f_s/f_c for the odd N or even N cases are around 1.35–2.51 or

1.92–2.61 respectively. Similar to the SE cases, the frequency increments are lower than the ideal values of $k = 2$ or 3 due to the larger edge transition times. The additional routing parasitics introduced are also a contributing factor to the larger edge transition times. The phase sequences of these differential NSROs are also as predicted by 6.2, verifying that there are 2 or 3 oscillating edges coexisting within these differential NSROs. The PDPs of differential SD NSROs are plotted in Figure 6.22. The PDPs of differential SCL NSROs are not shown as their power consumption are independent of f_s and L and depend only on N . Hence the PDP trend of differential SCL NSROs will follow their f_s/f_c trend. From Figure 6.21 and Figure 6.22, it can be observed that even N differential NSROs also outperform their odd N counterparts in terms of both f_s and PDP.

Figure 6.21 – Measured f_s / f_c of differential NSROs

Figure 6.22 – Measured PDPs of differential SD type conventional and NSROs

Hence, the extension of the negative skewed delay scheme to differential ring oscillators can enable more than 200% increment in their f_s . Although this increase in frequency is lower as compared to the commonly used multi-path technique, the negative skewed delay scheme does not require any additional transistors. Therefore, fewer active devices mean fewer noise sources in an NSRO, but both techniques still suffer from the same additional routing overhead issue.

A general trend can be observed from the above figures that the longer the length of an NSRO, the least effective the negative skewed delay scheme will be. This trend is due to the larger routing parasitics introduced when N is longer.

The measured phase noise performances of all the fabricated NSROs are tabulated and compared in Table 6.2, Table 6.3 and Table 6.4. For fair comparison, the phase noise performances are compared at the same frequency offsets from the center frequency. Note that in measurement, the outputs of the NSROs are divided-by-32 to reduce the sizes of the output buffers. For differential NSROs, due to the low $f_s/32$ for some of these NSROs, their phase noise are measured at relatively low frequency offsets in order to avoid their 2nd harmonic. Hence, only their close-in phase noise due to the upconversion of flicker noise can be compared. For SE NSROs, the frequency offset of 1MHz is after the $1/f$ corner of their phase noise spectrums. Hence, their phase noise due to white noise sources can be compared.

Table 6.2 – Measured phase noise performance of SE NSRO

N, L	f_s (MHz)	Power (μ W)	PN@100 KHz (dBc/Hz)	PN@1 MHz (dBc/Hz)	FoM @ 1 MHz
9,9	84.91	65.07	-69.80	-91.38	-141.82
9,7	110.72	134.64	-69.39	-92.04	-141.63
9,5	143.67	214.20	-65.55	-92.90	-142.74
10,3	165.14	184.50	-68.88	-91.46	-143.15
13,13	58.68	64.51	-72.35	-90.18	-137.45
13,11	71.06	136.13	-71.78	-90.78	-136.47
13,9	83.72	213.12	-69.94	-91.41	-136.58
16,7	93.30	191.34	-70.00	-92.16	-138.74

Table 6.3 – Measured phase noise performance of differential SCL NSRO

N, L	f_s (MHz)	Power (μ W)	PN@10 KHz (dBc/Hz)	PN@30 KHz (dBc/Hz)	FoM @ 30 KHz
11,11	1.72	19.80	-51.64	-57.30	-109.50
11,9	2.63	19.80	-46.71	-56.64	-112.53
11,7	4.32	19.80	-43.24	-55.87	-116.07
12,12	1.58	21.60	-54.20	-55.47	-106.53
12,5	4.11	21.60	-17.35	-30.59	-89.99
14,14	1.29	25.20	-55.43	-57.86	-106.52
14,11	3.09	25.20	-51.93	-57.31	-113.55
15,15	1.19	27.00	-57.76	-54.98	-102.64
15,13	1.61	27.00	-52.24	-56.19	-106.44
15,11	2.43	27.00	-39.27	-50.28	-104.13

Table 6.4 – Measured phase noise performance of differential SD NSRO

N, L	f_s (MHz)	Power (mW)	PN@10 KHz (dBc/Hz)	PN@100 KHz (dBc/Hz)	FoM @ 100 KHz
17,17	12.85	2.09	-64.66	-82.54	-121.52
17,15	24.84	2.23	-63.90	-79.14	-123.55
17,13	28.35	2.43	-62.30	-77.34	-122.53
18,18	13.32	2.09	-68.04	-83.67	-122.95
18,5	30.38	2.46	-62.12	-74.98	-120.72
19,19	12.75	2.06	-70.27	-83.45	-122.42
19,17	22.37	2.28	-63.94	-80.44	-123.85
19,15	24.26	2.46	-61.76	-78.74	-122.52
20,20	12.18	2.05	-69.95	-83.45	-122.04

20,9	23.41	2.47	-62.48	-77.85	-121.31
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For SE NSROs, their phase noise at 1MHz offset against the number of oscillating edges are plotted in Figure 6.23 using data from Table 6.2. In Figure 6.23, the conventional cases are the references for 0 dBc/Hz. However, since the $N = 10$ and 16 conventional SE ring oscillators do not oscillate, the conventional cases for $N = 9$ and 13 are used as the $N = 10$ and 16 references for 0dBc/Hz respectively. There is a trend where the phase noise due to white noise sources decreases when the negative skewed delay scheme is applied. This trend can be attributed to the lower f_s/f_c values of SE NSROs. From (6.19), this trend also indicates that the periodical jitters of SE NSROs are lower as compared to their conventional cases. Therefore, the negative skewed delay scheme is especially beneficial for applications such as clock generators and TDC where jitter is more important than phase noise performance.

The impact to phase noise due to the upconversion of flicker noise can be observed from the rest of the measured phase noise data. In line with 6.4.2, the phase noise increases when the negative skewed delay scheme is applied. The greater asymmetry between the rising and falling edges causes more upconversion of $1/f$ noise. Similar to Figure 6.23, the phase noise for SE NSROs at 100 KHz offset and differential NSROs at 10 KHz offset against the number of oscillating edges are plotted in Figure 6.24 to illustrate this phase noise increment trend.

Figure 6.23 – Phase noise of SE NSRO at 1-MHz offset versus k

Figure 6.24 – Phase noise of SE and differential NSRO versus k

The phase noise for differential NSROs at 30 KHz and 100 KHz offsets are not plotted to avoid cluttering Figure 6.24. These phase noise also have the increment trend. Note that the asymmetrical rising and falling edges of NSROs can be easily rebalanced through proper sizing of the transistors. Therefore, the amount of $1/f$ noise upconversion can be minimized.

Overall, the measurement results of NSROs with N varying from 9 to 20 validate the proposed analysis, the extension of the negative skewed delay scheme to differential ring oscillators and the impact of this scheme to phase noise.

A performance comparison between negative skewed and other reported multi-path ring oscillators is shown in Table 6.5. Since the oscillation frequencies of the ring oscillators are different, it is difficult to have a fair comparison between the NSRO and other architectures. Nevertheless, it can be observed from the table that the NSRO topology achieves low PDP when compared with other multi-path ring oscillator architectures.

Table 6.5 – Performance comparison

RO	NSRO	[105]	[106]	[107]	[108]
Architecture	NSRO	Multi-path	Multi-path	Multi-path	Multi-path
Process (nm)	180	130	130	180	65
No. of Stages	10	4	4	4	8
Frequency (GHz)	0.165	2.4	2.4	1.92	3.11
Power (mW)	0.184	8.25	7.22	13	3.23
PN (dBc/Hz)	-91.46	-120	-91.7	-102	-95.1
@ Offset	@ 1 MHz	@ 10 MHz	@ 1 MHz	@ 1 MHz	@ 1 MHz
PDP (pJ)	0.11	0.86	0.75	1.75	0.13

6.6 Summary and Discussions

Since the small signal analysis using Eigenvalues is mathematically complex and more time consuming, a time-domain analysis featuring the sequence tree is proposed for the negative skewed delay scheme. The proposed analysis is able to efficiently determine the optimum configuration and optimum oscillation behavior of an arbitrary length NSRO. It shows that the increase in frequency is due to the presence of multiple oscillating edges and the proposed analysis is able to cover the most important optimum cases where the tap-to-tap delays are the smallest for multi-phase outputs generation. The negative skewed delay scheme is also extended to differential ring oscillators and the impact to phase noise due to employing the negative skewed delay scheme is briefly investigated. The phase noise of NSRO depends on the amount of frequency increment, the number of oscillating edges, the periodical jitter of an oscillating edge and the symmetry between the rising and falling edges. Both simulation and measurement results are obtained to verify the above discussions. The results also show that NSROs with even N instead of odd N can be used to achieve higher oscillation frequencies while consuming lower power.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The ultimate goal of this PhD research work is to investigate and design low power circuit blocks for medical implant SoCs which are growing in the recent years due to an increasing incidence of chronic illnesses and growing older population across the world. 4 of the important and widely used circuit blocks were chosen for this research namely the flip-flop standard cell, time-to-digital converter, all-digital phase locked loop and negatively skewed ring oscillator. Extensive literature review of existing circuit architectures of flip-flop, TDC, ADPLL and ring oscillators is done in order to come out with new circuit architectures for these blocks that has superior performance than existing architectures.

The key aspects of the research work done are summarized below,

- Current flip-flops exhibit asymmetrical propagation delay (clock-to-output, C-Q), poor PDP performance, poor drive capability and switching speed at ultra-low V_{DD} . The existing FF architectures are also not able to sample low voltage swing data signals. Thus, a wide-input dynamic range capacitively boosted sense-amplifier flip-flop capable of sampling low swing data signals and operating reliably at 0.16 V is proposed and designed in CMOS 40 nm process. The proposed design achieves the

least power-delay product and clock-to-output propagation delay when compared with other existing state-of-the art SAFF architectures.

- Existing time-to-digital converters operate at a V_{DD} of 1 V and above. Reducing the V_{DD} of TDC leads to non-linearity, poor drive strength and unreliable sampling. Hence, a capacitive boosting TDC architecture is proposed, designed and fabricated in 180 nm CMOS technology. The TDC design has a time resolution of 1.74 ps and can operate at 0.6 V even when designed using 1.8 V transistors (standard threshold) available in the given process development kit (PDK) proving the capability of the proposed technique. The proposed capacitive boosting technique for TDCs is first of its kind and the technique can be extended to design various TDC architectures at a low supply voltage without affecting other performance metrics such as resolution and drive strength. The test chip has been fabricated and currently the chip is undergoing packaging.

- Existing biomedical all-digital phase locked loop architectures consume large silicon area due to the use of LC oscillators and TDC. Hence, a TDC-less ADPLL consuming a silicon area of 0.0186 mm² is proposed, designed and fabricated using CMOS 40 nm. Various design methodologies like fractional capacitor tuning, capacitive boosting ring oscillator, frequency control mechanism is incorporated in the design to achieve a balanced performance in terms of power consumption, silicon area, jitter and phase noise performance. The proposed ADPLL covers

the MedRadio band, operates at 0.68 V and demonstrates an 11.88 ps rms jitter and -98.76 dBc/Hz phase noise at 1-MHz frequency offset.

- Even though, all the existing ring oscillator design techniques increase the oscillation frequency by more than two-fold while generating multi-phase outputs, only the negative skewed delay technique uses the same number of transistors when compared to the conventional ring oscillator. Hence, the negative skewed delay technique is the simplest, adds least noise sources and area overhead which are all attractive metrics for use in medical implant SoCs. However, this technique has been conventionally used only to design single-ended ring oscillators, thus limiting its usability. Moreover, the original analysis proposed in [81] also does not adequately explain the increase in oscillation frequency creating a gap in the understanding of negative skewed delay scheme.

Hence, a sequence tree based time-domain analysis is proposed to determine the optimum oscillation behavior of negatively skewed ring oscillator. The negative skewed technique is also extended to design differential ring oscillators. The impact of the technique to phase noise of ring oscillators is also analyzed. Test chips containing various configurations of ring oscillators (both conventional and negative skewed) is designed and fabricated in CMOS 180 nm and the proposed analyses is validated using simulation and measurement results. The results show that NSROs with even N instead of odd N can be used to achieve higher oscillation frequencies while consuming lower power.

7.2 Recommendations for Future Work

- One of the limitations of the proposed TDC is its large silicon area which is due to the vernier architecture adopted for validating the proposed capacitive boosting technique for TDCs. This is a fundamental limitation of the vernier architecture where more buffer cells are needed to increase the dynamic measurement range of the TDC. For a 6 bit resolution, 64 buffer cells are required and since the vernier architecture has 2 delay lines, a total of 128 buffer cells are needed. This increases the overall area of TDC and becomes worse even more if the TDC needs to cover a large measurement range due to the need of more number of delay cells. However, the vernier architecture is a simple technique to quickly validate the functionality and efficiency of the proposed capacitive boosting TDC technique.

Thus, the proposed capacitive boosting TDC technique is not only limited to vernier architecture and the technique can be extended to design various other TDC architectures such as ring oscillator, vernier ring oscillator, gated ring oscillator and switched ring oscillator based TDCs for increasing the dynamic range and decreasing the silicon area at the same time without affecting the time resolution performance metric. Even though, the prototype TDC is designed and fabricated in CMOS 180 nm for low cost, the proposed capacitive boosting TDC technique can be extended to design TDCs at short-channel CMOS processes for further reducing the supply voltage and area consumption of the TDC.

- Current starving technique can be introduced in the DCO system of the proposed ADPLL for further reducing the power consumption of the ADPLL. Multiple cascoded PMOS current sources can be added together with the current starving technique to increase the number of tuning bits which can provide more degree of tuning freedom.

- The capacitive boosting technique can also be extended to design low supply voltage differential negative skewed ring oscillators. Such capacitively boosted negative skewed ring oscillators can in turn be used to design low power and high resolution TDCs and voltage controlled oscillators of PLL.

Author's Publications

This section presents the list of publications and invention disclosures that emerged out of this PhD research [26][27][28][29][30][89][109][110].

Journals:

1. **Arjun Ramaswami Palaniappan** and Liter Siek, "A TDC-less All-Digital Phase Locked Loop for Medical Implant Applications," *Elsevier Microprocessors and Microsystems*, vol. 69, pp. 168–178, 2019.
2. Jian Sen Teh, **Arjun Ramaswami Palaniappan**, and Liter Siek, "Analysis of Negative Skewed Delay Scheme for Ring Oscillator With Multi-Phase Outputs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Submitted, 2019.
3. **Arjun Ramaswami Palaniappan** and L. Siek, "Wide-input dynamic range 1 MHz clock ultra-low supply flip-flop," *Electronics Letters*, vol. 54, no. 15, pp. 938–939, Jun. 2018.

Invention Disclosures:

1. **Arjun Ramaswami Palaniappan**, Jos Verlinden, and Liter Siek, "Sense Amplifier Flip-Flop With Symmetrical Rise and Fall Output Propagation Delay," *IP.Com Prior Art Database: IPCOM000258511D*, 2019.
2. **Arjun Ramaswami Palaniappan**, Jos Verlinden and Liter Siek, "Sense Amplifier Flip-Flop With Symmetrical Rise and Fall Output Propagation Delay," *NXP Semiconductors Defensive Publication ID: 82095159*, 2018.

Conferences:

1. **Arjun Ramaswami Palaniappan** and Liter Siek, "A 0.6 V, 1.74 ps Resolution Capacitively Boosted Time-to-Digital Converter in 180 nm CMOS," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019.
2. **Arjun Ramaswami Palaniappan** and Liter Siek, "A 0.0186 mm², 0.65 V Supply, 9.53 ps RMS Jitter All-Digital PLL for Medical Implants," in *IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, 2018.
3. Jian Sen Teh, **Arjun Ramaswami Palaniappan**, Liter Siek, and Y. Zheng, "Review of pulse generators for gated ring oscillator based Time-to-Digital converters," in *International Symposium on Integrated Circuits (ISIC)*, 2016.

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