Implementation of full carbon-based three-dimensional interconnects

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SINGAPORE

**Implementation of Full Carbon-Based
Three-Dimensional Interconnects**

ZHU YE

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2019

Implementation of Full Carbon-Based Three-Dimensional Interconnects

ZHU YE

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

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Prof. Tan Chuan Seng

Authorship Attribution Statement

This thesis contains material from 1 paper published in the following peer-reviewed journal where I was the first author.

Chapter 6 is published as Ye Zhu, Chong Wei Tan, Shen Lin Chua, Yu Dian Lim, Boris Vaisband, Beng Kang Tay, Eby G. Friedman, Chuan Seng Tan, “Assembly Process and Electrical Properties of Top-Transferred Graphene on Carbon Nanotubes for Carbon-Based Three-Dimensional Interconnects”, *Components Packaging and Manufacturing Technology IEEE Transactions on*, DOI: 10.1109/TCPMT.2019.2940511.

The contributions of the co-authors are as follows:

- A/Prof. Chuan Seng Tan and Prof. Beng Kang Tay provided the initial project direction and A/Prof. Chuan Seng Tan edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr. Chong Wei Tan and Dr. Yu Dian Lim.
- I co-designed the study with Dr. Chong Wei Tan and performed all the laboratory work at the School of Electrical and Electronics Engineering. I also analyzed the data.
- All microscopy, including sample preparation, was conducted by me in Nanyang Nano Fabrication Centre (N2FC).
- Mr. Shen Lin Chua assisted in the fabrication and characterization of the graphene bridge structure.
- Dr. Boris Vaisband and Prof. Eby G. Friedman assisted in the simulations of CNT/graphene interface.

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Abstract

Attributing to its outstanding electrical properties and compatibility with modern electronic devices, there have been numerous studies reported on the fabrication and characterization of carbon nanotube (CNT)-graphene heterostructure. Although there have been some efforts toward the application of CNT-graphene heterostructure for interconnects, none of them demonstrated a full carbon-based implementation in the through silicon vias (TSVs) for three-dimensional integrated circuits (3-D ICs). In this study, the development and optimization of CNT-graphene heterostructure for its application in TSV interconnects were reported. Carbon nanotubes (CNTs) were firstly free-standing grown on the graphene with thermal chemical vapor deposition (TCVD) technique, yielding sufficient length ($\sim 334\mu\text{m}$) and density (estimated as $\sim 10^{11} \text{ cm}^{-2}$) which fulfilled the TSV application requirement. Subsequently, the growth of CNTs within TSVs on the bottom graphene electrodes was successfully demonstrated. The fabrication processes of top wafer with TSVs of various diameters ($5\text{-}50\mu\text{m}$) and bottom wafer with patterned graphene electrodes and catalyst deposition were successfully developed. Next, top TSV wafer and bottom graphene wafer were bonded and manually ground, followed by wet and dry etching to completely remove the handling wafer and buried oxide to expose the underlying TSV holes. By using the same TCVD technique, successful growth of CNTs within the fabricated TSVs on top of the graphene electrodes was achieved.

In order to complete the full-carbon 3-D interconnection, assembly process of top graphene layer after CNT growth needs to be further explored. In this work, transfer process of a top graphene layer onto the as-grown CNT bundles was successfully performed with direct graphene-to-CNT contact at the interface. The electrical properties of CNT/graphene contact were characterized by four-point-probe

(4PP) I-V measurements of the graphene bridge structure. The results suggested that an ohmic contact was achieved between the graphene and CNTs. Low CNT bump resistance of 2.1Ω for $90,000\text{ }\mu\text{m}^2$ CNT area including the CNT/graphene contact resistance was obtained, demonstrating reduction of contact resistance between CNT and Au under the same fabrication and measurement conditions.

The conditions of femtosecond laser annealing for the fusion of graphene and CNTs were explored in this work as well. After the laser power tuning, 0.0166W was selected as the optimized value for annealing. Laser line scanning was applied at the graphene/CNT interface and the electrical properties of the pristine graphene bridge and annealed graphene bridge samples were characterized. The total resistance of the bridge structure dropped to its lowest ($27.3\text{ }\Omega$) after the first laser scanning and increased after the second and third laser annealing. However, the obtained outcomes give insufficient evidences to conclude that the resistance dropping was due to the fusion of graphene and CNTs by the laser annealing. Further studies are needed to verify the formation of CNT-graphene bonding and its impact on the overall resistance upon laser annealing.

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Chapter 1 : Introduction

1.1 Background

1.1.1 Opportunities and Challenges in Next Generation Integrated Circuits

In year 1947, the transistor was invented by scientists John Bardeen, Walter Brattain, and William Shockley who later shared the Nobel Prize. The transistor replaced vacuum tubes, serving as the foundation for the development of modern electronics and making possible the marriage of computers and communications [1]. Since this invention, transistors have emerged as the main game-changer in semiconductor revolution, bringing tremendous changes to the electronics industry. In the 1950s, transistors have broadly adopted and manufactured by firms, where the transistor licenses were prominently granted to Cold War military contractors. The stringent requirements of military applications, for example, miniaturization of circuits, low power consumption and high reliability in rugged, high-temperature environments, served to elevate silicon over as the industry's material of choice [2]. Since then, the silicon-based semiconductor industry has been progressively grown and developed with growing number of transistors/devices per-unit-area on a silicon chip annually [3]. At the same time, the annual sales of semiconductor devices have been undergoing an exponential growth from 1960s to 1980s, as shown in Figure 1.1. Observing the spectacular success of transistors in their large scale integration, it has been prophesize by Gordon Moore, the co-founder of Intel Corp., that the number of transistors on a single chip will be doubled approximately every two years [4], where this prophecy is well known as the Moore's law [5].

Figure 1.1 Annual sales of US semiconductor firms by technology type [2]. Figure source: Khan et al., Nature Electronics. Reprinted with permission from [2], © 2018 Springer Nature Publishing AG.

However, it is believed now that the downsizing will reach its limit in several years due to some reasons [6]. First of all, the photolithography technologies for chip manufacturing is unable to “catch-up” with the development trend as predicted by Moore’s Law [3]. In the current state of semiconductor industry, Deep Ultraviolet (DUV) source with 193 nm wavelength is used to fabricate chips with ~10 nm feature size [7]. To further reduce the feature size, Extreme Ultraviolet (EUV) source with 13.5 nm wavelength is used. It has been demonstrated that EUV source can be used to fabricate chips with 7 nm feature size, and the proof-of-concept has recently been demonstrated in using EUV to achieve 5 nm feature size [8]. It is much anticipated and has taken a big step in the race to keep up with Moore's law, but the EUV technology is still facing a lot of difficulties for shipping products in volume [9]. Secondly, the downsizing of transistors will eventually reach the physical limitation. For example, upon reduction of transistor size to ~2 nm (equivalent to the size of ~10 atoms), various reliability issues of such small transistor arises. These issues include increase of off-leakage current, and the degradation of drain current which may result in

catastrophic damages in the device [4], [6], [10]. Besides the reliability issues, another possible issue is the power consumption due to inefficient operation of the device. As the transistors are closely connected to each other, the power consumption will increase significantly which may result in possible power loss in the device.

Looking beyond the Moore's law, the International Technology Roadmap for Semiconductors (ITRS) highlighted two prevailing trends in the semiconductor industries as depicted in Figure 1.2, namely, "More Moore" and "More than Moore". "More Moore" domain is internationally defined as an attempt to further develop advanced CMOS technologies and reduce the associated cost per function, emphasizes the improvement in performance. Meanwhile, "More than Moore" refers to a set of technologies that enable non digital micro-/nanoelectronic functions, which is characterized by increasing functionalities in an integrated packaged system using system-in-package (SIP) or system-on-chip (SOC) methodology [11].

To achieve continuous development in CMOS technologies which aligns with the Moore's Law, one of the keys towards future scaling is 3-dimensional (3-D) scaling. This involves stacking of chips with different functionalities in a 3-D direction and connects them with miniaturized interconnects [12]. For example, the development of smart phones and Internet of things (IoT) with diverse sensors and processors with low-power consumption requires highly integrated chips. The chips are required to include not only logic processing and cache module, but also memory and power management module. These highly integrated chips are designed to be used in GPS, mobile and WiFi networks, gyroscopes and accelerometers. In the past, these types of devices required individualized manufacturing processes and technologies to meet specific needs. To achieve a single-step fabrication technique, "More-than-Moore" presents a comprehensive strategy to integrate these devices in one single chip.

New processing and supporting technologies will be applied in the integration of different manufacturing technologies with different raw materials. In conjunction to the integration, various aspects need to be considered, including systematic coordination between chips, electrical interconnects for power and signal distributions, to achieve compact, stand-alone next-generation devices.

Figure 1.2 “More-Moore” and “More-than-Moore” concepts describing the scaling trends [13]. Figure source: “More-than-Moore” White Paper, International Technology Roadmap for Semiconductors (ITRS), 2010.

1.1.2 Interconnect Bottleneck

As mentioned in the previous section, interconnects are one of the essential factors in multi-chip, 3D integration. Interconnects are essential in the Integrated Circuit (IC) chips for the distribution of signals and power distribution. However, upon scaling down of devices, scaled chip wiring (interconnect) suffers from increased resistance due to a decrease in the cross-sectional area of the conductor. On top of that, miniaturized interconnects can result in discrepancy of height between metallic interconnects and conductor spacing, leading to the high inter-conductor capacitance. Thus, while scaling down of transistor size contributes to higher computing

capabilities and data processing feasibilities in a single chip, the delay caused by interconnects will be more prominent. As a result, the high resistance and inter-conductor capacitance of interconnects become the performance-limiting factor, which is known to as the “interconnect bottleneck”.

The main concern of interconnect scaling issue is the interconnect delay [13]–[15], or better also known as Resistive-capacitive (RC) delay, which can be expressed by the following formula [16]:

$$RC = 2\rho\kappa\epsilon_0 \left(\frac{4L^2}{P^2} + \frac{L^2}{T^2} \right), \quad (1.1)$$

where $P=W+S$ is the pitch between neighboring interconnects, L is the total line length, W is the interconnect line width, S is the distance between the edges of adjacent interconnects, T is the height of the interconnect, ρ is the resistivity of the interconnect material, κ is the dielectric constant of the dielectric materials between the interconnect lines, and ϵ_0 is the vacuum permittivity. Figure 1.3 shows a cross-sectional view of the interconnect layer illustrating the relevant parameters. Upon scaling down of the interconnect layer, P and T will be reduced, while L will increase, resulting in longer interconnect RC delays as deduced in Equation 1.1.

Figure 1.3 A scaling effect on RC delay in interconnects. Figure source: Ryu, Suk-Kyu's Ph.D. dissertation [17].

Since interconnect RC delay is proportional to the resistivity of the interconnect material ρ and the dielectric constant κ of the insulating layer between the interconnects, reducing ρ and/or κ can reduce the RC delay. In an effort to reduce ρ , copper has replaced aluminum as the interconnect material since the 1990s. At the same time, to reduce the dielectric constant κ of the insulating materials, low- κ dielectric materials [14] with the dielectric constant lower than silicon dioxide ($\kappa = 3.9$) has been introduced into the interconnects. Various low dielectric constant materials such as fluorine-doped silicon dioxide ($\kappa = 3.5$) [18], carbon-doped silicon dioxide ($\kappa = 3.0$) [19], and porous silicon dioxide ($\kappa = 2.0$) [20], have been integrated into the IC manufacturing process. Besides the abovementioned materials, it has been reported that the formation of air-gaps/bubbles ($\kappa = 1.0$) [15] in the trench dielectric levels can effectively reduce the dielectric constant of the interconnect structure. However, the air-gap structures at the trench level confronted serious challenges with poor structural integrity and mechanical stability [21], [22], which are undesirable for seamless fabrication of multi-functional 3-D integrated devices. As of today,

implementing low- κ interconnects with κ lower than 2.5 still remains a challenge among the semiconductor communities.

Besides lowering the metal resistivity and dielectric constant value, another approach in decreasing the interconnect delay can be achieved through modification of processes at packaging level. This includes implementation of 3-D integration multi-functionalities chips during the packaging of ICs, which will be further explained in the following sections.

1.1.3 Three-dimensional (3-D) Integrated Circuits (ICs)

3-D integration can be defined as a technology that involves stacking of multiple processed wafers containing ICs on top of each other with vertical interconnects between different layers. This 3-D structure provides opportunities for electrical performance improvement and enables the integration of devices with incompatible process flows [23]. The most compelling advantage of 3-D structure is the successful addressing of two-dimensional (2-D) problems with vertical interconnects by replacing the long horizontal interconnects with the short vertical interconnects [24]. As a result, the RC delay, cross talk and power dissipation within the IC will be significantly improved. With fixed-length of interconnects, a $> 25\%$ decrease in wire length [25] or interconnect power [26] could be achieved. In addition, by providing the opportunity for the integration of heterogeneous devices and technologies, the advent of 3-D ICs allows integration of multi-functional applications into a single device, achieving higher device density and smaller packaging size.

Figure 1.4 compares the 2-D and 3-D approaches in solving the fundamental wiring limits. Figure 1.4(a) shows the 2-D SiP (System-in-Package) solution. As illustrated in Figure 1.4(a), 2-D SiP possesses lengthy inter-chip connections between the logic and memory chips, which can result in serious memory latency. Meanwhile,

2-D SoC (System-on-Chip) solution involves built-in integration between the logic and memory chips, as illustrated in Figure 1.4(b). 2-D SoC can be speculated to improve the memory latency and device performance by combining blocks of logic and memory components in the same chip. However, such approach increases the fabrication cost significantly as it requires different processing technologies for the logic, memory, and other possible functions. To compensate the shortcomings from both 2-D SiP and SoC, 3-D integration scheme can be employed. As shown in Figure 1.4(c), the 3-D integration scheme involves electrical connections between the logic and the memory components via vertical interconnects. Due to the structural nature of 3-D integration scheme, much shorter interconnects are needed (as illustrated in Figure 1.5), where the memory latency can be significantly reduced, resulting in improved chip performance.

Figure 1.4 Schematic diagrams showing the difference between 2-D and 3-D interconnects (Source: Beyne [27]): (a) 2-D SiP integration; (b) SoC integration; (c) 3-D integration. Reprinted with permission from [27], © 2006 IEEE.

Figure 1.5 Replace the long global wire in the 2-D scheme by 3-D IC with vertical connections and shorter wires. Figure courtesy of Kuan-Neng Chen at National Chiao Tung University, Taiwan.

1.2 Motivation

1.2.1 Challenges of Flip Chip Bumping and Through Silicon Via (TSV)

Technology

The state-of-the-art wiring techniques to achieve electrical interconnections between chip and substrate include wire bonding, flip chip bump and through silicon via (TSV) technology [28]–[30]. Among the abovementioned techniques, flip chip bumps and TSVs offer a shorter, direct electrical path for interconnections between the chip and substrate as compared to wire bonding technique. Flip chip bumps are able to achieve higher input/output (I/O) counts and provide higher device operating speed as compared to its wire bonding counterpart, attributing to its shorter length of interconnects [31]; whereas TSV technology can enable faster, small-path length communication channels between the vertically stacked integrated circuits and devices through the vias [32].

Despite higher operational speed and I/O counts, an existing challenge in flip chip bumping and TSV technology is the discrepancy in coefficient of thermal

expansion (CTE) between copper bump/TSV-filler and its surrounding materials. Copper is widely used in the flip chip bumps and via fillings due to excellent electrical and mechanical properties, favourable compatibility with the back-end of line (BEOL) processes. However, due to the large CTE mismatch between silicon ($2.3 \times 10^{-6}/^{\circ}\text{C}$) and copper ($17 \times 10^{-6}/^{\circ}\text{C}$) [33], Cu-based pillar bumps and TSVs fabricated on Si substrate arises numerous electrical stability and reliability issues, especially under high temperature fluctuations. The CTE mismatch issue is particularly prominent for TSVs. Due to the large CTE mismatch between silicon and copper, the fabrication process can induce substantial thermomechanical stresses in silicon around the vias, resulting in thermomechanical failure in the device [34], [35]. In a typical TSV deposition process, an annealing step at a higher temperature (e.g. 200°C) is applied after the Cu electroplating in order to stabilize the Cu grain structures and relax the stresses in Cu. Upon cooling down to the room temperature, copper contracts much faster and pulls the surrounding silicon, inducing thermomechanical stresses in the silicon area around the vias. The TSV-induced stresses can cause reliability problems such as copper via extrusion and interfacial delamination [36]–[40], and undesirable mobility shifts in devices through the piezoresistivity effect [41], [42]. As most devices are located within a sub-micron depth from the wafer surfaces, the design rules with the near-surface TSV-stress awareness and stress-resulting carrier mobility change are crucial for the successful implementation of 3-D ICs.

Extrusions of Cu vias are frequently observed in the TSV structures upon undergoing high temperature excursion. The via pop-up phenomenon can cause interfacial failure of a TSV (Figure 1.6(a)) and/or cracking in Si near the lower ends of TSVs (Figure 1.6(b)) during the thermal processing [43]. The via-extrusion can be accompanied by interfacial delamination, as shown in Figure 1.6(c).

Figure 1.6 Reliability problems in TSV structures [43]: (a) Interfacial delamination; (b) Silicon cracking; (c) Via extrusion (Pop-up). Figure is from online web source: Cho, S. [43].

As mentioned earlier, piezoresistivity effect in interconnects may cause undesirable mobility shifts in the device. Consequently, TSV-induced stresses will result in variations in electron-hole mobility's in devices, leading to non-uniformity, uncontrollable device performances. To resolve this issue, most IC designers will be informed about the Keep-out-zone (KOZ) when designing devices with TSV structures. KOZ is defined as the area surrounding each TSV where all logic cells must “keep out” to avoid being influenced by the TSV-induced stresses. In actual designing of TSVs-included devices, the presence of abundant TSVs largely occupies the available floor space on 3D-IC layout. Additional KOZ areas further reduces the available floor space, where smaller area of KOZ is desirable to save circuit design floor space as illustrated in Figure 1.7.

Figure 1.7 Illustrations of layouts with small versus large KOZ around TSVs [44]. Yellow squares are TSV landing pads. Reprinted with permission from [44], © 2010 IEEE.

Upon scaling down of transistor feature size and further integration in state-of-the-art chips [45], [46], it can be speculated that TSVs will be facing higher degree of challenges as compared to flip chip bumps. As the TSV diameter scaled down to 2 – 4 μm with aspect ratio of ~ 10 , the requirements needed to achieve satisfactory performance is far more stringent [47], [48]. First of all, the resistance of TSV passivation liner will increase upon scaling down of TSV dimension. Passivation liner is a layer of insulator deposited at the sidewalls of TSVs, to prevent diffusion of Cu into the Si. Upon scaling down of TSV sizes, the volumetric occupancy fraction of passivation liner in TSVs will be more prominent, which increases the overall resistance of the TSV interconnect. Secondly, another technical challenge in scaled-down TSV is the conformal deposition of seed layer. In TSV filling process, it is fundamentally challenging to obtain a conformal deposition of the seed layer for latter Cu filling. In small diameter and high aspect ratio TSVs, the challenge becomes more prominent which may result in lower manufacturing yield in large-scale fabrication. Thirdly, upon reduction of TSV feature size, electro-migration issues become significant as the surface-to-volume ratio of TSV increases. Finally, with higher density of interconnects, the thermal dissipation for removing hot spots and reducing

thermal migration becomes more critical in 3-D ICs.

1.2.2 Advantages of Carbon Nanomaterials

In recent years, carbon nanomaterials, graphene and carbon nanotubes (CNTs) have emerged as promising materials for the integration in the next-generation advanced packaging technologies [28], [49], [50]. The main benefits of carbon nanomaterials, e.g. CNTs, lie in their excellent electrical, thermal and mechanical properties: (i) low electrical resistivity, measured in a range of 0.8~33.8 m Ω •cm for single CNT and CNT bundles [51]–[54]; (ii) high current density $\sim 10^9$ A/cm² in single CNT [55]; (iii) high thermal conductivity, reported in a range of 600-3,000 W/mK for individual multi-walled carbon nanotubes (MWCNTs) [56], [57]; and (iv) closer CTE to Si ($2.3 \times 10^{-6}/^\circ\text{C}$) as compared to Cu ($17 \times 10^{-6}/^\circ\text{C}$), e.g. single-walled carbon nanotubes (SWCNTs) $\sim 2 \times 10^{-6}/^\circ\text{C}$ [58].

Table 1.1 shows the comparison of typical physical properties between Si, Cu and carbon nanotube (CNT) at room temperature. Besides the smaller CTE with Si, the loosely-packed nature of CNT bundles can also ease the thermomechanical stress introduced in the Si substrate [59]. These advantages enable carbon nanomaterials to be a highly attractive candidate as both on-chip and off-chip interconnects in 3-D ICs. Currently, substantial works have been reported for the fabrication and characterization of CNT TSVs on conductive metal lines [60]–[62]. Meanwhile, CNT bumps have been demonstrated as the potential flip chip bumps by several groups [63]–[65]. Apart from CNTs, graphene has also been proposed as a potential candidate to augment copper as the next-generation planar interconnects due to its patterning feasibility and current carrying capacity [66]–[69].

Table 1.1 Typical physical properties of Si, Cu and CNT at room temperature [70].

Material	Young Modulus (GPa)	Poisson's Ratio	Thermal Conductivity (W/mK)	Electrical Resistivity ($\Omega\cdot\text{m}$)	CTE ($10^{-6}/^{\circ}\text{C}$)
Silicon (Si)	169 along $\langle 110 \rangle$ 130 along $\langle 100 \rangle$ (anisotropic)	0.064 along $\langle 110 \rangle$ 0.28 along $\langle 100 \rangle$ (anisotropic)	149	1×10^{-1} to $4 \times 10^{-6}*$	2.3
Copper (Cu)	128	0.34	385	1.68×10^{-8}	16.4
Carbon Nanotube (CNT)	1300	0.0344	3500	0.29×10^{-8} to 1.2×10^{-8} [73]	Axial: -0.6** Trans.: 6.6**
<i>* The resistivity of silicon depends strongly on the presence of impurities in the material</i> <i>**CNT CTE is an average value as there is a range found in the literature</i>					

1.2.3 Full Carbon-Based Interconnects

Recently, a concept of full carbon-based interconnects is proposed by implementing graphene-CNT heterostructures in BEOL and TSVs for 3-D ICs and packages as a higher-performance alternative to their copper counterparts [71]. Hybrid carbon nanostructures, e.g. the pillared CNT-graphene nanostructure shown in Figure 1.8 [72], are speculated as one of the graphene-CNT hetero-structures which can be potentially applied in the 3-D integration. Benefiting from the combination of one-dimensional (1-D) nanotubes and two-dimensional (2-D) graphene, 3-D graphene-CNT hetero-structure possesses desirable out-of-plane properties [73]–[75] while maintaining the in-plane properties. Attributing to the speculated benefits of this structure, it has attracted numerous innovative applications including new efficient electrodes for fuel cells [76], nano-porous structures for hydrogen storage [72] and supercapacitors [77], tailored orthogonal thermal transport materials [75] and building blocks for nano/microscale integrated devices [78], [79].

**Figure 1.8 Pillared CNT-graphene nanostructure with 3D network [72].
Reprinted with permission from [72], © 2008 American Chemical Society.**

Currently, various successful attempts for the fabrication of graphene-CNT hybrid structures [80]–[83] have been done reported. One of the pioneering studies of the graphene-CNT hybrid structures is reported by Y.S. Kim *et al* [73], where hybrid graphene-CNT structure comprising of out-of-plane CNTs grown on the graphene layer is fabricated and its electrical properties are characterized. Y. Zhu *et al* [84] developed a method to bond graphene and single-wall carbon nanotubes (SWCNTs) seamlessly (Figure 1.9(a)), which shows an ohmic contact formed between the bonded CNTs and graphene (Figure 1.9(b)). This study reports the first observation of the covalent transformation of sp^2 carbon between the planar graphene and the vertical-aligned SWCNTs under the atomic resolution by scanning transmission electron microscopy (STEM) (Figure 1.10). On the other hand, a novel carbon composite structure of multi-layered graphene combined with the upper ends of vertically aligned multi-wall CNTs (MWCNTs) on the substrate has been synthesized (Figure 1.11(a)) [23]. One of the unique features of this graphene-CNT composite is the self-organization within the atomic structure of the multi-layered graphene, prior the CNT growth. Attributing to the self-organizing nature, the upper ends of CNTs can be electrically connected to each other via the graphene (Figure 1.11(b)) [85]. On the

other hand, a similar hybrid material with graphene film tightly connected with the upper ends of the CNT arrays has also been reported, synthesized by a two-step chemical vapor deposition (CVD) process [80]. In general, most graphene-CNT hybrid structures are fabricated via CVD method during the CNT growth stage.

Most recently, a demonstration shows that the full integration of intercalation-doped multi-layer graphene (MLG) wires and CNT vias offer higher performance and better reliability as compared to the Cu interconnects at 5nm node [80]. Another successful fabrication of graphene-CNT heterostructure for the off-chip interconnects was made through a direct growth of CNTs within the vias and on top of the graphene [33]. To form a complete full-carbon 3-D interconnection, the assembly process of the top graphene layer after CNT growth shall be further explored.

Figure 1.9 (a) Scheme and SEM results for the synthesis of SWCNTs directly from graphene and (b) I–V measurements [84]. Reprinted with permission from [84], © 2012 Macmillan Publishers Limited.

Figure 1.10 TEM and STEM images of CNT–graphene junctions [84]. Reprinted with permission from [84],© 2012 Macmillan Publishers Limited.

Figure 1.11 SEM images of (a) synthesized graphene/CNT composite and (b) TEM images around the connection between graphene and CNTs [85]. Reprinted with permission from [85], © 2008 The Japan Society of Applied Physics.

1.3 Objective

In this thesis, the possibilities of implementation of the graphene-CNT hetero-structure in through silicon vias (TSVs) for novel 3-D interconnects will be explored. In this approach, vertical-aligned CNTs and graphene will be integrated into 3-D interconnect structures. Vertical-aligned will be developed to replace the conventional metal in TSVs, while graphene will be developed to replace the traditional horizontal metal lines. The key challenges include, but not limited to (1) process development in growing high density CNT bundles above bottom graphene electrode within TSVs, (2) accurate transfer of a top graphene layer onto the as-grown CNT bundles, (3) atomic fusion between transferred graphene and CNTs to form carbon covalent bonds to reduce CNT-graphene contact resistance, (4) microstructural and electrical characterization of CNT-graphene structure to justify the occurrence of atomic fusion between CNT bundles and graphene layer. Several objectives are intended to be achieved as follows:

- 1) Feasibility study of the CNT growth on the graphene under experimental conditions
- 2) Process design and development to grow high-density CNT bundles within TSVs
- 3) Process development of transferring graphene layer onto the as-grown CNT bundles
- 4) Microstructural studies of the fabricated structures (by Raman, SEM and TEM)
- 5) Electrical studies of the fabricated structures (by I-V measurements)
- 6) Development and exploration of the femtosecond laser annealing condition for the fusion of transferred graphene and CNTs

1.4 Major Contributions of Thesis

One of the significant outcomes of this thesis is the successful demonstration of CNT growth on the bottom graphene electrodes within TSVs. First of all, the fabrication processes of top wafer with TSVs of various diameters (5-50 μ m) and bottom wafer with patterned graphene electrodes and catalyst deposition were successfully developed. Next, top TSV wafer and bottom graphene wafer were bonded and manually grounded, followed by subsequent wet and dry etching steps to completely remove the handling wafer and buried oxide exposing the underlying TSVs. Finally, CNT growth was carried out using thermal CVD (TCVD) approach within the TSVs on the bottom graphene electrodes. As compared to the free-standing CNT growth with sufficient length ($\sim 334\ \mu\text{m}$) and high density (estimated as $\sim 10^{11}\ \text{cm}^{-2}$), inhibited growth of CNTs are obtained within the TSVs. The inhibited growth of CNTs can possibly be attributed to several process-engineering steps involved, e.g. wafer-bonding, grinding and wet/dry etching. Further modification and optimization of the process steps need to be done in order to attain higher density of CNT fillings within the unfilled TSVs.

Upon growing of CNT bundles on graphene electrode within TSVs, transfer process of a top graphene layer onto the as-grown CNT bundles was successfully performed with direct graphene-to-CNT contact at the interface. Four-point-probe (4PP) I-V characterization suggests that an ohmic contact was achieved between the graphene and CNTs. Low CNT bump resistance of 2.1Ω for $90,000\ \mu\text{m}^2$ CNT area including the CNT/graphene contact resistance was obtained, demonstrating reduction of contact resistance with additional graphene layer on the CNT bundles. The thesis presents preliminary outcomes for the assembly process of transferring a top-graphene layer onto CNTs, and the electrical properties of direct graphene-to-CNT contact. The obtained outcomes provide an insightful understanding on the application of CNT-graphene structures in electrical interconnects, paving the way for the implementation of full carbon-based 3D interconnects.

1.5 Organization of Thesis

This thesis is organized into 8 main chapters. Chapter 1 outlines the introduction of the research work carried out in this doctorate study. Chapter 2 introduces the literature review and the state-of-the-art of the relevant studies which have been reported. Chapter 3 reports the development and optimization of CNT growth on graphene layer. Chapter 4 demonstrates CNT growth within TSVs on top of the graphene electrodes. Chapter 5 explores the transfer of graphene onto the top of CNT bundles to physically secure the top graphene layer onto the CNT tips. Chapter 6 characterizes the electrical properties of direct graphene-to-CNT contact. Chapter 7 explores the feasibility of using femtosecond laser annealing for graphene-CNT fusion. Finally, Chapter 8 outlines the conclusion of this research, and the possible future continuation works from this research.

Chapter 2 : A Review of Carbon Nanotubes (CNTs) for Through Silicon Via (TSV) Interconnects

2.1 Through Silicon Vias (TSVs)

A critical structural element in the 3-D integration is the through silicon via (TSV) [27], [86], [87], as shown in Figure 2.1. TSV provides a preferable alternative to the long wiring in the 2-D schemes by vertical connections between the stacked dies. The use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs. However, the TSV fabrication process is technically-challenging due to the involvement of Deep Reactive Ion Etching (DRIE) to create through-structure deep hole for the accommodation of the Cu-based interconnect.

Figure 2.1: 3-D integration using TSV structures: (a) Illustration of TSVs. Figure courtesy of Chuan Seng Tan at Nanyang Technological University, Singapore. (b) TSV samples. Figure is from online web source: Ron Maltiel [88] .

The fabrication of TSVs involves three key processes [89]–[92] : 1) via hole etching, 2) TSV materials filling, and 3) Si wafer thinning and wafer bonding/debonding. For a reliable and efficient TSV fabrication, each of the three processes needs to be optimized. In general, DRIE, also known as the “Bosch” process, is applied to fabricate the through-substrate-deep hole vertically within the silicon wafer for via etching process.

However, careful control of the Bosch process is needed to prevent formation of scallop-shaped sidewalls (Figure 2.2(a)) [36], [92] . Formation of scallop-shaped sidewalls can be attributed to under-optimization of DRIE process, where the scalloped contours hinder the conformal deposition of barrier and seed layer. Non-conformal barrier and seed layer may increase the susceptibility of Cu (widely used via-filling material) diffusion into Si, resulting in under-filling of TSVs [93]. Under-filling of TSVs may result in the occurrence of voids and pinholes within the TSV Cu pillars (Figure 2.2(b)) [94], directly affecting the device reliability. In addition, the thinning-down process of the Si substrate by chemical-mechanical polishing (CMP) could cause wafer warpage (Figure 2.2(c)) [95], which leads to subsequent problems in 3-D stacking. To address various processing issues, several processing flows have been investigated [92], [96], [97]. As of today, two TSV integration processes are mostly used in the semiconductor industry: ‘via-middle’ and ‘via-last’ processes. The main difference in these two processes is the sequence of the TSV formation relative to the wafer thinning and wafer bonding/debonding processes.

Figure 2.2 Processing issues: (a) scallops at sidewall, where TEOS is an insulating liner material [92]; (b) voids inside TSV [94]; (c) wafer warpage [98]. Reprinted with permission from [92] [94] [98] , © 2008, 2010 IEEE.

Via-middle process

Figure 2.3 illustrates the via-middle process, which is performed following the FEOL fabrication process. A typical via-middle process flow to fabricate TSVs with a diameter of 10 μm and a depth of 50 μm in the Si substrate is described as follows. First, lithography is carried out to pattern the TSV openings across the wafer. Next, DRIE is used to fabricate the TSV holes of desired dimensions. Then, an oxide liner of $\sim 1 \mu\text{m}$ thickness is deposited within the TSV holes. The oxide layer (dielectric layer) reduces capacitance and improves electrical isolation between the TSVs and the Si substrate. In some cases, instead of oxide, polymeric dielectric materials [99], [100] such as benzocyclobutene (BCB) or parylene have been deposited as the sidewall insulators. To prevent diffusion of Cu into the Si substrate, a thin barrier layer ($\sim 50\text{nm}$) of Ta/TaN or Ti/TiN is deposited. For Cu electroplating, a thin Cu seed layer is first

deposited in the TSVs, followed by Cu electroplating process to filled the pre-fabricated TSVs. A subsequent annealing step could be applied to stabilize the Cu grain structures and relax the thermomechanical stresses in Cu for further processing. At the final stage of the TSV fabrication, CMP is carried out to remove the Cu overburden, top Ta/TaN and oxide layers, and to planarize the wafer surface. The fabrication of TSV structures is followed by the BEOL process in which interconnects are made and bonding pads are patterned. Finally, the Si substrate is thinned down to the optimized TSV height ($\sim 50\text{ }\mu\text{m}$).

Figure 2.3 Via-middle process for TSV structures. Figure is from online web source: Yannou, J. [101]

Via-last process

The via-last process involves similar processes as described in the previous sections, including etching of TSV holes and deposition of dielectric layer and barrier layers. However, although the final structure constructed by the via-middle or via-last process could be the identical, the process sequence used in the via-last process (Figure 2.4) is quite different from the via-middle process. In the via-last process, both FEOL and BEOL structures are first fabricated on the Si wafer. Then, the wafer is thinned down up to the depth that is optimized for the TSV height. This is then followed by etching of the via holes from the back side of wafer to reach the interface of BEOL interconnect lines, and filling the holes by the sequence of dielectric layer, Ta/TaN barrier layer, Cu seed, electroplating of Cu, and finally a CMP process.

Figure 2.4 Via-last process for TSV structures. Figure is from online web source: Yannou, J. [101] .

2.2 Growth and Fabrication of CNT TSVs

CNT growth and via-filling in TSVs can be done by two distinct process flows, either by growing CNT bundles directly in TSVs in a bottom-up approach, or otherwise by transferring CNT bundles, pre-growth, into the TSVs. For the bottom-up approach, catalyst layer shall first be deposited onto the bottom of TSVs first, followed by CNT growth using CVD method. Three catalyst deposition methods are commonly used for CNT growth: sputtering, e-beam evaporation and chemical deposition. Previous works done by R Xie et al [102] shown that sparsely-grown CNTs are obtained from sputtered catalyst layer at the bottom of TSVs (aspect ratio 5-10), possibly due to insufficient catalyst deposition at the bottom of TSVs (Figure 2.5). It can be explained that the mean free path of catalyst in a sputtering chamber is relatively short as compared to the distance between targeted material and the substrate during the sputtering process. On the other hand, e-beam evaporation-deposited catalyst can grow vertically-aligned CNT bundles from the bottom of vias openings. However, TSVs were only partially filled by CNTs grown using e-beam evaporation-deposited catalyst (Figure 2.6). Due to the isotropic nature of the evaporation process, not all vias are directed in parallel to the direction of evaporation. As a result, vias that are not parallel to the evaporation direction receive limited catalyst deposition. Apart from sputtering and e-beam evaporation, catalyst deposited by chemical method (e.g. dip-coating in a FeCl_2 solution) is found to be an alternative

method for realizing the bottom-up vertical-aligned CNTs fully filled the TSV holes (Figure 2.7).

The main disadvantage of the bottom-up approach for CNT growth is that it requires high growth temperatures, approximately 700°C to fully-fill the TSVs [53] which is incompatible with conventional CMOS process (usually <400°C). For the sake of compatibility with CMOS technology, successful TSV filling by a low-temperature CNT transfer process at 200 °C has been reported, replacing the direct growth of CNTs in the vias [29]. However, the post-growth transfer process is limited to large diameter TSVs [103], as small diameter (<30µm) TSV structures exhibit stringent alignment accuracy, hindering it from large scale, repetitive manufacturing process [29], [103].

Figure 2.5 SEM images of CNT forest on top of the TSV pattern: Fe-catalyst placement is done by sputtering on Al₂O₃ layer using (a) 1 nm, (b) 2 nm and (c) 3 nm Fe [102]. © 2013 IOP Publishing Ltd.

Figure 2.6 SEM images of CNT bundles grown inside the TSV vias with Al₂O₃ and an evaporated thin film of (a) 2 nm, (b) 3 nm, (c) and 4 nm Fe, with in (d) a zoom-in of the 2 nm Fe result [102]. © 2013 IOP Publishing Ltd.

Figure 2.7 SEM images after dip-coating in 0.1 M FeCl₂ (in ethanol) on Al₂O₃ and CNT growth (a), (b) in individual vias; (c) high-resolution image of a CNT bundle; (d) TEM image of a typical CNT removed from a TSV [102]. © 2013 IOP Publishing Ltd.

2.3 Contact Resistance between CNT and Metal

Despite outstanding electrical properties of CNTs and favourable CTE mismatch between CNTs and Si substrate, one of the major obstacles in the application of CNTs in TSV interconnects is the CNT-metal contact resistance. Due to the injection barrier at the interface between metal and both single- and multi-walled CNTs, CNT-metal contact resistance was reported to reach 10^{-6} to $10^{-9} \Omega \cdot \text{m}^2$ [104], [105]. The contact resistance between CNT-metal interface can be attributed to several factors, including wettability of CNTs [106], quantum resistance of CNTs [107], and the electrical-conducting temperature of the CNT-metal interfaces [108]. To resolve the CNT-metal resistance issue, various efforts have been reported. It has been reported by Hafizi et al. that the deformation of CNTs may reduce the contact resistance between CNT-metal interfaces. Upon deformations of CNTs, a band gap reduction in the deformed CNTs increases metal-induced doping of a nanotube, and thus increasing the number of the conduction channels and introduces additional scattering at the contact, resulting in the reduction of CNT-metal contact resistance [109]. Meanwhile, Fediai et al. reported that the reduction of CNT-metal contact resistance can be achieved by using incomplete metal coverage on the CNTs. Since CNT-metal interface possesses high contact resistance, incomplete coverage of metal

on CNT bundles can reduce the contact resistance, enhancing the overall electrical properties of the CNT-based interconnects [110].

Besides the abovementioned strategies, an effective approach in reducing the CNT-metal contact resistance is to introduce graphitic layers between the CNT-metal interfaces. Due to the formation of C-C bond between the graphitic layer and the CNTs, the CNT-metal contact resistance can be significantly reduced [111]. One of the commonly reported graphitic layers to be incorporated onto CNT interconnects is graphene. Due to the abundant presence of graphitic sp^2 bond and its associated unique electrical properties, graphene has been reported to reduce the CNT-metal contact resistance [112]. However, despite potential benefits from the hetero-structure, limited studies have been reported on the fabrication and application of Graphene-CNT structures in TSV interconnects.

2.4 Fabrication of Graphene-CNT Heterostructure

One of the pioneering works reported on the fabrication of planar graphitic-CNT hetero-structure is graphite-CNT structure. Labunov et al. has reported successful fabrication of multi-level composite nanostructures based on the arrays of vertically aligned CNTs and planar graphite layers. In the reported work, graphite-CNT structure is fabricated using a one-step injection CVD technique, utilizing high temperature catalytic pyrolysis of fluid hydrocarbon. It opens a way to the three-dimensional functional devices creation, in particular, multi-level graphite (graphene) very large scale integrated circuits with the vertical commutations on the basis of CNTs [113]. Meanwhile, Ghosh et al. reported CNT filling of TSVs, with graphene layers as electrical linings at the bottom of the TSVs. Upon including of graphene layers onto CNT-based TSV fillings, the contact resistance between CNTs and the underneath metal surface has been significantly reduced. At the same time, the CNT-

graphene heterostructure has approximately 15 times higher thermal conductivity of the carbonaceous materials compared to copper, providing excellent pathways for the effective heat-transfer from hotspots to the heat-sinks in multi-chip stacked configurations [114]. On the other hand, Jiang et al. introduces full integration of multilayer graphene and CNT vias, enabled by a unique carbon-nickel alloy contact technology. Owing to the extremely high current carrying capacity, thermal conductivity and large carrier scattering length of carbon nanomaterials, the reliability of the all-carbon interconnect technology is demonstrated to surpass that of Cu [115].

Despite availability of various works on CNT/graphene integration, the application of CNT-graphene onto TSV interconnect application is still under-explored. Therefore, exploratory and development work on the growth, fabrication, and characterizations of CNT-graphene heterostructure for TSV interconnect applications is called for.

2.5 Annealing Methods for Metal-CNT Fusion

In accordance to the proposed graphene-CNT heterostructure, a stable and low-resistance ohmic contact at graphene/CNT interface plays a major role for its application in 3-D interconnects. However, limited work has been reported on the fusing of graphene sheets onto CNT tip. In this thesis, possible annealing methods are explored by investigating the effect of various thermal treatments onto the CNT/metal interface. Fundamentally, CNT-graphene fusion can be achieved by thermal annealing to enhance the crystallinity within the CNT-graphene interface [116], [117]. Thermal annealing is a commonly-used method to improve the contact resistance between CNTs and metal electrodes [111], [118]. Y. Zhang et al [119] reported achievement of a low-resistance contact between single-wall carbon nanotubes (SWCNTs) and transition metal electrodes via a controlled solid–solid reaction (Figure 2.8) under

elevated temperature (800-1000°C). Apart from that, they found that the low-resistance contact originates from the formation of a crystalline heterostructure of CNT/metal carbide at the interface (Figure 2.8, suggesting the formation of chemical bonds between CNTs and metal carbide (TiC) after the thermal annealing [119]. Meanwhile, J. Lee et al [120] reported prolonged stable contacts with low resistance between the CNTs and the Ti–Au electrodes using rapid thermal annealing (RTA) under low temperatures (600-800°C). However, for integration of CNTs in silicon-based applications, thermal annealing exhibits serious technical challenges as silicon-based devices have lower thermal tolerance in general, where thermal-induced failure will possibly occur in high temperature (>600°C) conditions.

Using an electric current-induced Joule-heating annealing method, on the other hand, was demonstrated as an alternative way to modify the contact resistance between CNTs and metal. Annealing can be carried out through resistive heating of the substrate where CNTs are grown. By pulsed electrical annealing, Y. Woo et al [121] reduced the contact resistance between an individual single-wall carbon nanotube (SWCNT) and palladium (Pd) electrodes without destroying the field effect transistor devices.

Apart from the joule heating by chamber-heating or resistive heating, recent works have suggested pulsed laser annealing (PLA) as a favorable heating technique, especially in the fabrication of semiconductor thin films [122]. Utilizing a high intensity, short laser pulse to irradiate the sample, PLA creates either a melting front that subsequently solidifies into a single or polycrystalline material, or thermal heating in solid phase within the short laser pulse. Due to the non-destructive, rapid heating, of PLA, it has been considered as one of the most promising methods for the thermal-fusion of graphene and CNTs.

Figure 2.8 (a) Schematic illustration of the method for fabricating nanotube/carbide heterostructure by solid-solid reaction (M=Metal) [119]. © 1999 AAAS. (b) TEM and High-resolution TEM images of the interface between TiC and SWCNT bundle [119]. © 1999 AAAS.

Chapter 3 : Free-Standing CNT Growth on the Graphene

3.1 Introduction

As discussed in the previous chapters, graphene-CNT heterostructure possesses numerous benefits and exhibits promising potential towards its application in future 3-D interconnects. Vertically-aligned MWCNT bundles grown on the graphene are the preferred choice in through silicon vias (TSVs) for novel 3-D interconnects. Two commonly explored techniques to achieve vertical alignment within CNTs are by thermal chemical vapor deposition (TCVD) and plasma enhanced chemical vapor deposition (PECVD). Generally, TCVD-grown MWCNTs have smaller diameter with higher area density as compared to PECVD-grown MWCNTs.

Numerous researches have been reported to investigate the growth mechanism of CNTs on metal lines. However, growing CNTs directly on metal lines is challenging, as metallic catalyst will diffuse into metal surface during CNT growth, due to the requirement of elevated temperature (600~800°C) during CNT growth [123]. A solution to the diffusion of metallic catalyst is to introduce a barrier layer that blocks unwanted catalyst diffusion into the metal lines. However, can CNTs grown directly on graphene layer, or a barrier layer is still necessary, despite the presence of graphene? Thus, it is necessary to study the growth of CNTs on the graphene.

3.2 Experimental Objective and Scope

Despite the presence of prior studies reporting about CNT growth on graphene, significant discrepancies on the methodology, techniques, and outcomes can still be found across various reported studies. To realize the application of CNT-graphene heterostructure in TSV interconnects, it is important to investigate the feasibility of CNT growth on graphene layer. To optimize CNT growth on graphene layer with TCVD technique, effects of temperature profile and Fe catalyst thickness on the

morphological structure of grown CNTs were carefully studied. This is to obtain optimized CNT growth condition for its latter application in filling TSV voids with graphene bottom electrodes, which will be discussed in the next chapter.

3.3 CNT Growth Method

Aixtron Black Magic System was used for the growth of vertical-aligned MWCNTs under thermal CVD (TCVD) mode. The key advantage of this system is the presence of a shower head with patented design, located vertically above the substrate. This unique design allows the gases to be distributed uniformly across the 2" diameter substrate, leading to the growth of high uniformity CNTs. The picture of the deposition system and the description of available growth mode in Aixtron Black Magic System are shown in Figure 3.1.

Figure 3.1 Photograph of Aixtron Black Magic CVD system (left). The various growth modes and CNTs types available using Aixtron Black Magic system (right).

In TCVD mode, iron (Fe) catalyst aluminum oxide (Al_2O_3) or Al/ Al_2O_3 barrier layers are optimized in the manufacturer-default CNT growth recipes available in Aixtron Black Magic system. The optimum thickness of typical Fe catalyst reported in the literature is 1-2 nm [124]. As it is technically challenging to measure Fe catalyst

film of 1-2 nm using conventional thin film measurement equipment, the deposition time of Fe film will be used as an indication to gauge the Fe thickness, using the known deposition speed of 0.1~0.2 Å/sec.

It has been reported that CNTs grown from Fe catalyst on Al₂O₃ barrier layer possess high crystallinity structure with vertically-aligned CNT morphologies [50], [125]. However, one major drawback is that Al₂O₃ has low electrical conductivity, hindering its applicability in CNT-based interconnects. It has been reported that Al₂O₃ barrier layer of ≥ 4 nm thickness exhibits high resistivity, which will affect the overall electrical conductivity of the CNT/metal interface due to formation of non-ohmic contact. Meanwhile, omitting the Al₂O₃ barrier layer may solve the non-ohmic contact issue, but employing pure Al barrier layer result in the formation of sparsely-grown, short CNTs, which is undesirable for TSV interconnect applications [28]. Thus, a combination of Al and Al₂O₃ is preferred for TSV interconnect CNTs as it takes both factors into consideration: functionality and electrical properties of the barrier layer. By varying permutations of Al/Al₂O₃ layers thickness, the most preferable combination of barrier layers was optimized to be 8 nm Al/2 nm Al₂O₃ with a low resistivity of $2.7 \times 10^{-6} \Omega \cdot \text{cm}$ [50], [125].

In a typical TCVD growth process, acetylene (C₂H₂) is used as the carbon feedstock gas, where hydrogen (H₂) is used as the etchant. A typical cycle of TCVD growth ranges between 1 to 5 min depending on the required length of CNTs. The typical growth cycle of CNTs using TCVD technique is shown in Figure 3.2. As shown in Figure 3.2, “Ramping up” refers to the increase in heater temperature accompanied by flow of H₂ gas, “Pre-growth” refers to pre-growth of CNTs with slightly lower temperature than the actual growth stage, whereas “CNT growth” refers to the actual growth process, where the growth temperature is ramped up from the

“Pre-growth” stage, reaching the actual CNT growth temperature

Figure 3.2 Temperature profile of a typical TCVD growth cycle. The growth time can vary from 1 to 5 min.

3.4 Effects of Temperature Profile and Fe Catalyst Thickness

To obtain vertically-aligned CNTs with high crystallinity, the TCVD growth recipes for CNTs are optimized, varying various parameters such as durations and temperatures in annealing, pre-growth, growth, and post-growth stages. Pre-growth and growth stages refer to preliminary growth of CNTs with lower temperature and actual growth of CNTs with higher temperature, as described in the previous section. Annealing stage refers to the pre-growth annealing of Fe catalyst under continuous H₂ flow, whereas post-growth stage refers to annealing of CNTs after the growth process under continuous H₂ flow. At the same time, to optimize the growth recipe, Fe thickness, and C₂H₂/H₂ gas flows are varied. Considering all variable factors, 3 growth recipes were explored, as shown in Table 3.1. Recipe #1 contains an annealing process at 500°C and a pre-growth at 600°C. Recipe #2 contains an annealing process at 500°C and a post-growth at 700°C but without the pre-growth process. Recipe #3 only had a

direct CNT growth at 700°C without the annealing process or pre-/post-growth. The CNT growth temperature for the three recipes was fixed at 700°C. To understand the effect of the 3 investigated growth recipes on the quality of the obtained CNTs, preliminary characterizations are carried out, including CNT height and its associated Raman spectra, as summarized in Figure 3.3 and Table 3.1. From the obtained results, direct CNT growth at 700°C without the pre-/post-growth yields the highest length and I_G/I_D peak ratio among the investigated recipes, indicating high degree of CNT crystallinity. Using the same growth recipe, the CNTs grown from 1.1nm and 2.2nm Fe catalyst show the similar I_G/I_D peak ratio, suggesting that the catalyst thickness has limited impact on the CNTs' crystallinity.

To understand further, growth temperature is varied individually to investigate its impact on the obtained CNTs. By using similar CNT growth duration (2 min) without the annealing process or pre-/post-growth, the growth temperature is varied from 550°C to 700°C. The obtained CNT heights and morphological characteristics are shown in Table 3.2 and Figure 3.4, respectively. It can be observed that the CNTs grown at 550°C were not aligned well vertically and had a porous structure with relatively sparse inter-tube spacing as compared to CNTs grown at 600°C and 700°C. Also, the length of CNTs grown at 550°C is shorter than those grown at 600°C and 700°C. Thus, in order to have a vertically-aligned CNT growth with the adequate length and high density, the minimum CNT growth temperature should be around 600~700°C.

Table 3.1 Recipe tuning for MWCNT growth

Recipe No.	#1		#2		#3	
Annealing Temp.(°C)	500	500	500	500	-	-
Annealing Time(s)	15	15	15	15	-	-
Pre-growth Temp.(°C)	600	600	-	-	-	-
Pre-growth Time(s)	30	30	-	-	-	-
Growth Temp.(°C)	700	700	700	700	700	700
Growth Time(s)	270	270	300	300	300	300
Post-growth Temp.(°C)	-	-	700	700	-	-
Post-growth Time(s)	-	-	120	120	-	-
Barrier layer	Al 8nm/Al ₂ O ₃ 2nm					
Fe thickness(nm)	1.1	2.2	1.1	2.2	1.1	2.2
H ₂ Flow (sccm)	600	600	600	600	600	600
C ₂ H ₂ Flow (sccm)	200	200	200	200	200	200
CNT growth length(μm)	88	140	180	157	235	244

Figure 3.3 Raman spectra images of CNT growth using three different recipes with 1.1/2.2nm Fe as catalyst.**Table 3.2 Density and length of CNT growth with the same growth time (2 min) under different temperature (550, 600 and 700 °C).**

	Avg. CNT growth length (μm)	
Temp. (°C)	1.1nm Fe	2.2nm Fe
550	3.0	3.5
600	28	19
700	101	105

Figure 3.4 SEM images of CNTs grown on 2nm Fe with the same growth time (2 min) under (a) 550 °C, (b) 600 °C and (c) 700 °C.

3.5 Growth of Patterned CNT Pillars on the Graphene

Graphene-deposited wafers used in this section were purchased commercially (4" silicon wafers with 470nm SiO₂ with a 7cm × 7cm double-layer transferred graphene) from Hangzhou Gelanfeng Nanotechnology Co., Ltd. The full wafer was manually cleaved into small dies with 12mm × 12mm dimension before processing.

The crystallinity of the purchased graphene wafers was carefully checked by optical and Raman microscopy (Raman system: Witec Alpha 300R) before processing. Catalyst/barrier layer was deposited on the graphene with lift-off process. Negative photoresist (ma-N 1440) was used to pattern the area for catalyst/barrier layer deposition. 8nm Al, 2nm Al₂O₃ and 1.1nm Fe were sequentially deposited by e-beam evaporation. Pre-growth and CNT growth temperatures were set as 600/700°C respectively, with 30s and 300s as the pre-growth and CNT growth durations, respectively. Temperature ramping speed was set as 100 °C /min. C₂H₂ and H₂ gas flow during CNT growth were set as 200/600 sccm respectively. Figure 3.5 shows the SEM images of patterned CNT pillars grown on the graphene layer, showing dense, vertically-aligned CNTs with ~334 μm height which is sufficient for TSV interconnect application. The average diameter of CNTs was ~5 nm as shown in TEM images (Figure 3.6). CNT (ρ) can be estimated using the following equation:

$$\rho = \frac{F \times S}{\pi(d/2)^2}$$

where F is the filling factor ratio defined as the surface area covered with CNTs after densification over the surface area before densification, S is the surface area before densification, d is the average diameter of CNTs. To determine the filling ratio, bumps of 1 mm² were patterned (not shown) on each sample and subjected to same growth process. The densification process was performed by immersing the sample in IPA. The filling factor was calculated to be 0.132 ± 0.008 by using imaging software pixel calculation based on more than 10 CNT bumps. Subsequently, the surface density of CNTs can be calculated to be ~10¹¹ cm⁻².

The grown CNTs can be postulated to have high level of defectively due to low *I_G/I_D* peak ratio (Figure 3.7(a)). This reflects on the *I_G/I_D* peak ratio of CNTs grown on graphene, where the CNT-graphene hetero-structure exhibits wider D peak with higher

intensity as compared pristine graphene (Figure 3.7(b)), indicating the formation of amorphous carbon on the graphene sheet. The formation of amorphous carbon can possibly due to the pre-growth step which was carried out at relatively low temperature (600°C).

Figure 3.5 SEM images of patterned CNT pillars grown on the graphene layer.

Figure 3.6 Transmission electron microscopy (TEM) images of the as-grown CNTs.

Figure 3.7 Raman spectra images of (a) as-grown CNTs and (b) graphene before/after CNT growth.

3.6 Summary

In this chapter, recipes and methodology to grow free-standing CNTs on graphene sheet has been explored and optimized. TCVD approach yields sufficient length ($\sim 334\mu\text{m}$) and high density (estimated as $\sim 10^{11} \text{ cm}^{-2}$) CNT growth. Different growth parameters such as catalyst film thickness, growth time and growth temperature have been systemically studied. With the understanding of different growth parameters, the feasibility in growing CNTs within TSVs on the bottom graphene electrodes will be explored.

Chapter 4 : CNT Growth within TSVs on the Bottom Graphene Electrodes

4.1 Introduction

The state-of-the-art, industrial standard TSV technology prefers copper as the TSV-filler material due to its compatibility with the back-end of line (BEOL) processes, along with suitable electrical and mechanical properties of copper material. However, a technical challenge lies within Cu TSVs is the coefficient of thermal expansion (CTE) difference between copper and its surrounding materials, which is mainly silicon. Due to the relatively large mismatch of CTE between silicon ($2.3 \times 10^{-6} / ^\circ\text{C}$) and copper ($17 \times 10^{-6} / ^\circ\text{C}$), Cu TSVs give rises to many stability and reliability problems during chip operation, especially under high temperature fluctuation conditions.

The newly emerged concept of full carbon-based interconnects are expected to have numerous advantages over their copper counterparts. The advantages include: 1) less thermal mismatch stress in TSVs than Cu due to the low CTE and porous nature of CNTs; 2) favorable heat dissipation properties due to the high thermal conductivity of CNTs and graphene; and 3) possibly lower contact resistance of the CNT/graphene interface as compared to the CNT/metal interface.

4.2 Experimental Objective and Scope

In this chapter, bottom-up growth of CNTs on the bottom graphene electrode within TSVs is demonstrated. A fabrication process flow was designed and optimized to investigate the possibility of replacing the horizontal metal lines and metal-filled TSVs with graphene-CNT heterostructure. The introduction of extra fabrication steps onto the free-stranding CNT growth mentioned in Chapter 3 will expose the catalyst to foreign environments and adversely affect the growth of CNTs. Finally, the fabricated

structure was characterized by optical microscopy, Raman and SEM.

4.3 Designed Fabrication Process Flow

The designed fabrication process flow contains three parts: 1) top wafer with TSV etching, 2) bottom wafer with graphene patterning and catalyst deposition 3) process steps after top and bottom wafers bonding, as shown in Figure 4.1. For top wafer processing, silicon-on-insulator (SOI) wafer is used as the starting wafer for the fabrication. First, channel etching was designed to form a space for the accommodation of graphene and catalyst layers on the bottom wafer. After that, TSV holes and electrical probing trench were etched. On the other hand, bottom graphene electrodes were patterned on a graphene wafer, followed by the catalyst patterning and deposition on the graphene electrodes. The top and bottom wafers were then bonded, followed by the removal of top handling wafer and buried oxide layer of the SOI to expose the underlying TSV holes. Finally, CNT growth was carried out within the TSVs using TCVD technique.

Figure 4.1 Schematic illustration of the fabrication process flow of CNT growth within TSVs on the bottom graphene electrodes.

4.4 Top-wafer Process: TSV holes Fabrication

Process flow for the fabrication of TSVs starts with a bulk, 6" diameter silicon-on-insulator (SOI) wafer. The thicknesses of device layer, buried oxide layer and supportive handling wafer of the SOI are 20 μm , 1 μm and 600 μm , respectively. Channel area, which is designed to leave a space to accommodate graphene and catalyst layers on the bottom wafer, was patterned on the device layer of SOI. The channel area was patterned by means of lithographic techniques: spin-coating (S1813 positive photoresist), exposure (Karl Suss MA-6, Double Side Aligner) and standard developer were used for the patterning. Reactive-ion-etching (RIE) system (Oxford Plasmalab-80) was used to etch 50nm depth Si trenches for the channel area. After that,

the probing trench and circular holes of desired parameters were patterned using the abovementioned lithographic method. The designed diameters of TSVs vary from 5-50 μm . Deep-Reactive-Ion-etching (DRIE) system (SAMCO's RIE-800iPB) was used to form 20 μm deep TSV holes through the device layer till the buried oxide stop, via the widely-used BOSCH process. After removing the photoresist hard-mask, the full wafer was sent into the furnace for thermal oxidation in order to form an oxide layer ($\sim 100\text{nm}$) on the sidewall of TSVs for electrical insulation. The full wafer was then diced into small dies with 10mm x 10mm dimension. Figure 4.2 shows the SEM results of the fabricated TSVs with 5, 15 and 50 μm diameters. As shown in the SEM images, the vias exhibit straight sidewalls without much over-etching at the bottom of the TSVs. Here, vias of different diameters were fabricated through to the buried oxide etch-stop, with a highest aspect ratio of ~ 4 for 5 μm diameter.

Figure 4.2 SEM images of the cross-section of TSVs with (a) 5, (b) 15 and (c) 50 μm diameters (depths are all 20 μm).

4.5 Bottom-wafer Process: Graphene Patterning and Catalyst Deposition

Graphene wafers used in this chapter are purchased commercially, where 4" diameter silicon wafers (with SiO_2 470nm) are deposited with a 7cm x 7cm single-layer transferred graphene (Hangzhou Gelanfang Nanotechnology Co., Ltd). The full wafer was manually cleaved into small dies with 12mm x 12mm dimension before processing. The crystallinity of the original graphene wafers was carefully checked by

optical and Raman microscopy (Raman system: Witec Alpha 300R) prior to lithography processing. Standard lithography processes: spin-coating (AZ5214 positive photoresist), exposure (MJB4 Karl SUSS Mask Aligner) and developing were used for patterning of graphene as the bottom electrodes. O₂ plasma etching (1 min, 60 W, 20 sccm oxygen flow) was carried out in the RIE system (Oxford Plasmalab-80) to etch off exposed graphene area. The recipe of O₂ plasma etching was optimized to completely remove the graphene layer without over-etching to the SiO₂ underneath.

After graphene patterning, catalyst/barrier layer was deposited on the graphene electrodes using lift-off process. Negative photoresist (ma-N 1440) was used to pattern the area for catalyst/barrier layer deposition. 8 nm Al, 2 nm Al₂O₃, and 1.1 nm of Fe were sequentially deposited using e-beam evaporator at nominal vacuum of 5×10^{-6} mbar at low temperature (<80°C) conditions. Deposition speed was set around 0.1~0.2 Å/sec. The top thin Al/Al₂O₃ layer acts as an anti-diffusion barrier for the catalyst Fe during the high temperature process of the CNT growth, as mentioned in the previous chapters.

Figure 4.3 shows the optical images of the substrate after graphene patterning and catalyst deposition. No visible cracks/peeling-off of the graphene was observed after the lithography process. The crystallinity of graphene was also verified by Raman microscopy before and after lithography process, which shows no significant increase of I_D ($\sim 1350\text{cm}^{-1}$)/ I_G ($\sim 1580\text{cm}^{-1}$) peak ratio, i.e. no severe graphene degradation (Figure 4.4).

Figure 4.3 Optical images (with 5x, 20x and 50x magnification) after graphene patterning and catalyst deposition: long strips are patterned graphene electrodes and round circles are deposited catalyst/barrier layers.

Figure 4.4 Raman spectra images of the graphene before and after lithography process.

It is well-known that residue photoresists can adhere to the electrode surface after lithography process, resulting in severe interface contamination. In this work, the interface contamination due to the residue photoresists on the graphene electrodes can cause significant increasing in the contact resistance between the graphene and CNTs. Two methods commonly used in conventional semiconductor cleaning process: plasma cleaning or UV-ozone (UVO) treatment, may also be used to clean the graphene surface before catalyst deposition. On the other hand, the following wafer bonding process requires an activation step with the plasma or UVO treatment on the wafer surface for fusion bonding. Thus, the quality of graphene electrodes before/after

the wafer activation needs to be examined. In this work, Raman microscopy and atomic force microscopy (AFM) were used to investigate the effects of plasma cleaning and UVO treatment on the graphene.

The results of Ar plasma and UVO treatment for graphene samples are shown in Table 4.1. Graphene layer was completely etched off after 5s Ar plasma treatment, possibly due to the “aggressive” nature of Ar plasma towards graphene layer. On the other hand, UVO treatment (in Jelight UVO Cleaner) was much “gentler”. No severe degradation of the graphene layer after UVO treatment of up to 6 min (Figure 4.5). Thus, it can be preliminarily concluded that UVO treatment is more suitable for graphene surface cleaning after lithography and the activation of wafer bonding, as compared to Ar plasma treatment.

Table 4.1 Ar plasma and UV-ozone treatment for graphene samples.

Methods	Conditions	Results
Ar plasma	50W, 5 sec	X (graphene etched-off)
	30W, 5 sec	X (graphene etched-off)
UV-Ozone	30W, 3 min	√ (no severe degrades)
	30W, 6 min	√ (no severe degrades)

Figure 4.5 Raman spectra images of graphene before UVO treatment, after 3min and after 6 min UVO treatment.

Figure 4.6 shows the topography images of (a) pristine graphene layer, (b) graphene layer after lithography process and (c) patterned graphene layer after 3min UVO treatment. The graphene's root mean square (RMS) of the surface roughness increased from 1.28 nm (Figure 4.6(a)) to 4.41 nm (Figure 4.6(b)) and subsequently decreases to 3.45 nm (Figure 4.6(c)). The pristine graphene shows a RMS of 1.28 nm possibly due to PMMA residue after the graphene transfer process. Poly methyl-methacrylate (PMMA) layer is commonly used as a polymer support layer during the mechanical transfer process of the graphene onto the Si wafer, and will be removed at the end of the transfer process. Similar to photoresist residue, PMMA cannot be thoroughly removed with solvents and a thin residue layer will usually be found on the graphene surface. After lithography process, the increasing of roughness can be attributed to the resists residue present on the graphene surface. The surface appears smoother after 3 min UVO cleanness and the RMS decreased ~ 1 nm, indicating effective removal of resist residuals by UVO cleaning.

Figure 4.6 AFM topography images (top-row 3D and bottom-row 2D) of $10\mu\text{m} \times 10\mu\text{m}$ area of a) pristine graphene, b) graphene after lithography and c) graphene after lithography following a 3min UVO treatment.

4.6 Die-to-Die Wafer Bonding and Exposure of TSV holes

The two wafers, top TSV die and bottom graphene die, are then bonded face-to-face in a die-to-die bonder machine (FINEPLACER® matrix) by top-side alignment marks at normal temperature and atmospheric condition using the fusion bonding approach. 6 min UVO treatment was used as the activation step for bonding process without damaging the bottom graphene electrodes. Two dies were successfully bonded with good bonding strength. In order to expose the underlying TSV holes for CNT growth, the handling wafer and buried oxide layer of the top SOI wafer needs to be removed. However, the thickness of the handling wafer is too thick ($\sim 600\mu\text{m}$) to be removed by conventional micro-fabrication techniques. To remove wafer of such thickness, grinding process is usually used, but the process is not suitable for small die ($10\text{mm} \times 10\text{mm}$) samples. Since limited grips are anticipated on the die during the grinding process, the risk of die dislodging, damaged/missing during the process is significant. On the other hand, KOH wet etching is an alternative method for wafer removal. But the practical etching rate of Si in KOH solution is $\sim 60\mu\text{m}/\text{hour}$ in 80°C 20% KOH solution, which means that it will take ~ 10 hours to etch-off all the $600\mu\text{m}$ silicon and not practical for large-scale, seamless fabrication.

Nevertheless, a trial process was done to remove the handling wafer by manually grinding ($300\sim 400\mu\text{m}$ depth) following a KOH wet etching ($200\sim 300\mu\text{m}$ depth). After that, the exposed buried oxide was removed by RIE. Figure 4.7 shows the pictures of a die after the grinding and KOH etching process which, where the remaining buried oxide layer is not uniform. From the optical images, it can be seen that holes at the perimeter area (Figure 4.7(a)) were over-etched by KOH, where the over-etching is not found at TSVs in the middle portion of the die (Figure 4.7(b)). After buried oxide removal, it can be seen that there are some color changes in via

holes at different regions of the die (Figure 4.8). For example, TSVs at the ‘top left’ and ‘bottom left’ regions are green (i.e. the color of original 550nm SiO₂) and purple (i.e. ~450nm SiO₂) at the ‘top right’ region. This phenomenon occurs as manual grinding process will generally produce low surface uniformity throughout the whole die. The remaining Si thickness at the ‘top right’ region was thinner than the ‘top left’ or ‘bottom left’ regions. Due to the uneven Si thickness after grinding, the remaining Si at the ‘top right’ region was completely etched-off, leading to the over-etching of underlying buried oxide. Meanwhile, the Si layer at the ‘top left’ and ‘bottom left’ regions is still under-etched. Thus, the exposed buried oxide has thinner thickness at the ‘top right’ region as compared to ‘top left’ and ‘bottom left’ regions. Eventually, when RIE was applied to remove the buried oxide for via holes open, the ‘top right’ region was over-etched down to the bottom oxide layer of bonded wafer, resulting in the color changes of TSVs.

Figure 4.7 Optical images after the handling wafer removal: TSV holes (a) at the perimeter area and (b) in the middle portion of the die; (c) photo of a real sample after the grinding and KOH etching process.

Figure 4.8 Optical images after the handling wafer and buried oxide removal: exposed TSVs at (a) top left, (b) top right, (c) bottom left and (d) bottom right region of the die.

4.7 CNT Growth within TSVs

After opening of TSV holes, the whole die was transferred into the Axitron Black Magic System for vertical-aligned multi-wall carbon nanotubes (MWCNTs) growth under the thermal CVD (TCVD) mode with hydrogen (H_2) and acetylene (C_2H_2) gas flows. Pre-growth and CNT growth were set at 600/700°C with 30sec/30min, respectively. C_2H_2 and H_2 gas flows during the CNT growth were set as 200/600 sccm respectively. On the other hand, a sample of bottom die which has undergone graphene patterning and catalyst deposition process (similar conditions as mentioned in Chapter 3) was used for comparison.

As shown in Figure 4.9, we can see that CNT growth was inhibited and severely affected within the unfilled TSV (20 μ m diameter) despite that the growth

duration was six times longer than that for the free-standing CNT growth. This drastic reduction in growth of CNTs can be attributed to the process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. 1) Ar plasma activation of the bonding process and over etching of the buried oxide by RIE can possibly etch off the thin layer of catalyst, which leads to sparsely-grown, non-visible CNTs. 2) Bonding and grinding process can possibly shift the top TSV die resulting in a large misalignment between via holes and patterned bottom catalyst, leading to the partially filling of CNTs in TSV (Figure 4.9(a) and (b)). 3) Over-etching of the buried oxide by KOH solution may damage the catalyst or spread the catalyst particles on sidewall or on the top surface of TSVs, leading to scattered CNT growth (Figure 4.9(c) and (d)). Hence, it is reasonable that the CNT growth was quite restricted within the TSV after these process-engineering steps.

Figure 4.9 SEM images for CNT growth within TSV: (a) 3 out of 6 via holes have CNTs grown but none was completely filled by CNTs; (b) a shift of top die leading to the partially filling of CNTs in the via, inserted figure is a Raman image of CNTs as-grown; the scattered CNT grown on (c) sidewall and (d) top surface of TSV.

4.8 Summary

In this chapter, fabrication process flow of graphene-CNT heterostructure within TSVs was designed and explored. As compared to the free-standing growth of CNTs on the graphene, CNTs grown within the unfilled TSV holes are relatively sparse owing to the process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. Process steps of TSV fabrication for CNT growth shall be modified and optimized in order to improve the CNT fillings within the unfilled TSVs. On the other hand, in order to form a complete full-carbon 3-D interconnection, the assembly process of the top graphene layer after CNT growth needs to be explored, which will be further discussed in the following chapters.

Chapter 5 : Process Exploration of Transferring a Top-Graphene Layer onto CNTs

5.1 Introduction

In Chapter 4, direct growth of CNTs within TSVs on the bottom graphene electrodes has been demonstrated. In order to form a complete full-carbon 3-D interconnection, the assembly process of the top graphene layer after CNT growth needs to be explored. The assembly process includes: (1) transferring a top-graphene layer onto the as-grown CNTs and (2) fusion of transferred graphene and CNTs to enhance the conductivity and reliability of the graphene/CNT contact. Process (1) will be explored in this chapter and Chapter 6, while process (2) will be explored in Chapter 7.

5.2 Experimental Objective and Scope

This chapter aims to explore the process of transferring a top-graphene layer onto the CNTs for the formation of CNT-graphene heterostructure, and to study the electrical properties of the fabricated structure. Three test structures (i.e. single-side step structure, double-step structure and bridge structure) were designed and fabricated for CNT growth and top-graphene layer transfer. Meanwhile, three transferring methods of graphene layer (i.e. direct dry transfer, dry transfer with a thermal tape and wet transfer) were explored using the single-side step structure after CNT growth. From the electrical results, the best test structure and transferring method will be selected and optimized for the electrical characterizations of direct graphene-to-CNT contact in the next chapter.

5.3 Design and Fabrication of the Test Structures for Electrical Study

To investigate the electrical properties of the top-graphene layer transferred on the CNTs, a single-side step structure was initially designed for preliminary researches. Figure 5.1 illustrates the proposed structure and fabrication process flow. First, a $\sim 100\ \mu\text{m}$ depth step was etched in the silicon substrate using DRIE dry etching or KOH wet etching techniques as shown in Figure 5.1(a)-(c). After that, the remaining SiO_2 was etched off using buffered oxide etching (BOE) (Figure 5.1(d)) followed by $\sim 280\ \text{nm}$ thermal oxide growth (Figure 5.1(e)) to form an insulation layer from the conductive Si substrate. After that, 20nm Ti/100nm Au electrodes were deposited on both lower and higher side of the step followed the deposition of barrier/catalyst layer (8nm Al/2nm Al_2O_3 /1.1nm Fe) only on the lower side of the step, as shown in Figure 5.1(f). CNT growth was carried out and the growth recipe was tuned to obtain CNTs of similar heights with the step (Figure 5.1(g)). A layer of graphene will then be transferred on top of CNTs and the Au electrode on the unetched silicon surface (Figure 5.1(h)). Two or Four-point-probe (2PP/4PP) I-V measurements will be used for the electrical characterizations of this fabricated step structure.

Figure 5.1 (a)-(g) Fabrication process flow of the single-side step structure and (h) a top-graphene layer transferred on CNTs after CNT growth.

Figure 5.2 shows the SEM images of the samples after CNT growth in the steps etched by (a) KOH wet etching and (b) DRIE dry etching, respectively. The height of CNT growth was fine-tuned to be similar to the depth the step. However, from Figure 5.2, it can be observed that KOH-etched step exhibits a 54.7° sloped sidewall due to the anisotropic nature of KOH etching. As a result, a large gap existed between the top of vertical-aligned CNTs and the edge of the step. CNTs grown in KOH-etch step also exhibit uneven heights, as shown in Figure 5.2(a). On the other hand, the vertical sidewalls are observed on the DRIE-etched step, with smaller gaps between the CNTs and the edge of the step, with CNTs heights of high uniformity. Thus, DRIE is chosen as the preferred method for the fabrication of the step structure.

Figure 5.2 SEM images of the samples after CNT growth with the steps etched by (a) KOH wet etching and (b) DRIE.

With the single-side step structure, the graphene layer was successfully transferred on the top of CNTs and preliminary I-V results of the fabricated structure were obtained. However, there were some questionable issues which require further investigation and verifications. The details of these will be discussed in the following section. At the same time, to further characterize the electrical properties of the graphene layer transferred on CNTs, double-side step structure and bridge structure were designed.

Figure 5.3 illustrates the fabrication process flow of double-side step structure with a top-graphene layer transferred on grown CNTs. The advantages of double-side step structure include: (1) avoid the possibility of sidewall shortage; (2) symmetry structure with more flattened graphene contact to the CNTs; (3) I-V measurement result of Au-graphene-Au can be obtained from the structure to calculate the CNT bump resistance ($R_{Au-CNT-G}$). The possible underlying issues of double-side step structure and the associated feasibility in resolving them will be discussed in the following section.

Figure 5.3 (a)-(g) Fabrication process flow of the double-side step structure and (h) a top-graphene layer transferred on CNTs after CNT growth.

The bridge structure illustrated in Figure 5.4 is an optimization of the double-side step structure. The two steps in the bridge structure are only used for the supports for free-standing CNTs and the top Au electrodes on the steps are eliminated. A gap is present between two bottom Au electrodes to facilitate the probing and electrical characterizations of the Au-CNT-graphene-CNT-Au structure after graphene transfer. Large, uncertain contact resistances between the transferred graphene and Au electrodes in the double-side step structure can be avoided in the bridge structure (details will be discussed in the following section).

Figure 5.4 Top-view and side-view illustrations of the bridge structure (a) before and (b) after graphene transfer with the thermal tape.

5.4 Transferring Methods of Graphene Layer

Graphene samples used in this chapter were intrinsic CVD graphene grown on the Cu foil with a Polymethyl methacrylate (PMMA) layer coated on the top of graphene. The “float graphene” samples are made by etching off the Cu foil and transferring the PMMA/graphene layer on the top of sandpaper with a dimension of 10mm × 10mm for delivery (supplied by Hangzhou Gelanfeng Nanotechnology Co., Ltd). Thus, the “float graphene” can be directly peeled off, i.e. the PMMA/graphene layer (as shown in Figure 5.5(a)), from the sandpaper for the following transfer process. Different colors can be observed in Figure 5.5(a) due the non-uniform PMMA layer and the grain boundaries of poly crystal graphene, which was also observed in Figure 5.5(a). Raman characterization indicates that the obtained graphene is a single layer graphene as shown in Figure 5.5(b).

Figure 5.5 (a) Optical and (b) Raman images of the “float graphene” (PMMA/graphene layer).

Three transferring methods of graphene layer were proposed and conducted in this section. The single-side step structure after CNT growth was used for the trials of transfer processes. Figure 5.6 shows the optical and SEM images after different graphene transfer processes. The first method is direct dry transfer. The PMMA/graphene layer was peeled off from the sandpaper and then directly placed on the top of CNTs. After the transfer process, the graphene layer was mechanically pressed down onto the CNTs to make a better contact between the graphene and CNTs. From Figure 5.6(a), it can be observed that PMMA/graphene layer was creased after the transfer process. The PMMA/graphene layer is not flatten with visible wrinkles, making it highly susceptible to breaking and damaging as the PMMA/graphene layer is extremely thin and fragile. An improved method is to perform the dry transfer process with a thermal tape. The thermal tape increased the stiffness of the PMMA/graphene layer to obtain more flattened layer wrinkles, which may be potential break point of the layer (Figure 5.6(b)). The third method is wet transfer in the DI water. First, the PMMA/graphene layer was peeled off from the sandpaper and allowed to float on the DI water. After that, the single-side step structure with the CNT growth was dipped into the water, tilted 45° to fish the PMMA/graphene layer out.

Figure 5.6(c) shows the result after the wet transfer process. It can be observed that most CNTs collapsed after dipping into DI water except CNTs located around the step region, where the CNT heights are shorter compared to other growth regions. Despite obtaining flattened graphene was flattened at the edge of the step, no physical contact was established with the CNTs around the edge of the step because CNT lengths around the region were too short and insufficient to form physical contact. From the comparisons of the three transferring methods, dry transfer technique with the thermal tape is chosen as the primary technique for graphene transfer.

Figure 5.6 Optical and SEM images after three different graphene transfer processes: (a) direct dry transfer, (b) dry transfer with a thermal tape and (c) wet transfer in the DI water.

5.5 Results and Discussion

Figure 5.7(a) and (b) show the SEM images of the single-side step structure before and after graphene direct dry transfer. The electrical characterization results of 2PP I-V measurements (Keithley 4200-SCS Semiconductor Characterization System) between Au electrodes on the lower side and the higher side of the step before and

after graphene transfer were shown in Figure 5.7(c) and (d). After the graphene layer was transferred and mechanically pressed onto the CNTs, a linear response of the current was obtained when the voltage sweep ranged from -1 to 1V. The resistance of the structure was lowered down from 522 k Ω to 5.74 k Ω after graphene transfer and mechanical press. To rule out other contradicting factors, any possibilities of short circuiting need to be carefully examined and ruled out. There are two possible short passes in the single-side step structure. First possibility is the sidewall shortage as shown in Figure 5.8(a). As Au electrodes, barrier/catalyst layers are primarily deposited using anisotropic e-beam evaporation deposition technique, the possibility of metal deposition on the vertical sidewalls is rather low. However, possible sidewall deposition should not be neglect as the sidewall was not completely 90° vertical with anticipatedly rough surface by DRIE, as shown in Figure 5.8(b). Second possibility is that the shortage can also happen when the transferred graphene touched the bottom Au electrode on the bottom of the step after mechanical pressing. This possibility might happen as the free-standing CNTs grown on the lower side of the step can collapse when there no mechanical support is present to sustain the pressure. On the other hand, even if the short circuits can be assumed to be excluded, with the measured value being the total resistance of Au-CNT-graphene-Au, it is still not able to isolate the CNT bump resistance ($R_{Au-CNT-G}$) from the total resistance as the contact resistance between transferred graphene and Au electrode was unknown. Thus, the single-side step structure was improved by the double-side step structure to exclude the possibilities of short circuits, and to further characterize the electrical properties of the graphene transferred on CNTs.

Figure 5.7 SEM images of the single-side step structure (a) before and (b) after graphene direct dry transfer; (c) illustrations and (d) results of 2PP I-V measurements between Au electrodes on the lower side and the higher side of the step before and after graphene transfer.

Figure 5.8 (a) Sidewall shortage in the single-side step structure and (b) SEM images of the sidewall $> 90^\circ$ with rough surface

Figure 5.9 (a) and (b) show the tilted-view and side-view SEM images of the double-side step structure after CNT growth. It can be observed that the CNT length in the middle area ($\sim$ avg. $10\ \mu\text{m}$) was too short to reach the height of the step ($\sim 70\ \mu\text{m}$). This can be attributed to the inhibited the gas flow in the trench between two steps which affects the grown length of CNTs. After CNT growth, a graphene layer was transferred using the dry transfer with a thermal tape, and mechanically pressed to make a better contact between the transferred graphene and CNTs, as shown in Figure 5.10. Large gaps can be observed between the bottom Au electrode with CNTs grown on the top and the sidewalls of two steps, indicating that the possible shortages between the bottom Au electrode/CNTs and the top Au electrodes on two steps can be

omitted. Figure 5.11(a) and (b) show the illustrations and results of 4PP I-V measurements before and after the graphene transfer. Top electrode A to B, top electrode A to bottom electrode C and bottom electrode C to top electrode B were probed correspondingly. I-V measurement of two top electrodes A to B (i.e. Au-graphene-Au) shows the linear response to the current when the voltage sweep was applied, indicating that ohmic contact was achieved between the graphene and Au electrodes. However, the collapse of free-standing CNTs can still happen when mechanical pressure is applied after the graphene transfer. Since the CNT length was much shorter than the height of two steps, the steps are unable to serve as the mechanical supports. Thus, the shortage between the graphene and the bottom Au electrode is still possible in the double-side step structure.

Assuming the short circuits can be excluded, the total resistances of three measurements can be expressed as:

$$R_{G/Au(A)} + R_G(\text{left}) + R_{G/CNT} + R_{CNT} + R_{CNT/Au} \approx 2.87k\Omega \quad (1)$$

$$R_{G/Au(B)} + R_G(\text{right}) + R_{G/CNT} + R_{CNT} + R_{CNT/Au} \approx 4.55k\Omega \quad (2)$$

$$R_{G/Au(A)} + R_G(\text{left}) + R_G(\text{right}) + R_{G/Au(B)} \approx 7.30k\Omega \quad (3)$$

where $R_{G/Au(A)}$ is the contact resistance between graphene and Au electrode A, $R_{G/Au(B)}$ is the contact resistance between graphene and Au electrode B; $R_G(\text{left})$ is the left half of the graphene resistance, $R_G(\text{right})$ is the right half of the graphene resistance; $R_{G/CNT}$ is the graphene/CNT contact resistance, R_{CNT} is the resistance of bulk CNT and $R_{CNT/Au}$ is the CNT/Au contact resistance. The resistance of one CNT bump $R_{Au-CNT-G} = R_{G/CNT} + R_{CNT} + R_{CNT/Au}$, which can be calculated by $[(1) + (2) - (3)]/2 = 60\Omega$. First, we can conclude that the total resistance of Au-graphene-Au was large ($\sim 7.30k\Omega$), which may be due to the poor contacts between the transferred graphene and Au electrodes and/or the large resistance of graphene. Secondly, the

actual contact area between the transferred graphene and CNTs was unknown since an air-gap existed after graphene transfer, as shown in Figure 5.10. Finally, the calculated resistance of one CNT bump ($R_{Au-CNT-G}$) is small and immiscible with the background noise. Thus, the large uncertain contact resistances between the transferred graphene and Au electrodes should be avoided.

Figure 5.9 (a) Tilted-view and (b) side-view SEM images of the double-side step structure after CNT growth

Figure 5.10 Optical image of the double-side step structure after graphene dry transfer with the thermal tape on to the CNTs

Figure 5.11 (a) Illustrations and (b) results of 4PP I-V measurements of the double-side step structure before and after the graphene transfer.

The bridge structure is an optimized design based on the double-side step structure where the electrical properties of the Au-CNT-graphene-CNT-Au can be directly probed after graphene transfer. Figure 5.12(a) and (b) show the SEM images of the bridge structure before and after graphene dry transfer with the thermal tape. Similar to the double-side step structure, the grown length of CNTs was short and non-uniform at the middle region of the trench while the length was much longer at the edges, attributing to the inhibition of gas flow in the middle region of the trench. The optical image after the graphene layer is transferred and mechanically pressed onto the CNTs is shown in Figure 5.13. The gap (~ 0.5 mm) between two bottom Au electrodes

with CNTs grown on the top can be observed, suggesting that no shortage is present between two bottom Au electrodes (or two CNT bundles). The illustrations and results of 4PP I-V measurements of the bridge structure before and after graphene transfer were shown in Figure 5.14(a) and (b). After graphene transfer, the structure shows a linear response to the current when the voltage sweep (-1 to 1V) was applied. However, since the free-standing CNTs grown in the trench was too short, similar to the double-side step structure, the collapse of CNTs may also happen, leading to the shortage between the graphene and the bottom Au electrodes. The measured total resistance shows a small value (174Ω) since the large contact resistances between the transferred graphene and Au electrodes were omitted in the bridge structure. However, the actual contact area between the transferred graphene and CNTs was still unknown due to the existing air-gap between the transferred graphene and CNTs, as shown in Figure 5.13. Besides, to isolate the resistance of one CNT bump ($R_{Au-CNT-G}$) from the total resistance, the graphene resistance needs to be estimated. Further optimization of the bridge structure will be described in Chapter 6.

Figure 5.12 SEM images of the bridge structure (a) before and (b) after graphene dry transfer with the thermal tape.

Figure 5.13 Optical image of the bridge structure after the graphene layer transferred and pressed down on to the CNTs.

Figure 5.14 (a) Illustrations and (b) results of 4PP I-V measurements of the bridge structure before and after the graphene transfer.

5.6 Summary

In this chapter, the process of transferring a top-graphene layer onto the CNTs was explored and the electrical properties of the fabricated structures were studied. Using the bridge structure and graphene dry transfer with a thermal tape, the electrical properties of the Au-CNT-graphene-CNT-Au structure can be directly probed. The electrical characterization shows a linear response to the current when the voltage sweep (-1 to 1V) was applied after graphene transferred. At the same time, the total resistance of Au-CNT-graphene-CNT-Au was calculated as 174Ω . The optimization of the bridge structure is required to further investigate the electrical properties of direct graphene-to-CNT contact.

Chapter 6 : Electrical Properties of Direct Graphene-to-CNT Contact

6.1 Introduction

In Chapter 5, the process of transferring a top-graphene layer onto the CNTs using the bridge structure, and graphene dry transfer with a thermal tape has been explored. However, further process improvement is required due to some remaining issues. (1) The shortage between the graphene and the bottom Au electrodes was still possible as the free-standing CNTs grown in the trench was too short, making CNTs susceptible to collision upon graphene transfer and mechanical pressing. (2) The actual contact area between the transferred graphene and CNTs was still unknown due to the presence of an air-gap between the transferred graphene and CNTs. (3) The graphene resistance needs to be estimated to isolate the resistance of one CNT bump ($R_{Au-CNT-G}$) from the total resistance of the bridge structure.

6.2 Experimental Objective and Scope

This chapter aims to improve the bridge structure and graphene transferring process to further investigate the electrical properties of direct graphene-to-CNT contact. The resistance of one CNT bump ($R_{Au-CNT-G}$), including the CNT/graphene contact resistance, will be extracted from the total resistance of the graphene bridge structure to benchmark with the $R_{Au-CNT-Au}$, which include the CNT/Au contact resistance in the Au bridge structure. The resistance of one CNT bump ($R_{Au-CNT-G}$) will be compared with the state-of-the-art studies on similar work.

6.3 Design and Fabrication of the Graphene Bridge Structure

Major fabrication and assembly steps of the Au-CNT-graphene-CNT-Au structure are summarized in Figure 6.1. The fabrication uses Si substrate with 280 nm SiO₂ layer deposited using thermal oxidation technique (Figure 6.1, step 1). First, bottom Au pads (20nm Ti/100nm Au) and buffer/catalyst layer (8nm Al/2nm

Al₂O₃/1.1nm Fe) were sequentially patterned on a silicon wafer using e-beam evaporation deposition and lift-off process (Figure 6.1, step 2). Then, free-standing CNTs were grown using thermal chemical vapour deposition (TCVD) method with hydrogen (H₂) and acetylene (C₂H₂) gas flow ratio of 3:1 at 650°C (Figure 6.1, step 3). After CNT growth, two pieces of 80µm thickness polyethylene terephthalate (PET) with double-side non-conducting adhesives were assembled on the sides of CNT bundles as the spacers to support the free-standing CNTs when the top graphene layer was transferred (Figure 6.1, step 4). Finally, few-layer graphene on PET (or SiO₂/Si) substrate was flipped over and pressed down onto the CNT bundles (Figure 6.1, step 5). Graphene with the substrate was attached by the mechanical force of the top adhesive of PET spacers, creating direct contact between the graphene and CNTs (Figure 6.1, step 6).

Figure 6.1 Fabrication and assembly steps of the Au-CNT-graphene-CNT-Au structure.

6.4 Electrical Characterization Method

The high contact resistance between CNTs and metal is always a key obstacle in limiting their feasibility in the CNT interconnect application [51]. However, significant discrepancies are present in the state-of-the-art values of CNT/metal contact resistance, and there are no standard processes for the estimation. Different groups presented their results with various measurement techniques and assumptions on various samples. In this work, Au film (with SiO₂/Si substrate) replaced the graphene layer as the control sample when CNT growth conditions and assembly processes remained to be identical. Four-point-probe (4PP) I-V measurements (Keithley 4200-SCS Semiconductor Characterization System) were used to characterize the electrical properties of the graphene and Au bridge structure. The total resistance of the graphene and Au bridge structure can be expressed as:

$$R_{total} = R_{btm_Au} + 2R_{Au-CNT-G} + R_G \quad (1)$$

and

$$R_{total} = R_{btm_Au} + 2R_{Au-CNT-Au} + R_{top_Au} \quad (2), \text{ correspondingly,}$$

where R_{btm_Au} is the resistance of bottom Au pads; $R_{Au-CNT-G}$ and $R_{Au-CNT-Au}$ are the resistance of one CNT bump including the contact resistance of CNT/bottom Au, the resistance of bulk CNT and the contact resistance of CNT/graphene or CNT/top Au; R_G and R_{top_Au} are the resistance of top graphene layer and Au film, correspondingly.

To extract the $R_{Au-CNT-G}$ and $R_{Au-CNT-Au}$ in Equation (1) and (2), the values of R_{btm_Au} , R_G and R_{top_Au} need to be determined. R_{btm_Au} can be measured from the control groups with the same dimension of bottom Au pads. R_G and R_{top_Au} can be estimated using the equation of $R = \frac{L}{w_{eff}} R_S$ (3), where L is the distance between two

CNT bundles; W_{eff} is the effective width of top graphene layer or Au film; R_S is the sheet resistance of the graphene layer or Au film. Nevertheless, to utilize Eq. (1) and (2), CNT resistance needs to be subtracted. Using the reported CNT resistivity of 9.7 to 33.8 m Ω •cm [51], [53], CNT resistance can be determined using Ohm's law. However, the calculation is carried out based on the assumptions where the current density distribution and the crystallinity across the whole CNT bundles are similar. In actual CNT growth, discrepancies in crystallinity and current density across various regions of CNT bundles can be anticipated. Nevertheless, in this work, the overall electrical properties of CNT bundles are taken into consideration to explore the feasibility of CNT-graphene heterostructure in TSV interconnect applications.

6.5 Results and Discussion

Graphene samples on substrate used in this chapter were intrinsic CVD graphene transferred on the top of PET (or 350nm SiO₂/Si wafer) with a dimension of 10mm $\times$ 10mm. The structural characteristics of graphene were confirmed by optical microscopy and Raman characterization as 1-3 layers poly-crystal graphene (Figure 6.2). On the other hand, 20nm Ti/100nm Au was deposited by e-beam evaporator on 280nm SiO₂/Si wafer to be used as the control samples to benchmark against the graphene samples. The sheet resistances of graphene layer and Au film were in a range of 218-237 and 0.31-0.32 Ω /sq, respectively, measured by 4PP sheet resistance measurement machine. Large sheet resistance of graphene may be attributed to the grain boundaries of poly-crystal formed during the CVD growth, and the defects or deformations induced from the transfer process of micro-scale area onto the substrate. Based on Equation (3), R_G will be ~ 730 times larger than R_{top_Au} with the same dimension (L/W_{eff}), leading to a significant increase of the total resistance of the graphene bridge structure. To reduce the effect of R_G , another configuration of CNT

area (Figure 6.3, configuration A) with much smaller distance (L) between two CNT bundles was designed as a comparison to the regular square-shaped CNT area Figure 6.3, configuration B). The size of CNT area in configuration A and B was maintained at the same value.

Figure 6.2 (a) Optical and (b) Raman images of the graphene on SiO₂/Si and PET.

Figure 6.3 Schematic diagrams and SEM images of two configurations of CNT area with the same size (left: configuration A, right: configuration B).

Optical microscopy (OM) and scanning electron microscopy (SEM) images of the fabricated Au-CNT-graphene-CNT-Au structure of configuration A are presented in Figure 6.4. As shown in Figure 6.4(a) and (b), two uniform, well-aligned CNT walls were grown on the top of bottom Au pads. Figure 6.4(c) and (d) show the direct contact of poly-crystal graphene with the observable grain boundaries to the CNTs. Meanwhile, a dummy sample in the same batch with the real sample after CNT growth was sliced to observe the cross-section view of two CNT walls in SEM, as shown in Figure 6.4(e) and (f). The vertical length of CNTs was controlled by the growth time to be slightly higher than the thickness of PET spacers (80 μm).

Figure 6.4 (a) and (b) SEM images after CNT growth; (c) and (d) optical images after top graphene layer transferred; (e) and (f) SEM cross-section view of two CNT walls of the dummy sample cut in half.

The vertical length of CNT walls on the dummy sample was directly measured from the cross-section SEM image as shown in Figure 6.5(a). The planar length of CNT walls on the same dummy sample measured from the tilted-view SEM was shown in Figure 6.5(b). From the tilted-view SEM image, the planar length of CNT walls on the real sample was measured (Figure 6.6) with good uniformity. Using the same ratio of the planar and vertical length of CNTs on the dummy sample, the vertical length of CNT walls on the real sample can be calculated to be 110 μm as shown in Table 6.1. The I_G/I_D peak ratio and average diameter of the CNTs was ~ 1.5 and ~ 3 nm correspondingly as shown in Figure 6.7(a) and (b). CNT density was estimated to be $\sim 10^{11} \text{ cm}^{-2}$, which is expectedly much higher than PECVD grown CNTs ($\sim 10^9 \text{ cm}^{-2}$) [126].

Figure 6.5 (a) Cross-section SEM image of the vertical length of CNT walls on the dummy sample and (b) the planar length of CNT walls on the same dummy sample from the top-view SEM image tilted at 20°.

Figure 6.6 The planar length of CNT walls on the real sample from the top-view SEM image tilted at 20°.

Table 6.1 The vertical and planar length of CNT walls on the dummy sample and real sample.

Sample	Vertical length (μm)	Planar length (μm)	Ratio of the planar and vertical length
Dummy sample	154	52	0.34
Real sample	110 (calculated)	37	0.34

Figure 6.7 (a) Raman and (b) transmission electron microscopy (TEM) images of the as-grown CNTs.

4PP I-V measurement result of the Au-CNT-graphene-CNT-Au structure of configuration A is displayed in Figure 6.8. It is shown that the current increases linearly under the voltage sweep ranging from -1 to 1V. Short circuit between two CNT walls or bottom Au pads were excluded by I-V measurement before graphene transfer. After the transfer of graphene onto the CNTs, the gap between two CNT walls remains rigid as shown in Figure 6.4 (c) and (d), suggesting the absence of current shortage between two walls after the graphene transfer. Ruling out all possible shortages, it can be postulated that ohmic contact was achieved between the graphene and CNTs.

I-V curves of the graphene and Au bridge structure with two configurations of

CNT area are shown in Figure 6.8. The Au bridge structure shows a linear response to the current when the voltage is applied, similar to its graphene bridge counterpart. However, its total resistance was smaller compared to the value of the graphene bridge structure with the same configuration of CNT area. It is mainly because R_G was much larger than R_{top_Au} as explained above. Meanwhile, for the graphene bridge structure, configuration A ($30\mu\text{m}\times 3\text{mm}$) with closer distance (L) between two CNT walls had much smaller total resistance than the value of configuration B ($300\mu\text{m}\times 300\mu\text{m}$) as expected also due to the large R_G in configuration B. Figure 6.9 shows the SEM images of cross-section view of the graphene bridge structure (SiO_2/Si) with CNT area in configuration B, indicating that there was no shortage between the graphene and the bottom Au pads.

Figure 6.8 4pp I-V measurement results of the total resistance of the graphene and Au bridge structure with two configurations of CNT area.

Figure 6.9 SEM images of cross-section view of the graphene bridge structure (SiO₂/Si substrate) with CNT area in configuration B.

The measured values of R_{btm_Au} and estimated values of R_G and R_{top_Au} for various CNT area and graphene layer dimensions are listed in Table 6.3. R_G and R_{top_Au} can be estimated using the Equation (3): $R = \frac{L}{W_{eff}} R_S$, where L is the distance between two CNT bundles; W_{eff} is the effective width of top graphene layer or Au film; R_S is the sheet resistance of the graphene layer or Au film. Based on two configurations of CNT area and the physical width (W) of the graphene layer or Au film, as shown in Figure 6.3 and Table 6.3, we can conclude that

- 1) For the CNT area with configuration A, $W_{eff} \approx W$ since the width b of CNT area (3mm) is close to W (3.6 or 4.5mm) and the L (80µm) is much smaller compared to the value of b (3mm);
- 2) For the CNT area with configuration B, $W_{eff} < W$ since the width b of CNT area (300µm) is much smaller than W (4.2 or 3.4mm) and the L (770 or 610µm) is larger than the value of b (300µm).

For the CNT area with configuration B, W_{eff} can be determined by transfer length method (TLM) with two Cu electrodes replacing the two CNT bundles on the top of Au film with sample size of 5mm × 10mm, as shown in Figure 6.10. The total resistance between two Cu electrodes can be expressed as

$$R_{total} = 2(R_{Cu/Au} + R_{Cu}) + \frac{R_S}{W_{eff}} L_{Cu} \quad ,$$

where $R_{Cu/Au}$ and R_{Cu} are the contact resistance between Cu and Au and the bulk resistance of one Cu electrode, correspondingly; R_S is the sheet resistance of Au film; L_{Cu} is the distance between two Cu electrodes. By varying the distance between two Cu electrodes, the total resistance vs. L_{Cu} will have a linear response. The slope equals to R_S/W_{eff} .

Figure 6.11 shows the optical images of patterned two Cu electrodes on the Au film with three different values of L_{Cu} . Table 6.2 shows the 4PP I-V measured total resistances of different L_{Cu} from three batches of samples. Figure 6.12 plots the linear response of the total resistance vs. L_{Cu} with a slope of 194.3 mΩ/mm. R_S of Au film was measured to be 313 mΩ by 4PP sheet resistance measurement machine. Subsequently, W_{eff} was calculated to be 1.6 mm (applicable for L within the range of 396-794 μm).

Figure 6.10 Illustration of two Cu electrodes replacing the two CNT bundles on the top of Au film.

Figure 6.11 Optical images of patterned two Cu electrodes on the Au film with three different values of L_{Cu}

Figure 6.12 The linear response of the total resistance vs. L_{Cu} .

Table 6.2 4PP I-V measured total resistances of different L_{Cu} from three batches of samples.

L_{Cu} (mm)	Resistance (mΩ)		
	Batch 1	Batch 2	Batch 3
0.396	104	113	113
0.594	154	156	152
0.794	186	190	193

Table 6.3 Total and extracted one CNT bump resistance of the graphene and Au bridge structure with two configurations of CNT area.

Configuration	W (mm)	L (mm)	CNT area			R_{total} (Ω)	$R_{btm,Au}$ (Ω)	$R_{top,Au}$ (Ω)	R_G (Ω)	$R_{Au-CNT-G}$ or $R_{Au-CNT-Au}$ (Ω)
			a (mm)	b (mm)	S (mm^2)					
A with graphene bridge (PET)	3.6	0.08	0.03	2.95	0.09	10.0	0.7	/	5.1	2.1
A with Au bridge (SiO ₂ /Si)	4.5	0.08	0.03	2.96	0.09	5.2	0.7	0.01	/	2.2
B with graphene bridge (SiO ₂ /Si)	4.2	0.77	0.28	0.28	0.08	128.1	7.0	/	110.7	5.2
B with Au bridge (SiO ₂ /Si)	3.4	0.61	0.30	0.30	0.09	18.2	7.0	0.12	/	5.5

$R_{Au-CNT-G}$ and $R_{Au-CNT-Au}$ are extracted from Equation (1) and (2) as shown in Table 6.3. Under the same configuration, $R_{Au-CNT-G}$ was similar to $R_{Au-CNT-Au}$ suggesting that similar contact was formed at the CNT/graphene interface and at the CNT/top Au interface. The contact between CNTs and graphene can be possibly achieved by the Van der Waals forces as the current density ($\ll 10^8$ A/cm²) induced from I-V measurements is relatively insignificant to fuse the CNTs and graphene with covalent carbon bonds [127]. On the other hand, the contact resistance between CNTs and graphene was slightly smaller than the contact resistance between CNTs and Au. A possible reason for this can be attributed to the work function of graphene (4.6eV) which is closer to the value of CNTs (4.7~4.9eV at sidewalls, at tips it will be smaller [128]) as compared to Au (5.1eV), where the electron tunnelling was affected by the work function difference in this case. Under the identical CNT area, the contact resistances between CNTs and graphene (or between CNTs and Au) of configuration A and B were different. This shows that a non-uniform current density exists at the CNT/graphene (or CNT/Au) contact due to the current crowding effect [129]. The effective contact area of configuration A is larger than configuration B resulting in smaller contact resistance in configuration A. The Ohmic contact obtained aligns well

with the assumptions in using Eq. (1) and (2), as mentioned in the previous section. As Ohmic contact can be postulated, the contact resistance can be postulated to increase linearly with reduced contact area, as agreed by Ohm's law. In other words, a possible increase in contact resistance may be anticipated for miniaturized interconnects with smaller CNT-graphene contact area. However, in actual CNT-graphene interconnects, more uncertainties shall be considered, such as discrepancies in CNT height/crystallinity across CNTs, which requires further investigations to address these possible discrepancies.

The resistance of one CNT bump ($R_{Au-CNT-G}$) in this work is compared with the results from the state-of-the-art as shown in Table 6.4. With simple normalization of the CNT area, it shows that our result compares favourably with the literatures [130], [131]. However, as the reported studies used various CNT area dimensions, further study is needed to explore the possible factors affecting the CNT/graphene contact resistance.

Table 6.4 Resistance of one CNT bump (including the CNT/metal (CNT/graphene) contact resistance) of this work and the reported state-of-the-art.

	$R_{Au-CNT-Au}$ [130]	$R_{ZrN-CNT-Al}$ [131]	$R_{Au-CNT-Au}$ [51]	$R_{Au-CNT-G}$ (this work)
CNT bump resistance R (Ω)	280	457	16.1	2.1
CNT area (μm^2)	1963	2827	7854	90000
CNT height (μm)	120	300	132	110

Repeatability tests of the total resistance were conducted to each graphene and Au bridge structure as shown in Table 6.5. Except for the graphene bridge structure with PET substrate, other three structures with SiO_2/Si substrate show increasing trend in resistances under repeated voltage sweep (-1 to 1V). This can be attributed to the

damage of accumulating charges at the air gap between CNTs and graphene (or Au) contact. However, for the graphene bridge structure with PET substrate, the air gap can be shortened by the electrostatic force of accumulating charges after several voltage sweeps since the PET substrate is flexible. Thus, the total resistance of graphene bridge structure with PET substrate decreases initially, and then stabilized at the lowest value under repeated voltage sweep.

Table 6.5 Repeatability tests of the total resistance for the graphene and Au bridge structures.

Sample	$R_{total} (\Omega)$				
	1 st	2 nd	3 rd	4 th	5 th
A with graphene bridge (PET)	11.1	10.6	10.0	10.2	10.0
A with Au bridge (SiO ₂ /Si)	5.2	6.2	7.0	6.8	7.0
B with graphene bridge (SiO ₂ /Si)	128.1	135.4	135.0	135.0	133.7
B with Au bridge (SiO ₂ /Si)	18.2	21.3	21.8	22.3	23.3

6.6 Summary

In this chapter, transfer process of a top graphene layer onto the as-grown CNT bundles was improved. Direct graphene-to-CNT contact was formed at the CNT/graphene interface. 4PP I-V characterization suggests that an ohmic contact was achieved between the graphene and CNTs. Low CNT bump resistance of 2.1 Ω for 90,000 μm^2 CNT area including the CNT/graphene contact resistance was obtained, demonstrating reduction of contact resistance between CNT and Au under the same fabrication and measurement conditions. This chapter presents the preliminary results for the assembly process of top-transferred graphene on CNTs and the electrical properties of the direct CNT/graphene contact.

Chapter 7 : Femtosecond Laser Annealing for Graphene-CNT Fusion

7.1 Introduction

In Chapter 6, we fabricated the graphene bridge structure with the direct graphene-to-CNT contact. Mechanical pressing is used to enhance the CNT-graphene bonding. Next, annealing methods are explored for graphene and CNTs fusion, to form carbon covalent bonds which can further decrease the contact resistance and enhance the reliability. Three annealing methods, i.e. thermal annealing, electric-current-induced Joule heating and laser annealing, were proposed for graphene-CNT fusion. For the bridge structure in Chapter 6, thermal annealing may not be applicable as our preliminary results show that the global heating of the whole sample piece at a high temperature ($>400^{\circ}\text{C}$) will burn the PET spacers and destroy the bridge structure. For the method of electric-current-induced Joule heating, as discussed in Chapter 6, the current density which can be induced by probing in our Keithley 4200-SCS Semiconductor Characterization System is too small ($\ll 10^8 \text{ A/cm}^2$) to fuse the CNTs and graphene. Thus, laser annealing may be the most suitable method for the fusion trials on the graphene bridge structure.

7.2 Experimental Objective and Scope

Femtosecond laser irradiation can induce intense, localised annealing which is highly controllable and repeatable. This chapter aims to explore the conditions of femtosecond laser annealing for the fusion of graphene and CNTs in the bridge structure. First, the laser power was fine-tuned to generate optimized Joule heat on the graphene/CNT interface without damaging the CNT/graphene. After optimizing the laser power, laser annealing will be applied on the graphene bridge sample.

7.3 Femtosecond Laser Power Tuning

In this work, a Ti-Sapphire COHERENT Ultra II femtosecond laser was used.

The beam wavelength was set at 800 nm. The pulse duration was 140 fs with a repetition rate of 80 MHz. The laser beam was focused with a 10x microscope objective resulting in an effective laser spot diameter of $\sim 10\text{ }\mu\text{m}$.

Before the laser annealing of the graphene bridge sample, the laser power was tuned to an optimized value to generate optimized Joule heat on the graphene/CNT interface without damaging the CNT/graphene. A dummy bridge structure sample with graphene (with PET substrate) transferred onto CNTs was used for laser power tuning. Figure 7.1(a) shows the illustration of the laser beam focus position on the graphene/CNT interface while Figure 7.1(b) shows the burned marks of power tuning results. From the laser power values summarized in Table 7.1, it can be observed that any single-spot mode laser with power above 0.0166W would result in burning of CNTs, as shown in Figure 7.1(b). For the laser line scanning mode, the Joule heat generated by the laser beam was lower than the single spot with the same power (0.0394W). Nevertheless, a burned mark (G) can still be observed after the line scanning.

Figure 7.1 (a) Illustration of the laser beam focus position on the graphene/CNT interface and (b) The burn marks of laser power tuning results.

Table 7.1 Laser power value and beam mode for each test spot.

Laser spot	Power value	Laser beam mode
A	0.1W	Single spot
B	0.0625W	Single spot
C	0.0625W	Single spot with shorter shooting time than B
D	0.0394W	Single spot
E	0.0394W	Single spot with shorter shooting time than D
F	0.0166W	Single spot
G	0.0394W	Line scanning

7.4 Results and Discussion

After the laser power tuning, 0.0166W was selected as the optimized value for annealing. A fresh piece of bridge structure sample with graphene (with PET substrate) transferred onto the same CNT area as configuration A in Chapter 6 was used for the laser annealing trials. Figure 7.2 shows the illustration of laser line scanning approach. Since the width of CNT wall was 30 μm and the laser spot diameter was $\sim 10 \mu\text{m}$, 3 line scans (top + middle + bottom) for each CNT wall were carried out and the line scan length was fixed at 3 mm, covering the full length of each CNT wall. 4PP I-V measurements were used to characterize the electrical properties of the graphene bridge sample before and after laser annealing. From the results shown in Table 7.2, it can be observed that the total resistance of graphene bridge sample without annealing decreases initially when applying voltage sweep (-1 to 1V), From the 3rd sweep onwards, the total resistance increases after the repeated voltage sweep (-1 to 1V). After the first laser annealing, the total resistance dropped to the lowest value (27.3 Ω) but increased after the second and third laser annealing. Figure 7.3 shows the comparison of the I-V curves before and after 1st laser annealing, showing the decreasing of the total resistance upon laser annealing. However, it does not give sufficient evidences to conclude that the resistance dropping was due to the fusion of graphene and CNTs by the laser annealing as the resistance values before and after laser annealing did not exhibit much consistency and stability. The resistance after 1st laser annealing (27.3 Ω) was still close to the 3rd sweep without laser annealing (29.1 Ω). Another possibility in decrease in resistance may attributed to the air-gap shortened by the electrostatic force of accumulating charges after voltage stressing, which is not solely contributed by the fusion of graphene and CNTs after laser annealing.

Figure 7.4 shows the comparison of the graphene bridge sample after the laser annealing and graphene-on-CNT sample (discussed in Chapter 6) without laser annealing. The burned marks observed from the laser annealing sample indicating that after the 3rd laser scanning the sample was already over annealed, which partially explained the increase in resistance of graphene bridge structure after the 3rd laser annealing as shown in Table 7.2.

Figure 7.2 Illustration of 3 laser line scans covered the full length of one CNT wall.

Figure 7.3 Comparison of the I-V curves before and after 1st laser annealing.

Figure 7.4 Comparison of (a) the graphene bridge sample through the laser annealing and (b) graphene-on-CNT sample (discussed in Chapter 6).

Table 7.2 Resistances of the graphene bridge structure before and after laser annealing.

$R_{total} (\Omega)$							
Before laser annealing					After laser annealing		
1 st	2 nd	3 rd	4 th	5 th	1 st laser annealing	2 nd laser annealing	3 rd laser annealing
43.8	32.1	29.1	37.4	35.0	27.3	28.1	29.0

7.5 Summary

In this chapter, the conditions of femtosecond laser annealing for the fusion of graphene and CNTs in the bridge structure were explored. After the laser power tuning, 0.0166W was selected as the optimized value for annealing. Laser line scanning was applied at the graphene/CNT interface and the electrical properties of the pristine graphene bridge and annealed graphene bridge samples were characterized. The total resistance of the bridge structure dropped to its lowest (27.3 Ω) after the first laser scanning, but increased after the second and third laser annealing. However, the obtained outcomes give insufficient evidences to conclude that the resistance dropping was due to the fusion of graphene and CNTs by the laser annealing. Therefore, further studies are needed to verify the formation of CNT-graphene bonding its impact on the overall resistance upon laser annealing.

Chapter 8 : Conclusion and Future Work

8.1 Conclusion

In this study, development and optimization of CNT-graphene heterostructure were carried out for its application in TSV interconnects. First, recipes and methodology to grow free-standing CNTs on graphene sheet were optimized. CNTs grown with TCVD technique yield sufficient length ($\sim 334\mu\text{m}$) and density ($\sim 10^{11} \text{ cm}^{-2}$) for its application in TSV interconnects. Different growth parameters such as catalyst film thickness, growth time and growth temperature were systemically studied. With the understanding of different growth parameters, the feasibility in growing CNTs within TSVs on the bottom graphene electrodes can be explored.

After the development and growth of free standing CNTs, fabrication process flow of graphene-CNT heterostructure within TSVs was designed and explored. TSV fabrication was successfully demonstrated using lithography and DRIE techniques. Catalyst layer and graphene layer were also deposited onto the bottom wafer to accommodate latter growth of CNTs within the TSVs on top of the graphene layer. However, as compared to the free-standing growth of CNTs on the graphene, CNTs grown within the unfilled TSVs are relatively sparse owing to the process-engineering steps involved. Therefore, suitable process optimization and improvement steps have been carried out to improve the density of CNTs grown within TSVs.

After demonstration of CNT growth within TSVs on top of graphene layer, the process of transferring a top-graphene layer onto the CNTs was explored. At the same time, the electrical properties of the fabricated structures were studied. Using the bridge structure and graphene dry transfer with a thermal tape, the electrical properties of the Au-CNT-graphene-CNT-Au structure can be directly probed. The electrical characterization shows a linear response to the current when the voltage sweep (-1 to

1V) was applied after graphene transferred. At the same time, the total resistance of Au-CNT-graphene-CNT-Au was calculated as 174 Ω . The optimization of the bridge structure is required to further investigate the electrical properties of direct graphene-to-CNT contact.

To improve the electrical properties and reduce the contact resistance at the graphene-CNT interface, mechanical pressing was applied onto the structure. At the same time, graphene bridge structure was developed and fabricated to better characterize the electrical properties of the CNT/graphene interface. Direct graphene-to-CNT contact was formed at the CNT/graphene interface. 4PP I-V characterization suggests that an ohmic contact was achieved between the graphene and CNTs. Low CNT bump resistance of 2.1 Ω for 90,000 μm^2 CNT area including the CNT/graphene contact resistance was obtained, demonstrating reduction of contact resistance between CNT and Au under the same fabrication and measurement conditions.

In conclusion, this work demonstrates the feasibility of CNT-graphene heterostructure for its application in TSV interconnects. Various possible technical difficulties have been addressed and explored: (1) CNTs of sufficient height ($\sim 334\mu\text{m}$) and density ($\sim 10^{11} \text{ cm}^{-2}$) is grown for TSV interconnect application, (2) CNTs are successfully grown in fabricated TSVs on top of the graphene layer, (3) Graphene bridge structure is developed to improve the electrical characterization steps of CNT-graphene heterostructure, (4) Contact resistance between CNT-graphene is reduced by mechanical pressing. The outcomes from this research provide significant insights in the understanding of CNT-graphene heterostructure for TSV interconnect application, which paves the way for the latter researches in optimization and commercialization of CNT-graphene interconnects.

8.2 Future Work

In this thesis, development of CNT-graphene heterostructure for TSV interconnect applications has been demonstrated. CNTs with top/bottom graphene layers have been grown and assembled in pre-fabricated TSVs for full-carbon, miniaturized interconnect application. Various technical challenges have been addressed, such as difficulties in electrical properties characterizations, and contact resistance in CNT-graphene interface. For further realization of CNT-graphene heterostructure for TSV interconnect applications, the following studies and development work can be carried out.

In Chapter 4, CNT obtained within the unfilled TSV was sparse, with relatively few CNTs grown per unit area as compared to free-standing CNT bundles. This can be attributed to the process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. At the same time, the high aspect ratio (5~10) of the TSVs may hinder the flow of carbon precursors into the bottom of the TSV pits during Thermal Chemical Vapor Deposition (TCVD) process, which result in sparsely-grown CNTs. Hence, process steps of TSV fabrication and conditions for CNT growth need to be modified and optimized in order to obtain higher CNT fillings within the TSVs. At the same time, the TCVD recipe for CNT growth can be further fine-tuned, to ensure smooth flow of carbon precursor into the TSV pits during TCVD process.

Despite demonstration of reduced contact resistance within CNT-graphene interface and approximate calculation of contact resistance value, the exact relationship between the contact resistance and the contact area of graphene and CNTs is still unclear. Theoretically, for interconnects with larger area, the electron mobility will be higher, hence result in higher electrical conductivity. However, an opposing postulation may bring up where the presence of larger contact area results in larger

CNT-graphene electron barrier, hindering the flow of electrons through the interface. As this study demonstrates the calculation and deduction of contact resistance between CNT-graphene, it serves as a preliminary step for future studies where the relationship between contact resistance and the contact area of graphene-CNTs can be determined. Therefore, more experimental work can be conducted in order to quantify the contact resistance with the certain contact area.

In this work, low CNT bump resistance of 2.1Ω for $90,000\ \mu\text{m}^2$ CNT area including the CNT/graphene contact resistance was obtained. This suggests the reduction of contact resistance upon mechanical pressing technique. However, the CNT area fabricated in this work is $90,000\ \mu\text{m}^2$ which is too large for the application of CNT-graphene heterostructure for the state-of-the-art TSV interconnect applications. Nevertheless, the reduction of contact resistance paved a useful path for future miniaturization of the reported heterostructure. Combining the previous suggested future work on studying the relationship between contact resistance and the CNT-graphene contact area, the miniaturization of the CNT-graphene heterostructure can be carried out smoothly. Therefore, further study will be conducted to narrow down the CNT area and explore the possible factors affecting the CNT/graphene contact resistance.

Fusion of CNT-graphene structures by forming covalent bonds within CNT-graphene interface is important for further reduction of contact resistance and increasing the mechanical reliability of CNT-graphene heterostructure. In Chapter 7, the treatment of CNT-graphene heterostructure using femtosecond laser has been demonstrated. From the obtained electrical characterizations, it can be deduced that femtosecond laser treatment reduces the contact resistance in CNT-graphene interface, where this reduction can be attributed to the fusion of CNT/graphene interface.

Despite demonstration of reduced resistance upon femtosecond laser treatment, the fusion effect of femtosecond laser on CNT-graphene heterostructure remained unexplored. Therefore, fusion of the graphene and CNTs with carbon covalent bonds needs to be further studied.

Heat-dissipation and cooling issues are aggravated in 3-D ICs due to presence of different interfaces with widely-differing thermal and electrical conductivities, creating bottlenecks to facile heat transfer from chip to chip. Hotspots across various layers in chip-stacks severely degrade overall system performance, leading to critical and random device failures, and elevated temperatures severely affect carrier-mobility, and threshold voltages of the transistors. Different solutions have therefore been proposed to alleviate the thermal congestion, ranging from algorithmic approaches (i.e., thermal floorplanning and thermal TSV placement) to micro-fluidic channels. As an alternative, the integration of highly thermally conductive materials, e.g. CNT and graphene is one of the strongly promising ways to overcome the thermal bottlenecks. Since CNT and graphene possess high thermal-conductivity (1767 W/mK for CNT bundles and 1300 W/mK for multi-layer graphene, compared to copper's 400 W/mK and tungsten's 175 W/mK), the 3-D interconnects based on CNT-graphene heterostructure are supposed to remove the hot spots faster than traditional metals. Therefore, thermal property of the full carbon-based 3-D interconnects with CNT-graphene heterostructure is required to be further studied.

Another challenge topic for 3-D interconnects is the application for high frequency devices, where the traditional metals e.g. Cu or Au have the skin depth issues adversely leading to signal losses at high frequencies beyond 100 GHz. As one of the advantages, the large kinetic inductance and negligible magnetic inductance allow CNT to have a negligible skin depth effect. The integration of CNT and

graphene with seamless carbon covalent bonds can help to extend this advantage to three dimensions compared with the metal counterparts. Thus, high-frequency characterization of the full carbon-based 3-D interconnects with CNT-graphene heterostructure needs to be performed for future work in order to explore the possible applications in high-frequency electronic devices.

Author's Publication

During doctor's work

- 1) **Ye Zhu**, Chong Wei Tan, Shen Lin Chua, Yu Dian Lim, Boris Vaisband, Beng Kang Tay, Eby G. Friedman, Chuan Seng Tan, "Assembly Process and Electrical Properties of Top-Transferred Graphene on Carbon Nanotubes for Carbon-Based Three-Dimensional Interconnects", *Components Packaging and Manufacturing Technology IEEE Transactions on*, DOI: 10.1109/TCPMT.2019.2940511.
- 2) Chong Wei Tan, **Ye Zhu**, Shen Lin Chua, Maziar Shakerzadeh, Chuan Seng Tan and Beng Kang Tay, "Electrical properties of FCVA deposited nano-crystalline graphitic carbon thin films with in-situ treatment techniques", *Eur. Phys. J. Appl. Phys.*, 85, 20301 (2019). DOI: 10.1051/epjap/2019180097
- 3) **Ye Zhu**, Chong Wei Tan, Shen Lin Chua, Yu Dian Lim, Beng Kang Tay, Chuan Seng Tan, "Growth and Fabrication of Carbon-Based Three-Dimensional Heterostructure in Through-Silicon Vias (TSVs) for 3D Interconnects", *IEEE 19th Electronics Packaging Technology Conference (EPTC)*, 2017, pp. 1-5.

Pre-doctor's work

- 4) **Ye Zhu**, Kaushik Ghosh, Hong Yu Li, Yiheng Lin, Chuan Seng Tan, Guangrui (Maggie) Xia, "On the Origins of Near-Surface Stresses in Silicon around Cu-filled and CNT-filled Through Silicon Vias", *Semiconductor Science and Technology*, vol. 31, 2016, p. 055008.
- 5) **Ye Zhu**, Jiye Zhang, Hong Yu Li, Chuan Seng Tan and Guangrui (Maggie) Xia, "Study of Near-surface Stresses in Silicon around Through Silicon Vias at Elevated Temperatures by Raman Spectroscopy and Simulations." *IEEE Transactions on Device and Materials Reliability*, vol. 15, 2015, pp.142-148.

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