Self-heating and trapping effect in AlGaN/GaN high electron mobility transistors on CVD-diamond

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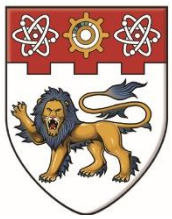

NANYANG TECHNOLOGICAL UNIVERSITY

SELF-HEATING AND TRAPPING EFFECT IN ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS ON CVD-DIAMOND

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University in partial fulfillment of the requirements for the degree of Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

30.12.2019 Kumud Ranjan

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I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Date Prof. Ng Geok Ing

Authorship Attribution Statement

This thesis contains material from 5 paper(s) published in the following peer-reviewed journals and from papers accepted at conferences in which I am listed as an author.

Chapter 3 includes 2 publications

- **K. Ranjan**, S. Arulkumaran, G. I. Ng, Sandupatla. A, "Investigations of self-heating effect in AlGaN/GaN HEMT on CVD diamond," *Electron device society (J-EDS),* Vol. 7, pp. 1264-1269,2019.

- **K. Ranjan**, G. I. Ng, S. Arulkumaran, S. Vicknesh, and S. C. Foo, "Enhanced DC and RF performance of AlGaN/GaN HEMTs on CVD-Diamond in high power CW operation". in Electron Devices Technology and Manufacturing (EDTM), Mar. 2019, Singapore

The contributions of the co-authors are as follows:

- I co-designed this project with Prof. G. I. Ng, and Dr. S. Arulkumaran and performed all laboratory works including design, device fabrication, simulation, measurements, analysis and preparation of manuscript drafts.
- Prof. G. I. Ng provided valuable guidance and funding support for semiconductor wafer and edited the manuscript drafts.
- Dr S. Arulkumaran assisted with epitaxy wafer which was used for device fabrication. He also provided direction of study and research and assisted in edited manuscript drafts.

- S. Vicknesh and S.C Foo helped in the study of epitaxy properties and initial fabrication of devices and edited the manuscript drafts.
- A. Sandupatla assisted in part of characterization of device and helped in editing the manuscript drafts.

Chapter 4 includes 2 publications

- **K. Ranjan**, S. Arulkumaran, G. I. Ng, “Investigations of temperature-dependent interface traps in AlGaN/GaN HEMT on CVD-diamond,” *Applied Physics Express,* 12,10, 2019.
- **K. Ranjan**, S. Arulkumaran, G. I. Ng, S. Vicknesh and K.S. Ang, “Self-heating effects in DC and RF performances of 0.25 μm T-Gate AlGaN/GaN HEMTs on Silicon and CVD-Diamond,” at 12th Topical Workshop on Heterostructure Microelectronics (TWHM), Aug 2017, Kirishima, Japan

The contributions of the co-authors are as follows:

- I co-designed this project with Prof. G. I. Ng and performed all laboratory work including measurements, analysis and preparation of manuscript drafts.
- Prof. G. I. Ng provided valuable guidance, assisted in interpretation of results and edited the manuscript drafts.
- Dr S. Arulkumaran provided initial project direction, assisted with the analysis and edited manuscript drafts.
- S. Vicknesh and K.S. Ang helped in the study of epitaxy properties and initial fabrication of devices, and edited the manuscript drafts.

Chapter 5 includes 1 publication

Chapter 5 was accepted as;

K. Ranjan, S. Arulkumaran, G. I. Ng and A. Sandupatla “Investigations of interface traps in AlGaN/GaN MIS-HEMTs on CVD-Diamond” in Electron Devices Technology and Manufacturing (EDTM) Conference – 2020, Malaysia.

The contributions of the co-authors are as follows:

- I co-designed this project with Prof. G. I. Ng and Dr. Arul, and performed all laboratory work including measurements, analysis and preparation of manuscript drafts.
- Prof. G. I. Ng provided valuable guidance, assisted in interpretation of results and edited the manuscript drafts.
- Dr S. Arulkumaran provided initial project direction, assisted with the analysis and edited manuscript drafts.
- A. Sandupatla helped in the measurement setup and edited the manuscript drafts.

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Date Kumud Ranjan

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Abstract

GaN-based high-electron-mobility Transistors (HEMTs) are widely used for high frequency, high voltage and high-power applications. However, there are still many major challenges facing these devices such as thermal management, size reduction and long-term reliable operation, especially when they are operating at very high voltage (e.g., $V_D \geq 48$ V). In such an operating condition, the device suffers substantial self-heating and encounters enhanced phonon scattering, which degrades device current due to the decrease of 2-DEG mobility and electron velocity as a result of the increased junction temperature. These problems are predominant particularly when GaN HEMTs are fabricated on conventional low thermal conductive substrates (e.g., Si (K_{Si}=130 W/m-K), Sapphire (K_{Sa}=46 W/m-K) and SiC (K_{SiC}= 450 W/m-K)).

The usage of high thermal conductivity substrates such as diamond (1000-2000 W/m-K) is now emerging as a viable technique to extract the heat under high-power operations for GaN-based high-electron-mobility transistors (HEMTs). Typically, for GaN-on-Diamond process development, both the host Si or SiC substrate and the growth-defect-rich stress mitigation transition layers are first removed. The remaining HEMT layers are then bonded onto CVD-diamond, which then acts as the new substrate. Thus, the HEMTs fabricated on transferred GaN-on-Diamond

will have different behaviour of self-heating and trapping than that of conventional HEMTs fabricated on GaN-on-Si.

In this thesis, the main objectives are to investigate the self-heating effect on DC and RF performance, and the trapping behaviour in GaN HEMTs-on-CVD Diamond.

The major contributions of this thesis are summarized below:

(1) The quantitative investigation of the self-heating effect on DC and RF performances was carried out for AlGaN/GaN HEMTs on CVD-Diamond (GaN/Dia) and Si (GaN/Si) substrates. The GaN/Dia HEMTs were found to exhibit ~5.7-times lower rate of I_D reduction than GaN/Si HEMTs. This behaviour was also confirmed by 2D device simulation. The f_T reduction rate was ~6.75-times lower in the case of GaN/Dia than GaN/Si HEMTs whereas no significant reduction of f_{max} was observed in GaN/Dia HEMTs. Small signal measurements and equivalent circuit parameter extraction were done to analyze the variation in the performance of the devices. The comparatively lower reduction rate of μ_{eff} and v_{eff} in GaN/Dia HEMTs made its performance less degraded (~15%) as compared to (~50%) GaN/Si HEMTs. These results show that GaN/Dia HEMTs can be operated even at higher V_D as well as at higher P_D which are paramount features for developing compact high power SSPAs for CW application.

(2) The hetero-interface trapping characteristics in AlGaN/GaN HEMT on CVD-diamond were investigated at different temperatures (25 °C to 200 °C) using the conductance method. The fast traps (0.16 to 10.01 µs) were identified as the dominating traps in our HEMT structure. The density of fast traps (D_{Tf}) increases with temperature from 6.7×10^{10} cm^{-2} eV^{-1} at 25 °C to 1.4×10^{12} $cm^{-2}eV^{-1}$ at 200 °C. For 25 °C to 200 °C, the interface trap state energy (E_T) was obtained to be between 0.27 and 0.51 eV below the conduction band. The observation of increased D_T with temperature could be due to the excitation of additional traps deeper in the bandgap. A lower value of D_{Tfmin} for GaN-on-CVD Diamond compared to GaN on Silicon devices is attributed to the removal of the defect-rich GaN transition layer during the substrate transfer process. Finally, the temperature-dependent pulsed I_{DS}-V_{DS} measurements revealed good agreement with the behaviour of D_T with temperature obtained using the conductance method. Further to improve the device performance, GaN-MISHEMTs-on-CVD diamond was fabricated and analyzed the g_m linearity, gate leakage, and interface trap behavior.

(3) For the first time, the investigation of interface traps in AlGaN/GaN metal-insulator-semiconductor (MIS) HEMTs on CVD-diamond was reported in this work. The critical issue in MIS-HEMTs is the dielectric

interface trap behaviour. The detailed investigation of dielectric interface and hetero-interface is carried out in AlGaN/GaN MISHEMTs on CVD-diamond and compared with the conventional Schottky AlGaN/GaN HEMTs on CVD-diamond. The finding of slow and fast type of traps in MISHEMTs on the contrary to only fast traps in conventional HEMTs indicated the source of traps. Such a study of interface trap behaviour in the device will help to identify and improve the reliability of AlGaN/GaN HEMTs and MISHEMTs-on-CVD diamond.

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1 Introduction

1.1 GaN HEMT technology: An overview

In the past few years, Gallium Nitride (GaN) based High-Electron-Mobility Transistors (HEMTs) have made tremendous progresses which makes them very attractive for high-frequency, high-power microwave and high-power switching device applications [1-4]. This is because GaN HEMTs are able to handle high current, high power, and capable to operate at high frequency due to the unique material properties of GaN such as large band gap, high electron velocity and critical breakdown field [5, 6]. A detailed explanation of the formation of two-dimensional electron gas (2DEG) of GaN HEMT and its structure has been provided in chapter 2.

Table 1.1 and figure 1.1 compare various material properties of GaN and other semiconductors which are generally used in field-effect transistors. The superior electron mobility and high saturated drift electron velocity in 2DEG of GaN HEMT enable the device to operate at high current densities and high frequencies. The high critical field of GaN allows GaN-based devices to operate at higher voltages while high electron mobility makes it more suitable for high-frequency applications.
The impact of material on the performance of semiconductor devices, figure-of-merit (FOM) are usually used. The FOM provides a rough

quantitative estimation of their relative strength with respect to specific device applications. To compare semiconductors for power device applications, the commonly used FOM are Johnson's FOM (JFOM) and Baliga FOM (BFOM). The JFOM characterizes the high-frequency performance of GaN devices and is proportional to the saturation velocity and critical electric field for impact ionization-initiated breakdown and is given by [7]:

$$JFOM = \left(\frac{E_c\, v_{sat}}{\pi}\right)^2$$

where v_{sat} is the saturation velocity, and E_c is the critical electric field. While the BFOM is used to define material parameters to minimize the conduction losses in the device at low-frequency operations. It is given by [7, 8]:

$$BFOM = \varepsilon \mu_n E_C^3$$

where ε is the relative dielectric constant, μ_n is the electron mobility and E_C is the critical electric field of semiconductor. Table 1 presents some figures of merit (FOM) used to quantify the device performance in high power and high frequency operation. All FOM values are normalized with respect to silicon. Due to its unique material properties, GaN-based HEMTs have exhibited much higher JFOM in comparison to GaAs and Si based transistors.

Table 1.1 Material properties of GaN and other semiconductor materials at 300K. All FOM values are normalized with respect to silicon [7].

Properties	Si	GaAs	4H-SiC	GaN
Bandgap, E_g (eV)	1.12	1.42	3.25	3.40
Dielectric Constant, ε_r	11.8	12.8	9.7	9.0
Breakdown field, E_{Br} (MV/cm)	0.25	0.4	3.0	3.3
Electron mobility, μ (cm^2 /V s)	1350	8000	800	2000
Maximum saturation velocity, v_{sat} ($\times 10^7$cm/s)	1.0	2.0	2.0	3.0
Thermal conductivity, k (W/m-K)	150	54	450	130
JFOM	1	7.1	180	760
BFOM	1	15.6	130	650

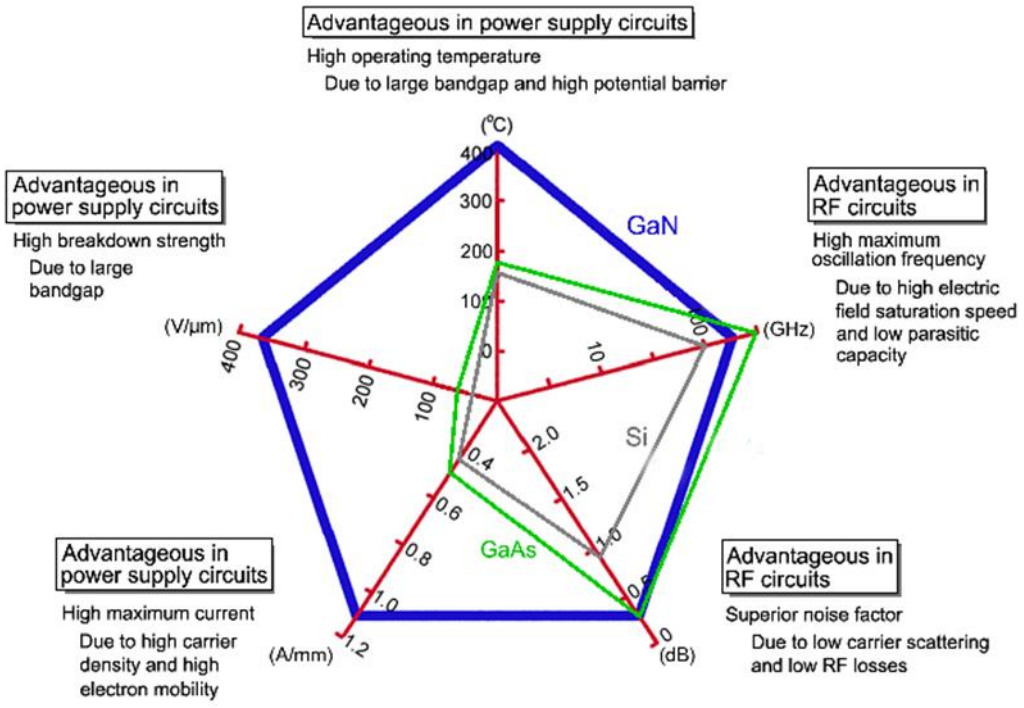


Figure 1.1 GaN material merits compared to Si and GaAs [9].

It is used in developing GaN HEMTs based devices and monolithic microwave integrated circuits (MMICs) for various electronic applications. Figure 1.4 shows the characteristics and area of application of GaN-based AlGaN/GaN HEMTs.

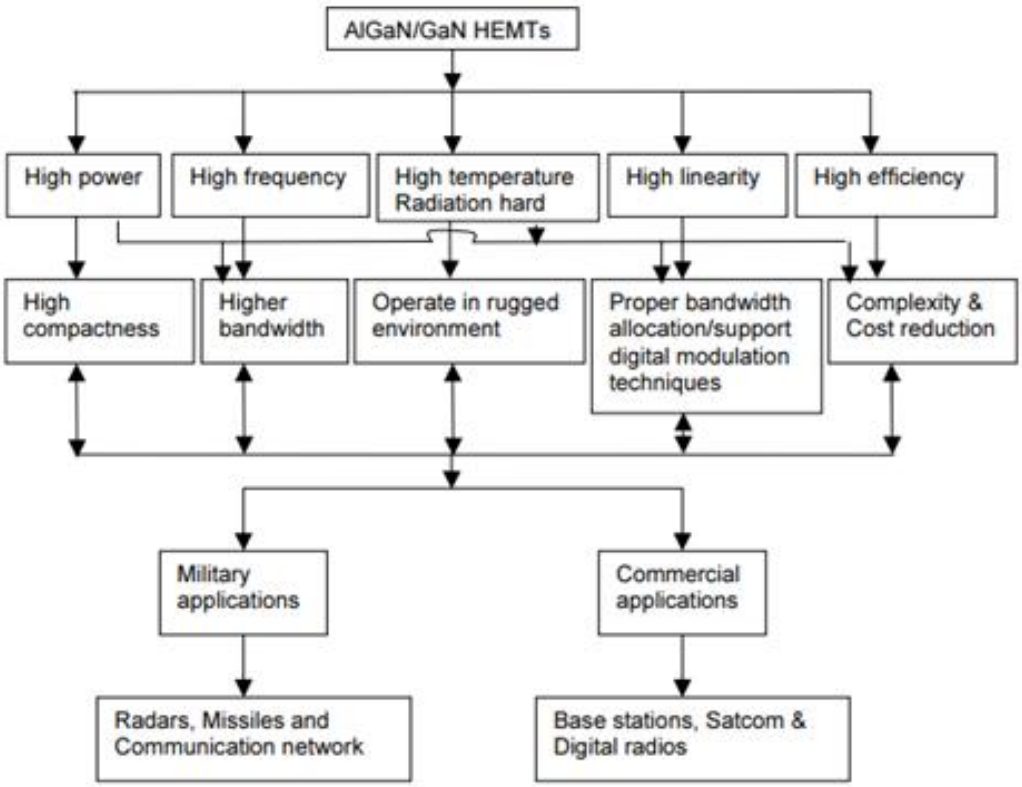


Figure 1.2 Characteristics and applications areas of GaN HEMTs [10].

Figure 1.3 shows the RF application spectrum of Si, GaAs and GaN-based power devices along with RF power requirements and power frequency limits. From fig. 1.3 it is clear that GaN-based amplifiers are superior to GaAs and Si-based amplifiers in terms of both the output power and operating frequency limit. The theoretical limit of the GaN-based power amplifier is ~150-times and ~30-times higher than Si and

GaAs based amplifiers, respectively. In addition, GaN-based amplifiers also cover higher frequency spectrum for RF power applications in commercial, defence, and space industries. Other applications such as satellite, cellular base station, high power radar, and military systems also benefit from compact GaN-based high-power RF amplifiers.

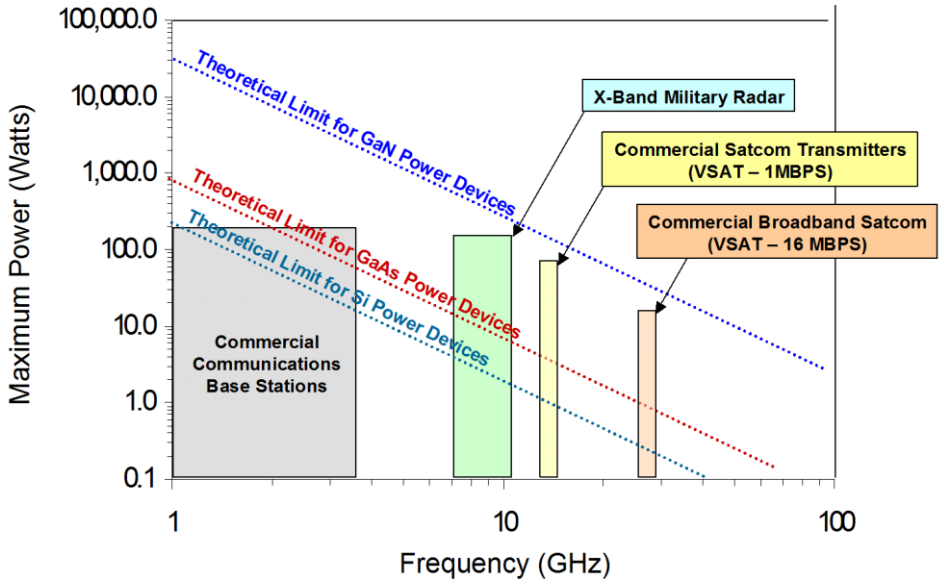


Figure 1.3 Some RF application spectrum showing RF power requirements as well as power frequency limits of Si, GaAs and GaN-based power devices [11].

Due to the superior current density and operating voltage, GaN-based HEMTs have started to be an attractive alternative to GaAs based amplifiers, especially in the high-power transceiver system. The size of GaN-based power amplifiers has also reduced significantly due to the increased power density in comparison to GaAs-based circuits. Fig. 1.4

shows the comparative size of the power amplifier, based on GaAs and GaN HEMTs. Using GaN HEMTs, size reduction is ~ 82% as compared to GaAs based PA [12].

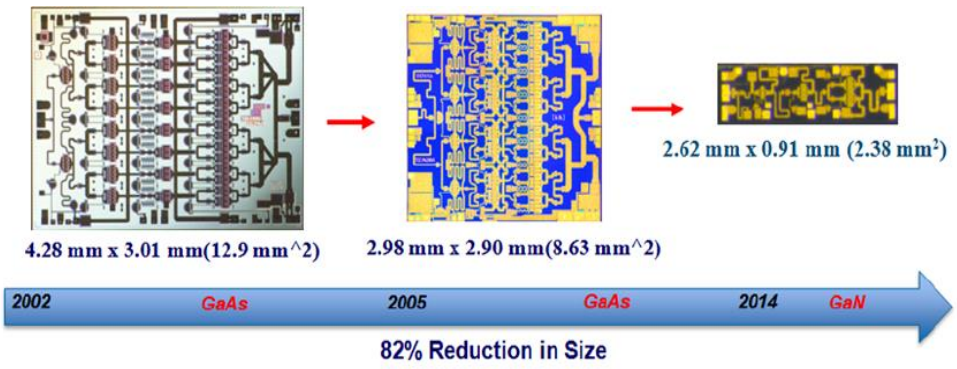


Figure 1.4 Advantage of GaN technology for power amplifiers (PAs) with efficient reduced size [12].

1.2 Issues in GaN HEMT for High Power Density Operation

1.2.1 Self-heating in GaN HEMTs

In GaN-based HEMTs, at high bias conditions generate a high electric field at the gate edge of the gate-drain region. This results in the generation of a large amount of heat due in the channel region which causes the channel temperature to rise and accelerating the phonon scattering (see figure 1.5 (a)). This will degrade the electron mobility in the channel and thereby a reduction of the drain current. The reduction of electron mobility in AlGaN/GaN HEMTs with temperature has been observed as $\mu \sim (T/T_0)^{-1.8}$ [13]. The negative slope observed in the drain current characteristics is due to the self-heating effect (see fig. 1.5(b)).

Figure 1.5 shows the location of the maximum heat zone which is between the gate and drain due to the high electric field density that exists in this area. If the heat spreading from GaN HEMTs is insufficient, the device junction temperature increases, and the reduction of drain current density (I_{ds}) will occur with increasing drain voltage (V_{ds}). This self-heating becomes more severe when the device size is further reduced. Therefore, thermal management in GaN-based devices is a major concern, especially when the device is operating in a very high drain voltage (e.g., $V_{ds} \geq 48$ V). In such an operating condition, the device suffers substantial self-heating, which degrades the electrical (DC and RF) performance of the device and the circuit [14-17].

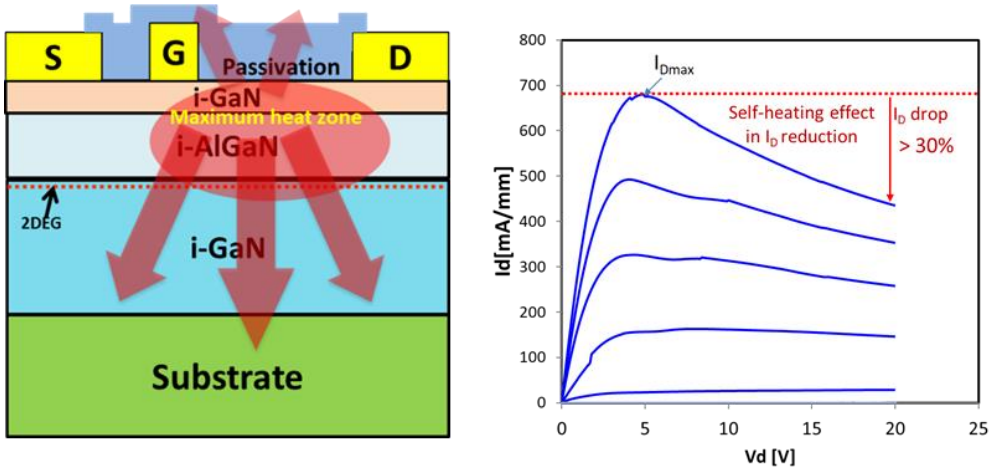


Figure. 1.5 (a) Schematic cross-section diagram of conventional, (b) Drain current reduction after I_{Dmax} due to self-heating effect in DC-IV output characteristics in GaN HEMTs-on-Si substrate AlGaN/GaN HEMTs showing the heat-spreading path from top and bottom.

These problems are predominant particularly when GaN HEMTs are employed on conventional substrates with low thermal conductivity (e.g., Si (K_{Si}=150 W/m-K), Sapphire (K_{Sa}=46 W/m-K) and SiC (K_{SiC}= 490 W/m-K)). Low thermal conductivity of substrates results in an increase of junction temperature (T_J) [18, 19], and hence a decrease of 2-DEG mobility of GaN HEMTs which limits the efficient continuous wave (CW) operation at large Power densities (P_D).

There are some conventional chip-level thermal management approaches to reduce the self-heating and junction temperature in the GaN-based device by using micro-channel liquid cooling or thermoelectric cooling. However, these methods have drawbacks like difficulty in implementation, MMIC incompatibility and in some cases need additional power and also the overall size of the module will be increased [20]. To overcome these problems, a high thermal conductive material diamond (See table 1.2) is employed near the device junction (maximum heat zone) (See Fig. 1.5). Two methods are used to extract the heat from the device, one from the top and another from the bottom of the device. However, heat extraction from the top has many challenges like high temperature (~800 C) diamond deposition, and diamond etching which can degrade the 2DEG properties of GaN HEMT. Another issue is the low effective thermal conductivity of thin diamond film which is unable to extract the significant amount of heat from the device channel. To extract the heat from the bottom of the device, thick diamond substrates, having much

higher thermal conductivity (1000-2000 W/m-K), have been reported for GaN HEMTs [20, 21]. A comparative study of substrate material is listed in table 1.2. The high thermal conductivity of a thick diamond substrate helps in the faster dissipation of generated heat from the device which helps in maintaining a low junction temperature (T_j). Low T_j reduces the 2DEG mobility degradation and improves the reliability and lifetime of the device. AlGaN/GaN HEMT-on-CVD diamond was developed using Metal-Organic Chemical vapor deposition (MOCVD) grown AlGaN/GaN HEMT-on-Si (Standard Wafer) by a proprietary process from the commercial company Element Six. The substrate transfer process was mainly done by the removal of Si substrate as well as GaN transition layer. Finally, the remaining AlGaN/GaN layers are attached to a polycrystalline diamond using a proprietary process of SiN adhesion layer in-between GaN and CVD diamond substrate [22, 23]. The schematic of the wafer transfer process is shown in figure 1.6.

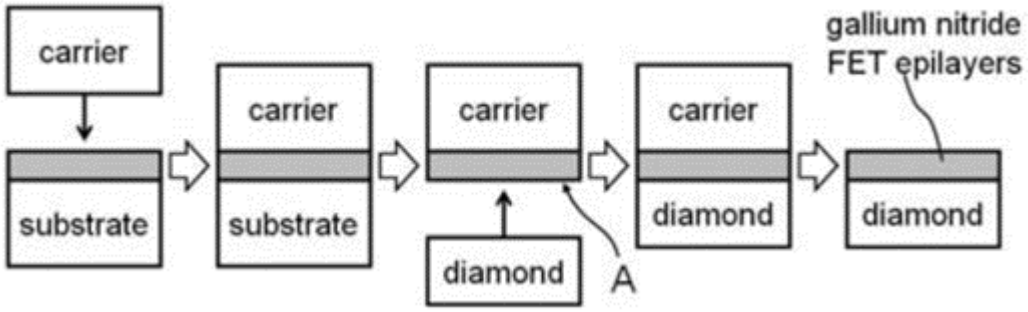


Figure 1.6: Schematic of transfer process from GaN-on-Si to GaN-on-Diamond [23].

The usage of high thermal conductivity substrates is an emerging viable technique to extract the heat under high-power operations for GaN-based high-electron-mobility transistors. Several authors have reported AlGaN/GaN HEMTs on diamond substrates with remarkable DC and RF performances [24-28]. Researchers have reported AlGaN/GaN HEMTs on Diamond with DC dissipated power density ($P_D = V_D \times I_D$) of 22 W/mm (CW) and 24 W/mm in pulse condition. Diduck et al has reported f_T of 85 GHz and f_{max} of 95 GHz. Felbinger et al has reported RF power of 4.1 W/mm at 10 GHz using gate field-plate structure and observed and 29% higher unity-current-gain frequency than identical structures on Si substrate [27] P. C. Chao et al has further improved the device RF performance of GaN-on-Diamond HEMTs which was transferred from GaN-on-SiC HEMT wafer. They observed 3.6-times higher RF power capability (i.e., RF output power per active area of the device) in GaN-on-Diamond HEMTs as compared to GaN-on-SiC HEMTs [28]. These results show strong manifestation of superior thermal conductivity of Diamond as a substrate for GaN HEMT.

Table 1.2 Thermal/electrical/physical properties of bulk substrate material for GaN semiconductor at 300 K.

Properties/Substrate	Sapphire	Si	SiC	GaN	Diamond
Thermal conductivity at 300K, k [W/m-K]	40±5	142.5±7.5	450±40	200±50	1500±500
Electrical resistivity at 300K, k [Ω.cm]	10^{17}	2.3×10^{5}	10^{4} to-10^{6}	10^{6}	10^{13}-10^{16}
Lattice mismatch with GaN [%]	14	17	3.5	0	89
Thermal Expansion Coefficient [$\times10^{-6}K^{-1}$]	7.5	2.6	4.46	5.5	1.0
Thermal expansion coefficient mismatch GaN [%]	36.4	52.7	18.9	0	81.8
Maximum available wafer diameter (mm)	150	300	150	30	150

1.2.2 Trapping Effect in GaN HEMTs

Trapping effects in GaN HEMTs cause current collapse, drain current degradation, threshold voltage shift, transconductance-frequency dispersion, etc. [29]. The existence of traps also leads to drain current dispersion results in the reduction of output-power during device operation [30, 31]. In addition, electron trapping also leads to an increase of dynamic-on resistance (Dyn-$R_{DS[ON]}$) under high-voltage operating conditions and degrades the switching performance of the device [32].

Various trapping mechanisms in GaN HEMT have been proposed to explain the device degradation due to electron trapping in different locations (e.g., surface traps, barrier traps, hetero-interface traps, and buffer traps) (See Fig. 1.6).

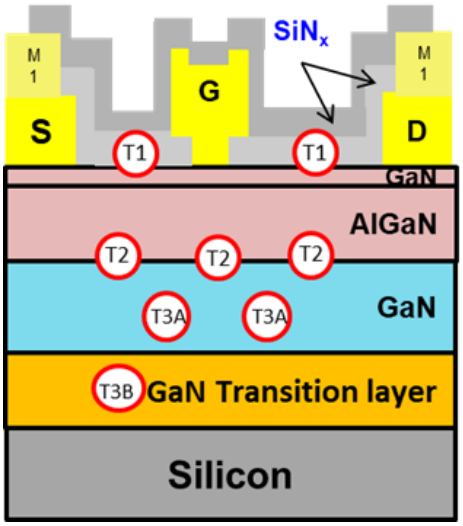


Figure 1.6 Schematic cross-sectional diagram of AlGaN/GaN HEMT on Si, illustrating the possible locations of traps: trap T1 at the surface, trap T2 at the GaN/AlGaN hetero-interface, and trap T3A in the GaN buffer and T3B in GaN transition layer.

The traps can be classified based on their energy level. The traps with an energy-level close to the conduction or valence bands are called shallow-level traps, which are responsible for parasitic doping effects. Traps with an energy level deeper within the forbidden bandgap are called deep level traps. Figure 1.7 illustrate the trap energy level in the bandgap showing presence of shallow and deep-level trap.

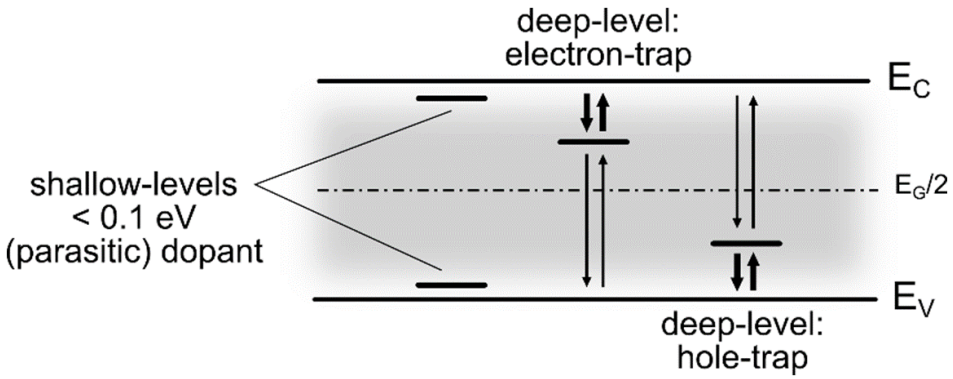


Figure 1.7. Illustration of the shallow and deep trap energy level in the bandgap [33].

The deep-levels which are localized in the upper-half of the bandgap which has higher probability to capture and emit electrons from and to the conduction-band and behaves as electron-traps. The physical origin of traps with reference to the conduction-band energy (E_c) in GaN HEMT are summarized in the table 1.3

Table 1.3. Database of physical origin of traps with the trap energy below conduction band in GaN-based devices (data taken from [32, 34]).

Trap Energies (eV)	Physical Origin	Ref
0.44,0.45 0.58	C/O/H Impurities	[32],[35]
0.58, 0.65	VGa+Oxygen complex	[32],[36],[37]
0.73	Nitrogen Interstitials	[32]
0.57, 0.72	Fe dopant	[38], [39]
0.27	Nitrogen vacancies	[40]
0.34	Possible AlGaN surface	[41]
0.8	Gallium vacancies	[42]

0.62, 0.65	GaN native defects	[35], [43]
0.51, 0.55, 0.69	Nitrogen Anti-sites	[36], [44]

Moreover, the density and the nature of these traps undermines the device reliability [45, 46]. The source of such traps is found to be either due to crystalline imperfections during the epitaxial growth, due to unintentional dope in barrier or buffer layer during epitaxy growth, or due to various device fabrications processes or wafer transfer process (in case of GaN-on-Si to GaN-on-CVD diamond). However, the exact origin and properties of these traps are still unclear in the transferred GaN HEMTs-on-CVD and need to be investigated as not many reports on the trapping behaviour are available.

1.3 Motivation and Objective

As we mentioned earlier, typically the GaN HEMTs-on-CVD diamond is transferred from GaN HEMTs-on-Si. In this process, two key structural changes occur in GaN HEMTs: one is replacing the high thermal conductive substrate and the other is the removal of trap rich GaN transition layer (See Fig. 1.8). These changes could affect the self-heating and trap behaviour in the GaN HEMTs-on-CVD diamond. Although the improvement in the electrical performance of GaN-on-Diamond AlGaN/GaN HEMTs has been previously reported [22-28,47-49], the detailed investigations of the self-heating effect and quantitative

estimation of electrical (mainly RF) performance have not been reported. In addition, due to the removal of the defect rich transition layer, there could be a change in the trap behaviour of the HEMT. This change in trap behaviour affects the device performance and reliability of the device. Unfortunately, so far, no detailed studies have been reported on the interface trap characteristics in GaN HEMTs-on-CVD diamond.

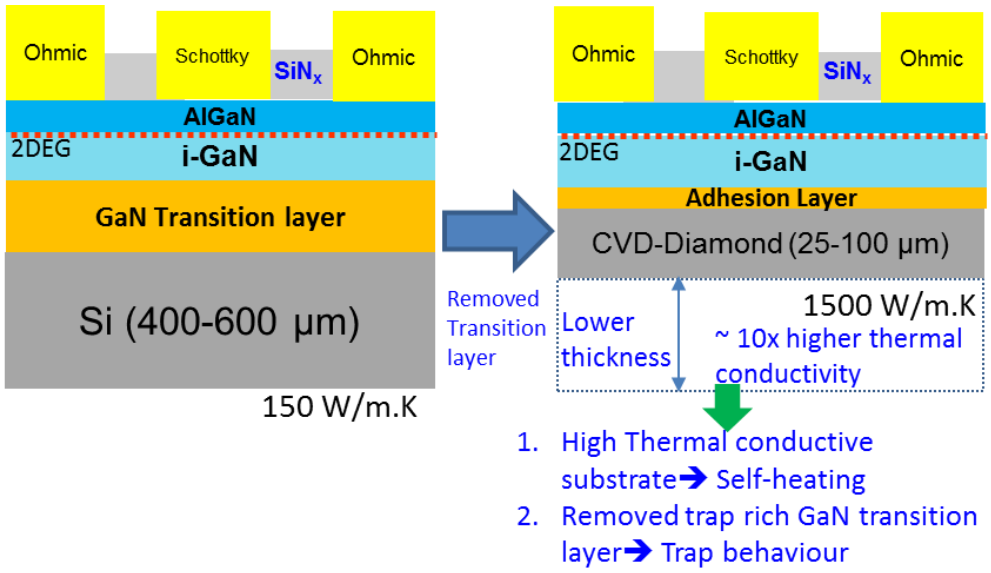


Figure 1.8 Schematic cross-section diagram of conventional GaN HEMTs-on-Si and GaN HEMTs-on-CVD diamond showing the major changes during the wafer transfer process.

1.4 Major contribution of the thesis

This thesis focuses on two key issues in the HEMTs fabricated on transferred GaN-on-Diamond from GaN-on-Si. First, the effect of substrate (CVD diamond) in the self-heating and second, the trapping

behaviour in GaN-on-Diamond.

In this thesis, a detailed investigation of the self-heating effect in DC (I_{dmax}, g_m) and RF (f_T, f_{max}, Gain) performance is carried out for a wide range of drain bias voltage. The degradation in 2DEG transport properties was also analyzed in the wide range of bias voltage. In addition, TCAD numerical simulation was carried out to investigate device junction temperature under the large electric field and high-power density dissipation. The effective carrier velocity and effective mobility were also investigated to analyze the variations in device performance due to self-heating effect. The 22-element small-signal equivalent circuit parameters were extracted and analyzed the variation in RF performances due to self-heating of GaN-on-Diamond HEMTs. Such work is helpful for developing the electrical and thermal model of device as well as improving the operating limit of GaN HEMTs for next-generation high power DC and RF applications.

In addition to the self-heating effect, interface traps behavior in GaN HEMTs-on-CVD diamond was also investigated. The conductance-frequency technique was used to estimate hetero-interface trap density, trap state energy, and trap time constants. Results were compared and benchmarked with reported GaN HEMTs on various substrates like Sapphire, Si, and SiC. Further to improve the device performance, GaN-MISHEMTs-on-CVD diamond was fabricated and analyzed the gm linearity, gate leakage, and interface trap behavior.

1.5 Thesis Outline

This thesis is written in six chapters. Chapter one stated the motivations and objectives of this work.

Chapter 2 provides an explanation of AlGaN/GaN HEMT principle and the device structure. This chapter also discusses the various characterization techniques used to evaluate the self-heating and trapping effects in AlGaN/GaN HEMTs. The basics of S-parameter measurements and small-signal equivalent circuit model is discussed which is crucial to investigate the variation in the device performance at high power density operation causes increased channel temperature in the device.

In chapter 3, the fabrication process of GaN HEMTs-on-CVD-diamond and Si substrates will be presented. The detailed quantitative investigation of the self-heating effect on DC and RF performances will be analyzed. The effect of bias conditions mainly on RF behaviour on HEMTs will also be analyzed. Using 22- element small-signal equivalent circuit parameters, RF performance of GaN HEMTs over a wide range of drain bias will be explained.

In chapter 4, the investigation of hetero-interface trapping characteristics in AlGaN/GaN HEMT on CVD-diamond using the conductance method will be presented. The conductance-frequency technique is used to estimate hetero-interface trap density and trap state

energy. The additional deeper traps in the bandgap are investigated by measurements performed at elevated temperatures (25 °C to 200 °C). The obtained results are benchmarked with the reported trap densities in GaN HEMTs on various substrates like Sapphire, Si, and SiC.

In chapter 5, the AlGaN/GaN metal-insulator-semiconductor (MIS) HEMTs on CVD-diamond is described to improve device characteristics further. The critical issue in MIS-HEMT is dielectric interface trap behaviour. The detailed investigation of dielectric interface and hetero-interface is carried out in AlGaN/GaN MISHEMTs on CVD-diamond and compared with the conventional Schottky AlGaN/GaN HEMTs on CVD-diamond.

In chapter 6, the summary of current work will be presented. Future research work and recommendations will also be given in chapter 6.

2 AlGaN/GaN HEMTs, Self-heating and trapping mechanism

In this chapter, the fundamentals of conventional AlGaN/GaN HEMT technology, the formation of the 2DEG channel, and current density in the device are briefly described. The self-heating issues in GaN HEMTs at high current, high dissipation power density operation and its effect in the channel temperature and device performance are also discussed. The electrical characterization techniques, which help to quantify and analyze self-heating induced device performance degradation, are also presented. To further understand the root cause of device performance degradation, a small signal equivalent circuit parameter is explained. At high power density, trapping phenomena in the device become critical for reliable operation. To understand the trapping mechanism and to evaluate the trapping behaviour, various characterization techniques are explained in this chapter. These methods are used to evaluate the self-heating and trapping effects in the device (GaN HEMTs-on-CVD diamond) described in this thesis.

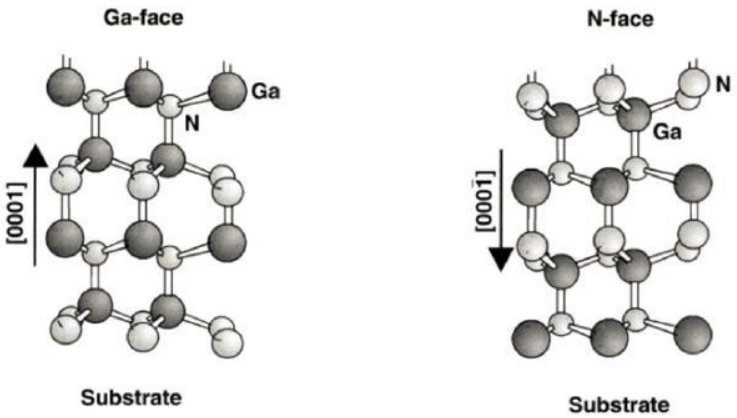
2.1 Introduction

GaN-based High-Electron-Mobility Transistors (HEMTs) have desirable intrinsic capacity for handling large current and power densities due to the unique material properties of GaN such as large band gap, high electron saturation velocity and high critical breakdown strength [5, 6]. However, the full potential of GaN HEMT has still not been fully realised due to the inherently low thermal conductivities of the conventional substrates used for GaN epitaxial growth e.g., Sapphire (K_{Sapp}=35 W/m-K), Si (K_{Si}=150 W/m-K) and SiC (K_{SiC}=490 W/m-K). Low thermal conductive substrate hinders the fast dissipation of lattice heat (self-heat) which is generated in the device during high-power operation of GaN HEMTs. The high retention of heat results in the increase of channel temperature, which leads to the degradation of direct current (DC) and radio frequency (RF) performance [50, 51]. The root cause of variation in device performances can be identified by investigation the self-heating effect on the equivalent circuit parameters of the GaN HEMTs. Therefore, a more precise equivalent circuit (22-elements) parameter extraction methodology is used in this study. Polycrystalline diamond is now emerging as the best thermal conducting substrate (1000-2000 W $m^{-1}.K^{-1}$) to extract the heat from high-power handling GaN devices [30]. Typically, for GaN-on-CVD Diamond process development, the host Si or SiC substrate and GaN transition layer (growth-defect-rich stress mitigation layer) is removed. Subsequently, the remaining HEMT layers

are then bonded onto CVD-diamond which then acts as the new substrate [24]. Thus, the overall quality of the epitaxial GaN layer will be affected in this substrate transfer process. This may lead to variation in the hetero-interface trap and buffer trap behaviour of GaN HEMT-on-Diamond. Detailed characterization methodologies for the investigation of self-heating effect and trapping behaviour are described later in this chapter .

2.2 AlGaN/GaN HEMT Principle

GaN crystalline structure is typically wurtzite and is more thermodynamically stable as compared to the Zinc blend and Rock Salt structure. The wurtzite structure of Gallium (Ga) and Nitrogen (N) atom - face are shown in Fig. 2.1 (a) and (b), respectively. The distribution of valence electrons in the GaN bonding is strongly asymmetric due to the electron affinity difference between Ga and N atoms [45].



(a) (b)

Figure 2.1 Crystal structure and polarization field in (a) Ga-face and (b) N-face GaN [52].

In the case of GaN crystal unit cell, Ga and N atoms are bounded partially covalent and partially ionically. The electronegativity difference of ~ 1.4 eV in GaN results in the ionicity of bonding ~ 40% [53]. The difference in ionicity leads to polarization in GaN. This kind of polarization without any external influence, such as an applied electric field or strain in the crystal lattice is called spontaneous polarization (P_{SP}). Another type of polarization is known as piezoelectric polarization (P_{PE}) which occurs due to deformation in the crystal lattice under external field or internal forces or stress. In the case of AlGaN/GaN heterostructure structure, the piezoelectric polarization occurs in the thin AlGaN layer, as it is below the critical thickness. Therefore, in AlGaN/GaN HEMT, both types of polarization occur to form 2DEG. Both the PE and SP occur in the same direction (See Fig. 2.2), and the total polarization in AlGaN/GaN interface can be written as [$P = P_{PE} + P_{SP}$] [54].

The total induced sheet charge (σ) is created at the interface between the AlGaN layer and the GaN layer of AlGaN/GaN heterostructures and can be expressed as [53];

$$|\sigma| = |P_{SP-AlGaN} + P_{PE-AlGaN} + P_{SP-GaN}|$$

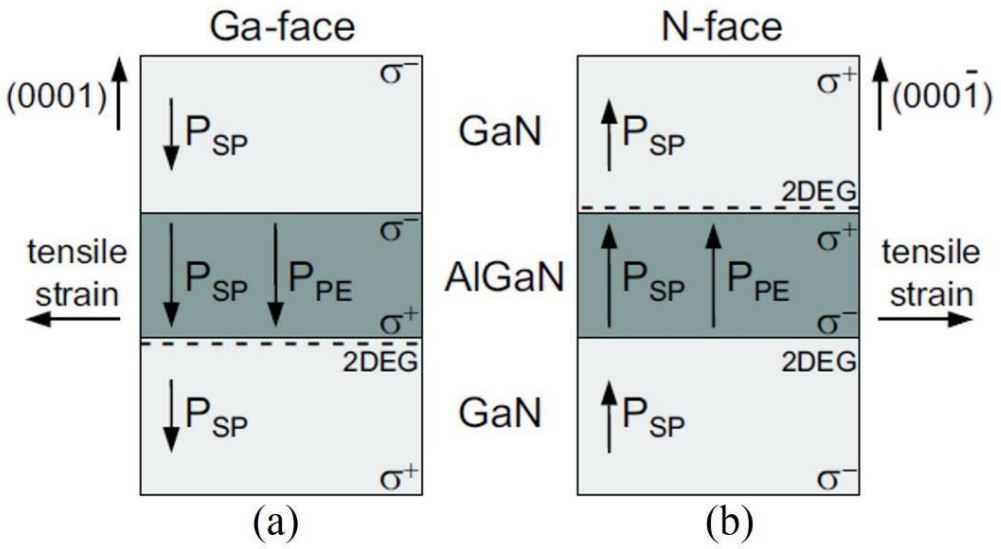


Figure 2.2 Spontaneous- and piezoelectric-polarization and the polarization induced sheet charge in AlGaN/GaN heterostructures with (a) Ga-face and (b) N-face [54].

The spontaneous polarization increases with increasing the Al mole fraction (x) in $Al_xGa_{1-x}N$ which results in the increase of total charge density. The sheet carrier concentration of a 2DEG and its dependence on alloy composition can be predicted for strained AlGaN/GaN based heterostructures. The total sheet carrier concentration n_s can be calculated using total sheet charge density and can be expressed as:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\varepsilon_0\,\varepsilon_r(x)}{q^2 d}\left[q\,\phi_b(x) + E_F(x) - \Delta E_c(x)\right]$$

where σ is the total sheet charge density, q is the electron charge, ε_0 is vacuum permittivity and ε_r is the relative permittivity, d is the thickness of the AlGaN barrier, $q\phi_b$ is the Schottky barrier of the gate contact on top of

AlGaN (or GaN cap layer), E_F is the position of the Fermi level with respect to the edge of the GaN conduction band energy, and $\Delta E_c(x)$ is the offset of conduction band energy at the AlGaN/GaN interface.

Polarization induced 2DEG sheet carrier density in AlGaN/GaN heterostructure for different thickness of AlGaN barrier is shown in fig.2.3.

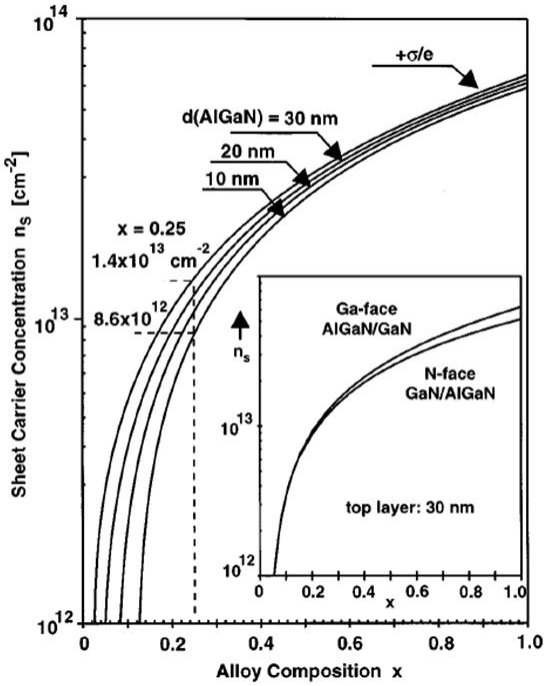


Fig.2.3 The sheet carrier concentration of 2DEG in $Al_xGa_{1-x}N$/GaN HEMT for different thickness of AlGaN barrier [54]

In the AlGaN/GaN HEMT epitaxy layer, the top layer is generally an undoped thin (2-3 nm) GaN layer. The undoped GaN cap layer has the advantage of large Schottky barrier height (> 1 eV) and gate metal is directly formed on this layer in this work. Below the GaN cap layer, there is an undoped thin (8-25 nm) AlGaN barrier layer [55, 56], which primarily

induces electrons into 2DEG and hinders hot-electron spilling over into the barrier. Below the AlGaN barrier layer, there is an undoped thick (~ 1 μm) GaN channel layer that has a lower bandgap than AlGaN barrier layer. Due to the large polarization difference between AlGaN barrier and GaN channel layer, a thin layer of 2DEG is formed in the GaN HEMT. GaN layer below the GaN channel is called the buffer layer which helps to reduce the parallel leakage current and parasitic capacitance between the source and drain electrodes. The GaN buffer layer could be un-doped, C doped or Fe doped based on the optimization of buffer quality for high-frequency high power application. Below the GaN buffer layer, GaN transition layer is one of the important epitaxy layers. GaN transition layer helps to accommodate the strain and TEC mismatch between the substrate and GaN buffer layer. The lattice mismatch between GaN and substrate is 3.6%, 13.8%, 17% for SiC, Sapphire and Si substrate, respectively [57]. Finally, the bottom part is the substrate. Generally, Si, Sapphire, or SiC substrate is used for GaN growth for GaN-based HEMT development. The substrate plays an important role in heat dissipation from the device during the operation [52-54]. Therefore, a substrate with high thermal conductivity is preferred. Good thermal conductivity of substrate is essential for high power AlGaN/GaN transistors to minimize the mobility-related performance degradation with fast dissipation of self-heat generated in GaN HEMTs at high power density.

Epitaxial growth of AlGaN barrier layer over GaN layer develops

large total polarization and develops a positive sheet charge density in the bottom of AlGaN layer which induces accumulation of free mobile electrons in the top of GaN layer in order to compensate positive charges. The induced mobile electrons are confined in the triangular quantum well at the interface of AlGaN/ GaN and form a two-dimensional electron gas (2DEG) conducting channel. Typically, the 2DEG carrier density is of ~ 1×10^{13} cm^{-2} in $Al_xGa_{1-x}N$/GaN heterostructure for $x\cong$ 0.2-0.5 [50-57]. The 2DEG channel is well separated from the top charge supply layer, the parasitic effects such as Coulomb scattering can be mitigated, thus resulting in a significant enhancement of electron mobility in the channel. The 2DEG quantum well is located in the un-intentionally doped GaN material. Impurity scattering can also be strongly reduced, resulting in an enhancement in the mobility of 2DEG electrons. The enhanced electron mobility in the 2DEG channel is the most important feature of the high electron mobility transistors (HEMTs).

In the thermodynamic equilibrium condition, the AlGaN/GaN heterostructure has a constant fermi level (E_F). The ΔE_C is a conduction band offset between AlGaN and GaN. Figure 2.4 shows the epi structure of AlGaN/GaN HEMTs and the energy band diagram with 2DEG formation. These 2DEG charge densities become the source for current flow in the channel of HEMT device.

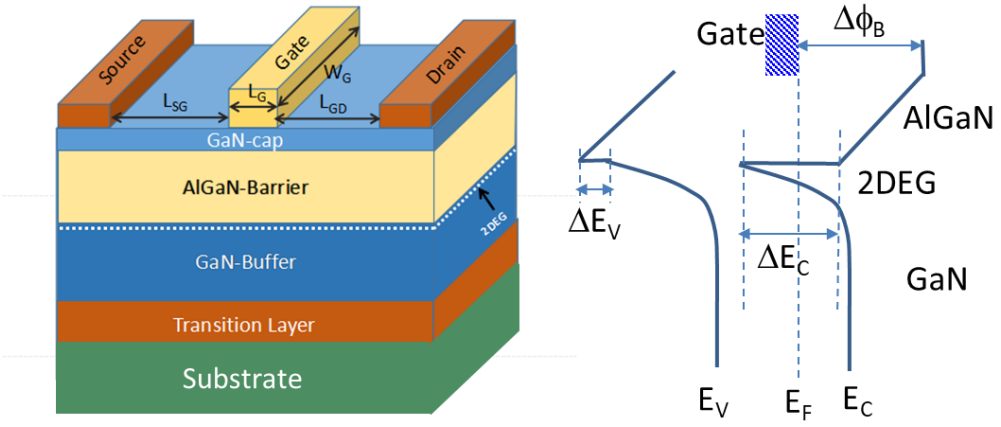


Figure 2.4 The schematic cross-section and respective energy band diagram of a typical AlGaN/GaN HEMT.

The 3D structure of GaN HEMT is shown in Fig. 2.4 whereby the 2DEG electron can move freely in two dimensions but is tightly confined in the third dimension. The 2DEG electron in AlGaN/GaN HEMT confined to a quantum well leads to quantized energy level and exhibits higher effective mobilities than those in MOSFET. The function of gate is to control the 2DEG density and hence the source-drain current in the channel of the device. In the conventional AlGaN/GaN HEMT, due to large inherent polarization, the high-density 2DEG presents even at no external gate bias (V_g= 0 V) is also known as D-mode (depletion mode). In this thesis, the D-mode AlGaN/GaN HEMT is used for device fabrication and analysis of device performance. The depletion of 2DEG depends on the gate bias condition. If the gate bias is positive (V_g = 0 V), more electrons are accumulated in the 2DEG quantum well, resulting in enhanced 2DEG density and increased source-drain current density. When the gate bias is

negative (V_g < 0V), electrons are depleted from the quantum well, resulting in reduced 2DEG density and decreased source-drain current density (See Fig. 2.5). The 2DEG is completely depleted at a certain gate voltage called pinch-off voltage.

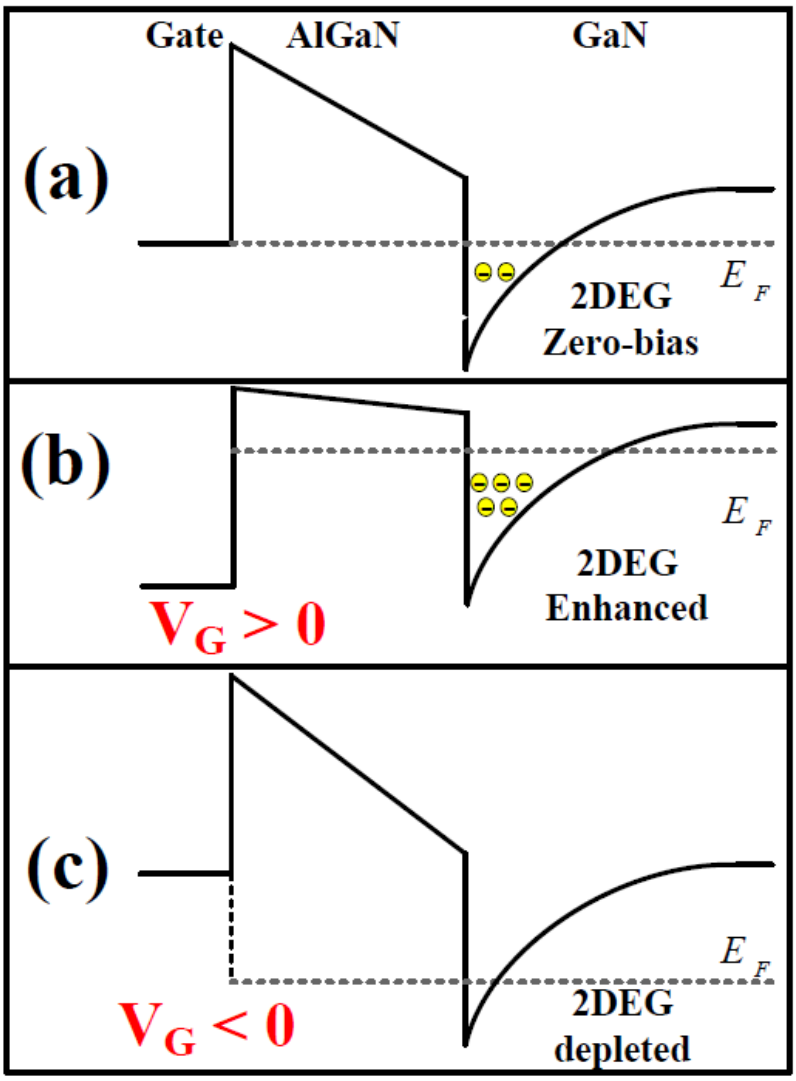


Figure 2.5 The energy band diagram of AlGaN/GaN HEMTs at (a) unbiased gate (b) positive gate bias, and (c) negative gate bias [58].

The GaN HEMT is generally grown using molecular beam epitaxy (MBE) or Metal-organic chemical vapor deposition (MOCVD) technique. After the growth of AlGaN/GaN HEMT, the 2DEG properties of HEMT are evaluated in terms of parameters such as, 2DEG carrier concentration (n_s), electron mobility (μ), and sheet resistance (R_{sh}).

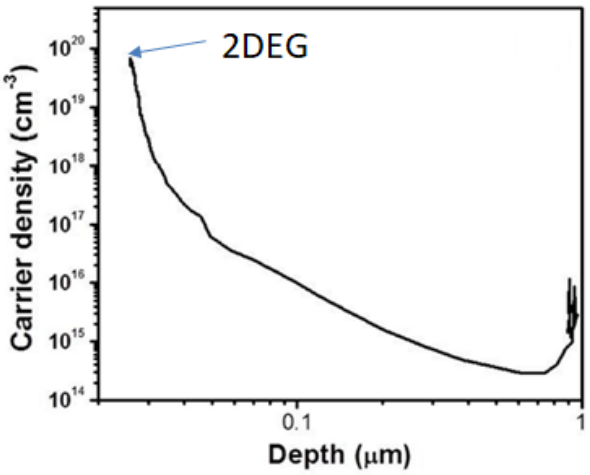


Figure 2.6 Typical depth versus carrier density profile of AlGaN/GaN HEMT [59].

Figure 2.6 shows the typical depth versus carrier density profile of AlGaN/GaN HEMT-on-Si substrate. The high carrier density (~ 10^{19} cm^{-3}) is at the interface between the AlGaN barrier and GaN channel region. Generally, background carrier density of ~ 10^{15} cm^{-3} exist in GaN layer. However, increased carrier density near the GaN/substrate interface was observed which could be due to interdiffusion at the GaN/substrate interface. This can be minimized by improving the epitaxy growth method by eliminating the degenerate layer at GaN/substrate interface [60].

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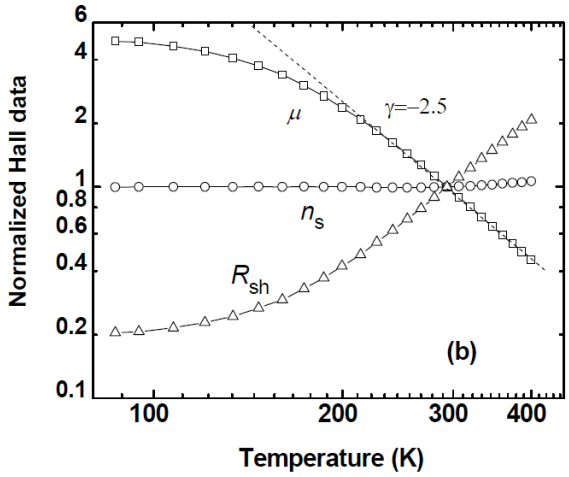


Figure 2.7 Temperature dependence sheet carrier density (n_s) and mobility (μ) and R_{sh} of AlGaN/GaN HEMT [59].

Typically, n_s in AlGaN/GaN HEMT is affected very little by temperature in the typical operating range of ~300 to 450 K (See Fig. 2.6) [59]. On the contrary, the 2DEG carrier mobility degrades with increasing temperature due to the optical phonon scattering [61,62]. The 2DEG mobility generally follows power-law relation with the temperature at T > ~ 200 K.

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{\gamma}$$

$\mu(T)$ is the mobility at required temperature T, μ_0 is the mobility at room temperature 300 K, and γ is the mobility exponent power index. The γ values are reported in between -1.5 to -2.7 for AlGaN/GaN HEMT. The 2DEG sheet resistance (R_{sh}) of GaN HEMT can be calculated as per the following expression

$$R_{sh} = \frac{1}{qn_s\mu}$$

The R_{sh} is inversely proportional to the n_s and μ. The degradation in R_{sh} is mainly by temperature dependence μ in the 2DEG.

The device is developed on the grown AlGaN/GaN hetero-structure and called AlGaN/GaN HEMTs in this thesis. The AlGaN/GaN HEMTs is a three-terminal transistor device which consists of three electrodes named Source (S), gate (G), and drain (D) (See Fig. 2.8).

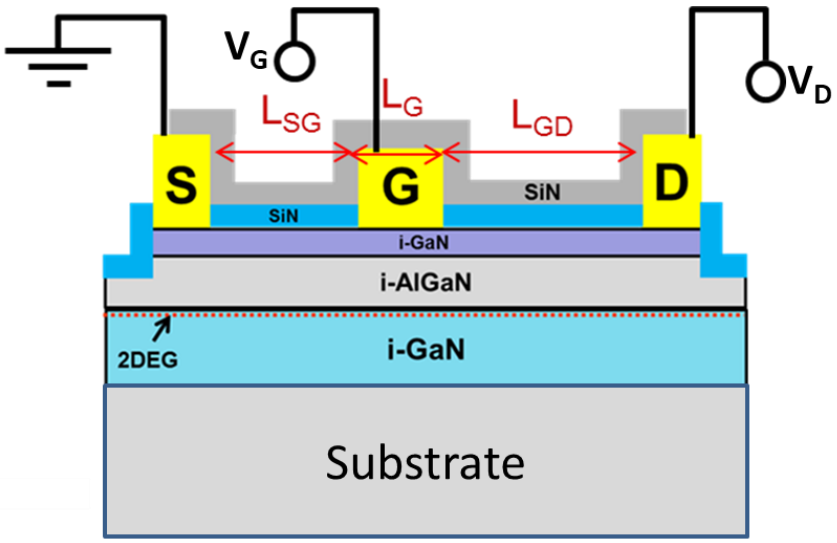


Figure 2.8 The schematic of AlGaN/GaN HEMTs with a bias terminal for DC *I-V* characteristics.

The source (S) and drain (D) are ohmic contacts and gate (G) is the Schottky contact. The source and drain electrodes are connected through the conducting 2DEG channel. During the device operation, drain

voltage (V_D) is applied at drain contact and source is grounded, current flow between drain and source called drain current (I_D). The gate electrode forms the Schottky contact and remains separated from the 2DEG channel. The gate voltage (V_G) is applied to control the electron density in the 2DEG channel and termed as modulation of channel current. The basic electrical characteristics of GaN HEMTs are known as Direct current (DC) and radio frequency (RF) characteristics.

The maximum current density (I_{dmax}) and maximum transconductance (g_m) of the intrinsic GaN HEMT device can be approximately estimated from the values of n_s and μ of grown AlGaN/GaN HEMT, assuming the saturation velocity model, using the following expressions:

$$I_{dmax} = q.n_s.v_{sat}$$

$$g_m = \frac{v_{sat}C_{gs}}{L_g}$$

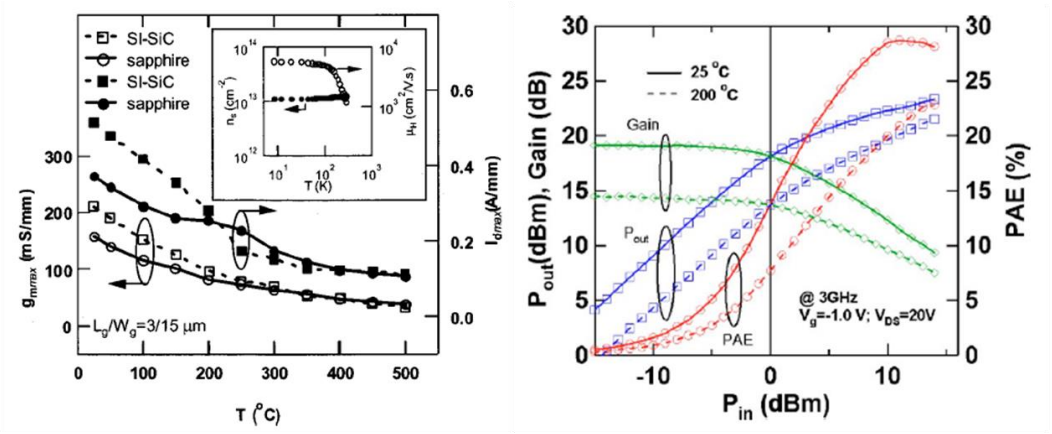
where q is the electron charge, n_s is the density of 2-DEG and v_{sat} is the electron saturation velocity. v_{sa} is equal to E.μ_e where E is the electric field strength and μ_e is the DEG effective carrier mobility. So, it is clear that I_d is directly proportional to μ_e. Therefore, the degradation in 2DEG carrier mobility directly affects the I_d when n_s is constant.

2.3 The self-heating in AlGaN/GaN HEMTs

Under high voltage and high-power operation, large current density flows in the channel region of the AlGaN/GaN HEMTs which in turn generates a significant amount of heat in the device. When the substrate of HEMT is not a good conductor of heat, the heat generated in the device channel region will be retained which further increases the lattice temperature [14]. This increase in lattice temperature is due to the collisional energy loss from the 2DEG electrons to the crystal lattice [63]. The increase in channel temperature at the gate-edge of the gate-drain region (hot-spot) is much higher than the ambient temperature of the device. This significant increase in temperature at the hot spot region affects the 2DEG transport properties, which in turn affects the mobility of electrons in 2DEG. The reduced mobility results in a drop in device current density with increased drain bias voltages (at constant gate voltage). The approximate temperature dependence of 2DEG mobility due to lattice scattering is $T^{-\gamma}$ where γ could be in between 1.5 to 2.7 [61].

Researches have reported the effect of temperature on 2DEG properties of GaN HEMT and device parameters. Figure 2.8 shows the dependence of n_s and μ_e of a HEMT heterostructure at elevated temperatures and its effect on device parameters g_{mmax} and I_{dmax} [64]. From figure 2.9 (a), it is clear that the μ_e decreases significantly with temperature beyond ~ 200 K

while n_s is unaffected till ~ 400 K of temperature. The degraded 2DEG properties also affect the RF power of GaN HEMTs (See Fig. 2.8 (b)).



(a) (b)

Figure 2.9 (a) The 2-DEG mobility and (b) RF power performance degradation with the increase of temperature in GaN HEMTs-on-Si and SiC substrates [64].

So, it is understood that the self-heating raises the channel temperature and degrades 2DEG mobility which causes the reduction of I_d and g_m.

The rise of the channel temperature of GaN HEMTs is different for different substrates (See Fig 2.10). The GaN-on-sapphire exhibited a maximum rise of channel temperature when compared to GaN-on-Si and GaN-on-SiC. At room temperature, the thermal conductivity of sapphire substrates is ~4 times lower than Si and ~ 10-times lower than that of SiC [(K_{Sapp}=0.35 W/cm-K), Si (K_{Si}=1.5 W/cm-K) and (K_{SiC}=4.9 W/cm-K)], which results in much higher channel temperature in GaN HEMTs-on-Sapphire substrate. Kuzmik et al. have reported the GaN HEMTs channel

temperature of ~ 320°C for sapphire and ~ 95 °C for Si substrate at 6 W/mm of dissipated power density.

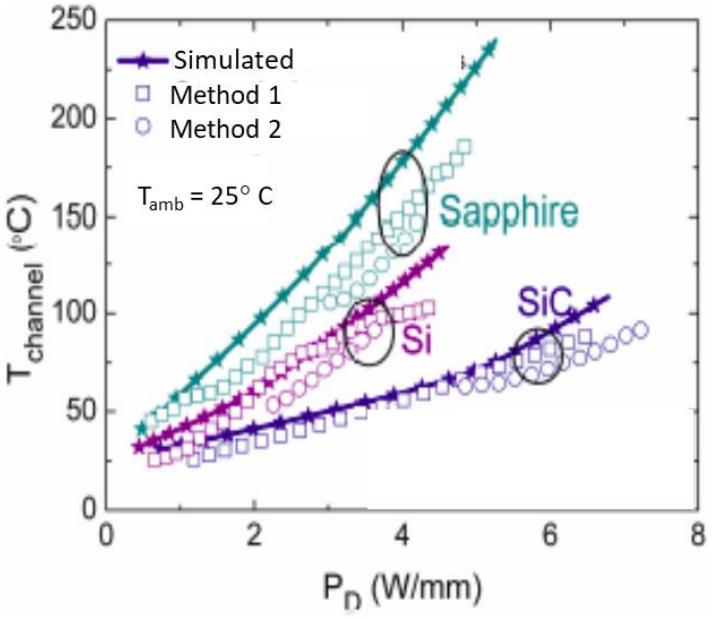


Figure 2.10 Comparison of the channel temperature versus dissipated power density (P_D) in GaN HEMTs on Sapphire, Si and SiC substrates [19].

From fig. 2.10, it is clear that the channel temperature reaches ~150° C at 4 and 5 W/mm of P_D in GaN HEMTs on-Sapphire and Si, respectively. GaN HEMTs-on-SiC substrate can be operated at higher P_D (8-10 W/mm) before it reaches a channel temperature of 150 °C. To further increase P_D in GaN HEMTs with a channel temperature lower than 150 °C, a high thermal conductive substrate is required. Recently, GaN HEMTs-on-diamond has been explored to work at a higher P_D of ~20 W/mm while keeping the channel temperature lower than 150 °C. To

further expand the suitability of diamond substrate for GaN HEMT a detailed device characterization and the effects of self-heating at higher voltages are required.

The self-heating effect in the GaN HEMTs can primarily be observed in the electrical characteristics in continuous wave (CW) DC measurements. In addition, channel temperature of device can also be estimated through electrical measurements [18, 19].

2.4 Electrical characterization and self-heating of AlGaN/GaN HEMTs

Effect of self-heating on device performance of AlGaN/GaN HEMT's can be quantitatively evaluated by -

- DC characterization
- Small-signal RF characterization

2.4.1 DC measurements of AlGaN/GaN HEMTs

The DC characteristics are typically presented by the output characteristics (I_D-V_D) and the transfer characteristics (I_D-V_G). On-wafer DC measurements are typically carried out using a probe station and a source measurement unit (SMU). The DC measurement setup block

diagram for the DC output and transfer characteristic measurements is shown in figure 2.11.

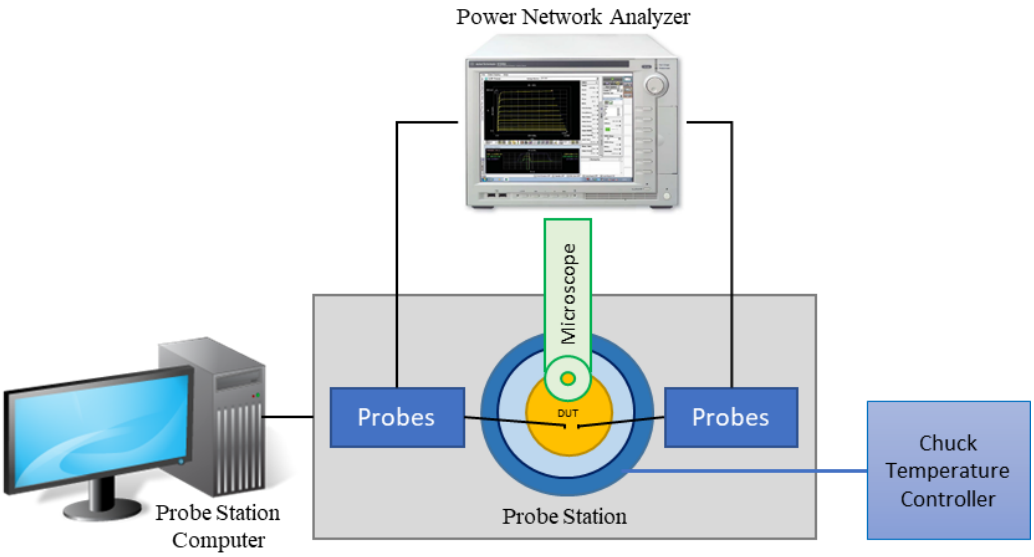


Figure 2.11 The typical block diagram of DC measurement setup.

Figure 2.12 shows the typical I_D-V_D characteristics of AlGaN/GaN HEMTs. In the linear region for which the drain current is proportional to the V_D, the maximum value of the current density (I_D) obtained in the device is called I_{Dmax}. The drain-source resistance (R_{DS}) can be estimated from the slope in the linear region of I_D-V_D curve at $V_G = 0$ V and is called static on-resistance (R_{on}). In the saturation region, the I_D typically remains quasi-independent of the V_D. However, we observe the I_D reduction beyond the I_{dmax} (See Fig. 2.12) with an increase in drain voltage (V_D). Such current reduction occurs mainly due to the self-heating in the device. Detailed discussion on self-heating and root cause is discussed later in this chapter.

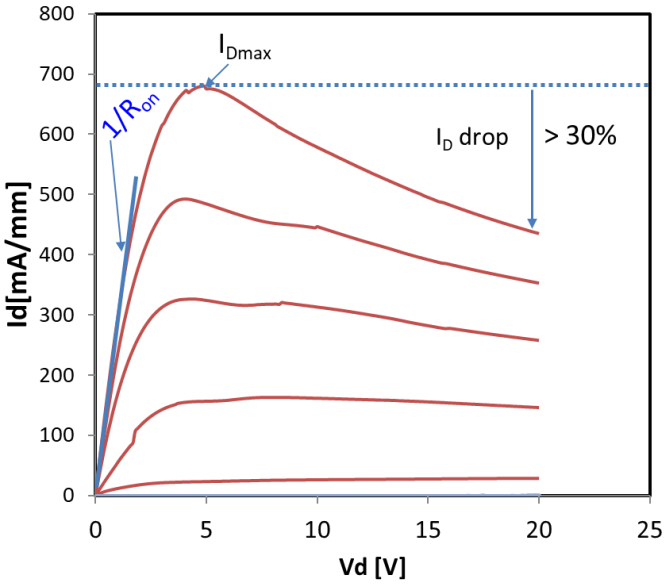


Figure 2.12 Typical DC I_D-V_D output curve characteristics of AlGaN/GaN HEMTs.

Figure 2.13 shows the transfer characteristics of AlGaN/GaN HEMTs. The transconductance (g_m) can be estimated by the derivative of I_D with respect to V_G.

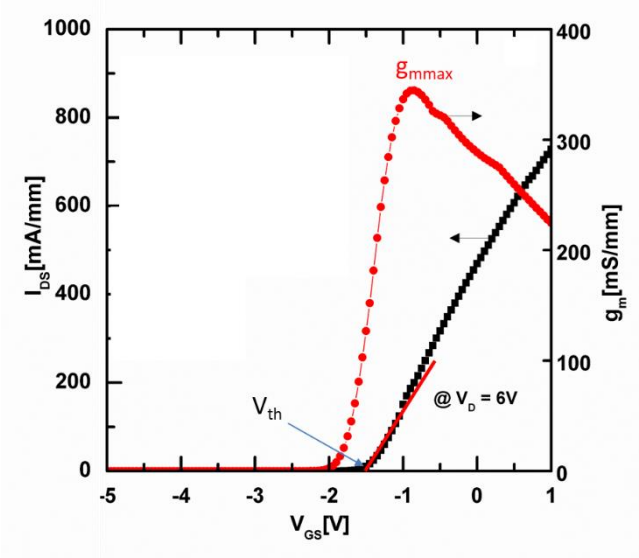


Figure 2.13 DC I_D-V_G transfer characteristics of AlGaN/GaN HEMTs.

The maximum value of g_m is called g_{mmax} which is a key parameter to decide the cut-off frequency of device. The g_m value decreases beyond g_{mmax} due to increasing source and drain resistance, thermal effect as well as the presence of defects in the structure.

The output power (P_{out}), power gain, and power-added efficiency (PAE) are key parameters of RF power transistors. The maximum RF output power of AlGaN/GaN HEMTs can also be estimated from DC I_D-V_D output characteristics (See Fig. 2.14) using the following equation [18];

$$P_{out,max} = \frac{\Delta I_D \Delta I_V}{8} = \frac{I_{Dmax}(V_{br} - V_{knee})}{8}$$

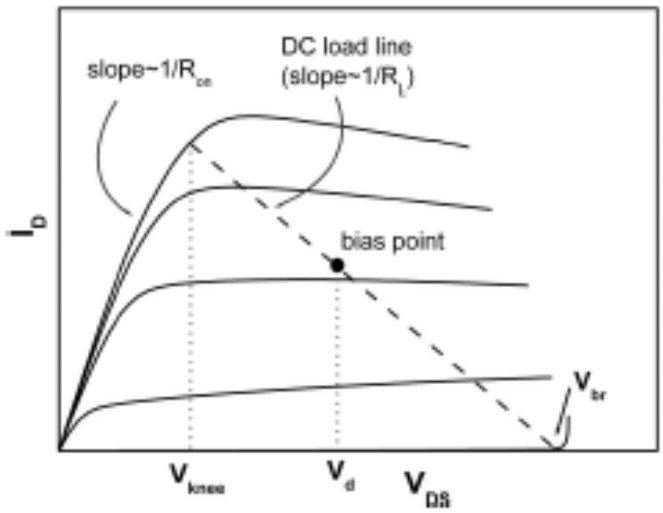


Figure 2.14 Load line in typical DC output characteristics of a Class A power amplifier [58].

The P_{out} of AlGaN/GaN HEMTs can be increased by increasing I_{dmax}, minimizing the knee voltage, and increasing the breakdown voltage. The V_{knee} can be minimized by reducing the source-drain resistance (R_{DS}). However, due to the self-heating in the device, P_{out} can be degraded due

to reduced I_{dmax} and increased V_{knee}.

2.4.2 RF characterization

Basic RF performances of GaN HEMTs are evaluated by small-signal S-parameter characterization. A typical S-parameters (Scattering parameter) measurement setup uses Probe station, Vector network analyzer, and the source measurement unit (SMU) (See Fig. 2.15).

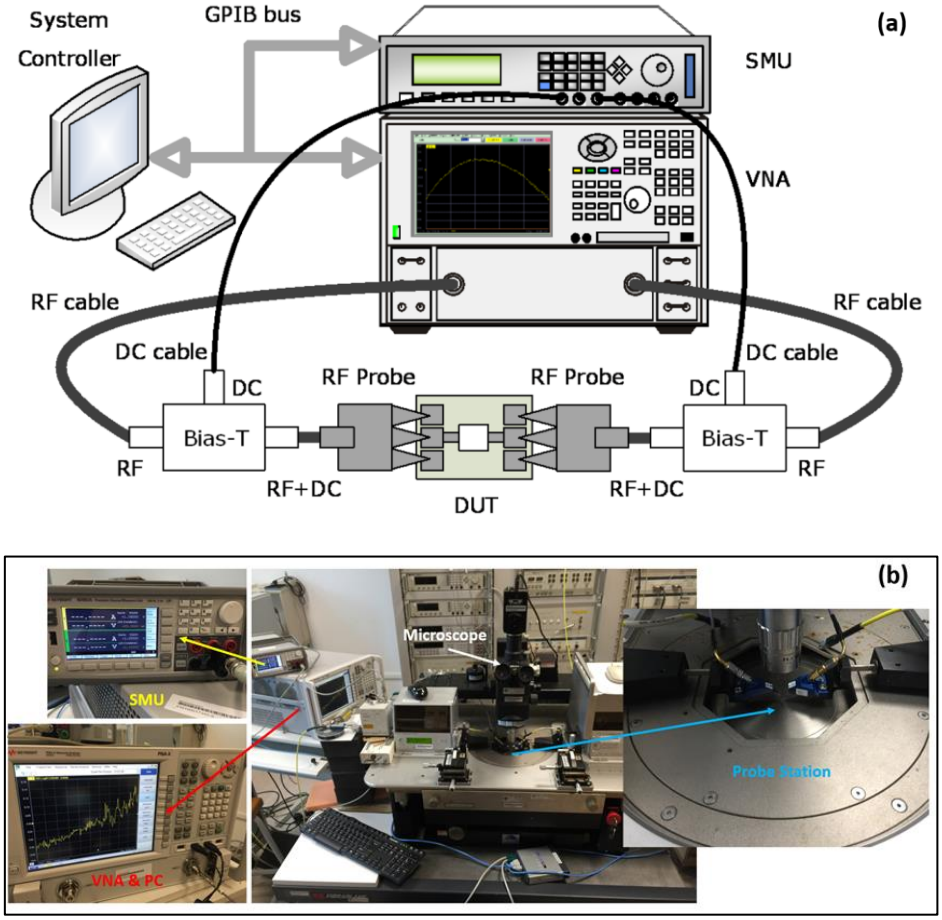


Figure 2.15 (a) A schematic of measurement setup and (b) actual image for on-wafer RF characterization of the device.

S-parameters are mostly used for networks operating at RF and microwave frequencies, where signal power and energy considerations are more easily quantified than voltages and currents at the input and output ports. Two-port S-parameters are most commonly used to define the small-signal gain, input, and output impedance properties of any linear two-port network. Typically, the S-parameter measurements are carried out at characteristic impedance, Z_0 = 50 Ω. A typical two-port network is shown in Fig. 2.16.

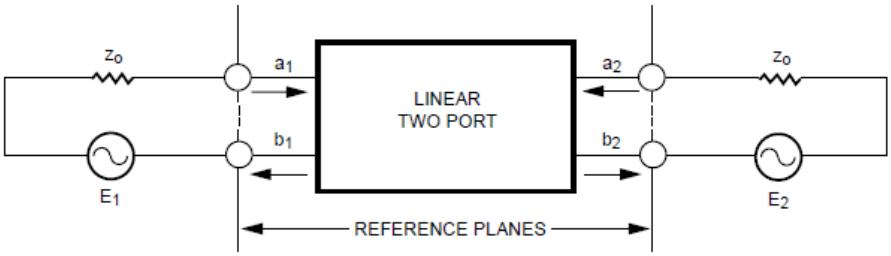


Figure 2.16 A typical diagram of a two-port network.

S-parameters are defined analytically in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where,

a_1 = (Incoming power at Port 1)$^{1/2}$, b_1 = (Outgoing power at Port 1)$^{1/2}$

a_2 = (Incoming power at Port 2)$^{1/2}$, b_2 = (Outgoing power at Port 2)$^{1/2}$

E_1, E_2 = Electrical Stimuli at Port 1, Port 2, Z_0 = Characteristic Impedance

Defining linear equations for E_1 = 0, then a_2 = 0, and:

$$S_{11} = \frac{b_1}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{\frac{1}{2}}$$

$$S_{21} = \frac{b_2}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{\frac{1}{2}}$$

$$= [\text{Forward Transducer Gain}]^{\frac{1}{2}}$$

Similarly, at Port 2 for $E_1 = 0$, $a_1 = 0$:

$$S_{12} = \frac{b_1}{a_2} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Output Power}}\right]^{\frac{1}{2}}$$

$$= [\text{Reverse Transducer Gain}]^{\frac{1}{2}}$$

$$S_{22} = \frac{b_2}{a_2} = \left[\frac{\text{Outgoing Output Power}}{\text{Incoming Output Power}}\right]^{\frac{1}{2}}$$

$$= \text{Output Reflection Coefficient}$$

Usually, the magnitude of S-parameters is expressed in decibels (dB) below:

$| S_{11} |\ dB = 10\ log_{10} | S_{11} |^2 = 20\ log_{10} | S_{11} |$, $| S_{22} |\ dB = 20\ log | S_{22} |$

$| S_{21} |\ dB = 20\ log | S_{21} |$, $| S_{12} |\ dB = 20\ log | S_{12} |$

In the RF characteristics, the small-signal microwave characteristics evaluate the current gain cut-off frequency (f_T) and power gain maximum oscillation frequency (f_{max}) of HEMTs device. These are two important performance parameters for RF transistors. A f_T is the frequency at which the short circuit current gain becomes unity ($20\log(h_{21}) = 0$ dB) and f_{max} is the frequency at which power gain (U) of device is unity. These parameters are estimated from the measured *S*-parameter of the device.

The stability factor (*k*), current gain (h_{21}), power gain (Maximum Available Gain (MAG), Maximum Stable Gain (MSG) or Mason's Gain (*U*)) are also determined from measured S-parameters of Device using following equations;

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

Maximum Available Gain (Use only for K > 1)

$$MAG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}$$

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}S_{21}|}$$

$$D = S_{11}S_{22} - S_{12}S_{21}$$

Maximum Stable Gain (Use only for *K* < 1)

$$MSG = \frac{|S_{21}|}{|S_{12}|}$$

Mason's Gain (Use for all *K*)

$$U = \frac{S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

The maximum oscillation frequency is the highest operating frequency with power gain > 0 dB of a transistor. It is also possible to model the GaN HEMTs using its physical parameters to a small-signal equivalent circuit. A typical plot of f_T and f_{max} for AlGaN/GaN HEMTs are shown in fig. 2.17

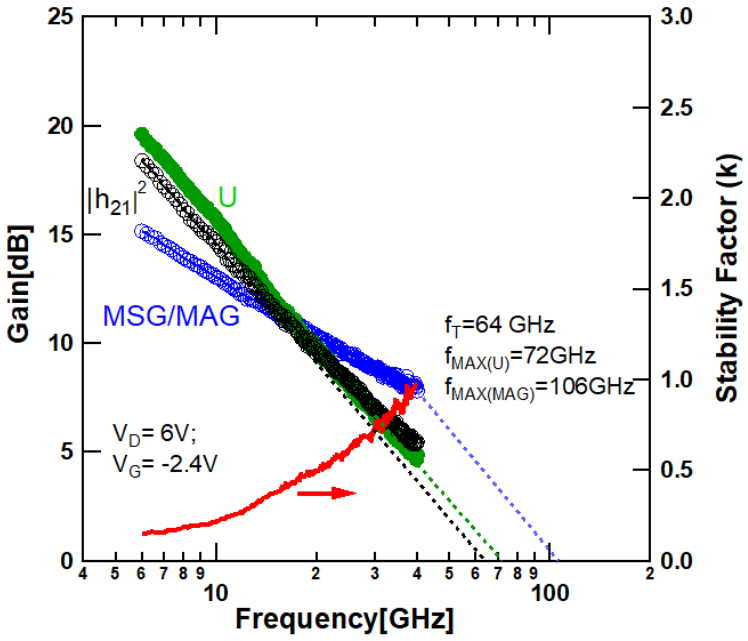


Figure 2.17 A typical gain versus frequency plots for the determination of f_T and f_{max} [56].

The microwave performance of device depends on 2DEG properties of HEMT epitaxy structure, device geometry, and process involved for its fabrication. For the development of monolithic microwave integrated circuit (MMIC) effective utilization of this HEMT device in circuit design is important. It is also important to establish an equivalent circuit for this device. Equivalent circuit models apply a circuit element to a physical attribute of the device. Fig 2.18 shows the electrical equivalent circuit model to represent the HEMT device.

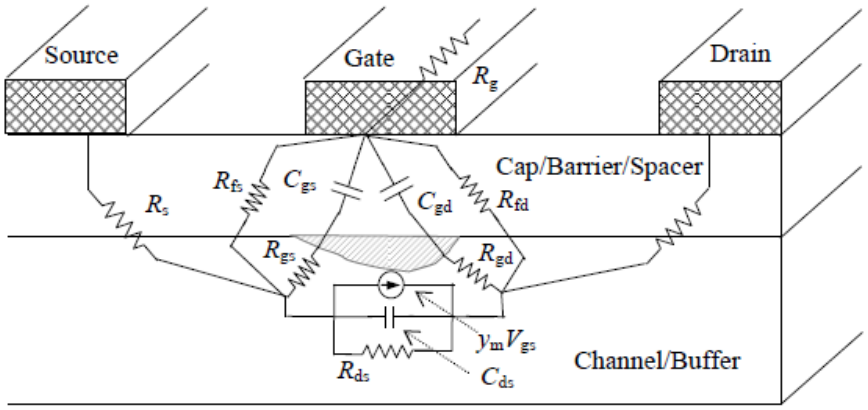


Figure 2.18 The schematic of the cross-section and the physical origins of the small-signal equivalent circuit for a GaN HEMT [65].

The RF performance of the device depends on the quantitative values of these circuit elements which can vary with the bias voltage and the channel temperature [35, 67]. Fig. 2.19 shows the degradation of f_T with an increase of channel temperature [35]. It is suspected that the equivalent circuit parameters get affected by the increased channel temperature in the device at high power density operation. Therefore, it is necessary to extract the small-signal equivalent circuit parameters and investigate the relationship between these circuit parameters and the variations in the device DC & RF performance due to self-heating.

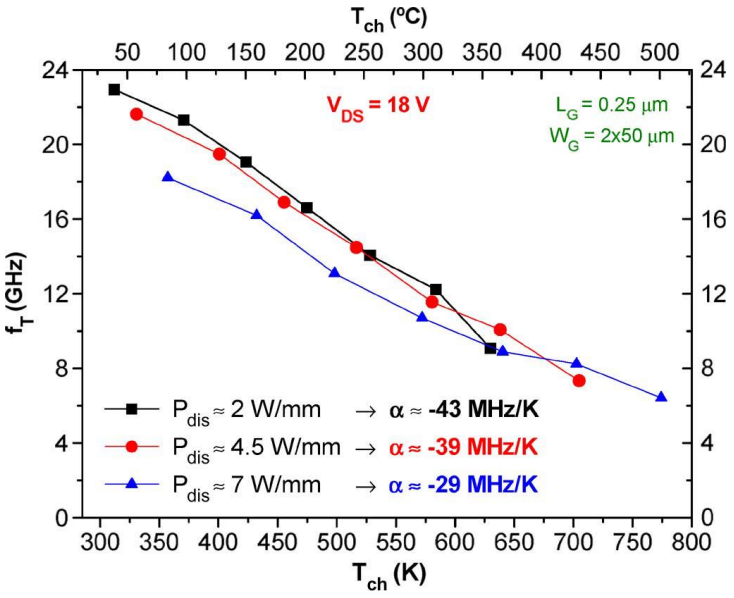
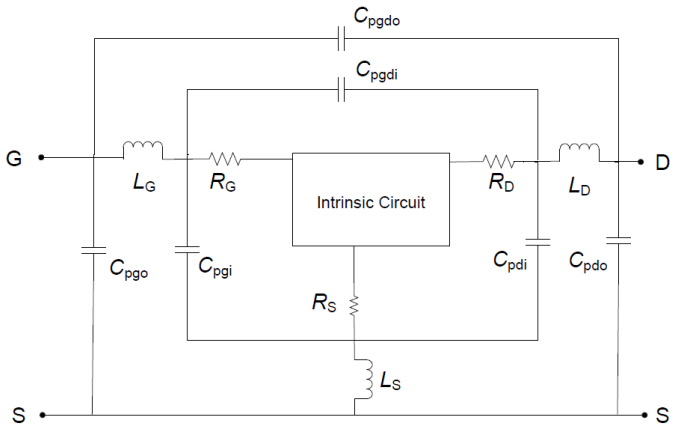
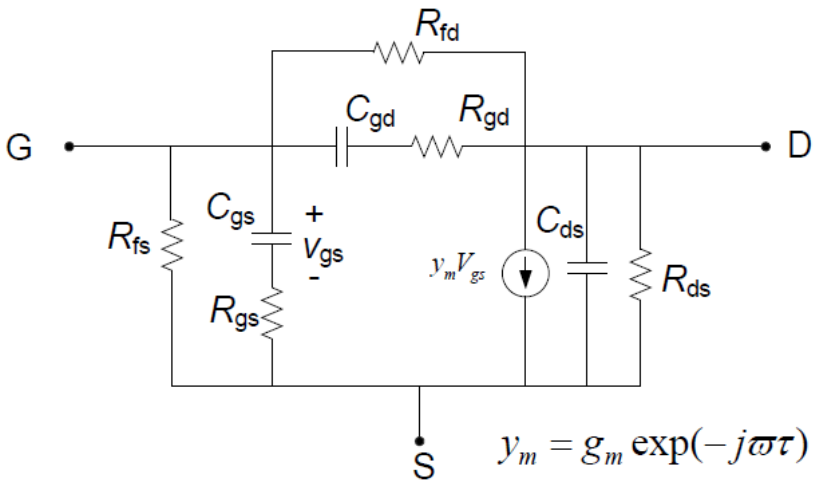


Figure 2.19 Dependence of f_T with the channel temperature at different dissipated powers. The lowering of f_T is related to self-heating and parasitic effects [50].

Fig. 2.20 shows the schematic of (a) extrinsic parameters and (b) intrinsic parameters of a small-signal equivalent circuit for a GaN HEMTs [65].



(a)



(b)

Figure 2.20 (a) Extrinsic elements and (b) intrinsic elements of a small signal equivalent circuit of a GaN HEMTs.

In the extrinsic circuit, the parasitic capacitances the C_{pgo} and C_{pdo} are the pad-to-buffer/substrate capacitances and the pad-to ground/ source capacitances for gate and drain, respectively. The C_{pgdo} is the capacitance between the gate and drain pads. C_{pgi}, C_{pdi}, and C_{pgdi} are the capacitances between the interconnect metals of gate, drain and source. L_g, L_s and L_d are the parasitic inductances of the pad. R_g is the distributed gate resistances arising from the gate metal at microwave frequencies. R_s and R_d are the ohmic contact resistance in series with the AlGaN/GaN wafer resistance at the gate to source region and gate to drain region, respectively [65].

In this intrinsic circuit, C_{gs} is the capacitance due to the space

charge region between the gate and the source; C_{ds} is the capacitance of the substrate between the drain and the source. C_{dg} is the capacitance between the drain and the gate, R_{DS} is the output resistance of the channel. When the depletion width under the gate changes as a sinusoidal voltage is applied, the voltage on the gate swings from positive to negative. The $g_{m.}v_{gs}$ is the voltage-controlled current source and is dependent on the voltage on C_{gs}. When one considers the high-frequency operation of the device, the C_{gs} shorts the voltage across it becomes zero, and consequently, the output of the voltage-controlled current source decreases to zero. g_m is the gain parameter of the HEMT device. Also, these component models a delay time, τ which represents the time it takes the depletion width to respond to a change in voltage on the gate.

The parameter extraction from the measured S-parameters of GaN HEMTs-on-CVD diamond was carried out using proposed model described in the literature [65], and presented in chapter 3. The purpose of parameter extraction is to understand the effects of bias dependent self-heating on these parameters and thus variation in the device performances. After the extraction of small-signal extrinsic and intrinsic parameters, we can estimate the f_T and f_{max} of the device using the following equations [66],

$$f_T = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\right]}$$

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_G + R_S) + 2\pi f_T R_g C_{gd}}}$$

From the above equations, it is clear that the f_T and f_{max} are dependent on the values of intrinsic and extrinsic parameters, and self-heating can affect these parameters result in the variation of f_T and f_{max}. The detailed mechanism of the f_T and f_{max} variation with the self-heating is described in chapter 3

2.5 Trapping effects in AlGaN/GaN HEMTs

GaN HEMTs-on diamond, due to its higher thermal conductivity substrate, is emerging as an attractive candidate for next-generation microwave and power devices especially at a very large operating voltage and dissipated power density. However, high bias voltage generates a large electric field in the device that can cause trapping effect and performance degradation. Various kinds of trapping effects such as transconductance frequency-dispersion, threshold voltage shift, current collapse (gate- and drain-lag), and restricted microwave power output have been reported for GaN HEMTs [32]. Figure 2.21 illustrates the presence of traps in the surface, barrier, AlGaN/GaN interface, buffer, and transition regions of the AlGaN/GaN heterostructure.

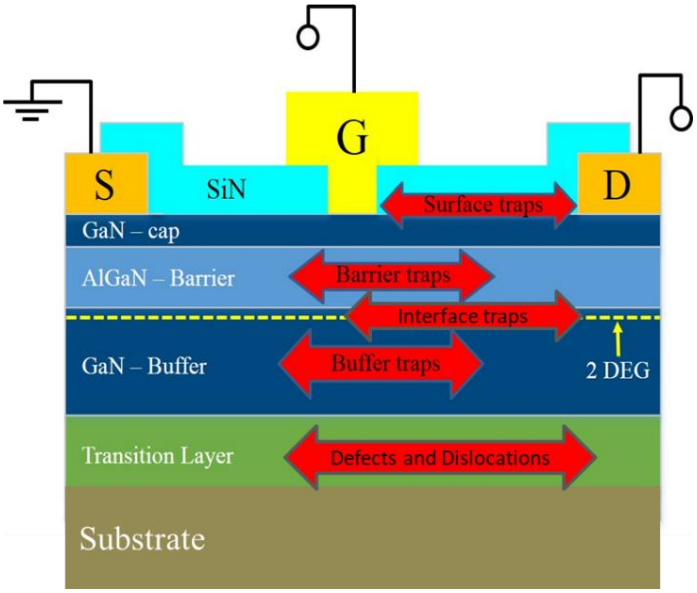


Figure 2.21 Schematic of the AlGaN/GaN heterostructure showing various trapping mechanisms.

Trapping of electrons results in the reduction of carrier density in the 2DEG channel thus leads to a reduction in the overall drain current density. Reduction of drain current density due to trapping affects the dynamic-on resistance results in degraded power figure of merit of AlGaN/GaN HEMTs for switching applications. The reduction in the drain current due to trapping is termed as "*current collapse*"[6]. The current-voltage (I_D – V_D) characteristics showing the effect of current collapse on the output power of HEMTs are illustrated in fig. 2.22.

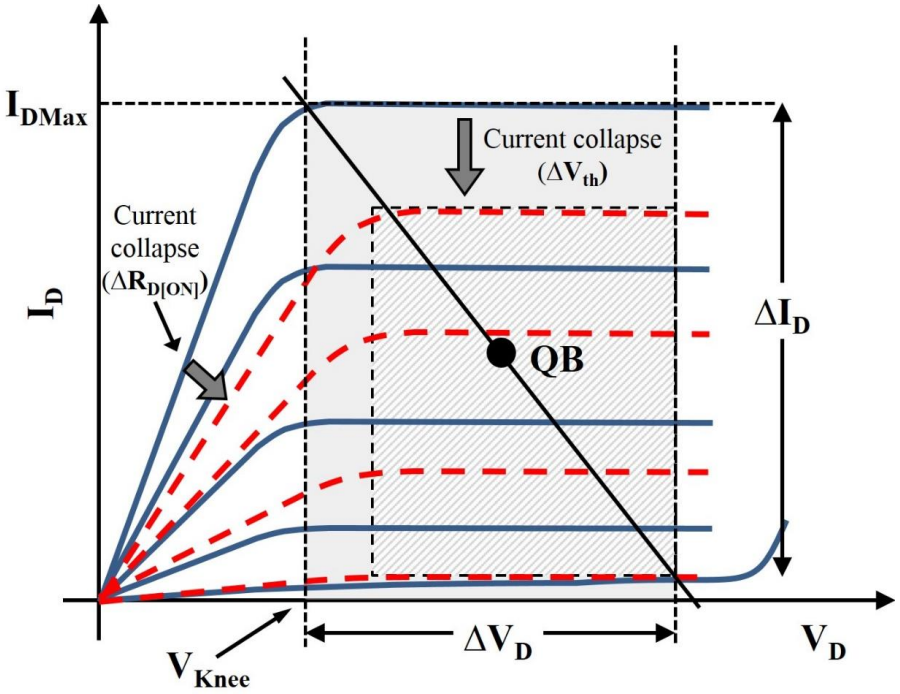


Figure 2.22 A plot of I_D–V_D characteristics for HEMTs before (solid lines) and after (graded lines) current collapse at some stress condition. Shifting the V_{knee} and reducing the I_{Dmax} will degrade the maximum attainable device output-power [67].

From the pulsed I_D – V_D characteristics, we can estimate the dynamic R_{on} of the device (See Fig.2.22). The traps in AlGaN/GaN HEMTs, which are electrically activated during device operation, are broadly classified into two types:

Surface traps [32, 68-70] are traps that exist on the GaN surface of the AlGaN/GaN HEMTs. Surface traps are more significant in GaN-based Metal-insulator-semiconductor HEMTs (MIS-HEMTs), also known as interface traps. The removal of positive charges from the GaN surface or

surface states of the heterojunction transistor causes the removal of an equal number of 2DEG electrons results in degradation of drain current is called current collapse due to surface traps [71]. The interface trap in the GaN-MISHEMTs-on-CVD diamond is presented in chapter 4. For conventional HEMTs, these surface traps can be suppressed by an effective passivation technique [72].

Bulk traps [6, 32, 68, 70] are traps that exist within the heterostructure, such as in the AlGaN barrier, AlGaN/GaN interface, GaN buffer or in GaN transition layer (See Fig. 2.21). The AlGaN/GaN interface trap is known as a hetero-interface trap. Trapping of 2DEG electron by the buffer traps present in the gate-drain access region leads to current collapse which is generally characterized by dynamic-on resistance (Dyn.R_{on}).

In this thesis, trapping characteristics are investigated for AlGaN/GaN HEMT-on CVD diamond substrate. Since GaN HEMTs-on-CVD diamond was developed from GaN HEMT-on-Si by substrate transfer process in which grown AlGaN/GaN HEMT structure on Si substrate was transferred by the complete removal of host Si substrate as well as the grown stress mitigated transition layer (AlN/GaN superlattice structure). The transferred AlGaN/GaN HEMT on CVD-Diamond is having only GaN buffer layer (i.e. without the defect-rich transition layer) may be having a different interface and buffer trap behaviour when compared with the reported AlGaN/GaN HEMTs on Si substrate. The detailed characteristics of interface trap in

GaN HEMTs-on-CVD diamond are presented in chapter 4 and chapter 5.

2.6 Trapping characterization techniques

There are various electrical characterization techniques used to investigate the trapping behaviour in AlGaN/GaN HEMTs. Pulsed I_d-V_d [60], which is caused by the capture of electrons within the AlGaN/GaN heterostructure can help to estimate the changes in drain current, on-resistance, and threshold voltage shift. Other methods are deep-level transient spectroscopy (DLTS), constant capacitance deep-level transient spectroscopy (CC-DLTS), deep-level optical spectroscopy (DLOS), frequency-dependent g_m dispersion, conductance-frequency (G-f), and current transient measurements are used in GaN HEMTs to study their trapping behaviour [32, 34, 73, 75]

2.6.1 Pulsed I_D-V_D characterization

A quick and reliable characterization of the current collapse can be obtained through the execution of pulsed drain-current versus drain (or gate) voltage measurements (pulsed I_D–V_D or I_D–V_G characterization) [75], which helps to investigate the changes in drain current, static and dynamic on-resistance, and threshold voltage induced by the capture of electrons within the AlGaN/GaN HEMTs.

The pulsed (dynamic) I_D –V_D characterization technique is considered to be a suitable technique to characterize traps in AlGaN/GaN HEMTs [76].

This technique has two distinct advantages over CW DC I_D –V_D characterization when used to examine the electrical response of the devices. First, by limiting the amount of time of measurements between bias points, thermal heating effects are minimized and respond low self-heating in the device. Second, by making measurements on a time scale that is shorter than the time constants of surface states that cause RF dispersion, pulsed I_D –V_D can effectively reflect the degraded device performance.

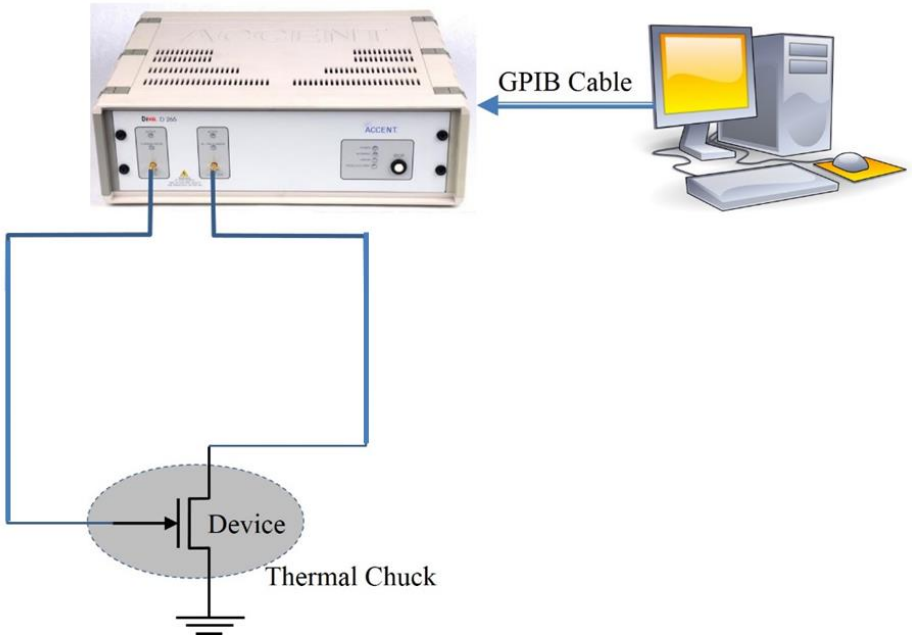


Figure 2.23 Pulsed I_D – V_D setup for GaN HEMT characterization with Accent Diva D265 analyzer.

A schematic of the pulsed I_D – V_D measurement setup using Accent Diva D265 is shown in Fig. 2.23, which is used to characterize the fabricated AlGaN/GaN HEMTs. It consists of power supplies and input/output source

measurement units which are embedded in the Accent Diva D265. The minimum pulse width of this setup is 200 ns. For pulsed I_D –V_D measurements, voltage signals of the square pulse are applied from a static quiescent bias point to obtain currents before the end of the pulse duration and, then, devices under test returns to and stay at the quiescent bias point until the next voltage pulse is applied.

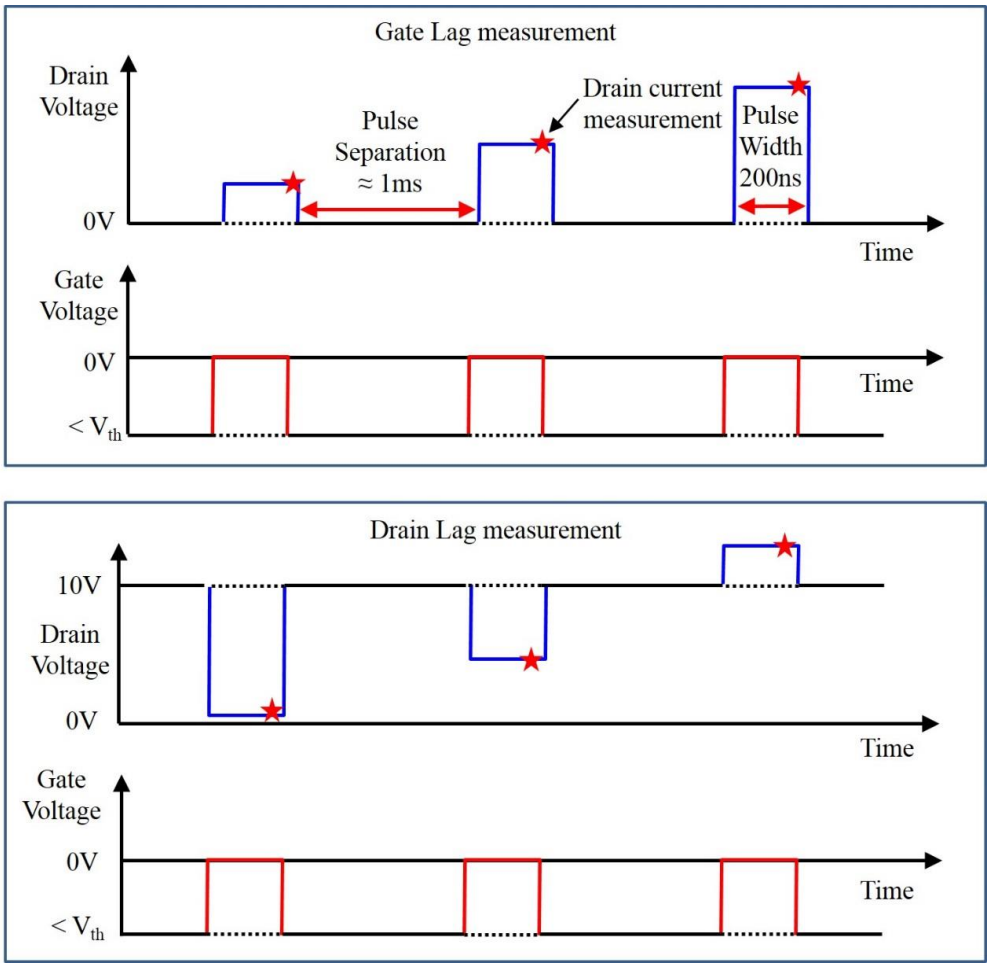


Figure 2.24 The applied voltage and time plot for pulsed I_D – V_D for gate lag condition and drain lag condition [77].

If the pulse duration is short enough compared with the separation time

between consecutive voltage pulses, both temperature and trapping effects are dependent mainly on the quiescent bias point. In the case of very short pulse duration and large pulse width (duty cycle < ~ 0.01 %), thermal effects are less prominent, whereas trapping effects are more responsive when emission/capture time constants are smaller than the pulse duration. The pulse width is 200 ns (system limitation) and the pulse separation is 1 ms (duty cycle ~0.0002 %) is shown in Figure 2.24. The purpose of selecting minimum pulse width is to avoid self-heating as well as is to get a response from maximum traps in the GaN HEMTs structure having fast (~ < 10 µs) and slow (~> 1 ms) response. Fig. shows the pulse pattern of a pulsed $I_D - V_D$ measurement under the gate- lag and the drain-lag condition.

- (V_{GS0}, V_{DS0}) = (0 V,0 V): this bias condition corresponds to negligible electron trapping and can be used as reference for estimation of current collapse in the device.
- (V_{GS0}, V_{DS0}) = (-5 V,0 V): This condition is called gate-lag stress condition ($V_{GS0} < V_{th}$). This condition generally provides characteristics of trapping of electrons under the gate region.
- (V_{GS0}, V_{DS0}) = (-5 V,10 V): This condition exposes the trapping of electrons under the gate-drain region and the current collapse obtained in such bias stress condition is also called gate-lag and

drain-lag in the device. You may provide our old papers published using these stress conditions.

Moreover, with increasing the V_{DS0} keeping the V_{GS0} same, increased trapping behaviour of electron can be observed due to activation of deeper traps in the bandgap. As V_{DS0} stress increases, the GaN conduction band bends downwards activating different trap energy levels (see fig.2.25) [78].

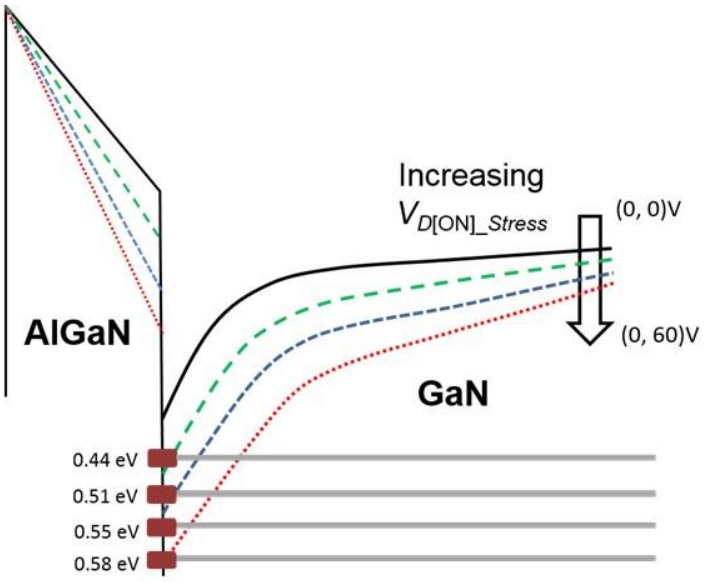


Figure 2.25 Schematic representation of AlGaN/GaN heterojunction energy band bending with different V_{DS0} stress conditions and the distribution of traps in the GaN energy band-gap [77].

- *Gate-Lag Condition* (V_{GS0} = <V_{th}, V_{DS0} = 0): In this case of quiescent bias point, both the gate pulse is in the sub-threshold regime and the drain pulses is usually 0 V. The negative voltage applied to the gate terminal will cause tunneling of gate

electrons into the AlGaN barrier and AlGaN/GaN hetero-interface. At the moderate quiescent bias condition, V_{GS0} = ~ V_{th}, V_{DS0} = 0 V, we can investigate AlGaN/GaN hetero-interface trap behaviour. This condition was used to investigate the AlGaN/GaN hetero-interface trap behaviour in GaN HEMTs-on-CVD diamond and presented in chapter 4.

- *Drain-Lag Condition* (V_{GS0} <V_{th}, V_{DS0} = V_{DD}): In this case of quiescent bias, gate pulses are in the deep sub-threshold regime, while a drain pulses equivalent to the value of V_{DD} is applied. In this case, due to the high voltage bias applied to the drain terminal, a large intensity of the electric field is created in the drain side edge of the gate leading to trapping of the tunneled gate electrons in the access regions and surface of the AlGaN/GaN barrier. The 2DEG electrons are also trapped in the GaN buffer and transition layer and the trapping behaviour depends on the electric field intensity in the hetero-structure. With the increase of V_{DS0} the increase of the dynamic $R_{DS[ON]}$ occurs in the device. This technique is used in this work for investigating trap behaviour and dynamic on resistance in GaN transition free AlGaN/GaN HEMTs-on-CVD diamond. The detailed results and analysis are described in chapter 5.

There is a reference quiescent bias condition, cold conditions [(V_{GS0}, V_{DS0}) = (0, 0) V], in which almost no trapping occurs, and device exhibits maximum current without dispersion. Hence, by comparing the pulsed I_D –V_D characteristics result in the gate-lag quiescent bias conditions and the drain-lag quiescent bias conditions with that of cold quiescent bias conditions, it can be quantified the effects of trapping in the corresponding regions of prominence. Since a very short pulse width is applied, the pulsed I_D –V_D characteristics can be treated as quasi-static based measurements.

In this thesis, the pulsed I_D−V_D measurements were carried out using Accent DIVA 265 dynamic I_D –V_D analyzers with a pulse width of 200 ns and a pulse separation of 1 ms. This pulse condition ensures that the emission/capture processes of electrons by trap centres are not affected by each measurement point, but by the applied quiescent bias condition. We have limited to these minimum pulse width (200 ns) condition due to equipment limitations.

2.6.2 Conductance frequency technique

The frequency-dependent conductance (*G-f*) analysis near the gate depletion bias is generally employed to estimate the trap densities at AlGaN/GaN channel interface. The conductance method is one of the most sensitive methods to estimate the interface trap density and trap state time constant. This method was first proposed by Nicollian and

Goetzberger in 1967 [79] In the conductance technique, the interface trap density can be obtained. The AC conductance method provides the loss which is caused by the change in the trap charge state [66]. This method is used to investigate the interface trap density in the depletion and weak inversion layer, the capture cross-section, and surface potential fluctuations [80].

Fig.2.26 shows the schematic and the equivalent circuit of a MIS-Diode with typical AlGaN/GaN heterostructure. Fig.2.26 shows (a) the top view of the layout for a typical circular MIS diode, (b) it's cross-section and equivalent circuit element distribution, and (c) its simplified equivalent circuit topology. There are two types of interface traps located in AlGaN/GaN HEMTs. One at the surface interface between gate insulator and III-nitride semiconductor and other is the heterostructure interface between AlGaN barrier and GaN buffer.

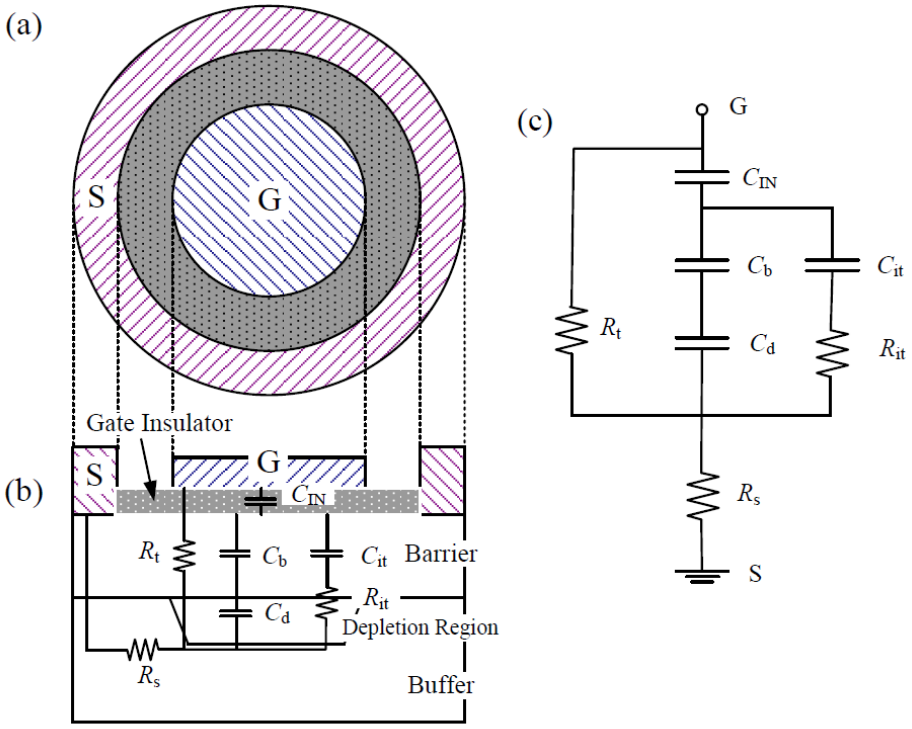


Figure 2.26 The typical schematic and equivalent circuit of a Metal-insulator-Semiconductor (MIS) diode: (a) the top view of the layout for a typical circular MIS diode; (b) the cross-section and equivalent circuit element distribution; (c) the equivalent circuit topology [65].

The hetero-interface trap behavior will be studied in this chapter. The resistance R_S is the series resistance from the ohmic contact to the device channel through the access region between the source and gate electrodes. The resistance R_t is the gate leakage current through the gate to the channel. C_{IN} represents the capacitance of the gate insulator. In the conventional diode, there is no gate insulator between the gate metal and GaN cap layer. C_b accounts for the capacitance of the AlGaN barrier layer

(GaN cap layer also included in C_b). C_d represents the capacitance of the GaN channel depletion region. The C_{it} and R_{it} in series describe the capacitance effect of the traps located at the interface between the gate insulator and III-nitride semiconductor materials. The time constant of these interface traps is given by $\tau_{it} = R_{it}.C_{it}$. With the change of gate bias (V_g), the number of trapped electrons at the interface states varies, thus an effective capacitor C_{it} is formed. The R_{it} together with C_{it} can describe the time delay (τ_{it}) required for the electrons trapped at the interface to reach equilibrium with those in the channel and C_{it} which is related to the trap density (D_{it}). Fig. 2.27 shows the simplified equivalent circuit of a diode for interface trap density calculation.

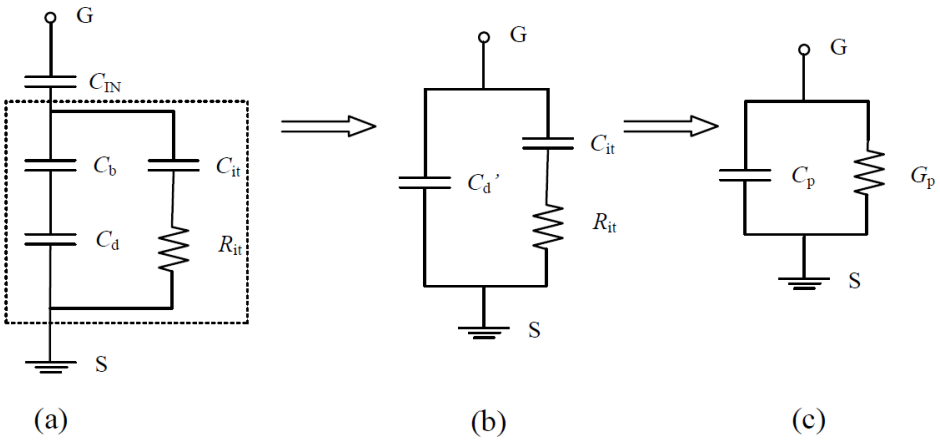


Figure 2.27 Simplified equivalent circuit of a diode for interface trap density calculation by AC conductance method, where G_p is parallel conductance which is measured at a wide range of frequencies by conductance frequency technique.

A typical G_p/ω versus radial frequency is shown in fig. 2.28 [65].

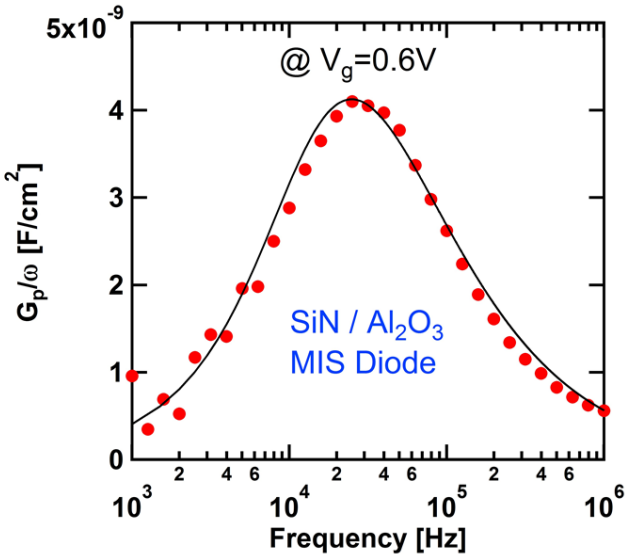


Figure 2.28 Frequency-dependent conductance as a function of radial frequency [77].

Trap density calculation:

The trap density (D_T), assuming a continuum of trap levels, can be estimated by fitting the experimental G_p/ω data using equation [61, 66],

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln[1+(\omega\tau_T)^2]$$

where ω is the radial frequency, D_T is the trap density, and τ_T is the trap time constant. Generally, G_p/ω has a maximum value at $\omega \cong 2/\tau_T$. Hence, D_T can also be estimated as $D_T \approx (2.5/q)\ (G_p/\omega)_{max}$ [65]. After the estimation of trap density and trap time constant, the trap state energy can be estimated using the expression [81],

$$E_T = -kT\ \ln(\tau_T\sigma_T v_t N_C)$$

Where σ_T is the capture cross-section (3.4×10^{-15} cm^{-2}), v_t is the thermal velocity of electrons (2.6×10^7 cm/s), T is the temperature, and N_C is the effective density of states ($4.3 \times 10^{14} \times T^{3/2}$ cm^{-3}) at the conduction band in GaN and k is the Boltzman constant.

So far, researchers have reported the AlGaN/GaN interface trap characteristics using *G-f* method in the GaN HEMTs on Si, Sapphire, and SiC substrates [74, 80, 83-88] (See Fig. 2.29). Most of the reported D_{Tmin} values are in the range of 10^{10} - 10^{13} cm^{-2} eV^{-1}, measured at room temperature. No reports are available on the hetero-interface trapping behaviour in the GaN HEMTs on CVD diamond.

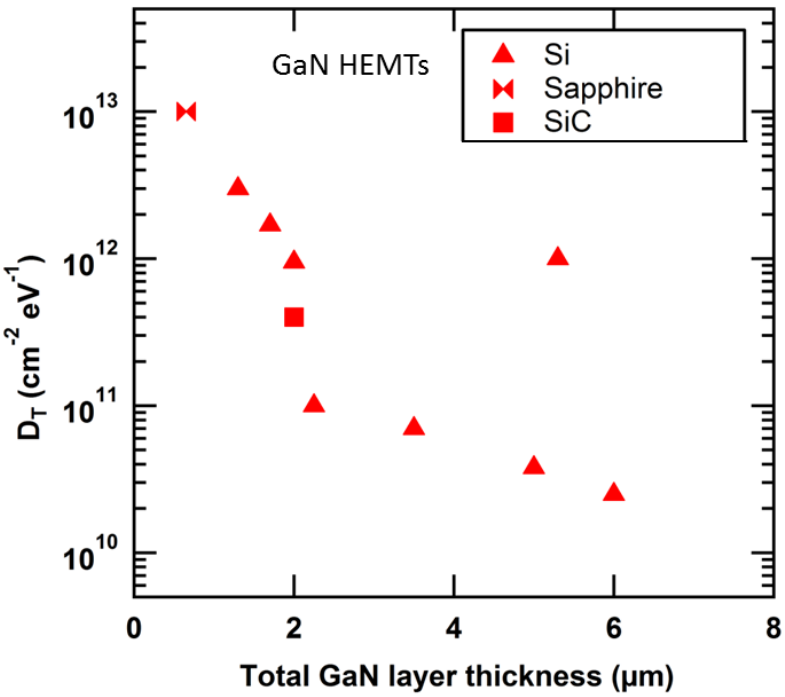


Figure 2.29 A comparative chart of interface trap density (D_{it}), estimated using the conductance method, in GaN HEMTs on Si [74, 80, 83-87], GaN

HEMTs on Sapphire, and GaN HEMTs-on-SiC substrates [88].

In this thesis, we will present the systematic investigation of hetero-interface traps in GaN HEMTs-on-CVD-Diamond substrate using *G-f* method. The detailed results and analysis are described in chapter 4.

3 Self-heating in GaN HEMTs on Si and CVD diamond

In the previous chapter, the effect of self-heating in AlGaN/GaN HEMTs is briefly discussed. This chapter elaborates further on the investigations of self-heating effect on the DC and RF performances of fabricated AlGaN/GaN HEMTs on CVD-Diamond (GaN/Dia) and compares the results with those of AlGaN/GaN HEMTs-on-Si (GaN/Si) substrates. Device performances such as I_D, I_G, g_m, f_T, and f_{max} were analyzed to measure the influence of large longitudinal electric fields by applying a wide range of bias voltage. 2-D TCAD numerical simulations were performed to analyze the junction temperature (T_j) of the device. Further investigation of the root cause of device performance degradation was completed by extracting the small-signal equivalent circuit parameters at various bias conditions.

3.1 Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising candidates for high power continuous wave (CW) operations in compact solid-state power amplifier (SSPA) modules which are ideal for civil avionics, communications, industrial, scientific, and medical applications. However, thermal management, size reduction, and long-term reliable operation for GaN-based devices are some of the major challenges,

especially when the device is operating at high drain bias voltage (e.g., V_D 28-48 V). The poor heat emission from conventional substrates (e.g. Si, Sapphire) accelerates self-heating, which causes additional phonon scattering in the channel and degrades the 2DEG effective carrier mobility (μ_{eff}). This eventually may lead to degradation in DC and RF performance which accelerates further with increasing drain voltage (V_D). To avoid self-heating effect, a superior thermal conductive material such as Diamond (1000-2000 W/m-K), has been employed as a substrate to dissipate the generated heat from the active region of the device. Researchers have also reported AlGaN/GaN HEMTs on Diamond with dissipated DC power density ($P_D = V_D \times I_D$) of 22 W/mm (CW), and 24 W/mm in pulse condition as well as 3.6-times higher RF power capability over GaN/SiC HEMTs. These results show the strong manifestation of extracting improved transport properties of GaN HEMT by using Diamond as a substrate. However, the bias conditions effect on self-heating and transport properties in AlGaN/GaN HEMTs-on-Diamond have not been reported so far. Such work is needed for developing the electrical and thermal model of device as well as understanding the operating limit of GaN HEMTs for next-generation high power density DC and RF application.

3.2 AlGaN/GaN HEMT structure and device fabrication

AlGaN/GaN HEMT-on-CVD diamond was developed using Metal-Organic Chemical vapor deposition (MOCVD) grown AlGaN/GaN HEMT-on-Si (Standard Wafer) by a proprietary process from the commercial company Element Six. The substrate transfer process was mainly done by the removal of Si substrate as well as GaN transition layer followed by an interface layer (adhesion layer) deposition bonding of CVD diamond. The AlGaN/GaN heterostructure is shown in Fig. 3.1. The GaN cap layer, AlGaN barrier, the i-GaN channel, and the buffer layer are unintentionally doped.

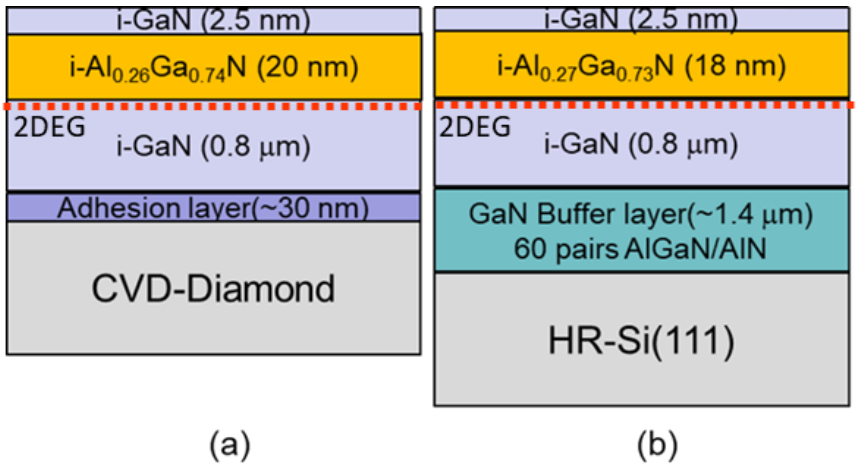


Figure 3.1 Cross-sectional schematic diagram of AlGaN/GaN HEMT on (a) CVD-Diamond substrate (b) Si (111) substrate.

Before the device fabrication, the 2DEG properties (2DEG carrier mobility and sheet resistance) were measured for both the HEMT

structures at room temperature. GaN/Dia (GaN/Si) HEMT exhibited an average room temperature 2DEG mobility of 1502 (1450) $cm^2V^{-1}s^{-1}$, sheet carrier density of 0.97×10^{13} (1.0×10^{13}) cm^{-2} and average sheet resistance of 425 (430) ohm/sq. with a variation of ±3% over the full 4-inch wafer. In this case, the 2DEG property of the GaN/Dia HEMT structure remains almost the same as GaN/Si HEMT. For this study, the 4” diameter AlGaN/GaN HEMT on CVD-diamond wafer was diced into 1” x 1” for the device fabrication. The AlGaN/GaN HEMTs devices were fabricated using standard GaN HEMTs processing techniques, as shown in Fig. 3.2. The fabrication processes consist of the following steps;

For this study, the 4” diameter AlGaN/GaN HEMT on CVD-diamond wafer was diced into 1” x 1” for the device fabrication. The AlGaN/GaN HEMTs devices were fabricated using standard GaN HEMT processing techniques, as shown in Fig. 3.2. The fabrication processes consist of the following steps;

I. Mesa Isolation

II. Ohmic contact formation (Source and Drain contact)

III. Schottky Gate contact formation

IV. Metal pad Interconnection

V. Surface passivation

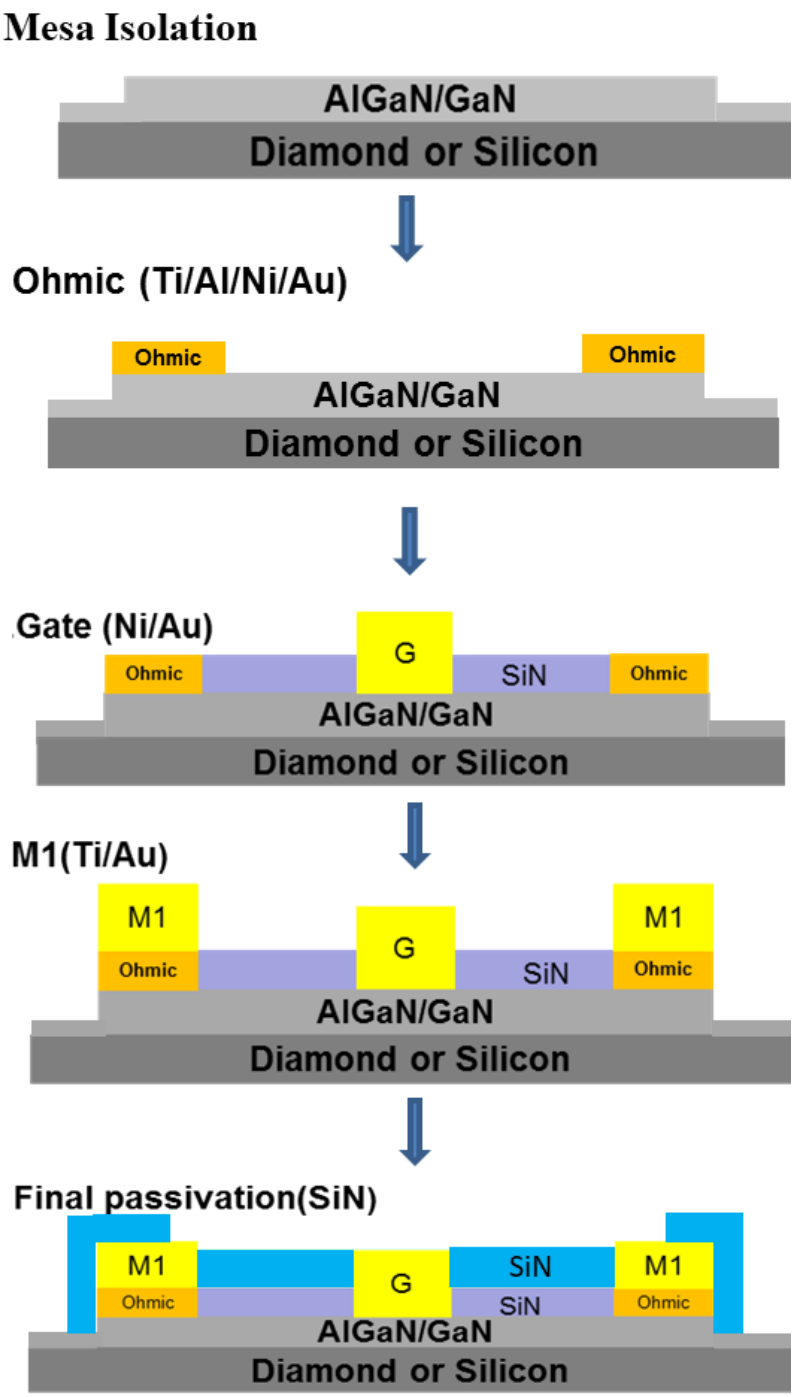


Figure 3.2 Process flow used in the device fabrication of 2-µm gate AlGaN/GaN HEMTs-on-Si and CVD substrate.

Mesa Isolation

It is necessary to electrically isolate two adjacent active devices to prevent leakage current between them. The device fabrication was started with the mesa isolation process. The etching of GaN/AlGaN/GaN layer (~150 nm) was done by dry etching process using Inductive coupled plasma (ICP) system. The GaN layer etching depth was much deeper than that of the 2DEG depth (~25 nm). The isolation current between the mesa region was obtained around 10^{-6} A/mm at 20 V which was measured after the ohmic contact formation.

Ohmic Contact

Low ohmic contact for Source and drain contact resistance is very important to achieve high drain current as well as low on-resistance in the device. After optical lithography, samples were treated in HCl:H_2O to remove the native oxide from the ohmic metal region. The ohmic contact was formed by depositing conventional Ti/Al/Ni/Au metal stacks followed by rapid thermal annealing at 825 °C for 30s in a N_2 atmosphere.

Gate Contact

Gate contact is the Schottky contact with the top GaN layer in GaN HEMTs. This is achieved by using metals with high work function. Thus, in order to achieve low gate leakage currents and high breakdown voltages, gate contact with high Schottky barrier height is required.

Furthermore, since the GaN HEMTs exhibit high channel currents resulting in high channel temperatures which is mainly at the gate edge of the gate-drain region, the gate metal should have high thermal stability. Also, the gate metal should have good adhesion with the GaN surface. The gate metal contact is formed by E-beam evaporation. In this case, the Ni/Au (150/300 nm) gate metalization was formed using conventional lithography and e-beam evaporation followed by a lift-off process.

Interconnect Metallization

Finally, thick Ti/Au (50/1000 nm) was formed in order to withstand high current density that flows through the source and drain electrode[38]. This Ti/Au (50/1000 nm) metalization helps to protect the device from metal punch through during high voltage DC measurements.

Surface Passivation

In GaN HEMTs, surface passivation is very vital to minimize DC and RF dispersion by reducing current collapse during device operation. Generally, a large amount of surface states presents at the surface of the III-Nitride semiconductor. These surface states are due to the dangling bonds/dislocations/defects at the surface originated during the growth or fabrication process thus act as a source of electron traps. The electrons are trapped at these surface states and create charge imbalance which deplete the 2DEG channel electrons by forming a virtual gate. Thus, it is important to mitigate the surface states through an appropriate material

passivation process. In this work, the devices were passivated with 120-nm-thick SiN_x (SiN is used in this thesis to represent SiN_x) using plasma-enhanced chemical vapor deposition (PECVD) at 300 °C.

AlGaN/GaN-on-Diamond HEMTs (GaN/Dia), AlGaN/GaN-on-Si HEMTs (GaN/Si) were fabricated with the same device structure ($L_{SG}/W_G/L_G/L_{GD}$ =2/(2×100)/2/3 μm) and same processing steps where L_{SG} is the gate-source spacing, W_G is the gate width, L_G is the gate length, and L_{GD} is the gate-drain spacing. Figure 3.3 shows the cross-sectional schematic diagram of AlGaN/GaN HEMTs device.

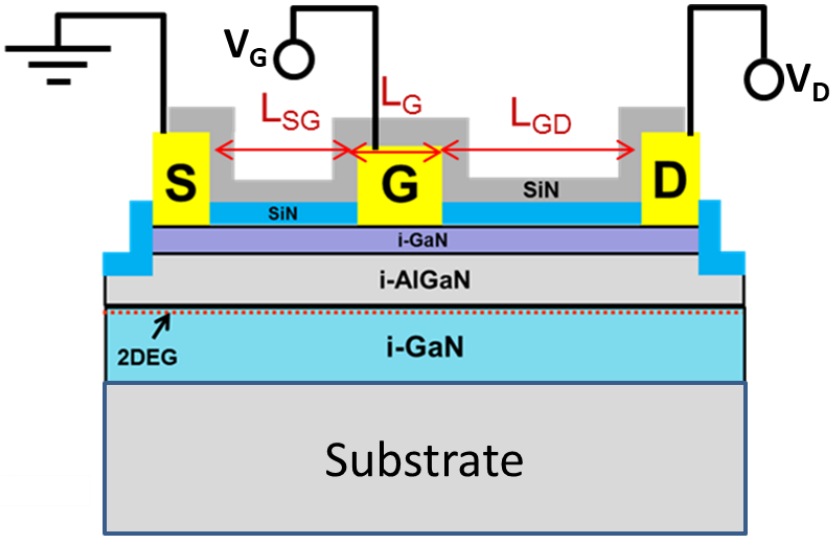


Figure 3.3 Cross-sectional schematic diagram of AlGaN/GaN HEMTs device

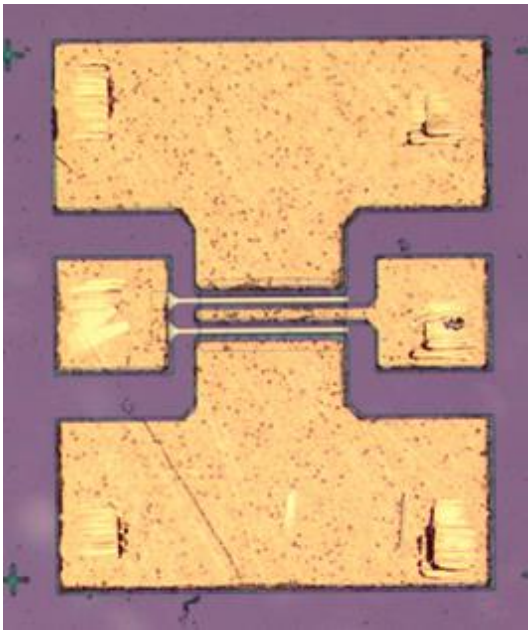


Figure 3.4 Optical microscope image of fabricated AlGaN/GaN HEMTs-on-CVD diamond

3.3 DC characterization and self-heating analysis

The DC characterization was performed at room temperature on both types of HEMTs using the measurement setup mentioned in chapter 2. Figure 3.5 shows the combined plot of DC I_D-V_D of GaN/Dia and GaN/Si HEMTs. GaN/Dia HEMTs were measured first up to V_D=20 V and later increased up to V_D=60 V (system limit) whereas GaN/Si HEMTs were measured up to V_D=20 V at V_G=+1 V to avoid on-state device breakdown. Catastrophic burnt out of GaN/Si HEMTs device during CW high voltage measurements was observed which could be due to larger heat retention

in the channel. The GaN/Si and GaN/Dia HEMTs exhibited maximum drain current density (I_{Dmax}) of 652 and 662 mA/mm respectively. As shown in figure 3.5, GaN/Si suffered a significant reduction of I_D beyond the maximum current density (I_{Dmax}) as compared to GaN/Dia. The I_D reduction rate at V_g = +1V was obtained as 15 mA/mm.V and 3.3 mA/mm.V for GaN/Si and GaN/Dia, respectively. The large current droop in GaN/Si is due to excessive self-heating in the GaN/Si HEMTs. The GaN/Dia exhibited a much smaller percentage of drain current reduction which is 10 % compared to the 33 % in GaN/Si HEMTs (See Fig. 3.5).

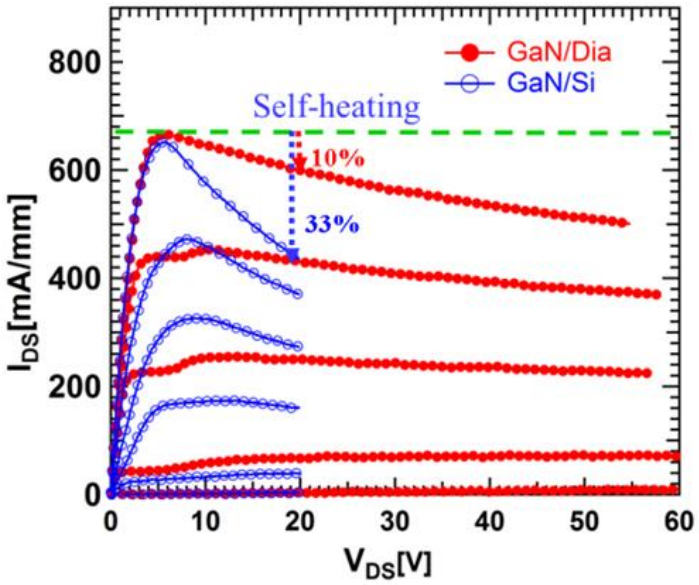


Figure 3.5. I_{DS}-V_{DS} of GaN/Dia and GaN/Si HEMTs. Device dimensions: $L_{sg}/W_g/L_g/L_{gd}$ =2/(2×100)/2/3 with gate to gate pitch (L_{gg}) =23 um

The maximum dissipated DC power density ($P_D = V_D \times I_D$) in GaN/Dia was calculated to be 27.56 W/mm as compared to the 8.7 W/mm in

GaN/Si. The I_D reduction ($I_{Dreduc.}$) versus P_D was shown in fig. 1.6. The $I_{Dreduc.}$ rate in GaN/Dia is ~ 1 %.mm /W as compared to 5.89 %.mm /W in GaN/Si HEMTs, which is ~5.7-times lower rate of I_{Dreduc} in GaN/Dia as compared to GaN/Si .

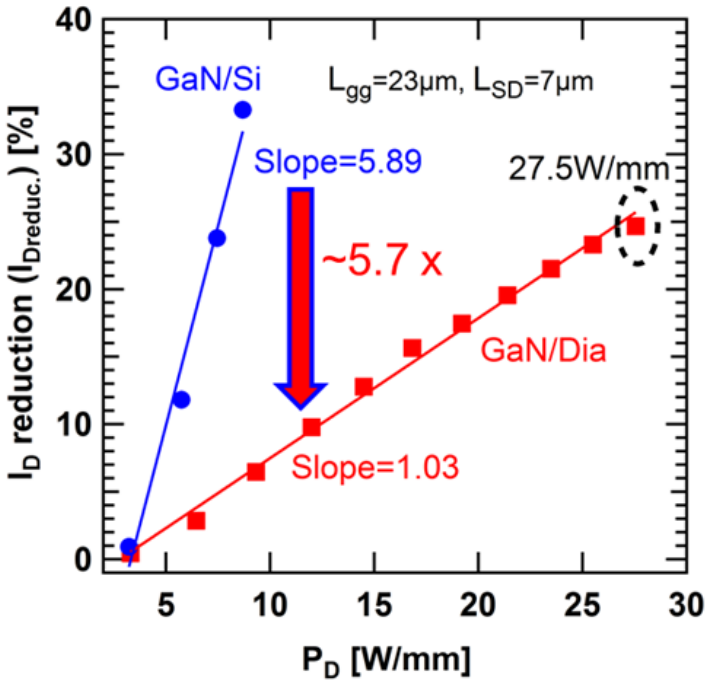


Figure 3.6 I_D reduction ($I_{Dreduc.}$) versus DC P_D of GaN/Dia and GaN/Si HEMTs. Device dimensions: $L_{sg}/W_g/L_g/L_{gd}$ =2/(2×100)/2/3 with L_{gg}=23 µm

It is worth to mention that GaN/Dia sustained a higher P_D of 27.56 W/mm even without on-state breakdown. In contrast, GaN/Si was burnt around ~9 W/mm of DC P_D, which could be due to intense self-heating and increased channel temperature in GaN/Si. Such inherent characteristics make GaN/Dia transistor very suitable for high power CW operation. The

degradation of maximum transconductance (g_{mmax}) and maximum drain current density (at V_G = 0 V) were analyzed from the measured transfer characteristics. By limiting the V_G up to 0 V, we increased the CW V_D up to 40 V for GaN/Si and the device was measured without observing catastrophic failure. The HEMTs exhibited peak extrinsic transconductance (g_{mmax}) of 162 and 199 mS/mm for GaN/Si and GaN/Dia respectively at V_D = 10 V(See Fig. 3.7).

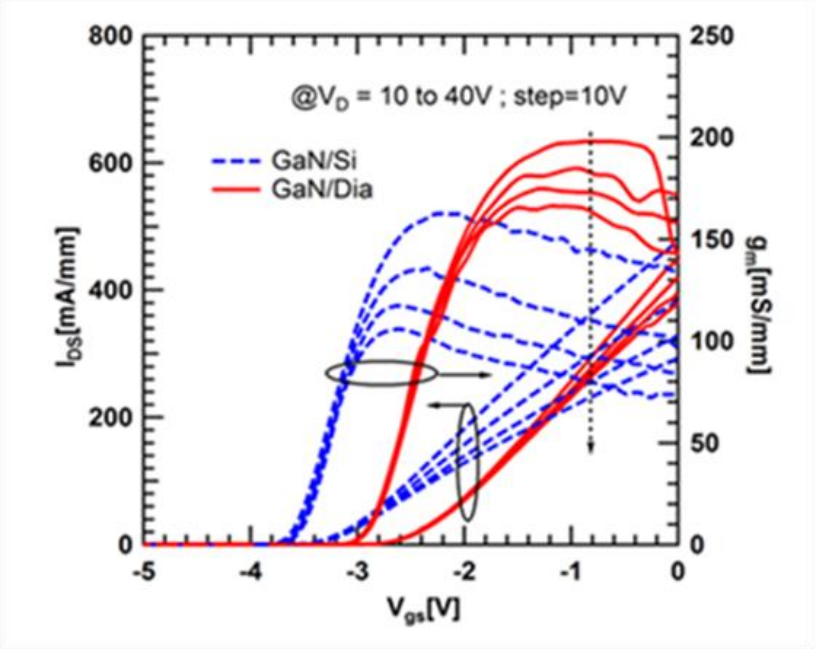


Figure 3.7. Transfer characteristics of GaN/Dia and GaN/Si HEMTs at different V_D

It is clearly observed that as V_D increases, the g_{mmax} decreases. The reduction of g_{mmax} could be due to the reduction of effective mobility of 2DEG carrier at higher V_D. Further analysis was done for the drain bias

dependent I_{Dmax} (at V_g = 0 V, V_D= 10 - 40 V) and g_{mmax} reduction. The percentage of I_D reduction ($I_{Dreduc.}$) was calculated based on the formula:

$$I_{Dreduc.} = ((I_{Dmax} - I_{D\text{-}Vd}) / I_{Dmax}) \times 100$$

The I_{Dmax} is the maximum I_D value from transfer characteristics at V_D=10 V and $I_{D\text{-}vd}$ is taken as maximum I_D at a particular V_D for the calculation of $I_{Dreduc.}$.

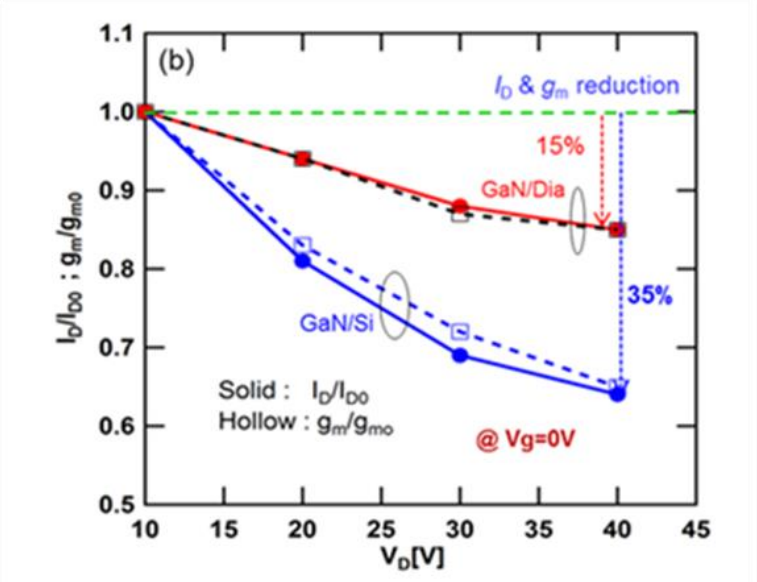


Figure 3.8 Normalized I_{dmax} and g_{mmax} reduction at different V_D.of GaN/Dia and GaN/Si HEMTs at different V_D.

Similarly, the g_{mmax} reduction [$g_{mreduc.}$ = (g_{mmax} - $g_{m\text{-}vd}$)×100/g_{mmax}] (g_{mmax} is the maximum g_m value extracted from the transfer characteristics at V_D=10 V and $g_{m\text{-}vd}$ is taken as maximum g_m at a particular V_D for the calculation of $g_{mreduc.}$) was also calculated. The $g_{mreduc.}$ was found to be 15

% and 35 % at V_D=40 V with a rate of 1.0 mS/mm.V^{-1} and 1.9 mS/mm.$V^{-1,}$ respectively for GaN/Dia and GaN/Si HEMTs (See Fig. 3.8). Lower g_{mmax} reduction of GaN/Dia also indicates a lower reduction of effective mobility (μ_{eff}) which was extracted further in this work. Lower $I_{Dreduc.}$ and $g_{mreduc.}$ in GaN/Dia HEMTs confirms the low self-heating effect in the device which is due to the efficient heat dissipation through the Diamond substrate. Therefore, GaN/Dia enables the device to operate at higher V_D without much compromise of current density and transconductance, which are key requirements for devices operating at higher CW power.

In addition to the I_D and g_m, gate current was also measured on the same device with increasing V_D at V_G =0 V. Fig. 3.9 shows the I_G versus V_D for both GaN/Si and GaN/Dia HEMTs. From fig. 1.9, it is clear that I_G is increasing at a higher rate in GaN/Si than GaN/Dia under similar longitudinal electric field conditions. However, I_g increase is more prominent at V_D > ~15 V. This increase of I_G could be due to the increased channel temperature at higher drain bias voltage. Increased gate current with temperature which is due to temperature assisted tunneling [90, 91].

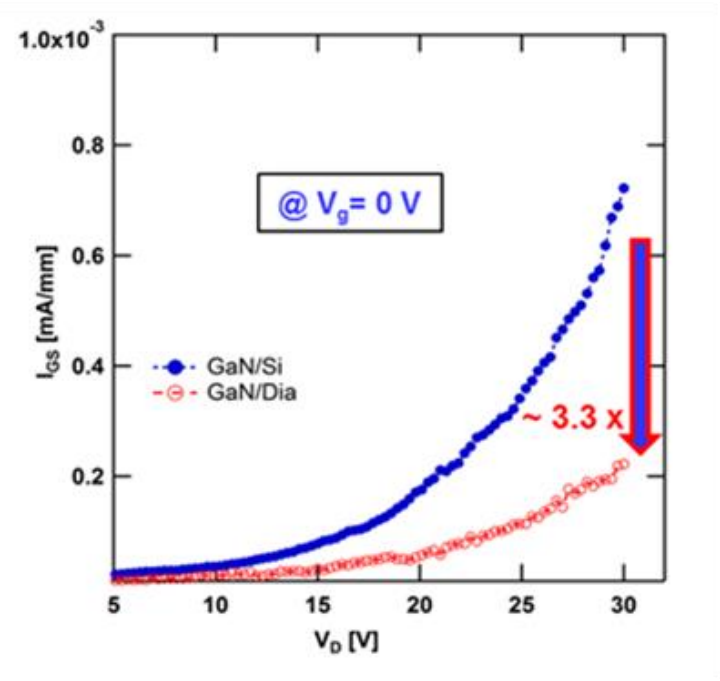


Figure 3.9 Gate current characteristics of GaN/Dia and GaN/Si HEMTs with V_D at V_G = 0 V.

The rate of I_G increase in GaN/Dia is ~3-times lower than GaN/Si. Lower rise of I_G with V_D implies higher gate stability and reliable device performance at high voltage operation of GaN/Dia. The high gate-leakage currents limit the positive gate voltage swing and thus the maximum output power as well the microwave performance [92,93].

3.4 TCAD simulation and Junction temperature estimation

To evaluate the effect of Diamond substrate on the channel temperature distribution in AlGaN/GaN HEMTs, 2D TCAD simulation (SILVACO) was also performed [94]. The Atlas^{TM} program was used to model the above mentioned AlGaN/GaN HEMT device structure. In order to investigate the bias dependent temperature distribution in these devices, 2D TCAD simulation (SILVACO) was also performed using the GIGA module consistently with BLAZE.

There are several boundary conditions provided by AtlasTM such as: Insulated, Schottky, Ohmic contacts, and Neumann boundaries. The boundary conditions of voltage and current at these contacts are provided in the simulation. Ohmic and Schottky contacts are implemented as Dirichlet boundary conditions. The boundary condition at the bottom of the substrate is defined as thermo-contact 300 K. For implementing the thermal boundary resistance (TBR) of SiN (~30nm) -Diamond interface, effective thermal conductivity of 0.01 W/cm.K was included in the model parameters which is taken from the reported literature [95].

The temperature-dependent model of thermal conductivity was implemented and is listed in the following table.

Table: 3.1 The temperature-dependent model of thermal conductivity used in simulation

Material	Thermal Conductivity (W/cm.K)
GaN	$K(T) = 1.3\left(\frac{T}{300}\right)^{-0.28}$
Si3N4	0.3
AlN	$K(T) = 2.85\left(\frac{T}{300}\right)^{-1.64}$
Si	$K(T) = 1.48\left(\frac{T}{300}\right)^{-1.65}$
Diamond	15

The thermal boundary conditions can be expressed as;

$$(J_{tot}.s) = \frac{1}{R_{th}}\left(T - T_{ref}\right)$$

where J_{tot} is the total energy flux, s is the unit external normal of the boundary, T_{ref} is the reference boundary condition of the thermo-contact in the simulation environment, and R_{th} is the material-dependent thermal resistance. In our simulation, the bottom of the devices is used as the reference thermo-contact at 300 K. TCAD simulation accounted GIGA module consistently with BLAZE in order to find out the lattice temperature at elevated V_D using Lattice flow equation by defining the parameter LAT.TEMP in the MODEL command of Atlas.

$$C\frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + \mathrm{H}$$

$$C = \rho C_p$$

where *C* is the heat capacitance / unit.volume, *κ* denotes the temperature-dependent material thermal conductivity, *H* denotes the heat generation and T_L denotes the lattice temperature at the specific location. *Cp* is the specific heat, *ρ* is the material density. Fig. 3.11 shows the cross-sectional thermal profile by 2D simulation for (a) GaN/Si, and (b) GaN/Dia HEMTs.

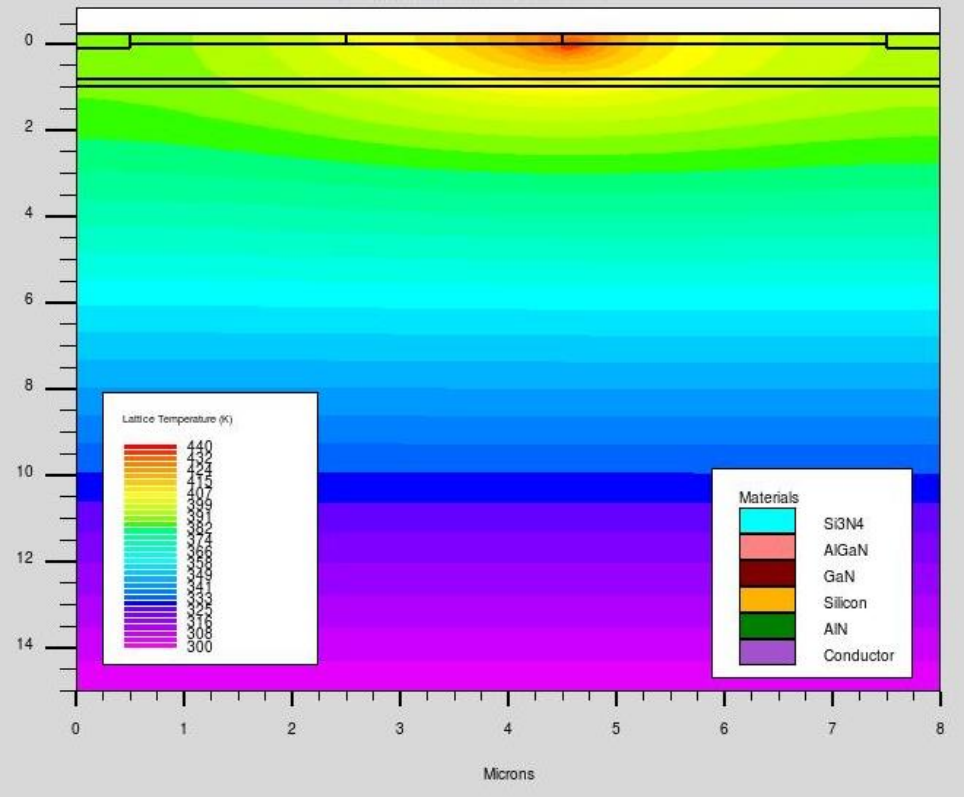


Figure 3.10. Cross-sectional thermal profile by 2D simulation for GaN/Si HEMTs

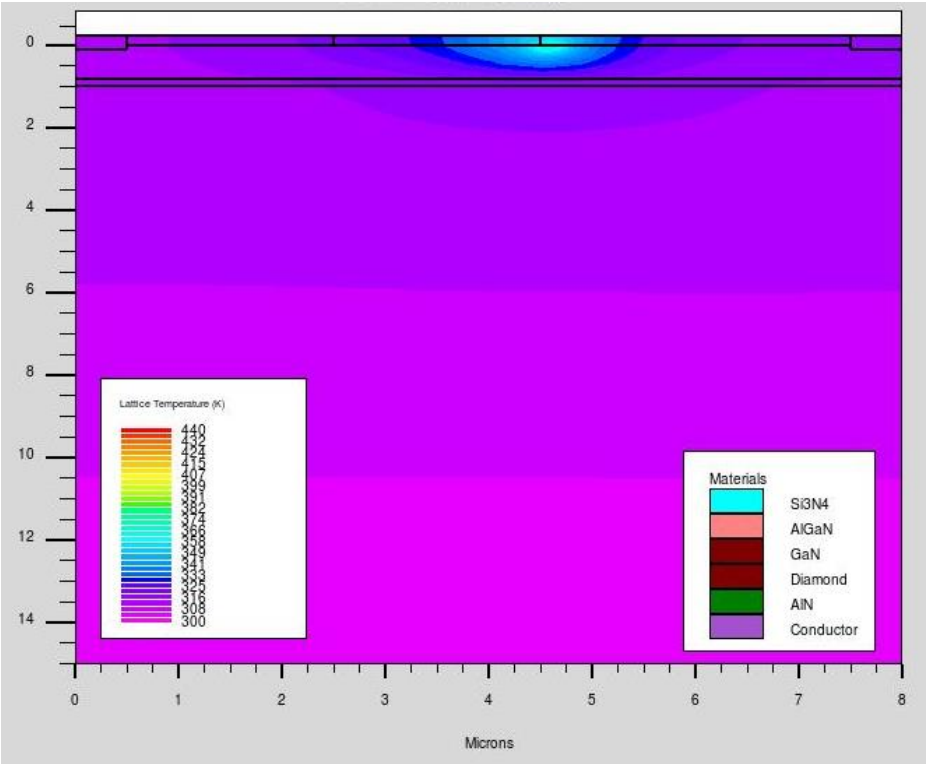


Figure 3.11. Cross-sectional thermal profile by 2D simulation for GaN/Dia HEMTs

Fig. 3.11 shows the cross-sectional simulated 2D thermal profile of GaN/Dia HEMTs. From the figures 3.10 and 3.11, it is clear that GaN/Dia has a much lower temperature as compared to GaN/Si HEMTs. The simulated thermal profile indicates that the maximum temperature region is near the gate edge of gate-drain region. Fig. 3.12 (a), and (b) shows the thermal profile, focusing on the high-temperature region of the GaN/Dia and GaN/Si HEMTs respectively. The highest temperature in the channel (hot spot) is referred here as junction temperature (T_j).

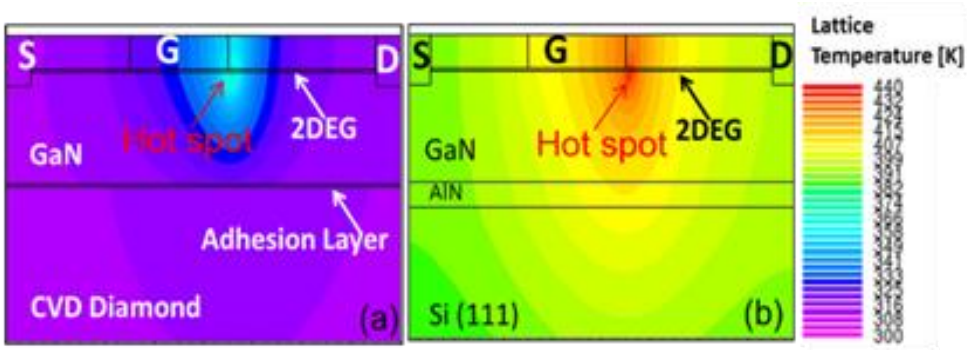


Figure 3.12 TCAD Simulated cross-sectional thermal profile for (a) GaN/Dia, (b) GaN/Si at V_D =20V, V_G = +1 V.

The obtained temperature profile across the device channel from source to drain clearly indicates that the GaN/Si HEMTs have T_j of 440 K, whereas it is 370 K in the GaN/Dia HEMTs for the same drain and gate bias condition.

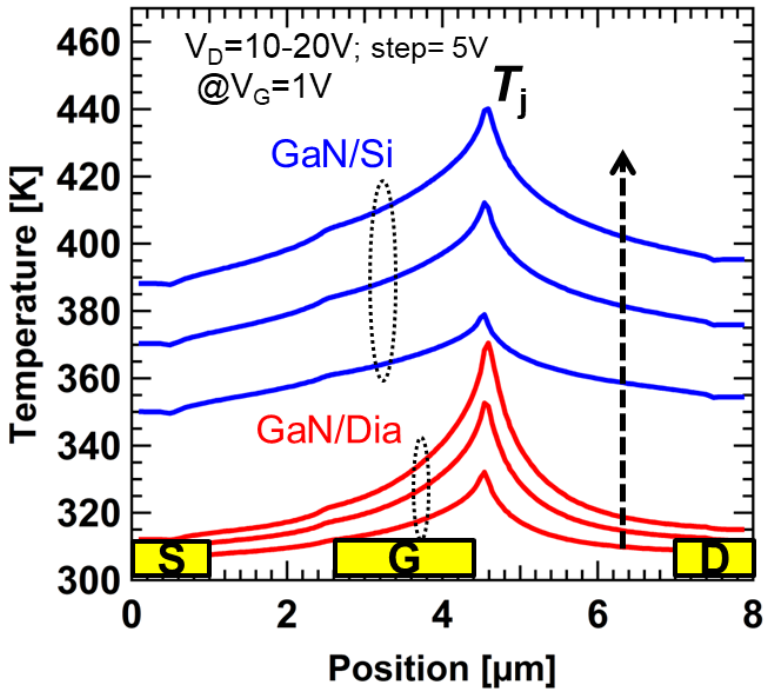


Figure 3.13 TCAD Simulated device temperature profile across the source-drain region for different V_D=10, 15, and 20 V (d) ΔT_j versus P_D of GaN/Dia and GaN/Si HEMTs.

Fig. 3.14 shows TCAD simulated junction temperature rise (ΔT_j) of the device with DC dissipated power density. From the figure, it is clear that the junction temperature rises more rapidly in GaN/Si HEMT (140 K) than GaN/Dia HEMT (36 K) at P_D (7 W/mm). A similar trend of temperature rise (ΔT_j) in GaN/Dia HEMTs was also observed by Pomeroy et al. [96]. Thermal resistance (R_{th}) values were calculated from the slope of the rise of junction temperature versus P_D for both GaN/Dia (6.7 K.mm/W) and GaN/Si (26.2 K.mm/W) HEMTs (See Fig. 3.14).

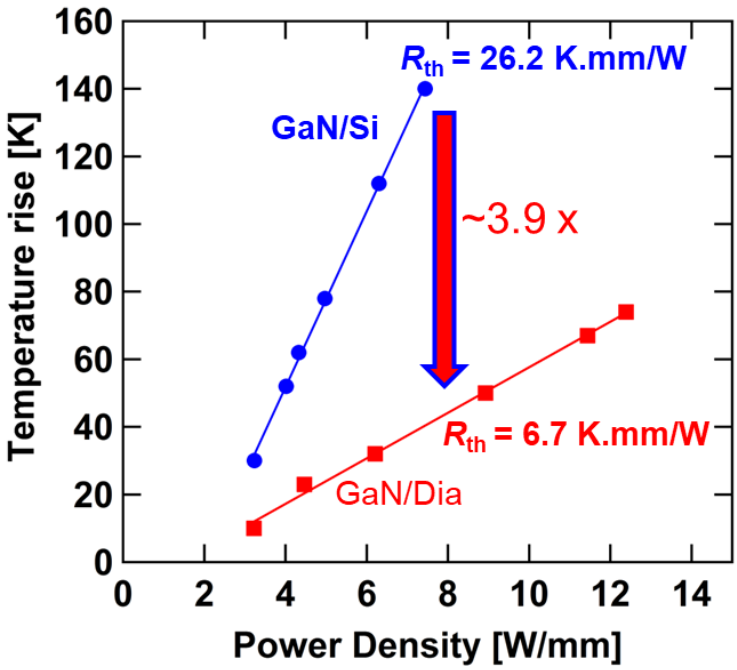


Figure 3.14. TCAD Simulated ΔT_j versus P_D of GaN/Dia and GaN/Si HEMTs.

The extracted values of R_{th} closely matched the reported values (~6.5 K.mm/W) for GaN/Dia HEMTs [16], and (24.6 K.mm/W) for GaN/Si HEMTs [97]. The GaN/Dia shows ~3.9-times lower R_{th} value than GaN/Si HEMTs. This is in good agreement with the reported results by Pomeroy et al. [98]. The R_{th} of GaN/Dia can further be minimized by optimizing the interface layer between GaN and CVD-Diamond [99].

3.5 RF characteristics and Self-heating analysis

S-parameter measurements were carried out on GaN/Dia and GaN/Si HEMTs at V_d=10 V and V_g was selected to get I_d of ~200 mA/mm where both the devices exhibited their maximum transconductance (g_m). The values of the short-circuit current gain (H_{21}) and the unilateral power gain (G_u) was calculated from measured S-parameters. Figure 3.15 shows the microwave small-signal gain characteristics of GaN/Dia and GaN/Si HEMTs. At V_D=10V, the GaN/Dia and GaN/Si HEMTs exhibited a unity current gain cutoff frequency (f_T) of 10.2 GHz and 7.0 GHz and a maximum oscillation frequency (f_{max}) of 31.4 GHz and 18.2 GHz, respectively.

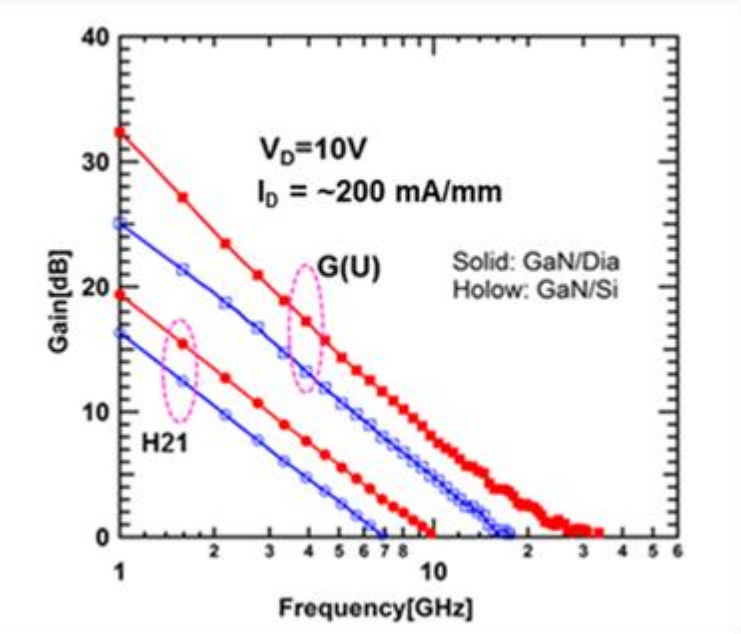


Figure 3.15 Small-signal microwave characteristics of GaN/Dia and GaN/Si HEMTs of a 2-μm gate device.

S-parameters measurements were further performed on both the HEMTs from V_D=10 - 40 V at almost constant current density. The forward current gain (H_{21}) was deduced from measured S-parameters at different V_D. At 2 GHz, about 1.0 dB reduction of H_{21} was observed in GaN/Dia HEMT when compared to 7 dB reduction in GaN/Si HEMTs from V_D=10 - 40 V (See Fig. 3.16).

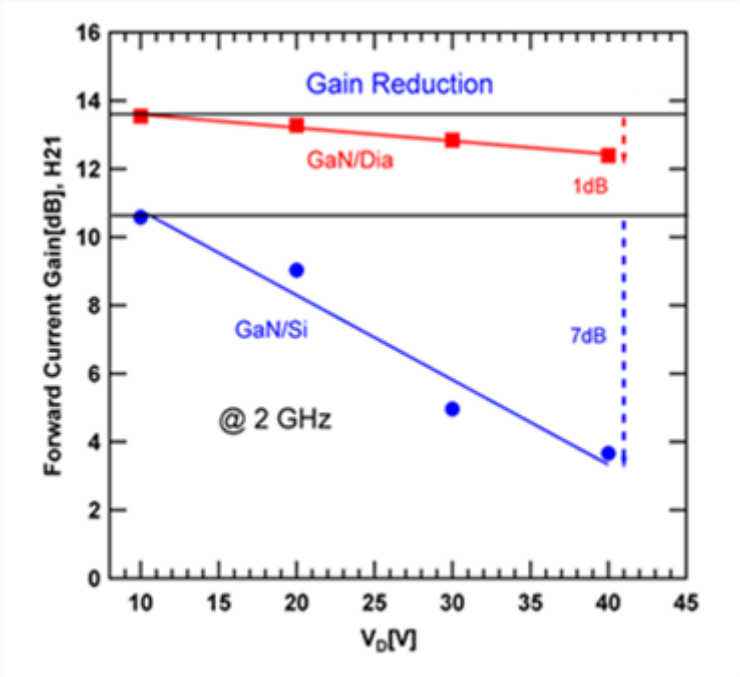


Figure 3.16 Current gain (H_{21}) of GaN/Dia and GaN/Si HEMTs for different V_D of a 2-µm gate GaN/Dia and GaN/Si HEMTs.

The reduction of H_{21} is associated with g_m reduction in the device as H_{21} depends on g_m as follows;

$$H_{21} = \frac{\partial I_d}{\partial I_g} = \frac{g_m \partial V_G}{j\omega C_g}$$

The reduction of H_{21} as a function of V_D is small (0.033 dB/V) in GaN/Dia which is almost constant in comparision with 0.233 dB/V in the case of GaN/Si. The lower reduction in H_{21} of GaN/Dia is mainly due to smaller reduction in g_m when compared with GaN/Si. These results indicate that GaN/Dia will be a better choice for developing high-power high-frequency

amplifier with almost flat gain for a wide range of drain bias operation. The f_T and f_{max} were also evaluated for different V_D from 10 – 40 V with V_g fixed at -1.0 V and -1.5 V for GaN/Dia and GaN/Si respectively as the respective f_T value was the highest at these gate bias voltages. The f_T reduction ($f_{Treduc.}$) was calculated using the formula;

$$f_{Treduc.}=(f_{Tmax} - f_{T\text{-}vd})\times 100/f_{Tmax}$$

where, f_{Tmax} is the maximum f_T value measured at V_D=10 V and $f_{T\text{-}vd}$ is the f_T obtained at different V_D). Fig. 3.17 shows the $f_{Treduc.}$ and $g_{mreduc.}$ versus P_D for both GaN/Dia and GaN/Si HEMTs. At 7 W/mm, GaN/Dia HEMTs exhibited only 8.2 % of $f_{Treduc.}$ whereas GaN/Si HEMTs exhibited much higher $f_{Treduc.}$ of 55%. This f_T ($f_T = g_m/2pi(C_{gs} + C_{gd})$) reduction is predominantly due to the g_m reduction (42 %) in GaN/Si devices. The additional reduction of 13 % in f_T could be attributed to the slight increase of $C_{gs} + C_{gd}$, as was observed for GaN on Si devices. It is also clear that the GaN/Dia HEMTs has ~6.75-times lower $f_{Treduc.}$ rate with P_D as compared to GaN/Si HEMTs. It is also observed that GaN/Si HEMTs have larger $f_{Treduc.}$ than $g_{mreduc.}$ at higher V_D whereas GaN/Dia HEMTs has an almost similar rate of $f_{Treduc.}$ and $g_{mreduc.}$ The reduction of f_{max} with increasing V_D was also calculated using the formula;

$$f_{maxreduc.}=(f_{max(max)} - f_{max\text{-}vd})\times 100/f_{Tmax}$$

where $f_{max(max)}$ is the f_{max} obtained at V_D=10 V and $f_{max\text{-}vd}$ is the f_{max}

obtained at a particular V_D.

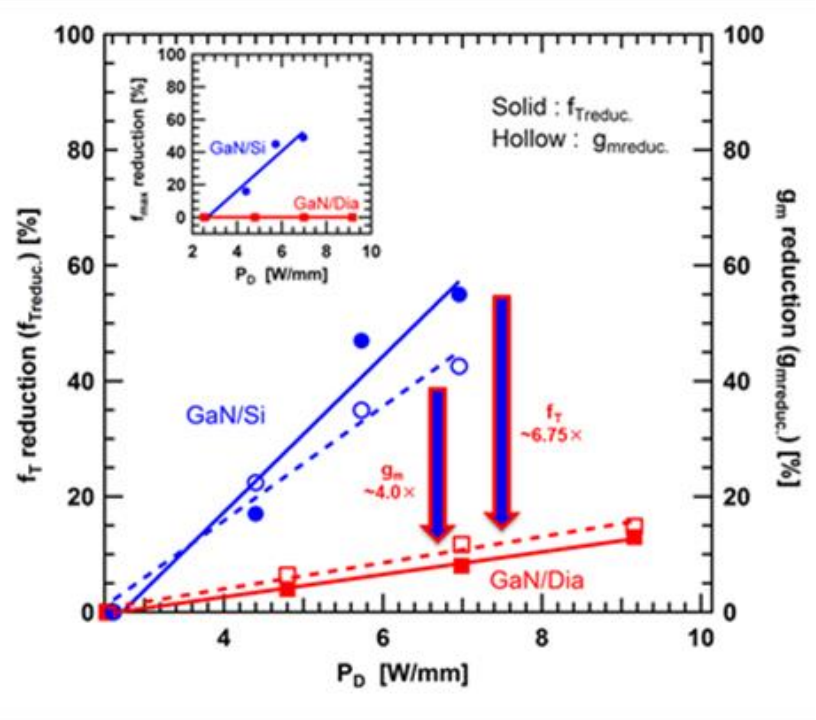


Figure 3.17 The f_T reduction ($f_{Treduc.}$) and g_{mmax} reduction ($g_{mreduc.}$) versus P_D of GaN/Dia and GaN/Si HEMTs. Inset: f_{max} reduction ($f_{maxreduc.}$) versus P_D for GaN/Dia and GaN/Si HEMTs.

The inset of fig. 3.17 shows the $f_{maxreduc}$ for both GaN/Si and GaN/Dia HEMTs. The $f_{maxreduc.}$ was obtained to be 49 % in the GaN/Si HEMTs while no significant reduction was observed in GaN/Dia HEMTs

To confirm these RF characteristics, small-signal equivalent circuit parameters were extracted from measured S-parameters at different V_D, following the proposed 22-element equivalent circuit model in the literature [65]. The small-signal equivalent circuit is explained in the

previous chapter. After the extraction of circuit parameters, the equivalent circuit model was incorporated in Advance Design System (ADS) circuit simulation software, as shown in fig. 3.18. The optimization method was used in ADS simulator to tune the extracted parameters.. Then the optimization process is carried out repeatedly in order to minimize the error between measured and simulated S-parameters through searching for the optimal values for those elements with some initially assumed values during the extraction procedure. Finally, small-signal equivalent circuit parameters were obtained. The circuit model and extracted parameters were verified by a comparison plot of measured and simulated S-parameters of device at respective bias conditions.

Figure 3.19 shows the comparison of measured (Smeas) and simulated (Smodel) S-parameters (1-20 GHz) (a) S11 and S22, and (b) S12 and S21 plots of 2-µm gate GaN HEMTs-on-CVD diamond at V_D=10V and I_D = 200mA/mm. The average error between the measured and simulated S-parameters over the entire frequency range was calculated to be ~ 2.5 %.

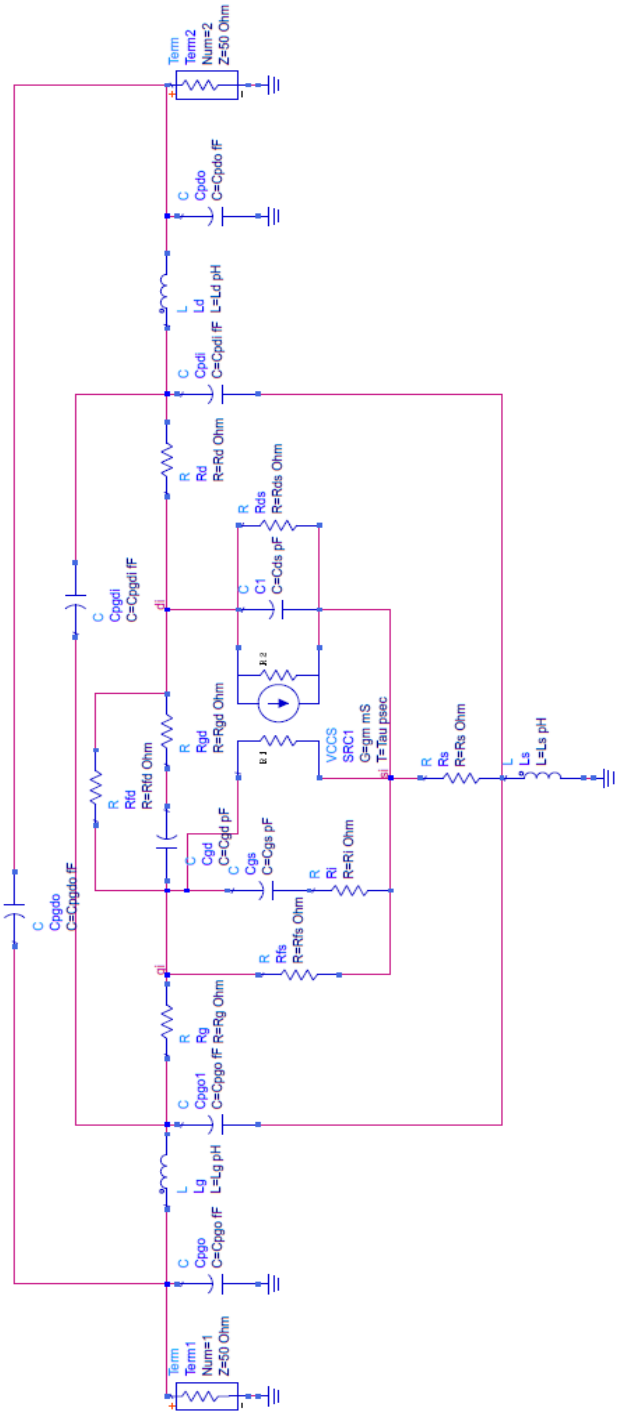


Figure 3.18 The small-signal equivalent circuit of 22-elements GaN HEMT modelled in ADS circuit simulator. Circuit elements are described in chapter 2.

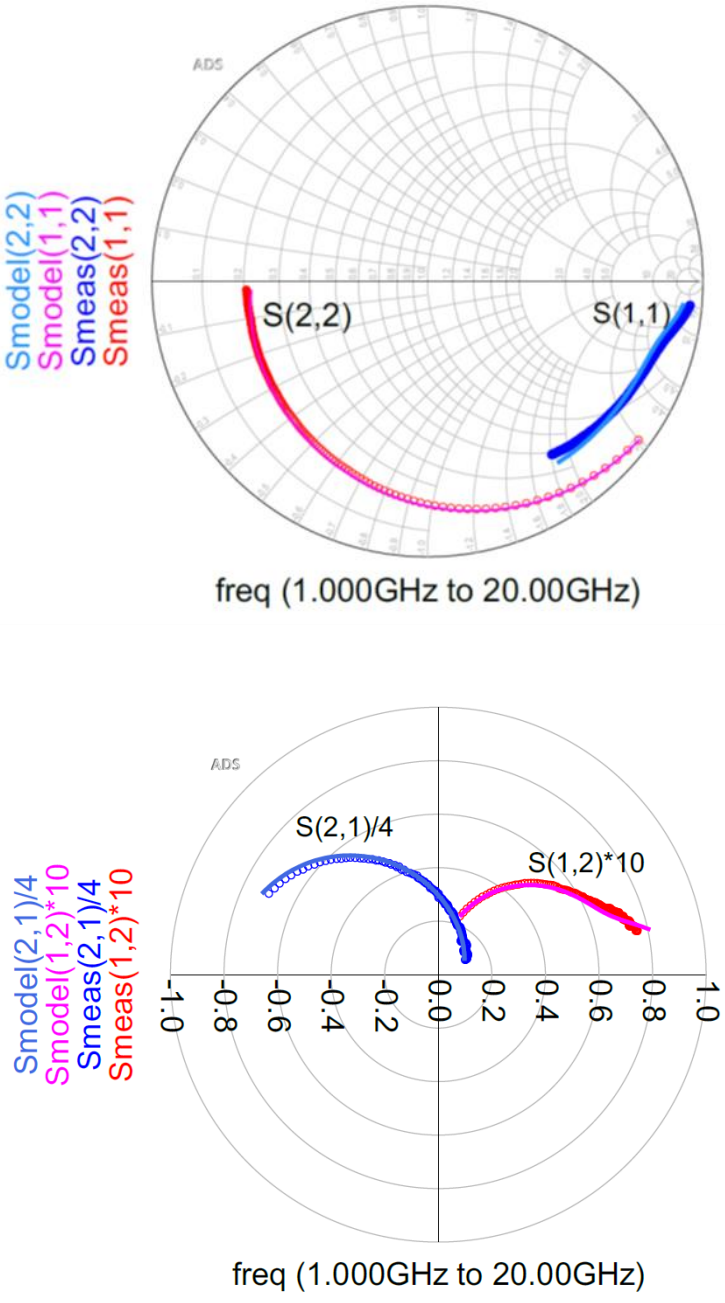


Figure 3.19 A comparison of the measured and modelled S-parameters for a GaN HEMTs-on-CVD diamond with a bias condition of V_D = 10 V and I_D ~ 200 mA/mm. (a) shows the S11 and S22, and (b) shows the S12 and S21 plot in smith chart.

It is observed that the intrinsic parameters, mainly g_m intrinsic (g_{mo}), C_{gs} and C_{gd} were affected more significantly at high V_D which is due to the increased junction temperature in the device. Extrinsic parameters have relatively less effect in small-signal performance in our device. It could be due to a lower rise of temperature in the parasitic area of the device than hot spot region. The extracted C_g (C_{gs}+ C_{gd}) at different V_D was shown in figure 3.20.

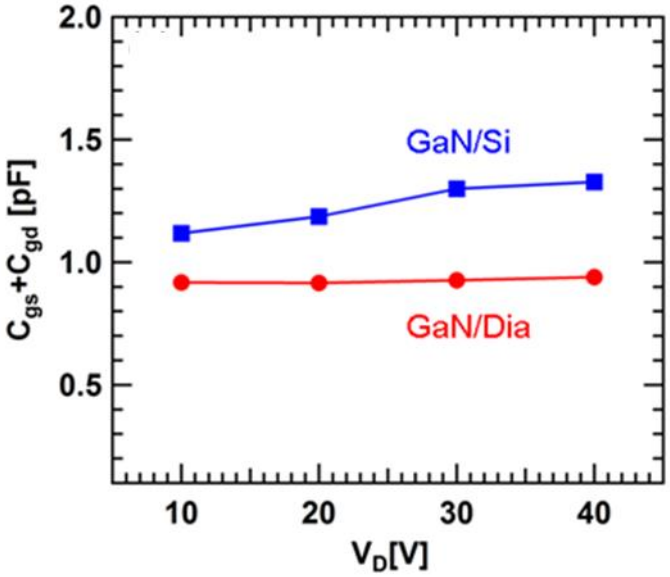


Figure 3.20 Extracted gate capacitance from measured small-signal characteristics GaN/Dia and GaN/Si HEMTs.

A small increase of C_g (~3 %) was observed in GaN/Dia as compared to ~16 % increase in GaN/Si. A large reduction of f_T in GaN/Si is due to the reduction of g_m and increase of C_g as f_T (f_T α (1/C_g)). A higher increase of C_{gs} in GaN/Si could be linked to the large junction temperature (T_j) at

higher V_D. The increase of C_{gs} with temperature in AlGaN/GaN HEMTs have also been reported by Roberto et al. [50]. This could be related to the changes that occurred in SiN passivate and AlGaN permittivities. The observed decreasing trend of C_{gd} with V_D has been previously reported [100, 101]. This could be due to the extension of the depletion region towards the drain side with an increase of V_D [101]. The reduction of C_{gd} can help to improve the f_{max} at higher V_D [102], assuming the f_T and gare resistance (R_g) is constant, as f_{max} is inversely proportional to the square root of C_{gd} and can be expressed as;

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_g \cdot C_{gd}}}$$

In addition, effective carrier mobility (μ_{eff}) was estimated from the extracted intrinsic transconductance (g_{mo}) which is associated with the device channel and can be expressed as;

$$g_{mo} = (\mu_{eff} C_{gs} \text{ x } W/L_g)(V_G - V_{TH}))$$

where W is the gate width (200 µm) and L_g is the gate length (2 µm), V_{TH} is the threshold voltage of device. The v_{eff} (effective carrier electron velocity) were also calculated from the measured f_T ($v_{eff} \approx f_T \times 2\pi L_g$), for both GaN/Si and GaN/Dia. The normalized μ_{eff} and v_{eff} versus V_D were plotted for both the HEMTs (See Fig. 3.21). Around 55 % reduction of μ_{eff} was observed in GaN/Si as compared to 18% in the case of GaN/Dia. A

comparatively higher reduction of μ_{eff} in GaN/Si occurred due to increased T_j at higher V_D. Extracted effective 2-DEG mobility with temperature in GaN HEMT has shown a similar trend in the reported literature [103] .

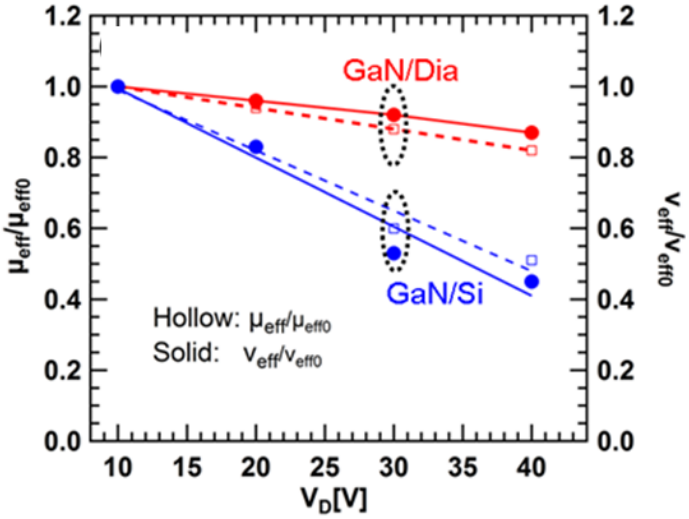


Figure 3.21 Extracted normalized effective carrier mobility (μ_{eff}) and effective carrier velocity (v_{eff}) versus drain bias characteristics V_D of a 2-µm gate GaN/Dia and GaN/Si HEMTs.

GaN/Dia HEMTs suffer ~ 3-times lower rate of μ_{eff} and v_{eff} reduction as compared to the GaN/Si HEMTs. These results show that GaN/Dia HEMTs can be operated even at higher V_D as well as at higher P_D which are paramount features for developing compact SSPAs for high power high-frequency CW application. But, for reliable operation of GaN/Dia HEMTs, trap behaviour needs to be well understood. We present a systematic trap characteristics investigation in GaN/Dia HEMTs in chapter

4 and chapter 5 of this thesis.

3.6 Summary

In conclusion, a quantitative investigation of the self-heating effect on DC and RF performances was carried out for AlGaN/GaN HEMTs on CVD-Diamond and Si substrates. Self-heating induced device performances were extracted at different values of dissipated DC power density (P_D) in continuous wave (CW) operating conditions. The GaN/Dia HEMTs exhibited ~ 5.7-times lower rate of $I_{Dreduc.}$ than GaN/Si HEMTs. This behavior was also confirmed by 2D device simulation which showed ~3.9-times lower rate of increase in junction temperature and lower thermal resistance (R_{th}) in GaN/Dia HEMTs in comparison with GaN/Si HEMTs. The f_{Treduc} reduction rate was ~6.75-times lower in the case of GaN/Dia than GaN/Si HEMTs whereas no significant reduction of f_{max} was observed in GaN/Dia HEMTs. Comparatively lower reduction rates (~3-times) of μ_{eff} and v_{eff} in GaN/Dia result in less performance degradation (~15%) as compared to (~50%) GaN/Si. These results show that GaN/Dia HEMTs can be operated even at higher V_D as well as at higher P_D which are paramount features for developing compact high power SSPAs for CW application.

4 Hetero-interface trap in AlGaN/GaN HEMTs -on-CVD diamond

In chapter 3, the self-heating effect in AlGaN/GaN HEMTs-on-CVD at high power density conditions was presented. For reliable operation at high power density, device trapping behavior needs to be understood. This chapter presents the investigation of hetero-interface trapping characteristics in AlGaN/GaN HEMT on CVD-diamond (GaN/Dia) using the conductance method. The conductance-frequency technique is used to estimate hetero-interface trap density and trap state energy. Temperature-dependent measurements were also carried out to study the deeper traps in the bandgap. Finally, the pulsed I_{DS}-V_{DS} measurements were carried out to correlate AlGaN/GaN interface trap behavior and current collapse in AlGaN/GaN HEMTs-on-CVD diamond.

4.1 Introduction

Traps arising from defects in the AlGaN/GaN heterostructure are responsible for current degradation, threshold voltage shift, and current collapse. These, in turn, limit the RF power and switching performance of the device during operation. Typically, for GaN-on-Diamond process development, the host Si or SiC substrate, and the growth-defect-rich stress mitigation transition layers are first removed. The remaining HEMT layers are then bonded onto CVD-diamond which now acts as the new

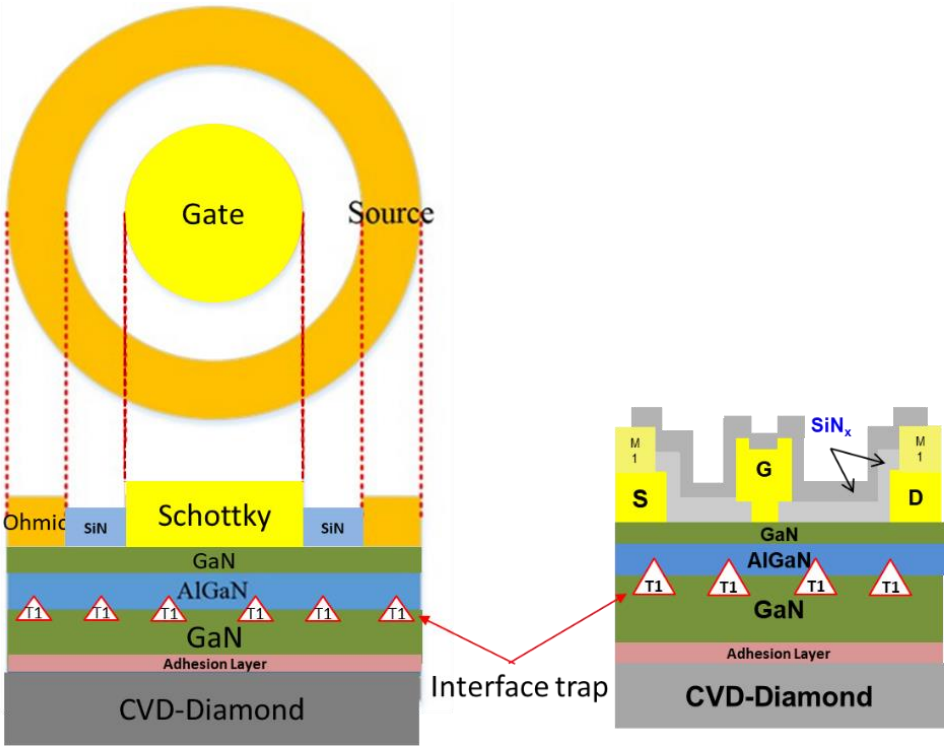
substrate. Thus, the overall quality of the GaN heterostructure could be affected by the substrate transfer process.

The host GaN HEMT-on-Si has a thick and complex GaN transition layer. It is typically used to minimize the lattice mismatch stress and help to grow the high-quality GaN buffer layer. The GaN transition layer in GaN HEMT-on-Si usually consists of pairs of AlGaN/AlN superlattice structures. Although this transition layer minimizes the stress/strain, still a significant stress/strain is present in the GaN transition layer and near-interface GaN region. Therefore, a high density of defects may present in the GaN transition layer as well as in the hetero-interface region. The GaN transition layer is generally referred to as defect rich transition layer [104]. Therefore, it is essential to investigate the trapping behaviour in the transferred GaN HEMTs on CVD-diamond.

4.2 AlGaNGaN HEMTs-on-CVD diamond: Device fabrication

The detailed epi structure of GaN HEMTs-on-CVD diamond was presented in chapter 3. In this study, GaN HEMT Schottky circular diode and sub-micron gate (0.25-µm) AlGaN/GaN HEMTs device were fabricated. The device fabrication started with the multiple energy Ar^+ implantations to define the device (AlGaN/GaN active region) isolation regions [105]. The ohmic contacts were formed by depositing

conventional Ti/Al/Ni/Au metal stacks followed by rapid thermal annealing at 825 °C for 30 s in an N_2 atmosphere. Next, 120-nm-thick SiN was deposited using plasma-enhanced chemical vapor deposition (PECVD). The gate foot-print of 0.25-μm for transistors, and of 50-μm diameter for Schottky diode, was formed by the electron beam lithography (EBL) followed by the etching of 120-nm SiN. The detailed gate process has been reported elsewhere [105]. The gate metal deposition was done with Ni/Ti/Au Schottky gate for diode and HEMTs. Then thick Ti/Au (50/1000 nm) metal layer was deposited, and the devices were passivated with 120-nm-thick SiN using PECVD. Figure 4.1 shows the schematic cross-sectional diagram of the (a) Schottky diodes and (b) 0.25-um gate AlGaN/GaN HEMTs on CVD-Diamond. Fig. 4.1 also illustrates the location of AlGaN/GaN hetero-interface traps in the heterostructure.



(a) (b)

Figure 4.1 Schematic cross-sectional diagram of the fabricated (a) Schottky diodes and (b) 0.25-um gate AlGaN/GaN HEMTs on CVD-Diamond.

Figure 4.2 shows the optical microscope image of fabricated AlGaN/GaN Schottky diode on CVD diamond. The ohmic region of circular diode was extended in the device layout. For trapping analysis, the Capacitance-Voltage (*C-V*) and Conductance–Frequency (*G-f*) measurements were carried out on 50-µm diameter Schottky diodes (See Fig.4.2). The *G-f* measurements are done for the various frequency points between 5 KHz and 5 MHz. Both the *C-V* and *G-f* measurements were performed at different temperatures (25, 50, 100, 150, and 200 °C) using Cascade

Microtech Summit 200 thermal probe station integrated with B1505A Power Device Analyzer / Curve Tracer. The AC signal amplitude of 50 mV was maintained for *C-V* and *G-f* measurements. To observe the interface trap effects on drain current collapse, pulsed (pulse width/period = 200 ns/1 ms I_{DS}-V_{DS}) characterization was conducted on 0.25-µm gate HEMTs (W_g = 2 × 150 µm) (see Fig. 4.3) using Accent DiVA D265 system.

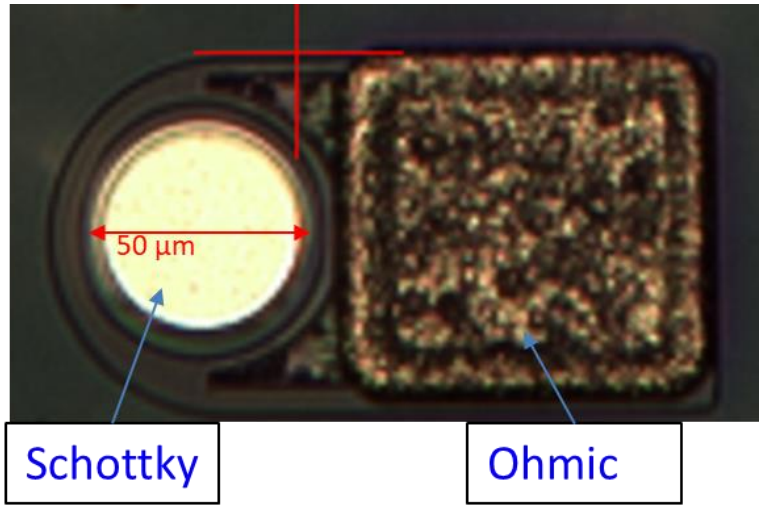


Figure 4.2 Optical microscope image of fabricated AlGaN/GaN Schottky diode on CVD diamond.

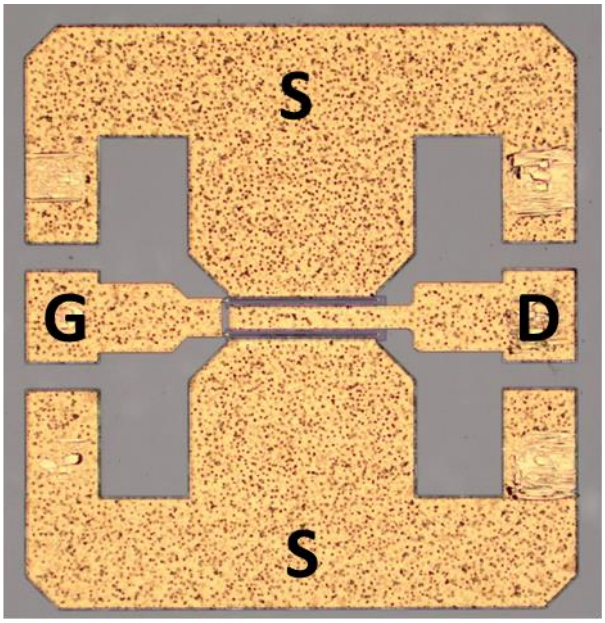


Figure 4.3. Optical microscope image of fabricated AlGaN/GaN HEMTs on CVD diamond, showing source (S), Gate (G), and Drain electrode (D).

4.3 C-V characteristics

Temperature-dependent *C-V* measurements were performed on a 50-µm diameter Schottky diode. Figure 4.4 shows the *C-V* characteristics at a frequency of 1 MHz of the fabricated Schottky diode at different ambient temperatures. The quantitative value of accumulated capacitance was obtained around ~320 nF/cm^2 at room temperature. The measured capacitance is close to the reported values of accumulated charge capacitance in the MOCVD grown AlGaN/GaN HEMT [106, 107]. The accumulation region capacitance values are almost the same at all the measured temperature. A threshold voltage (V_{th}) of ~ -2.5 V was obtained from the *C-V* plot. A negligible V_{th} shift (ΔV_{th} ~ 30 mV) was also observed

in the *C-V* characteristics when the measurement temperature increases from 25 °C to 200 °C. For the same range of temperature, a large positive V_{th} shift (ΔV_{th} ~ 1.5 V) was observed in the C-V characteristics in the AlGaN/GaN HEMT-on-Si substrate.

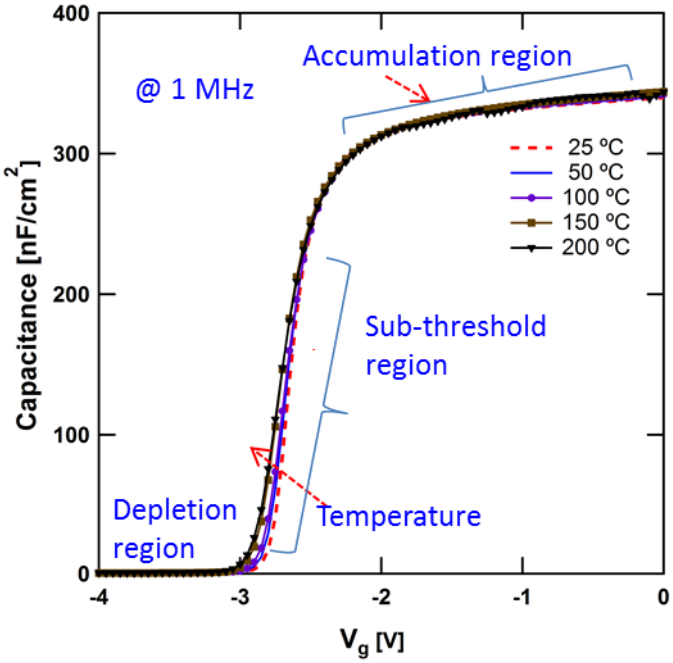


Figure 4.4 Normalized C-V characteristics of AlGaN/GaN Schottky diode-on-CVD diamond at 1 MHz for different temperatures (25 - 200 °C).

The 2DEG concentration (from accumulation region in the *C-V* plot) with temperature is almost constant in the measured temperature of 25-200 °C. The depth versus concentration was estimated from the C-V characteristics by using the following equation [88],

$$n_s = \frac{1}{e}\int C\,dV$$

Figure 4.5 shows the depth versus concentration was estimated from the *C-V* characteristics, and the maximum value is indicating 2DEG concentration, which is almost the same for all the measured temperature.

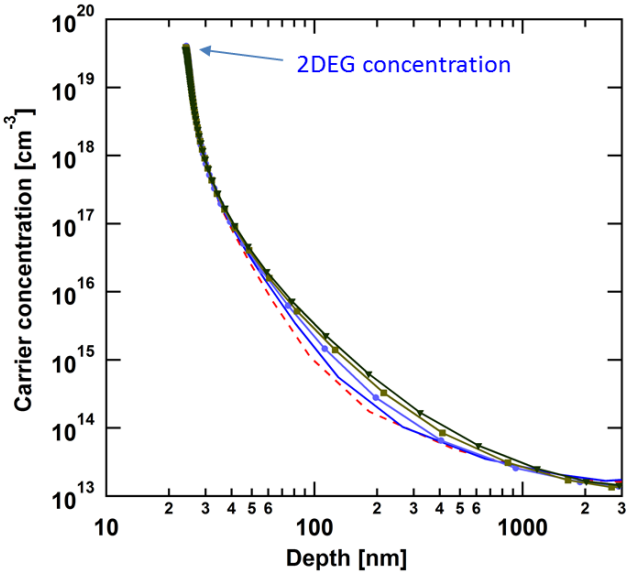


Figure 4.5 Depth versus concentration profile of AlGaN/GaN HEMT-on-CVD diamond.

4.4 *G-f* characteristics and trap density estimation

The energy band diagram schematic illustrating traps at AlGaN/GaN interface trap was shown in fig. 4.6. To quantify these interface traps, parallel conductance (G_p) at AlGaN/GaN interface was evaluated by *G-f* measurements [68] on the fabricated Schottky diode.

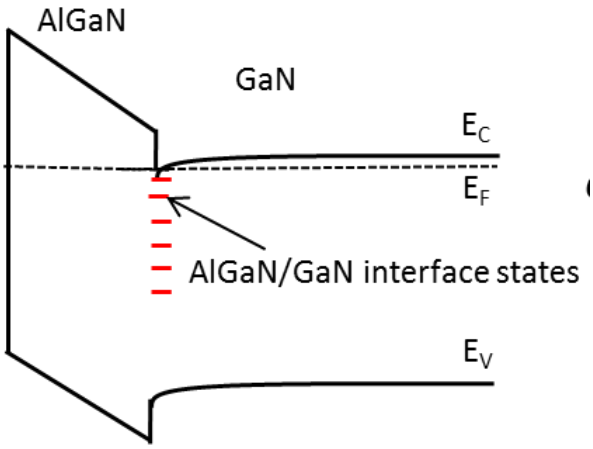


Figure 4.6 Schematic energy band diagram illustrating traps at AlGaN/GaN interface trap

The conductance (G_p) in the device represents the loss mechanism due to the capture and emission of carriers at the AlGaN/GaN interface traps. AC conductance method is based on evaluating the loss which is caused by the change in the trap level charge state and thus is a sensitive method to determine trap density [97]. The conductance method has been widely used to measure the interface trap density in GaN HEMT [92, 95]. Figure 4.7 shows a simplified equivalent circuit of a diode for interface trap density calculation by AC conductance method.

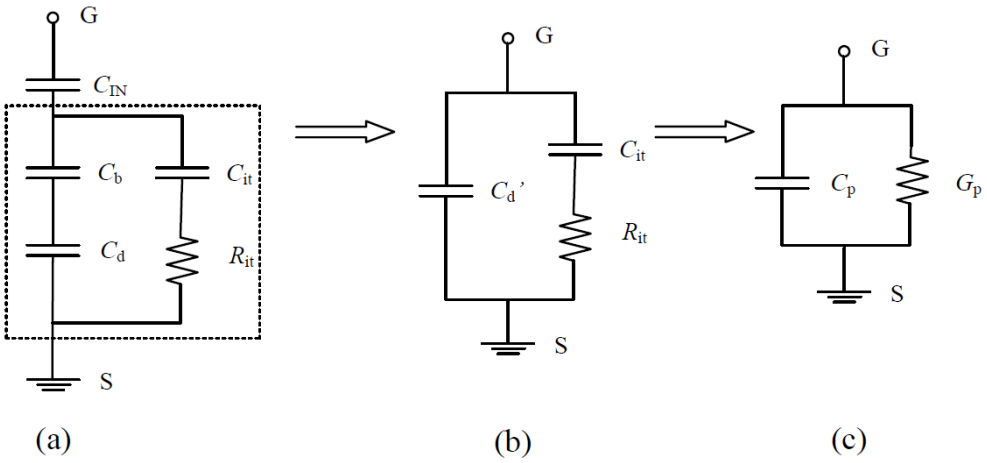


Figure 4.7 Simplified equivalent circuit of a diode for interface trap density calculation by AC conductance method (*G-f*), where G_p is parallel conductance which is measured at a wide range of frequencies by conductance frequency technique [65].

The *G-f* measurements were performed on the Schottky diode at room temperature at different *V*g. Fig. 4.8 shows the G_p/ω versus ω plot of GaN/Dia Schottky diodes at 25 °C, where ω is radial frequency. The G_p/ω peak value increases as the V_g increases from -2.9 to -2.6 V (towards V_{th} = -2.5 V). This indicates that the Fermi level (E_F) at the AlGaN/GaN interface moves towards the conduction band and the traps respond to the AC signal during *G-f* measurements resulting in an increase of G_p/ω. Similar behaviour of G_p/ω with V_g has been reported by researchers [80, 87]. Fig. 4.8 also shows that the single peak was observed in G_p/ω curve at each V_g, which indicates that only one type of dominating trap exists at the AlGaN/GaN interface in the measured frequency range.

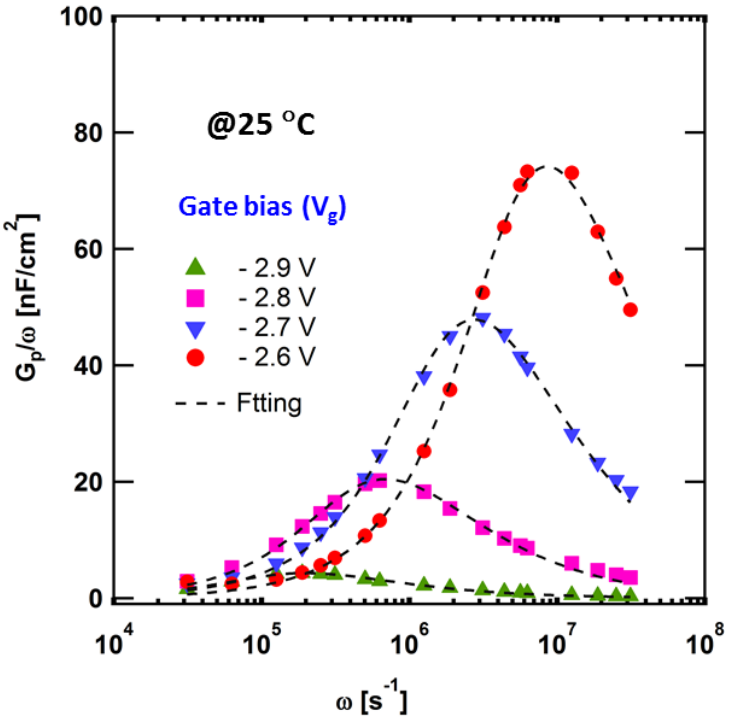


Figure. 4.8 Variation of conductance versus radial frequency for different gate voltages at 25 °C, dotted black lines represent the fitting curve of experimental G_p/ω values.

Furthermore, estimation of the trap density (D_T), assuming a continuum of trap levels, was extracted by fitting the experimental G_p/ω data using equation (1),

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln[1+(\omega\tau_T)^2] \qquad (1)$$

The trap time constant (τ_T) was extracted by fitting the experimental G_p/ω data using equation (1). The value of τ_T can also be obtained from the frequency where G_p/ω peak occurs, as $\tau_T \cong 2 / \omega$ [65]. At 25°C, τ_T was found to be in the range of 0.21 - 10.01 µs and considered as a fast trap

in this work. A similar range of τ_T has been reported as a fast trap in the AlGaN/GaN HEMTs [88]. Researchers have also reported the presence of fast traps in the AlGaN/GaN interface near the channel which was confirmed by techniques such as frequency-dependent conductance analysis [108], noise spectral studies [109], and deep level transient spectroscopy (DLTS) [110]. The trap state energy (E_T) was estimated with obtained τ_T using the equation, deduced from Shockley-Read-Hall (SRH) statistics.

$$\tau_T = \frac{1}{\sigma_T v_t N_C} \exp\left(\frac{E_C - E_T}{kT}\right)$$

where σ_T is the capture cross-section (3.4×10^{-15} cm^{-2}), v_t is the thermal velocity of electrons (2.6×10^7 cm/s), T is temperature, and N_C is the effective density of states ($4.3 \times 10^{14} \times T^{3/2}$ cm^{-3}) at the conduction band in GaN and k is the Boltzman constant [80, 82]. Fig. 4.9 shows the trap density versus trap state energy level, obtained at 25 °C of measurement temperature.

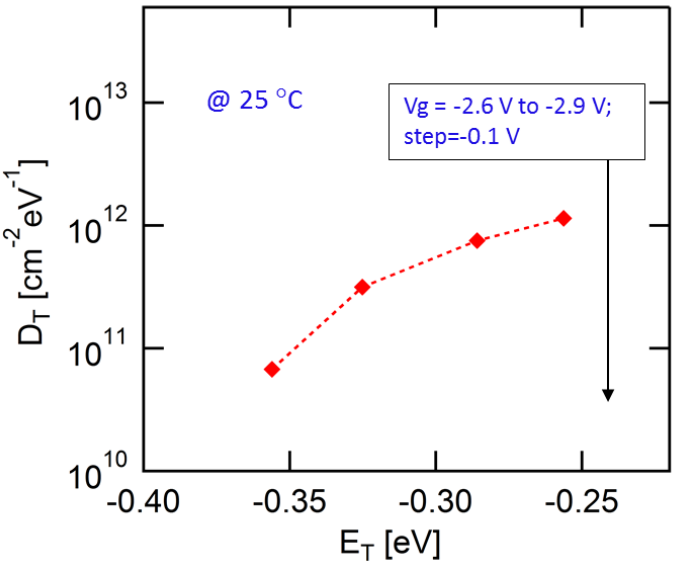


Figure 4.9 Estimated interface trap density and trap state energy level, relative to the conduction band, for different V_g (-2.9 V to -2.6 V, ΔV= -0.1 V) measured at 25 °C.

Figure 4.9 shows the trap density versus trap state energy extracted from the G_p/ω measurements at 25 °C. The D_T was obtained in the range of 6.7×10^{10} – 1.1×10^{12} cm^{-2} eV^{-1}. The trap state energy (E_T) was obtained in the range of 0.27 – 0.37 eV below the conduction band. The G-f measurements were also carried out at elevated temperatures different temperatures (25, 50, 100, 150, and 200 °C) at fixed Vg. Figure 4.10 shows the G_p/ω versus ω plot at V_g = -2.7 V for different temperatures (25 to 200 °C). The G_p/ω peak increased with increasing temperatures which could be attributed to the excitation of deeper traps in the bandgap with an increase in temperature [80, 88]. Apart from the increase in G_p/ω

peaks, it was also observed that the G_p/ω peak shifts towards the higher frequencies (reducing the time constant).

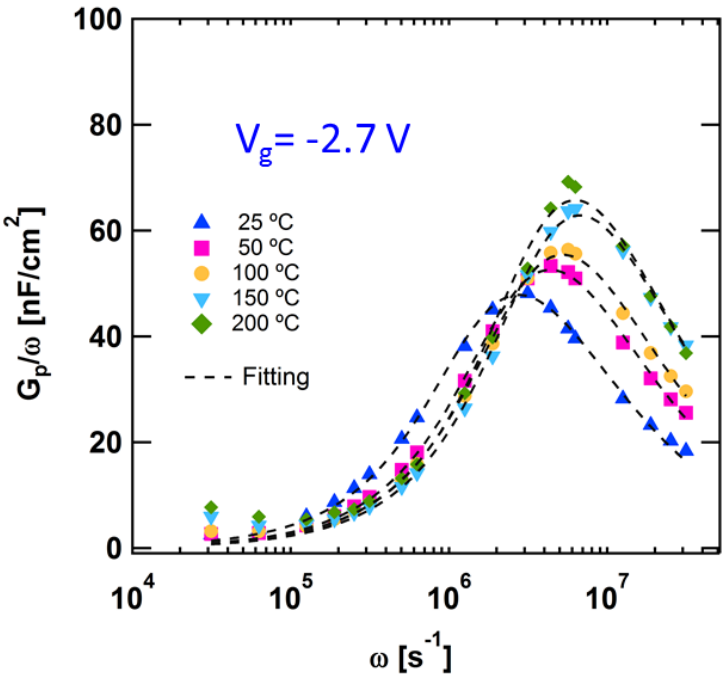


Figure 4.10 Variation of conductance versus radial frequency at a fixed gate voltage for different temperatures (25- 200 °C). Dotted black lines represent the fitting curve of experimental G_p/ω values.

The trap time constant values were detected from fitting the equation (1) and obtained in the range of 0.71 – 0.31 µs between 25 °C and 200 °C (See Fig. 4.11).

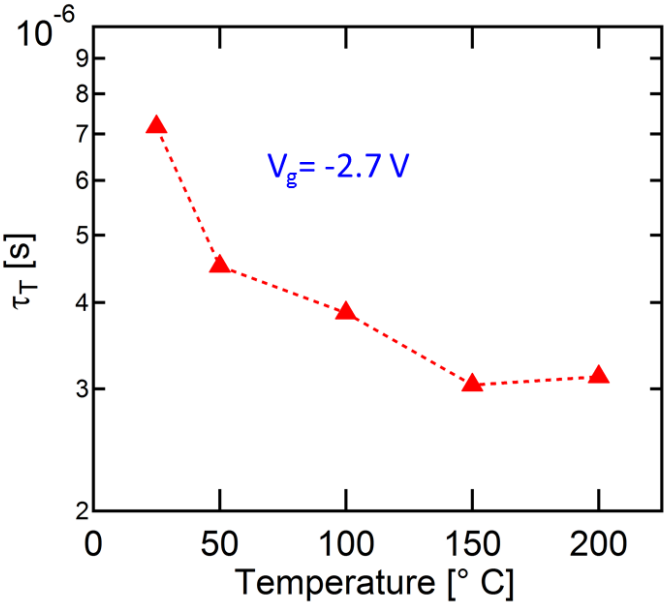


Figure 4.11 Trap time constants extracted from fitted data at different temperatures at fixed V_g.

Figure 4.12 shows the trap density versus trap state energy extracted from the G_p/ω measurements at various temperatures (25 - 200°C). At 25 °C, the D_T was obtained in the range of 6.7×10^{10} – 1.1×10^{12} cm^{-2} eV^{-1} and increased to the maximum value (D_{Tmax}) of 1.4×10^{12} cm^{-2} eV^{-1} at 200 °C. The increase of D_T with temperature implies that the additional deep traps are getting activated at elevated temperatures. This was confirmed by the increase in E_T from 0.27 – 0.37 eV at 25 °C and increased to 0.45-0.51 eV at 200 °C. A similar increase in trap energy states at elevated temperature was also reported by Kordos et al. [106].

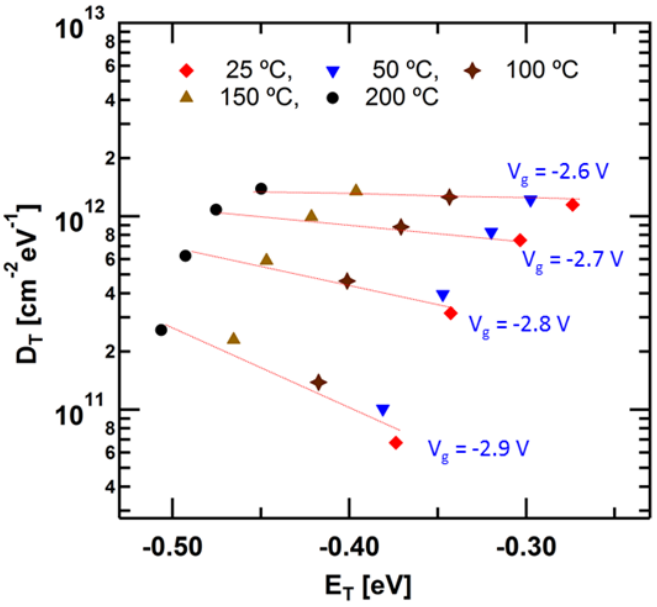


Figure 4.12 Estimated interface trap density and trap state energy level, relative to the conduction band, for different V_g (-2.9 V to -2.6 V, ΔV= -0.1 V) measured at various temperatures (25- 200 °C).

The D_T obtained in this study was also compared with the reported D_{Tmin} in AlGaN/GaN HEMT on different substrates. For a fair comparison, we selected references in which D_T estimation was done using the conductance technique only. Figure 4.13 shows the comparison of D_{Tmin} in AlGaN/GaN heterostructure on various substrates. Most of the reported D_{Tmin} values are in the range of 10^{10} - 10^{13} cm^{-2} eV^{-1}, measured at room temperature. We obtained the D_{Tmin} of 6.7×10^{10} cm^{-2} eV$^{-1,}$ which is around one order lower than that of reported value for thin GaN layer (< 1 µm) based AlGaN/GaN HEMTs on conventional substrates [107]. This could be due to the absence of the trap rich transition layer (AlN/GaN

superlattice structure) as compared to the conventional GaN/Si HEMT structure [107].

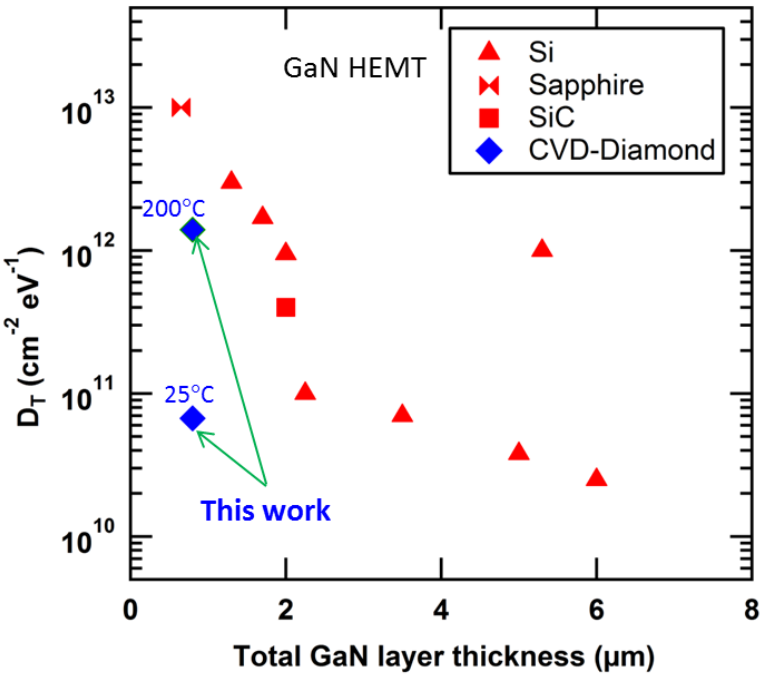


Figure 4.13 A comparative chart of interface traps density (D_T), estimated using conductance method, in GaN HEMTs on Si [74, 80-83, 87], GaN HEMTs on Sapphire [111], GaN HEMTs-on-SiC [88], and GaN HEMTs-on-CVD diamond substrates (this work).

4.5 Pulsed-IV characteristics

After the estimation of interface trap density, the I_D collapse due to a hetero-interface trap was investigated by doing pulsed I_{DS}-V_{DS} measurements in the fabricated HEMTs at selective stress bias

conditions. Moderate bias (Q-Bias for Gate-lag) was applied for pulse measurements to correlate the hetero-interface traps (T3 in fig 4.14) [112].

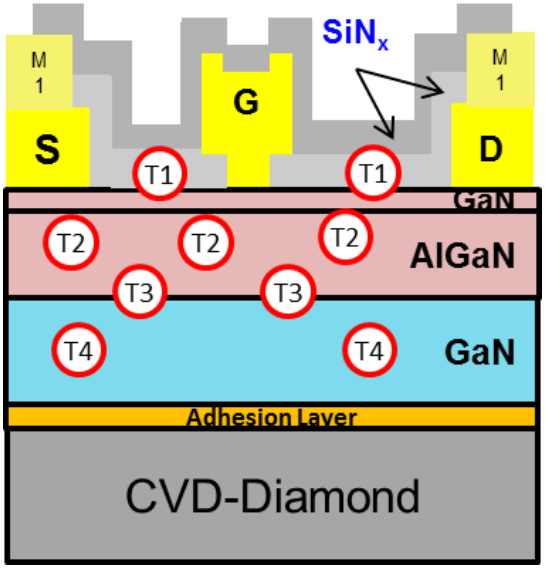


Figure 4.14 Schematic cross-sectional diagram of AlGaN/GaN HEMT illustrating the possible locations of traps: trap T1 at the surface, trap T2 in the AlGaN barrier, trap T3 at the GaN/AlGaN interface, and trap T4 in the GaN buffer.

The gate quiescent voltage (V_{GS0}) was applied close to the V_{th} (-2.5 V), and drain quiescent voltage (V_{DS0}) was fixed to zero volt. In this condition, gate electrons could be trapped mainly under the gate in the AlGaN/GaN interface region [113], and drain current collapse can be observed during Pulsed I_{DS}-V_{DS} characterization. Fig. 4.15 shows the pulsed I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs at V_{GS} = +1 V with unstressed condition [(V_{GS0}, V_{DS0} = (0, 0) V] and different quiescent voltage [(V_{GS0}, V_{DS0}= (-2.5/ -2.7/ -2.9, 0) V]. It is

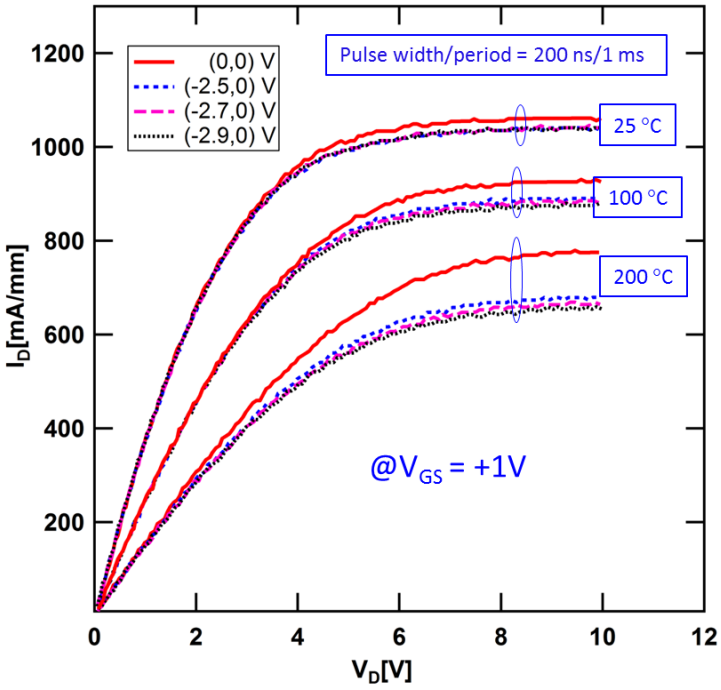


Figure 4.15 Temperature-dependent pulsed I_{DS}–V_{DS} characteristics of HEMTs stressed at various quiescent bias conditions.

The I_D collapse in the device was found to be as low as 1.9 % at 25 °C. The I_D collapse increased with temperature and found to be 9.5 % at 200 °C (See Fig. 4.16).

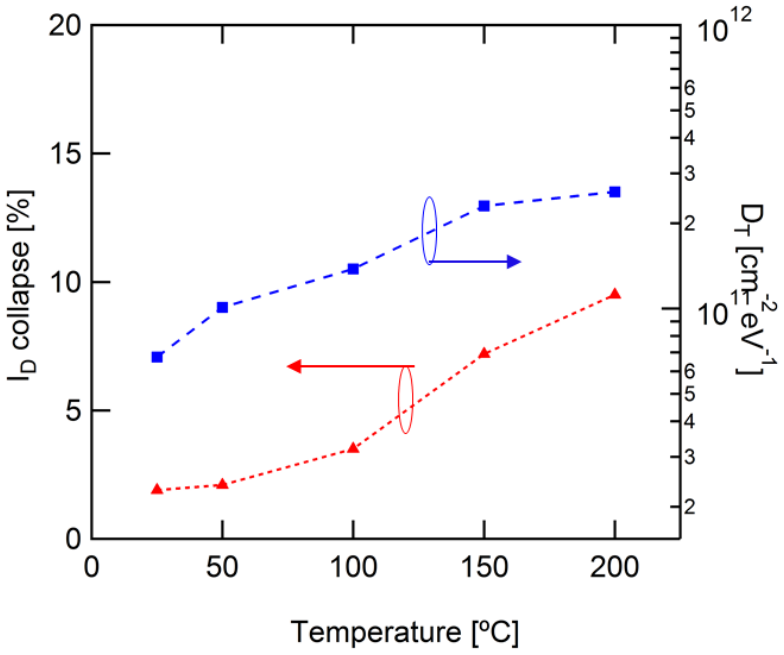


Figure 4.16 Variation of I_D collapse and D_T at different temperatures (25-200 °C).

The increase of I_D collapse also indicates the activation of more hetero-interface traps at higher temperatures. This is in good agreement with the behavior of D_T with temperature obtained using the *G-f* method in AlGaN/GaN HEMTs-on-CVD diamond. In addition, higher stress bias was also applied to the device to observe current collapse characteristics. Typically, higher drain quiescent bias is used for buffer related traps. The current collapse was measured with higher V_{gs0}= -5 V and V_{ds0}= 10 V and observed increased current collapse (14%) compared with gate-lag (~2%) measurements (See Fig. 4.17). Increased current collapse at higher

stress conditions indicates the excitation of more traps which could be associated with GaN buffer layer [30].

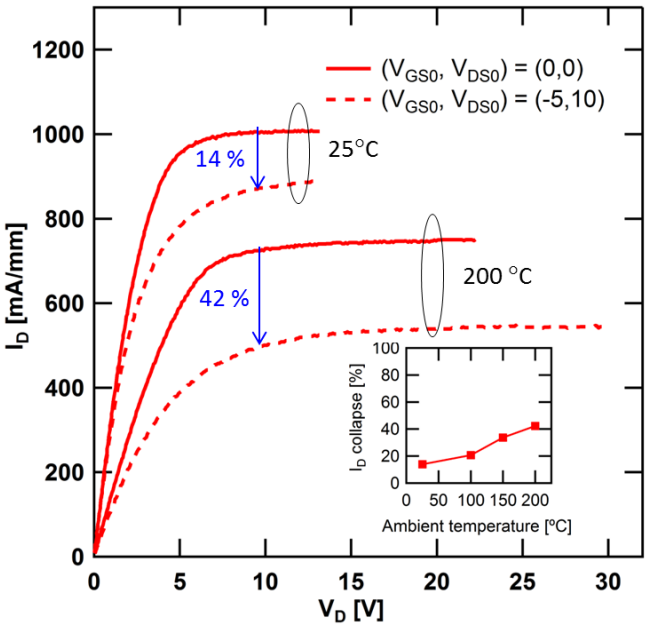


Figure 4.17 Temperature-dependent pulsed I_{DS}–V_{DS} characteristics (V_g=+1V) of HEMTs stressed at higher quiescent bias conditions, (Inset) variation of I_D at collapse at different temperatures (25- 200 °C).

4.6 Summary

In conclusion, we have investigated the hetero-interface trapping characteristics in AlGaN/GaN HEMT on CVD-diamond at different temperatures (25 °C to 200 °C) using the conductance method. The fast traps (0.16 to 10.01 µs) were identified as the dominating traps in our HEMT structure. The density of fast traps increases with temperature from 6.7×10^{10} cm^{-2} eV^{-1} at 25 °C to 1.4×10^{12} $cm^{-2}eV^{-1}$ at 200 °C. For

temperatures of 25 °C to 200 °C, the interface trap state energy (E_T) was obtained to be between 0.27 and 0.51 eV below the conduction band. The observation of increased D_T with temperature could be due to the excitation of additional traps deeper in the band-gap. The observation of a lower value of D_{Tmin} for GaN-on-CVD Diamond compared to GaN on Silicon devices is attributed to the removal of the defect-rich GaN transition layer during the substrate transfer process. Finally, the temperature-dependent pulsed I_{DS}-V_{DS} measurements revealed good agreement with the behaviour of D_T with temperature obtained using *G-f* method.

5 Interface trap in AlGaN/GaN MIS-HEMTs - on-CVD diamond

In the previous chapters, a detailed analysis of improvement in the device performance of GaN/Dia HEMTs has been presented. To further improve the device performance such as reduced gate leakage, AlGaN/GaN Metal-Insulator-Semiconductor HEMTs (MIS-HEMTs)-on CVD diamond were fabricated and analyzed. However, MIS-HEMTs may inherit large interface trap densities between the gate dielectric and GaN cap layer that need to be investigated. In this chapter, a systematic investigation of interface trap characteristics in SiN_x/AlGaN/GaN MIS-HEMTs on-CVD diamond was carried out. Conductance-Frequency (*G-f*) measurement techniques were used to estimate the trap densities which were compared with identically fabricated conventional Schottky GaN HEMTs-on-CVD diamond substrate (conv. HEMT).

5.1 Introduction

AlGaN/GaN MIS-HEMT exhibits improved device performance, such as high linearity high current density (I_D) and low gate leakage current [113-116]. Low gate leakage current in MIS-HEMTs helps improve device operation at the higher gate and drain voltages. Moreover, MIS-HEMTs can also exhibit high output power (P_{out}), operating at high drain current

and high drain voltage. However, increasing the operating voltage of the GaN MIS-HEMTs on conventional substrates results in significant self-heating of the device and degrades the drain current in saturation region. The use of a highly thermal conductive substrate (Diamond) overcomes this self-heating problem and allows the operation at high power density.

Even though the use of diamond substrate facilitates devise performance in high power densities, they may inherit large interface trap densities (~ 10^{12} -10^{14} cm^{-2}) during the introduction of an additional gate dielectric layer in comparison to conventional HEMTs [117]. These interface traps deteriorate the device switching performance through charging and discharging phenomenon which is dependent on the trap time constants [118]. Therefore, understanding the trapping behaviour and quantitative estimation of such interface traps are essential for GaN-based MISHEMTs. The location of these trap states can be identified by using a frequency-dependent conductance technique. To the best of our knowledge, no reports are available on interface trap density investigation in GaN MIS-HEMTs on CVD diamond.

In this work, we have systematically investigated the trap density (D_T) and trap state energy (E_T) in SiN_x/GaN/AlGaN/GaN MIS-HEMTs on-CVD diamond. Conductance-Frequency (*G-f*) measurement techniques were used to estimate the trap densities which were compared with identically fabricated conventional Schottky GaN HEMTs-on-CVD diamond

substrate (conv. HEMT). The cross-sectional schematic diagram of AlGaN/GaN MIS-HEMT on CVD diamond substrate is shown in fig. 5.1.

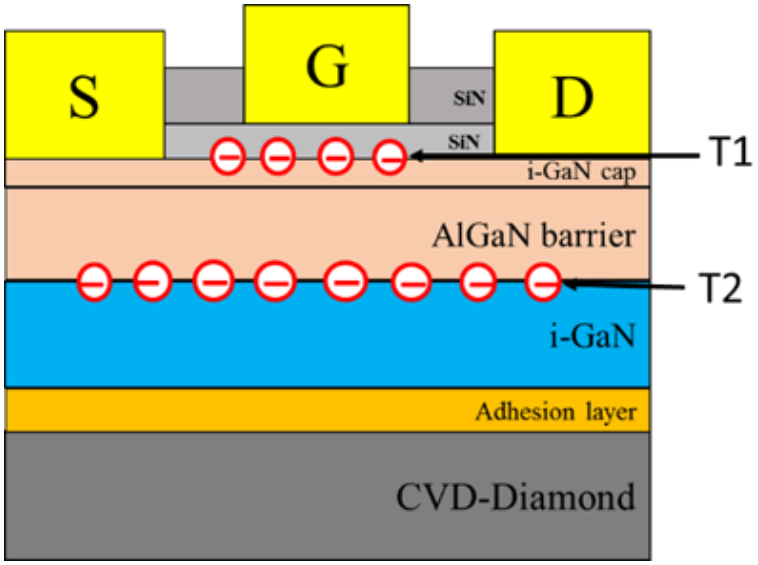


Figure 5.1 Cross-sectional schematic diagram of AlGaN/GaN MIS-HEMT with SiN dielectric on CVD diamond substrate. T1 and T2 represent the SiN/GaN interface trap and AlGaN/GaN hetero-interface traps, respectively.

5.2 Device fabrication

The samples were fabricated using a conventional optical lithography process. The fabrication processes started with mesa isolation by ICP etch using BCl_3/Cl_2 gas chemistry. Subsequently, the ohmic contacts were formed with a metal stacks scheme of Ti/Al/Ni/Au (20/120/40/50-nm) followed by rapid thermal annealing at 825 °C for 30 s in N_2 atmosphere.

A low R_C value of 0.23 ± 0.03 Ω-mm was achieved. The samples went through ammonium sulphide [$(NH_4)_2S_x$] surface treatment before subjecting SiN insulator deposition. The [$(NH_4)_2S_x$] surface treatment was done to minimize the interface traps and dangling bonds on the surface of GaN [72, 119]. A 20 nm thick SiN_x gate dielectric was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 300 ºC. The gate metal contact is formed by E-beam evaporation. In this case, the Ni/Ti/Au (150/100/300 nm) gate metalization was formed using conventional lithography and e-beam evaporation followed by a lift-off process. The devices were passivated with 120-nm-thick SiN. The cross-sectional schematic diagram of AlGaN/GaN MIS-HEMT with SiN dielectric is shown in fig. 5.2. The optical microscope image of fabricated AlGaN/GaN MIS-Diode and MIS-HEMTs is shown in fig. 5.3 (a) and 5.3 (b), respectively.

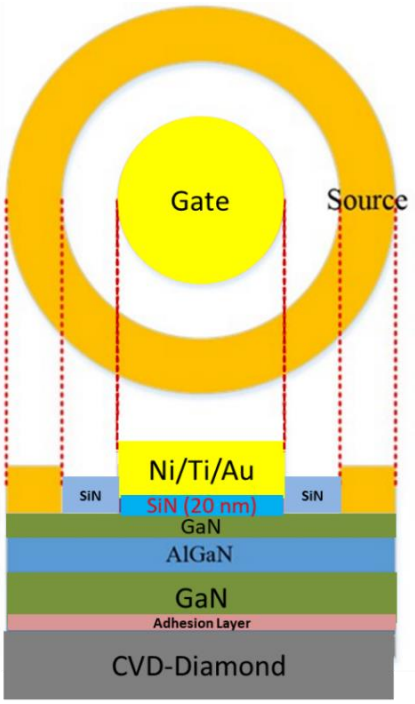


Figure 5.2 Cross-sectional schematic diagram of AlGaN/GaN MIS-HEMT with SiN dielectric on CVD diamond substrate.

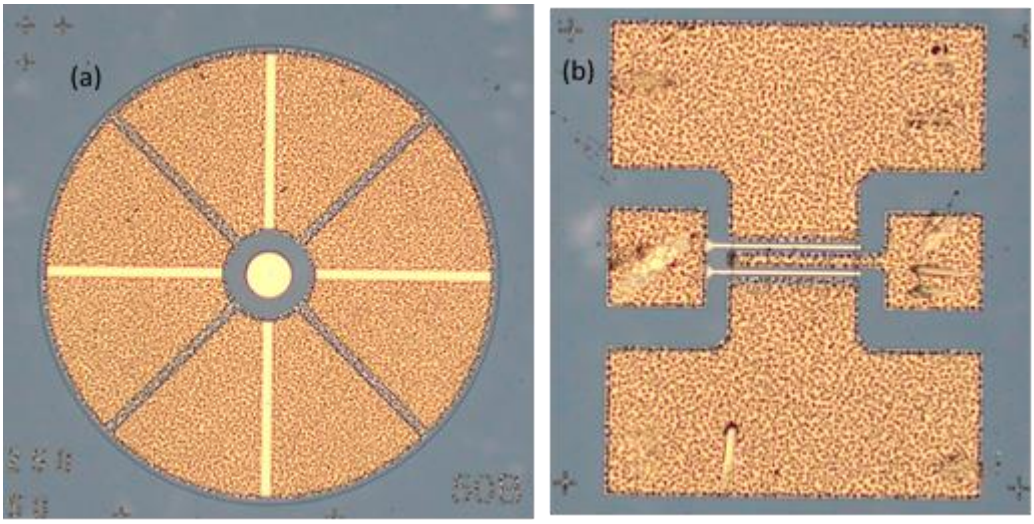


Figure 5.3 Optical image of AlGaN/GaN (a) MIS Diode and (b) MIS-HEMT on CVD diamond substrate.

The cross-sectional TEM image of fabricated AlGaN/GaN MIS-HEMT on CVD diamond shows the SiN thickness ~ 19.4 nm (See Fig. 5.4).

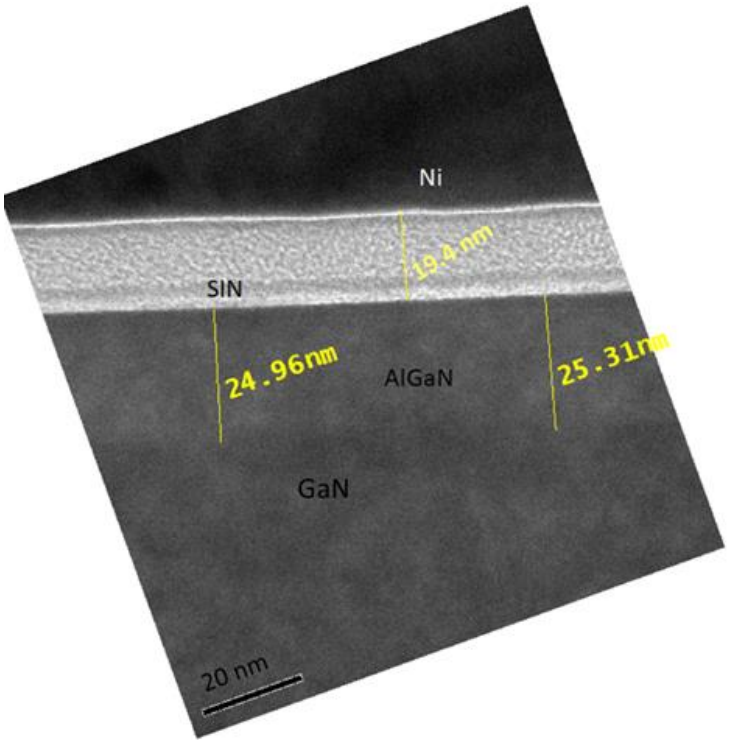


Figure 5.4 Cross-sectional TEM image of fabricated AlGaN/GaN MIS-HEMT on CVD diamond, focusing SiN dielectric on CVD diamond substrate.

The DC transfer characterization was conducted on 2-µm gate HEMTs (W_g = 2 × 100 µm). For trapping analysis, Capacitance-Voltage (*C*-*V*) and Conductance–Frequency (*G*-*f*) measurements were carried out on 50-µm diameter circular diodes in the frequency range between 5 KHz and 5 MHz at room temperature using Cascade Microtech summit 11000M Tesla probe station integrated with B1505A Power Device Analyzer/Curve Tracer.

5.3 DC characteristics

Figure 5.5 (a) shows the DC I_{DS}-V_{DS} characteristics of AlGaN/GaN MISHEMTs on CVD diamond and 5.5 (b) shows the DC I_{DS}-V_{DS} characteristics of AlGaN/GaN MISHEMTs on Si substrate. The self-heating effect in drain current (I_D) reduction in the saturation region can be clearly observed in GaN/Si MIS-HEMTs. In contrast, no significant I_D reduction was observed in GaN-on-CVD diamond MIS-HEMTs. Thus, GaN/Dia MIS-HEMTs can be operated at much Vd and dissipation power density (P_D= V_D × I_D) as compared to GaN/Si MISHEMTs.

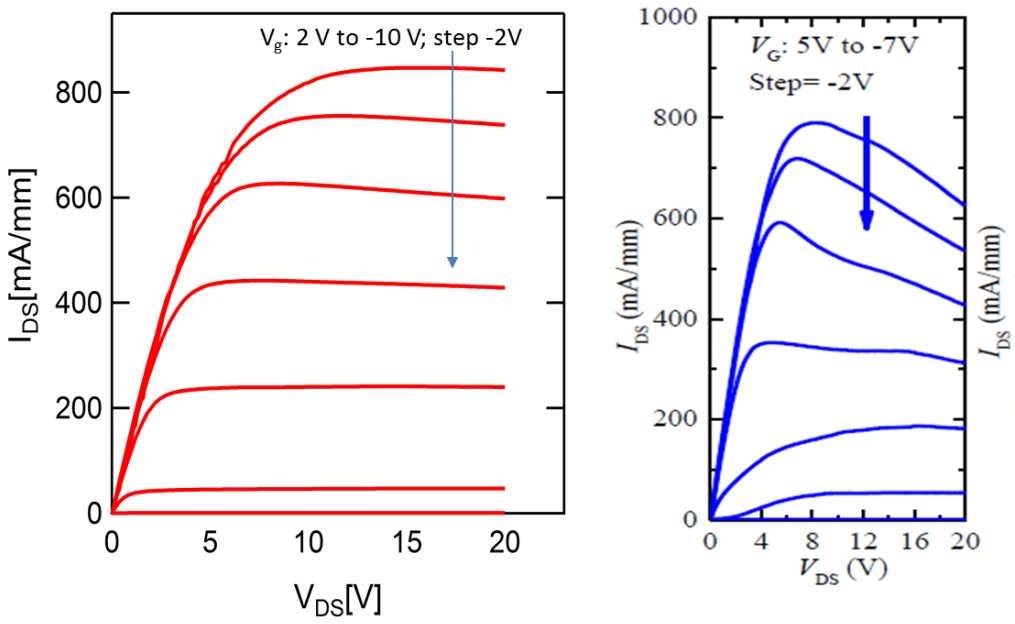


Figure 5.5 I_{DS}-V_{DS} characteristics for (a) AlGaN/GaN MISHEMTs on CVD diamond (b) AlGaN/GaN MIS-HEMTs on Si substrate [117].

Figure 5.6. shows the comparative DC transfer characteristics of GaN/Dia MIS-HEMTs and GaN/Dia HEMTs. The advantage of higher drain current density in MIS-HEMTs compared with the conventional HEMTs can be observed. MIS-HEMTs exhibited ~ 28 % higher drain current density than that of conventional HEMTs at the same bias of V_D=10 V, V_g=1 V. The increase of output current is due to the improvement in 2-DEG transport characteristics by the passivation effect [116, 120].

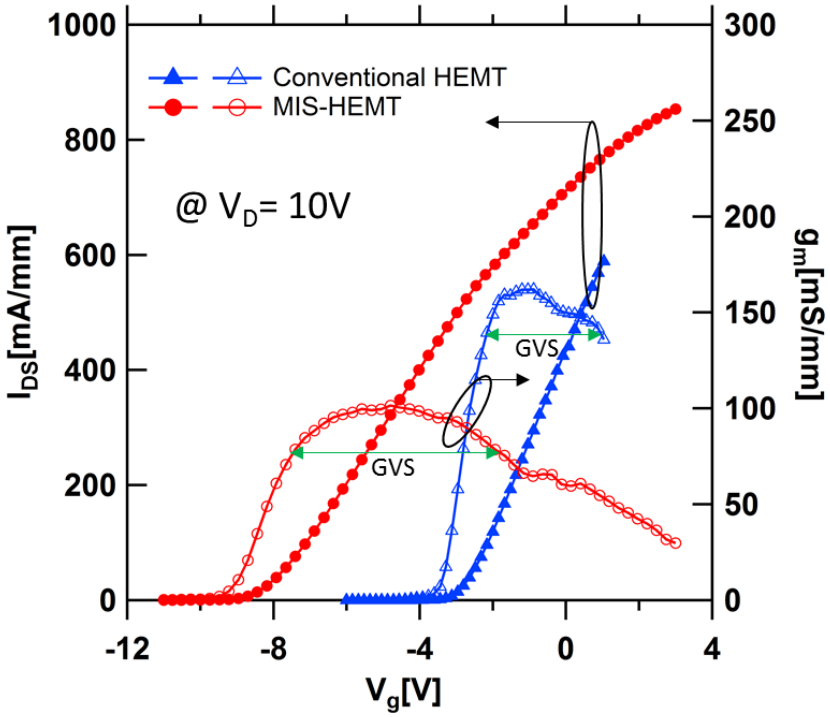


Figure 5.6. Transfer characteristics of conventional HEMTs and MIS-HEMTs on CVD diamond substrate.

In addition, the MIS-HEMTs also exhibited higher g_m linearity, gate voltage swing (GVS) of 5.8 V compared to the 3.2 V for conventional HEMTs. The V_{th} shift (~6 V) in MIS-HEMTs is due to increased gate-to-channel separation by SiN_x dielectric layer.

Schottky *I-V* characteristics for conventional and MIS-Diodes are shown in figure 5.7. The MIS-diode exhibited approximately two orders lower reverse leakage current at ~1.1 x 10^{-8} in comparison to conventional Schottky diode at ~0.94 x 10^{-6}. The reduction in reverse leakage current is due to the increased effective barrier hight of the SiN_x MIS-diode. More importantly, a forward gate current in MIS-diode is around ~ 4 orders lower in magnitude as compared to conv. diode at the same bias condition of + 3V.

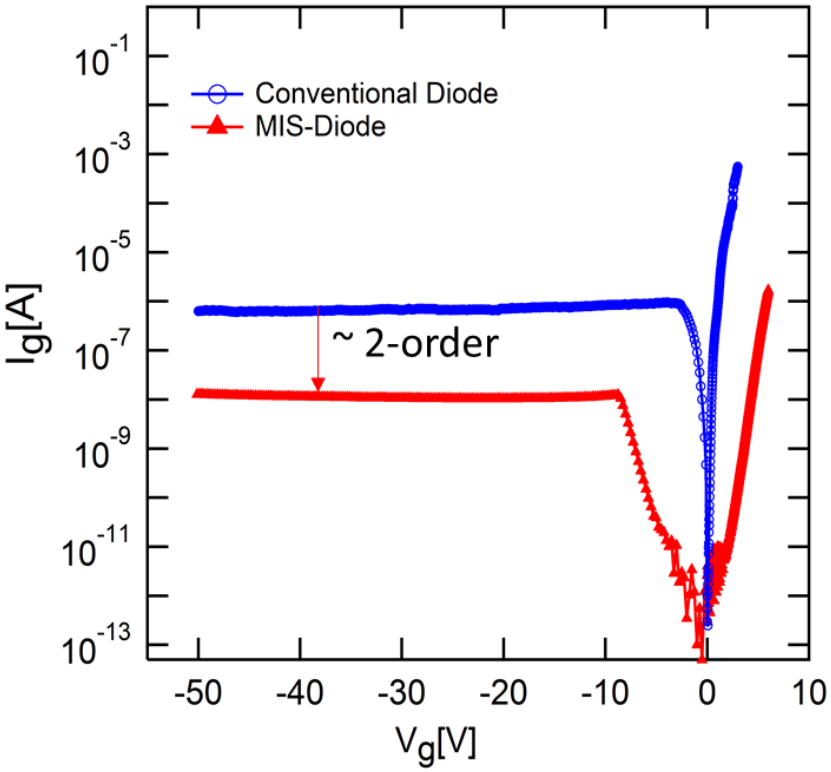


Figure 5.7 Two terminal gate leakage current characteristics of AlGaN/GaN MIS-diode and conv. diode on CVD diamond substrate

The forward bias voltage as high as 6 V was applied in MIS-diode, and the gate leakage current was observed to be ~ 4 x 10^{-2} mA/cm^2. The high forward gate bias voltage allows for higher input voltage swing to be applied at the gate during device operation.

5.4 C-V characteristics

Figure. 5.8 shows typical *C-V* characteristics of the conventional Schottky Diode (conv. Diode) and MIS-Diode. At 1 MHz, the zero-bias capacitance (accumulation region) of 331 nF/cm2 and 155 nF/cm2 for conventional Diode and MIS-Diode were obtained respectively at V_g = 0 V. The V_{th} shift of ~ 6 V was observed in the MIS-Diode, obtained from the C-V characteristics.

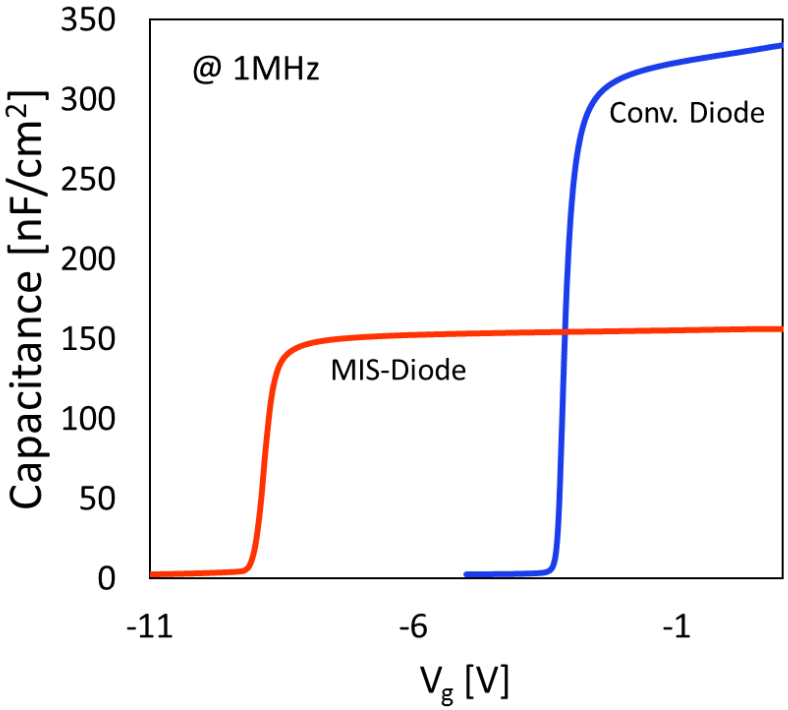


Figure 5.8 *C-V* characteristics of AlGaN/GaN MIS-Diode and conventional Schottky (conv.) Diode at 1 MHz.

The depth versus concentration was estimated from the C-V characteristics by using the following equation [87],

From the depth versus concentration profile (See inset of Fig. 5.9), the thickness of dielectric SiN_x was estimated as ~ 20 nm, which was also verified using the equation;

$$d_{SiN} = \frac{\varepsilon_{SiN}\, d_{2DEG}}{\varepsilon_{AlGaN}} \left(\frac{C_{MIS-Diode}}{C_{Diode}} - 1 \right)$$

where ε_{SiN} and ε_{AlGaN} are the dielectric permittivity of SiN (7.0) and AlGaN layer (9.0), respectively [121]. $C_{MIS\text{-}Diode}$ and C_{Diode} are the capacitance of MIS-Diode and conventional Diode, respectively.

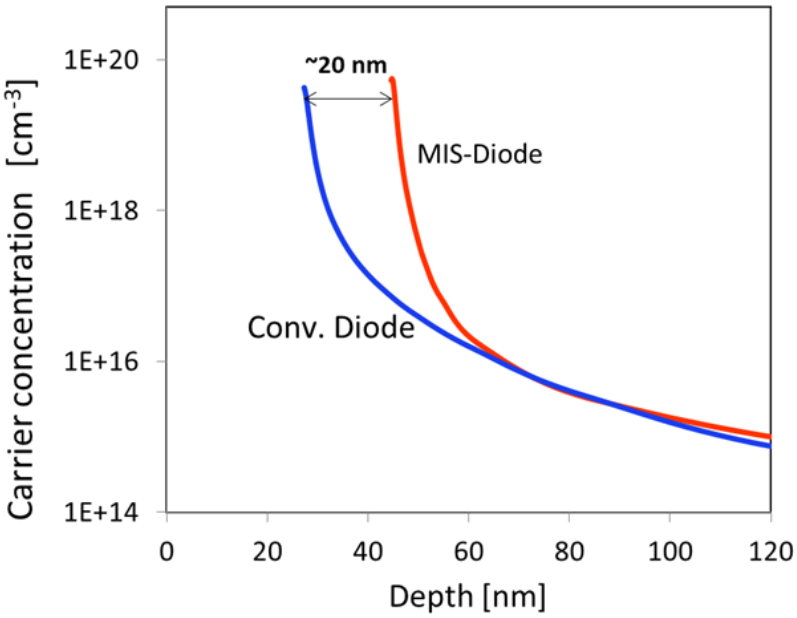


Figure 5.9 Depth - carrier concentration profile of conv. Diode and MIS-Diode estimated from *C-V* measurements.

5.5 G-f characteristics and Trap density estimation

Frequency-dependent conductance measurements of MIS-Diodes and the conventional diode was performed at selected bias conditions ($V_g \leq V_{th}$) to estimate the trap density. The G_p/ω versus ω curves for the MIS-diode and the conventional diode was plotted and are shown in fig. 5.10 (a) and 5.10 (b), respectively. Both MIS-diode and conventional diode show the G_p/ω peak at high frequency. The similar characteristics of G_p/ω exhibited at higher frequencies in both devices indicates common trap behaviour of fast traps. These fast traps are probably the hetero-interface traps of AlGaN/GaN of epitaxy, which is identical in both the devices. In addition, MIS-diodes also exhibit an increase of G_p/ω at lower frequencies which indicates the presence of slow trap at the interface. The additional observation of an increase of G_p/ω in MIS-diode is linked to the dielectric interface of SiNx/GaN.

Assuming a continuum of trap energy levels, the parallel conductance G_p can be expressed as [81];

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln[1 + (\omega\tau_T)^2]$$

where ω is the radial frequency, D_T is te trap density, and τ_T is the trap time constant. In the equation, G_p/ω has a maximum value at $\omega \cong 2/\tau_T$. Hence, D_T can be estimated as $D_T \approx (2.5/q)\,(G_p/\omega)_{max}$ [65].

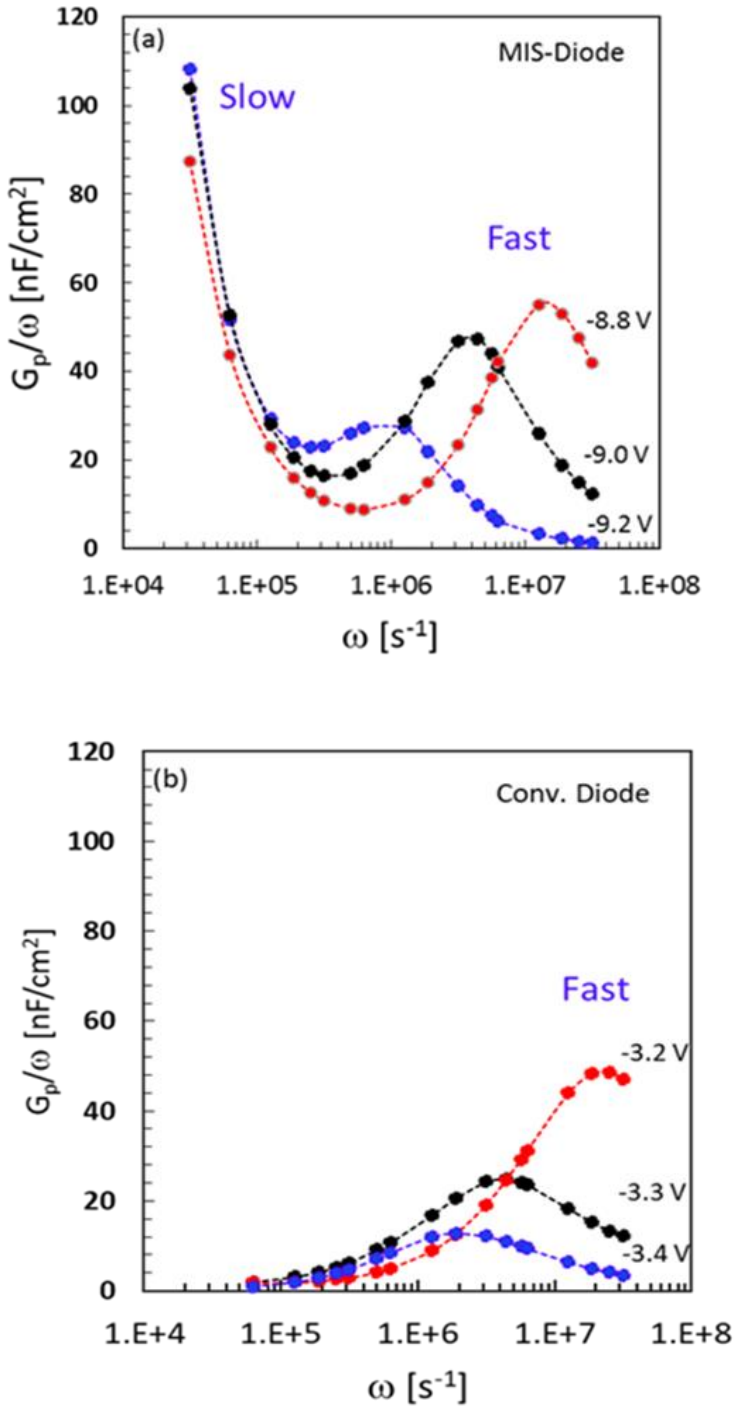


Figure 5.10 Frequency-dependent conductance as a function of radial frequency for AlGaN/GaN (a) MIS-Diode, and (b) conventional Diode on CVD diamond.

From the peak of G_p/ω at a higher frequency, the density of fast traps D_{Tf} in MIS Diode and conventional diode were obtained in the range of (4-8) × 10^{11} cm^{-2} eV^{-1} and (0.7–7.6) × 10^{11} cm^{-2} eV^{-1}, respectively (See Fig. 5.11). The fast trap density is nearly the same in both the devices indicating a common location for these fast traps, which are probably at the AlGaN/GaN hetero-interface. However, the behaviour of slow traps is different and higher in trap density in MIS-diode than in conventional diode, which could be related to the Schottky/dielectric interface. The trap state energy was estimated using the expression;

$$E_T = -kT \ln(\tau_T \sigma_T v_t N_C)$$

where σ_T is the capture cross-section, v_t is the thermal velocity of electrons, T is the temperature, and N_C is the effective density of states at the conduction band in GaN, and E_T is the trap state energy below the conduction band. The trap state energy was estimated for the fast traps of both the diodes. Fig. 5.11 shows the trap state density as a function of trap state energy of MIS-Diode and Conv.Diode.

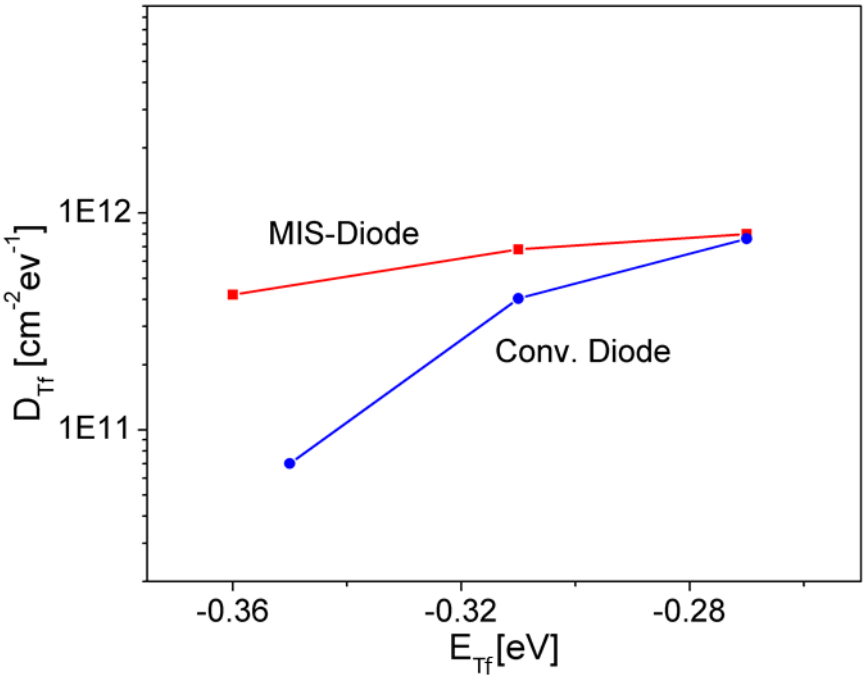


Figure 5.11 Trap state density as a function of trap state energy of MIS-Diode and Conv. Diode.

The time constant of fast traps (τ_{Tf}) was obtained in the range of $\cong$ 0.1–3.6 µs. The estimated fast-trap time constant has been shown in fig. 5.12 for both MIS-Diode and Conv. Diode. An almost similar range of trap energy and trap time constants were identified for fast traps in both conv. Diode and MIS-diode, which signifies these fast traps exist in the same location of AlGaN/GaN hetero-interface, whereas the observation of slow traps only in MIS-diode is linked with the SiN_x/GaN interface.

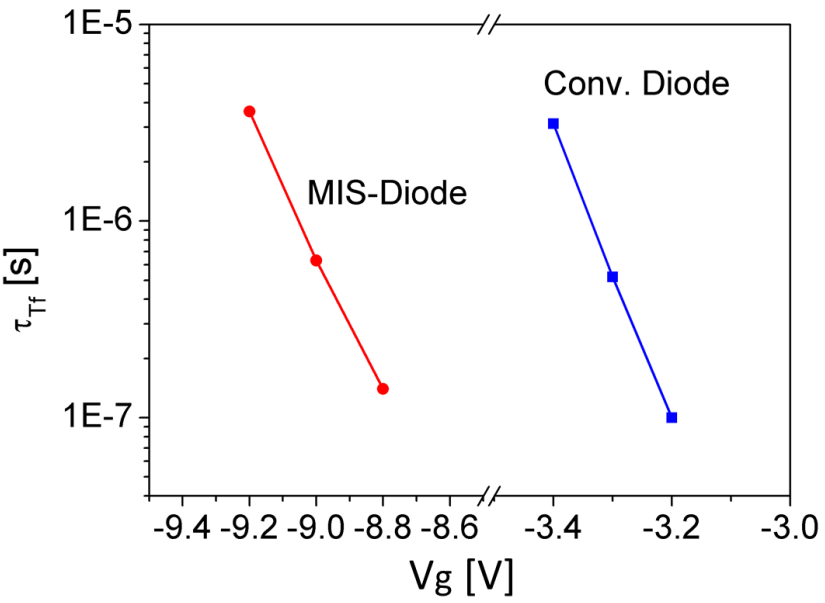


Figure 5.12 Trap state time constant as a function of the gate voltage of MIS-Diode and Conv. Diode.

As the G_p/ω peak was not observed for slow traps in the measured frequency range, D_{Ts} in the MIS-diode was estimated by fitting and simulating the experimental G_p/ω curve of the slow trap region. The simulated trap density (slow traps) was obtained as ~ 6 –11 × 10^{12} cm^{-2} eV^{-1} with $\tau_T \cong$ 6 ms. So, in MIS diodes, two different types of traps, namely fast traps with the time constant $\tau_T \cong$ (0.1-3.6) µs and slow traps with $\tau_T \cong$ 6 ms were identified. The obtained minimum interface trap density of fast traps (4× 10^{11} cm^{-2} eV^{-1}) in our GaN-on-CVD diamond MIS-diode.

5.6 Summary

In conclusion, AlGaN/GaN MIS-HEMTs, MIS diodes and conv. HEMTs, conv. Schottky diodes on-CVD diamond were fabricated and analyzed in terms of the DC performances and interface trap characteristics. MIS-HEMTs exhibited ~ 28 % higher current density, ~ 80% higher g_m linearity and lower reverse gate leakage current by ~ 2-orders of magnitude as compared to the conv. HEMTs. The interface trap behaviour in MIS-Diode and conv. Diode were investigated using parallel conductance techniques. In MIS-Diode, two different types of traps were identified, fast with the time constant $\tau_T \cong$ (0.1–3.6) µs and slow with $\tau_T \cong$ 6 ms whereas, only fast traps were obtained in conventional diodes. The characteristics of fast traps, trap density ($D_{Tf} \cong$ 0.7–8 x 10^{11} cm^{-2} eV^{-1}), trap state energy ($E_T \cong$ 0.28 – 0.36 eV) and trap time constants ($\tau_{Tf} \cong$ 0.1–3.6 µs) are almost similar for both MIS-Diode and conventional Diode which indicates a common location of interface in the heterostructure. These fast traps would be related to AlGaN/GaN hetero-interface which are identical in both the devices. The density of slow trap (D_{Ts}) in MIS-HEMTs was obtained ~ 6–11 x 10^{12} cm^{-2} eV^{-1}. These slow traps in MIS-HEMTs which could be related to the Schottky/dielectric interface surface states. This investigation of interface trap behaviour in device will help to identify and improve the reliability of AlGaN/GaN MISHEMTs-on-CVD diamond.

6 Conclusions and Recommendations for future work

6.1 Conclusions

AlGaN/GaN high-electron-mobility transistors (HEMTs) have been identified as excellent candidates for high power continuous wave (CW) operations such as compact solid-state power amplifier (SSPA) modules which are ideal for civil avionics, communications, industrial, scientific, and medical applications. However, the full potential of GaN HEMT has still not been fully realized due to the inherently low thermal conductivities of the conventional substrates used for GaN epitaxial growth, e.g., Si, Sapphire, and SiC. Low thermal conductive substrate hinders the fast dissipation of lattice heat (self-heat) which is generated in the device during high-power operation of GaN HEMTs. Self-heat further increases the junction temperature and degrades the 2DEG mobility results in degradation of device performance. To minimize the self-heating effect, a superior thermal conductive material such as Diamond has been employed as a substrate to dissipate the generated heat from the active region of the GaN HEMTs.

Typically, the GaN HEMTs-on-CVD diamond is transferred from GaN HEMTs-on-Si. In this process, two key structural changes occur in GaN HEMTs: one is replacing the high thermal conductive substrate, and the other is the removal of trap rich GaN transition layer. These changes

could affect the self-heating and trap behaviour in the GaN HEMTs-on-CVD diamond. This thesis focuses on these two key issues in the GaN/Dia HEMTs.

The quantitative investigation of the effects of self-heating on DC and RF performances was carried out for AlGaN/GaN HEMTs on CVD-Diamond (GaN/Dia) and Si (GaN/Si) substrates. The GaN/Dia HEMTs exhibited ~5.7-times lower rate of I_D reduction than GaN/Si HEMTs. This behaviour was also confirmed by 2D TCAD simulation which showed ~3.9-times lower rate of increase in junction temperature and ~ 4-times lower thermal resistance (R_{th}) in GaN/Dia HEMTs in comparison with GaN/Si HEMTs. The f_T reduction rate was extracted to be ~6.75-times lower in the case of GaN/Dia when compared with GaN/Si HEMTs. Similarly, no significant reduction in f_{max} was observed for GaN/Dia HEMTs while GaN/Si HEMTs exhibited ~49 % reduction. Small signal measurements and equivalent circuit parameter extraction were also done to analyze the variation in the performance of the devices. The lower reduction rate of μ_{eff} and v_{eff} in GaN/Dia (~15%) in comparison to GaN/Si (~50%) has resulted in the improvement of GaN/Dia at high power densities (P_D). These results show that GaN/Dia HEMTs can be operated even at higher V_D as well as at higher P_D which are paramount features for developing compact high power SSPAs for CW application.

The thesis also investigates the hetero-interface trapping mechanism in transition free (trap rich GaN superlattice layer) GaN HEMT-on-CVD diamond. The

conductance-frequency technique was used to estimate hetero-interface trap density and trap state energy. The fast traps (0.16 to 10.01 µs) were identified as the dominating traps in GaN/Dia HEMT structure. The density of fast traps increases with temperature from 6.7×10^{10} cm^{-2} eV^{-1} at 25 °C to 1.4×10^{12} $cm^{-2}eV^{-1}$ at 200 °C. For temperatures of 25 °C to 200 °C, the interface trap state energy (E_T) was obtained to be between 0.27 and 0.51 eV below the conduction band. The observation of increase in D_T with temperature is due to the excitation of additional traps situated deeper in the band-gap. The observation of a lower value of D_{Tmin} for GaN-on-CVD Diamond compared to GaN on Silicon devices is attributed to the removal of the defect-rich GaN transition layer during the substrate transfer process. Finally, the temperature-dependent pulsed I_{DS}-V_{DS} measurements revealed good agreement with the behaviour of D_T with temperature obtained using *G-f* method.

To further improve the device performance such as the linearity of g_m, and the gate-leakage currents in AlGaN/GaN MIS-HEMTs, MIS-Diodes and conventional HEMTs, conventional Schottky Diodes on-CVD diamond were fabricated and analyzed in terms of the DC performances and interface trap characteristics. MISHEMTs exhibited ~ 28 % higher current density, ~ 80% higher g_m linearity and lower reverse gate leakage current by ~ 2-orders of magnitude as compared to the conventional HEMTs. The interface trap behaviour in MIS-Diodes and conventional Diodes were investigated using parallel conductance techniques. In MIS-Diodes, two different types of traps were identified, fast with the time

constant $\tau_T \cong$ (0.1-3.6) µs and slow with $\tau_T \cong$ 6 ms whereas, only fast traps were obtained in conventional diodes. The characteristics of fast traps, trap density ($D_{Tf} \cong$ 0.7-8 x 10^{11} cm^{-2} eV^{-1}), trap state energy ($E_T \cong$ 0.28 – 0.36 eV) and trap time constants ($\tau_{Tf} \cong$ 0.1-3.6 µs) are almost similar for both MIS-Diodes and conventional Diodes which indicates a common location of interface in the heterostructure. These fast traps would be related to AlGaN/GaN hetero-interface which are identical in both the devices. The density of slow trap (D_{Ts}) in MIS-HEMTs was obtained ~ 6-11 x 10^{12} cm^{-2} eV^{-1}. These slow traps in MIS-HEMTs which could be related to the Schottky/dielectric interface surface states.

6.2 Key contributions of this work

The motivation of this thesis to study two key issues in the HEMTs fabricated on transferred GaN-on-Diamond. First, the effect of substrate (CVD diamond) in the self-heating and second, the trapping behaviour in GaN-on-Diamond because the trap rich GaN transition layer was removed during the wafer transfer process from GaN-on-Si to GaN-on-CVd diamond.

In this thesis, for the first time, a detailed investigation of the self-heating effect in GaN-on-Diamond, mainly on RF performance, was carried out. The effect on small-signal equivalent circuit parameters was extracted and analysed with increasing bias conditions which unveiled the variation in RF performances due to self-heating of GaN-on-Diamond

HEMTs. Such work is required for developing the electrical and thermal model of device as well as improving the operating limit of GaN HEMTs for next-generation high power DC and RF applications.

In addition to the self-heating effect, interface traps behaviour in GaN HEMTs-on-CVD diamond was also investigated for the first time. The conductance-frequency technique was used to estimate hetero-interface trap density and trap state energy. Deeper trap at the interface was also identified through elevated temperature measurements. Results were compared with identical GaN HEMTs-on-Si and benchmarked with reported GaN HEMTs on various substrates like Sapphire, Si and SiC.

For the first time, AlGaN/GaN metal-insulator-semiconductor (MIS) HEMTs on CVD-diamond was fabricated and described the improved DC characteristics. The critical issue in MIS-HEMTs is the dielectric interface trap behaviour. The detailed investigation of dielectric interface and hetero-interface is carried out in AlGaN/GaN MISHEMTs on CVD-diamond and compared with the conventional Schottky AlGaN/GaN HEMTs on CVD-diamond. The finding of slow and fast type of traps in MISHEMTs on the contrary to only fast traps in conventional HEMTs indicated the source of traps. Such a study of interface trap behaviour in the device will help to identify and improve the reliability of AlGaN/GaN HEMTs and MISHEMTs-on-CVD diamond.

6.3 Recommendations for Future Work

Although the GaN-on-Diamond has exhibited improved device performance at the high-power density in CW operation by minimizing the self-heating and reducing the junction temperature, there is still much scope for improvement in the device performance. Two key areas can be focused further to improve the device performance in GaN HEMTs-on-CVD diamond; one is the device topology, and the second is the GaN-on-CVD diamond HEMT epitaxy structure.

From the device topology perspective, the exhibited maximum dissipation power density in GaN/Dia in this work can be further increased by reducing the lateral electric field intensity in the gate-drain region. This can be achieved by the incorporation of field plate structure in device topology. The gate field plate or source filed plate method can be used to suppress the peak of the lateral electric field and also the junction temperature of GaN/Dia HEMTs. However, the field plate structure also introduces gate capacitance which needs to be optimized for improved device DC and RF performances in GaN HEMTs-on-CVD diamond. More study is required to understand the behaviour of 2DEG transport properties and their effect on device performances with field plate structure in GaN HEMTs-on-CVD diamond.

The quality of epitaxy structure in HEMT affects the trap behaviour in the device and becomes more significant during high power density

operation. In this thesis, AlGaN/GaN hetero-interface trap in GaN-on-CVD diamond has been studied, but there is still room to investigate the trapping mechanism in the GaN buffer layer. The investigation of buffer traps and its effect on dynamic ON-resistance (dyn-$R_{ds[ON]}$) are needed to be studied in AlGaN/GaN HEMTs on CVD-diamond at large drain-quiescent biases stress condition for high voltage switching application.

Author's Publication

List of Publications

Journal papers:

[1] **K. Ranjan**, S. Arulkumaran, and G. I. Ng, "Investigations of temperature-dependent interface traps in AlGaN/GaN HEMT on CVD-diamond", *Applied Physics Express, 12,10,* 2019.

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