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**POWER MANAGEMENT IN ENERGY
HARVESTING**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

2019

POWER MANAGEMENT IN ENERGY HARVESTING

LAU WEE YEE WENDY

**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2019

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The contributions of the co-authors are as follows:

- A/Prof Siek provided the initial project scope.
- I prepared the manuscript.
- I designed the circuits, performed all simulations and analysed data.

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- I designed the circuits, performed all simulations and conducted data analysis.

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The contributions of the co-authors are as follows:

- Dr Ho provided project direction and guidance on machine learning.
- Dr Ho and I co-edited the manuscript.
- I designed the circuit, prepared the dataset and performed simulations on various optimization algorithms.

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SUMMARY

A dual-path wide-power-range rectifier for RF energy harvesting is presented in this thesis. The proposed idea focuses on maximizing efficiency in harvesting energy from the surrounding environment and designated energy source to support wide variety of applications in low power devices' wireless charging. The harvester consists of a low-power rectifier, a high-power rectifier and a voltage-aware block. In the low-power rectifier, novel DC-boosted gate bias technique is proposed to enhance power conversion efficiency (PCE) by improving forward peak current, reducing diode forward voltage drop and suppressing reverse leakage current. A novel internal body-biasing technique is proposed in the high-power rectifier to regulate the transistors' threshold voltage (V_{th}) for optimal efficiency. A voltage-aware block, which consists of a voltage detector, a switch and an adjustable-offset comparator, has been incorporated into the high-power rectification path to minimize overall power consumption.

The proposed circuit is fabricated in 65 nm 6M/1P standard CMOS technology. Peak PCE of 70.4% is measured on the low-power rectifier with -5.5 dBm input power at 2.45 GHz when driving a 15 k Ω load. For high-power rectifier, peak PCE of 56.6% is measured with 1.3 dBm input power at 2.45 GHz when driving a 15 k Ω load. The chip has PCE higher than 20% over a 19.8 dB of extended input power range from -13.5 dBm to 6.3 dBm.

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LIST OF ABBREVIATIONS

AC	Alternating current
ADE	Analog design environment
AI	Artificial intelligence
ANN	Artificial neural network
AR	Augmented reality
AVDD	Analog circuit DC supply
BFGS	Broyden-Fletcher-Glodfarb-Shanno algorithm
CCCR	Complementary cross-coupled rectifier
CG	Common gate
CMOS	Complementary metal-oxide-semiconductor
COB	Chip-on-board
DC	Direct current
DNN	Deep neural network
DUT	Device under test
EDA	Electronic design automation
ELU	Exponential linear unit
ESR	Equivalent series resistance
ET	Electrical test
FOM	Figure-of-merit
GCPW	Grounded coplanar waveguide
GIDL	Gate-induced drain leakage

GPU	Graphics processing unit
HVTP	High- V_{th} PMOS
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
ISM	Industrial, scientific and medical
IVC	Internal V_{th} -cancellation circuit
LVTP	Low- V_{th} PMOS
LVTN	Low- V_{th} NMOS
MATLAB	Matrix laboratory
MLP	Multiple layer perception
MN	Matching network
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPPT	Maximum power point tracker
NMOS	N-type metal-oxide-semiconductor
PCB	Printed circuit board
PCE	Power conversion efficiency
PEX	Parasitic extraction
PMOS	P-type metal-oxide-semiconductor
PMU	Power management unit
RCC	Reverse current control
RF	Radio frequency
SPICE	Simulation program with integrated circuit emphasis
SR latch	Set/reset latch

TEH	Thermoelectric energy harvester
TEG	Thermoelectric generator
UK	United Kingdom
USA	United States of America
V_{DS}	Drain-to-source voltage
V_{SG}	Source-to-gate voltage
V_{th}	Threshold voltage
w/i	With
w/o	Without
Wi-Fi	Trademark phrase for IEEE 802.11x
W/L	Transistor width/length
WLAN	Wireless local area network
WPT	Wireless power transfer
WSN	Wireless sensor network
6M/1P	6 metal layers and 1 polysilicon layer

CHAPTER 1 INTRODUCTION

In recent years, industry-leading manufacturers, researchers, network providers, service providers and consumers have shown great interests on Internet of Things (IoT) [1]. IoT is the network of physical objects with embedded technologies and network connectivity that enable these objects to collect information, transmit data and receive data. Areas of application for IoT encompass home automation, smart cities, automotive, healthcare, wearable, agriculture, and smart grid.

Fig. 1.1. Key emerging technologies' adoption rate in the coming decade [2].

The advances in hardware (transistor reduction), processing power of graphics processing unit (GPU), proliferation of data with increased use of IoT, and requirement for speed and secure peer-to-peer transaction will drive the advances

and adoption of blockchain, artificial intelligence (AI) and augmented reality (AR). It is predicted that around 125 billion devices will be connected to internet by year 2030 from 11 billion in year 2018 [2]. According to [3], the global IoT market is predicted to grow till US\$ 457 billion by year 2020. The global IoT market will be dominated by smart cities (26%), industrial IoT (24%) and connected health (20%).

Fig. 1.2. Forecast of IoT market growth by year 2020, and market share according to sub-sector with smart cities, industrial IoT and connected health dominating the global IoT market [3].

1.1 Ambient Sources Energy Harvesting

One of the vital elements in IoT is the wireless sensor network (WSN), which is formed by network of sensor nodes connected wirelessly to monitor and record physical, environment, chemical or biometric conditions [4], [5]. Fig. 1.3 illustrates typical structure of a WSN. Sensor node is estimated to consume around $10\ \mu\text{W}$ to $100\ \mu\text{W}$ of average power, depending on the sensor type and application [6]-[8].

Fig. 1.3. Structural view of typical wireless sensor network.

Despite extensive research on minimizing power consumption of WSN and sensor nodes, one major constraint on sensor network is the longevity of sensor node [12]. Sensor nodes are usually powered by batteries and deployed in large

volume. Sensor node applications are restricted due to cost and feasibility considerations because of the fixed stored energy and the constant need for recharging or replacement of battery [13], [14]. Energy harvesting is able to overcome battery limitations and to support emergence of IoT [13], [15], [16].

Fig. 1.4. Architecture of wireless sensor platform with energy harvesting system [25].

Energy harvesting is the process of capturing readily available ambient energy and converting it into usable electrical energy. Advantages of energy harvesting include self-sustainability, environmental friendliness, portability, cost saving, safety, and inaccessible and remote sites deployment [17]. Fig. 1.4 shows an energy harvesting system within wireless sensor platform, which consists of ambient energy source, energy harvesting management unit to convert the ambient energy to electrical energy, and energy storage to store converted energy and supply power to load. Energy sources include solar [18]-[20], vibration [21],

thermal [22], wind, hydro, radio frequency (RF) [23] and kinetic energy [24].

Table 1.1 summarizes the advantages and disadvantages of various ambient energy sources for harvesters.

Table 1.1. Summary of comparisons between various energy sources.

Energy Source	Pros and Cons	References
Solar	<ul style="list-style-type: none"> Solar energy has high power density: <ul style="list-style-type: none"> 100 mW/cm² (outdoor); 100 μW/cm² (indoor) Solar panel has low efficiency which resulted in large panel size required to collect substantial amount of solar energy <ul style="list-style-type: none"> Amorphous type panel (42 x 45 mm²): maximum efficiency 4.57 % under 1000 Wm⁻² solar intensity Polycrystalline type panel (45 x 76 mm²): maximum efficiency 11.84 % under 1000 Wm⁻² solar intensity 	[18]-[20], [25], [94]-[98]
Thermal	<ul style="list-style-type: none"> Thermoelectric generator (TEG) produces power density: <ul style="list-style-type: none"> 20-60 μW/cm² (from human body); 1-10 mW/cm² (industrial) TEG are lightweight and can conform to 	[22], [25], [27], [99]-[100]

	<p>human body and clothing</p> <ul style="list-style-type: none"> Requires large amount of TEG to generate substantial amount of power. Example of commercial TEGs: <ul style="list-style-type: none"> Micropelt TPG751 (15 x 10 x 9.3 mm³): 110 mV/K Eureca TEG1-40 (40 x 40 x 3.6 mm³): 82 mV/K Eureca TEC2L-15 (15 x 15 x 4.4 mm³): 12.5 mV/K Continuous temperature difference is required for continuous energy generation 	
Vibration/ motion	<ul style="list-style-type: none"> Vibrational micro-generator power density: <ul style="list-style-type: none"> 4 $\mu\text{W}/\text{cm}^3$ (from human motion); 800 $\mu\text{W}/\text{cm}^3$ (from machine vibration) Easy application Continuous vibration/motion is needed for continuous energy generation 	[21], [24], [26], [101]
RF	<ul style="list-style-type: none"> RF energy has low power density: <ul style="list-style-type: none"> 0.1 $\mu\text{W}/\text{cm}^2$ (GSM 900 MHz); 0.001 $\mu\text{W}/\text{cm}^2$ (Wi-Fi) Easily available due to increasing amount 	[23], [25], [77]

	of radio transmitters <ul style="list-style-type: none"> • Application in healthcare and biomedical electronics system • Provide option of targeted RF signal for powering remote applications 	
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Solar power is the use of photovoltaic cell to convert light energy to electrical power. It is commonly deployed due to its high power density. Besides light intensity, the amount of power extracted relies on the size, material and orientation of solar panel which results in large panel size required for collection of substantial amount of solar energy due to its low efficiency of 10-40% [25], [94]-[98]. A single stage DC/DC converter performing as maximum power point tracker and output voltage regulator has been proposed in [18]. Under same solar intensity of 1000 Wm^{-2} , amorphous type solar panel of size $(42 \times 45) \text{ mm}^2$ has maximum efficiency of 4.57 % while polycrystalline type solar panel of size $(45 \times 76) \text{ mm}^2$ has maximum efficiency of 11.84%. Discrete analog integrated circuit components are used to materialize an ultra-low-power maximum power point tracking circuitry. The solar energy harvester is reported to have an efficiency of 87 % to 93 %. The work in [20] proposes storing charges to supercapacitors through feed-forward, phase frequency modulated converter. The solar voltage optimal power point is tracked through open-circuit voltage method for its simplicity at the expense of accuracy, and the harvester is reported to achieve efficiency of more than 89 %. In [97], a buck-boost converter controlled by fuzzy

logic system which generates variable duty cycle according to solar panel voltage is proposed.

Piezoelectric energy is generated through materials response to mechanical stress. The power density of piezoelectric varies according to the intensity of motion. This approach has low conversion efficiency because it is able to generate large output voltage but extremely small current [26]. In [21], automobiles vibration energy harvesting is proposed. The prototype creates a piezoelectric transducer formed by piezoelectric element QP21B with sizing $(41.4 \times 17 \times 0.76) \text{ mm}^3$ on cantilever beam of sizing $(300 \times 25 \times 2) \text{ mm}^3$. Depending on road conditions, average energy of $13.3 \mu\text{W}$ can be harvested over a 10 km distance.

Thermal energy harvesting involves conversion of temperature change to power through thermoelectric device. Energy is generated as long as temperature gradient is maintained. TEG has the benefit of able to work in harsh environment, no noise and no vibration. However, it usually requires larger volume to generate substantial amount of power and the cost of thermoelectric element is much more than batteries [25], [27]. In wearable electronic applications, TEGs have limited output voltage of 50 mV due to 1 – 2 K difference between ambience and body temperature [22]. According to [27], the thermoelectric energy harvesters (TEHs), regardless of size and shape, generate power in the range of $200 \mu\text{W}/\text{cm}^3$ to $10 \mu\text{W}/\text{cm}^3$ over ambient temperature range of -5°C to 25°C when worn on different body parts. A battery-less TEH which can operate from 35 mV is

proposed in [22]. A temporary storage block is used to store excess energy harvested and acts as buffer for interface circuit. The work is reported to have efficiency of 58% with 1.8 V regulated output. A TEH using micropelt TGP-751 for aircraft low-power sensors is proposed in [100]. The TEG-pad used has size of 2.4 – 2.9 mm. The TEH is reported to achieve maximum efficiency of 92 % with maximum 5.5 mW power stored in supercapacitor.

1.2 Wireless Power Transfer

In the 19th century, Heinrich Hertz and Nikola Tesla first came up with the concept of propagating electromagnetic wave in free space and detecting it at some distant away [28]. The idea was put on halt due to non-existence of device which could provide the required energy at very short wavelengths.

Wireless power transfer (WPT) can be attained through three technologies, as shown in Fig. 1.5, which can be classified into two methods [29]:

- i. Near-field technique
 - a. Inductive coupling
 - b. Resonant inductive coupling
 - c. Resonant capacitive coupling
- ii. Far-field technique
 - a. Microwave/ radio wave power transmission
 - b. Laser

Fig. 1.5. Wireless power transfer technologies and techniques [29].

Inductive coupling occurs when change in magnetic field of primary conductor induces voltage on the secondary conductor [31]. The main disadvantage of this technique is the short operation range. Capacitive coupling is the transfer of energy between two metallic plates (forming capacitors), induced by high-frequency electric field. Efficiency of capacitive coupling is limited by the distance between two conductive plates. For inductive coupling, the efficiency degrades when distance between the two conductors increases. Magnetic resonance coupling is the phenomenon when both the primary and secondary coils resonant at same frequency, resulting in more power being transferred over

larger distance [32]. Microwave power transmission is the transmission of power through directional radio wave [33]. The transmission-end consists of converter to convert energy to microwave and transmit through antenna while a rectenna is used at the receiving-end to convert the microwave back to energy [34]. Table 1.2 summarizes the comparisons between different types of wireless power transfer techniques.

Table 1.2. Comparisons between different wireless power transfer techniques, in terms of received power, operating distance, operating frequency, convenience, efficiency and biological impact [30].

	Inductive coupling	Magnetic resonance coupling	Microwave power transmission	Laser	Capacitive coupling
Received power	Few W to hundreds of kW	Hundreds of W	$\leq$ tens of kW	Expected MW	$\leq$ 1 W
Operating distance	Few cm	Few m	Tens of km	Tens of km	Few mm
Operating frequency	Few kHz to tens of kHz	Few MHz	$\leq$ 300 GHz	$\geq$ 1 THz	Up to MHz
Convenience	Acceptable	High	High	High	Acceptable
Efficiency	Highest	High	Medium	Medium	Low
Biological impact	Minor	Medium	Significant	Significant	Minor

1.3 Project Motivation

Fig. 1.6. Example of RF energy sources.

Fig. 1.6 shows the common RF energy sources, such as Wi-Fi networks, mobile networks, TV/radio broadcast stations. RF energy has the following benefits as compared to other energy sources from the environment:

- i. Readily obtainable from the ample amount of radio transmitters (mobile phone base stations, mobile handsets, wireless local area network, and TV/radio broadcasting)
- ii. Accessible wirelessly
- iii. Immune to natural environment effects
- iv. Mobility
- v. Power is controllable
- vi. Relatively low cost.

RF energy harvesting, which is a form of far-field wireless power transfer, is the process of capturing radiated electromagnetic wave from ambient with antenna and converting it into usable DC voltage. Fig. 1.7 presents block diagram of an RF energy harvester. RF signals are electromagnetic waves with frequency range from 3 kHz to 300 GHz. 900 MHz and 2.4 GHz are the two most commonly exploited frequency bands for RF energy harvesting [16], [39]-[43]. Its areas of application include wireless sensor network [44], wireless body network [45], and wireless charger network [46]. Example of feasible applications for RF energy harvester include wireless sensor node which has an estimated power consumption of 1 – 100 μW [102], temperature sensor which consumes 3.75 pW – 0.15 μW [103]-[104], hearing aid which consumes 38 μW [105], and heart rate variability detector which consumes 3 μW [106].

Fig. 1.7. Block diagram of generic RF energy harvester, comprising antenna, matching network, RF-DC converter with DC-DC converter and/or energy storage unit and/or voltage regulator.

Smart building [47]

Wireless sensor node [48]

Body sensor network [50]

Noise quality and air pollutant sensor [49]

Fig. 1.8. Examples of potential applications of RF energy harvester.

Despite the numerous advantages of RF energy source, RF energy harvesting continues to be a challenge due to low power density, limited maximum transmit power in compliance with RF communication standards and spurious emissions, and degradation in sensitivity of energy harvester circuit at low power.

The main objective of this research is to propose an RF energy harvesting circuit which operates over wide input power range. The targeted operating frequency for

this energy harvester is 2.45 GHz, which is the frequency band for industrial, scientific and medical (ISM) and IEEE 802.11/Wi-Fi. This work will focus on the design of high efficiency RF-DC rectifier through novel circuit design and methodology.

1.4 Organization of the Thesis

This thesis is organized and presented as follows:

Chapter 2 provides an overview of the various types of rectifier. It then proceeds to discuss the design and performance of some of the state-of-the-art rectifiers. Rectifier design optimization methodologies are discussed.

Chapter 3 elaborates the design of proposed dual-path RF energy harvester. The circuit simulation results are presented. It then detailed the automated design optimization methodology using deep neural network.

Chapter 4 discusses on the robustness of proposed rectifiers against variations in process, temperature and frequency.

Chapter 5 demonstrates the fabricated chip performance under various input power. Silicon measurement data are collected and compared to circuit simulation results.

Chapter 6 concludes the thesis with summary of key contribution of this research project. Future works are proposed for system-level automated design optimization using artificial neural network, automated rectification path selection and chip preparation for wire-bonding or packaging.

CHAPTER 2 LITERATURE REVIEW

2.1 Rectifier Design

Integrated rectifier in standard CMOS process has been proposed by many works, for both near-field and far-field power transfer systems. The following popular rectifier architectures are reviewed in this chapter:

- i. Diode-type Rectifier
- ii. Diode-connected MOSFET Rectifier
- iii. V_{th} -cancellation Rectifier
- iv. Self- V_{th} -cancellation Rectifier
- v. Bootstrapped CMOS Rectifier
- vi. Boosted-gate CMOS Rectifier
- vii. Active Diode Rectifier
- viii. Complementary Cross-coupled Rectifier.

The feasibility of these rectifiers to be employed for ultra-high frequency far-field system will be discussed, according to their operating frequency, input power or voltage range and maximum power conversion efficiency (PCE).

2.1.1 Diode-type Rectifier

Fig. 2.1 shows a conventional diode-type rectifier. During the negative half cycle when V_{in} is negative, capacitor C_c is charged through diode $D2$. During the positive half cycle when V_{in} is positive, C_c discharges to output capacitor (C_L)

through diode $D1$. Rectifier output voltage V_{OUT} is defined as $[2 \times (v_{in,p} - V_D)]$, where $v_{in,p}$ is the RF signal amplitude and V_D is the diode forward voltage drop. The forward current is large while reverse leakage current is negligible. The rectifier is commonly used in high voltage application but the large 0.7 V to 1.0 V forward voltage drop renders diode not suitable for low voltage system.

Fig. 2.1. Schematic of diode-type rectifier [51].

Schottky diode, with its fast switching speed and negligible forward voltage drop, is an attractive alternative to enhance the rectifier efficiency [52], [53]. However, Schottky diode is not supported in all standard CMOS process. The special process requirement for Schottky diode will introduce higher production cost which restricts its implementation in low-cost but highly integrated applications.

2.1.2 Diode-Connected MOSFET Rectifier

Fig. 2.2. Schematic of diode-connected MOSFET rectifier [54].

Fig. 2.2 shows a diode-connected MOSFET rectifier [54]. The diode-connected MOSFET rectifier can be implemented with NMOS-only, PMOS-only or CMOS transistors. Diode-connected MOSFET reduces the forward voltage drop with rectifier output voltage V_{out} being defined as $[2 \times (v_{in,p} - V_{th})]$, where V_{th} is the MOSFET threshold voltage. The forward current is usually sufficiently large such that reverse leakage current can be ignored. However, the rectifier efficiency is still affected by V_{th} drop. Zero-threshold MOSFET can eliminate threshold voltage drop but it has large reverse leakage current, which cause severe degradation in rectifier PCE.

2.1.3 V_{th} -Cancellation Rectifier

Fig. 2.3 shows a V_{th} -cancellation rectifier [55] where the gate of MOSFET is biased to cancel effect of threshold voltage. The gate bias voltage can be

generated internally or supplied externally. For PMOS, gate is biased with a negative voltage such that it can turn on during positive cycle when $v_{in,p}$ is smaller than $|V_{th}|$. For NMOS, gate is biased with a positive voltage such that it can turn on during negative cycle when $|v_{in,p}|$ is smaller than V_{th} . Rectifier output voltage V_{out} is ideally $(2 \times v_{in,p})$.

Fig. 2.3. Schematic of V_{th} -cancellation rectifier [55].

Fig. 2.4 shows a rectifier design with internal V_{th} -cancellation circuit (IVC) [56]. The threshold voltage compensation voltage is generated internally using diode-connected transistors which replicate the threshold voltage of rectification transistor. Capacitors C_{pb} and C_{pn} are used for maintaining the gate bias voltage. The IVC is able to track process and temperature variation through the delta between rectification transistor and its gate bias transistor. Ferroelectric capacitor is used as input coupling capacitor for its high permittivity characteristic, which resulting in smaller area and input parasitic capacitor C_{Pr} .

Fig. 2.4. Rectifier with internal V_{th} -cancellation circuit [56].

However, the fixed gate-drain voltage in V_{th} -cancellation rectifiers will cause transistor not able to turn off completely during reverse bias, resulting in substantial reverse leakage current. Moreover, internal circuitry used to generate the gate bias voltage will consume some power, resulting in slight degradation in rectifier PCE.

2.1.4 Self- V_{th} -Cancellation Rectifier

Fig. 2.5 shows a self- V_{th} -cancellation rectifier [57]. It has similar operating principle as the V_{th} -cancellation rectifier but the gate of PMOS is connected to ground and gate of NMOS is connected to rectifier output. The threshold voltage effect of transistor is cancelled off by amount equivalent to rectifier output voltage, and no additional circuitry is required. The rectifier yields high PCE at low RF input power. However, both transistors will turn on concurrently when

rectifier output voltage is larger than $|V_{th}|$ of both PMOS and NMOS, which resulted in large leakage current.

Fig. 2.5. Schematic of self- V_{th} -cancellation rectifier [57].

2.1.5 Bootstrapped CMOS Rectifier

Fig. 2.6. Schematic of bootstrapped CMOS rectifier [58].

Fig. 2.6 shows a bootstrapped CMOS rectifier [58], [59]. During positive cycle, when V_{in} is larger than rectifier output voltage V_{OUT} by at least a V_{th} , auxiliary diode-connected transistor M_5 will turn on. M_5 turns on and charges output capacitor C_L . Concurrently, bootstrap capacitor C_{BI} is being charged through M_7 and V_{CBI} is $|V_{th}|$ lower than V_{OUT} . Hence, V_{OUT} is defined as $[2 \times (v_{in,p} - (|V_{th,3}| - |V_{th,7}|))]$. However, the rectifier requires very large C_B and is slower as compared to other topologies due to its need for frequent charging and discharging of capacitors.

2.1.6 Boosted-gate CMOS Rectifier

Fig. 2.7. Schematic of boosted-gate CMOS rectifier [60].

Fig. 2.7 shows a boosted-gate CMOS rectifier [60]. It has similar operating principle as the V_{th} -cancellation rectifier but the gate of transistor is driven by

auxiliary floating rectifier. As compared to loaded rectifier, floating rectifier is able to produce larger output voltage. This characteristic of floating rectifier is used to supply bias voltage to the gate of transistors in main rectifier. Hence, each main rectifier requires eight additional transistors for the bias generation circuitry. Although the floating rectifiers consume very low power, careful design consideration is required to prevent over-boosting the gate voltage of transistors in main rectifier, which will cause large reverse leakage current and degradation in rectifier PCE.

2.1.7 Active Diode Rectifier

Fig. 2.8. Schematic of active diode rectifier [61].

Fig. 2.8 shows an active diode rectifier [61], [62]. Active diode is a comparator-controlled transistor that works almost like an ideal switch. The comparator will sense the difference in drain-source voltage of transistor and bias the gate

accordingly to turn on or off the transistor. This design is reported to provide higher PCE as compared to other passive topologies. However, during the starting point of rectification when no output voltage is available, the comparator might not function. This limits its application to circuits with auxiliary power source or a second parallel rectifier with lower efficiency for bootstrap. Another major drawback of this rectifier is the inefficient power conversion at high frequency because active circuit draws more current to drive the switch due to larger parasitic effects at high frequency. The propagation delay of comparator and gate-drive buffer will shorten the current conduction time during turn on and delay the turn off causing reverse current to flow from rectifier output, as shown in Fig. 2.9.

Fig. 2.9. Transient simulation showing reverse current issue in active diode M_{N1} and M_{N2} due to delay in transistor turn-off [61].

The different types of delay compensated comparator used in active diode can be categorized as follow:

A. Comparator with Fixed Offset

Fig. 2.10. Unbalanced-biased comparator [63]. V_{OUT} is the rectifier output voltage.

Fig. 2.10 shows an unbalanced-biased comparator for active diode rectifier [63]. The transition time for rectifier input to increase from $-1V$ to $0V$ can be 10-20% larger than comparator delay time to accommodate process variation to reduce reverse leakage current. $CGA1$ and $CGA2$ form push-pull stage at node A. I_{s1} is set larger than I_{s2} such that

$$\Delta V = \frac{\sqrt{I_{s1}} - \sqrt{I_{s2}}}{\sqrt{\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)}} \quad (2.1)$$

For proper operation, the rectifier output needs to be larger than the comparator minimum operating voltage requirement. The smallest input voltage amplitude which the rectifier is able to process:

$$|V_{in,min}| = \max\{(\max(|V_{thp}|, V_{thn}) + 2V_{ov}), (|V_{dsp}| + V_{dsn})\} \quad (2.2)$$

where V_{ov} is the overdrive voltage, and $|V_{dsp}|$ and V_{dsn} are the drain-to-source voltage of PMOS and NMOS rectification transistor, respectively.

Fig. 2.11. Cross-coupled latched comparator [64]. V_{OUT} is the rectifier output voltage.

Fig. 2.11 shows a rectifier with cross-coupled latched comparator [64]. The comparator comprises a main comparator and a speed-up comparator. M_{P3} in the main comparator creates an unbalanced sizing between M_{P2} branch and M_{P1} , for a faster pull-up response to reduce reverse conduction time. When rectifier input

voltage is higher than output voltage, M_{P5} will turn on and speed-up comparator will tie nodeX to high, resulting in a strong turn on for M_{N2} . This will improve the forward conduction time of rectifier. When input voltage is lower than output voltage, M_{N4} will turn on and nodeX will be tied to ground. This will result in a faster turn on for M_{P2} and reduce the reverse conduction time of rectifier.

For comparators with fixed offset, the switch transistors are turned off earlier to minimize reverse leakage current. They usually have slower response in turning on the switch during forward conduction period.

B. Comparator with dynamic offset for reverse conduction

Comparator with reverse current control (RCC) for active rectifier is shown in Fig. 2.12 [65]. M_4 needs to be supplied by V_{in+} instead of V_{OUT} because:

- i. The rectifier will not be able to startup if M_4 is connected to V_{OUT} because $V_{OUT} = 0$ V when idle
- ii. Comparator will start to operate when $V_{in+} > |V_{thp}| + V_{thn}$. It does not consume current when $V_{in+} \leq |V_{thp}| + V_{thn}$ or $2|V_{thp}|$. Comparator operates on dynamic bias without the need for startup circuit.

M_5 acts a resistor to introduce different time constants on V_{AP} and V_{AN} , resulting in dead-time between the rise-time and fall-time of the signal pair. This will minimize the shoot-through current during signal transitions. When M_{N1} turns ON, M_9 will turn on and more current is drawn by M_4 . Since $\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4}$, M_3 will draw more current, resulting in faster rise-time for V_{AP} and V_{AN} . Hence, M_{N1}

Fig. 2.12. Comparator with reverse current control (RCC) [65]. V_{OUT} is the rectifier output voltage.

Fig. 2.13. Delay time compensated comparator with switched-offset [61].

V_{GN1} and V_{GN2} are the gate bias for NMOS rectification transistor.

Fig. 2.13 shows the delay-time compensated comparator used in Fig. 2.8 [61].

When $V_{in1} < 0$ V, M_1 sinks more current than M_2 . This increases the current sourced by M_5 , which is being mirrored to M_6 . V_{OUT} and V_{GN1} will be pulled high and M_{N1} turns ON. V_{SW} will change state from high to low, turning ON M_{I1} and M_{I2} . The offset voltage introduced by M_9 and M_{I0} is expressed as

$$V_{OS} = \sqrt{\frac{2I_{M10}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}} - \sqrt{\frac{2I_{M7}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}} = (\sqrt{n} - 1) \sqrt{\frac{2I_{M7}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}} \quad (2.3)$$

where $I_{M10} = nI_{M7}$. With I_{M9} and I_{M10} sourcing M_1 and M_4 respectively, V_{OUT} is pulled low faster. M_{N1} is turned OFF earlier before $V_{in1} > 0$ V, eliminate reverse

current issue. *SR* latch is added between comparator output and V_{SW} to prevent multiple-pulsing problem caused by dynamic offset operation. Comparator operates on dynamic bias to reduce power consumption.

For comparators with RCC, the dynamic offset will be off when the power switch is turned off. This offset is susceptible to process variations [61], and might suffer from multiple-pulsing issue.

C. Comparator with dynamic offset for both forward and reverse conductions

Fig. 2.14 shows an ON-OFF response compensated comparator. When $V_{in+} > V_{out}$, M_1 is sourcing more current than M_2 . V_{cgo1} will be pulled high, turning on PMOS rectification transistor. M_4 is sized larger than M_3 to create an offset such that V_{cgo1} will go high earlier before V_{in+} exceeds V_{out} . This rise-time compensation will cause fall-time to increase, resulting in larger reverse current loss. Hence, auxiliary bias circuit (M_{b1} and M_{s1}) is added. When V_{cgo1} ties high, V_{s1} will set the output Q of *SR* latch to 'HIGH'. M_{s1} will be turned on, sinking current from M_{b1} to pull V_{cgo1} low. This will cause V_{ctl1} to turn the PMOS rectification transistor off earlier before V_{in+} falls below V_{out} . When complementary PMOS rectification transistor turns on, V_{r1} will set Q to 'LOW' to turn off the auxiliary bias circuit.

Fig. 2.14. Comparator with ON-OFF response compensation [66]. M_4 is sized larger than M_3 to create an offset such that comparator response can be improved. V_{out} is the rectifier output voltage.

Fig. 2.15 shows a high speed comparator with offset-control. When $V_{INI} > V_{REC}$, P_8 sources more current than P_7 and V_A will be tied high and V_{OUT} goes 'LOW'. PMOS rectification transistor will be turned on. In the meantime, P_{12} will also be turned on and activate the $Offset_R$ control block by sourcing current to N_5 . N_6 will sink more current and pull V_A to 'LOW' and turn PMOS rectification transistor off earlier before $V_{INI} < V_{REC}$. When V_{OUT} is tied high, P_{15} will be turned on and activate the $Offset_F$ control block. V_A will rapidly increase such that PMOS rectification transistor is turned on earlier before V_{INI} rises above V_{REC} .

voltage drop of conducting transistor. This rectifier has been reported to provide excellent PCE for both low and high frequency application at small input power. Even though the rectifier has high PCE, it suffers from reverse leakage issue during the on-off transition when a switching pair conducts in reverse bias. Fig. 2.17 shows the reverse leakage current during on-off transition. Moreover, the circuit will experience gate-induced drain leakage (GIDL) when V_{in} is large, limiting its application for near-field power transfer.

Fig. 2.16. Schematic of complementary cross-coupled rectifier [68].

Fig. 2.17. Transient simulation showing reverse leakage current in M_{P1} during on-off transitions. Reverse leakage current (I_{D1}) occurs when difference between V_{out} and V_{RF-} is equal/larger than M_{P1} threshold voltage, with V_{out} larger than V_{RF+} and V_{RF+} larger than M_{N2} threshold voltage [69].

In order to overcome issue faced by [68], [71] proposes a dual-mode rectifier as shown in Fig. 2.18. When V_{OUT} is lower than pre-determined V_{DETECT} of the voltage detector circuitry, switch control signal S_1 will be tied high. The rectifier will function as a cross-coupled rectifier (Fig. 2.19(a)). When input voltage increases and causes the output voltage to increase, S_1 will be tied low while S_2 will go high. The rectifier will then be connected as a cross-coupled bridge rectifier (Fig. 2.19(b)). Fig. 2.20 shows the improvement in dual-mode rectifier PCE over an input power range.

Fig. 2.18. Schematic of dual-mode rectifier [71]. S_1 and S_2 are the switches control signal.

Fig. 2.19. (a) Cross-coupled rectifier when S_1 in Fig. 2.18 is tied high. (b) Cross-coupled bridge rectifier when S_2 is tied high [71].

Fig. 2.20. PCE of dual-mode rectifier as compared to cross-coupled rectifier and cross-coupled bridge rectifier [71].

In order to achieve larger output voltage, combination of rectifier with charge pump or DC-DC converter can be implemented. Fig. 2.21 shows a topology consisting cross-coupled rectifier and cross-coupled charge pump [72]. N-stage rectifier is needed to generate DC voltage large enough for clock generator and charge pump to operate. The converted DC voltage is then being boosted to higher level by the charge pump.

Fig. 2.21. RF-DC converter with cross-coupled rectifier and cross-coupled doubler [72].

In [73], the large reverse current with increasing input voltage is overcome by using thick-oxide MOSFET. Fig. 2.22 shows a comparison in the amount of reverse leakage current between nominal PMOS and thick-oxide PMOS. Due to higher threshold voltage introduced by the thick-oxide MOSFET, the reverse leakage is reduced even though PMOS is not fully turned off.

Fig. 2.22. Comparison on I-V response between nominal MOSFET and thick-oxide MOSFET [73].

2.1.9 Other Rectifier Topologies

In other to improve the operating input power range of rectifier, dual path rectifier topology has been proposed in [84], as shown in Fig. 2.23. The system uses five-stage complementary cross coupled rectifier [68] for each path with different transistor types to maximize the sensitivity and PCE. An additional five-stage rectifier is used to generate reference voltage for path selection. The rectifier is

reported to achieve peak PCE of 36.5 %, and maintaining high PCE (i.e. > 20%) over 11 dB range.

Fig. 2.23. Block diagram of dual-path rectifier [84]. The comparator compares output voltage of reference path and high power path for path selection.

Fig. 2.24 shows the quasi-floating gate bias approach which is proposed in [107] for extending the rectifier high PCE range. Bandgap reference circuit is implemented to generate DC bias voltage for the gates of the rectification transistors. When V_{in} is smaller than optimal point, a positive boost voltage is provided to the transistor gate to improve the forward conduction. When V_{in} is larger than optimal point, a negative boost voltage is generated to reduce the reverse leakage current. The work achieves maximum PCE of 66.6 %.

Fig. 2.24. Schematic of single-stage quasi-floating gate bias rectifier [107].

The gate bias is supplied by bandgap reference circuit. G_{N1} is gate voltage of M_{N1} and G_{P1} is the gate voltage of M_{P1} .

In the WLAN energy harvesting system proposed in [81], the rectifier is realised with combination of Greinacher rectifier [51] and Cockroft-Walton charge pumps as shown in Fig. 2.25. The 4-stage rectifier has maximum efficiency of 37.5 %.

Fig. 2.25. Rectifier for WLAN energy harvesting implemented with combination of Greinacher rectifier and Cockcroft-Walton charge pump.

2.1.10 Comparison of Rectifier

Rectifier is the first stage of RF-DC energy harvesting circuit. The selection of rectifier topology is determined by three major criteria, i.e. intended application, operating frequency and input power or voltage range. As the operating frequency increases, PCE of all rectifier topologies will degrade due to larger transistor switching loss and parasitic effects. Table 2.1 summarizes and compares the different rectifier topologies discussed in this chapter.

Table 2.1. Comparison of different rectifier topologies, including minimum input voltage and PCE.

Rectifier topologies	Operation/performance	Pros	Cons
Diode-type rectifier	i. $V_{in,min} > 0.7 - 1.0 \text{ V}$	i. Large forward current ii. Negligible reverse leakage current	i. Large forward voltage drop (0.7-1.0 V) ii. Low PCE
Diode-connected MOSFET rectifier	i. $V_{in,min} > V_{th} $ ii. PCE = 29.6% [54]	i. Large forward current ii. Negligible reverse leakage current	i. Forward voltage drop of $ V_{th} $ ii. Zero-threshold MOSFET eliminates $ V_{th} $ drop but large reverse leakage current iii. Low PCE
Vth-cancellation rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 11.0% @ 950 MHz, -6.0 dBm input [55]	i. Smaller turn-on voltage	i. Significant reverse leakage current ii. Additional gate bias generation circuit iii. Low PCE

Rectifier topologies	Operation/ performance	Pros	Cons
Self-V _{th} -cancellation rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 29.0% @ 953 MHz, -9.9 dBm input [57]	i. Smaller turn-on voltage ii. No additional circuit for gate bias iii. Excellent PCE at low input power	i. Large reverse leakage when $V_{OUT} > V_{th} $
Bootstrapped CMOS rectifier	i. $(V_{in} - V_{OUT}) \geq V_{th} $ ii. Operates at low frequency iii. PCE = 80.0% @ 10 MHz, 2.7 V input [58]	i. Excellent PCE at low frequency	i. Low PCE at high frequency ii. Large footprint
Boosted-gate CMOS rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 73.0% @ 950 MHz, 0.29 V input [60]	i. Smaller turn-on voltage ii. Excellent PCE	i. Each main rectifier required eight additional transistors

Rectifier topologies	Operation/ performance	Pros	Cons
Active diode rectifier	i. $V_{in,min} < V_{th} $ ii. Operates at low frequency iii. PCE = 94.2% @ 200 Hz, 1 V input [62]	i. Function like ideal switch ii. Small forward voltage drop (= V_{DS}) iii. Excellent PCE at low frequency	i. Require auxiliary power source ii. Low PCE at high frequency
Complementary cross-coupled rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 67.5% at 953 MHz, -12.5 dBm input [68]	i. Smaller turn-on voltage ii. No additional circuit for gate bias	i. Reverse current due to GIDL at large V_{in} ii. Low PCE at large V_{in}
Dual-path rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 36.5 % at 900 MHz, -10 dBm input [84]	i. Extended high PCE range	i. Reference voltage generator rectifier consumes power which affected the PCE
Quasi-floating gate bias rectifier	i. $V_{in,min} < V_{th} $ ii. PCE = 66.6 % at 2.4 GHz, 0.3 – 0.5 V input [107]	i. Extended high PCE range	i. Required bandgap reference circuit to generate gate bias voltage

Rectifier topologies	Operation/ performance	Pros	Cons
Rectifier-booster regulator	i. $V_{in,min} > 0.7 - 1.0$ V ii. PCE = 37.5 % at 2.45 GHz, 13 dBm input [81]	i. Relatively high output voltage	i. Low PCE

2.2 Optimization of Rectifier

Although the overall efficiency of RF energy harvesting system is contributed by every single block along the system chain from antenna to matching network and rectifier, rectifier is the key component that dictates the system efficiency. Design optimization methodology which aids the optimization of rectifier design will expedite the design cycle and ease technology portability.

Fig. 2.26. Voltage doubler with Kirchhoff voltage loop including parasitics [74].

An analytical model based on decoupling the MOS diode mean and variable voltages required to provide the load current in steady state is presented in [74]. Fig. 2.26 shows the voltage doubler from [74]. Firstly, the diode and capacitors (coupling capacitor and load capacitor) characteristics are modeled through mathematical representations.

$$v_{D1} = v_{in} - v_{C1} \text{ and } v_{D2} = -v_{D1} + v_{C2} \quad (2.4)$$

Next, the mean point around the voltage applied on D1 and D2 ($\overline{V_{Dx}}$) is identified.

$$\frac{1}{T} \int_0^T i_D(v_{Dx} - \overline{V_{Dx}}) dt = I_{load} \quad (2.5)$$

Then, the parasitic capacitances are deduced. The capacitors voltages are represented as:

$$\Delta v_{C1}(t) = \frac{(-i_{D1}(t) - i_{Cpar1}(t) + i_{D2}(t) + i_{Cpar2}(t))}{C_1} \Delta t \quad (2.6)$$

$$\Delta v_{C2}(t) = \frac{(-i_{D2}(t) - i_{Cpar2}(t) - I_{load}(t) - i_{CparOUT}(t))}{C_2} \Delta t \quad (2.7)$$

The equations are solved through iterations in MATLAB with look-up table consisting transistors' DC and AC characteristic computed from SPICE models. Application of this methodology on a voltage doubler design yields an output voltage with absolute mean error lower than $5e^{-4}$ V in around 1 minute, as shown in Fig. 2.27. This methodology takes into consideration the AC and DC characteristics of devices, input voltage, frequency, load current, temperature, backgate voltage and parasitic capacitors.

Fig. 2.27. Comparison for v_{OUT} calculated from MATLAB and ELDO (SPICE-like), for MOS diode width/length = 300/2, $I_{load} = 1.5\mu\text{A}$ and $C_1 = C_2 = 5\text{pF}$ [74].

An automated design methodology to design CMOS multi-stage Dickson rectifiers is proposed in [75]. The design and layout can be generated according to specifications including the impedance matching. Fig. 2.28 shows the automated design flow from [75]. Firstly, the number of stages needed to achieve the required output voltage is determined.

$$V_{out} = N \left(\frac{C}{C + C_S} V_{ac} - \frac{I_0}{f(C + C_S)} - V_{th} \right) \quad (2.8)$$

where V_{ac} is the input signal peak-to-peak voltage, C is the coupling capacitor, I_0 is the average current drawn by output load, C_S is the parasitic capacitance at each pumping node and f is the operating frequency [75]. Next, the power loss due to

transistor operating in super-threshold region and leakage power is computed for rectifier efficiency calculation.

$$\eta = \frac{P_{out}}{P_{out} + NP_{loss}} \quad (2.9)$$

Then, the circuit input impedance is estimated through curve fitting and device sizing is calculated. Interval halving method is used to find the optimum solution based on objective function in (2.10).

$$Obj = \alpha(1 - \eta) + \beta|R_{in} - 50| + \gamma X_{in} \quad (2.10)$$

where α , β and γ are user-defined relative weightage between the specifications. This methodology considers impedance matching and power efficiency. Although the cost for matching network can be reduced, the circuit has lower efficiency.

Fig. 2.28. Automated rectifier design flow. Based on input specifications, the tool will calculate design parameters and generate netlist. The generated netlist will be simulated via Spectre simulation to verify circuit performance. The tool will then calculate matching network device sizing for system performance [75].

Fig. 2.29. Schematic of diode doubler with its fundamental frequency equivalent input impedance without parasitic series loss resistance [76].

An analytical methodology to design Schottky diode rectifier is presented in [76]. Fig. 2.29 shows the diode doubler schematic used in [76]. Firstly, a first order approximation with constant factor χ is used in relationship between diode peak current (I_{DPEAK}) and load current (I_{LOAD}). The diode peak voltage is expressed as:

$$\begin{aligned}
 V_{DPEAK} &\cong nV_T \ln\left(\frac{I_{DPEAK}}{I_S}\right) \\
 &\cong nV_T \ln\left(\frac{\chi I_{LOAD}}{I_S}\right)
 \end{aligned} \tag{2.11}$$

The non-ideal diode threshold voltage with load current is considered. Next, the circuit input impedance is derived.

$$R_{DBLR} \cong \frac{V_{IC}}{4I_{LOAD}} \left(\frac{C_C}{C_C + C_{PARA}} \right) \left(\frac{C_C + C_{D2} + C_{TUBD2}}{C_C} \right)^2 \quad (2.12)$$

$$C_{DBLR} \cong C_{PARA} \left(\frac{C_C}{C_{PARA} + C_C} \right) + C_{cp} \quad (2.13)$$

Then, the parasitic resistive losses (diode and capacitor losses, and components fixed loss) are transformed to the input. Finally, the RF to DC equation is established.

Fig. 2.30. Comparison between predicted output voltage, SPICE simulation and measurement. Predicted output voltage is 7.1-8.5% higher than actual measurement for rectifier with more than 12 diodes [76].

Fig. 2.30 shows the comparison between predicted output voltage and actual SPICE simulation. Although parasitic capacitance and input impedance are

considered, this methodology assumes voltages applied to different diodes are same.

Fig. 2.31. Comparison between simulated and measured PCE based on iterative optimization methodology [77].

An iterative optimization methodology for efficiency is proposed in [77]. A two stage Greinacher rectifier (with diode-connected MOSFET) is designed in the study. Firstly, numerical approach is used to calculate transistor bias point.

$$\frac{P_{OUT}}{V_{OUT}} = \frac{1}{T} \int_0^T I_D \left[V_M - \left(\left(\frac{V_{OUT}}{2N} \right) - V_M \right) (1 \pm \sin(\omega t)) \right] dt \quad (2.14)$$

where V_M is the voltage drop across transistor and N is number of stages. Next, the input impedance in steady-state conditions is defined. Rectifier input capacitance is simplified as:

$$C_{IN} = \alpha C_{MOS}(0) W_n \left(1 + \frac{I_{Sn}}{I_{Sp}} \right) N \quad (2.15)$$

where α is empirical coefficient ($=1.1$), C_{MOS} is the transistor's capacitance, W_n is NMOS width and I_S is the reverse current. The efficiency of matching network is calculated, followed by the rectifier PCE. W_n and N are varied for iterative calculation of PCE. Fig. 2.31 shows comparison between simulated and measured PCE for rectifier design based on this optimization methodology. The rectifier efficiency curve is affected by input impedance mismatch between antenna and rectifier. The difference in simulated and measured PCE is attribute to higher transistor threshold voltage on silicon and ohmic losses which are not fully represented in model file and post-layout simulations.

A gradient-base optimization methodology, combining with SPICE simulation, is proposed in [78]. A three stage Greinacher rectifier (with ultra-low-power diode) is designed in the study. Firstly, the transistor type, transistor channel length and number of stages are pre-determined. Next, transistor width is obtained through steepest ascent iteration method for each stage. Fig. 2.32 shows the first stage transistors widths optimization whereby different initial width value converges to same optimal PCE. The time needed for obtaining the optimum transistor width is between 8 to 39 hours. The predicted PCE has an absolute mean error of 0.01%. Next, the capacitors are optimized by restricting the total capacitance value to cater for tradeoff between PCE and chip area. Fig. 2.33 shows the area-constrained optimization of capacitor value among the stages.

Fig. 2.32. A three-stage rectifier's first stage transistors widths optimization. Diamond symbols indicate different initial transistors widths used in the optimization algorithm, and all iterations converge to same final transistors widths which result in optimum efficiency [78].

Fig. 2.33. Area-constrained optimization of capacitance distribution between stages of a three-stage rectifier. V_{out} is higher than 1.8 V when $C_{i,j}$ is larger than 5 pF for $V_{in} = 1$ Vpp, $I_{load} = 10$ μ A and frequency = 13.56 MHz [78].

[74], [76] and [77] proposed analytical method for circuit optimization. The accuracy in prediction for analytical or numerical methodology depends heavily on the accuracy and completeness of the mathematical models used to characterise the devices and circuit behaviours. [75] combines numerical approach with SPICE simulation for design automation from schematic to layout. The input impedance is estimated through curve fitting, and user defines the optimization weightage between PCE and input impedance. Hence, PCE is impacted due to consideration of input impedance. [78] proposed gradient-base optimization methodology with SPICE simulation. This approach is appropriate for circuit with concave function. The algorithm is comparable to parametric analysis which explains the long duration required for optimizing single parameter.

CHAPTER 3 PROPOSED DUAL-PATH RF ENERGY HARVESTER

In order to acquire wide applications in wireless charging for low power devices and to maximize efficacy in harvesting energy from surrounding environment and designated source, a dual-path rectifier for RF energy harvester has been proposed. The rectifier is optimized to operate at 2.45GHz, which is the frequency band for industrial, scientific and medical (ISM) and IEEE 802.11/Wi-Fi, while is able to support 950MHz operation.

3.1 System Overview

Fig. 3.1. Block diagram of wireless sensor node with integrated energy harvesting system, which is comprised of antenna, matching network, RF-to-DC converter, energy storage unit, control unit and sensors with internal circuitries.

Fig. 3.2. Block diagram of proposed dual-path RF energy harvester, which is comprised of antenna, switches, baluns, matching networks, low input power rectifier, high input power rectifier and voltage aware circuitry.

Fig. 3.1 shows block diagram of a typical RF energy harvesting system. RF antenna captures and converts received power into signal voltages. The power unit converts the extracted signal voltages to DC voltage. Optionally, the system might include voltage regulator and control circuitry according to system load requirements. The efficiency of harvester in converting received power to DC output voltage is expressed as

$$Eff_{TOTAL} = Eff_{MN} \times Eff_{RECT} \quad (3.1)$$

where Eff_{RECT} is the rectifier efficiency and Eff_{MN} is the matching network efficiency.

Fig. 3.2 shows the proposed dual-path RF energy harvester, which consists of a low input power rectifier, a high input power rectifier, a voltage detector, a switch and an adjustable-offset comparator. During low input power, the low-power rectification path is enabled to extract power from antenna and to convert the RF power into DC power. During high input power, the high-power rectification path is enabled. A comparator controlled switch is inserted along the output of high-power rectification path to prevent current flowing back to source from the output capacitor. The comparator has built-in adjustable offset and it compares V_{RECT2} and V_{OUT} to enable/disable the output switch. In order to minimize power consumption, V_{RECT2} detector is used to sense and assess rectifier output voltage, and output control signal EN_COMP . The EN_COMP signal determines when to enable the comparator.

3.2 Low-Power Rectifier

For low received power with small input voltage amplitude, the effective threshold voltage of the main rectification diodes needs to be reduced for proper operation of the circuit. Complementary cross-coupled rectifier (CCCR) is a commonly used topology in many prior arts due to its ability to provide high PCE at small input voltage and its passive threshold-voltage-compensation capability. However, this topology suffers from high leakage problem when input amplitude is large. Hence, it has narrow high-PCE range which limits its application. Focus of this research work is to design rectifier for high frequency operation with high PCE over wide input range.

When $V_{in+} > V_{in-}$, P_I turns on when difference between V_X and V_{DI} is equal or larger than PMOS threshold voltage. When $V_{in+} < V_{in-}$, P_I turns off with gate connected to V_{OUTI} .

During the initial phase of this research work, a rectifier with dynamic V_{th} -cancellation gate bias has been proposed, as shown in Fig. 3.3. Transistor $P_{1,2}$ are the main rectification diodes. Unlike conventional V_{th} -cancellation topology [55] with fixed gate bias which resulted in main rectification diode not able to turn on

and off completely, the proposed V_{th} -cancellation biasing circuitry will bias the transistor gate dynamically.

During positive half cycle of input signal when $V_{in+} > V_{in-}$, P_2 is off with gate connected to V_{OUT1} . N_2 will turn on when $(V_X - V_Y)$ is equal or larger than NMOS threshold voltage (V_{thn}) and coupling capacitor C_{c2} will ideally be charged up to $(|V_{in1} - V_{DS,N2}|)$. P_1 will turn on when $(V_{D1} - V_X)$ is larger than PMOS threshold voltage (V_{thp}), where V_{D1} is the drain-to-source voltage of FB_1 . Minimum V_{D1} is determined by the ON resistance of FB_1 . The ON resistance of FB_1 can be represented as:

$$R_{FB_on} = \frac{L}{W\mu C_{ox}(V_X - V_{thn} - V_{D1})} \quad (3.2)$$

where μ is the electron mobility, C_{ox} is the gate-oxide capacitor per unit area, W/L is the aspect ratio of the transistor, V_{thn} is the NMOS threshold voltage, V_X is the transistor gate voltage and V_{D1} is the transistor drain voltage. Hence, V_{D1} is defined as:

$$V_{D1} = \frac{R_{FB_on}}{R_{FB_on} + R_{D1}} \quad (3.3)$$

During negative half cycle of input signal when $V_{in+} < V_{in-}$, P_1 is off with gate connected to V_{OUT1} . N_1 will turn on when $(V_Y - V_X) \geq V_{thn}$ and coupling capacitor C_{c1} will theoretically be charged up to $(|V_{in+} - V_{DS,N1}|)$. P_2 will turn on when $(V_{D2} - V_Y) \geq V_{thp}$, where V_{D2} is the drain-to-source voltage of FB_2 . Minimum V_{D2} is determined by the ON resistance of FB_2 .

The gate of $P_{1,2}$ is not biased at negative potential during conduction. This is to prevent excessive source-to-gate voltage applying to $P_{1,2}$, which might cause transistor to breakdown, when input voltage is large. The dynamic gate biasing circuitry generates a low gate potential for $P_{1,2}$ during on-state while connect $P_{1,2}$ into diode-connected configuration during off-state. The rectifier output voltage V_{OUT1} is defined as $[2 \times (V_{in+} - (|V_{thp}| + V_D))]$.

Fig. 3.4. Comparison in PCE performance of dynamic gate bias rectifier and CCCR across different input amplitude at 2.45 GHz with 5 k Ω load. Due to controlled gate voltage, the dynamic gate bias rectifier achieves higher PCE for input voltage larger than 0.8 V as compared to CCCR.

Fig. 3.4 shows the simulated PCE of dynamic gate bias rectifier at 2.45 GHz with 5 k Ω load. The proposed rectifier provides higher PCE for input voltage amplitude larger than 0.8 V as compared to CCCR. For same load condition (i.e. 5 k Ω), it is able to attain PCE above 20% for input voltage range of 0.95 V as compared to voltage range of 0.63 V for CCCR. This shows the dynamic gate biasing circuitry is able to mitigate high leakage issue faced by CCCR at high input voltage. However, the peak PCE of 33.2% is much lower as compared to CCCR's peak PCE (48.4%). This low PCE is attributed to the power consumption of the dynamic gate biasing circuitry, the delay in response of $FB_{1,2}$ to change in $V_{X,Y}$, and the gate of main rectification diode being tied to a small positive potential instead of negative potential during conduction which restricted the amount of forward current.

3.2.2 Rectifier with DC-boosted gate bias

In this work, we propose a novel rectifier with DC-boosted gate bias [15], [89]. This topology is chosen to be implemented in the proposed dual-path energy harvester. Fig. 3.5 displays the fundamental building block of our proposed low-power rectifier, consisting single-stage rectifier with DC-boosted gate voltage compensation. $MP_{1,2}$ are PMOS transistor pair functioning as main rectification diodes while $MN_{1,2}$ are NMOS transistor pair providing current return path to RF source. Auxiliary gate capacitors (C_{aux}) and self-cascode PMOS transistor pair ($MB_{1,2}$) forms the auxiliary gate bias circuit to supply DC-boosted gate bias to $MP_{1,2}$, respectively.

(a) Single stage of proposed rectifier

(b) During positive half cycle

When input signal $V_{in+} > V_{in-}$ during positive half cycle of, MP_1 and MN_2 are turned on while MP_2 and MN_1 are turned off. Current flows from V_{in+} through MP_1 to load, and back to V_{in-} through MN_2 . Ideally, Cc_2 will be charged up to $(|V_{in-}| - |V_{in+}|)$.

$-V_{DS,MN2}|)$. Both MP_1 and MN_2 operate in linear region. MP_1 will turn on when $(V_{G1} - V_1)$ is equal or smaller than PMOS threshold voltage (V_{thp}). MN_2 will conduct when $(V_1 - V_2)$ is equal or larger than V_{thn} . MP_1 and MN_2 drain-to-source current (I_{DS}) can be defined as:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \left(\frac{V_{DS}}{2} \right)^2 \right] \quad (3.4)$$

where V_{GS} is the transistor gate-to-source voltage, V_{th} is the threshold voltage and V_{DS} is the transistor drain-to-source voltage. The ON resistance (R_{DS_ON}) of MP_1 and MN_2 can be expressed as:

$$R_{DS_ON} = \frac{L}{W \mu C_{ox} (V_{GS} - V_{th} - V_{DS})} \quad (3.5)$$

From (3.4) and (3.5), can be concluded that lower V_{th} will give rise to larger I_{DS} and larger transistor aspect ratio will lead to smaller R_{DS_ON} , reducing the forward voltage drop. However, lower V_{th} and larger W/L will lead to larger subthreshold current flowing in reverse direction when $V_{in+} < V_{in-}$. In the auxiliary gate bias branch, V_{G1} is confined by the source-to-gate voltage (V_{SG}) of MB_1 and the parasitic PN diode between drain-bulk of MB_1 . MB_1 is a diode-connected self-cascode transistor which sets the DC bias voltage at V_{G1} . A DC-boosted bias voltage is supplied to the gate of MP_1 by superimposing the AC component of V_{in-} onto this DC bias voltage. The current flowing through the auxiliary gate bias branch ($I_{MB1,2}$) is defined as:

$$I_{MB1,2} \quad (3.6)$$

$$= \begin{cases} I_{s0}\mu \frac{W}{L} * \exp^{\frac{V_{OUT1}-V_{G1,2}-|V_{thp}|}{nV_T}} * \left(1 - \exp^{\frac{-(V_{OUT1}-V_{G1,2})}{V_T}}\right), & V_{SG} < |V_{thp}| \\ I_{s0}\mu \frac{W}{L} \left(1 - \exp^{\frac{-(V_{OUT1}-V_{G1,2})}{V_T}}\right) + \frac{1}{2}\mu C_{ox} \frac{W}{L} (V_{OUT1} - V_{G1,2} - |V_{thp}|)^2, & V_{SG} \geq |V_{thp}| \end{cases}$$

where I_{s0} is the sub-threshold saturation current, n is the sub-threshold region swing parameter and V_T is the thermal voltage. Assuming $(V_{OUT1} - V_{G1,2}) > 3V_T$,

$\left(1 - \exp^{\frac{-(V_{OUT1}-V_{G1,2})}{V_T}}\right) \approx 1$. Therefore, (3.6) can be simplified as:

$$I_{MB1,2} \quad (3.7)$$

$$= \begin{cases} I_{s0}\mu \frac{W}{L} * \exp^{\frac{V_{OUT1}-V_{G1,2}-|V_{thp}|}{nV_T}}, & V_{OUT1} - V_{G1,2} < |V_{thp}| \\ I_{s0}\mu \frac{W}{L} + \frac{1}{2}\mu C_{ox} \frac{W}{L} (V_{OUT1} - V_{G1,2} - |V_{thp}|)^2, & V_{OUT1} - V_{G1,2} \geq |V_{thp}| \end{cases}$$

$$I_{aux} = 2\pi * freq * C_{aux} * V_{in+,-} \quad (3.8)$$

$I_{aux} \approx I_{MB1,2}$. Hence, $V_{G1,2}$ can be expressed as:

$$V_{G1,2} = \begin{cases} V_{OUT1} - |V_{thp}| - \left(nV_T \ln\left(\frac{I_{aux}}{I_{s0}\mu \frac{W}{L}}\right)\right), & I_{aux} \leq I_{s0}\mu \frac{W}{L} \\ V_{OUT1} - |V_{thp}| - \sqrt{\frac{2\left(I_{aux} - \left(I_{s0}\mu \frac{W}{L}\right)\right)}{\mu C_{ox} \frac{W}{L}}}, & I_{aux} > I_{s0}\mu \frac{W}{L} \end{cases} \quad (3.9)$$

When input signal $V_{in+} < V_{in-}$ during negative half cycle, MP_2 and MN_1 are ON while MP_1 and MN_2 are turned off. Current flows from V_{in-} through MP_2 to load, and back to V_{in+} through MN_1 . Ideally, C_{C1} will be charged up to $(|V_{in+} - V_{DS,MN1}|)$.

Both MP_2 and MN_1 operate in linear region. MP_2 will conduct when $(V_{G2} - V_2)$ is equal or smaller than V_{thp} . MN_1 will turn on when $(V_2 - V_1)$ is equal or larger than V_{thn} . In the auxiliary gate bias branch, V_{G2} is confined by the V_{SG} of MB_2 and the parasitic PN diode between drain-bulk of MB_2 . MB_2 is a diode-connected self-cascode transistor which sets the DC bias voltage at V_{G2} . A DC-boosted bias voltage is supplied to the gate of MP_2 by superimposing the AC component of V_{in+} onto this DC bias voltage.

In order to achieve higher DC output voltage, more stages of rectifier are needed due to limitation on maximum achievable output voltage from single-stage rectifier. However, there will be issue of higher power dissipation with increasing number of stages, which degrades the PCE. In this work, a 2-stage rectifier has been implemented since two stages are able to produce at least 1 V output voltage for minimum -17 dBm input power and do not cause significant degradation on PCE. Fig. 3.6 shows the proposed 2-stage rectifier. In the first stage, the auxiliary gate bias circuitry generates boosted negative gate voltage for $MP_{1,2}$ so that it can turn on when input voltage is lower than V_{th} during on-state. When $MP_{1,2}$ is in off-state, the auxiliary gate bias circuitry confines the positive gate voltage for $MP_{1,2}$ to prevent GIDL for large input voltage while minimizing reverse leakage current. The output voltage of first stage rectifier (V_{OUT1}) is defined as:

$$V_{OUT1} = 2 \times [v_{in,p} - (V_{th} - V_{Boost1})] \quad (3.10)$$

where $v_{in,p}$ is the RF peak input voltage and V_{Boost1} is the boosted gate voltage. The C_{aux} are connected to $V_{3,4}$ instead of $V_{1,2}$ in the second stage so that its auxiliary

gate bias branch provides slight boost to the positive gate voltage for $MP_{3,4}$ during off-state. This will minimize the reverse leakage current. Fig. 3.7 shows the simulated voltage signals at V_2 , V_{G1} , V_4 and V_{G3} of the 2-stage rectifier for 300 mV input voltage at 2.45 GHz.

Fig. 3.6. Schematic of 2-stage rectifier with DC-boosted gate bias.

Fig. 3.7. Simulated voltage signals at V_2 , V_{G1} , V_4 and V_{G3} with 300 mV input voltage at 2.45 GHz.

Since the rectifier circuit is symmetrical, positive half cycle operation is taken as consideration for circuit power loss calculation. For each rectifier stage, the power loss is primarily determined by PMOS switching loss and conduction loss of both PMOS and NMOS rectification diode, and can be approximated as [67]:

$$P_{loss_1stage} = fV_{OUT}^2 C_{gp} + D_{eff} I_{rms}^2 R_{on,p} + D_{eff} I_{rms}^2 R_{on,n} \quad (3.11)$$

$$P_{in} = P_{OUT1} + (fV_{OUT1}^2 C_{gp} + D_{eff} I_{rms1}^2 R_{on,p} + D_{eff} I_{rms1}^2 R_{on,n}) + P_{aux1} \quad (3.12)$$

$$P_{OUT1} \approx P_{OUT} + (fV_{OUT}^2 C_{gp} + D_{eff} I_{rms2}^2 R_{on,p} \quad (3.13)$$

$$+ D_{eff} I_{rms2}^2 R_{on,n}) + P_{aux2}$$

$$P_{in} \approx P_{OUT} + fC_{gp}(V_{OUT1}^2 + V_{OUT}^2) \quad (3.14)$$

$$+ D_{eff} R_{on,p}(I_{rms1}^2 + I_{rms2}^2)$$

$$+ D_{eff} R_{on,n}(I_{rms1}^2 + I_{rms2}^2) + P_{aux1} + P_{aux2}$$

where C_{gp} is the PMOS gate capacitance, f is the operating frequency, D_{eff} is the effective duty cycle when rectifier is turned on, R_{on} is the transistor ON resistance, P_{aux} is the auxiliary branch power consumption for each stage, V_{OUT1} is the first stage output voltage, and P_{OUT1} is the first stage output power.

The PCE of rectifier is defined as:

$$PCE = \frac{P_{out}}{P_{in}} \times 100\% = \frac{P_{in} - P_{loss} - P_{aux1} - P_{aux2}}{P_{in}} \times 100\% \quad (3.15)$$

$$= \frac{\frac{1}{T} \int_{t1}^{t1+T} v_{out}(t) \times i_{out}(t) dt}{\frac{1}{T} \int_{t1}^{t1+T} v_{in}(t) \times i_{in}(t) dt} \times 100\%$$

$$V_{OUT}^2 / R_{load}$$

$$= \frac{V_{OUT}^2 / R_{load}}{\frac{1}{T} \int_{t1}^{t1+T} v_{in}(t) \times i_{in}(t) dt} \times 100\%$$

where T is one period of the input signal, P_{in} is the average received RF power, P_{loss} is the total power loss, $t1$ is the start time of input signal, V_{OUT} is the DC output voltage, P_{out} is the average DC output power, and R_{load} is the output load.

Fig. 3.8. Simulated low-power rectifier PCE for different input power and loads at 2.45 GHz.

Fig. 3.9. Comparison in PCE between proposed 2-stage rectifier with DC-boostered gate bias and CCCR with different input voltage at 2.45 GHz and 2.2 k Ω load (without matching network). The boosted gate voltage improves the rectifier efficiency and extends the input voltage range for PCE above 20 %.

Fig. 3.8 presents the PCE of proposed 2-stage rectifier for different input power and load conditions, with matching network. As shown, the PCE is a concave function of input power and load whereby each input power has an optimum load condition. PCE degrades with increasing load due to reduction in output power while power dissipation in rectifier elements dominates. The rectifier achieves peak PCE of 72.2% at -10 dBm input power and 15 k Ω load. For same load condition (i.e. 15 k Ω), PCE is above 20% for input power range from -17 dBm to 5 dBm. Fig. 3.9 shows comparison in efficiency between the proposed rectifier

and a 2-stage CCCR at 2.45GHz without matching network and with 2.2 k Ω load, to illustrate novelty of DC-boosted gate bias circuitry in improving rectifier PCE across wide input range.

Fig. 3.10 illustrates the achievable output voltage for different input power level and load conditions at 2.45 GHz. With 15 k Ω load, the proposed rectifier is able to produce 1 V output with minimum input power of -10 dBm. The sensitivity of rectifier is -17 dBm, for 1V output. Fig. 3.11 illustrates the impact of loading effect on output power. Minimum input power of 158.49 μ W (i.e. -8 dBm) is required for output power of 100 μ W.

Fig. 3.10. Simulated low-power rectifier output voltage versus input power at 2.45 GHz for various load conditions. Output voltage 1 V is achieved with minimum input power of -10 dBm for 15 k Ω load.

Fig. 3.11. Simulated low-power rectifier output power versus input power at 2.45 GHz for various load conditions. For 100 μW output power, minimum 158.49 μW input power is required.

3.3 High-Power Rectifier

When RF source is too close to the harvester, transistor gate compensation for effective V_{th} reduction may not be feasible. We propose a 6-stage rectifier with internal body bias to regulate the transistors' V_{th} for optimal efficiency. Fig. 3.12 shows the proposed 6-stage rectifier with internal body bias.

When input signal $V_{in+} < V_{in-}$ during negative half cycle, as shown in Fig. 3.13(a), voltage at node7 is:

$$V_7 = V_{C7} + V_{in} \approx 2V_{in} \quad (3.16)$$

With the charge of V_{in} on C_7 (charged by V_{in-} during previous positive half cycle), voltage at node7 is ideally $2V_{in}$. N_I will turn ON when $V_{gs,NI} \geq V_{thn}$ while P_I will

turn OFF. Both P_1 and N_2 are OFF to prevent reverse charge transfer from higher potential at node2 to lower potential at node1. When N_1 is ON, C_1 is charged to V_{in} . Since $V_1 \approx 0$ V and $V_7 \approx 2V_{in}$, N_7 is turned off and P_7 is turned on. The charge on C_7 is subsequently transferred to node8 through P_7 and N_8 .

The threshold voltage of PMOS and NMOS in forward biased can be defined as:

$$V_{thp} = V_{t0,p} - \gamma \left(\sqrt{|2\Phi_F - V_{SB}|} - \sqrt{|2\Phi_F|} \right) \quad (3.17)$$

$$V_{thn} = V_{t0,n} + \gamma \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right) \quad (3.18)$$

where V_{SB} is the source-to-body voltage, V_{t0} is the threshold voltage when V_{SB} is zero, Φ_F is the surface potential coefficient and γ is the body effect coefficient.

PMOS is intrinsically slower than NMOS. Hence, the body of P_1 and P_7 are connected to respective gate to lower the threshold voltage. The respective intermediate stages' voltage is ideally as follow:

$$V_1 \approx 0 \quad (3.19)$$

$$V_2 = V_3 = 3V_{in}$$

$$V_4 = V_5 = 5V_{in}$$

$$V_6 = 7V_{in}$$

$$V_7 = V_8 = 2V_{in}$$

$$V_9 = V_{10} = 4V_{in}$$

$$V_{11} = V_{12} = 6V_{in}$$

Fig. 3.12. Schematic of 6-stage rectifier with internal body bias.

Fig. 3.13. High-power rectifier first stage operation. (a) Operation during negative half cycle, when P_7 and N_1 are turned on. P_7 will turn on when voltage difference between node7 and node1 is equal or larger than PMOS threshold voltage. The charge on C_7 will be transferred to the next stage. (b) Operation during positive half cycle, when P_1 and N_7 are turned on. P_1 will turn on when voltage difference between node1 and node7 is equal or larger than PMOS threshold voltage. The charge on C_1 will be transferred to the next stage.

When input signal $V_{in+} > V_{in-}$ during positive half cycle, as shown in Fig. 3.13(b), the voltage at node1 is ideally $2V_{in-}$. N_7 is turned on while P_7 is turned off. After

the discharge in previous half cycle, voltage at node7 will be close to ground during this half cycle. C_7 will be charged to V_{in} . Since $V_7 \approx 0$ V and $V_1 \approx 2V_{in}$, N_1 is turned off and P_1 is turned on. The charge on C_1 is subsequently transferred to node2 through P_1 and N_2 .

In subsequent stages, the body of PMOS in N -th stage is connected to $(N-1)$ -th stage holding state. The body of PMOS will be biased at a lower potential as compared to its source and drain. This technique utilizes internally generated DC voltage to lower the threshold voltage when PMOS is turned on, allowing the rectifier to function at lower input voltage.

During initial start-up phase, the intermediate voltage at each stage is not established. However, a fast output ramp-up time is desired to maximize rectifier utilization due to inconsistent availability of input signal source. Hence, the PMOS threshold voltage of first stage and last stage is lowered much more by connecting its body to gate.

Fig. 3.14. Simulated high-power rectifier PCE for different input power and load conditions at 2.45 GHz. Peak PCE of 65.4 % is achieved with 1 dBm input power and 15 k Ω load.

Fig. 3.15. Simulated high-power rectifier output voltage versus input power for various load conditions at 2.45 GHz. Output voltage of 1 V is achieved which minimum -4 dBm input power with 15 k Ω load.

Fig. 3.16. Simulated high-power rectifier output power versus input power for various load conditions at 2.45 GHz. In order to generate 100 μW , minimum input power required is 398.11 μW .

Fig. 3.14 illustrates the PCE of proposed 6-stage rectifier, with matching network, for different input power and load conditions. Peak PCE of 65.4% is attained at 1 dBm input power and 15 $\text{k}\Omega$ load. With same load condition (i.e. 15 $\text{k}\Omega$), PCE is above 20% for input power range from -4 dBm to 8 dBm. Fig. 3.15 illustrates the achievable output voltage for different input power level and load conditions at 2.45 GHz. The proposed rectifier is able to produce 1 V output with minimum input power of -4 dBm with 15 $\text{k}\Omega$ load. Fig. 3.16 shows the impact of loading effect on output power. Minimum input power of 398.11 μW (i.e. -4 dBm) is required for output power of 100 μW .

3.4 Voltage-Aware Block

Fig. 3.17. Block diagram of voltage-aware block, which is comprised of voltage detector, adjustable-offset comparator, gate driver buffer and PMOS switch.

In the event that high-power rectification path is enabled, in order to ensure the output of high-power rectifier (V_{RECT2}) is able to charge the output load and not the reverse, a switch needs to be present in between V_{RECT2} and the load. When V_{RECT2} is lower than harvester output voltage V_{OUT} , the switch should remain open to prevent current from flowing back to source from the output. A comparator is used to compare between V_{RECT2} and V_{OUT} , and turn ON the switch when $V_{RECT2} \geq V_{OUT}$. The comparator needs to be powered-down when no comparison activity is required so as to minimize the overall power consumption. A voltage detector is inserted to sense V_{RECT2} and generate toggle signal, EN_COMP , to enable or

disable the comparator. Fig. 3.17 shows the block diagram of proposed voltage-aware block, which consists of a voltage detector, an adjustable-offset comparator and a PMOS switch.

The voltage detector, which is implemented based on Schmitt trigger, is shown in Fig. 3.18. Fig. 3.19 illustrates the operation states of this Schmitt trigger when V_{RECT2} increase from zero till the low-to-high trigger point (V_{L-H}). As shown in Fig. 3.19(a), when V_{RECT2} is zero, $M4$ and $M5$ are off while $M1$ and $M3$ are operating in linear region. Since I_{DET} is almost equal to zero, $V_{DETECTOR}$ is pulled high to $AVDD$. When V_{RECT2} increases till V_{thn} (Fig. 3.19(b)), $M5$ will start to turn on. Current flowing through $M5$ and $M6$ can be expressed as $I_{M5} = \frac{1}{2}\mu_{M5}C_{ox}\left(\frac{W}{L}\right)_{M5}(V_{RECT2} - V_{thn})^2$. $V_{DETECTOR}$ remains tied high while drain-to-source voltage of $M5$ ($V_{DS,M5}$) starts to decrease. When V_{RECT2} increases till V_{L-H} (Fig. 3.19(c)), due to concurrent increase in V_{RECT2} and decrease in $V_{DS,M5}$, $M4$ turns on and $V_{DETECTOR}$ is pulled low to ground. The voltage detector's V_{L-H} and high-to-low trigger point (V_{H-L}) can be determined by:

$$\frac{\left(\frac{W}{L}\right)_{M5}}{\left(\frac{W}{L}\right)_{M6}} = \left(\frac{\mu_{M6}C_{ox,M6}}{\mu_{M5}C_{ox,M5}}\right)\left(\frac{AVDD - V_{L-H}}{V_{L-H} - V_{thn}}\right)^2 \quad (3.20)$$

$$\frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{M3}} = \left(\frac{\mu_{M3}C_{ox,M3}}{\mu_{M1}C_{ox,M1}}\right)\left(\frac{V_{H-L}}{AVDD - V_{H-L} - |V_{thp}|}\right)^2 \quad (3.21)$$

Fig. 3.18. Schematic of voltage detector.

(a) When $V_{\text{RECT2}} = 0$

(b) When $V_{RECT2} \geq V_{thn}$ (c) When $V_{RECT2} = V_{L-H}$

Fig. 3.19. Operation states of Schmitt trigger when V_{RECT2} increase from zero till the low-to-high trigger point (V_{L-H}). (a) When V_{RECT2} is zero, $V_{DETECTOR}$ is pulled high to $AVDD$. (b) When V_{RECT2} reaches V_{thn} , $V_{DETECTOR}$ remains at $AVDD$ while $M5$ starts to turn on with decreasing drain-to-source voltage. (c) When V_{RECT2} reaches V_{L-H} , $V_{DETECTOR}$ is pulled low to ground.

When V_{RECT2} increases above V_{L-H} , the voltage detector will output an enable signal ($EN_COMP = '1'$) to the comparator. The comparator will be enabled and started comparing the voltage level between V_{RECT2} and V_{OUT} . The gate driver will be enabled to drive the gate of PMOS switch to turn it on or off according to comparator output. When V_{RECT2} drops below V_{H-L} , the voltage detector will output a disable signal ($EN_COMP = '0'$) to the comparator. Both the comparator and gate driver will be disabled, and PMOS switch will remain open. Fig. 3.20 shows the simulated response when V_{RECT2} increases from 0 V to 1.5 V, and vice versa. The voltage detector is designed to have a low-to-high trigger point of 675 mV and a high-to-low trigger point of 515 mV.

Fig. 3.20 Simulated response of voltage detector when V_{RECT2} increases from low-to-high and decreases from high-to-low. The low-to-high trigger point is 0.675 V, and the high-to-low trigger point is 0.515 V.

Fig. 3.21 shows schematic of the proposed comparator. For low voltage application, common gate (CG) configuration is preferred. A complementary common-gate amplifier has been proposed to maximize the operational input voltage range, and to optimize the rise-time and fall-time of comparator. In this design, $\left(\frac{W}{L}\right)_{MP1C} = \left(\frac{W}{L}\right)_{MP2C}$ and $\left(\frac{W}{L}\right)_{MN4C} = \left(\frac{W}{L}\right)_{MN5C}$. MP_{1C} and MP_{2C} form a current mirror pair with gates connected together at potential V_A . MN_{4C} and MN_{5C} form another current mirror pair with gates connected together at potential V_B .

When V_{RECT2} is higher than V_{OUT} , MP_{1C} will draw more current as compared to MP_{2C} and pull output of comparator-N (V_{CMPN}) high. At the same time, more current will flow through MP_{4C} as compared to MP_{5C} , and output of comparator-P (V_{CMPP}) is pulled high. Both V_{CMPN} and V_{CMPP} will drive the gate driver. The gate driver output voltage (V_{SW}) will be set low and PMOS switch is turned on. In order to optimize the conduction time when V_{RECT2} is greater than V_{OUT} , an offset can be introduced in comparator-N by altering the transistors sizing ratio between MN_{2C} and MN_{3C} . MN_{3C} is sized larger than MN_{2C} such that I_{MN2C} is smaller than I_{MN3C} . Hence, V_{CMPN} will trigger an earlier low-to-high transition when V_{RECT2} is higher than V_{OUT} .

When V_{RECT2} is lower than V_{OUT} , MP_{2C} will draw more current and pull V_{CMPN} low. At the same time, more current will flow through MP_{5C} and pull V_{CMPP} low. Both V_{CMPN} and V_{CMPP} will drive the gate driver. V_{SW} will be set high and the PMOS switch is turned off. In order to minimize the reverse conduction when

V_{RECT2} is smaller than V_{OUT} , an offset can be introduced in comparator-P by altering the transistors sizing ratio between MP_{4C} and MP_{5C} . MP_{5C} is sized larger than MP_{4C} such that I_{MP5C} is larger than I_{MP4C} . Hence, V_{CMPP} will introduce an earlier high-to-low transition when V_{RECT2} is lower than V_{OUT} .

Control signals CP_1 - CP_6 and CN_1 - CN_6 are meant for post-fabrication trimming to tune the intended current offset between MN_{2C} and MN_{3C} , and MP_{4C} and MP_{5C} .

Fig. 3.21. Schematic of complementary common-gate adjustable-offset comparator.

Fig. 3.22. Comparison in output response for different types of CG comparator. PMOS CG comparator responds fast when V_{RECT2} falls below V_{OUT} but slower response when V_{RECT2} rises above V_{OUT} . NMOS CG comparator responds fast when V_{RECT2} rises above V_{OUT} but slower response when V_{RECT2} falls below V_{OUT} . Complementary CG responds faster than PMOS CG when V_{RECT2} rises above V_{OUT} and faster than NMOS CG V_{RECT2} falls below V_{OUT} .

Fig. 3.22 shows the output responses of different types of CG comparator. PMOS CG comparator has a faster response when V_{RECT2} is lower than V_{OUT} , introducing an earlier high-to-low transition to the gate driver. The gate driver output (V_{SW})

will pull high earlier to turn off the PMOS switch. NMOS CG comparator has a faster response when V_{RECT2} is higher than V_{OUT} , introducing an earlier low-to-high transition to the gate driver. V_{SW} will pull low earlier to turn on the PMOS switch.

The complementary CG comparator combines the best characteristics of PMOS-type comparator and NMOS-type comparator. It has a relatively fast low-to-high output response to exploit the conduction period when V_{RECT2} is higher than V_{OUT} while having a fast high-to-low output response to minimize reverse leakage current when V_{RECT2} is lower than V_{OUT} .

Fig. 3.23. Impact of reference current on output response of complementary CG comparator.

Fig. 3.23 illustrates the impact of referent current setting on the output response of complementary CG comparator. For reference current setting of 500 nA, comparator shows a fast response in suppressing reverse leakage current when $V_{RECT2} < V_{OUT}$. However, it is slower in switching on the PMOS switch when $V_{RECT2} > V_{OUT}$. This will impact the amount of conduction current being transferred from high-power rectifier output to the harvester output, which will degrade the PCE.

When reference current is set to 50 nA, comparator is slow in response to the difference between V_{RECT2} and V_{OUT} . This delay in switching off the PMOS when $V_{RECT2} < V_{OUT}$ will cause significant amount of reverse leakage current flowing from harvester output back to source. The PCE of harvester will be impacted.

Fig. 3.24 shows the simulated response of voltage-aware block. When V_{RECT2} rises from 0 V to 675 mV, voltage detector will sense the low-to-high transition and output $XEN_COMP = '0'$ to enable the comparator and gate driver. Comparator will be activated to start comparing between V_{RECT2} and V_{OUT} . When V_{RECT2} is greater than V_{OUT} , V_{SW} will be pulled low and the PMOS switch is turned on. When V_{RECT2} is smaller than V_{OUT} , V_{SW} will be pulled high and the PMOS switch is turned off. When V_{RECT2} decreases till 515 mV, voltage detector will sense the high-to-low transition and disable both the comparator and gate driver.

Fig. 3.24. Simulated response of voltage-aware block. When V_{RECT2} rises from 0 V to 0.675 V, voltage detector will enable comparator and gate driver ($XEN_COMP = '0'$). When V_{RECT2} falls till 0.515 V, voltage detector will disable comparator and gate driver ($XEN_COMP = '1'$).

3.5 System-level Performance

In order to widen the operational input power range, a dual-path RF energy harvester has been proposed. The low-power rectifier has been optimized at low input power while the high-power rectifier has been designed for higher input power. Fig. 3.25 shows the overall PCE performance of harvester with 15 k Ω load at 2.45 GHz. The PCE is above 20% for input power from -17 dBm to 8 dBm, accounting for power range of 25 dB.

Fig. 3.25. Simulated PCE of dual-path rectifier at 2.45 GHz.

3.6 Other Design Considerations

3.6.1 Transistor Sizing

In order to achieve high PCE, proper sizing of rectifier transistors is required. The circuit needs to be optimized between smaller voltage drop across transistor source-drain junction, minimum leakage current and smaller transistor parasitic capacitance. Transistor with larger W/L will improve the forward current resulting in better sensitivity but transistor with smaller W/L will result in lower reverse leakage current and smaller parasitic loss.

Fig. 3.26. Simulated PCE as a function of transistor sizing and load.

Fig. 3.26 shows simulated PCE as a function of transistor sizing. For a fixed load, PCE degrades with transistor sizing. For this study,

- i. NMOS sizing is fixed at $\left(\frac{W}{L}\right)_N = \frac{1}{3} \left(\frac{W}{L}\right)_P$
- ii. Input to the rectifier is a signal source with $50 \, \Omega$ series impedance
- iii. Input amplitude is fixed at $0.3 \, \text{V}$
- iv. Simulation without input matching network.

3.6.2 Coupling Capacitor

In low-power rectifier, the first-stage coupling capacitors (C_c) act like a high-pass filter. When C_c is smaller than the threshold value, RF signal will be blocked from coupling to the transistors. Fig. 3.28 shows the effect of C_c on PCE when $V_{in} = 0.5 \, \text{V}$ and $R_{load} = 5 \, \text{k}\Omega$. C_c value of $10 \, \text{pF}$ appears to be optimal choice in terms of impact on PCE and size.

Fig. 3.27. RC model of single-stage low-power rectifier.

Fig. 3.28. Effect of coupling capacitor on PCE (for $V_{in} = 0.5V$, $R_{load} = 5$ k Ω). $C_{Cl,2}$ act like high-pass filter, blocking RF signal from coupling to transistors when they are smaller than 5 pF.

3.6.3 Output Capacitor

(a)

(b)

Fig. 3.29. (a) Effect of output capacitor on PCE. (b) Effect of output capacitor on output voltage ripple.

Output capacitor (C_{load}) acts as a low-pass filter and smoothes the output voltage ripples. As shown in Fig. 3.29, C_{load} of 20pF is sufficient to provide good attenuation for output voltage ripple without compromising the PCE.

3.6.4 Input Matching Network

In real-life application, the input of harvester will be connected to an antenna (typically 50 Ω). In order to ensure maximum power transfer from antenna (source) to the harvester's input ports (load), input matching network is often required to match their impedances at the desired operating frequency. The rectifier can be modeled as a pair of parallel resistor (R_{rect}) and capacitor (C_{rect}), as shown in Fig. 3.30.

Fig. 3.30. Rectifier with equivalent parallel resistor and capacitor model for impedance and matching network calculation.

The input impedance of rectifier can be written as:

$$Z_{rect} = R_{rect} // \frac{1}{j\omega C_{rect}}, \omega = 2\pi f \quad (3.22)$$

$$= \frac{R_{rect}}{1 + j\omega R_{rect} C_{rect}}$$

The input impedance of matching network can be expressed as:

$$Z_{in} = j\omega L_{MN} + \left(\frac{1}{j\omega C_{MN}} // Z_{rect} \right) \quad (3.23)$$

$$= j\omega L_{MN} + \frac{R_{rect}}{1 + j\omega R_{rect}(C_{rect} + C_{MN})}$$

$$= \frac{[1 + j\omega R_{rect}(C_{rect} + C_{MN})](j\omega L_{MN}) + R_{rect}}{1 + j\omega R_{rect}(C_{rect} + C_{MN})}$$

$$= \frac{R_{rect}}{1 + j\omega R_{rect}(C_{rect} + C_{MN})} \left[1 + j\omega \frac{L_{MN}}{R_{rect}} - \omega^2 L_{MN}(C_{rect} + C_{MN}) \right]$$

Equating the real part of Z_{in} to R_S ,

$$R_s = \frac{L_{MN}}{R_{rect}(C_{rect} + C_{MN})} \quad , \text{ assuming } R_{rect}(C_{rect} + C_{MN}) \gg 1 \quad (3.24)$$

$$Q = \sqrt{\frac{R_{rect}}{R_s} - 1} \quad (3.25)$$

$$L_{MN} = \frac{Q R_s}{\omega_0} = \frac{R_s \sqrt{\frac{R_{rect}}{R_s} - 1}}{\omega_0} = \frac{\sqrt{R_s(R_{rect} - R_s)}}{\omega_0} \quad (3.26)$$

$$C_{MN} + C_{rect} = \frac{Q}{\omega_0 R_{rect}} = \frac{1}{\omega_0 R_{rect}} \sqrt{\frac{R_{rect}}{R_s} - 1} \quad (3.27)$$

$$C_{MN} = \left(\frac{1}{\omega_0 R_{rect}} \sqrt{\frac{R_{rect}}{R_s} - 1} \right) - C_{rect}$$

Due to nature of operation states of rectifier, its small-signal input impedance varies within single cycle of input signal. Hence, the values of L_{MN} and C_{MN} need to be fine-tune iteratively through computational or simulation to obtain the optimal values. Fig. 3.31 shows the simulated return loss of both low-power rectifier and high-power rectifier across frequencies.

(a) Low-power rectifier S_{11} (b) High-power rectifier S_{11}

Fig. 3.31 Return loss (with and without matching network) of rectifiers versus frequency with 15 k Ω load.

3.7 Automated Design Optimization using Artificial Neural Network (ANN) – Input Power and Load Optimization

For complex circuitry, iterative method to design, simulate, redesign and optimize design parameters is often being carried out to identify the best conditions (input setting, load condition, active and passive devices sizing) for optimum performance. This iteration usually consumes a lot of time if being carried out through electronic design automation (EDA) software. The optimization process is further complicated by conflicting constraint between maximum performance and device performance limitations. Larger size transistors improve circuit sensitivity but smaller size transistors introduce lower reverse leakage current and parasitic losses. For a given input power, increasing load resistance beyond optimum loading condition will cause degradation in PCE due to rectifier elements' power dissipation dominating over output power.

We propose a neural network approach complementing SPICE simulation to identify maximum PCE as the figure-of-merit (FOM). Two parameters (input power and load) optimization has been used as proof of concept. Optimization of PCE is a regression problem where the predicted output is a continuous variable. Multiple layer perception (MLP) is found to be suitable for this task. A 5-step methodology using deep learning optimization to identify PCE has been proposed:

i. Data collection

The rectifier circuit is simulated on Cadence Virtuoso to collect a series of dataset. Two variable parameters are broadly stepped during simulation to obtain the profile of circuit's PCE performance. Fig. 3.32 shows nonlinear relationship between the two parameters and maximum efficiency. A well designed dense neural network will be able to capture this nonlinear relationship between the two parameters and identify local maximum.

Fig. 3.32. Data from circuit simulation to establish rectifier performance. Circuit performance shows nonlinear relationship between input power, load resistance and PCE.

ii. Data pre-processing

Initial simulation shows that the maximum PCE is confined within the simulation boundaries. The two parameters are normalized due to the vastly difference in scale between the parameters. This step is essential to ensure subsequent training phase can complete effectively without much oscillation due to the difference in parameters range.

iii. Training

Network parameters such as amount of layers, number of nodes per layers, type of activation function and number of Epoch are adjusted to achieve high prediction accuracy. The model with finalized internal weights is validated with test data to obtain the validation loss. The comparison between training loss and validation loss will provide information if the network has been over- or under-trained.

iv. Prediction/ inference

After the training phase, the model which represent rectifier is used to generate predicted PCE based on new set of variable parameters with finer steps.

v. Verification

Based on the new set of PCE generated by neural network, the variable parameters setting which predict maximum PCE is identified. These

parameters' values are input into Virtuoso for SPICE simulation with foundry's models for cross-validation.

Fig. 3.33. DNN performance using ELU activation function. A maximum PCE of 70.1% with input power of -9 dBm and 13.79 k Ω load is predicted by ELU activation model.

Figure 3.33 shows the PCE prediction for activation function using exponential linear unit (ELU). The ELU activated model predicts maximum PCE of 70.1%, which is close to simulated value of 70.9% with an error of 0.8%. Table 3.1 compares the maximum PCE obtained from various deep neural network (DNN), Virtuoso Analog Design Environment (ADE) parametric analysis, and Virtuoso ADE GXL optimization algorithms. Parametric analysis accurately represents the circuit performance based on model file but it is time consuming when the

number of variables to be simulated increases and sweep step size reduces. Virtuoso ADE GXL optimization algorithms are useful only when there is reasonable degree of confidence in the variable parameters initial value and range. For ADE GXL, different optimization algorithm, initial value and total number of steps for a fixed variable range will produce different optimal efficiency with its corresponding variable setting. ELU activated DNN is able to accurately predict maximum PCE within shorter time, and proven a plausible method to aid analog/RF circuit optimization.

Table 3.1. Comparison in maximum PCE prediction between neural network and Virtuoso optimization, with corresponding input power setting, load condition and simulation time respectively. ELU activated model predicts maximum PCE, with its corresponding input power and load settings, which is closest to simulated value with an error of 0.8% within shortest time.

Platform	Method	Simulation/ training time	Load (k Ω)	Pin (dBm)	Predicted max. PCE (%)	Virtuoso verification (%)
Virtuoso ADE L	Parametric analysis	200 hrs	15.000	-10	-	69.5
Neural network	ELU	39.80 sec	13.790	-9	70.1	70.9

Platform	Method	Simulation/ training time	Load (k Ω)	Pin (dBm)	Predicted max. PCE (%)	Virtuoso verification (%)
Virtuoso ADE GXL	BFGS	98.69 sec	4.898	-7	-	51.2
Virtuoso ADE GXL	Conjugate gradient	136.01 sec	15.00	-12	-	65.2
Virtuoso ADE GXL	Brent- Powell	98.09 sec	3.500	-1	-	54.4
Virtuoso ADE GXL	Hookie- Jeeves	76.81 sec	6.055	-9	-	50.4

CHAPTER 4 DESIGN ROBUSTNESS

In order to study the robustness of proposed work, the energy harvester design has been simulated across all process corners, industrial operating temperature range (which encompass commercial temperature grade) and different operating frequency.

4.1 Process Variations

Process corners refer to the extremes of variation in fabrication parameters. The five possible process corners are typical (TT), slow-slow (SS), fast-fast (FF), slow-fast (SF) and fast-slow (FS). Fig. 4.1 illustrates the impact of process corners on transistor's threshold voltage.

Fig. 4.1. Transistor threshold voltage variation across process corners [79].

(a) Low-power rectification

(b) High-power rectification

Fig. 4.2. PCE versus P_{in} for all process corners at 2.45 GHz and 15 k Ω load. (a) PCE for low-power rectification path. Maximum delta in PCE across process corners is -1.7 % (worst case: FS corner) at -10 dBm input power. (b) PCE for high-power rectification path. Maximum delta in PCE across process corners is -4.3 % (worst case: SF corner) at 1 dBm input power.

Table 4.1. PCE for all process corners at 2.45 GHz and 15 k Ω load.

Rectifier path	Process corner	PCE
Low-power path @ $P_{in} = -10$ dBm	SS	72.5%
	SF	72.5%
	TT	72.2%
	FS	70.5%
	FF	71.6%
High-power path @ $P_{in} = 1$ dBm	SS	60.1%
	SF	57.6%
	TT	61.9%
	FS	63.4 %
	FF	61.1%

The proposed energy harvester circuit is optimized at 25⁰C in typical (TT) condition. This circuit is simulated across different process corners (with global process variations defined by random distributions) to evaluate impact of process variations on the circuit performance. Fig. 4.2 shows the rectifiers simulated PCE as a function of P_{in} for all process corners at 2.45 GHz and 15 k Ω load. As observed from Fig. 4.2(a), the PCE of low-power rectification path is relatively consistent across process corners for $P_{in} = -10$ dBm; the lowest maximal PCE obtained is 70.5% for FS corner (TT optimized design evaluated in FS). For high-power rectification path, the lowest maximal PCE obtained is 57.6% for SF corner (TT optimized design evaluated in SF) as presented in Figure 4.2(b). Table 4.1

summarizes the corners' simulated PCE at input power setting which contributes to maximum PCE in TT corner.

4.2 Temperature

Fig. 4.3. Plots illustrating temperature dependency of MOSFET parameters (threshold voltage, leakage current, drain-to-source ON resistance, and drain current) [80].

Besides room temperature (25°C), the proposed work is simulated at -40°C and 90°C to study the circuit performance under temperature stress. Fig. 4.3 illustrates the impact of temperature on MOSFET parameters (threshold voltage,

subthreshold leakage current, ON resistance, and current versus gate-source voltage).

(a) Low-power rectification path

(b) High-power rectification path

Fig. 4.4. Simulated PCE of rectifier versus temperature at different input power setting at 2.45 GHz and 15 k Ω load. (a) PCE from low-power rectifier. (b) PCE from high-power rectifier.

Fig. 4.4 illustrates the simulated PCE of energy harvester at different operating temperature. The peak PCE of low-power rectifier is not affected much by temperature variation and delta is in the range of -3.8% (at 90 °C) to 6.1% (at -40 °C). This is due to DC-boosted gate biasing circuitry regulating the gate voltage of main rectification diode and minimizing its susceptibility to temperature change. For high-power rectifier, the peak PCE is affected by temperature with delta in the range of -20.7% (at 90°C) to 5.4% (at -40°C). This is due to the way transistors are biased in this topology. As temperature increases, the leakage current predominates over forward current, causing a reduction in efficiency.

4.3 Frequency

Despite the proposed energy harvester's devices sizing are optimized for 2.45 GHz operation, it is worth assessing the circuit performance at 950 MHz since 900 MHz frequency band is also broadly used for RF energy harvesting. The original matching network is optimized for matching at 2.45 GHz. In order to minimize any mismatch when circuit operates at 950 MHz, a new L-section matching network needs to be implemented. Fig. 4.5 illustrates the simulated return loss for the proposed high-power rectifier with original matching network (optimized for 2.45 GHz) and new matching network (optimized for 950 MHz). Fig. 4.6 presents the frequency dependence of proposed harvester at 950 MHz and 2.45 GHz input frequencies. Even though the proposed design is optimized at 2.45 GHz, up to 2.6% higher peak PCE is achieved for low-power rectifier and

5.2% higher maximum PCE is achieved for high-power rectifier at 950 MHz due to reduced parasitic effects and transistor switching loss.

Fig. 4.5. Simulated return loss for the proposed high-power rectifier with matching network designed for 0.95 GHz and 2.45 GHz operating frequencies.

(a) Low-power rectification path

(b) High-power rectification path

Fig. 4.6. Rectifiers simulated PCE versus input power at 0.95 GHz and 2.45 GHz. (a) Low-power rectification path achieves 2.6 % higher maximum PCE at lower frequency. (b) High-power rectification path achieves 5.2 % higher maximum PCE at lower frequency.

CHAPTER 5 SILICON VALIDATION RESULTS AND DISCUSSIONS

The proposed energy harvester is implemented in GLOBALFOUNDRIES 65LPe 6M/1P Complementary Metal-Oxide-Semiconductor (CMOS) process. Fig. 5.1 shows the circuit layout, and Fig. 5.2 shows the chip micrograph. This chip has a total size of 1 mm^2 including the pads, with total active area occupying 0.288 mm^2 .

Fig. 5.1. Layout of proposed dual-path rectifier, which is implemented on 65LPe CMOS process.

Fig. 5.2. Chip micrograph of the proposed RF energy harvester. The chip has total size of 1 mm^2 including pads.

An evaluation board has been designed and manufactured to measure the performance of this proposed energy harvester. Fig. 5.3 shows photograph of the 4 layers rigid RO4350B laminated printed circuit board (PCB) with chip-on-board (COB), i.e. die is directly mounted and wired onto PCB.

Fig. 5.3. Prototype measurement board for the proposed RF energy harvester, which is fabricated on 4 layers rigid RO4350B.

5.1 Measurement Setup

All measurements are performed on board level. The 2.45 GHz RF input power is provided by N5182B Keysight signal generator with $50\ \Omega$ source impedance. PSPL5310R Tektronix phase-matched balun is used to convert the single-ended input signal to a pair of differential signals for the rectifier. The cables loss and balun insertion loss have been considered, and the path attenuation is measured via N9030B Keysight signal analyser. V_{OUT} is measured with MSO7104B Keysight oscilloscope, which can be modeled as a $2.2\ \text{M}\Omega$ resistance in parallel with a 12 pF capacitance.

5.2 Low-Power Rectification Path Performance

Fig. 5.4. Comparison between simulated and measured low-power rectifier V_{OUT} versus input power at 2.45 GHz with 15 k Ω load under unmatched condition (i.e. without input matching network).

Fig. 5.4 shows difference in simulated and measured V_{OUT} for low-power rectifier, as a function of input power with 15 k Ω load at 2.45 GHz under unmatched condition (i.e. without input matching network). For P_{in} less than 4 dBm, the measured V_{OUT} is lower as compared to both pre- and post-layout simulation results. This could be attributed to sensitivity of circuitry to process shift (as reflected by device electrical test data), long V_{OUT} routing path causing significant voltage drop, power loss along critical input paths, and inaccurate foundry model or un-modeled leakage current.

Fig. 5.5. Impact of wafer V_{tlin} shifts on V_{out} . The V_{tlin} values were obtained from device electrical test (ET) data, and are compared to wafer target values.

Fig. 5.5 shows the wafer V_{tlin} performance for high- V_{th} PMOS (*HVTP*), low- V_{th} PMOS (*LVTP*) and low- V_{th} NMOS (*LVTN*) as compared to wafer target values. Higher V_{tlin} for both *HVTP* and *LVTP* is found to correlate well with higher V_{OUT} .

In actual applications, input of rectifier is connected to antenna. Antenna typically has a resistance of 50 Ω . The input power received by antenna (P_{in}) with an effective area of A_E can be expressed as:

$$P_{in} = \frac{P_{Tx} G_{Tx} A_E}{4\pi R^2} \quad (5.1)$$

where G_{Tx} is the transmit antenna gain, P_{Tx} is the transmit power, and R is the separation distance between two antennas. The rectifier input impedance needs to be matched to antenna impedance through impedance matching network to ensure maximum power transfer from antenna to rectifier. The average power available at input of matching network (P_M) is given by:

$$\begin{aligned} P_M &= \frac{1}{2} Re \left(\frac{v_{in}^2}{R_A + Z_M} \times \frac{Z_M}{R_A + Z_M} \right) \\ &= \frac{1}{2} \frac{v_{in}^2 R_M}{|Z_M + R_A|^2} \\ &= \frac{v_{in}^2}{8R_A} \left(1 - \left| \frac{Z_M - R_A}{Z_M + R_A} \right|^2 \right) \end{aligned} \quad (5.2)$$

where v_{in} is the antenna peak input voltage, Z_M is the matching network input impedance and R_A is the antenna resistance. From (5.2), the available power from antenna (P_{avail}) is expressed as:

$$P_{avail} = \frac{v_{in}^2}{8R_A} \quad (5.3)$$

and the complex reflection coefficient (Γ) is presented as:

$$\Gamma = \frac{Z_M - R_A}{Z_M + R_A} \quad (5.4)$$

An RF signal source with 50 Ω impedance is deployed during measurement. Among various matching network topologies, L-section matching network is implemented because it introduces minimal losses and offers passive voltage boost of the input voltage to improve circuit sensitivity. Fig. 5.6 shows the simulated and measured S_{11} (dB) of low-power rectifier with matching network and 15 k Ω load. Fig. 5.7 presents the V_{OUT} performance before and after implementing input matching network, at 2.45 GHz with 15 k Ω load. With proper input matching network, both the simulated and measured results show good agreement over different input power settings at 2.45 GHz. For P_{in} smaller than -7.5 dBm, measured V_{OUT} is slightly lower than target. For P_{in} greater than -7.5dBm, measured V_{OUT} is slightly higher than target. Fig. 5.8 shows the output transient waveform when load is fixed at 15 k Ω . The output voltage requires around 60 μ s to rise to 0 V to 1.19 V with -8.5 dBm input power.

(a) Simulation

(b) Measurement

Fig. 5.6. S_{11} (dB) of low-power rectifier from schematic and parasitic extracted simulation, and chip measurement.

(a) Without matching network

(b) With matching network

Fig. 5.7. Effect of input impedance matching network on V_{OUT} at 2.45 GHz with 15 k Ω load. The low-power rectifier is able to achieve V_{OUT} larger than 0.4 V with input power larger than -13.5 dBm, and V_{OUT} of 1 V with input power of -9.5 dBm.

Fig. 5.8. The measured output transient response with -8.5 dBm input power and 15 k Ω load. The output voltage requires around 60 μ s to rise from 0 V to 1.19 V.

The rectifier PCE performance agrees with V_{OUT} observation from Fig. 5.7, as reflected in Fig. 5.9. The measured peak PCE is 70.4% at -5.5 dBm input power as compared to simulated peak PCE of 72.2% at -10 dBm for $R_{load} = 15$ k Ω . The delta in peak PCE between measurement and simulation is -2.62%. A post-silicon simulation has been carried out to study the impact of wafer's V_{tlin} shifts on the rectifier performance. As shown in Fig. 5.9, implementing the V_{tlin} delta based on devices' ET data on the rectifier circuit, the post-silicon simulation results agree well with measurement data. This explains the peak PCE shift is mainly due to the process shift and inaccurate foundry model which impact the rectifier operation at such low input power. Fig. 5.10 presents the output power response with respect to input power. Minimum input power of 178 μ W (i.e. -7.5 dBm) is required for 100 μ W output power.

Fig. 5.9. Comparison between simulated and measured PCE versus input power for low-power rectifier with 15 k Ω load at 2.45 GHz. Post-silicon simulations based on wafer's V_{tlin} value agrees with measured data, which explains the shift in chip's PCE performance.

Fig. 5.10. Measured output power of low-power rectifier with reference to input power at 2.45 GHz and 15 k Ω load.

5.3 High-Power Rectification Path Performance

Fig. 5.11. Comparison between simulated and measured high-power rectifier V_{OUT} versus input power at 2.45 GHz with 15 k Ω load under unmatched condition (i.e. without matching network).

The difference in simulated and measured V_{OUT} for high-power rectification path with respect to input power at 2.45 GHz with 15 k Ω load under unmatched condition (i.e. without input matching network) are shown in Fig. 5.11. Due to the insertion of voltage-aware block, $V_{OUT} \approx V_{RECT2}$ when V_{RECT2} is greater or equal to 700 mV. Although there are slight mismatches between simulated and measured performance, the V_{OUT} performance suggests high-power rectifier's robustness towards process shift and discrepancy in foundry model. Fig. 5.12 shows the simulated and measured S_{11} (dB) of high-power rectifier. With proper input matching network, both the simulated and measured V_{OUT} indicate good

agreement over different input power settings at 2.45 GHz as illustrated in Fig. 5.13. The rectifier is able to output voltage larger than 1 V with input power of -3.7 dBm and 15 k Ω load.

(a) Simulation

(b) Measurement

Fig. 5.12. S_{11} (dB) of high-power rectifier from schematic view and parasitic extracted view simulation, and chip measurement.

(a) Without matching network

(a) With matching network

Fig. 5.13. Effect of input impedance matching network on V_{OUT} at 2.45 GHz with 15 k Ω load. The high-power rectifier is able to achieve V_{OUT} larger than 1 V with input power of -3.7 dBm.

Fig. 5.14. The measured output transient response with -3 dBm input power and 15 k Ω load. The output voltage requires around 80 μ s to rise from 0 V to 1.8 V.

Fig. 5.14 shows the output transient waveform when load is fixed at 15 k Ω . The output voltage requires around 80 μ s to rise to 0 V to 1.8 V with -3 dBm input power. Fig. 5.15 presents the rectifier PCE performance. The measured maximum PCE is 56.6% at 1.3 dBm while simulated maximum PCE is 61.9% at 1 dBm. The delta in maximum PCE between measurement and simulation is -8.63%. From Fig. 5.16, minimum input power of 427 μ W (i.e. -3.7 dBm) is required for 100 μ W output power.

Fig. 5.15. Comparison between simulated and measured high-power rectifier PCE versus input power at 2.45 GHz with 15 k Ω load.

Fig. 5.16. Measured output power of high-power rectifier with reference to input power at 2.45 GHz and 15 k Ω load.

5.4 System-level Performance

Fig. 5.17. Dual-path rectifier measured PCE versus input power at 2.45 GHz and 15 k Ω load.

Besides the chip, the energy harvesting system includes two baluns, two discrete-component matching networks and discrete-component output load. Fig. 5.17 shows the overall energy harvester's measured PCE as compared to simulated performance at 2.45 GHz with 15 k Ω load. Despite the process shift, the chip is able to achieve PCE higher than 20% from -13.5 dBm to 6.3 dBm input power, which is an extended power range of 19.8 dB.

5.5 Performance Comparison

Table 5.1 summarizes the performance of proposed RF energy harvester and compares with prior works. As depicted, the proposed harvester consists of dual-

path with rectifiers utilizing DC-boosted gate bias and internal body bias, respectively. Instead of using discrete Schottky diode in [51], [81] and [82] to lower the diode forward voltage drop, the proposed low-power rectifier employs DC-boosted gate bias to compensate the transistor's V_{th} . [70] and [83] focuses on design optimization methodology for conventional cross-coupled rectifier, with [83] using discrete MPPT PMU to boost and regulate V_{OUT} . [70] achieves high PCE but it is pure circuit simulation with ideal current load. [84] consists of dual path with switch only at the input of low-power path and an additional reference path which uses same transistor type and same number of stages as per high-power rectifier. The additional reference path in [84] causes additional P_{in} consumption which impacts its PCE. It is also a challenge to design single matching network that satisfies different input impedance conditions of the two paths. The proposed energy harvester is able to achieve peak PCE of 70.4%, which is amongst the highest reported RF energy harvester PCE operating on same frequency. This work also provides comparable input power range of 19.8 dB for PCE above 20%. The total active area of this chip is 0.288 mm^2 , which is not small. However, considering the relatively large coupling capacitors used and dummy capacitors placed on layout to mitigate process impact, it is comparable to prior works.

Table 5.1. Performance comparison between this work and prior arts, in term of operating frequency, topology, number of stages, load condition, technique to improve converter efficiency, achievable PCE, PCE range, sensitivity and chip size.

	APMC '17 [51]	TMTT '19 [81]	ICCSP '18 [82]	ICECS '16 [70]	JSSC '19 [83]	TCAS '17 [84]	This work
Technology	Discrete (SMS-7630)	Discrete (SMS-7630)	Discrete (HSMS-2820)	65 nm	65 nm	65 nm	65 nm
Frequency	2.45 GHz	2.45 GHz	2.45 GHz	2.45 GHz	2.45 GHz	900 MHz	2.45 GHz
Topology	Greinacher	Greinacher + Cockcroft- Walton	Half-wave	Cross-coupled	Cross-coupled	Cross-coupled	Cross- coupled
No. of stages	1	4	1	2	1	5 + 5	2 + 6
Load condition	Resistor 20 k Ω	Resistor 20 k Ω	Resistor 235 Ω	Current sink 100 μ A	PMU	Resistor 147 k Ω	Resistor 15 kΩ

	APMC '17 [51]	TMTT '19 [81]	ICCSP '18 [82]	ICECS '16 [70]	JSSC '19 [83]	TCAS '17 [84]	This work
Techniques	T-section dual band impedance matching network	Impedance matching boost converter		Derivative- free optimization algorithm	MPPT, modelling and parasitic- aware design	Dual path, different transistor type for different path	Dual path, DC-boosted gate bias, internal body bias
Peak PCE @ $R_{load}; P_{in}$	50.7% @ 20 k Ω ; 0 dBm (simulated)	37.5% @ 20 k Ω ; 13 dBm (measured)	70.0% @ 235 Ω (simulated)	71.8% @ 100 μ A; -8.56 dBm (simulated)	48.3% @ -3 dBm (measured)	36.5% @ 147 k Ω ; -10 dBm (measured)	70.4% @ 15 kΩ; -5.5 dBm (measured)
PCE range *	20 dB	N.A.	N.A.	N.A.	N.A.	11 dB	19.8 dB

	APMC '17 [51]	TMTT '19 [81]	ICCSP '18 [82]	ICECS '16 [70]	JSSC '19 [83]	TCAS '17 [84]	This work
Sensitivity @ V_{OUT} ($R_{load} = \infty$)	N.A.	N.A.	N.A.	N.A.	-17.1 dBm @ 0.4 V	-17.7 dBm @ 1.0V	-16.0 dBm @ 0.4V; -12.0 dBm @ 1.0V
Effective area	N.A.	N.A.	N.A.	N.A.	0.000125 mm^2 **	0.048 mm^2	0.288 mm^2

* $\text{PCE} \geq 20\%$

** Estimated from figure

CHAPTER 6 CONCLUSION AND FUTURE WORKS

6.1 Conclusion

In this thesis, a 2.45 GHz dual-path wide-power-range rectifier for RF energy harvesting is presented. A novel CMOS rectifier with DC-boosted gate biasing is proposed to improve PCE at low input power. The DC-boosted biasing circuitry is small and consumes negligible power. A novel CMOS rectifier with internal body-biasing technique is proposed for operation at higher input power. A voltage aware block has been incorporated into the high-power rectification path to minimize overall chip power consumption. The schematic simulation and prototype chip measurement results show good match across various input power settings at 2.45 GHz and 15 k Ω load.

The measurement results for prototype chip of proposed circuit show that the low-power rectifier is able to achieve peak PCE of 70.4% with -5.5 dBm input power and 15 k Ω load at 2.45 GHz. The DC output voltage is 1.72 V at peak PCE. The peak PCE of 70.4% is amongst the highest reported RF energy harvester PCE operating on same frequency. The high-power rectifier is able to attain maximum PCE of 56.6% with 1.3 dBm input power and 15 k Ω load at 2.45 GHz, and the DC output voltage is 3.37 V. The proposed RF energy harvester attains PCE greater than 20% over an extensive input power range of 19.8 dBm. The proposed circuit has demonstrated its feasibility to harvest energy from surrounding environment and designated source.

6.2 Recommendation for Future Works

Deployment of Artificial Neural Network (ANN) as complement to SPICE-level simulation for energy harvester design optimization is proposed as a future research work. Traditional method of parametric analysis using Cadence Virtuoso Analog Design Environment (ADE) for circuit optimization can be highly computationally expensive. Virtuoso ADE GXL optimization algorithms (BFGS, Conjugate Gradient, Brent-Powell, Hooke-Jeeves) are useful when there is a certain degree of confidence in initial value of the parameters to be optimized. The analytical approach in [85] requires some assumption and is not a straightforward automated optimization while the derivative-free optimization algorithm in [70] requires prior knowledge on the expected trend of the parameters to be optimized. In deep learning optimization, a series of dataset for the rectifiers is collected by running simulation on Cadence. Different neural network models are under consideration for training on this dataset. Neural network parameters (number of layers, number of nodes per layers, type of activation function and number of Epoch) are adjusted to achieve high prediction accuracy. The devices' sizing, coupling capacitors, smoothing capacitor, load and input power level that result in predicted peak PCE can be cross validated on Virtuoso, and implement on subsequent tapeout. We have introduced and demonstrated the use of exponential linear unit (ELU) activated deep neural network (DNN) to identify input power setting and load condition which contributes to peak PCE on an existing rectifier (with fixed capacitors value and

transistors sizing) in [86]. The research work is extended to optimizing the rectifier, and subsequently the entire chip.

In this proposed dual-path energy harvester, the low-power rectification path and high-power rectification paths are enabled/disabled externally to facilitate the evaluation of each individual path's performance. An RF power detector to be integrated at the RF input for automatic-path selection is on conception and will be implemented in future tapeout.

The existing chip is without backgrind to prevent wafer from cracking in the event that nanoprobeing and physical failure analysis are required to debug any fault on this prototype. However, this has resulted in longer bonding wires required for connecting chip's pads to PCB, which contributes to larger parasitic along critical signal paths. In subsequent tapeout, it is recommended to thin down the die thickness for better bonding wire looping control.

APPENDIX A SIMULATION TESTBENCH AND MEASUREMENT SETUP

For board-level measurement, the input impedance matching needs to take into consideration of parasitic effects from PCB traces, bond pads and bond wires besides the input impedance of rectifier. A simulation testbench including models of parasitic components along the RF input signal path of rectifier chip has been created, with Fig. A.1 showing simulation testbench of single rectification path. The board-level elements' parasitic effects need to be taken into consideration during circuit-level simulations to minimize discrepancies between simulation and measurement.

At 2.45 GHz, the grounded coplanar waveguide PCB traces can be modeled with a 11 nH inductor in series with 0.8 Ω resistor and a 3.8 pF shunt capacitor. The coupling capacitor (C_c) of 0.5 fF between two signal traces can be estimated from [90]:

$$C_c = \frac{1}{2}(C_o - C_e) \quad (\text{A.1})$$

where C_o is the odd mode capacitance when tangent of electrical field is zero, and C_e is the even mode capacitance when tangent of magnetic field is zero.

$$C_e = C_p + C_f + C_{f'}, \quad (\text{A.2})$$

$$C_p = \frac{\epsilon_0 \epsilon_r W}{h} \quad (\text{A.3})$$

$$C_f = \frac{1}{2} \left[\frac{\sqrt{\epsilon_r}}{cZ_0} - C_p \right] \quad (\text{A.4})$$

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{re}}} [W/h + 1.393 + 0.667 \ln(W/h + 1.444)]^{-1}, \quad (\text{A.5})$$

$$W/h \geq 1$$

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \sqrt{1 + 10h/W} \quad (\text{A.6})$$

$$C_{f'} = \frac{C_f^4 \sqrt{\epsilon_0/\epsilon_{re}}}{1 + A(h/s) \tanh(10s/h)} \quad (\text{A.7})$$

$$A = \exp[-0.1 \exp(2.33 - 1.5 W/h)] \quad (\text{A.8})$$

where C_p is the parallel plate capacitance, C_f and $C_{f'}$ are the fringing capacitances, ϵ_0 is permittivity in vacuum ($\epsilon_0 = 8.85$ pF/m), ϵ_r is the PCB substrate relative dielectric constant ($\epsilon_r = 3.66$ for RO4350B), W is the width of metal trace, h is the substrate thickness, $c = 3 \times 10^8$ m/s, Z_0 is the characteristic impedance of microstrip trace, and s is the separation between two metal traces.

$$C_o = 0.5C_{os} + C_{cps} \quad (\text{A.9})$$

$$C_{os} = 4\epsilon_0\epsilon_r \frac{K(k_0)}{K(k_0')} \quad (\text{A.10})$$

$$C_{cps} = \epsilon_0 \frac{K(k')}{K(k)} \quad (\text{A.11})$$

$$k = \frac{s}{s+2W} ; k' = \sqrt{1 - k^2} \quad (\text{A.12})$$

$$k_0 = \tanh\left(\frac{\pi W}{4h}\right) \coth\left[\frac{\pi}{4}\left(\frac{W+s}{h}\right)\right] ; k_0' = \sqrt{1 - k_0^2} \quad (\text{A.13})$$

$$\frac{K(k')}{K(k)} = \begin{cases} \frac{1}{\pi} \ln\left(2 \frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right), & 0 \leq k \leq \frac{1}{\sqrt{2}} \\ \pi / \ln\left(2 \frac{1+\sqrt{k}}{1-\sqrt{k}}\right), & \frac{1}{\sqrt{2}} \leq k \leq 1 \end{cases} \quad (\text{A.14})$$

where C_{os} is the coupling strip line odd mode capacitance, C_{cps} is the coplanar strip line capacitance, $\epsilon_0 = 8.85 \text{ pF/m}$, $\epsilon_r = 3.66$ for RO4350B, $K(k)$ is the complete elliptical function, W is the width of metal trace, h is the substrate thickness, and s is the separation between two metal traces. C_{b1} and C_{b2} are 0.03 pF PCB bond pad parasitic capacitors which can be calculated from the following equation [91]:

$$C(pF) \approx \frac{0.0886\epsilon_r A}{h} \quad (\text{A.15})$$

where ϵ_r is 3.66 for RO4350B, A is the area of plane in cm^2 , and h is the substrate thickness in cm. C_{b3} and C_{b4} are the extracted parasitic capacitors of rectifier's bonding pads. A single bond wire from die to PCB can be represented with a 2 nH inductor in series with a 0.3Ω resistor [84]. Both C_{RECT} and R_{RECT} are the rectifier equivalent input impedance, L_M and C_M are the input matching network elements with their respective equivalent series resistors, C_L is the output capacitor and R_L is the load.

For board-level measurement, the input impedance of device under test (DUT) needs to be determined for matching network optimization in order to minimize impedance mismatch between the device plane and measurement plane. Fig. A.2 shows the setup s-parameter measurement. Firstly, the cables and balun are connected, and calibration is performed till the end of differential cables (i.e. cable end that is to be connected to measurement board) using the 85052D Keysight calibration kit. The calibration error terms are written into the network analyzer. Next, the s-parameter measurement is performed at the measurement

plane which includes the effect of PCB, bond wire and rectifier chip. Subsequently, s-parameter measurements are carried out on the “open” and “short” measurement boards. The “open” board is a dummy measurement board consisting all PCB traces, similar to actual prototype measurement board but without the rectifier chip. The “short” board is a dummy measurement board with input PCB traces grounded at the edge of device plane. De-embedding calculation is performed to remove effects of all elements between measurement and device planes, to obtain the rectifier chip input impedance. The de-embedding calculation can be performed in following steps:

Fig. A.1. Schematic representation of simulation testbench for single rectification path, including models of matching network, PCB traces, bond pads and bond wires parasitic elements.

(a) Calibration of cables and balun till board edge (measurement

(b) S-parameter measurement at measurement plane

Fig. A.2. S-parameter measurement setup. Measurement is de-embedded till device plane for matching network design and optimization.

(a) Setup for measuring signal loss from signal generator till end of differential cables

(b) Setup for rectifier chip measurement

Fig. A.3. Measurement setup for rectifiers' performance evaluation. (a) Setup to measure signal loss due to cables and balun. (b) Setup for measuring rectifier chip performance.

Fig. A.3 shows the measurement setup for evaluating the rectifiers' performance. The input path loss between signal generator and measurement plane (i.e. board edge), contributed by the cables losses, connectors losses and balun insertion loss, needs to be measured to obtain the actual input power supplied to the measurement board input port. Fig. A.3(a) shows the setup for measuring signal attenuation along input path.

APPENDIX B RF SIGNAL TRACES LAYOUT ON PCB

Fig. B.1. Layout of RF input traces on measurement board. G is ground pad and S is signal pad.

The RF input traces routing on measurement board is shown in Fig. B.1. The RF signal traces layout adopts grounded coplanar waveguide (GCPW) design. Although microstrip is more robust towards fabrication variations, such as

conductor/space etching variation and conductor thickness variation, GCPW has been adopted due lower radiation loss and better spurious mode suppression at high frequencies [92]-[93]. The GCPW traces have been loosely coupled (width = 20 mil, separation = 20 mil) to improve its effective dielectric constant and lower insertion loss [93]. In order to minimize the cross-talk effect of dual-path signals, the input signal traces of low-power rectifier is perpendicular to the input signal traces of high-power rectifier and they have separate ground plane.

LIST OF PUBLICATIONS AND AWARD

Peer-Reviewed Publications

- [1] W.W.Y. Lau and L. Siek, “A 2.45GHz CMOS rectifier for RF energy harvesting,” in *IEEE Wireless Power Transfer Conf. (WPTC)*, Aveiro, Portugal, May 2016, pp. 1-3.
- [2] W.W.Y. Lau and L. Siek, “2.45GHz wide input range CMOS rectifier for RF energy harvesting,” in *IEEE Wireless Power Transfer Conference (WPTC)*, Taipei, Taiwan, May 2017, pp. 1-4.
- [3] H.W. Ho and W.W.Y. Lau, “Automated design optimization for CMOS rectifier using deep neural network (DNN),” in *IEEE Wireless Power Transfer Conference (WPTC)*, London, UK, Jun. 2019, pp. 1-4.

Manuscript in Preparation for Submission for Peer-Review

- [1] W.W.Y. Lau, H.W. Ho and L. Siek, “ANN optimized design of 2.45 GHz dual-path rectifier with adjustable-offset comparator for RF energy harvesting,” *manuscript submitted to IEEE Trans. Circuits Syst.*.
- [2] W.W.Y. Lau, H.W. Ho and L. Siek, “Deep Neural Network (DNN) optimized design of 2.45 GHz CMOS rectifier with 73.6% peak efficiency for RF energy harvesting,” *manuscript submitted to IEEE Trans. Circuit Syst.*.

Award

Best Student Paper Award, *IEEE Wireless Power Transfer Conference* (2016).

Defensive Disclosure

[1] W.W.Y. Lau, “Wide-input-range CMOS rectifier for UHF RF energy harvesting/RFID,” IPCOM000261465D, Mar. 06, 2020.

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