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D-band Surface-wave Modulator and Signal Source with 40 dB Extinction Ratio and 3.7 mW Output Power in 65 nm CMOS

Yuan Liang^{1,2}, Hao Yu^{*3}, Chirn Chye Boon^{*1}, Chenyang Li¹, Dietmar Kissinger², Yong Wang^{*2}

¹School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

²IHP, Innovations for High Performance Microelectronics, Germany 15236

³Southern University of Science and Technology, China 51805

*Contact author: cccboon@ntu.edu.sg, yuh3@sustc.edu.cn, yongwang@ihp-microelectronics.com

Abstract— High extinction ratio (ER) modulator and high output power source are demonstrated in 65 nm CMOS by generating the surface-wave at D-band. By introducing sub-wavelength periodic corrugation structure, surface plasmon polariton (SPP) is established to propagate TM-mode signal with strongly localized surface-wave, significantly reducing the radiation loss at sub-THz. A high- Q surface-wave resonator is formed by periodically drilling grooves onto split ring resonator (SRR) unit-cells with interleaving placement. Modulation is realized by tuning the inner ring of the stacked SRR. A four-ways power combined fundamental 80 GHz coupled-oscillator-network (CON) is realized by incorporating the surface-wave resonator unit-cell, which is frequency doubled to 160 GHz. Measured results show that modulator achieves the best isolation and ER under the smallest area, and the proposed CON achieves high power efficiency and power density.

Keywords—CMOS oscillator, resonator, surface plasmon polariton, metamaterial, modulator, coupled oscillator network.

I. INTRODUCTION

Future Exa-scale data server requires integration of 1000 cores with high speed communication on-chip with high energy efficiency (<1 pJ/b/mm). The optical interconnects have shown good energy efficiency with reconfigurable capability [1], but it is difficult to be fully integrated in CMOS technology, furthermore the broadband electronic I/O [2] is constrained by loss and EM crosstalk at high frequencies.

To fill the gap between electronics and photonics, the THz band has attracted great attention for low power, high speed communication. Recently, we have proposed the transmission and detection of the surface plasmon polariton (SPP) [3], one special TM-polarized *surface-wave* localized onto the metal/dielectric interface. By artificially designing periodical sub-wavelength metal strips onto the metal line, or called spoof SPP, one can establish and propagate TM-mode surface wave signal between the metal and dielectric at sub-THz region. It greatly alleviates the metal skin/proximity effect, reducing radiation loss into the high conductivity substrate. As such, it is promising to utilize surface wave as signal for on-chip modulation and source generation at sub-THz. The all-surface-wave crosstalk immune I/O is proposed as shown in Fig. 1(a), where the output power of the surface-wave source

Fig. 1. (a) The proposed dual-channel sub-THz OOK crosstalk immune I/O transceiver; (b) CMOS D-band surface-wave T-line [3] and the near-field confinement result, and (c) CMOS D-band surface-wave converter [3] and the near-field conversion result.

must be strong enough for long channel non-coherent OOK transmission, and the extinction ratio (ER) of the surface-wave modulator is critical for the distinction of the transmit binary data for low BER detection. Dramatic frequency switching is achieved in a compact area by exciting the surface-wave without consuming the DC power.

Measured results show the proposed passive modulator achieves 40 dB ER at 125 GHz implemented on an area of only $40 \mu\text{m} \times 67 \mu\text{m}$. The CON achieves 6.3% tuning range, 3.7 mW peak output power and phase noise of -104.65 dBc/Hz at 10 MHz offset at 160 GHz in an active 0.053 mm^2 area. It leads to a state-of-the-art 5.5% DC-RF efficiency, 70.1 mW/mm^2 power density, FOM of -171 dBc/Hz and FOM_T of -172.7 dBc/Hz.

II. ON-CHIP SURFACE-WAVE TRANSMISSION

One dual-channel spoof surface-wave transmission line (T-line) is prototyped in Fig. 1(b) with $2.4 \mu\text{m}$ channel spacing,

Fig. 2 ((a) The closed-loop 4-ways power combined coupled oscillator network (CON); CON realized via (b) transmission line coupled [4, 6-9], and (c) magnetic coupled by transformer [5]; (d) the proposed on-chip surface-wave generator, and (e) the equivalent circuit of the proposed surface-wave CON, and (f) the proposed four-way power combined sub-THz signal source CON by the surface-wave resonator.

and a gradient groove (Fig. 2(c)) is necessary for both momentum and impedance matching. The E -field distributions in Fig. 1(b) and (c) suggests that most of the EM energy has been coupled to the surface-wave T-line and confined into periodical grooves with only a small portion reflected. The E -field component perpendicular to the propagation interface is strongly damped, demonstrating the attenuated radiation loss.

III. ON-CHIP SURFACE-WAVE GENERATION

To improve the output power and phase noise in silicon, multiple oscillator unit-cell can be coherently combined to form a coupled oscillator network (CON) [4-9] as shown in Fig. 2(a). The coupling network commonly realized by $\lambda/4$ transmission line (T-line) [4, 6-9] in Fig. 2(b) is bulky and lossy at THz. Shown in Fig. 2(c). The combined approach by transformer [5] suffers from phase/amplitude mismatches, leading to the degraded output power and phase noise.

To address the above, the surface-wave generation is proposed in Fig. 2(d), where the periodical grooves are modeled by multiple T-network unit-cell. When the grooves are face-to-face coupled, the surface-wave CON can be realized as shown in Fig. 2(e). To shrink the size of resonator in Fig. 2(d), the grooves are now drilled onto the stacked SRR with E -field coupling to the external surface-wave T-line. The completed 160 GHz CON design is depicted in Fig. 2(f), where each 80 GHz fundamental VCO is loaded by the proposed surface-wave resonator. Three layer of interleaved SRRs are stacked to obtain high- Q in exchange of reduced resonance frequency. Harmonic balance results in Fig. 3(a) and (b) imply that by biasing the single surface-wave oscillator into the boundary of voltage and current limit region with 10 mA tail current, the phase noise of 4-way power combined CON improves 9 dB. As the VCO output swing $V_o \propto I_{ss} Q \omega_o L$, the boosted Q improves output swing, and the push-push frequency doubler experiences more abrupt on/off switching. The doubler is biased via R_b to near the threshold region in which harmonics are rich. The strong 2nd harmonics current is extracted and combined at the CON geometry center.

Fig. 3 (a) The simulated Harmonic balance (HB) result of the single surface-wave oscillator, and (b) the HB result of the CON.

Fig. 4 (a) The proposed stacked-SRR based CMOS D-band surface-wave modulator, and (b) the analytical resonance frequency versus ring gap slit g and radius R .

IV. ON-CHIP SURFACE-WAVE MODULATION

The design of stacked SRR based modulator [3] is proposed in Fig. 4(a). By suppressing the surface residue current, the E -field is strongly established inside the ring slit, and switching the ring slit has significant impact on the resonance frequency, thus achieving effective modulation. In this work we arrange the MOS switches into both the upper and the lower ring to attain better ER. The dependence of resonance frequency on ring slit g and radius R is depicted in Fig. 4(b). It shows that the modulator can be sized very compact to obtain strong magnetic resonance.

V. MEASUREMENT RESULTS

Both the proposed stacked SRR-based modulator and the surface-wave CON were fabricated in 65 nm CMOS technology. Calibration is done before probing the DUTs.

Fig. 5 (a) Die photo of CMOS D-band surface-wave modulator, and (b) the D-band measurement setup.

Fig. 6 The measured S_{11} at the on-state of modulator.

Fig. 7 The measured modulator loss, isolation, ER and Q .

Fig. 8 The statistical distribution of the peak ER of modulator.

Fig. 5 shows the modulator die photo and the testing setup. The area is only $40 \mu\text{m} \times 67 \mu\text{m}$. Fig. 6 shows the measured reflection coefficient S_{11} of the modulator, which is smaller than -10 dB from 125-150 GHz. As demonstrated in Fig. 7, a strong resonance is observed at 125 GHz. The measured insertion loss and isolation at 125 GHz is 3 dB and 43 dB, respectively, implying a peak 40 dB ER. The resulting quality factor Q can be evaluated by $Q = f_0 / \Delta f_{-3\text{dB}} = 89$. To verify the robustness of the proposed modulator, the statistics of peak ER is collected by randomly measuring 36 dies. Shown in Fig.

Fig. 9 (a) Die photo of CMOS D-band signal source, and (b) the D-band measurement setup

Fig. 10 The measured output spectrum of the CON at 159.12 GHz.

8, the worst case is 33.4 dB, while the dominant case ranges from 35 dB to 38 dB.

State-of-the-art performances are summarized in Table I. The proposed modulator achieves the best isolation and ER under the smallest area without power consumption.

Fig. 9 shows the CON die photo with active area of 0.053 mm^2 and the measurement setup. The CON design burns 67 mW from a 1.2-V power supply. Fig. 10 shows the spectrum at 159.12 GHz. After calibration of all losses of total 15.7 dBm including probe losses of 4.7 dB, harmonic mixer loss of 9 dB, waveguide, connector and IF cable loss of 2 dB, the measured output power is 5.7 dBm. The reflection is illustrated in Fig. 11, implying -20 dB and below reflection loss. Therefore, the peak power is 3.7 mW, leading to the DC-to-RF efficiency of 5.5%.

Due to the limitation of instruments, the phase noise cannot be directly measured. Instead, we measure the phase noise through the spectrum in Fig. 10 and using the equation below:

$$PN = P_{\text{carrier}} - P_{\text{Noise}@10\text{MHz}} - 10\log(RBW) \quad (1)$$

With the resolution bandwidth (3 MHz) known, the measured phase noise at 10 MHz offset is -104.65 dBc/Hz . Supply noise, harmonic mixer noise, spectrum analyzer oscillator noise and acquisition time all contributes to the distortion of spectrum.

Thanks to the high- Q resonator, the CON can even start-up at 0.7 V supply, and the frequency tuning is manipulated by adjusting both varactor and the supply voltage. The measured frequency tuning is shown in Fig. 12. Wide tuning range from 156.1 to 166 GHz can be observed, equivalent to 6.3% FTR. Fig. 13 shows the output power and DC-RF efficiency over wideband. The output power >0 dBm and the DC-RF power efficiency $>2\%$ is observed. State-of-the-art performances are

Fig. 11 The measured output reflection coefficient of the CON.

Fig. 12 The measured frequency tuning range of the CON.

Fig. 13 The measured output power and the DC-to-RF efficiency.

summarized and compared in Table II. The proposed CON achieves the highest power efficiency and power density.

VI. CONCLUSION

The surface-wave modulator and surface-wave CON were designed and fabricated in 65 nm CMOS. The surface-wave is generated on-chip with low loss and high- Q for sub-THz modulation and power combining. Measurement results show that the proposed modulator achieves 40 dB extinction ratio within only $40 \mu\text{m} \times 67 \mu\text{m}$ area without power consumption. The proposed CON achieves 3.7 mW output power, 5.5% DC-RF efficiency, 6.3% FTR and -104.65 dBc/Hz phase noise at 10 MHz offset, leading to 70.1 mW/mm^2 power density, FOM of -171 dBc/Hz and FOM_T of -172.7 dBc/Hz.

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TABLE I MODULATOR PERFORMANCE SUMMARY

Ref/Parameters	[10]	[11]	[12]	[13]	[14]	[15]	This work
Type	Passive	Passive	Passive	Passive	Active	Active	Passive
Freq. (GHz)	135	110	144	60	120	140	125
Reflection(dB)	-16.3	<-15	-8.7	/	/	/	<-30
Loss (dB)	4.3	3–4	<3.6	6.6	0.1*	3*	3
Isolation (dB)	12.5	25	>19.5	33.2	18.1	42.1	43
ER (dB)	8.2	22	17.4	26.6	18.2	39.1	40
BW(GHz)	20	50	60	/	>10	10	25
Power (mW)	/	/	0	0	28	55†	0
Area (mm ²)	0.21	0.3	0.013	0.18	0.11	0.34†	0.002
CMOS Process	0.13 μm	90 nm	65 nm	90 nm	45 nm	65 nm	65 nm

*: Gain. †: with oscillator embedded

TABLE II CON PERFORMANCE SUMMARY AND COMPARISON

Ref/Parameters	[4]	[5]	[6]	[7]	[8]	[9]	This Work
Process (nm)	65	32	0.13 μm SiGe	45nm SOI	65	65	65
Frequency (GHz)	105	136	190.5	170	215	132	160
Power (dBm)	4.5	2.3	-2.1	0	5.6	5.4	5.7
PN (dBc/Hz)	-93 @1M	/	-103 @10M	/	-94.6 @1M	-104 @25M	-104.65 @10M
Efficiency (%)	5.3	5.3	0.22	1.1	4.6	2.4	5.5
FTR (%)	9.5	24	20.7	13.6	0.7	9.7	6.3
Area (mm ²)	0.228	0.28	0.64	0.56	0.08	0.13	0.053
Power density (mW/mm ²)	12.4	6.1	0.96	1.8	45.4	26.7	70.1
FOM (dBc/Hz)	-172	/	-171.8	/	-159.1	-158	-171
FOM _T (dBc/Hz)	-175	/	-169.7	/	-164.7	-154	-172.7

$$\text{FOM}_T = \mathcal{L}(\Delta f) - 20 \log \left(\frac{f_c}{\Delta f} \times \frac{\text{FTR}}{10} \right) + 10 \log \left(\frac{P_{\text{DC}}}{1 \text{ mW}} \right) - P_{\text{out}}$$

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