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A Crosstalk-immune Sub-THz All-surface-wave I/O Transceiver in 65-nm CMOS

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Abstract—A surface-wave I/O transceiver is proposed and validated at 140 GHz in 65 nm CMOS. By generating, modulating and propagating surface plasmonic signal, the all-surface-wave I/O is prototyped with crosstalk-immune owing to the sub-wavelength localization of electromagnetic wave at the metal/dielectric interface. A four-way surface-wave signal source is power-combined via coupled oscillator network. A surface-wave modulator is realized by stacking two split-ring-resonator (SRR) unit-cells with opposite placement. It is further integrated into the all-surface-wave I/O with a surface-wave transmission line and matching converter. Measured results show that the proposed dual-channel I/O delivers a localized 140 GHz surface-wave signal, demonstrating crosstalk-immune on-chip transmission by supporting 13.5 Gb/s data-rate communication with 2.6 pJ/bit power efficiency and a bit-error rate less than 10^{-12} .

Index Terms—CMOS oscillator, Terahertz, surface plasmonic wave, crosstalk, split ring resonator, modulator, coupled oscillator network, I/O transceiver.

I. INTRODUCTION

Future high-performance servers require low power yet high speed on-chip communication between memory and microprocessor cores. The data-rate is increasing for tens of Gigabit per second wireline communication, and becomes a challenge at terahertz (THz) region between electronics and photonics [1, 2]. The optical I/O [2] may have overhead of conversion and integration on silicon for short-distance on-chip communication, yet the electronic I/O [1] is constrained by loss and crosstalk beyond GHz.

The main loss of electronic signal at THz is from radiation loss in the form of crosstalk. The surface plasmonic wave is a localized EM-wave signal generated by introducing periodical groove structure on metal lines, and hence the energy is tightly confined onto the surface and dielectric interface for transmission [3]. It hence prevents the electrical field (E -field) from penetrating into silicon substrate or adjacent conductors. However, no surface-wave signal source, modulator are demonstrated with an integrated all-surface-wave I/O in CMOS.

In this paper, a surface-wave signal source and modulator are proposed with an integrated all-surface-wave I/O. The signal source is realized through magnetic coupling of four surface-wave oscillator unit-cells, using

Fig. 1. The dual-channel sub-THz on-chip surface-wave I/O comprised of a 4-way power combined surface-wave source, two SRR modulator, one surface-wave channel and receivers.

stacked split-ring-resonator (SRR). The modulator is also evolved from the stacked SRR resonator [4]. On-off switching is attained by shifting the resonance frequency through the OOK data pattern. Finally, a dual-channel 140 GHz all-surface-wave I/O is integrated in 65 nm CMOS, as shown in Fig. 1. The two surface-wave T-lines are only 2.4 μm apart. Measured results show that the surface-wave signal source achieves 6.3% tuning range, 3.7 mW peak output power (5.5% DC-to-RF efficiency) and phase noise of -105 dBc/Hz at 10 MHz offset centred at 160 GHz in an active area of 0.053 mm^2 . The surface-wave modulator achieves 3 dB insertion loss, 43 dB isolation, and 40 dB extinction ratio at 125 GHz in an active 40 $\mu\text{m} \times 67 \mu\text{m}$ area. With 2.4 μm channel spacing, the surface-wave I/O can simultaneously support 13.5 Gb/s OOK wireline communication at 140 GHz with 2.6 pJ/bit power efficiency and a bit-error rate (BER) less than 10^{-12} .

II. ON-CHIP SUB-THz COMMUNICATION WITH SURFACE WAVE SIGNAL

Surface plasmon polaritons (SPPs), commonly recognized with negative permittivity behaviour, are one

Fig. 2 (a) THz dual-channel SPP T-line in 65-nm CMOS [5] and the near-field confinement, (b) the on-chip surface-wave converter [3], (c) near field result of the converter, (d) S_{11} and crosstalk of the dual-channel SPP T-line, and (e) S_{11} and loss of the converter.

special TM-polarized wave localized onto the metal/dielectric interface [5]. It propagates in parallel with the conductors' interface, while its E -field exponentially decays perpendicularly to the metal interface. By corrugating periodical subwavelength metal strips onto the traditional transmission line, one can establish and propagate TM-mode surface plasmonic wave between the metal and dielectric at THz region.

One dual-channel spoof SPP T-line [5] is prototyped in Fig. 2(a) with only $2.4\ \mu\text{m}$ channel spacing, and a gradient groove (Fig. 2(b)) is necessary for both momentum and impedance matching [6]. E -field distribution of the proposed SPP T-line is illustrated in Fig. 2(a) and (c). It shows that most of the EM energy has been coupled to SPP T-line and confined into periodical grooves with only a small portion reflected. The E -field component perpendicular to the propagation interface is strongly damped, demonstrating attenuated radiation loss. As illustrated in Fig. 2(d), the measured insertion loss is flat from DC to beyond 325 GHz, whereas the traditional on-chip T-line suffers from strong radiation loss with $\sqrt{f}$ dependency due to the skin and proximity effects. A broadband 19-dB crosstalk reduction is experimentally observed as well at 300 GHz and beyond, as shown in Fig. 2(e). As such, it is promising to utilize SPP as signal for on-chip communication at THz.

III. SUB-THZ SURFACE-WAVE SIGNAL SOURCE

Phase noise and output power of the signal source are two critical factors in the sub-THz communication [7-11]. Fig. 3 illustrates the way to generate surface-wave signal using the magnetic SRR resonator and the 4-way power combined coupled-oscillator-network (CON). The loop is naturally a self-sustained synchronized system, where each oscillator will converge to a certain frequency at the

steady state. It has been analysed and measured that, even the mutual coupling has finite phase shift ($\Phi \neq 0$) and the coupling strength is weak ($\epsilon < 1$), the phase noise of a CON is $1/N$ times of a single oscillator [10]. As such, the phase noise of the oscillator unit-cell can be improved by using the high- Q stacked SRR, which inherently eliminates the metal surface residue current at THz. Moreover, by periodically corrugating the SRR lanes, the TM-polarized surface-wave is now coupled into the SRR core, leading to a strong resonance with low radiation loss. Note that while the two surface-wave T-line are face-to-face placed, the mutual coupling is enhanced [3]. Therefore, the low loss TM mode generated by each oscillator can be effectively coupled through the surface-wave T-line with low phase noise yet high output power. Moreover, the doubler can be biased in the subthreshold region to generate strong 2nd harmonics and combined through CON.

IV. SUB-THZ SURFACE-WAVE MODULATOR

On-chip THz communication also needs CMOS modulator. One compact modulator is evolved from the stacked SRR structure [4], as shown in Fig. 4. Four MOS switches are connected to the inner ring for frequency modulation. When the data bit is low, the carrier will be strongly rejected as normal resonance. The carrier can pass through the structure when the data bit is high, at which the MOS switches turn on and shift the SRR resonance frequency by shorting the inner ring to ground.

The motivation of stacked SRR structure can be illustrated as follows. As electrical dipoles are sensitive to skin/proximity effect, it is preferable to eliminate the electrical dipole but maintain the excitation of magnetic dipole in the resonator, which also forms a TM-mode

Fig. 3. The 4-way power combined surface-wave source.

Fig. 4. The surface-wave modulator based on stacked SRR.

Fig. 5. The die photo of the all-surface-wave I/O transceiver.

surface-wave. To achieve this, multiple SRR unit-cells can be vertically stacked inside a compact area to reinforce the excitation of magnetic field, while the E -field is established only between the slit of each ring. This can result in a high extinction ratio in a compact area that is hardly achieved by active designs [12-15].

V. SUB-THZ ALL-SURFACE-WAVE I/O TRANSCEIVER

The all-surface-wave sub-THz OOK I/O transceiver is illustrated in Fig. 1. Two 1-mm long surface-wave channels are in communication with only 2.4 μm apart.

Fig. 6 (a) The measured output spectrum at 159.12 GHz, and (b) the measured frequency tuning range of the CON.

Fig. 7 (a) The measured S_{11} at the on-state, and (b) the measured insertion loss, isolation, and ER of modulator.

The receiver is composed of one input balun, one self-mixing mixer and a cascade of baseband amplifiers. The mixer recovers the baseband signal by down-conversion and filtering out of the carrier and harmonics. The two TRx operates individually with channel crosstalk strongly attenuated. All devices in the I/O link are optimized at 140 GHz with no clock and data recovery circuit used.

VI. MEASUREMENT RESULTS

The proposed surface-wave signal source, modulator and T-line were integrated into the I/O transceiver and were fabricated in standard 65 nm CMOS process. Fig. 5 shows the die photo of each components and also the integrated I/O transceiver. All prototypes were measured in Cascade Microtech Probe Station.

Fig. 6(a) shows the measured spectrum of the surface-wave signal source optimized at 159.12 GHz. After calibration of all losses of total 15.7 dBm including: probe losses of 4.7 dB, harmonic mixer loss of 9 dB, waveguide, connector and IF cable loss of 2 dB, the measured output power is 5.7 dBm (3.7 mW). The phase noise is measured through the spectrum in Fig. 6(a). With 3 MHz resolution bandwidth, the phase noise at 10 MHz offset is -105 dBc/Hz. By tuning both the supply and varactor, the measured frequency tuning is from 156.1 to 166 GHz as shown in Fig. 6(b), equivalent to 6.3% FTR.

Fig. 7(a) shows the measured S_{11} of the passive surface-wave modulator, which is smaller than -10 dB from 125-150 GHz. Shown in Fig. 7(b), the measured insertion loss and isolation at 125 GHz is 3 dB and 43 dB, respectively, implying a peak 40 dB extinction ratio. The resulting quality factor Q can be evaluated by $Q = f_0/\Delta f_{-3\text{dB}} = 89$.

The integrated all-surface-wave I/O is measured by N4903B J -BERT and DSOZ634A oscilloscope. A 2^7-1 PRBS is used for the eye diagram and BER measurement. Fig. 8(a) and (b) demonstrates the 13.5 Gb/s data rate for single and dual channel OOK communication. The

Fig. 8 The measured (a) 13.5 Gb/s single channel OOK communication, and (b) 13.5 Gb/s dual channel OOK communication.

proposed I/O transceiver inherently suppresses the channel crosstalk. State-of-the-art sub-THz signal source and I/O transceiver performances are summarized in Table I and II.

VII. CONCLUSION

An all-surface-wave I/O transceiver is designed and measured in 65 nm CMOS. Localized surface plasmonic wave is generated, modulated and transmitted for sub-THz communication. It has been shown that the surface-wave effectively suppresses the channel crosstalk through field confinement, and the on-chip high- Q resonator can be realized by exciting the surface-wave in small area as well. Measured result shows that the proposed surface-wave I/O can support 13.5 Gb/s dual-channel communication when the channel spacing is only 2.4 μm without data recovery.

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TABLE I SUB-THz SOURCES PERFORMANCES SUMMARY

Ref./Para.	[7]	[8]	[9]	[10]	[11]	This work
Process (nm)	65	32	130 SiGe	65	65	65
Freq. (GHz)	105	136	190.5	132	215	160
Power (dBm)	4.5	2.3	-2.1	5.4	5.6	5.7
Phase Noise (dBc/Hz)	-93 @1M	/	-103 @10M	-104 @25M	-94.6 @1M	-105 @10M
Efficiency	5.3%	5.3%	0.22%	2.4%	4.6%	5.5%
FTR	9.5%	24%	20.7%	9.7%	0.7%	6.3%
Area (mm ²)	0.228	0.28	0.64	0.13	0.08	0.053
FOM	-172	/	-171.8	-158	-159.1	-171
FOM _T	-175	/	-169.7	-154	-164.7	-172.7

$$FOM_T = L(\Delta f) - 20 \log \left(\frac{I_0}{\Delta f} \times \frac{P_{TR}}{10} \right) + 10 \log \left(\frac{P_{DC}}{1 \text{ mW}} \right) - P_{out}$$

TABLE II SUB-THz OOK I/O PERFORMANCES SUMMARY

Ref./Para.	[1]	[12]	[13]	[14]	[15]	This work
Frequency (GHz)	140	135	152	210	106	140
P _{out} (dBm)	-9	-8.7	3.0	0.6	-2.3	5.7
TRx P _{DC} (mW)	235	17.9	55	240	34	51.3
Tx DC-to-RF	0.1%	0.73%	3.7%	0.48%	2.3%	5.5%
Data rate (Gb/s)	2.5	10	10	10	8.5	13.5
Bit error rate	4.1×10^{-6}	10^{-11}	10^{-12}	10^{-5}	10^{-12}	10^{-12}
Efficiency (pJ/bit)	94 [#]	1.79	5.5	12	4	2.6*
TRx Area (mm ²)	0.15	0.32	0.39	3.5	0.34	0.23*
CMOS Process	65nm	40nm	65nm	32nm	65nm	65nm

*: Single channel

#: channel loss > 40 dB

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