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2020

Beniwal, N., Townsend, C. D., Farivar, G. G., Pou, J., Ceballos, S., & Dehghani Tafti, H. (2020). Band-limited three-level modulation for balancing capacitor voltages in neutral-point-clamped converters. *IEEE Transactions on Power Electronics*, 35(9), 9739-9754. doi:10.1109/TPEL.2020.2969452

<https://hdl.handle.net/10356/139660>

<https://doi.org/10.1109/TPEL.2020.2969452>

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Band-Limited Three-Level Modulation for Balancing Capacitor Voltages in Neutral-Point-Clamped Converters

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An earlier incarnation of the work shown in this paper was presented at the IEEE Energy Conversion Congress and Exposition (ECCE) on October 2, 2019 in Baltimore, MD, USA. The name of the paper at ECCE 2019 was ‘Balancing Average Capacitor Voltages in Neutral-Point-Clamped Converters Using Band-Limited Three-Level Modulation’ [26].

Abstract—In this paper, a band-limited three-level modulation scheme is proposed for a three-phase neutral-point-clamped (NPC) converter with an aim to balance the average capacitor voltages under all operating conditions. When conventional carrier-based pulsewidth modulation is applied, the amplitude of neutral point (NP) voltage ripple tends to increase under linear imbalances, while the NP voltage can shift leading to instability in the presence of nonlinear loads. A previously proposed three-level modulation scheme was able to eliminate all low-frequency capacitor voltage ripple by switching a phase between three levels in each switching period. This approach significantly increased switching loss. The proposed modulation scheme limits the increase in switching loss by employing two operational bands, one fixed band applied to the capacitor voltages and another variable band applied to the phase currents. If the instantaneous capacitor voltages exceed the voltage band, then an appropriate phase-leg is switched in three-levels to guarantee the capacitor voltages cannot diverge further. If the instantaneous capacitor voltages reside within the voltage band, a variable current band is used to regulate switching in three voltage levels in order to obtain lower switching losses as compared to the conventional three-level modulation scheme. Therefore, the proposed modulation scheme presents a trade-off between switching losses and capacitor voltage ripple. Experimental results are obtained under different loading conditions for validating the performance of the proposed modulation scheme.

Index Terms—Carrier-based pulsewidth modulation, low-frequency neutral-point voltage ripple, neutral-point-clamped converter, three-level modulation.

I. INTRODUCTION

The neutral-point-clamped (NPC) converter, introduced in 1981 [1], is a widely employed topology. Fig. 1 shows the circuit diagram of a three-phase NPC converter feeding a linear and a nonlinear load. The main features of NPC converters are lower ac-side harmonic distortion and reduced dv/dt as compared to conventional two-level voltage source converters [2]. Various applications of NPC converters include wind power systems [3]–[5], solar photovoltaic systems [6]–[9] and ac drives [10]–[13].

However, NPC converters face many challenges [14]–[16]. The biggest issue is to balance the dc-link capacitor voltages

equally under all operating conditions. Moreover, the neutral point (NP) suffers from low-frequency voltage ripples while operating under high modulation indices and low load power factors. These low-frequency ripples are also reflected onto the ac-side of the NPC converter, degrading the ac voltages. Pou *et al.* [16] have also discussed other challenges which appear when an NPC converter feeds imbalances and nonlinear loads. Due to the presence of negative sequence currents under linear imbalances, the amplitude of the NP voltage ripple obtained is higher as compared to balanced linear loads. Under nonlinear loads, the low-frequency NP voltage ripples further increase with odd-order harmonics, while even-order harmonics can shift the NP voltage leading to instability.

Various modulation techniques have been presented in the literature to combat these challenges, which can be classified into two main categories, i.e., space-vector pulsewidth modulation (SVPWM) and carrier-based pulsewidth modulation (CBPWM). Seo *et al.* [17] developed a SVPWM technique for a three-level inverter by extending the standard two-level SVPWM without using a lookup table. However, the com-

Fig. 1. Circuit diagram of a three-phase NPC converter.

putational complexity is still high due to repeated coordinate transformations and shifting of the origin for the duty cycle calculations, which further exacerbates with increase in the number of voltage levels. A virtual SVPWM technique is presented in [18] for achieving capacitor voltage balancing at all modulation indices and power factors. However, a significant increase in the switching frequency of the power devices is the drawback. Moreover, the output voltages suffer from additional high frequency distortion. In [19], the virtual SVPWM is optimized to develop a new modulation technique, which has lower number of commutations and produces less switching loss. However, the drawback of this technique is the increase in the capacitor voltage ripples. An improved virtual SVPWM is presented in [20], which eliminates capacitor voltage ripples with reduced common mode voltages. However, the power devices still switch at higher frequencies. Many of the abovementioned modulation techniques also fail to demonstrate the NP voltage stability under nonlinear loads. For a practical NPC converter system, it is important to design a modulation technique which stabilizes the NP voltage under all loading conditions.

Other commonly employed modulation techniques are based on CBPWM. One of the first attempts in this direction was made by Ogasawara and Akagi [21]. The authors presented a standard CBPWM technique with zero-sequence addition and analyzed the NP voltage variation based on the average current flowing in or out of the NP. They also discussed the importance of adding the zero-sequence voltages for controlling the NP voltage variation. In this modulation scheme, all the phases switch only among two consecutive voltage levels in each switching period, i.e., either between the positive dc-rail and the NP rail or between the NP rail and the negative dc-rail. As a result, the observed capacitor voltages are sometimes unbalanced with this modulation scheme even after the zero-sequence voltage injection. In [22], another CBPWM technique was proposed wherein the authors used a searching-optimization and precise calculation algorithm to calculate an appropriate zero-sequence voltage to ensure the voltage balance between the dc-link capacitors. However, the observed capacitor voltage ripples are uncontrollable at high modulation indices and low power factors. Pou *et al.* [23] developed a CBPWM strategy based on zero-sequence voltage injection obtained by using a duality between the nearest three-vector space-vector modulation (NTV-SVM) and sinusoidal PWM for mitigating NP voltage oscillations. However, this strategy fails to address the issue of NP voltage stability associated with nonlinear loads. In [24], the authors presented another CBPWM based modulation technique ‘three-level modulation’ which completely eliminates the capacitor voltage ripples irrespective of the loading conditions. Though three-level modulation mitigates the NP voltage issues, the switching losses increase substantially as one of the phases is chosen to switch in three voltage levels, i.e., positive dc-rail, NP rail and negative dc-rail, in one switching period. Therefore, it is important to find a trade-off between switching losses and NP voltage ripples for an NPC converter. In order to attain such a trade-off, the authors regulated the capacitor voltage ripples within a predefined voltage band in [25] by intermittently

switching between two- and three-level modulation. A major drawback of this technique is that the capacitor voltages can ‘bounce’ along the voltage band boundaries under certain nonlinear load conditions, leading to steady-state imbalance in average capacitor voltages and more switching losses. This phenomenon arises due to the steady state differences in the average capacitor voltages. Thus, it is important to take the average capacitor voltage difference into account in order to develop an effective modulation technique for NPC converters.

An initial attempt in this direction is presented in [26], wherein a current band is defined to minimize the switching losses. However, no experimental validation was provided. Furthermore, this modulation technique fails to regulate the maximum NP voltage ripples. This paper is an extension of the work done in [26] and proposes a new band-limited three-level (BL-3L) modulation.

The proposed BL-3L modulation aims to balance the average capacitor voltages irrespective of the loading conditions without any substantial increase in the switching losses, thereby concentrating mainly on enhancing the steady state performance of the system. This scheme employs two operational bands as mentioned below:

- Fixed voltage band- Applied to the capacitor voltages. This band limits the maximum voltage across the dc-link capacitors. If any of the capacitor voltages go beyond the predefined voltage limit, one of the phases is chosen to switch in three voltage levels using three-level modulation [24]. Within the voltage band, the NP voltage ripples are allowed to remain.
- Variable current band- Applied to the phase currents. This band ensures average capacitor voltage balance by switching a phase in three voltage levels intermittently. Within the voltage band, the number of times that a phase is switched in three levels is limited by the variable current band, i.e., a phase is only switched in three-levels in sampling periods where the absolute value of the corresponding phase current is low, i.e., when the phase current resides within the current band. The size of the current band is varied based on the tendency of the operational condition to unbalance the NP, which ensures that the number of sampling periods where three-level modulation is employed is minimized.

As switching a phase in three levels is limited, the obtained switching losses are lower than the conventional three-level modulation [24]. Therefore, the proposed BL-3L modulation scheme facilitates a trade-off between voltage ripple magnitude and switching losses.

However, as the instantaneous capacitor voltages are allowed to vary within the voltage band, low-frequency distortion is produced in the ac-side voltages. For eliminating this low-frequency distortion, a feedforward compensation is employed in the proposed BL-3L modulation scheme [25]. The main benefits of the proposed modulation scheme are as follows:

- The average capacitor voltages are balanced irrespective of the loading conditions.

- The NPC converter design process is made easier as the predefined voltage band limits the maximum voltage across the switches and the dc-link capacitors.
- A variable current band is defined to limit switching in three voltage levels, thereby, reducing the incurred switching losses compared to the conventional three-level modulation.

This paper builds on the early work in [26] with addition of the following:

- Modification of how the variable current band in BL-3L modulation is calculated, such that any interaction between the multiple control loops is mitigated, which subsequently improves capacitor voltage balancing performance.
- A more detailed description of the proposed algorithm, including step-by-step flow charts that describe how the variable current band is calculated.
- Integration of the proposed BL-3L concept with feedforward modulation [25] to improve harmonic performance.
- Integration of the proposed BL-3L concept with a fixed voltage band [25] that ensures instantaneous capacitor voltages cannot exceed a maximum / minimum value.
- Comparison between the proposed scheme and the author's previously proposed scheme in [25].
- Extensive experimental confirmation of the proposed approach.

The rest of this paper is organized as follows. Section II presents a brief review to the two- and three-level modulation techniques. Section III explains the steps involved in the proposed band-limited three-level modulation. To validate the performance of the proposed modulation technique, experimental results are presented in Section IV. Section V summarizes the main conclusions of this work.

II. REVIEW OF TWO- AND THREE-LEVEL MODULATION TECHNIQUES

As discussed in the previous section, many CBPWM techniques [21]–[24] have been developed using different zero-sequence additions. In this paper, a standard CBPWM with min-max based zero-sequence voltage injection is utilized for comparison with the proposed strategy, and is subsequently referred to as two-level modulation [24]. Under this modulation technique, all the phases switch in two consecutive levels, i.e., either they switch between the positive dc-rail and NP rail or between the negative dc-rail and NP rail, in each switching period. Consider that v_{aREF} , v_{bREF} and v_{cREF} are the phase voltage references to be generated. Firstly, these voltage references are normalized ($v_{in} \in [-1, 1]$) as shown below:

$$v_{in} = \frac{v_{iREF}}{V_{dc}/2} \quad \text{for } i = \{a, b, c\}, \quad (1)$$

where, V_{dc} is the total dc-link voltage. A min-max based zero-sequence voltage is added to these normalized voltage references in order to extend the linear modulation region and to fully utilize the dc-link voltage,

$$v_i = v_{in} + v_{offm} \quad \text{with } i = \{a, b, c\}, \quad (2)$$

where,

$$v_{offm} = -\frac{\max(v_{an}, v_{bn}, v_{cn}) + \min(v_{an}, v_{bn}, v_{cn})}{2} \quad (3)$$

The obtained normalized phase voltages with zero-sequence addition are then utilized to calculate the NP duty cycles. The duty cycle for the i^{th} phase connecting to NP, switching with two-level modulation, is given by [21], [24]:

$$d_{NP_i} = 1 - |v_i| \quad \text{with } i = \{a, b, c\}. \quad (4)$$

The duty cycle for the i^{th} phase connecting to the negative dc-rail is calculated as:

$$d_{li} = \frac{1 - d_{NP_i} - v_i}{2}. \quad (5)$$

Similarly, the duty cycle for i^{th} phase connecting to the positive dc-rail is given by:

$$d_{hi} = 1 - d_{NP_i} - d_{li}. \quad (6)$$

Accordingly, the NP current over a switching cycle is averaged as:

$$i_{NP} = d_{NP_a} i_a + d_{NP_b} i_b + d_{NP_c} i_c, \quad (7)$$

where i_a , i_b and i_c represent the three-phase currents.

The tendency of the average capacitor voltages to diverge under two-level modulation is dependent on the loading conditions. Under linear load, the average capacitor voltages are balanced, however, they can become unbalanced under nonlinear loads.

Lopez *et al.* [24] presented a modulation algorithm that is able to balance the instantaneous capacitor voltages by switching one phase in three levels when required. Switching a phase in three levels implies that the phase will switch among the positive dc-rail, NP and negative dc-rail in a switching period. This technique also incorporates the same min-max zero-sequence voltage injection. The NP current is predicted using (7), assuming all the phases switch in two levels. The reference NP current, which is required to achieve capacitor voltage balance after one switching period, under three-level modulation is calculated as:

$$i_{ref3L} = 2C \frac{(v_{C1} - \frac{V_{dc}}{2})}{T_s}. \quad (8)$$

Here, C is the value of each dc-link capacitance, v_{C1} is the voltage of lower dc-link capacitor, and T_s is the switching period. Depending on the values of i_{NP} and i_{ref3L} , it is decided whether all the phases will switch in two levels, or one of them will be chosen to switch in three levels. Assume, phases ' l ' and ' m ' are switching in two levels (their NP duty cycles will be calculated using (4)) and phase ' p ' is switching in three levels, then, the NP duty cycle for phase ' p ' connected to NP is given by [24]:

$$d_{NP_p} = \frac{i_{ref3L} - d_{NP_l} i_l - d_{NP_m} i_m}{i_p}. \quad (9)$$

The duty cycles for all the phases connecting to negative dc-rail and positive dc-rail are same as (5) and (6), respectively.

Three-level modulation has the capability to balance the instantaneous capacitor voltages irrespective of the loading

conditions. However, the major drawback is the substantial increase in the switching losses, which results due to the large number of switching periods where switching between three voltage levels occurs.

III. PROPOSED MODULATION TECHNIQUE

The proposed technique aims to balance the average, rather than instantaneous, capacitor voltages under all loading conditions. A voltage band is defined for limiting the maximum voltage across the dc-link capacitors. If any of the capacitor voltages go beyond the defined voltage limit, one of the phases is chosen to switch in three voltage levels using three-level modulation [24]. Within the voltage band, the NP voltage ripples are allowed to remain while the average capacitor voltages are balanced. In addition to the voltage band, a variable current band is also defined which restricts phases switching in three levels only to those instants when the absolute value of their corresponding phase current resides within the current band. Moreover, feedforward compensated duty cycles are incorporated to eliminate the effect of capacitor voltage imbalances on the ac-side voltages.

The step-by-step procedure for the proposed technique is shown in Figs. 2-4 and is explained below:

- **Step-I. Calculation of the reference NP current**

As the proposed technique aims to balance the average voltage of the two capacitors, the reference NP current is calculated as (Fig. 2):

$$i_{ref_{BL}} = C \frac{v_{C1} - v_{C2}}{T_s}, \quad (10)$$

Fig. 2. Calculation of NP current and its reference.

where, v_{C1} and v_{C2} represent the voltage of lower and upper dc-link capacitors, respectively. $v_{C1} - v_{C2}$ represents the average of the difference between the capacitor voltages and is obtained by using a low pass filter with a cut-off frequency of $(0.1f)$ Hz, where f is the ac-side frequency.

- **Step-II. Calculation of the NP current**

As opposed to the two- and three-level modulation techniques, the offset voltage added to the normalized reference voltages under BL-3L modulation comprises of two components,

- Min-max zero-sequence voltage (v_{off_m})

For completely utilizing the dc-link voltage, v_{off_m} as calculated in (3), is added to the normalized reference voltages.

- Capacitor voltage offset

The second component for the offset voltage is calculated using the capacitor voltage difference and is given by:

$$v_{off_c} = \mp \frac{v_{C1} - v_{C2}}{V_{dc}}. \quad (11)$$

The negative sign of v_{off_c} is used when the converter is operating as an inverter and positive sign is used during the rectifier operation.

The two offsets are added to the reference normalized phase voltages (v_{in}) as shown below:

$$v_i = v_{in} + v_{off_m} + v_{off_c} \quad \text{with } i = \{a, b, c\}. \quad (12)$$

The v_{off_c} term helps in enhancing the capacitor voltage balancing capability, by ensuring that the converter only switches between three voltage levels in a switching period when absolutely necessary. The obtained normalized voltages with added offsets are used to obtain new duty cycles using (4)-(6). These duty cycles have been derived assuming that both the capacitor voltages are equal to half of dc-link voltage. However, as the instantaneous capacitor voltages (v_{C1} and v_{C2}) are not equal while operating with the proposed modulation technique, the duty cycles need to be compensated for producing the correct reference voltage signal and thereby avoiding low-frequency distortion in the ac-side voltages. The feedforward compensated duty cycle for connecting phase 'i' to the positive dc-rail is given as [25]:

$$d'_{hi} = d_{hi} \frac{V_{dc}/2}{v_{C2}} \quad \text{with } i = \{a, b, c\}. \quad (13)$$

Similarly, the feedforward compensated duty cycle for connecting phase 'i' to the negative dc-rail is given as [25]:

$$d'_{li} = d_{li} \frac{V_{dc}/2}{v_{C1}}. \quad (14)$$

The feedforward compensated NP duty cycle for phase 'i' is calculated as:

$$d'_{NPi} = 1 - d'_{hi} - d'_{li}. \quad (15)$$

Fig. 3. Calculation of variable current band.

Fig. 4. Flowchart diagram of the proposed band-limited three-level modulation.

The adjusted average NP current over a switching period is then calculated as (Fig. 2):

$$i_{NP} = d'_{NP_a} i_a + d'_{NP_b} i_b + d'_{NP_c} i_c. \quad (16)$$

The obtained feedforward-adjusted duty cycles after the addition of the offset zero-sequence voltage has the tendency to balance the average capacitor voltages, and is the only balancing mechanism that is required under balanced linear loads. However, under unbalanced linear loads and nonlinear loads, the capacitor voltage offset is insufficient to regulate the maximum capacitor voltages, as will be shown in Section IV.B. and Section IV.C. An additional 'push' is still required to achieve voltage balance under these operational conditions, which is obtained by switching one of the three phases in three levels. Unlike three-level modulation, in the proposed modulation technique if the capacitor voltages are within the predefined voltage band, switching a phase in three levels is prohibited unless its current is within the calculated variable current band, thereby, incurring lower switching losses over the former.

- *Step-III. Calculation of the variable current band*

Fig. 3 shows the calculation of the variable current band using two controller feedback loops, which is explained next.

- In the first controller feedback loop, the difference between the two capacitor voltages (v_{C1} and v_{C2}) is fed to a low pass filter (with cut-off frequency of $0.1f$ Hz) for obtaining the average voltage difference. If the calculated difference is large, the band limit will increase consequently, increasing the probability of switching a phase in three-levels and thus, helping to balance the average capacitor voltages. It is noted that the necessary use of the absolute value of the average capacitor voltages (as the current band cannot be negative) precludes use of an integral component to eliminate steady state error.

- A second controller feedback loop is required to remove the steady state error by eliminating the dc component of the NP current, which causes divergence of the average capacitor voltages.

This is achieved by using the second control loop to force the average of the NP current (i_{NP}) calculated in (16) to be equal to the average NP current which no longer flows to the NP due to switching periods in which three-level modulation is applied via the variable current band ($\bar{i}_{NPp}$). Suppose phase 'p' is chosen to switch in three levels as it has the tendency to compensate the NP current in the right direction and its current is within the current band. The contribution of phase 'p' to NP current (i_{NPp}) that no longer flows to the NP is calculated using (13)-(15), as follows:

$$i_{NPp} = d'_{NP_p} i_p. \quad (17)$$

The phase switching in three levels is decided using reference NP current ($i_{ref_{BL}}$) and NP current (i_{NP})

(as will be discussed in Step IV). If the average of i_{NP} is equal to the average of i_{NPp} (the current that is no longer injected into the NP), then there is no average current that unbalances the NP. The $\bar{i}_{NP}$ and $\bar{i}_{NPp}$ are obtained by low pass filtering (with cut-off frequency of $0.1f$ Hz) (16) and (17), respectively.

Calculating the variable current band using the above-mentioned feedback loops restricts the number of switching periods where switching in three levels occurs. Consequently, this reduces the switching losses while still provides the additional push required to balance the average capacitor voltages.

- *Step-IV. Calculation of feedforward compensated duty cycles*

Depending on the values of v_{C1} , i_{NP} , $i_{ref_{BL}}$, $i_{ref_{3L}}$ and the voltage/current band limits, it is decided whether all the phases will switch in two levels, or one among them will be chosen to switch in three levels as shown in Fig. 4 and explained below :

- 1) Case-I. If ($v_{C1} > V_{Cmax}$) or ($v_{C1} < V_{Cmin}$)

Here, V_{Cmax} and V_{Cmin} are the capacitor voltage limits defined to restrict the voltage ripples on the dc-link capacitors. When the capacitor voltages go beyond the predefined limits, three-level modulation [24] is applied and a phase is chosen to switch in three levels depending on the values of $i_{ref_{3L}}$ and i_{NP} , as shown in (9). These predefined capacitor voltage limits not only help in limiting the voltage stress on the capacitors but also enhance the transient balancing response of the system. Unlike [24], the duty cycles are feedforward compensated in the proposed modulation technique. The feedforward compensation helps in avoiding low frequency distortion in the ac voltages due to capacitor voltage imbalances [25]. For the phases switching in two levels, the feedforward duty cycles are calculated as (13)-(15). Assuming phases 'l' and 'm' are switching in two levels, and phase 'p' is switching in three levels, the feedforward compensated NP duty cycle for phase 'p' is calculated as [25]:

$$d'_{NP_p} = \frac{i_{ref_{3L}} - d'_{NP_l} i_l - d'_{NP_m} i_m}{i_p}. \quad (18)$$

The feedforward compensated duty cycle for connecting phase 'p' to the positive dc-rail is given by [25]:

$$d'_{hp} = \frac{v_p}{2} + \frac{(1 - d'_{NP_p})v_{C1}}{V_{dc}}, \quad (19)$$

and the feedforward compensated duty cycle for phase 'p' connected to the negative dc-rail is calculated as [25]:

$$d'_{lp} = 1 - d'_{hp} - d'_{NP_p}. \quad (20)$$

Under this case, as the phases are switching according to the three-level modulation, the value of i_{NPp} is 0.

- 2) Case-II. If $(V_{Cmin} \leq v_{C1} \leq V_{Cmax})$ and $(i_{NP} \times i_{refBL}) > 0$ and $|i_{NP}| \leq |i_{refBL}|$

As the capacitor voltages are below the voltage stress limits, and the NP current is in the same direction as the reference NP current, no additional action is required. All the phases are chosen to switch in two levels and their feedforward compensated duty cycles are calculated using (13)-(15). In this case, as all the phases are switching in two levels, the value of i_{NPp} is 0.

- 3) Case-III. If $(V_{Cmin} \leq v_{C1} \leq V_{Cmax})$ and $(i_{NP} \times i_{refBL}) < 0$

In this case, the direction of NP current is opposite to the direction of the required NP current. As a result, one of the phases is required to switch in three levels. The prerequisite for a phase switching in three levels is that its phase current is within the calculated variable current band limit. The absolute values of the phase currents are compared to the current band one-by-one. The phases lying within the current band are then tested if they have the capability to compensate the NP current in the required direction. Suppose phase 'p' has a phase current within the band, then $d'_{NPp}=0$ in (16) and the new i'_{NP} is calculated. If $(i'_{NP} \times i_{refBL}) > 0$ or $(i'_{NP} \times i_{refBL}) < 0$ such that $|i'_{NP}| < |i_{NP}|$, then phase 'p' is allowed to switch in three levels. If there are more than one phase satisfying these conditions, the phase with lower value of phase current is chosen to switch in three levels. On the other hand, if no phase satisfies these conditions, all phases switch in two levels. Eqs. (13)-(15) are utilized to calculate the feedforward compensated duty cycles for the phases switching in two levels. Suppose phase 'p' is chosen to switch in three levels, while phases 'l' and 'm' switch in two levels, the feedforward duty cycle for phase 'p' connecting to NP is calculated as [25]:

$$d'_{NPp} = \frac{i_{refBL} - d'_{NP_l} i_l - d'_{NP_m} i_m}{i_p}. \quad (21)$$

Using the value of d'_{NPp} calculated above, the feedforward compensated duty cycle for connecting phase 'p' to the positive and negative dc-rails are calculated from (19) and (20), respectively. The i_{NPp} contribution of phase 'p' switching in three levels for determining the band is calculated using (13)-(17).

- 4) Case-IV. If $(V_{Cmin} \leq v_{C1} \leq V_{Cmax})$ and $(i_{NP} \times i_{refBL}) > 0$ and $|i_{NP}| > |i_{refBL}|$

As the magnitude of the NP current is greater than the required NP current, one phase is required to switch in three levels to reduce i_{NP} magnitude lower than i_{refBL} . Similar to Case-III, firstly, the phases below the variable current band are selected. Then, the phases are tested if they can compensate the NP current magnitude in the required manner. Let's suppose, phase 'p' has a phase current within

TABLE I
EXPERIMENTAL PARAMETERS

Parameter	Value
DC-link capacitors (each), C	130 μ F
DC-link voltage, V_{dc}	300 V
AC-side frequency, f	5 Hz
Carrier frequency, f_s	2 kHz
Voltage band limit, $[V_{Cmax}, V_{Cmin}]$	[165V, 135V]

the band, imposing $d'_{NPp}=0$ in (16), the new i'_{NP} is calculated. If $(|i'_{NP}| < |i_{refBL}|)$ or $(|i'_{NP}| > |i_{refBL}|)$ such that $|i'_{NP}| < |i_{NP}|$, then phase 'p' is suitable for switching in three levels. If there are two phases which are suitable, the phase with lower phase current is chosen to switch in three levels. On the other hand, if no phase satisfy these conditions, all phases will continue switching in two levels. The feedforward compensated duty cycles for phases switching in two levels are calculated using (13)-(15), while for the phase switching in three levels are calculated using (21) and (19)-(20). The i_{NPp} contribution of phase 'p' switching in three levels required for the band calculation is evaluated using (13)-(17).

The obtained duty cycles are then compared to a triangular carrier signal for generating the switching pulses for the NPC converter, using CB1 PWM from [27].

IV. EXPERIMENTAL RESULTS

To validate the performance of the proposed BL-3L modulation technique, different experimental tests are performed on a hardware prototype, shown in Fig. 5. The experimental parameters are listed in Table I. The ac-side frequency utilized is 5Hz in order to attain noticeable voltage ripples with the available dc-link capacitors in this experimental setup.

A. Balanced Linear Loading Condition

A balanced star-connected RL load is connected to the three-phase NPC converter with S open in Fig. 1, such that

Fig. 5. Picture of the hardware prototype.

Fig. 6. Balanced linear load operating at $m = 1$ under: (a) two-level modulation and (b) three-level modulation.

Fig. 7. Balanced linear load operating with BL-3L modulation at m : (a) 1, (b) 0.7, and (c) 0.4.

$R = 25\Omega$ and $L = 6.3\text{mH}$. Fig. 6 shows the waveforms of line-to-line voltage (v_{ab}), capacitor voltages (v_{C1} and v_{C2}) and load currents (i_a , i_b and i_c) at modulation index $m=1$, using two-level and three-level modulation techniques. Under balanced linear load with two-level modulation, the average capacitor voltages are balanced as observed in Fig. 6(a). From Fig. 6(b), it is clear that when three-level modulation [24] is applied, the low-frequency capacitor voltage ripples are completely eliminated. Fig. 7 shows the same waveforms and the variable current band at different modulation indices operating with the proposed BL-3L modulation. From these figures, it is clear that the average of the capacitor voltages is equal irrespective of the modulation index and also, the voltages lie within the predefined voltage band, i.e. [165V, 135V], unlike the case of two-level modulation. As the average difference between the two capacitor voltages is very small, the obtained variable current band is also very small, thereby, limiting the switching in three-level modulation to very few instants.

B. Linear Unbalanced Loading Condition

Under linear imbalances, negative sequence currents are present which lead to additional NP voltage ripples in comparison to balanced linear loads [16]. Fig. 8 shows the same waveforms when the star-connected RL load has a load imbalance,

such that $R_{a,b} = 25\Omega$, $R_c = 50\Omega$ and $L_{a,b,c} = 6.3\text{mH}$ operating under two-level and three-level modulation techniques. As expected, under two-level modulation, the capacitor voltages show additional voltage ripples, while the capacitor voltages are balanced under three-level modulation [24]. Fig. 9 presents the same waveforms along with the variable current band while feeding the same linear unbalanced load. From the figures, it is clear that the average capacitor voltages are balanced within a fundamental period. Also, the obtained NP voltage ripples are limited within the voltage band, i.e. [165V, 135V], under all cases.

C. Nonlinear Loading Condition

Fig. 10 shows the same waveforms when switch S is closed such that the NPC converter feeds a combination of a balanced linear ($R = 25\Omega$ and $L = 11.3\text{mH}$) and a nonlinear load under two-level and three-level modulation techniques. The nonlinear load is constituted by a half-bridge diode rectifier feeding a resistor ($R_s = 104\Omega$) resulting in harmonic currents enriched in second harmonics. As observed in Fig. 10(a), the average capacitor voltages are unbalanced while operating with two-level modulation. The capacitor voltages are balanced even in the presence of nonlinear load under three-level modulation. Fig. 11 shows the results of the same

Fig. 8. Linear unbalanced load operating at $m = 1$ under: (a) two-level modulation and (b) three-level modulation.

Fig. 9. Linear unbalanced load operating with BL-3L modulation at m : (a) 1, (b) 0.7, and (c) 0.4.

case study with the proposed variable current band operating under the proposed BL-3L modulation technique feeding the same load at different modulation indices. It is clear that the average capacitor voltages are balanced even in the presence of nonlinear load and lie within the predefined voltage band [165V, 135V] under all modulation indices.

D. Initial Capacitor Voltage Imbalance

Fig. 12 shows the performance under two- and three-level modulation when an initial imbalance is forced, such that $V_{C1} = 200V$ and $V_{C2} = 100V$, while feeding the same nonlinear load as in *Case C*. The two-level modulation fails to balance the average capacitor voltages and the obtained capacitor voltages show large ripples. On the other hand, with three-level modulation, the capacitor voltages are balanced in the steady state. Fig. 13 shows the results of the same case study with the variable current band when the proposed BL-3L modulation technique is applied under initial capacitor voltage imbalance. As the initial imbalance is greater than the predefined voltage band limit, i.e. [165V, 135V], the proposed BL-3L modulation technique operates as three-level modulation [24] all the time until the capacitor voltages reach the voltage band. As the bandwidth of the loop responsible for regulating the current band is low (due to presence of low pass filter), the transient

response is relatively slow. However, in steady state (which is the targeted case for which the variable current band has been designed), the average capacitor voltages are balanced and the obtained capacitor voltages lie within the predefined voltage band.

E. Distortion Analysis

Fig. 14 shows the harmonic spectra of the line-to-line voltage (v_{ab}) obtained under two-level modulation, three-level modulation and the proposed BL-3L modulation technique with two different voltage bands operating with balanced linear load. The total harmonic distortion (THD) obtained under three-level modulation is higher when compared to two-level and both the cases of BL-3L modulation. The THD obtained with three-level modulation [24] is higher due to the presence of larger high-frequency components resulting from switching one of the three phases in three voltage levels frequently within a fundamental period. In Fig. 14(a), low-frequency components are observed near the fundamental component of v_{ab} , i.e., between 0 and 100 Hz due to capacitor voltage imbalances. As a result, the obtained weighted total harmonic distortion (WTHD) for two-level modulation is higher. Under BL-3L modulation technique, no such low-frequency components are observed even in the presence of

Fig. 10. Nonlinear load operating at $m = 1$ under: (a) two-level modulation and (b) three-level modulation.

Fig. 11. Nonlinear load operating under the proposed BL-3L modulation at m : (a) 1, (b) 0.7, and (c) 0.4.

Fig. 12. Initial capacitor voltage imbalance at $m = 1$ under: (a) two-level modulation and (b) three-level modulation.

Fig. 13. Initial capacitor voltage imbalance using BL-3L modulation at m : (a) 1 and (b) 0.7.

Fig. 14. Harmonic spectra of v_{ab} at $m=1$ with (a) two-level modulation, (b) three-level modulation, (c) proposed BL-3L modulation with voltage band [165V,135V], and (d) proposed BL-3L modulation with voltage band [172.5V,127.5V].

capacitor voltage imbalance. This is due to the incorporation of feedforward compensated duty cycles which eliminate the effect of capacitor voltage imbalances on the output voltages. The WTHD obtained with three-level modulation is lower as compared to two-level modulation as the harmonic spectra is constituted by high-frequency components. Moreover, it can be observed that the band-limited three-level modulation with narrow voltage band [165V,135V] shows higher THD as compared to wider voltage band [172.5V,127.5V]. This is due to the fact that with a narrow voltage band, one of the phases switches more frequently in three levels and the observed THD performance is closer to three-level modulation. As the voltage band widens, the THD performance (in the high frequency range) of the band-limited three-level modulation becomes closer to two-level modulation.

V. SIMULATION RESULTS

For comparing the performance of the proposed BL-3L modulation technique with two-level, three-level [24] and feedforward compensated modulation [25] for practical systems, different simulation tests are performed. The simulation parameters are listed in Table II.

A. Power Loss Analysis

The switching losses increase whenever a phase switches among three voltage levels within a switching period due to increased number of transitions. The main aim of the proposed BL-3L modulation technique is to balance the average capacitor voltages under all operating conditions by restricting the phases to switch in three levels to fewer instants. For benchmarking the losses under different modulation techniques, an

TABLE II
SIMULATION PARAMETERS

Parameter	Value
DC-link capacitors (each), C	5800 μ F
DC-link voltage, V_{dc}	1500 V
AC-side frequency, f	50 Hz
Carrier frequency, f_s	2.5 kHz

insulated gate bipolar transistor (IGBT) DIM1200SM17-E000 with a continuous collector current of 1200A and maximum collector-emitter voltage of 1700V is considered. Using the characteristic curves provided in the IGBT manufacturer's datasheet, the switching and the conduction losses have been calculated [28].

Fig. 15 shows the loss comparison between two-level modulation and the proposed BL-3L modulation technique at different modulation indices and load phase angles for a linear load. As with the proposed BL-3L modulation technique one of the phases switches in three voltage levels to limit the capacitor voltages within predefined limits and to balance the average capacitor voltages, the obtained switching losses are higher than two-level modulation. The conduction losses of both of techniques are almost the same as the only difference lies in the conducting device (IGBT/diode) at various instants. The total losses operating under proposed BL-3L modulation technique are higher than those obtained under two-level modulation.

In Fig. 16, the switching and total losses obtained under the proposed BL-3L modulation are lower as compared to three-level modulation under all operating conditions. This is due to the fact that switching a phase in three levels is restricted to fewer instants under the proposed BL-3L modulation technique. From Figs. 15 and 16, it is clear that the total losses obtained under the proposed BL-3L modulation lies between two- and three-level modulation, with significant dependency on power factor.

Fig. 17 presents the switching losses obtained under the proposed BL-3L modulation under different modulation indices and phase angles with different loading conditions and voltage bands. From Fig. 17, it is clear that the obtained switching losses are lower with a wider voltage band irrespective of the loading conditions. With a narrow voltage band, switching a phase in three levels happens more frequent so as to maintain the capacitor voltages between the narrow limits. From these results, it can be concluded that for narrow voltage bands, the performance of the proposed modulation moves close to three-level modulation. The equivalent switching frequency increases in such a case and the switching losses obtained are close to three-level modulation. When the capacitor voltage limits are wider, the performance is closer to two-level modulation. If the band is increased sufficiently, the proposed modulation technique exactly behaves like two-level modulation. Therefore, the proposed BL-3L modulation technique basically presents a trade-off between voltage ripple magnitude and switching losses. For achieving lower switching losses, some increased capacitor voltage ripple is required and vice

versa. Considering the switching losses obtained with voltage band [840V, 660V] in Figs. 17(a) and (b), as the voltage band is large, BL-3L modulation technique operates within the band limits. The performance with the balanced linear load is very close to two-level modulation (Fig. 15(a)), while the corresponding losses are higher with nonlinear load. This difference arises due to the variable current band. For balanced linear load, the obtained variable current band is very small and switching a phase in three levels is rare. However, with the nonlinear load, the capacitor voltages tend to diverge leading to a dc component in the NP current, thereby, increasing the variable current band. As a result, switching a phase is more prominent under nonlinear loads, thus leading to more switching losses.

B. Performance Comparison between Feedforward Compensated Modulation and the Proposed Band-Limited Three-Level Modulation

Fig. 18(a) shows the waveforms of line-to-line voltage (v_{ab}), capacitor voltages (v_{C1} and v_{C2}), load currents (i_a , i_b and i_c) and the phase switching in three-levels ($a/b/c/\text{None}$) at modulation index $m = 1$ under the modulation scheme mentioned in [25] while feeding a nonlinear load. The voltage band limit is set at [840V, 660V]. From this figure, it is clear that the feedforward compensated modulation achieves its objective of confining the capacitor voltage ripples within the predefined voltage band. However, the capacitor voltages tend to bounce along the voltage band boundaries. As the capacitor voltage reaches the band limit, one of the phases switches in three levels to keep the voltage within the band. However, the nonlinearity in the load tries to diverge the capacitor voltages more and more [16]. Due to the opposing nature of these two, the capacitor voltages keep on bouncing along the band. As a result, the switching transitions increase leading to an increase in switching losses as well. Thus, it is important to regulate the average capacitor voltages. The proposed band-limited three-level modulation aims to balance the average capacitor voltages irrespective of the loading conditions. Fig. 18(b) shows the same waveforms while operating under same loading conditions. From this figure, the importance of variable current band in balancing the average capacitor voltages is clearly visible. The capacitor voltages do not bounce along the voltage band. The main objective of adding the voltage band to the band-limited three-level modulation is to limit the maximum capacitor voltage ripples across the capacitors. Consequently providing an advantage of designing the converter beforehand. Moreover, if we look closely at Fig. 18(b), the switching transitions are fewer in comparison to Fig. 18(a). As a result, the switching losses obtained with three-level modulation are 2.13 times the switching losses obtained with BL-3L modulation under this operating condition.

C. Comparison Among Different Modulation Schemes for the Three-Phase NPC Converter

Table III sums up the comparison among two-level modulation, three-level modulation [24], feedforward modulation with

Fig. 15. Loss comparison between two-level modulation and the proposed BL-3L modulation. (a) Switching, (b) conduction, and (c) total power losses.

Fig. 16. Loss comparison between three-level modulation [24] and the proposed BL-3L modulation with voltage band [765V, 735V]. (a) Switching, (b) conduction, and (c) total power losses.

Fig. 17. Switching losses under band-limited three-level modulation operating with: (a) linear load and (b) nonlinear load.

Fig. 18. Performance with nonlinear load under: (a) feedforward compensated modulation with confined capacitor voltage ripples [25] and (b) proposed band-limited three-level modulation.

TABLE III
COMPARISON AMONG DIFFERENT MODULATION SCHEMES

	Two-Level Modulation	Three-Level Modulation [24]	Feedforward Modulation with Confined Capacitor Voltage Ripples [25]	Proposed Band-Limited Three-Level Modulation
Maximum voltage applied to the dc-link capacitors and semiconductors	It depends on the operating point (capacitor voltage ripple amplitude)	The lowest ($V_{dc}/2$)	Predefined by maximum limit (V_{Cmax})	Predefined by maximum limit (V_{Cmax})
Average capacitor voltages	Dependant on the loading conditions	Always balanced ($V_{dc}/2$)	Dependant on the loading conditions	Always balanced ($V_{dc}/2$)
Switching losses	The lowest	The highest	Much lower than three-level modulation	Much lower than three-level modulation
Operation under nonlinear loads with even harmonics	May become unstable	Always stable	Stable (Capacitor voltages can 'bounce' along the voltage band increasing switching losses)	Always stable
Low frequency distortion in the output voltages	Exist due to the low-frequency capacitor voltage ripples	No (due to absence of low-frequency capacitor voltage ripples)	No (feedforward compensated)	No (feedforward compensated)
High frequency distortion in the output voltages	The lowest	The highest	Low	Low

confined capacitor voltage ripples [25] and the proposed BL-3L modulation technique on account of different parameters. From the comparison, it is clear that the proposed BL-3L modulation technique provides a trade-off between voltage ripple magnitude and switching losses.

VI. CONCLUSION

In this paper, a band-limited three-level (BL-3L) modulation technique has been presented, which balances the average capacitor voltages irrespective of loading conditions without increasing the switching losses substantially. The main aim of the proposed BL-3L modulation is to enhance the steady state performance of the system. A voltage band has been employed in this paper to limit the maximum voltage across the dc-link capacitors and semiconductors, which gives a freedom to design the NPC converter beforehand. Within the voltage band, a variable current band is defined which restricts switching a phase in three levels to fewer instants, thereby, reducing the switching losses as compared to three-level modulation. Moreover, feedforward compensated duty cycles are utilized to mitigate the low-frequency ripples in the output voltages that occur due to capacitor voltage imbalance. The performance of the proposed BL-3L modulation technique has been tested under balanced linear, linear imbalance and nonlinear loads. Under all the loading conditions, the average capacitor voltages are balanced and the voltages adhere to the predefined voltage limits. Moreover, the obtained losses under the proposed BL-3L modulation technique lies in between the losses obtained under two-level and three-level modulation.

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