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Non-volatile Organic Transistor Memory based on Black Phosphorus Quantum dots as Charge Trapping Layer

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Abstract

High performance organic nano-floating gate transistor memory (NFGTM) has important prerequisites of low processing temperature, solution-processable layers and charge trapping medium with high storage capacity. We demonstrate organic NFGTM using black phosphorus quantum dots (BPQDs) as a charge trapping medium by simple spin-coating and low processing temperature ($< 120\text{ }^{\circ}\text{C}$). The BPQDs with diameter of $12.6 \pm 1.5\text{ nm}$ and large quantum confined bandgap of $\sim 2.9\text{ eV}$ possess good charge trapping ability. The organic memory device exhibits excellent memory performance with a large memory window of 61.3 V , write-read-erase-read cycling endurance of 10^3 for more than 180 cycles and reliable retention over 10,000 sec. In addition, we successfully improved the memory retention to ON/OFF current ratio $> 10^4$ over 10,000 sec by introducing PMMA as the tunneling layer.

Index terms: Black phosphorus, quantum dots, floating gate transistor, organic memory, solution-processed.

I. INTRODUCTION

Organic electronic devices have been considered as potential candidates for non-volatile memory applications due to their simple structure and low processing cost. Among the various organic memory approaches, flash or floating gate memories have gained wide spread popularity owing to their non-volatile type of storage, low power consumption, high-speed access, and easy integration with NOR and NAND array [1], [2]. Various kinds of charge trapping layers have been explored, including polymer electrets [3], [4], discrete metal nanoparticles [5], [6], conjugated polymer nanoparticles [7], [8], and 2D nanomaterials

such as graphene oxide sheets and molybdenum disulphide nanoflakes [9], [10]. Compared to metal nanocrystals, the utilization of semiconductor nanoparticles as the floating gate has advantages of (i) tunable bandgap through the control of quantum size effects [11], [12] and (ii) able to trap both types of charge carriers [13], [14].

Recently, black phosphorus (BP), a 2D layered material, has gained a substantial research interest for various electronic and optoelectronic devices due to its intriguing properties such as (i) layer dependent bandgap of 0.3 eV (bulk) to >2 eV (monolayer) [15], [16], (ii) ambipolar transport [17], and (iii) high carrier mobility ($\sim 1,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) [18]. Therefore, few layers of BP have been explored as both active channel and charge trapping layer in transistor configuration with program/erase ratio over 10^3 for more than 1,000 sec [17], [18], [19]. In the 0D form, BP quantum dots (BPQDs) have a higher bandgap, higher surface-to-volume ratio and more active sites than BP nanosheet [20]. BPQDs can also be facily prepared by a liquid exfoliation method [21]. There are few reports of BPQDs based memory devices [15], [16]. However, to the best of our knowledge, there are no current reports of using BPQDs as a charge trapping layer in organic thin film transistor floating-gate memory.

In this work, we demonstrated solution-processed BPQDs can serve as an effective charge trapping layer in an organic floating gate transistor memory, using poly[(5-fluoro-2,1,3-benzothiadiazole-4,7-diyl)(4,4-dihexadecyl-4*H*-cyclopenta[2,1-*b*:3,4-*b'*]dithiophene-2,6-diyl)(6-fluoro-2,1,3-benzothiadiazole-4,7-diyl)(4,4-dihexadecyl-4*H*-cyclopenta[2,1-*b*:3,4-*b'*]dithiophene-2,6-diyl)] (PFT-100) as an active organic semiconducting channel layer [22]. The nano-floating gate transistor memory (NFGTM) was electrically characterized for memory window (turn-on voltage shift), ON/OFF switching endurance cycles and change in retention over time. We also incorporated a thin layer of poly(methyl methacrylate) (PMMA) as a tunneling layer in the memory device to further enhance the retention ability.

II. DEVICE FABRICATION

BPQDs were synthesized by liquid phase exfoliation method as reported earlier [15]. Briefly, 5 mg of bulk BP was grinded in a mortar and pestle for 30 min in 4 ml of N-Methyl-2-pyrrolidone (NMP) followed by ice bath sonication for 7 hours and the resultant dispersion was centrifuged at 7000 rpm for 30 min. The supernatant containing BPQDs were then separated carefully from the bottom precipitate. Highly doped p^{++} -Si wafer with 200 nm of SiO_2 was first cleaned in acetone and isopropyl alcohol (IPA) followed by UV-ozone treatment. The synthesized BPQDs solution was spin coated onto Si/ SiO_2 wafer at 1000 rpm for 30 sec. The BPQD layer was dried at 70°C for 10 min to remove residual solvent. PFT-100 semiconductor (from 1-Materials) [22] solution was prepared in chlorobenzene (4 mg/ml). The PFT-100 film was deposited on BPQDs film through spin-coating at 1500 rpm for 60 sec ($\sim 30 \text{ nm}$ thick) and annealed on hot

plate at 120 °C for 20 min. Finally, 100 nm of gold source-drain electrodes were deposited through shadow mask by thermal evaporation (Channel length (L)/width (W): 100/300 μm). For fabrication of NFGTM devices with PMMA as tunneling layer, 1 wt% PMMA in NMP was spin coated on top of the BPQDs at 2000 rpm for 50 sec and dried at 70 °C for 10 min. The thickness of PMMA layer was ~50 nm. Control devices (without BPQDs) were fabricated using similar processes. The electrical characterization was carried out using a semiconductor analyzer (Keysight, B2912A). All electrical measurements were carried out in a nitrogen-filled glove box.

III. RESULTS AND DISCUSSION

Fig. 1a shows the transmission electron microscopy (TEM) image of the BPQDs, indicating an average diameter of 12.6 ± 1.5 nm and correlates well with the result of 13.5 nm from dynamic light scattering (DLS) measurements (Fig. 1b) [23]. Tyndall effect in the BPQDs solution was also observed as shown in Fig. 1b, inset. The bandgap (E_g) value of BPQDs was found to be ~2.9 eV, as extracted from Tauc plot of UV-Vis measurement (Fig. 1c), [21] and thus confirmed quantum size effect.

The device architecture of bottom gate top contact (BGTC) organic NFGTM device is shown in Fig. 2a. Fig. 2b shows the transfer curve of BPQDs based NFGTM device. The extracted ON/OFF current ratio, field effect mobility and turn-on voltage (V_{on}) are 1.3×10^6 , $0.07 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and 7.50 V, respectively (V_G from 20 V to -20 V at $V_D = -20$ V). The dual sweep hysteresis measurements were carried out to study the memory effect in BPQDs (Fig. 2b). The hysteresis window increased from 5.6 V to ~50 V with increasing gate bias sweep from ± 40 V to ± 80 , clearly indicating the increase of charge trapping events in BPQDs with increasing voltages [24]. On the contrary, the reference device (without BPQDs) displayed almost negligible hysteresis (Fig. 2c). When a gate pulse of +80 V was applied for 20 sec (represented as programming operation), the entire transfer curve was shifted with a positive V_{on} of 61.9 V (Fig. 2d). The device therefore exhibited a high conductance state at $V_G = 0$ V, which corresponds to ON state. This can be explained with energy band diagram in Fig. 2e [16], [22]. When a positive gate pulse is applied, electrons from lowest unoccupied molecular orbital (LUMO) of PFT-100 get injected and trapped in the conduction band (CB) of BPQDs, causing positive V_{on} shift of transfer curve. On the contrary, when a gate pulse of -80 V was applied for 80 sec (represented as erasing operation), trapped electrons from BPQD get released to PFT-100 channel and the transfer curve shifted towards its initial position, exhibiting low conductance state at $V_G = 0$ V, corresponding to OFF state [24], [25]. The memory window (ΔV_{on}) between the turn-on voltage shift after the programming and erasing operations was found to be 61.3 V.

The charge trap density in BPQDs NFGTM was calculated using the following equation [13], [14], [26];

$$n = \frac{|\Delta V_{on} \times C_i|}{e} \quad (1)$$

where n is the charge trap density per unit area, e is the element charge, C_i is gate dielectric capacitance, and ΔV_{on} is the memory window. The capacitance was measured to be 15.43 nF/cm^2 at 10 kHz . The BPQDs charge trap density was therefore calculated to be $5.90 \times 10^{12} \text{ cm}^{-2}$ which is comparable to most reported values ($1.0 \times 10^{12} \text{ cm}^{-2} - 7.2 \times 10^{12} \text{ cm}^{-2}$) for other 2D materials as charge trapping medium in organic NFGTM devices [9], [10], [24], [27]-[31]. This confirms that BPQDs is an excellent trapping medium with a large storage capacity required for high performance NFGTM.

To further evaluate device performance, the endurance cycle and retention test were carried out. Fig. 2f shows write- read-erase-read (WRER) cycle. The gate voltage sequence of $+80 \text{ V}$, 0 V , -80 V , 0 V at $V_D = -20 \text{ V}$ was maintained. The device showed good switching between ON and OFF states. For stress endurance test, the device maintained a stable ON/OFF current ratio of 10^3 for more than 180 cycles (Fig. 2g), indicating an excellent endurance characteristic. The retention of the trapped charges is another important figure of merit, shown in Fig. 2h. Gate pulse bias of $+80 \text{ V}$ and -80 V was applied for programming and erasing operations respectively. Read voltage conditions were kept at $V_G = 0 \text{ V}$ and $V_D = -20 \text{ V}$ over $10,000 \text{ sec}$. The initial ON/OFF current ratio was about 10^5 . It was observed that the device was able to maintain distinct ON and OFF state with a current ratio of about 10^2 even at $10,000 \text{ sec}$. The good retention of charges confirms that BPQDs provides deep levels to trap charges, similar to previous observations for Au nanoparticles [18]. The reason for gradual decay in ON and OFF states is most likely due to the direct contact between BPQDs and the organic semiconductor film which can lead to leakage of the trapped charges. To further improve the retention characteristics, we incorporated a tunnelling layer of PMMA between the channel and the BPQDs nanotraps. The addition of PMMA as a tunneling layer resulted in similar transistor performance and memory behaviour (Fig. 3a). For instance, the ON/OFF current ratio, field effect mobility and V_{on} are 0.8×10^5 , $0.03 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and 2 V respectively ($V_G = 20 \text{ V}$ to -20 V , $V_D = -20 \text{ V}$). We note that the PMMA tunneling layer does not severely affect the hysteresis window. We postulate that there is enough large tunneling electric field on the BPQD/PMMA layer for injecting enough charges into BPQDs [32]. For retention test, programming gate voltage of $+60 \text{ V}$ and erasing gate voltage of -60 V were applied for 20 sec and 100 sec respectively. The trapped charges in BPQDs exhibited slow relaxation characteristics, where an ON/OFF current ratio of $\sim 10^4$ is maintained over $10,000 \text{ sec}$ (Fig. 3b). Therefore, the retention of the NFGTM devices is significantly improved by incorporation of PMMA tunneling layer, as it helps to prevent the leakage of trapped charges [13], [26], [27], [33]. The extrapolation of ON-OFF retention graphs (not shown) indicates the device is expected to maintain distinguishable ON/OFF states $\sim 1.0 \times 10^2$ even after ten years.

We have also summarized the crucial parameters of the BPQDs based NFGTM and compared with some of the existing reports using various charge trapping medium (Table I). It can be seen that BPQDs based

NFGTM device is one of the promising candidate for future memory applications owing to its good charge storage capability, excellent memory window, solution processability and low-temperature processing. The operating voltage of device can be further reduced by using thinner oxide or high- k material as a gate dielectric [14].

IV. CONCLUSIONS

In conclusion, we have demonstrated organic NFGTM using solution-processed BPQDs as a charge trapping medium. The organic NFGTM displayed a large memory window of 61.3 V after writing and erasing modes, stable ON/OFF current ratio of $\sim 10^3$ for more than 180 cycles and reliable retention ability with distinct 10^2 ON/OFF states over 10,000 sec. The memory retention was further enhanced to ON/OFF current ratio of 10^4 over 10,000 sec through the incorporation of PMMA tunneling layer. Our results are encouraging and prove that BPQDs based NFGTM device is a potential candidate for future high performance organic NFGTM.

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Fig.1: (a) TEM image of BPQDs at 10 nm scale (b) BPQDs particle size distribution measured by DLS. The Tyndall effect of BPQDs suspension is shown in the inset. (c) Tauc plot from UV-Vis absorption spectrum of BPQDs.

Fig.2: (a) Schematic of bottom gate top contact NFGTM device. (b) BPQDs device transfer characteristic with varying dual gate bias sweep. (c) Transfer characteristic of reference device without BPQDs (dual sweep). (d) Shift in transfer curve after programming and erasing operation. (e) Band diagram explaining memory mechanism under positive gate bias. (f) Repeated ON-OFF cycling test by sequential gate bias. (g) Endurance cycle test. (h) Retention characteristic of the memory device. The V_D was kept at -20 V.

Fig.3: (a) Transfer characteristic of device with varying gate bias double sweeps. (b) Retention characteristic of memory device. (Read voltage: +7 V).

TABLE I

MEMORY PROPERTIES OF ORGANIC NFGTM DEVICES BASED ON DIFFERENT CHARGE TRAPPING MEDIUM (2D MATERIALS AND OTHER NANOPARTICLES).

CTM	ΔV_{on} (V)	V_P/V_E (V)	V_D (V)	N_D (cm^{-2})	Proce-ssing	T_{proc} ($^{\circ}C$)	Ref.
rGO	~9	+100/-100	NA	NA	SP	110	29
rGO/ APTES	~10	-70/+28	-40	NA	NSP	180	30
GO	20	+80/-30	-20	NA	NSP	120	9
GO	6	-25/+25	-6	3.8×10^{12}	SP	210	31
GO	~24	+80/-30	-20	NA	NSP	200	27
GQDs	35	+60/-40	-20	7.2×10^{12}	NSP	120	24
MoS₂	~23	+80/-80	-30	NA	SP	150	10
MoS₂/ PS-NH₂	20	-50/+50	10	1.0×10^{12}	SP	NA	28
MoSe₂/PS- NH₂	5	-50/+50	10	NA	SP	NA	28
WS₂/ PS-NH₂	11	-50/+50	10	NA	SP	NA	28
CuPc/ PS₄	21	-50/+50	-50	NA	NSP	100	34
CdSe/ ZnS	58	+40/-40	-40	5.7×10^{12}	NSP	180	13
Polyfluore ne	~23	+50/-50	-30	4.8×10^{12}	NSP	50	7
Au	51.7	-80/+80	30	NA	NSP	110	35
Cu	22.4	-80/+80	30	NA	NSP	110	35
Ag	29.1	-80/+80	30	NA	NSP	110	35
BPQDs	61.3	+80/-80	-20	5.9×10^{12}	SP	120	This Work

* SP indicates solution processed, NSP indicates non-solution processed (eg. thermal evaporation, atomic layer deposition). Solution processable accounts for solution processability of charge trapping layer, tunneling layer and channel layer. NA-data not available, CTM is charge trapping medium, ΔV_{on} is memory window, V_P/V_E are programming and erasing voltage, V_D is drain voltage, N_D is charge trap density and T_{proc} is maximum processing temperature.