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Wideband Variable-Gain Amplifiers Based on a Pseudo-Current-Steering Gain-Tuning Technique

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Abstract—This paper reports two single-ended voltage-control variable-gain amplifiers (VGAs) featuring a new pseudo-current-steering gain-tuning technique. In the first VGA (VGA-I), a single-bias-controlled dual-branch current mirror is developed as a standalone gain control block. In the second VGA (VGA-II), two NMOS transistors, which are biased by the same voltage, are integrated into a conventional common-source amplifier to adjust each single-branch current. Fabricated in 40-nm CMOS process, the VGA-I (VGA-II) occupies a tiny area of 0.03 mm² (0.024 mm²) and consumes 22 mW (20 mW). Measured over a gain range of >64 dB, the -3-dB bandwidth of the VGA-I (VGA-II) is 9 and 6.6 GHz. For the time-domain tests, the VGA-I (VGA-II) exhibits a jitter of 40 ps (30 ps), under a 2⁷-1 PRBS input at 12 Gb/s. Their power efficiencies (1.83 and 1.67 pJ/bit) compare favorably with state-of-the-art.

Keywords—variable-gain amplifier (VGA), CMOS, wide-tuning gain control, pseudo-current steering, bandwidth (BW), wireless transceiver, negative capacitance, peak-to-peak jitter.

I. INTRODUCTION

Wideband variable gain amplifier (VGA) is widely used in high-frequency and high-speed communications, such as 60-GHz wireless transceivers [1] and tens-of-Gb/s backplane receivers [2]. It regulates the wide-varying input power level to attain a constant output signal strength, maximizing the dynamic range of the overall system. The desirable feature of gain-tuning characteristic affects the evolution of the VGA's topologies. Generally, the state-of-the-art VGAs can be categorized into two groups: one of which requires a standalone gain-control block, either to convert the linear control voltage to an exponential output [3]-[5] or to enlarge the gain-control range [6], while the other topology possesses the gain-control feature with the amplifier itself [7]-[10]. The advantage of standalone topology is that the separate gain-control block is isolated from the signal path. Consequently, the performance of the amplifier, involving frequency response, linearity and power consumption, can be optimized independently. Further, according to different requirements for each application, different exponential generators with different accuracies and gain ranges can be chosen, which provides the designers additional flexibility. The integrated VGAs, on the other hand, usually have a simple structure, thereby reducing the size and complexity of the designs. Yet, the architecture is more confined with its corresponding gain-tuning algorithms, exacerbating the trade-off between the bandwidth (BW), linearity and power consumption.

Fig. 1. (a) Illustration of pseudo-current-steering technique. (b) Current flow versus gain-control signal (V_{CTRL}) corresponding to (a) when $\alpha_1=\alpha_2$.

In this paper, a pseudo-current-steering gain-tuning method is proposed and implemented in both standalone and integrated gain-control VGAs. Two fabricated architectures are compared and optimized respectively to achieve similar performance.

II. PROPOSED GAIN-TUNING METHOD

A. Pseudo-current-steering gain-tuning method

Although the VGA designed in [5] has achieved extreme low complexity by employing a negative exponential generator and a pseudo-folded Gilbert cell, it generates a differential control signal in the voltage domain, and subsequently converts it into the current domain, controlling the two branches of the amplifier. To further simplify its structure, the two-step conversion can be saved if the gain-control signal is converted to a differential output in the current domain directly. The illustration is shown in Fig. 1(a), in which two voltage-dependent current sources share a constant total current of I_0 , and the junction voltage (V_m) is flexible. Assuming one of the current sources is related to a variable voltage, V_{CTRL} , while the other is related to a fixed voltage, V_{REF} , and then both of them have a negative voltage-to-current relationship regarding V_m . As a result,

$$I_1 = \alpha_1 (V_{CTRL} - V_m) \quad (1)$$

$$I_2 = \alpha_2 (V_{REF} - V_m) \quad (2)$$

where α_1 and α_2 are the voltage-to-current conversion coefficients of the two voltage-dependent current sources, respectively. Since the sum of I_1 and I_2 is immutable, V_m will change accordingly such that,

$$\alpha_1 (V_{CTRL} - V_m) + \alpha_2 (V_{REF} - V_m) = I_0 \quad (3)$$

The above condition in (3) is always satisfied. The mechanism of current flows in the two branches is summarized in Fig. 1(b).

Fig. 2. Schematic of (a) VGA-I with standalone pseudo-current-steering gain control and (b) VGA-II with integrated pseudo-current-steering gain control.

I_1 increases from 0 to I_0 as the gain-control voltage increases, and I_2 decreases to maintain a constant total current. If we set $\alpha_1 = \alpha_2$, each of the branches shares the same current, which equals to $I_0/2$, when V_{CTRL} is equal to V_{REF} . With the help of this algorithm, two varying currents can be obtained from one single gain-control voltage, thereby controlling the transconductance (g_m) of the transistors and thus the gain of the amplifier. To implement this control method to VGA design, both standalone and integrated gain-control topologies are developed later.

B. Two Proposed Implementations

Fig. 2(a) shows our proposed variable gain single stage with a standalone gain-control block, in which a single-ended V_{CTRL} is converted to a pseudo-differential current output, thereafter mirrored to the current tail of the gain amplifier on the right-hand side. To guarantee the amplifier's gain increases monotonically across the gain-control voltage range, one of the PMOS (M_1) is connected to V_{CTRL} , while the other (M_2) is tight to ground, such that the two branches draw an identical current from the current source (M_0) when $V_{CTRL} = 0$. As V_{CTRL} is increased, the overdrive voltage of M_1 becomes smaller than that of M_2 , resulting in a larger current flowing through M_2 while less current through M_1 . The difference keeps increasing until M_1 is turned off and the entire current goes through M_2 , reaching the maximum gain of the amplifier. Note that, when $V_{CTRL} = 0$, the amplifier's gain will be zero if the effects of the transistors' nonidealities are not considered. In a practical design, the layout routing from M_4 to M_5 is considerably shorter than the one from M_3 to M_6 , leading to a relatively larger voltage drop of the latter and thus a minimum gain close to zero. Simulation results reveal that one such stage is able to provide a wide-tuning gain range from -40 to 2 dB, with a BW of 20 GHz.

Interestingly, our proposed pseudo-current-steering gain-control method can be integrated with a conventional amplifier as illustrated in Fig. 2(b). An auxiliary NMOS pair, M_3 and M_4 ,

Fig. 3. (a) Complete design-I for VGA-I with standalone gain control. (b) Complete design-II for VGA-II with integrated gain control. Schematic of (c) fixed gain amplifier and (d) negative capacitance (NC) circuit.

Fig. 4. Die photos and detailed layouts of (a) design-I and (b) design-II.

is placed parallel with the input differential pair, M_1 and M_2 , while its gate is connected to V_{CTRL} instead of the input signal. As a result, the input pair steers more current if V_{CTRL} is lower, providing a higher g_m and thus the overall gain. Compared to the topology in Fig. 2(a), this integrated design employs fewer transistors, but the parasitic capacitance accumulated at the output node may introduce concerns for high-speed applications. Consequently, a BW of 17 GHz is obtained along with a gain ranging from -30 to 4 dB.

III. COMPLETE ARCHITECTURES

Plotted in Fig. 3(a) and (b), two completed architectures are implemented with the above VGA-I/-II, respectively. Following two cascaded variable gain stages, both of them employs post amplifiers, realized by fixed gain amplifier (FGA) with resistive and capacitive degeneration, to boost the overall gain. The DC offset cancellation (DCOC) network and test buffer are included.

Fig. 5. Measurement results: (a) frequency response of design-I in dB scale, (b) frequency response of design-I in linear scale, (c) gain characteristic of design-I in dB scale, (d) frequency response of design-II in dB scale, (e) frequency response of design-II in linear scale, and (f) gain characteristic of design-II in linear scale.

Fig. 6. Measured peak-to-peak jitter: (a) design-I and (b) design-II with different V_{in} , when the input pattern is 2^7-1 PRBS.

To accommodate different features of the two variable gain stages introduced in the above section, care must be taken when incorporating them into the complete architectures [Fig. 3(a) and (b)]. In design-I, since pseudo-Gilbert cell in Fig. 2(a) works in such a way that the gain provided by one input pair is minus from that of another, the resultant maximum gain is lower compared to the integrated design. Thus, five stages of the fixed

gain amplifiers [Fig. 3(c)] are required to elevate its maximum gain up to 25 dB, each of which provides a gain of 4 dB with a power consumption of 3.5 mW. To further improve the internal BW of design-II, the negative capacitance [11-12] circuit [Fig. 3(d)] is inserted between stages to partially cancel the larger node-to-ground capacitance. With a similar power budget, three stages of the fixed gain amplifiers are cascaded, such that an overall gain of 23 dB is achieved.

IV. MEASUREMENT RESULTS

Fig. 4 shows the die micrographs of the proposed prototypes, both of which are fabricated in a standard 40-nm CMOS process, with an active area of 0.03 and 0.024 mm², respectively. Their frequency responses are measured by the network analyzer and are shown in Fig. 5, both in conventional dB scale and linear magnitude scale. While design-I has a higher BW up to 9 GHz, Design-II rolls off earlier ~7 GHz. When plotting their gain characteristic over the gain-control voltage (V_{CTRL}) in both dB and linear scales, it is interesting to observe that both preserve a linear-in-magnitude feature in the high-gain mode while a linear-in-dB feature in the low-gain mode. Furthermore, time-domain performance is verified by the pattern generator outputting the pseudo-random binary sequence (PRBS) with a length of 2^7-1 , and the eye diagram is captured by the real-time oscilloscope. Fig. 6 plots the measured peak-to-peak jitter of both designs, covering a data rate from 2 to 14 Gb/s, with different levels of input swing as weak, moderate and strong conditions. Under the low data rate of 2 Gb/s, the jitter is prominent due to the DC wander resulting from the DCOC network. However, at the higher data rate beyond 12 Gb/s, the

TABLE I.
PERFORMANCE SUMMARY AND COMPARISON OF RECENT STATE-OF-THE-ART VGAS

Parameters	JSSC'12 [3]	JSSC'16 [4]	TCAS-I'18 [5]	ISSCC'04 [6]	TCAS-I'12 [13]	MWCL'15 [14]	This work	
							Design-I	Design-II
Technology	130nm BiCMOS	130nm CMOS	65nm CMOS	180nm CMOS	90nm CMOS	65nm CMOS	40nm CMOS	
Data rate (Gb/s)	5	10	10	3.125	N/A	N/A	12	
Jitter (ps)	< 40	< 44	< 36	< 95	N/A	N/A	46	38
PRBS	2 ¹⁵ -1	2 ³¹ -1	2 ⁷ -1	2 ³¹ -1	N/A	N/A	2 ⁷ -1	
BW (GHz)	0.0002 to 7.5	0.0001 to 5.0	0.0001 to 7.0	0.0004 to 2	0.0002 to 2.2	0.0002 to 4	0.0001 to 9	0.0001 to 6.6
dB-linear	Yes	Yes	Yes	No	No	No	No	
Gain range (dB)	40 (-10 to 30)	40 (-15 to 25)	57 (-26 to 31)	50 (-16 to 34)	60 (-10 to 50)	60 (-39.4 to 20.2)	74 (-47 to 27)	64 (-44 to 20)
Power (mW)	72	50	28	40	2.5	26	22	20
Power eff. (pJ/bit)	14.4	5.0	2.8	12.8	N/A	N/A	1.83	1.67
Active area (mm ²)	1	0.4	0.045	0.7	0.01	0.06	0.03	0.024

jitter becomes worse as the amplifiers are not fast enough. Additionally, the high-frequency peaking and the corresponding phase distortion incur the data-dependent jitter and inter-symbol interference (ISI), worsening the time-domain waveform. In both cases, it is observed that higher input levels can lead to a better jitter performance.

Table I shows the performance summary and comparison with recent state-of-the-art VGAs [3-6, 13, 14] targeting similar applications. Both designs show a wider gain range, higher power efficiency as well as a smaller core area.

V. CONCLUSION

This paper presented the pseudo-current-steering voltage-control method. Two design examples (VGA-I and VGA-II) were prototyped in 40-nm CMOS. Measurement results show that this work achieves a wide gain range (>64 dB) and BW (> 6.6 GHz), while occupying a small active area (<0.024 mm²) and achieving a better power efficiency (<1.83 pJ/bit) up to 12 Gb/s.

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