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Alternate Arm Converters-Based HVDC Model Compatible with the CIGRE B4 DC Grid Test System

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Abstract—This paper develops an alternate arm converter (AAC)-based point-to-point high-voltage direct current (HVDC) transmission system compatible with the existing benchmark models of modular multilevel converter (MMC)-based HVDC and multiterminal dc (MTDC) grids. The developed AAC-based HVDC system expedites the future development of multi-converter, multiterminal benchmark models that enable the system level studies with detailed models of multiple topologies. The configuration and design parameters of the topology, are derived in alignment with the existing MMC-based benchmark systems. Detailed analysis and simulation studies based on real-time digital simulations verify the operation and performance of the developed AAC-based HVDC system and the associated control functions. The model developed in RTDS is also provided as supplementary material in order to enable further research and development on multiple topologies-based dc grids.

Index Terms—Multilevel converters, alternate arm converter, benchmark systems, HVDC transmission.

I. INTRODUCTION

VOLTAGE source converter (VSC)-based high-voltage direct current (HVDC) transmission and multiterminal dc (MTDC) networks have become popular in recent research and development. Both point-to-point (PTP) VSC-HVDC and MTDC are prospective solutions for the challenges of future power systems enriched with renewable and distributed energy sources [1]. HVDC systems provide access to remote locations and MTDC networks offer flexibility in handling the intermittency of distributed generation, currently in the form of large-scale off-shore wind farms and in the near future large-scale solar PV and energy storage systems.

In recent years, the number of installed VSC-HVDC projects based on modular multilevel converters (MMCs) has increased with numerous ongoing and planned, many systems above 1 GW. Alongside, VSC-based MTDC have also been developed. Nanao [2] and Zhoushan [3], currently in operation in China, are the two pioneering MTDC systems based on MMCs featuring three and five terminals, respectively. The application of commercial dc-breakers in the Zhoushan system [4] is a major step towards fully functional dc-grids. Further research

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Fig. 1. Circuit configuration of a three-phase alternate arm converter.

on dc-breakers [5] and dc-fault tolerant topologies for VSC-based HVDC will assure more resilient MTDC grids in the future [6].

The economical and technological scale of HVDC and MTDC systems necessitates detailed validation and testing before actual implementation. Hence, development of benchmark dc systems is a paramount requirement [7]–[9]. One of the main purposes of benchmark models is to provide a common basis for the testing and performance of research concepts and algorithms. Data availability is important for diverse types of studies ranging from high-level load flow analysis all the way to detailed semiconductor behavior [10]. In addition to the required controllers, dc-grid power flow analysis, interactions and coordination between ac and dc-grids, and protection strategies may also be included.

Currently, the most widely accepted benchmark model for HVDC and MTDC system studies is developed by the CIGRE B4-57 Committee [11], [12]. The motivation behind the main benchmark model and its subsystems was the study of HVDC systems operation and the interactions between MTDC system and multiple ac networks. However, limited to VSC-HVDC based on MMCs, the CIGRE benchmark model is not open to diverse types of studies, e.g. line-commutated converter (LCC)-HVDC systems, long-distance ultra-HVDC (UHVDC) transmission, ac network interconnection with back-to-back (BTB)-HVDC systems and energy storage integration [12]. In order to fill this gap, a benchmark HVDC system has been proposed by the Smart Grid Research Institute of the

State Grid Corporation of China [13]. Moreover, the current trend is the research and development of emerging dc-fault tolerant multilevel converter topologies for HVDC systems. Therefore, attention needs to be paid on the development of benchmark models based on emerging dc-fault tolerant multilevel converter topologies.

MMCs with half-bridge unipolar SMs are used in the majority of current VSC-based HVDC projects in operation or under construction. Other multilevel converter topologies for such applications include *i)* full-bridge SMs (FB-SMs) or other bipolar SMs-based MMCs [14], *ii)* MMCs with hybrid SM configurations, *iii)* the dc-fault tolerant alternate arm converter (AAC) [15], and *iv)* hybrid converter configurations [16]. A future dc-network implementation will require an organized operation of HVDC stations from multiple vendors. This coordination will depend on the development of grid-codes and pre-determined functional specifications for dc networks. Hence, the development of benchmark models that include multiple network and diverse converter configurations enables multiple users and vendors to have access to a common basis for testing.

Based on the above, this paper aims to derive, develop and verify an AAC-based PTP HVDC transmission system compatible with the existing CIGRE B4-57 benchmark models, in order to complement the existing literature in the area of HVDC systems and MTDC networks. The derived benchmark model is a necessary step towards detailed simulation models of MTDC networks based on multiple converter topologies.

The paper is structured as follows. Section II describes the basic overview and operating principles of the AAC. The considerations and parameters of the AAC-based HVDC system in equivalence with existing MMC-based models are derived in Section III. Section IV provides real-time digital simulations and performance of the proposed model and Section V summarizes the conclusions.

II. THE ALTERNATE ARM CONVERTER

A. Topology and Basic Operation

The AAC is an emerging dc-fault tolerant multilevel converter topology [15] from the same family as the state-of-the-art MMC in terms of circuit configuration and control requirements. The three-phase AAC model is shown in Fig. 1. Each phase-leg consists of two arms with N series-connected FB-SMs, one director switch (DS), and one inductor (L) per arm. Fully controllable bipolar SMs are required for the normal operation of the AAC, in order to reach the over-modulation range [17]. Combined with the normal operating requirements, the bipolar SMs provide the dc-fault tolerant capability to the AAC. Each DS comprises an array of switches that can withstand to the maximum off-state voltage.

The operation of two DSs is similar to a typical two-level converter. Two DSs, DS_u and DS_l alternatively conduct the total phase-current during the positive and negative half-cycles of the output reference voltage $v_{am} = m_a \cos(\omega t)$, respectively. Therefore, the total arm voltage requirement of the AAC is half the dc-link voltage; significantly lower compared to that of the MMC. The alternate operation of DSs restricts the

Fig. 2. AAC-based HVDC system control hierarchy.

energy exchange between the two arms of a phase-leg. This limitation confines the natural energy balance of the AAC to a single operating point $M_a = 4/\pi \approx 1.27$ called sweet-spot [15]. The peak output voltage ($\hat{V}_a$) at the sweet-spot is:

$$\hat{V}_a = M_a \frac{V_{dc}}{2} = \frac{2V_{dc}}{\pi}. \quad (1)$$

Unlike the MMC, there is no continuous energy exchange between the upper and lower arm of the AAC leading to unbalanced stored energy in the SM capacitors at nonsweet-spot operating points (deviation of SM capacitor voltages from their reference). The unbalanced SM energy can be exchanged using a circulating current (i_{circ}) that flows through the phase-leg during an overlap period, introduced by switching on both of the DSs around the zero-crossing points of v_{am} . The overlap operation of the AAC mimics the MMC operation, and AAC arm currents (i_u and i_l) during the overlap period can be defined based on the MMC operation [18].

B. Control and Modulation

The control hierarchy for an AAC-based HVDC system is shown in Fig. 2. The top layer (“AC/DC Grid Control”) defines the dispatch schedules for the overall power system [12]. The second layer (“Coordinated System Control”) responds to the unscheduled events of the power system providing frequent set-points to the third layer with the timely coordination of all converter stations [19]. The third layer (“Converter Station Control”) is the high-level control of the HVDC converter station which regulates active/reactive power, node voltages and frequency based on the set points. The bottom layer (“Internal Converter Control”) performs low-level control functions that are essential for robust internal converter operation.

The combined high- and low-level detailed control structure for the AAC-based HVDC converter station is shown in Fig. 3. The controller is structured in three stages as *i)* outer controller, *ii)* inner current controller, and *iii)* modulation & sorting. The outer control loop determines the references for the inner current controller based on the voltage and power set points. The inner current controller calculates the output voltage reference for the modulation stage by regulating the output currents in the synchronous reference frame. The modulation stage determines the required number of SMs to be inserted for

Fig. 3. Control structure of the AAC-HVDC station.

the output voltage generation [20]. Although different pulse-width modulation (PWM) techniques can be applied, nearest level modulation methods are the most feasible with large number of levels [21].

Simultaneously, the overlap period and circulating current controller determine the switching signals for the DSs and required number of additional SMs to be inserted, respectively. The AAC can operate with either a short-overlap ($\lesssim 18^\circ$) [22] or an extended-overlap ($> 60^\circ$) [23], [24] to achieve energy balancing. Compared to the short-overlap mode, the extended-overlap mode provides active filtering for the dc current but, DSs are subjected to increased voltage stress and may require more redundant SMs depending on the zero-sequence voltage injection. Different circulating current control techniques can be adopted considering their energy balancing performance [25]–[29].

The alternate operation of the two arms of a phase-leg leads to arm current interruptions for inverter (rectifier) mode operation with a lagging (leading) power factor. Hence, achieving zero-current switching (ZCS) [30], [31] of the DSs is important. ZCS is achieved by controlling arm currents during the overlap period. Moreover, snubber circuits are used in order to reduce the voltage stress on DSs due to current interruption through the arm inductance [32].

III. PROPOSED BENCHMARK AAC-HVDC SYSTEM

A. Modeling and MMC Equivalence

The CIGRE benchmark MMC-MTDC system (Fig. 4) consists of three dc subsystems as DCS 1, 2, and 3. DC System 1 (DCS 1) is a typical PTP-HVDC transmission system that integrates an offshore wind farm to an onshore ac-grid. The proposed AAC-HVDC system is developed maintaining similar power and voltage ratings for the dc-grid and the two ac-grids. Hence, the parameters of both AAC-HVDC stations are determined by translating from the CIGRE benchmark MMC-HVDC stations and based on the recommendations and guidelines of the existing literature [33], [34].

1) *Operating Point:* Depending on the topology and operation, the output voltage of the AAC is different compared to

Fig. 4. CIGRE B4 multi-terminal dc test system [12].

the MMC for a similar dc voltage rating. Hence, the secondary voltage of the converter transformer has to be redefined satisfying the standards of network operators. Typically, the HVDC converter station should operate within a tolerance of $\pm 10\%$ in the ac-grid voltage [34]. Considering sweet-spot operation (1) for the 10% over-voltage, the standard operating point of the AAC can be defined as:

$$m_a = \frac{M_a}{1.1} \approx 1.15, \quad (2)$$

setting a typical operating range of $m_a \in (1, 4/\pi)$.

The over-modulation range is beneficial for the typical operating range in terms of the AAC energy balancing performance. For $m_a > 1$, SMs are oppositely inserted in order to increase the output voltage above the dc-link voltage changing the arm current direction relative to the SM capacitor voltage. The change of arm current direction assists the discharging (charging) of SMs for the inverter (rectifier) mode of the AAC. Hence, the required energy balancing effort of the circulating

current controller is lower at the defined typical operating range $m_a \in (1, 4/\pi)$.

2) *Number of SMs and Director Switch Ratings*: The requirement of bipolar SMs for the AAC has two considerations: i) to operate in the over-modulation range and ii) to reduce the fault current during a dc-fault by blocking the ac voltage. The number of SMs per AAC arm is determined in order to block the sweet-spot ac-voltage ($m_a = M_a$) as:

$$N = \left\lceil \frac{\hat{V}_a}{V_C} \right\rceil = \left\lceil \frac{M_a V_{dc}}{2V_C} \right\rceil, \quad (3)$$

where V_C is the nominal SM capacitor voltage.

Due to the alternate operation of the two arms of a phase-leg, the DS of the nonconducting arm is subjected to a high voltage at the peak of the output voltage. The DS voltage also depends on the operating point. The DS voltage stress can be reduced by keeping all the SMs of the nonconducting DS inserted. The peak voltage stress across the DS is:

$$\hat{v}_{DS} = (m_a + 1 - M_a) \frac{V_{dc}}{2}, \quad (4)$$

and is maximum at sweet-spot operation ($m_a = M_a$). Considering the FB-SM, and assuming that the identical switches are used in SMs and DSs, the required number of series-connected switches (N_{DS}) per DS can be determined as:

$$N_{DS} = \frac{\hat{v}_{DS}|_{(m_a=M_a)}}{V_C} = \frac{\pi}{4} N. \quad (5)$$

N_{DS} is 20% compared to the total number of switches ($4N$) within an arm.

3) *Redundant Voltage and Overlap Period*: The redundant voltage [17] and the overlap period are important for circulating current control. Both parameters are limited by the collective operation of the two arms of a phase-leg that generate the output voltage avoiding distortions. Depending on the number of SMs per arm, the maximum redundant voltage of an arm is:

$$V_r = NV_C - \frac{V_{dc}}{2}, \quad (6)$$

and it is available for circulating current control at the zero-crossing points of the output voltage. Around the zero-crossing points, availability of the redundant SMs varies according to the duty cycles of the two arms and it should be accounted for circulating current control.

The overlap period under normal operating conditions can be different according to the requirements of circulating current control method applied to the AAC [25]–[28]. However, the maximum achievable overlap period ($\hat{t}_{ov}$) should not be exceeded in order to avoid output voltage distortions. Considering (6) and the operating point, the maximum achievable overlap period is:

$$\hat{t}_{ov} = \frac{2}{\omega} \sin^{-1} \left(\frac{M_a - 1}{m_a} \right). \quad (7)$$

Moreover, for a given operating point, the maximum overlap period can be expanded beyond t_{ov} using zero-sequence injection [23], [35].

4) *SM Capacitance and Arm Inductance*: The energy storage requirements of the AAC are considerably lower compared to that of the MMC; approximately equal to one third of the typical stored energy of the MMC [34]. The typical range of the stored energy of the MMC is 30~40 kJ/MVA that limits the SM capacitor ripple to 10% of the nominal voltage V_C [12]. According to the recommendations of [34], the stored energy of the AAC (E_{AAC}) is set to 11 kJ/MVA in order to achieve the same 10% ripple target. Similarly to the CIGRE benchmark MMC-HVDC, the required SM capacitance for the AAC can be determined as a function of the converter rating S and is:

$$C = \frac{S E_{AAC}}{3 N V_C^2}. \quad (8)$$

The arm inductance of the MMC is selected to satisfy the capability of circulating current control and to limit the fault current rate [36]. The MMC requires significantly larger arm inductances in order to provide coupling between the two arms of a phase-leg that are continuously connected and for the flexibility of controlling the circulating current during the normal operation. The coupled operation of the two arms of an AAC phase-leg is confined only to the overlap period. Moreover, the AAC inherits the dc-fault blocking capability from the use of bipolar SMs. Therefore, the arm inductance requirement of the AAC is comparatively small and can be determined only depending on the flexibility for circulating current control [30].

The circulating current controller has two objectives within the overlap period: i) SM capacitor energy regulation and ii) ZCS of the DS by forcing the arm current through the anti-parallel diode. The redundant voltage (6) and the maximum overlap period (7) are the limiting factors that need to be considered for circulating current control [28]. Deriving from (3) and (6), the impact of the SM capacitor voltage ripple ($\pm 10\%$) on the variation of redundant voltage can be expressed as:

$$(0.9 M_a - 1) \frac{V_{dc}}{2} \leq V_r \leq (1.1 M_a - 1) \frac{V_{dc}}{2}. \quad (9)$$

Hence, only 50% of V_r (the lower bound of (9)) can be utilized all times for circulating current control without considering the influence of the SM capacitor voltage ripple. Additionally, the availability of the redundant SMs around zero-crossing points of v_{am} is higher for a shorter overlap period. Therefore, it can be considered that $0.5V_r$ is consistently available throughout an overlap period of $0.5\hat{t}_{ov}$. In order to provide the circulating current control flexibility, the arm inductance is chosen to have a minimum circulating current gradient of $2\hat{I}_a/0.5\hat{t}_{ov}$ with a differential voltage of $0.5V_r$. Considering $S = 3\hat{V}_a\hat{I}_a/2$, (6), and (7), the arm inductance can be determined as:

$$L \leq \frac{3V_{dc}V_r}{4\omega\pi S} \sin^{-1} \left(\frac{M_a - 1}{m_a} \right). \quad (10)$$

5) *DC-Link and Transmission Line*: The dc-link current of the AAC contains a six-pulse ripple due to the alternate operation of the arms. Therefore, an AAC requires a dc-link capacitance and inductances to filter the dc current. The dc-filter parameters can be determined depending on

Fig. 5. Benchmark AAC-HVDC system.

TABLE I
PARAMETERS OF THE AAC-HVDC STATIONS

Parameter	AAC-1	AAC-2
Rated Power	800 MVA	800 MVA
DC Voltage	± 200 kV	± 200 kV
Number of SMs per arm	255	255
SM Voltage	1 kV	1 kV
Stored Energy	11 kJ/MVA	11 kJ/MVA
SM Capacitance	11.5 mF	11.5 mF
Arm Inductance (p.u.)	0.016	0.016
Nominal Frequency	50 Hz	50 Hz
Nominal Operating Point (p.u.)	1.15	1.15
Transformer Resistance (p.u.)	0.004	0.004
Transformer Leakage Inductance (p.u.)	0.11	0.11
Transformer Ratio	0.778	0.297
AC-Grid Voltage	380 kV	145 kV
Short-circuit Power	30 GVA	4 GVA
R/X Ratio	0.1	0.05
DC Capacitance	88 μ F	
DC Inductance	50 mH	

the significant low-order harmonic component in the dc-link, mainly the sixth harmonic generated by the six-pulse ripple. Considering the characteristics of an LC filter [37], the filter cut-off frequency (ω_c) can be chosen well below 6ω . Based on the recommendations for typical dc-side energy storage requirements and smoothing inductance [23], [34], the dc-link parameters can be calculated as:

$$\frac{1}{\sqrt{2L_{dc}C_{dc}}} < \omega_c \quad (11)$$

Based on the above derivations, the calculated parameters for each AAC-HVDC station are shown in Table I and the schematic diagram of the benchmark AAC-HVDC system is shown in Fig 5. Equivalent lumped parameters of the dc transmission line and control parameters of both high- and low-level controllers are given in Table II.

B. Real-Time Model and Computational Requirements

A detailed equivalent model of the AAC-HVDC system has been developed based on an RTDS real-time digital simulator. Fig. 6 shows the hardware requirement for the proposed AAC-HVDC system, which includes two racks with a total of seven PB5 processor cards. RTDS performs the real-time simulation using two time-steps. Computations of control components, network solution, and transmission line model are performed during the large time-step ($\approx 50\mu$ s) where the simulation of VSC networks and power system components are executed using a smaller time-step (3μ s).

TABLE II
TRANSMISSION LINE AND CONTROL PARAMETERS

Transmission Line Parameters [12]	
Length	200 km
Resistance	0.011 Ω /km
Inductance	0.2615 Ω /km
Capacitance	0.2185 Ω /km
Control Parameters (Fig. 3)	
DC Voltage Control	$K_P = 8, K_I = 272$
Active/Reactive Power Control	$K_P = 0, K_I = 33$
AC Voltage/Frequency Control	$K_P = 0.2, K_I = 30, K_D = 0.0025$
Energy Balancing	$K_P = 2.9, K_I = 75$

Fig. 6. RTDS hardware requirement for real-time simulation

The AAC arms are implemented using “Multilevel Chain-link Converter Model” (*rtids_vsc MMC5*). The arm model *rtids_vsc MMC5* assumes ideal internal SM capacitor voltage sorting and balancing. This model is sufficient for general HVDC and MTDC studies. The real-time AAC-HVDC model¹ can be used for detailed studies of internal converter control, power flow, grid-faults, and transients. The two AACs, ac-grids, converter transformers and director switches are implemented inside VSC networks which are computed within the smaller time-step. One PB5 processor card is required for each AAC-based converter station as shown in Fig. 6.

The distributed nature of the transmission line parameters and the frequency dependency is vital for detailed transient studies. A frequency dependent HVDC transmission line is modeled using RSCAD T-Line tool, equivalent to the existing MMC benchmark HVDC system [12]. One PB5 processor card is required for the computation of the transmission line and simulated within the large time-step. The small time-step to large time-step interfaces connect the two ends of the HVDC transmission line to AACs implemented in small time-step VSC networks.

IV. REAL-TIME SIMULATION RESULTS AND VERIFICATION

A. Steady-State Operation

In steady-state, both AACs operate at the standard operating point ($m_a = 1.15$) and unity power factor [12]. AAC-1 and AAC-2 operate in inverter and rectifier modes, respectively. The power flow (800 MW) is from AAC-2 to AAC-1. Figs. 7 and 8 show the steady-state voltages and currents of the two HVDC stations. The %THD of ac-grid currents are below

¹The RTDS model files of the AAC-HVDC system can be downloaded from http://bit.ly/AAC_Model_UNSW.

Fig. 7. Steady-state results of AAC-1 (Inverter mode): (a) ac-grid voltages, (b) ac-grid currents, (c) SM capacitor voltage of phase *a*, and (d) arm currents of phase *a*.

Fig. 8. Steady-state results of AAC-2 (Rectifier mode): (a) ac-grid voltages, (b) ac-grid currents, (c) SM capacitor voltage of phase *a*, and (d) arm currents of phase *a*.

2.7% and agree with the network operating standards. SM capacitor voltages are well regulated to the reference (1 p.u.) in both modes of operation. SM capacitor voltage ripples are according to design considerations of (8). However, the shape of the SM capacitor voltages is different between the two operating modes due to the current direction and overlap current as seen in Figs. 7(d) and 8(d).

The arm currents are more likely to be interrupted by the operation of DSs in rectifier mode. Fig. 8(d) shows these

Fig. 9. Power reversal: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of grid-1, (f) ac currents of grid-2, (g) SM capacitor voltages of AAC-1, and (h) SM capacitor voltages of AAC-2.

interruptions within the overlap period. The voltage spikes generated across the arm inductors slightly affect the output voltages (Fig. 8(a)). In order to avoid or minimize hard switching, ZCS methods should be applied [28], [30], [31].

B. Active/Reactive Power Control

Independent power control is one of the key capabilities of VSCs. The performance of the AAC-HVDC system under active power reversal and reactive power step changes are shown in Figs. 9 and 10, respectively. The active power reference of AAC-2 is changed from -1 p.u. to 1 p.u. within 400 ms while maintaining unity power factor operation (Figs. 9(a) and (b)). The dc voltages, dc currents, and ac-grid currents of Figs. 9(c)-(f) demonstrate the stable performance of the high-level dc

Fig. 10. Reactive power step changes: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of grid-1, (f) ac currents of grid-2, (g) SM capacitor voltages of AAC-1, and (h) SM capacitor voltages of AAC-2.

voltage controller and power regulation. SM capacitor voltages of the two AACs slightly deviate from the reference during the power ramp as shown in Figs. 9(g) and (h). Nevertheless, SM capacitor voltages are always maintained at the reference during steady-state operation.

In order to demonstrate the reactive power support capabilities, a power step of 0.5 p.u. is applied to both AACs while maintaining a fixed active power reference of 0.9375 p.u. Fig. 10 demonstrates the performance of the AAC-HVDC system under reactive power step changes. At 0.2 s, reactive power reference of AAC-1 is changed from -0.25 p.u. to 0.25 p.u. and for AAC-2, the opposite change is applied at 0.5 s. Figs. 10(a)-(f) show that the reactive power step changes applied to the AAC operating in the rectifier mode are

Fig. 11. Single-line to ground fault at ac-grid 1: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of grid-1, (f) ac currents of grid-2, (g) SM capacitor voltages of AAC-1, and (h) SM capacitor voltages of AAC-2.

more likely to slightly deviate the dc- and ac-side quantities compared to the AAC operating in the inverter mode. It is also reflected in the SM capacitor voltages of Fig. 10(h). However, the SM capacitor voltages are always regulated to the reference during the steady-states before and after the transients.

C. Performance Under AC-Faults

Robust operation under fault conditions is important for an HVDC system. Hence, the fault-ride-through (FRT) capability is essential. The proposed AAC-HVDC system performance was tested under two fault conditions, single line-to-ground (SLG) fault and a three-phase short circuit fault. Fig. 11 shows the operation performance under a 200-ms SLG fault

Fig. 12. Three-phase fault at ac-grid 1: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of grid-1, (f) ac currents of grid-2, (g) SM capacitor voltages of AAC-1, and (h) SM capacitor voltages of AAC-2.

at the ac-grid 1. Figs. 11(a)-(d) show dc-side voltage and current oscillations caused by the ac-side (Fig. 11(e)) power oscillations. AC currents of grid-2 (Fig. 11(f)) reduce due to the power drop in the dc-side during SLG fault at grid-1. As shown in Figs. 11(g) and (f), the SM capacitor voltages of the faulted and nonfaulted AAC-HVDC stations approximately deviate by 0.6 p.u. and 0.2 p.u., respectively during the fault [38].

Fig. 12 shows the AAC-HVDC system operation under a three-phase fault at ac-grid 1 for 200 ms. The active power in both ac-sides drops to zero during the fault as shown in Figs. 12(a)-(f). The SM capacitor voltages deviate similarly to the case of SLG fault as shown in Figs. 12(g) and (f). However,

Fig. 13. Pole-to-pole dc-fault at the terminals of AAC-1: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of grid-1, (f) ac currents of grid-2, (g) SM capacitor voltages of AAC-1, and (h) SM capacitor voltages of AAC-2.

post fault system recovery is satisfactory in both cases as the pre-fault operating conditions are restored in less than 100 ms as shown in Figs. 11 and 12.

D. Performance Under DC-Faults

One of the key advantages of the AAC compared to the typical half-bridge SMs-based MMC is its dc-fault blocking capability which is an important requirement for HVDC and MTDC applications [1], [15]. The proposed AAC-HVDC system performance is tested applying a permanent pole-to-pole dc-fault at the dc terminals of AAC-1, which is the dc-voltage controlling HVDC terminal. Test conditions are

specified similarly to [12]. Following the dc-fault detection, AAC-1 and AAC-2 are blocked after delays of 0.62 ms and 1.59 ms, respectively [12]. In MMC-based HVDC systems ac-grid breakers open after converter blocking in order to block the fault current flow from ac-side to dc-side. In the proposed AAC-HVDC system ac-breakers remain closed regardless of the dc-fault as the AACs are capable of blocking the fault currents from ac-side to dc-side.

Fig. 13 shows the performance of the AAC-HVDC system under pole-to-pole dc-fault. Active power of both terminals drop to zero and reactive powers do not significantly deviate as shown in Figs. 13(a) and (b), respectively. Figs. 13(c) and (d) demonstrate the response of dc-side voltages and currents. The dc voltages drop to zero with slight oscillations caused by dc-link capacitors and the smoothing inductances, and the rise of dc-currents shows the discharging of dc-link capacitors of the two terminals. The ac-side currents do not rise following the fault as shown in Figs. 13(e) and (f), even if the ac-breakers remain open. Also, the SM capacitor voltages of Figs. 13(g) and (h) remain charged as the converters are blocked. The results of ac-currents and SM capacitor voltages of the two terminals demonstrate the dc-fault blocking capability of the AACs for HVDC applications.

V. CONCLUSION

The AAC is an emerging converter topology with dc-fault tolerance capability and a potential candidate in future multiterminal dc networks. This paper derives and develops an AAC-based HVDC transmission system in equivalence with the existing HVDC benchmark dc-grid systems as applicable for real-time simulations. The performance of the developed model is demonstrated through real-time simulation results based on an RTDS under multiple operation scenarios. The operation of the overall control system is verified by the demonstration of accurate steady-state results, active/reactive power control performance, SM capacitor voltage control, and operation under ac- and dc-faults. The developed AAC-HVDC model is made openly available for use. This work is the first step towards the development of multiterminal HVDC networks that include multiple converter topologies.

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