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Deadbeat Control for a Single-Inductor Multiple-Input Multiple-Output DC–DC Converter

Benfei Wang , *Member, IEEE*, Xinan Zhang , *Member, IEEE*, Jian Ye , *Student Member, IEEE*,
and Hoay Beng Gooi , *Senior Member, IEEE*

Abstract—This paper presents a deadbeat-based method for the single-inductor multiple-input multiple-output (SI-MIMO) dc–dc converter. By solving the cross regulation problem of the SI-MIMO dc–dc converter, the proposed method is capable of achieving the input current regulation (ICR) and the output voltage regulation (OVR) simultaneously. Moreover, the output current observers are adopted to replace the output current sensors, which are required by the conventional model based methods for dc–dc converters. The proposed control approaches including ICR and OVR are discussed in detail. To verify the effectiveness of the proposed deadbeat-based method, simulation runs and experiments are conducted on the single-inductor dual-input dual-output buck converter simulation platform and hardware prototype, respectively. The simulation and experimental results are analyzed in detail, and the comparison with the previous works is conducted.

Index Terms—Cross regulation, current observer, deadbeat control, multiple-input, multiple-output, single-inductor.

I. INTRODUCTION

THE multiple-input multiple-output (MIMO) dc–dc converters are developed for the integration of various energy sources and loads, with less component count, smaller circuit size, and lower system cost [1]. Moreover, most of the state-of-art MIMO dc–dc converters can be extended to an arbitrary number of inputs or outputs. In view of such desirable features, the MIMO dc–dc converters have been utilized widely in different applications, including fuel cell integration, future smart homes, electric vehicles, etc. [1]–[12].

Based on the number of the inductors, the MIMO dc–dc converters can be further categorized as multiple-inductor MIMO (MI-MIMO) dc–dc converters [1]–[4] and single-inductor MIMO (SI-MIMO) dc–dc converters [5]–[11]. However, the MI-MIMO dc–dc converters of a large number of inputs and outputs still face with the issues of high electromagnetic interference, bulky system size, and high cost due to the adoption

of numerous inductors. The single-inductor topology is an effective solution to the aforementioned issues associated with a multiple-inductor topology. Therefore, various research works have been conducted on SI-MIMO dc–dc converters because of their advantages, with the diverse applications such as electric vehicles [5], [7], and solar and thermoelectric energy harvesting systems [10]–[12].

In [5], Nahavandi *et al.* have proposed an SI-MIMO boost converter for electric vehicle applications. The small-signal models for the different operation modes of the proposed converter have been developed for regulating the input power and output voltage. However, the small-signal model based control method indicates that the regulation performance is easily affected by the variations of system operation points. In [6], a zero-voltage switching SI-MIMO converter with step up/down capability has been presented. The authors have designed the switching pattern for the converter for different operation modes to achieve the soft-switching target; however, the stable output voltage regulation (OVR) is not validated. An SI-MIMO buck–boost converter has been presented for electric vehicles applications in [7]. The converter can generate the output voltages, which can be higher than the maximum input voltage or lower than the minimum input voltage. The authors have further developed this SI-MIMO buck–boost converter with series-output configuration and elaborated the input power budgeting and OVR [8], [9]. In addition, the multiple-variable feedback control method has been proposed. The converter works on the principle of sequential operation derived from a time-multiplexing strategy (TMS), so that either one source or one load is connected to the shared inductor in every sequential control cycle. The proposed method is capable of individually controlling input power for input power budgeting, and independently regulating the output voltages for different load demands. A single-inductor dual-input dual-output (SI-DIDO) dc–dc converter has been developed for harvesting the solar energy [10]. The authors have proposed a control method based on the different operation modes including the heavy load mode and light load mode. In addition, the mode detection circuit is required to detect the operation modes. In each mode, the proposed method contributes toward good OVR and power flow scheduling among photovoltaic cells, rechargeable batteries, and loads. However, the specially designed topology of the SI-DIDO dc–dc converter is not suitable for the extension for an arbitrary number of inputs or outputs. In [11], the integrated circuit chip of an SI-DIDO dc–dc converter has been

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The authors are with the Nanyang Technological University, 639798, Singapore (e-mail: bwang7@e.ntu.edu.sg; zhan0342@e.ntu.edu.sg; jye007@e.ntu.edu.sg; ehbgooi@ntu.edu.sg).

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presented for the thermoelectric energy harvesting. With the dual-mode control and the auxiliary programmable-capacitor-array, the maximum power point tracking can be achieved. Similarly, the extension of the proposed converter in [11] to MIMO topology is difficult due to the application-specific circuit design. In [12], a single-inductor dual-input tri-output (SI-DITRO) buck-boost converter has been developed for indoor solar energy harvesting. The proposed SI-DITRO converter works in a discontinuous-conduction mode with pulse-skipping modulation and pulse-frequency modulation to achieve energy management of the solar panel and battery.

Based on the previous discussions, there are several drawbacks of the SI-MIMO/SI-DIDO dc-dc converters and the corresponding control methods in [5]–[12]. First, the cross regulation problem, which is critical for the OVR of the converters with a single-inductor topology [13], [14], has not been well considered in [5]–[12]. The cross regulation is defined as the interference among multiple output channels through the shared inductor, which means that each output channel can be directly affected by the operation point of the SI-MIMO dc-dc converter. The failure in solving this problem can lead to severely degraded OVR. Second, the mode-based control methods and application-specific circuit design in [10] and [11] are not feasible for the extension to an arbitrary number of inputs or outputs. In [15], a generalized method based on model predictive control (MPC) is proposed, which significantly attenuates the cross regulation effect and supports an arbitrary extension. However, the proposed method in [15] inherits the disadvantages of MPC including varying switching frequency and high computational complexity. The output current sensors are required because accurate output current is imperative for MPC, which results in a significant cost increase when there are numerous loads.

In order to control the SI-MIMO dc-dc converters with consideration of solving cross regulation, maintaining generality for easy extension, and reducing the computational burden and hardware cost, a deadbeat-based method with online output current observation is presented for the input current regulation (ICR) and OVR in this paper. The deadbeat control strategy has been extensively applied to different types of power converters [16]–[19]. Deadbeat control is a model-based strategy, and it can generate the duty ratio for regulation error minimization in one control cycle. It possesses the features of implementation simplicity and fast dynamic response, which are inherited by the proposed method for SI-MIMO dc-dc converters. Additionally, the proposed method can dynamically manipulate the duty ratio according to the target reference value in every control cycle, so that cross regulation can be effectively reduced in real time. Last but not the least, the adoption of output current observers can avoid the rising hardware cost when there are numerous loads.

The rest of this paper is organized as follows. Section II introduces the configuration of the SI-MIMO dc-dc converter. The proposed deadbeat-based method, including ICR, OVR, output current observers, and the control scheme, is presented in details in Section III. The component design and performance index are discussed in Section IV. In Section V, simulation and experimental results are provided to verify the effectiveness of the proposed method. The comparison between the proposed

Fig. 1. Illustration of the SI-MIMO buck converter. (a) Topology. (b) Basic operation principle.

method and state-of-the-art methods for the SI-MIMO dc-dc converter is conducted. Section VI draws the conclusion of this paper.

II. SI-MIMO BUCK CONVERTER

A. SI-MIMO Buck Converter Topology

The SI-MIMO buck converter is utilized in this paper to illustrate the proposed deadbeat-based method. Fig. 1(a) presents the topology of the SI-MIMO buck converter.

On the input side, it can be seen that there are m input channels. For the j th channel in m input channels, $v_{in,j}$ and $i_{in,j}$ denote the input voltage and current. The j th input channel is assigned with a forward-conduction bidirectional-blocking (FCBB) switch P_j , which is regulated by the corresponding control signal p_j . The FCBB structure is capable of avoiding the uncertain power flow between the multiple input power sources [8], [13]. On the output side, there are n output channels. $v_{out,i}$, $i_{out,i}$, C_i , and R_i represent the output voltage, current, filter capacitor, and load of the i th output channel. Moreover, the value of all output filter capacitors ($C_1, C_2, \dots, C_i, \dots, C_n$) is C . The corresponding switch and control signal are Q_i and q_i , respectively. It is noted that p_i (or q_i) = 1 and 0 indicates the ON and OFF states of P_i (or Q_i), respectively.

Between the input and output channels, there is a shared inductor L and a shared diode D . Moreover, i_L denotes the inductor current, and v_{in} represents voltage between the joint point of input channels and ground.

B. Basic Operational Principle

The basic operational principle of the SI-MIMO buck converter is shown in Fig. 1(b). There are only one input channel and one output channel connected to the shared inductor at a

Fig. 2. Block diagram of the proposed deadbeat-based method for the SI-MIMO converter.

given time instant, so that it is a simple buck converter. For instance, the j th input channel and the i th output channel are selected to connect to the shared inductor. In other words, the TMS is adopted to select the input and output channels [8], [9], [15]. In the next section, the method for selecting the input and output channels to achieve ICR and OVR of the SI-MIMO buck converter will be discussed in details.

III. DEADBEAT-BASED METHOD

Based on the TMS, ICR and OVR requirements related approaches are developed to determine which input or output channel is connected to the shared inductor. The ICR and OVR approaches form the deadbeat-based method. Fig. 2 presents the overall block diagram of the proposed method.

A. Input Current Regulation Approach

1) *Average Input Current Calculation:* As shown in the ICR block in Fig. 2, the ICR approach is actually controlling the average input current $\bar{i}_{in,j}$ of $i_{in,j}$ to track the current reference $i_{ref,j}$. The moving average filter (MAF) is employed to calculate $\bar{i}_{in,j}$ in real time. The MAF can be implemented as a low-pass filter (LPF) with a time window of T_{MAF} [20], [21]. The relationship between $\bar{i}_{in,j}$ of $i_{in,j}$ in the discrete-time domain is

expressed as follows:

$$\bar{i}_{in,j}(k) = \frac{\sum_{l=0}^{N_{MAF}} i_{in,j}(k-l)}{N_{MAF}} \quad (1)$$

and the integer N_{MAF} is given as

$$N_{MAF} = \frac{T_{MAF}}{t_s} \quad (2)$$

where t_s is the sampling time of the proposed method. In other words, T_{MAF} is the integral times of t_s .

2) *Control Signal Generation for ICR:* The pulsewidth modulation (PWM) duty ratio of the j th input channel is defined as δ_j to generate the control signal p_j for the switch P_j . As shown in the ICR block diagram in Fig. 2, after the MAF, $\bar{i}_{in,j}$ is sent to the proportional-integral (PI) controller with the reference $i_{ref,j}$, so δ_j is obtained as follows:

$$\delta_j = k_p (i_{ref,j} - \bar{i}_{in,j}) + k_i \int (i_{ref,j} - \bar{i}_{in,j}) dt \quad (3)$$

where k_p and k_i are the PI coefficients. Because of the adoption of FCBB and when multiple input power sources are connected to the shared inductor simultaneously, only the power source with the highest voltage will be conducted and the other power sources are blocked [8]. Therefore, strictly conducting the multiple input power sources in sequence and exclusively is

Fig. 3. Control scheme of the ICR control signals.

imperative to a successful ICR. To achieve this goal, the accumulated duty ratio δ'_j ($j = 1, 2, \dots, m$) is defined and expressed as follows:

$$\delta'_j = \sum_{k=1}^j \delta_k, \quad 1 \leq j \leq m, \quad 0 \leq \delta_k \leq 1. \quad (4)$$

Similarly, the temporary control signals ($p'_1, p'_2, \dots, p'_j, \dots, p'_m$) are defined and generated using the synchronized PWM generator with the duty ratios ($\delta'_1, \delta'_2, \dots, \delta'_j, \dots, \delta'_m$). To generate the ICR control signals ($p_{s1}, p_{s2}, \dots, p_{sj}, \dots, p_{sm}$), the logic XOR gates are required, as shown in Fig. 2. Hence, p_{sj} is given as follows:

$$\begin{cases} p_{s1} = p'_1 \\ p_{sj} = p'_j \text{ XOR } p'_{j-1}, \quad 2 \leq j \leq m. \end{cases} \quad (5)$$

Specifically, p_1 is directly obtained since $v_{in,1}$ is the first power source to be connected to the shared inductor. The control scheme of ($p_{s1}, p_{s2}, \dots, p_{sj}, \dots, p_{sm}$) is shown in Fig. 3. Note that the period of ($p_{s1}, p_{s2}, \dots, p_{sj}, \dots, p_{sm}$) is t_{ps} , which is the integral times of t_s . It can be seen from Fig. 3 that ($p_{s1}, p_{s2}, \dots, p_{sj}, \dots, p_{sm}$) generated from (5) can strictly turn ON the switches ($P_1, P_2, \dots, P_j, \dots, P_m$) in Fig. 1 in sequence and exclusively. Meanwhile, the turn-ON duration for P_j is guaranteed as $\delta_j t_{ps}$, so that the input current $\tilde{i}_{in,j}$ can be regulated to its target $i_{Ref,j}$. In other words, without the XOR process in (5), ($P_1, P_2, \dots, P_j, \dots, P_m$) will be turned ON simultaneously and all the input channels will be connected to the shared inductor at the same time. Consequently, according to [8], the input channels with a lower voltage will be blocked and their ICR will fail due to FCBB. Therefore, the XOR process in (5) is imperative for a successful ICR.

The real applicable control signals ($p_1, p_2, \dots, p_j, \dots, p_m$) for the switches ($P_1, P_2, \dots, P_j, \dots, P_m$) are generated as the logical conjunction of ($p_{s1}, p_{s2}, \dots, p_{sj}, \dots, p_{sm}$) and p_{db} , as

shown in the following equation, where p_{db} is obtained by the OVR strategy and it will be elaborated in the following section:

$$p_j = p_{sj} \text{ AND } p_{db}, \quad 1 \leq j \leq m. \quad (6)$$

This is because the basic unit of the converter in Fig. 1 is a buck converter, and the OVR control signal p_{db} is implemented on the switches ($P_1, P_2, \dots, P_j, \dots, P_m$). With the knowledge of the control signals ($p_1, p_2, \dots, p_j, \dots, p_m$), the input voltage v_{in} for the shared inductor is obtained as follows:

$$v_{in} = \sum_{j=1}^m p_j \cdot v_{in,j}. \quad (7)$$

B. Output Voltage Regulation Approach

1) *Output Channel Selection:* As the TMS is adopted, selecting the output channel to connect the shared inductor at every control cycle is critical. One simple and effective method is selecting the output channel with the most urgent power demand, which can be expressed in the form of priority as follows:

$$pr_i > pr_k, \text{ if } v_{out,i} - v_{Ref,i} \leq v_{out,k} - v_{Ref,k} \quad (8)$$

where pr_i and pr_k denote the priorities of the i th and j th output channel, respectively. Therefore, the channel with the highest priority $pr_{\max}$ can be determined by comparing all priorities. This can be expressed as follows:

$$\begin{cases} q_i = 1, & \text{if } pr_i = pr_{\max} \\ q_i = 0, & \text{if } pr_i < pr_{\max}. \end{cases} \quad (9)$$

2) *Control Signal Generation for OVR:* After the selection of the i th output channel, the deadbeat control strategy is employed to regulate the output voltage $v_{out,i}$. The deadbeat control method can manipulate the duty ratio to steer the output voltage to its reference in the next cycle, so that $v_{out,i}$ can track $v_{Ref,i}$ tightly. Moreover, the regulation of the selected output voltage $v_{out,i}$ is achieved by a proper control of inductor current i_L , so that $v_{Ref,i}$ needs to be transformed into inductor current reference $i_{L,Ref}$. In this paper, $i_{L,Ref}$ is determined based on the dynamic input-output energy balance and voltage regulation error. The dynamic energy balance among the shared inductor, filter capacitor, and load of the selected i th channel in two adjacent control cycles k and $k+1$ can be expressed as follows:

$$\frac{1}{2} L i_L^2(k+1) - \frac{1}{2} L i_{out,i}^2(k) = \frac{1}{2} C v_{out,i}^2(k+1) - \frac{1}{2} C v_{out,i}^2(k). \quad (10)$$

The input-output energy balance equation indicates that the inductive energy through the shared inductor can be divided into the load feeding energy and capacitive energy change. Moreover, $i_L(k+1)$ and $v_{out,i}(k+1)$ in (10) should be equal to their targets, i.e., the inductor current reference $i_{L,Ref}$ and output voltage reference $v_{Ref,i}$, respectively. Hence, (10) can be rewritten as

$$\frac{1}{2} L i_{L,Ref}^2 - \frac{1}{2} L i_{out,i}^2(k) = \frac{1}{2} C v_{Ref,i}^2(k+1) - \frac{1}{2} C v_{out,i}^2(k). \quad (11)$$

Accordingly, the inductor current reference $i_{L,\text{Ref}}$ can be calculated from (11) with the knowledge of output current $i_{\text{out},i}$ as follows:

$$i_{L,\text{Ref}} = \sqrt{\frac{C}{L} [v_{\text{Ref},i}^2 - v_{\text{out},i}^2(k)] + i_{\text{out},i}^2(k)}. \quad (12)$$

It is noted that (12) is derived based on the assumption of ideal devices without any power loss. In practical implementation, the power loss of the inductor, capacitors, and switches cannot be avoided and this results in deviations between the actual inductor current demand and the inductor current reference $i_{L,\text{Ref}}$ calculated in (12). To compensate for these deviations, an integral term of the OVR error is added into (12) so that it can be rewritten as follows:

$$i_{L,\text{Ref}} = \sqrt{\frac{C}{L} [v_{\text{Ref},i}^2 - v_{\text{out},i}^2(k)] + i_{\text{out},i}^2(k)} + kc_i [v_{\text{Ref},i} - v_{\text{out},i}(k)]. \quad (13)$$

With (13), $i_{L,\text{Ref}}$ can be adjusted with the integral term using a proper range to help it converge to the correct value of the actual inductor current demand. The integral gain kc_i is generally chosen as a small positive constant, i.e., $kc_i = 10^{-4}$ in this paper.

Based on the real-time calculated $i_{L,\text{Ref}}$, deadbeat current control can be implemented. The deadbeat control is derived based on the state-space equation

$$L \frac{di_L(t)}{dt} = v_{\text{in}}(t)d_{db}(t) - v_{\text{out},i}(t). \quad (14)$$

By discretizing (14) with the forward Euler's method, it can be rewritten as follows:

$$L \frac{i_{L,\text{Ref}} - i_L(k)}{t_s} = v_{\text{in}}(k)d_{db}(k) - v_{\text{out},i}(k). \quad (15)$$

From the control point of view, $i_L(k+1)$ should be equal to $i_{L,\text{Ref}}$ to achieve a successful regulation. By replacing $i_L(k+1)$ as $i_{L,\text{Ref}}$, $d_{db}(k)$ can be obtained for the desired deadbeat duty cycle as follows:

$$d_{db}(k) = \frac{v_{\text{out},i}(k)t_s + L[i_{L,\text{Ref}} - i_L(k)]}{v_{\text{in}}(k)t_s}. \quad (16)$$

It can be seen from (16) that the duty cycle is calculated based on the real-time data, so that the SI-MIMO buck converter is regulated using the optimal duty cycle in every control cycle. This contributes toward the fast dynamic response for the proposed deadbeat-based method.

The current derivative term in (14) makes the generation of d_{db} sensitive to measurement noises. Hence, a nonideal generalized integrator is utilized to replace the purely derivative term in the s domain with a highly accurate approximation and a slight phase error, as shown in (17). The design guideline of this filter is discussed in [22]

$$\frac{1}{s}i_L(s) \approx \frac{\omega_1^2}{s^2 + \omega_2 s + \omega_1^2}i_L(s) \quad (17)$$

where ω_1 represents the frequency with the largest but finite gain, and ω_2 denotes the cutoff frequency that helps attenuate

the peak gain in the frequency response. In this paper, ω_1 is chosen as $2\pi \times 20$ krad/s to provide a broad derivative range, and ω_2 is set at $2\pi \times 10$ krad/s.

Based on the above discussion, d_{db} for the selected i th output channel can be calculated using the values of $i_{L,\text{Ref}}$, $v_{\text{out},i}$, $i_{\text{out},i}$, $v_{\text{Ref},i}$, v_{in} , and C_i . The corresponding control signal p_{db} can be obtained by comparing d_{db} with a sawtooth waveform of period t_s . Then, p_{db} is applied into (6) to generate $(p_1, p_2, \dots, p_j, \dots, p_m)$ to regulate the output voltage $v_{\text{out},i}$. In previous works, the output current $i_{\text{out},i}$ is directly measured via the current sensors [15], which will significantly increase the cost when there is a large number of output channels. To avoid such a cost increase, a simple current observer is employed and discussed in following section.

3) Observer for the Output Current: Mathematically, the output voltage equation of the selected output channel can be described by

$$C \frac{dv_{\text{out},i}(t)}{dt} = i_L(t) - i_{\text{out},i}(t). \quad (18)$$

Based on (18), it is feasible to observe the output current $i_{\text{out},i}$ with the measurement of i_L and $v_{\text{out},i}$. However, the existence of the voltage derivative term in (18) introduces noises to the observer. Moreover, the output current $i_{\text{out},i}$ usually varies much slower than the inductor current i_L , considering that most loads do not vary drastically. A first-order LPF with a comparatively low cutoff frequency can be applied to $i_{\text{out},i}$, which is shown in (18) in the Laplace domain

$$\hat{i}_{\text{out},i}(s) = [i_L(s) - C_i s v_{\text{out},i}(s)] \times \frac{\omega_o}{s + \omega_o} \quad (19)$$

where $\hat{i}_{\text{out},i}$ is the observed output current, and s and ω_o denote the differential operator and the angular cutoff frequency. By applying the bilinear transform to (19), $\hat{i}_{\text{out},i}(k)$ can be expressed using a modification by the control signal q_i in

$$\begin{aligned} \hat{i}_{\text{out},i}(k) = & a_1 \hat{i}_{\text{out},i}(k-1) + a_2 [q_i(k)i_L(k) + q_i(k-1)i_L(k-1)] \\ & + a_3 [v_{\text{out},i}(k) - v_{\text{out},i}(k-1)] \end{aligned} \quad (20)$$

where the coefficients a_1 , a_2 , and a_3 are given as follows:

$$a_1 = \frac{2 - \omega_o t_s}{2 + \omega_o t_s}; \quad a_2 = \frac{\omega_o t_s}{2 + \omega_o t_s}; \quad a_3 = \frac{-2\omega_o C_i}{2 + \omega_o t_s}.$$

The presence of $q_i(k)$ and $q_i(k-1)$ in (20) is due to the adoption of the TMS, which determines when the i th output channel can be connected to the shared inductor. Moreover, the observer in (20) is applicable to not only the selected output channel but also all the output channels because (20) considers $q_i(k)$ and $q_i(k-1)$. The observed output current $\hat{i}_{\text{out},i}(k)$ will be utilized to replace the value of $i_{\text{out},i}$ in (13) as follows:

$$i_{L,\text{Ref}} = \sqrt{\frac{C}{L} [v_{\text{Ref},i}^2 - v_{\text{out},i}^2(k)] + \hat{i}_{\text{out},i}^2(k)} + kc_i [v_{\text{Ref},i} - v_{\text{out},i}(k)]. \quad (21)$$

The structure of the current observer is given in the OVR block diagram in Fig. 2.

Fig. 4. Control scheme of the proposed deadbeat-based method based on the SI-DIDO converter.

C. Control Scheme of the Deadbeat-Based Method

To illustrate the control mechanism of the proposed method, the SI-DIDO buck converter is taken as an example and the corresponding control scheme is presented in Fig. 4 showing the waveforms of q_1 , q_2 , i_L , p_{db} , p_{s1} , p_{s2} , p_1 , and p_2 . It can be seen that q_1 and q_2 are dynamically adjusted based on the priorities, and p_{db} is generated using (16) with a fixed period but a varying duty ratio. The varying slopes of i_L result from the different values of input voltage, output voltage. Moreover, p_{s1} and p_{s2} are the envelopes of p_1 and p_2 , respectively, because p_1 (p_2) is the logical conjunction of p_{s1} (p_{s2}) and p_{db} .

IV. COMPONENT DESIGN AND PERFORMANCE INDEX

A. Selection of LC Components

The values of the inductor and capacitors for the SI-MIMO buck converter in this paper are determined as follows [12]:

$$L = (v_{in,j} - v_{out,i}) \times \frac{v_{out,i}}{v_{in} f_{sw} \Delta i_L} \quad (22)$$

$$C_i = \frac{L(i_{out,i} + 0.5\Delta i_L)^2}{(v_{out,i} + \Delta v_i)^2 - v_{out,i}^2} \quad (23)$$

where f_{sw} is the switching frequency, which is equal to $1/t_s$, Δv_i is the ripple of the i th output voltage, and Δi_L is the ripple of the inductor current. Due to different values of $v_{in,j}$ and $v_{out,i}$, (22) and (23) will generate a series number of values of L and C_i . According to [8], the final value of L or C_i should be selected as the maximum value among the different calculated outcomes from (22) or (23), so that the SI-MIMO buck converter can work successfully for all input channels and output channels.

B. Performance Index

Several indices have been defined in [15] to quantify the regulation performance of the SI-MIMO dc-dc converter. These

TABLE I
SETTING OF THE SI-DIDO BUCK CONVERTER

Symbol	$v_{in,j}$	$v_{out,i}$	R_i	t_s	f_{sw}
Value	18, 22 V	8, 12V	5.16~10Ω	12.5μs	80kHz
Symbol	t_{PS}	L	C	T_{MAF}	ω_o
Value	50μs	100μH	220μF	1ms	1200π rad/s

Fig. 5. Prototype of the SI-DIDO buck converter.

indices are employed in this paper to estimate the performance of the proposed deadbeat-based method in terms of ICR and OVR. For the ICR performance estimation, the performance index to input voltage step change and the performance index to input current step change are expressed as follows:

$$S_{vin,j}^{vout,i} = \frac{|\Delta v_{out,i}|}{|\Delta v_{in,j}|} \times \frac{v_{in,j}}{v_{out,i}} \quad (24)$$

$$S_{iin,j}^{vout,i} = \frac{|\Delta v_{out,i}|}{|\Delta \bar{i}_{in,j}|} \times \frac{\bar{i}_{in,j}}{v_{out,i}} \quad (25)$$

where $\Delta v_{out,i}$ is the shift of the average voltage of the i th output channel, $\Delta v_{in,j}$ is the variation of the input voltage of the j th input channel, and $\Delta \bar{i}_{in,j}$ is the variation of the average current of the j th input channel. Similarly, the performance indices for OVR are defined as FOM (self) and FOM (cross) as follows:

$$\text{FOM}(\text{self}) = \frac{|\Delta v_{out,i}|}{|\Delta i_{out,i}|} \times \frac{i_{out,i}}{v_{out,i}} \quad (26)$$

$$\text{FOM}(\text{cross}) = \frac{|\Delta v_{out,j}|}{|\Delta i_{out,j}|} \times \frac{i_{out,j}}{v_{out,j}} \quad (27)$$

where the i th channel and the j th channel are the self-channel and the cross channel, respectively.

V. SIMULATION AND EXPERIMENTAL RESULTS

To validate the performance of the deadbeat-based method, the SI-DIDO buck converter is developed via the software and hardware setup. The setting of the SI-DIDO buck converter is tabulated in Table I, and an experimental prototype is shown in Fig. 5. The devices adopted in the experimental prototype and the controllers for the implementation of the proposed deadbeat-based method are listed in Table II. It is noted that the logical XOR between p'_j and p'_{j-1} in (5) is achieved in dSpace Micro-LabBox via the XOR function module, and the logical AND

TABLE II
MAIN COMPONENTS ADOPTED IN A PROTOTYPE

Component	Device
MOSFET switch (P_1, P_2, Q_1, Q_2)	IRF540
MOSFET driver	HCPL-J314
AND gate	HD74HC08
Diode (D)	MBRB60H100CT
Inductor (L)	1140-101K-RC
Current transducer ($i_{in,1}, i_{in,2}$)	LAH 25-NP
DSP controller (OVR)	TI TMS320F28335
dSpace (ICR)	MicroLabbox

Fig. 6. Simulation results of a current observer of the proposed deadbeat-based method.

between p_{sj} and p_{db} in (6) is realized by the HP74HC08P AND gate, which is listed in Table II and shown in Fig. 5. The values of L and C are calculated based on (22) and (23).

A. Simulation Results

The performance of the output current observers is worth investigating, since the observers are critical to the determination of the inductor current reference value for OVR. Due to the fact that the observed current cannot be directly measured in experiments, the corresponding simulation study is conducted to compare the actual and the observed values of the output current. The simulation results are shown in Fig. 6. The output voltages are set as $v_{out,1} = 8.0$ V and $v_{out,2} = 12.0$ V, and the output currents are $i_{out,1} = 0.8$ A and $i_{out,2} = 1.2$ A. The waveforms of the actual currents $i_{out,1}$ and $i_{out,2}$ and the observed currents $\hat{i}_{out,1}$ and $\hat{i}_{out,2}$ are presented in subplots 3 and 4 in Fig. 6. Moreover, a load step change occurs in R_2 when its value is decreased from 10 to 5 Ω at $t = 0.25$ s. It can be seen that the observed current of the two channels can track their actual current tightly, even during a step load change. Moreover, the two observed currents are barely affected by each other, which

Fig. 7. Overall simulation results of the proposed method, including responses to input current step change, input voltage step change, and load step change.

contributes to the excellent independent OVR performance for the two output channels.

The overall simulation results of the proposed method are presented in Fig. 7, including the responses to input current step change, input voltage step change, and the load step change. First, there is a step change set in $i_{Ref,1}$ from 0.5 to 0.7 A at $t = 0.2$ s, so that $\bar{i}_{in,1}$ is increased accordingly. Because the values of input voltages $v_{in,1}$ and $v_{in,2}$, output voltages $v_{out,1}$ and $v_{out,2}$, and output currents $i_{out,1}$ and $i_{out,2}$ are fixed, $\bar{i}_{in,2}$ is reduced from 0.95 to 0.75 A to balance the total input power. Then, a step change is set at $v_{in,1}$ from 18 to 22 V at $t = 0.4$ s. Similarly, $\bar{i}_{in,2}$ is reduced to 0.63 A due to the fact that the other parameters are fixed. Finally, the load R_1 is decreased from 10 to 5 Ω at $t = 0.6$ s. Consequently, $i_{out,1}$ is increased from 0.8 to 1.6 A and $\bar{i}_{in,2}$ is increased to 1.1 A to meet the load demand. It can be seen from the second subplot in Fig. 7 that the output voltages $v_{out,1}$ and $v_{out,2}$ are regulated to track their references, i.e., 8 and 12 V, by the proposed deadbeat-based method against the step changes introduced.

B. Steady-State Operation

1) *Steady-State Waveforms*: Fig. 8 presents the steady-state waveforms of the SI-DIDO buck converter. The output voltages are $v_{out,1} = 8.0$ V and $v_{out,2} = 12.0$ V. Accordingly, the output currents are $i_{out,1} = 0.79$ A and $i_{out,2} = 1.18$ A. The input currents are represented by the voltage signals from the MicroLab-Box controller, which are processed by the MAF implemented in the controller. It can be seen from Fig. 8 that the values of average input current are $\bar{i}_{in,1} = 0.92$ A and $\bar{i}_{in,2} = 0.47$ A. In addition, the output voltage ripples are 280 mV and 350 mV, which are 5% and 4% of the corresponding voltage references. The waveforms in Fig. 8 indicate that the proposed method controls the SI-MIMO converter with ICR and OVR effectively.

Fig. 8. Steady-state waveforms of the SI-DIDO buck converter.

Fig. 9. Control scheme of the proposed deadbeat-based method.

2) *Control Signal Waveforms*: The waveforms of control signals q_1 , q_2 , p_{db} , p_{s1} , p_{s2} , p_1 and p_2 , and i_L in the steady-state operation are presented in Fig. 9 to explain the operation of the deadbeat-based method. The control signals q_1 and q_2 are dynamically adjusted based on the real-time priorities p_{r1} and p_{r2} . Consequently, the slopes of i_L vary due to the different values of R_1 and R_2 . In addition, the duty cycle of p_{db} is adjusted by the OVR approach according to the measured inductor current, the selected output voltage, the corresponding voltage reference, and the observed output current. It can be observed that the switching frequency of p_{db} is 80 kHz. The control signals p_{s1} and p_{s2} are manipulated by the ICR approach with a fixed switching frequency of 25 kHz. With the assistance of the logical AND gate, the p_1/p_2 waveform is generated as the logical conjunction of p_{db} and p_{s1}/p_{s2} . This can be reflected that p_{s1} and p_{s2} are the envelopes of p_1 and p_2 , respectively. It can be seen that the experimental results of the controls signals follow the theoretical analysis of the control scheme in Fig. 3 tightly.

(a)

(b)

Fig. 10. Input current step change of the proposed deadbeat-based method. (a) Step change in $i_{Ref,1}$ from 1.0 to 0.5 A, and back to 1.0 A. (b) Step change in $i_{Ref,1}$ from 0.5 to 0 A.

Hence, the proposed method can effectively achieve ICR and OCR simultaneously.

C. Dynamic Operation

1) *Response to Input Current Step Change*: To verify the performance of ICR, the input current step change experiment is conducted, and the experimental results are presented in Fig. 10.

In Fig. 10(a), the initial setting is $i_{Ref,1} = 1.0$ A, $v_{Ref,1} = 8.0$ V, and $v_{Ref,2} = 12.0$ V, and corresponding values are $\bar{i}_{in,1} = 0.95$ A, $v_{out,1} = 8.1$ V, and $v_{out,2} = 12.0$ V. A sudden increment of $i_{Ref,1}$ from 1.0 to 0.5 A is set at t_1 , as shown in the left side in Fig. 10(a). It can be seen that $\bar{i}_{in,1}$ is regulated from 0.95 to 0.50 A to track the reference. Accordingly, to compensate the reduced power from the input power source $v_{in,1}$, the input current $\bar{i}_{in,2}$ is automatically increased from 0.43 to 0.81 A, so that $v_{in,2}$ will deliver more power to meet the load demand. It is visible that the step change in $i_{in,1}$ leads to disturbances on $v_{out,1}$ and $v_{out,2}$, which are reflected by the average voltage values

Fig. 11. Input voltage step change of the proposed deadbeat-based method.

shift of $\Delta v_{out,1} < 20$ mV and $\Delta v_{out,2} = 50$ mV, as shown in the zoom-in figures in Fig. 10(a). A subsequent step up of $i_{Ref,1}$ from 0.5 to 1.0 A is implemented at t_2 to further investigate the response of the proposed deadbeat-based method. From the right side in Fig. 10(a), it can be observed that $\bar{i}_{in,1}$ and $\bar{i}_{in,2}$ recover back to 0.92 and 0.45 A, respectively. Similarly, there are negligible disturbances on $v_{out,1}$ and $v_{out,2}$, and the absolute values of $\Delta v_{out,1}$ and $\Delta v_{out,2}$ are close to the corresponding values of the disturbances on the output voltage at t_1 . In practical situations, variations of input power sources availability occasionally happen. The SI-MIMO converter should be functional when there is an absence of input power source. Hence, the step change of $i_{Ref,1}$ from 0.5 to 0 A at t_1 has been conducted, as shown in Fig. 10(b). Consequently, $\bar{i}_{in,1}$ and $\bar{i}_{in,2}$ are regulated from 0.49 to 0.0 A and 0.90 to 1.35 A, respectively. The output voltages $v_{out,1}$ and $v_{out,2}$ are disturbed with $\Delta v_{out,1} < 30$ mV and $\Delta v_{out,2} < 20$ mV.

2) *Response to Input Voltage Step Change:* The SI-MIMO converter can be utilized to integrate the input power sources with varying voltage, for example, the photovoltaics system. Hence, the step change of the input voltage is conducted to verify the performance of the proposed method for the integration of varying input voltage, and the experimental results are presented in Fig. 11. It can be observed that the initial values are $\bar{i}_{in,1} = 0.51$ A, $v_{out,1} = 8.1$ V, and $v_{out,2} = 12.0$ V, and $v_{in,1}$ are set from 18.0 to 22.0 V at t_1 . Consequently, $\bar{i}_{in,2}$ is decreased from 0.85 to 0.68 A to maintain the input power since $\bar{i}_{in,1}$ is regulated at 0.51 A. The step change in the input voltage has impacted the two output voltages. One impact is that the output voltage ripples become larger due to the unbalanced input voltage values, i.e., Δv_1 is increased from 380 to 420 mV, and Δv_2 is increased from 300 to 350 mV. The other influence is that the average voltage values are shifted upwards with $\Delta v_{out,1} < 50$ mV and $\Delta v_{out,2} < 20$ mV, as shown in the zoom-in figures.

3) *Load Regulation:* The load regulation is implemented in two output channels to examine the OVR performance of the proposed deadbeat-based method. The experimental results are presented in Fig. 12, with the initial settings of $i_{Ref,1} = 1.0$ A,

(a)

(b)

Fig. 12. Load step change of the proposed deadbeat-based method. (a) Step change in output channel 1. (b) Step change in output channel 2.

$v_{Ref,1} = 8.0$ V, and $v_{Ref,2} = 12.0$ V. In Fig. 12(a), a step change is set on R_1 from 10 to 5.16 Ω at t_1 , so that $i_{out,1}$ is increased from 0.79 to 1.55 A, i.e., 96% in load increment. It can be seen from the zoom-in figures in Fig. 12(a) that the average voltage value of $v_{out,1}$ has a drop of $\Delta v_{out,1} = 200$ mV, and the average voltage value of $v_{out,2}$ is also decreased by $\Delta v_{out,2} = 50$ mV because of cross regulation. Due to the sudden rising in load demand, $\bar{i}_{in,2}$ is increased from 0.50 to 0.90 A because $i_{Ref,1}$ is set as 1.0 A. At t_2 , R_1 is set back to 10 Ω , so that the previous values of $v_{out,1}$, $v_{out,2}$, $i_{out,1}$, and $\bar{i}_{in,2}$ are restored.

A similar 87.3% load step increment is implemented in the second output channel by setting R_2 from 10 to 5.43 Ω at t_1 , as shown in Fig. 12(b). Due to a comparatively higher value of $v_{out,2}$, such a load step increment results in a larger average voltage drop on $v_{out,2}$. The value is $\Delta v_{out,2} = 200$ mV, as shown in the upper zoom-in figure in Fig. 12(b). The cross regulation between the two output channels leads to the average voltage drop on $v_{out,1}$, which is $\Delta v_{out,1} = 150$ mV, as shown in the lower zoom-in figure in Fig. 12(b). In addition, to

TABLE III
COMPARISON WITH PREVIOUS WORKS

Reference	[5]	[8]	[10]	[12]	[15]	Proposed Work
Process	Discrete Components	Discrete Components	0.35 μ m CMOS	0.18 μ m CMOS	Discrete Components	Discrete Components
Input Voltage	35, 48V	30, 20V	2~4V, 3.7~4.2V	1.5V, 2.5V	24, 20V	18, 22V
Output Voltage	80, 40V	21,8V	1.8V, 3.7~4.2V	1.0V, 1.8V	12, 8~10V	12, 8V
Load Current	0.63~1.18, 1.2~2.36A	0.84~1.18, 1.33A	9mA	3 μ A, 1 μ A	1.2~2.4, 0.8~1.6A	1.18~2.21, 0.79~1.55A
Output Power	121, 236W	35.4W	~18mW	400nW	35W	33W
f_{sw}	10kHz	40kHz	147kHz	10kHz	20~100kHz	80kHz
L	2mH	250 μ H	47 μ H	10 μ H	100 μ H	100 μ H
C	1000 μ F	2200 μ F	1 μ F	10 μ F	220 μ F	220 μ F
FOM (self)	-	0.238	0.167	-	0.022	0.026 0.019
FOM (cross)	-	-	-	-	0.025	0.004 0.021
$S_{iin,1}^{vout,1}, S_{iin,1}^{vout,2}$	-	-	-	-	0.017, 0.016	0.0063 , <0.0025
$S_{vin,1}^{vout,1}, S_{vin,1}^{vout,2}$	-	0.625, -	0.85, -	-	0.042, -	<0.0025 , <0.0042
Current Sensor Number	-	-	-	-	$n+m$	m
Extension capability for arbitrary inputs/outputs	Yes	Yes	No	No	Yes	Yes

compensate the increasing load demand, $\bar{i}_{in,2}$ is increased from 0.49 to 1.35 A since $\bar{i}_{in,1}$ is maintained at its fixed reference value of $v_{Ref,1} = 1.0$ A. The value of R_2 is changed from 5.43 to 10 Ω at t_2 . Accordingly, the previous values of $v_{out,1}$, $v_{out,2}$, $i_{out,1}$, and $\bar{i}_{in,2}$ are restored.

D. Comparison With Previous Works

To further illustrate the performance of the proposed deadbeat-based method for the SI-MIMO dc–dc converter, the comparison between the proposed method and the existing methods is conducted. The comparison results are presented in Table III.

By comparing the key performance indices in Table III, the excellent performance of the proposed method can be clearly seen. It is noticeable that the output power of this work is 33 W, which is similar to [8] of 35.4 W and [15] of 35 W. The power level of this work determines the selection of the switching frequency as 80 kHz, inductor as 100 μ H, and output capacitor as 220 μ F, which are similar to the values in [8] and [15]. Although one FOM (self) index 0.026 is higher than the corresponding index of 0.022 in [15], the other indices including FOM (cross), $S_{iin,1}^{vout,1}$, $S_{iin,1}^{vout,2}$, $S_{vin,1}^{vout,1}$, and $S_{vin,1}^{vout,2}$ of the proposed method are all lower than those of all the other methods. These performance indices indicate that the proposed method possesses excellent transient response including the step changes of input current, input voltage, and load. In other words, the deadbeat-based method is superior to the previous method compared for ICR and OVR of the SI-MIMO dc–dc converter. The number of current sensors in this work is also much less than that of the previous work in [15], which is the benefit due to the adoption of the output current observers. Additionally, the capability of the extension is also compared in Table III. It can be seen that [5], [8], [15], and this work can be easily extended because the designed methods are developed with the consideration of an

arbitrary number of input or output channels. Moreover, considering that the multivariable PID method is adopted in [8] and the MPC method is adopted in [15], the complexity of the proposed deadbeat method is medium since PID is simpler in terms of implementation, while MPC requires high computational resources [15]. In summary, the deadbeat-based method is promising in controlling the SI-MIMO dc–dc converter to achieve ICR and OVR.

VI. CONCLUSION

This paper proposes a deadbeat-based method for the SI-MIMO dc–dc converter to achieve ICR and OVR simultaneously. The advantages of the proposed method include low computational complexity and fast dynamic response. In addition, the current observers are developed for the output channels of the SI-MIMO dc–dc converter to reduce the implementation cost without sacrificing the performance of OVR. An SI-DIDO buck converter hardware prototype is built for validation of the proposed method. The steady-state and dynamic operation, and a comparison with previous works are conducted. Experimental and comparison results demonstrate the excellent performance of the deadbeat-based method for ICR and OVR of the SI-MIMO dc–dc converter.

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Benfei Wang (S'12–M'17) received the B.Sc. degree in electronic information science and technology from the University of Science and Technology of China, Hefei, China, in 2011, and the Ph.D. degree from the Nanyang Technological University (NTU), Singapore, in 2017.

He is currently a Research Fellow with the Energy Research Institute, NTU. His research interests include model predictive control, multiport dc-dc converter, hybrid energy storage system, and microgrids.

Xinan Zhang (S'10–M'14) received the B.E. degree in electrical engineering and automation from Fudan University, Shanghai, China, in 2008, and the Ph.D. degree from the Nanyang Technological University (NTU), Singapore, in 2014.

Then, he worked as a Postdoc Researcher with the NTU and the University of New South Wales, from 2014 to 2017. He joined the NTU as a Lecturer in June 2017. His research interests include electrical machine drives, control and modulation of power electronic converters, and management of hybrid energy storage systems.

Jian Ye (S'15) received the B.Eng. degree in electrical engineering from Wuhan University, Wuhan, China, in 2012, and the M.Sc. degree in 2013 from the Nanyang Technological University, Singapore, where he is currently working toward the Ph.D. degree at the School of Electrical and Electronic Engineering.

His research interests include power electronics for various applications such as connecting renewable energy sources, energy devices to microgrids, and power quality compensation.

Hoay Beng Gooi (SM'95) received the Ph.D. degree in electrical engineering from Ohio State University, Columbus, OH, USA, in 1983.

From 1983 to 1985, he was an Assistant Professor with Lafayette College, Easton. From 1985 to 1991, he was a Senior Engineer with Empros (now Siemens), Minneapolis, where he was responsible for the design and testing coordination of domestic and international energy management system projects. In 1991, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, as a Senior Lecturer, where he has been an Associate Professor since 1999. He was the Deputy Head of the Power Engineering Division during 2008–2014. His current research interests include microgrid energy management systems dealing with energy storage, renewable energy sources, electricity market, and spinning reserve.

Dr. Gooi has been an Editor for the IEEE TRANSACTIONS ON POWER SYSTEMS since 2016.