Reliability-oriented design and control of DC-link capacitors in power converter systems

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**RELIABILITY-ORIENTED DESIGN AND CONTROL OF
DC-LINK CAPACITORS IN POWER CONVERTER
SYSTEMS**

LU NANJUN

**INTERDISCIPLINARY GRADUATE SCHOOL
ENERGY RESEARCH INSTITUTE @ NTU**

2020

**RELIABILITY-ORIENTED DESIGN AND CONTROL OF
DC-LINK CAPACITORS IN POWER CONVERTER
SYSTEMS**

LU NANJUN

INTERDISCIPLINARY GRADUATE SCHOOL

A thesis submitted to the Nanyang Technological
University in partial fulfilment of the requirement for the
degree of Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

23/1/2020

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Date

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Tang Yi

Authorship Attribution Statement

This thesis contains material from 3 papers published in the following peer-reviewed journal and conferences where I was the first author.

Chapter 3 is published as N. Lu, S. Yang, and Y. Tang, "Ripple Current Reduction for Fuel-Cell-Powered Single-Phase Uninterruptible Power Supplies," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6607-6617, Aug. 2017. DOI: 10.1109/TIE.2017.2677329.

The contributions of the co-authors are as follows:

- Asst. Prof Tang Yi provided the research idea and commented on the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Asst. Prof. Tang Yi and Dr. Yang Shunfeng.
- I co-designed the simulation with the help of Asst. Prof Tang Yi and Dr. Yang Shunfeng and performed all the laboratory work at the School of Electrical and Electronics Engineering. I also analyzed the data exported from the oscilloscope and conducted Fast Fourier Transform analysis on the results.
- All mathematical modeling, theoretical analysis, and the derived transfer functions of control diagrams were completed by me.
- Asst. Prof Tang Yi and Dr. Yang Shunfeng assisted in setting up the experimental prototype as well as conducting the experiments.
- Dr. Yang Shunfeng and Dr. Fang Jingyang assisted in addressing the questions and comments from the reviewers.

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The contributions of the co-authors are as follows:

- Asst. Prof Tang Yi provided the research idea and kept track of my progress.
- I wrote the drafts of the manuscript. The manuscript was revised by Asst. Prof Tang Yi.
- I performed all the simulations, conducted controller stability analysis, derived the control diagrams and their corresponding transfer functions.
- Asst. Prof Tang Yi and Mr. Zhang Lei assisted me in setting up the experimental prototype and conducting experiments.
- I collected data from the oscilloscope and prepared the data for Fast Fourier Transform analysis.

Chapter 4 is published as N. LU, J. Fang, Y. Tang and B. Hredzak, "A Frequency Deadband-Based Virtual Inertia Control for Grid-Connected Power Converters," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 1-6.

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- Asst. Prof Tang Yi provided the research idea and kept track of my progress.
- I wrote the drafts of the manuscript. The manuscript was revised by Dr. Fang Jinyang and Dr. Branislav Hredzak.
- I performed the simulations, conducted quantitative correlation analysis between variables, derived the control diagrams and their corresponding transfer functions.
- Dr. Fang Jinyang assisted me in conducting experiments.

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Abstract

One simple and intuitive approach to improving the reliability of power converter systems would be replacing the widely used electrolytic capacitors (E-Caps) with the more reliable film capacitors (F-Caps). The main shortcoming of F-Caps, however, is their low energy density. This means for the same amount of energy or capacitance required by power converters, the volume of F-Caps is much larger than that of E-Caps. On the other hand, large capacitance is typically required for high power dc-link applications due to the high instantaneous power difference and power oscillation managed by the dc-link capacitors. A feasible approach to condensing the volume of F-Caps is simply by reducing the capacitance required by the normal operations of power converters. Since the instantaneous power difference is determined by the power source and the load it supplies. The only way to lower the system requirement on capacitance is by mitigating the magnitude of ripple power processed by the dc-link capacitors. In addition, the ripple components existed in the dc current could significantly undermine the performance and even the operating lifetime of renewable energy sources (RESs) when utilized as the dc source.

To suppress current ripples in single-phase power converters powered by RESs, control-based active power decoupling methods are proposed by the thesis and applied to two practical cases. Both cases attempt to address uncommonly difficult situations revolving around current/voltage ripples in the context of RESs. The first case considers the multiple low-frequency ripple components in the point of power coupling (PCC) voltage introduced by the grid background harmonics. To address such issue in a photovoltaic (PV) powered grid-connected single-phase power converter, the design of the active power decoupling control has to consider both the distorted grid current as a result of the grid background harmonics as well as the ripple components penetrated into the dc current. The derivation of the control schemes employs the idea of virtual impedance to conceptually link the controller design to circuit configuration. The nature of the virtual impedance is a modified repetitive controller which is capable of compensating low-order current ripples at periodic frequencies. Through meticulous controller design, the ripple components in both currents are dramatically mitigated. More importantly, the effective current ripple suppression is achieved at a significantly

reduced dc-link capacitance, which allows the adoption of more reliable F-Caps for the purpose of balancing the instantaneous power difference and manage voltage variations at the dc link. The effectiveness of the proposed active power decoupling control design is verified by both experimental and simulated results.

The second case attends to the situation where nonlinear loads are supplied by fuel cells through power converters. The existence of nonlinear loads creates harmonic distortion that could penetrate into the dc current and affect the inner chemical reactions of fuel cells. To neutralize the adverse effect, a dual-mode control scheme design is proposed for single-phase differential inverter to combat current ripples. The proposed control scheme adopts a three-layer structure and regulates dc offset voltage, ac voltage, and dc current separately through closed-loop control. Two modified repetitive controllers are embedded in the control loops to provide even/odd-frequency periodic signals to track and compensate multiple even/odd-frequency current ripples. The proposed control design maintains equally excellent performance in current ripple suppression under both linear and nonlinear load conditions. Apart from the effective mitigation of low-frequency current ripples, the current ripples at the switching frequency are also successfully suppressed thanks to the proposed interleaved modulation. Note that the proposed control design also enables the inverter to operate normally under the significantly reduced capacitance. Hence, the more reliable F-Caps can be adopted in this case for voltage/current regulation. The effectiveness of the dual-mode active power decoupling control is verified experimentally by a 500 W single-phase differential inverter prototype in the laboratory.

Another reliability-oriented issue the thesis attempts to address is related to frequency regulation when the grid is connected to RESs through three-phase power converters. Unlike synchronous generators, renewable generators cannot provide rotating inertia when integrated to the grid. Consequently, excessive grid frequency deviations may occur in the event of generator tripping and/or load shedding. Fortunately, by proportionally associating the dc-link voltage of power converters with the grid frequency, the power converters can be controlled to produce virtual inertia for frequency support. Based on this idea, a frequency deadband-based controller is proposed to support frequency regulation by further increasing the virtual inertia generated from power converters. As a result, the frequency nadir is notably improved

and the energy required for inertia emulation is considerably reduced. In addition, the thesis also reveals that by embedding a frequency deadband into the system controller, the dc-link voltage only changes when the maximum frequency deviation exceeds the preset frequency deadband. Thus, unnecessary voltage changes under normal system operations can be avoided. The less frequent voltage change is the key to extending the operating lifetime of dc-link capacitors. Since capacitor is considered a reliability-critical electrical component in power converter systems, hence the proposed frequency deadband-based controller also contributes to improving the system reliability. Both simulations and experimental results demonstrate its effectiveness.

To further explore the impact of different system parameters on the value of frequency nadir, an artificial neural network (ANN) based approach is proposed to estimate the improved frequency nadir with respect to different system parameters. The ANN is trained to act as a surrogate model of power converters that maps four critical system parameters into frequency nadir. Compared to the conventional mathematical modeling-based approach, the ANN model demonstrates substantially higher accuracy in calculating the value of frequency nadir according to the simulation results. Besides, the ANN-based approach is capable of handling high-dimensional and even nonlinear relationship between the input and output data. Meanwhile, the proposed method is also found to be around four orders of magnitude faster than running a simulation model.

In the context of growing demand on renewable energy, power electronics has emerged to be a key enabling technology covering every corner of power generation, transmission, distribution, and energy storage. As renewable penetration continues to rise, the reliability-oriented research of power converter systems has demonstrated its unprecedented values from both economic and manufacturing point of view.

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Abbreviations

AC	Alternating Current
ANN	Artificial Neural Network
C-Cap	Ceramic Capacitor
CM	Common Mode
DC	Direct Current
DG	Distributed Generation
DM	Differential Mode
E-Cap	Electrolytic Capacitor
ESR	Equivalent Series Resistor
ESS	Energy Storage System
F-Cap	Film Capacitor
FFT	Fast Fourier Transform
GCC	Grid-Connected Converter
HPF	High Pass Filter
HVDC	High-Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law
LCOE	Levelized Cost of Electricity
LPF	Low Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
O&M	Operation and Maintenance
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PI	Proportional Integral
PM	Phase Margin
PLL	Phase-Locked-Loop
PV	Photovoltaic
PR	Proportional Resonant
PWM	Pulse Width Modulation

RES	Renewable Energy Source
R&D	Research and Development
RoCoF	Rate of Change of Frequency
SCR	Second-Order Ripple
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VSG	Virtual Synchronous Generator
ZOH	Zero-Order Hold

Chapter 1

Introduction

This chapter broadly touches the latest renewable installation trends worldwide and its implications to modern power systems. The highlight of this chapter sits on the underlying challenges faced by renewable generators when integrated to the grid or supplying loads through fast response power converters. A set of system reliability issues associated with power converter systems are reviewed and analyzed, which become the motivation of the thesis. In addition, the scope, objectives as well as main contributions of the thesis are also discussed in this chapter.

1.1 Background

Despite artificial intelligence, cryptocurrencies and their ramifications might have been dominating the headlines and buzzwords of every news media today, a come-back-to-earth fact to remember is that none of these technologies could run on their own, particularly without sufficient and reliable supply of electric power. On the other hand, the accelerating array of technological advances has also imposed higher requirements on the quality, efficiency, and reliability of electric power. A reliable and cost-efficient power supply is among the core agenda of virtually every organization today. In the meantime, the rollout of governmental policies in favor of clean energy as well as the trend of decarbonization of the economy is also driving the growing demand for renewable energy globally.

Solar and wind, among other renewables, are considered the ‘Energy Choices of 21st Century’ [1]. Today, the major economies worldwide are aggressively exploring the potentials of renewable energy to fuel their economic growths, technological advancement, and even social welfare. Taking China, the world 2nd largest economy for instance, when solar power conversion efficiency reaches 10%, this energy resource alone could produce 3200 TW.h electricity, while only occupying 0.23% of the nation’s territory. According to China’s *13th Five Year Plan*, hydropower installation capacity is projected to exceed 350 GW by 2020, followed by wind and solar with each being targeted at 200 GW and 100 GW, respectively [3]. In the United States (U.S.), more than 17% of electricity generation was provided by renewable energy resources in 2018,

Figure 1.1: 2000-2020 China’s installed capacity of solar and wind. [Taken from China Water Risk based on CEC, NEA.]

Figure 1.2: U.S. annual renewable generation, by fuel type (million megawatt hours) [4].

according to the Energy Information Administration (EIA). The organization also estimated that an additional 30 billion kWh of electricity was generated by small-scale solar photovoltaic (PV) systems last year [4]. Despite the dramatically growing utilization of solar energy, hydropower and wind are still the two leading renewable energy sources (RESs) that power the U.S. today. Hydropower accounted for 7% of total American electricity generation in 2018, seconded by wind's 6.6% share among other RESs [4]. In the emerging market, Chile has reached 20.8% share of renewables in the country's power portfolio at the beginning of 2019, according to the Ministry of Energy [5]. A breakdown of the statistics shows that a whopping 92% of the newly installed 715 MW capacity in Chile came from renewables in 2018. Unsurprisingly, solar and wind contributed a dominating 80% of the freshly installed capacity [5].

With the rapid growth of renewable-powered electricity generation worldwide, it becomes increasingly critical to ensure the reliability of power, particularly at its

Figure 1.3: Global renewable electricity production by region. [Source: International Energy Agency]

transmission and conversion stages. From the economic point of view, the cost of failures and regular operation and maintenance (O&M) could be humongous. Whereas, from the personnel safety perspective, even the smallest scale of system fault or failure could potentially result in disastrous consequences. Considering the massive costs of system failures, it is at all parties' interests to design and develop more reliable power electronic systems. As a fundamental interface between renewable energy generators and the grid, the reliability of power electronic converters is particularly worth the attention.

1.2 Motivation

The reliability of power electronic converters has caught much attention in both industries and academia due to its high stakes and costs. Across industries, the “failure per million/billion device hours [6]” is widely considered being equivalent to tens of thousands of dollars' loss per day or even per hour. The massive costs of system failures and besmirched reputation ensued are essentially what have been driving corporate efforts in pursuit of highly reliable systems. In the aerospace industry, for instance, even the tiniest reliability issue with the power electronic applications in an aircraft or satellite can lead to the catastrophic consequences, such as death toll, loss of critical information and millions of dollars. In the case of onshore wind farms, the operation and maintenance costs usually account for 20% of the total Levelized Cost of Electricity (LCOE), which could vary from \$12/MWh to \$25/MWh depending on different environmental conditions [7]. When the renewable generators are connected to the grid via single-phase or three-phase power converters, the cost of failures could amount to four times as much since more devices are at stake [7]. Besides the reliability issue associated with the renewable generators, power converters' low conversion efficiency and failures of transmitting high-quality power are also widely blamed for causing the power loss and power distortion [8]. Therefore, it is crucial to maintain and even improve the reliability of power converter systems from both safety and economic points of view.

Figure 1.4: Reduce costs by improving reliability upfront [9].

One of the most established paradigms in system reliability research recognizes the identification of system failures at an early stage. The rationale behind this idea is that the earlier the unreliability issue is identified, the less cost it is going to incur. The researchers from Aalborg University, Denmark, have conducted extensive research in this field and concluded their findings in Figure 1.4. Apparently, the ideal time to identify the unreliability issue of a power converter system is at its conceptualization stage, the cost of which approximates the time and efforts dedicated by a group of researchers or engineers. However, as more resources and time are invested in developing the system, the “cost bricks” are piling up, which indicates the rising cost of unreliability. For a research group, the worst timing of diagnosing the unreliability issue is at testing and verification stage. Whereas for a corporate or profit-driven organization, the unreliability issue uncovered during the product launch stage may not only cost them a fortune to retract the products but also taint its reputation in the long run.

Considering the exponentially growing cost of unreliability at the later stage of research and development (R&D), it is in any organization’s interests to improve the reliability upfront. According to Figure 1.4, there is no better timing than the idea/sketch stage from the economic perspective. Based on this very philosophy, the thesis aims at improving the reliability of power converters at their conceptualization and design stage.

Figure 1.5: Shifting paradigms on reliability-oriented issues across industries.

Apart from the economic consideration, the shifting paradigms in both industry reliability standards and customer expectations are also among the main drivers of improving the reliability power electronic systems as suggested in Figure 1.5. For example, a couple of decades ago, manufacturers were striving to achieve the return rates that wouldn't poke a deep hole on their budget. This was largely due to both technical incompetence as well as inadequate consciousness on reliability-oriented issues industry-wide. Whereas today, their successors are giving sweat and blood to ensure the lowest possible return rates on products in an effort to maintain their market shares and growth. By the year 2030, the return rates are expected to be statistically negligible, or parts per million, according to Dr. Wang Huai's presentation at ECCE-Asia 2016 [9].

On the other hand, the increasing intensity of market competition and the wide availability of substitutes have given more bargaining power to customers over the course of the past twenty years. In 1990, customers would tolerate a certain amount of failures as long as the replacements are provided as per the terms specified in the warranty. This tolerance has worn much thinner today as customers would choose products with superior quality and expect more of maintenance than replacement. In the future, predictive maintenance will be advertised by the suppliers to appeal to the group of customers who are pursuing peace of mind when choosing one product out of

many.

To summarize, shifting paradigms on reliability standards have essentially forced the industries to invest more resources, capital, and energy in developing systems that could meet the evolving customer demands and competitions. This trend also confirms the underlying values of the research work presented in this thesis.

1.3 Scope

1.3.1 Reliability-Critical Components

The previous research and industry surveys have justified why it is necessary to investigate and solve the reliability-oriented issues in power converter systems at the earliest stage possible. The next step would be determining which part of the system is particularly critical to the system reliability before exploring various approaches to addressing the issue. According to an industry survey on reliability in power converter systems conducted and organized by Yang *et al.*, semiconductor power devices and capacitors top the list of the most fragile components with each being voted by 34% and 20% of survey participants, respectively [6]. The dual is followed by gate drives and connectors, both of them are believed to be fragile by more than 10% of the responders as shown in Figure 1.6.

The pie chart indicates that the semiconductor power devices are considered the most fragile component in power converter systems by the majority of survey participants. Intuitively, this is worth studying more than any other components on this list. In fact, however, capacitors are found to be more susceptible to ambient temperature, humidity, capacitance size, energy density, voltage stress, current ripple, and frequency deviation [10]. These characteristics give capacitors more upside potentials to boost the reliability of a system which frequently suffers from voltage and current ripples of different scales. Capacitors are commonly utilized at the dc link of power converter systems to offset the instantaneous power difference between the dc/ac power source and loads as well as minimize the voltage variation. For example, by simply equipping a power decoupling circuit along with power converters, the system requirement on capacitance can be lowered. Because the ripple components in the current or voltage are now

Figure 1.6: Most fragile components in power electronic converters [6].

diverted to the auxiliary circuits or other passive electrical component dedicated to containing them. The lowered requirement on capacitance prompts the replacement of the conventional electrolytic capacitors (E-Caps) with the more reliable film capacitors (F-Caps), which contributes to improving the overall system reliability.

1.3.2 Concept of Reliability

The definition of reliability varies across industries. In power electronics, reliability of an electronic component is frequently linked to its failure rate, i.e. failures per million hours [8]. Table 1.1 shows the experimental results of a 200 W inverter prototype designed by Krein *et al* [11]. The research attempts to boost the reliability of single-phase inverter systems through the introduction of a ripple port circuit. According to the table, F-Caps have a significantly lower failure rate than E-Caps. In power converter systems, this means the replacement of traditional E-Caps with F-Caps would immediately improve the reliability of the system. In the meantime, this table also demonstrates that despite semiconductor power device is considered the most fragile electrical components in power converter systems, the improvement on system reliability obtained by switching to a superior alternative is marginal compared to replacing E-Caps with F-Caps. However, F-Caps are not flawless, and they do have shortcomings. For the same capacitance requirement, the size of the F-Caps is much larger than that of E-Caps. Moreover, the cost per capacitance is another disadvantage of F-Caps in this competition.

Table 1.1: Key component failure rates in the power converter. [11]

Component	Base reliability (failures per million hours)	Stress factor, 85°C in Fig. 6	Expected failure rate per device
<i>Electrolytic Capacitor</i>	<i>0.0455</i>	<i>3.2</i>	<i>0.1456</i>
<i>MOSFET</i>	<i>0.012</i>	<i>2.3</i>	<i>0.0276</i>
<i>Film Capacitor</i>	<i>0.0005</i>	<i>3.2</i>	<i>0.0016</i>
<i>SCR</i>	<i>0.002</i>	<i>0.27</i>	<i>0.00054</i>

In conclusion, capacitors account for a large proportion of system size, costs, and failures. Meanwhile, they suffer more from issues on energy density, ambient temperature, humidity, current and voltage ripples, cost, and reliability than most other electrical components. Hence, capacitors are considered the key to improving the overall power converter system reliability by this research. There is a trend towards replacing E-Caps at the dc link of power converter systems with F-Caps due to the latter's superior performance in most areas of concerns. However, the capacitance allowed by F-Cap based converters will be notably lower considering the higher cost and larger volume of this type of capacitors. The reduced dc-link capacitance will then impose another design challenge on power converter systems as the harmonic impedance at the dc link will become much lower, bringing in difficulties for instantaneous power balancing as well as ripple power decoupling. Hence, it is worth to investigate how to maintain the system's capability of power balancing and ripple power decoupling in the context of reduced dc-link capacitance.

1.3.3 Challenges to System Reliability

Power converter systems can transmit the electric power generated by RESs to power grids or serve as components of power supplies for high voltage dc (HVDC) power transmission. They are playing significant roles in reducing carbon emissions and combating global climate change. Despite the numerous benefits and merits owned by power converter systems, they also bring in operating challenges, such as the issues with power quality.

Power quality can be broadly considered as voltage and current deviations that cause malfunctions or failures of customer equipment, according to [12]. And issues pertaining to power quality can be further broken down to voltage quality issues and current quality issues. Common voltage quality issues are voltage ripples, unbalances, swells, sags and etc [12]. Most of these voltage quality issues are, in fact, caused by current quality issues along the transmission lines, which are usually manifested in the form of current ripples. Current ripples are frequently described as the current components appearing at the multiples of the fundamental frequency. Grid codes such as IEEE Standard 519-2014 prescribe standards on current ripples as demonstrated in Table 1.2 [13]. And there is a trend to roll out even more stringent standards as these undesirable current components may not only prompt additional power losses and noises but also jeopardize the performance of the power source. For instance, single-phase converters are one of the most commonly used power converters for low power (e.g. <5 kW) grid-connected PV and energy storage applications. A well-known issue with such single-phase systems is that the performance of the dc side may be affected by the second-order ripple power resulted from the grid side [14]. For PV systems, the pulsating power may undermine the efficiency of maximum power point tracking (MPPT), while for energy storage systems (ESSs) it may shorten the lifespan of batteries [15]. Moreover, there is a risk of magnifying current ripples through system resonances, which may end up having an even more detrimental impact on system reliability. Hence, effective methods need to be developed and implemented to attenuate and ideally, eliminate current ripples.

Table 1.2: Current distortion limits for systems rated from 120 V through 69 kV [13].

Maximum current ripple distortion in percent of I_L						
Individual ripple order (odd-frequency ripple) _{a,b}						
I_{sc}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TDD
< 20 _c	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

_aEven-frequency ripples are limited to 25% of the odd-frequency ripple limits above.

_bCurrent distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

I_{sc} = maximum short-circuit current at the point of common coupling (PCC).

I_L = maximum demand load current (fundamental frequency component) at the PCC under normal operating conditions.

Conventionally, a bulky E-Cap is employed to decouple the power oscillation [16]. However, as discussed previously, the utilization of E-Cap gives rise to the reduced power density and shortened operation lifetime under most circumstances (note that F-Caps could have shorter lifetime than E-Caps under humid condition), hence undermining the system reliability. A more reliable alternative would be F-Caps in this context. However, the volume and cost of F-Caps in the same capacitance are higher than that of E-Caps. Therefore, in order to opt for F-Caps, the system requirement on dc-link capacitance needs to be lowered. Hence, one of the thesis's core objectives is to explore and investigate different approaches for power converter systems to achieving the same or even superior performance in suppressing current ripples under the reduced dc-link capacitance.

1.3.4 Reliability Issues with Frequency Regulation

Apart from improving system reliability by adopting more reliable F-Caps, another promising area to study would be the reliability issues associated with frequency regulation when the grid is connected to the renewable generators via power converters.

Unlike synchronous generators, renewable generators cannot provide rotating inertia when connected to the grid via power converters. As a consequence, excessive grid frequency deviations are likely to occur in the event of generator tripling and/or load shedding. Apparently, large scale frequency deviations would have a detrimental effect on the reliability of the power system. Fortunately, there is an effective approach to addressing this challenge simply by controlling power converters. By proportionally associating the grid-connected converters' (GCCs) dc-link voltage with the grid frequency, the power converters can generate a fixed amount of virtual inertia for frequency support [17].

By embedding a frequency deadband into the system controller design, power converters are able to produce an even higher amount of virtual inertia in the event of frequency deviation. The frequency deadband-based system controller design allows the increase of virtual inertia in shorter time duration, leading to the reduced frequency deviations and output energy of power converters. More importantly, the dc-link

voltage is found to change only when the maximum frequency deviation passes the lower or upper limit of the preset frequency deadband. Therefore, unnecessary voltage changes during frequency events can be avoided, which reduces voltage ripples, and hence extending the lifespan of dc-link capacitors. Since capacitors are viewed as the reliability-critical component in power converter systems, the extension of capacitors' lifespan contributes to improving the system reliability.

1.4 Objectives

Following the above discussion, the objectives of the thesis are summarized as follows:

- Explore different approaches to improving the reliability of power converters used in renewable energy systems;
- Review the state of the art active power decoupling methods reported in the literature and evaluate their individual strengths and weaknesses;
- Investigate the methods to substitute E-Caps with the more reliable F-Caps at the dc link without affecting the normal operations of power converters;
- Design control-based approaches to achieving effective current ripple suppression for single-phase power converters considering the most difficult scenarios;
- Further develop the idea of improving system reliability during the frequency event through power converter inertia emulation, when the grid is connected to renewable generators.

1.5 Major Contributions

In view of the aforementioned objectives, several major contributions have been made by the thesis and are summarized as follows:

a. Current ripple reduction for PV powered two-stage single-phase power converters considering weak grid conditions

The virtual impedance-based control design is proposed for PV powered two-stage single-phase GCCs to suppress the ripple components in the dc current. The control design considers multiple low-frequency harmonic components at the PCC voltage introduced by the grid background harmonics. Through meticulous system controller design and parameter tuning, the low-frequency current ripples are considerably reduced. Meanwhile, the system maintains excellent stability and dynamic response. Note that only three 30 μ F dc-link capacitors are required to achieve the impressive results thanks to the proposed controller design. The significantly reduced dc-link capacitance required for active power decoupling also allows the employment of F-Caps, which contributes to improving the reliability of the power converter system.

b. Current ripple mitigation for fuel cell-powered single-phase differential inverters supplying nonlinear loads

The reliability-oriented issues associated with fuel cells when used to power single-phase differential inverters are thoroughly studied. The analysis reveals the detrimental impact of low-frequency current ripples on the reliability, efficiency and even operating lifetime of fuel cells as the power source. To neutralize the impact, a dual-mode operated single-phase differential inverter with a dedicated control scheme design is designed. The designed control scheme maintains equally excellent performance in current ripple mitigation under both linear and nonlinear load conditions. Apart from the effective suppression of multi-order low-frequency current ripples, the current ripples at switching frequency are also considerably reduced thanks to the proposed interleaved modulation. The control scheme design allows the differential inverter to operate normally under two 60 μ F output capacitors. Hence, the more reliable F-Caps can be adopted for dc offset voltage regulation.

c. Frequency deadband-based virtual inertia control for grid-connected power converters

Since renewable generators cannot provide rotating inertia when connected to the grid via power converters, system-wide reliability issues, such as excessive grid frequency deviations could occur in the event of generator tripping or load shedding. An effective approach to addressing this issue is by associating power converters' dc-link voltage with the grid frequency. This allows power converters to generate a fixed amount of virtual inertia for frequency support. To further develop this idea, a frequency deadband-based controller is proposed for power converters to generate virtual inertia and support frequency regulation. Compared to the methods reported in the literatures, the proposed control design can further increase virtual inertia generated by power converters, thereby improving frequency nadir and reducing the energy required for inertia emulation. In addition, the proposed method avoids unnecessary voltage changes under normal system operations. The reduced voltage changes contribute to extending the lifespan of dc-link capacitors.

d. Artificial neural network-based frequency nadir estimation approach for virtual inertia control

By embedding a frequency deadband in the system controller, the power converter is able to generate an even higher amount of virtual inertia, thereby improving frequency nadir and boosting the reliability of the power system during the frequency events. However, it is difficult to either quantify the improvement on frequency nadir through mathematical modeling or identify the decisive parameters that contribute to such improvement. In light of the issue, an artificial neural network (ANN) based method is introduced to estimate the value of frequency nadir while bypassing the sophisticated mathematical modeling and calculations. The ANN essentially acts as a computational surrogate model of the power converter that is capable of establishing a functional relationship between the system parameters and the frequency nadir. In addition, ANN completes the estimation task several orders of magnitude faster than running a simulation model. Furthermore, the results produced by ANN also maintain much higher accuracy than the conventional mathematical modeling.

1.6 Thesis Organization

This chapter introduces the motivation and background of studying the reliability-oriented issues associated with power converters in the context of renewable energy systems. The scope, objectives, and main contributions of the research are also introduced.

Chapter 2 reviews the development and recent progress in active power decoupling, which is the key enabling technique to relieve capacitors' stress in buffering ripple power and scale down the size of capacitance required for the normal operations of power converters.

Chapter 3 introduces two practical cases where control-based active power decoupling is applied to suppress current ripples in single-phase power converters powered by RESs. Both cases attempt to address uncommonly difficult situations revolving around current/voltage ripples. The first case considers multiple low-frequency harmonic components in the PCC voltage introduced by the grid background harmonics. Whereas the second case attends to the situation where nonlinear loads are supplied by the fuel cell-powered converter. The proposed control-based methods successfully suppressed multiple low-frequency current ripples in both cases while maintaining excellent dynamic response and system stability. The validness of the proposed methods is verified by both experimental and simulated results.

As an effort to support frequency regulation during frequency events, Chapter 4 proposes a frequency deadband-based controller to increase virtual inertia generated by power converters. As a result, the frequency nadir is further improved and the energy required for inertia emulation is substantially reduced. In addition, both experimental and simulated results have shown that the dc-link voltage only changes when the maximum frequency deviation exceeds the preset frequency deadband. Hence, unnecessary voltage changes during frequency events can be avoided, which contributes to extending the lifespan of dc-link capacitors.

To quantify the improvement on frequency nadir in Chapter 4 and identify the underlying parameters that contribute to such improvement, Chapter 5 proposes an

ANN-based approach to estimating the value of frequency nadir without engaging sophisticated mathematical calculations. The simulation studies demonstrate that the results produced by ANN are fourteen times more accurate than that of mathematical calculations. Meanwhile, ANN is able to estimate the frequency nadir as a function of system parameters several orders of magnitude faster compared to running the simulation model.

Lastly, Chapter 6 concludes the research work presented in the thesis and outlines a few interesting areas for future work.

Chapter 2

Literature Review

Having discussed the idea of system reliability improvement through replacing the conventional E-Caps with the more reliable F-Caps, this chapter starts by systematically comparing and evaluating the two types of capacitors with respect to reliability, ripple-handling capability, self-healing capability, and failure mechanisms. A major shortcoming of F-Caps is identified through the performance evaluation. To crush this shortcoming, this chapter presents the concept of power decoupling which enables power converters to operate normally under the reduced dc-link capacitance. An evolving array of power decoupling methods are reviewed and compared comprehensively in this chapter, aiming to reveal their respective strengths and weaknesses.

2.1 Why Film Capacitor

As more stringent reliability-oriented constraints are rolled out and applied to aerospace, manufacturing, automotive and energy industries, multiple challenges are encountered by researchers and engineers when it comes to designing the dc links. As discussed in Chapter 1, capacitors are one of the most fragile components considering their average failure rates in power converter system operations. In addition, capacitors are frequently exposed to harsh environmental and operational conditions, i.e. high ambient temperatures, humidity, and radiation as well as current and voltage ripples in some applications. Besides, the cost pressure from market competitions also drives organizations to cut the design margin. Furthermore, the constraints on the volume of capacitors and the trends for high power density systems are also dictating the design and selection of dc-link capacitors [18]. Over the past two decades, tremendous efforts have been committed to addressing these challenges, which can be summarized into the following four categories [19]:

- a. Develop and optimize dc-link design solutions on the basis of the existing capacitor technology to achieve improved reliability, reduced system size, and costs.
- b. Advance the capacitor technology by taking advantage of refined dielectric materials and improved manufacturing processes and integrate reliability-oriented considerations when designing the products.
- c. Implement reliability condition monitoring devices to continuously assess if the system is operating under normal conditions and regularly carry out preventive maintenance.
- d. Conduct predictive maintenance by applying machine learning algorithms to gain more insights from the data collected.

Compared to the latter three categories, the first one is clearly more relevant from the power electronics researchers and engineers' point of view. Hence, it is the main approach that is investigated by this thesis.

2.1.1 Qualitative Analysis

Conventionally, dc-link capacitors are employed to fulfill the following duties in power converters: a) offset the instantaneous power difference between the output and input; b) reduce voltage variation at dc bus; c) make sufficient energy available during the hold-up time. In the outburst of ripple current due to, for instance, the ac-side instantaneous power pulsating at twice the fundamental frequency, the capacitors are also responsible for accommodating the power oscillation. Thus, it is safe to conclude that dc-link capacitors are playing a fairly critical role in power converters. Normally, a bulky E-Cap is used as dc-link capacitor to decouple such power oscillation. However, both physical and chemical properties of E-Caps may lower the power density and shorten the operating lifetime of power converters under most conditions. Hence, there is a trend to replace E-Caps with the more reliable F-Caps.

Figure 2.1 presents the qualitative comparison of the performances among the three types of capacitors. Despite the widely-criticized shortcomings, E-Caps do possess the merits of low cost per Joule and high energy density. However, they are also characterized by low current ripple ratings and high equivalent series resistances (ESRs). In addition, this type of capacitors is generally considered having low reliability mainly due to its potential wearout issues caused by electrolyte evaporation [19].

In contrast, ceramic capacitors (C-Caps) maintain excellent reliability and are capable of operating under a much wider spectrum of frequency. Besides, their maximum operating temperature is approximately 200 °C, which is considerably higher than the

Figure 2.1: Performance comparison between electrolytic and film capacitors [9].

other two types [20]. Nevertheless, the relatively high cost and poor voltage derating performance are the main drawbacks that hinder C-Caps from being the ideal option for dc-link applications.

According to Figure 2.1, F-Caps appear to be the relatively well-rounded type of capacitors among the three. They not only excel in reliability-oriented metrics but also hold explicit advantages in terms of ESRs, capacitor stability, voltage derating, ripple current handling capability as well as the frequency range. Despite they are generally more expensive than E-caps, F-Caps are considered cost-effective enough for most power converter systems, particularly the high voltage applications. One notable flaw of this type of capacitors is its lower upper operating temperature. However, this has been overcome by technological advances in material science. According to [21], polytetrafluoroethylene F-Caps, whose dielectric is made of the synthetic fluoropolymer polytetrafluoroethylene, possess high-temperature resistances up to 200 °C. The main shortcoming of F-Caps, however, is their low energy density. This means for the same amount of energy and/or capacitance required, F-Caps would appear in a much larger volume than the equivalent E-Caps. This may dramatically increase the overall size of the power converter systems.

2.1.2 Ripple Handling Capability

Having figured out the differences in physical, chemical and electrical characteristics among the three types of capacitors, the next step would be determining which type of capacitors is suited for dc-link applications. According to [19], dc-link applications can be classified by the amount of ripple current that they are expected to handle. And there is a positive correlation between the three types of capacitors' current ripple capabilities and their individual capacitance values as displayed in Figure 2.2. According to this figure, all three types of capacitors manage to meet the voltage ripple specification with a low capacitance value C_1 when serving low ripple current applications. However, when it comes to operating under high current ripple applications, E-Caps with a capacitance value of C_1 can no longer meet the requirement and are hence forced to increase their capacitance value to C_2 in order to maintain normal operations. In contrast, both F-Caps and C-Caps can still manage to sustain C_1 due to their higher ripple current handling capability. Thus, it is beneficial to replace E-Caps with either F-Caps or C-

Figure 2.2: Capacitance requirement for different ripple current applications [19].

Caps for power converters from the ripple current tolerance point of view. Nevertheless, after taking both cost-effectiveness and capacitor mechanical sensitivity into consideration, it is concluded that F-Caps are better suited to work with high ripple current application. Meanwhile, it is worth to note that for certain applications, the requirements on minimum energy storage instead of ripple current are the decisive factors when choosing dc-link capacitance. Therefore, the required capacitance might not be reduced merely because of the lowered ripple current rating.

2.1.3 Failure Mechanisms and Self-Healing Capability

There are numerous factors that could lead to the failures of dc-link capacitors. The most prominent extrinsic factors include ambient temperature, humidity, radiation, voltage, and current ripple stress. Meanwhile, intrinsic factors such as device aging, wearout, and design flaws also account for a substantial proportion of failure cases. Table 2.1 demonstrates the differences among the three different types of capacitors in terms of failure modes as well as their corresponding critical stressors, failure mechanisms, and self-healing capability.

The main causes and mechanisms of failures in E-Caps have been thoroughly investigated and reported in [22-24]. For E-Caps in smaller size, electrolyte evaporation is the dominant cause of failure. Because this type of E-Caps is more severely affected by the issues of high ESR than the one in a larger size, although [22] pointed out that

Table 2.1: Failure mechanisms and self-healing capabilities of the capacitors [19].

Type of Capacitor	E-Caps	F-Caps	C-Caps
Main failure modes	Ageing/wearout		
	Open circuit	Open circuit	Short circuit
Main failure mechanisms	Electrolyte vaporization; electrochemical reaction	Moisture corrosion and dielectric loss	Insulation degradation; physical cracking
Critical stressors	Ambient temperature; Voltage stress; Ripple current stress	Ambient temperature; Voltage stress; Humidity	Ambient temperature; Voltage stress; Physical vibration
Self-healing capability	Moderate	Excellent	No

its circumscribed surface for heat dissipation might be another reason. Whereas, the leading factor for large-sized E-Caps' failures is the disrupted or irregular electrochemical reactions occurred at the oxide layer [25]. The amplitude of leakage current is considered having a direct impact on that chain of reactions and hence determining the operating lifetime of E-Caps. As far as critical stressors are concerned, E-Caps are affected by both voltage stress and ripple current stress. Particularly, their poor performance in the presence of ripple current stress is the primary reason that they are not the ideal option to work as dc-link capacitors in power converters. Finally, E-Caps do possess a certain level of self-healing capability, but it is considered inferior to that of F-Caps.

Self-healing capability is commonly recognized as one of the most prominent reliability functions of F-Caps [26]. According to Table 2.1, F-Caps undoubtedly own the best performance in that regard among the three types of capacitors. Unlike E-Caps, F-Caps maintain excellent ripple current handling capabilities and perform significantly better in such environment. However, F-Caps are not impeccable either, its metalized layer is thin and particularly susceptible to moisture corrosion as a result of atmospheric humidity [27]. The moisture corrosion may occur at both outer layers as well as inner layers, which may result in the reduction of capacitance. Another cause of F-Caps' capacitance shrinking is dielectric breakdown occurred at their weak points due to sudden temperature rise or overvoltage. Although this level of capacitance reduction is considered negligible, the increased appearance of such weak points may have a permanent impact on the lifetime of capacitors.

Compared to E-Caps and F-Caps, C-Caps are known for higher durability. The dielectric materials of this type of capacitors maintain stronger resistance against degradation when the capacitor operates under normal use conditions [28]. Despite being made of superior dielectric materials, C-Caps are not immune to failures. In particular, this type of capacitors is vulnerable to physical cracking and insulation degradation. Physical cracking could be caused by different forms of vibration, while insulation degradation occurs as the thickness of dielectric layers become thin. It is worth to note that insulation degradation may lead to leakage current burst, which could escalate into Avalanche Breakdown in a high voltage or high-temperature environment [29]. In addition, unlike the previous two types of capacitors, the main failure mode of C-Caps is short circuit, which poses a substantially higher threat to power converter systems. Finally, the lack of self-healing capability is another shortcoming of this type of capacitors.

By conducting detailed failure analysis and comparing failure modes and mechanisms among three types of capacitors, it is increasingly clear that F-Caps champion the list in terms of reliability, ripple current handling capability, risk concerns, and self-healing capability. This further confirms the earlier hypothesis that F-Caps are better suited for dc-link applications due to their physical, chemical and electrical characteristics.

Having determined the most suitable option for dc-link capacitors, the next question is how to neutralize an inherent flaw of this type of capacitors. As discussed previously, the most prominent shortcoming of F-Cap is its much lower energy density as compared to the other two types of capacitors. Energy density is defined as per unit volume energy stored between plates of a parallel-plate capacitor [30], the equation of which is normally expressed as:

$$u = \frac{C \times V^2}{2A \times d} \quad (2-1)$$

where C stands for capacitance, V is a fixed potential difference or dc-link voltage for dc-link applications. d and A denote the distance between the two plates and the area of capacitor plates, respectively. In other words, $C \times V^2 / 2$ represents capacitor energy, while $A \times d$ equals to the volume of the capacitor. Due to its relatively low energy

density, F-Cap is more suitable for dc-link applications that can operate just as good, if not better, under the lower value of capacitance. According to equation 2-1, for dc-link applications that require a higher value of capacitance, the employment of F-Caps would significantly increase the size of the applications. Apparently, this is an extremely undesirable feature for most power converter applications.

2.2 Approaches to Neutralizing the Shortcoming of F-Caps

The previous subsection conducts qualitative comparisons among three types of capacitors in terms of reliability, ripple current handling capability, failure modes, and mechanisms, self-healing capability as well as other chemical and electrical characteristics. The results suggest that F-Caps are better suited to be utilized as dc-link capacitors in power converter systems due to their relatively well-rounded performance on all those areas. Meanwhile, it is also found that for the same capacitance value, F-Caps' volume tends to be much larger than the other two types of capacitors. This is because the energy density of F-Caps is relatively lower than that of either E-Caps or C-Caps. The volume issue could become more serious when multiple capacitors are required for operations, which may significantly add burden to the overall size of the power electronic converter system.

Assuming the value of the capacitor's energy density remains fixed throughout its operational lifetime, there are only two ways to reduce the volume of such capacitor according to equation 2-1. One way to do so is by scaling down the voltage applied to the capacitor. However, for most power converter systems, especially those operating under high power, this requirement is almost impossible to meet and considered preposterous. For instance, the dc-link voltage, which depends on the scale of ac voltage, is usually set to a higher value with a decent margin. Because a higher dc-link voltage could not only diminish the risks of overmodulation but also help reduce power loss. This explains why a higher dc-link voltage is generally considered the standard practice and also becoming the trend for both academic research and industry operations.

Since voltage scale-down is identified as a dead end towards solving this problem. The only other approach to decreasing the volume of F-Caps, based on equation 2-1, is by

reducing the capacitance required for system operations. Fortunately, there is no existing literature that has reported any detrimental effects of the reduced capacitance requirements might have on power converter systems. Hence, this becomes the main approach adopted by this research to counteracting the volume issues with F-Caps.

Large capacitance is usually required by high power dc-link applications for the sake of high instantaneous power difference as well as power oscillation. Particularly, the latter issue has become more prominent as renewable energy resources are increasingly deployed in modern power systems. For example, a common issue with PV powered single-phase inverter system is that the performance and operating lifetime of the dc source might be affected by the second-order ripple components in dc current due to the double line frequency instantaneous power pulsating at the ac side [31]. Conventionally, a large size of E-Cap would be used as the dc-link capacitor to counteract such an issue. However, the most obvious repercussion of this approach is that the flawed electrochemical characteristics of this type of capacitor may pose reliability-related risks to the power converter system as elaborated in Section 2.1. In light of this concern, the more reliable F-Caps are widely considered as a promising substitute by both academia and industrial researchers. Nevertheless, as discussed previously, a tangible shortcoming of this type of capacitor is its large volume. According to the quantitative analysis on equation 2-1, a feasible approach to condensing the volume of F-Cap is via the reduction of capacitance required by dc-link applications. A straightforward means of realizing that would be isolating the ripple power from fundamental power processed by dc-link capacitors in single-phase power converters. Fortunately, in power electronics research, there is a family of techniques dedicated to achieving this very goal.

2.3 Categorization of Power Decoupling

Power decoupling, as the name suggests, separates the ripple power at double or multiple the fundamental frequency from the instantaneous power by employing advanced control algorithms and/or auxiliary circuits that possess energy storage capability in power converter topology design. For single-phase power converters, the instantaneous power at the ac side typically includes a second-order ripple component. Power decoupling is a key enabling method to intercept the pulsating power from propagating through the power converter's dc side [31]. The simplified diagram of a single-phase power converter with power decoupling capability is displayed in Figure 2.3. Depending on the specific system segment targeted in the design, power decoupling techniques are typically classified into two categories, i.e. hardware power decoupling and software power decoupling.

2.3.1 Hardware Power Decoupling Techniques

Hardware power decoupling simply refers to the group of techniques that are capable of separating ripple power from fundamental power and containing the oscillating power via the introduction of auxiliary circuits, passive electric components, (i.e. capacitor, inductors) or the combination of both. Hardware power decoupling can be further broken down into active power decoupling and passive power decoupling. Unlike active power decoupling, the passive power decoupling is usually implemented by equipping extra passive electrical components, such as inductors and capacitors, to help decouple the power oscillation. In contrast, active power decoupling leverages the organic combination of auxiliary circuits and energy storage components to provide energy buffer solutions with improved power density. Depending on the circuit

Figure 2.3: Power flow of a single-phase power converter.

Figure 2.4: General classification of power decoupling techniques.

configuration, active power decoupling is implemented as either shunt or series compensation circuit, which is installed in parallel or sometimes in series with the dc-link, dc or even ac side of the power converter. Figure 2.4 gives an overview of different power decoupling techniques.

In order to prevent the ripple power from propagating through the single-phase system, the power converter needs to possess storage features to buffer such power during the operation. The most straightforward option, in this case, would be passive power decoupling. And the most widely used passive power decoupling technique is by raising the capacitance of the intermediate capacitor at dc link [16]. Nevertheless, the elevated capacitance would prompt the utilization of E-Cap, leading to undermined system reliability due to E-Cap's lower power density and limited operational lifetime. A qualitative analysis of E-Cap's intrinsic electrochemical characteristics has been discussed in the previous section. As a more reliable substitute, F-Cap has been popularly introduced in a broad spectrum of dc-link applications. However, the low energy density nature of F-Cap makes its volume the major shortcoming for this type of capacitor. In certain cases, the energy storage component volume can be slightly

reduced provided that the load side does not have a very strict requirement on the proportion of ripple current. Nevertheless, for most of the reliability-critical applications such as data center, aerospace, and hospital, there is a very stringent requirement regarding the capacitance of the dc-link capacitor. Because load sensitivity to the ripple current has a high impact on the capacitance, and hence the volume of the energy storage component [31]. Considering these factors, it is recommended to employ exclusively designed energy buffer solution to accommodate the ripple power in order to lower the requirement on the capacitance magnitude, and hence the volume of the dc-link capacitor. This is where active power decoupling comes into play.

Active power decoupling is generally considered more versatile, flexible and optimizable than passive power decoupling. This type of techniques essentially leverages the organic combination of auxiliary circuit and energy storage components to provide an alternative energy buffering solution. This solution is capable of containing oscillating power while lowering the requirement on the capacitance, and

Figure 2.5: Active power decoupling techniques: (a) parallel connection; (b) series connection.

hence the volume of dc-link capacitors. As discussed above, the circuit for active power decoupling is implemented either in parallel or in series with respect to the single-phase power converter as presented in Figure 2.5. Meanwhile, power converters may comprise one or sometimes two stages. For example, the first case study in Chapter 3 will discuss a single-phase PV powered power converter system that is configured in two stages. The converter topology is made of an upstream dc-to-dc conversion and a downstream dc-to-ac conversion stage. The second case study in Chapter 3 will look into one-stage inverter topologies, where a direct dc-ac conversion manages to perform two tasks: step up or down the dc voltage and subsequently convert it into an ac waveform. In the following review of active power decoupling techniques, both one-stage and two-stage converter topologies will be covered.

The simplest active power decoupling method involves installing an LC circuit at the dc bus as demonstrated in Figure 2.6. This technique is also known as pulse-link, which is reported in [32]. The introduction of the LC circuit in series with dc bus is able to cancel current ripple components effectively. Therefore, it is no longer required to install a bulky capacitor between the boost dc-dc converter and the pulse-width modulation (PWM) converter stage. However, this method brings additional energy storage, which has lower power density and higher ESR compared to F-Cap. Furthermore, the inductance can fluctuate under high current stress, leaving a question mark on both the reliability and durability of the approach.

Figure 2.6: Schematic circuit of pulse-link inverter for fuel cell application.

Figure 2.7: Schematic circuit of two-stage power converter with a bidirectional full-bridge converter for power decoupling.

Another classic topology includes a bidirectional full-bridge dc-dc converter operating in parallel with dc bus as demonstrated in Figure 2.7. The auxiliary circuit is implemented for the purpose of supplying ripple power for the ac side, immunizing the dc side from being affected by the power oscillation [33-36]. Also, with such a full-bridge converter being installed, there is no need to insert a sizable E-Cap at the dc link. The rationale behind the operation is based on the fact that lower capacitance is good enough to handle the fluctuating power should those restrains on the capacitor voltage ripple be loosened. Therefore, replacing the power matching dc-link capacitor with a bidirectional power converter enables a considerable decrease in the capacitance value required. Nevertheless, the drawbacks for this approach is obvious, the four additional switches configured on the full-bridge converter would inevitably increase overall power losses. In the meantime, the extra circuit could significantly elevate both the complexity and the size of the system, no to mention the cost incurred due to the hardware components.

Figure 2.8: Shunt compensation circuits (a) dc power decoupling circuits; (b) ac power decoupling circuits.

Some other shunt compensation circuits are reported in [37-40]. From the polarities of the decoupling capacitor voltage, they are typically categorized into dc decoupling circuits and ac decoupling circuits as shown in Figure 2.8 (a) and (b). Some of them do exhibit impressive performance in current ripple suppression with the minimized size of additional electrical components. Nevertheless, similar to the previous topology discussed, the additional hardware would still add burden to the size and elevate the cost of the system. In [41], the decoupling circuit is designed to share the switches of a full-bridge converter. Hence, the main advantage of this topology is that the overall number of switches is the same as a conventional full-bridge converter as shown in Figure 2.9. Nonetheless, the major shortcoming of this design lies in the fact that it might turn into a converter featured in half-bridge when there is no load attached, in which case the requirement on dc voltage would be doubled.

Figure 2.9: Active power decoupling circuit with no extra switch.

More recent progress (2018 - present) in hardware active power decoupling is reported in [42-46]. A single-phase power factor correction rectifier to realize ripple power decoupling without using E-Caps is proposed by Liu *et al* [42]. The rectifier comprises a boost power factor correction circuit and a voltage regulation circuit as shown in Figure 2.10. An advantage of this topology is that it enjoys fewer constraints on decoupling capacitor voltage. Particularly, the minimum value of the decoupling capacitor voltage can be tuned less than the highest value of the grid voltage. This advantage allows a much smaller F-Cap to be installed at the dc bus and assimilate the low-frequency power oscillation. Unfortunately, the additional energy storage devices required to absorb the ripple power would swell the system volume as well as manufacturing costs.

Furukawa *et al.* proposed a power decoupling technique for single-phase voltage source

Figure 2.10: Active power decoupling circuit with high power factor and wide output voltage.

inverter that does not require any additional electrical component [43]. In this topology, a small capacitor in the dc-dc converter featured in flying capacitor is utilized for both second-order power ripple compensation as well as boost operation as presented in Figure 2.11. Hence, the value of dc-link capacitance can be substantially scaled down, which allows the F-Caps to replace the large and less reliable E-Cap. Apart from its excellent power decoupling capability, the maximum system efficiency of this topology is 95.4% at a 1.1 kW load, which is considered superior among the existing topologies that do not require additional hardware for power decoupling. Despite being efficient, the voltage stress for the devices are relatively higher in this topology.

Another recent attempt to decouple the dc-link active power for a low-cost bridgeless power factor correction boost rectifier was introduced by Nguyen *et al* [44]. The solution is to force the voltage ripple to be assimilated by a capacitor in the auxiliary circuit. Hence, a 150 μF F-Cap can be utilized at the dc link and replace what would normally require an E-Cap of 2000 μF for the same scale of voltage ripple as presented in Figure 2.12. The main advantage of this topology besides system reliability enhancement is that less electrical components are involved which translates to 44% volume reduction and 12% cost decrease.

A single-phase bidirectional converter topology is introduced by Mozaffari *et al.*, which is able to manage the mismatch between output and input power by incorporating a

Figure 2.11: Active power decoupling circuit for dc to single-phase ac converter with flying capacitor dc-dc converter.

Figure 2.12: Active power decoupling circuit for dc to single-phase bridgeless power factor correction boost rectifier.

ripple port in the circuit design [45]. No inductor is required to be installed in series with the decoupling capacitor in the said configuration. The operating principles of the power converter allow the maximum utilization of the energy coming from capacitors, which significantly reduces the capacitance needed for power decoupling purposes. The minimized capacitance requirement encourages the utilization of a small thin F-Cap for power decoupling, which directly contributes to the improvement of system lifespan and reliability. Another advantage of this topology in Figure 2.13, is that it is featured in soft-switching operations, which is carried out by installing a tiny capacitor in parallel with the inductor. This feature not only enhances system efficiency but also considerably decreases the switching loss and voltage stress withstood by the semiconductor power devices. Nevertheless, the drawback of this topology is pronounced, both the ripple port and ac-link bridge introduce extra electrical devices, which increases the system volume and elevates manufacturing costs.

Another interesting approach to mitigating voltage ripple is by attaching plug-and-play voltage ripple mitigator as discussed in [46]. According to Li *et al.*, the ripple mitigator can achieve the similar performance in voltage ripple reduction as the existing active power filter design. In the meantime, it can be either connected to or detached from the dc-link of an ac-dc power system without incurring any modification to the hardware of the host system. Therefore, the major advantages of this method over the previous art are its flexibility and non-intrusive property. In addition, the analysis and experiments provided in this literature have also proved the capability of the device in hot-swap operation as well as reducing system thermal stress. However, the main shortcoming of this topology as shown in Figure 2.14, is the introduction of this device

Figure 2.13: Active power decoupling circuit for bidirectional single-phase inverter or rectifier topology with three ports.

itself. Two additional switches will inevitably incur additional power loss and the extra hardware would elevate the size as well as the cost of the entire system.

Clearly, it is a fairly challenging mission to reduce the ripple components in either current or voltage into minimum without incurring auxiliary circuits or electrical components. Most of the existing active power decoupling approaches are based on the idea that by forcing the pulsating power to divert to the auxiliary circuit or a dedicated decoupling capacitor, the dc-link capacitance does not have to be that large anymore.

Figure 2.14: Active power decoupling circuit for a hybrid ac-dc system powered by boost power factor correction rectifier with plugged-in ripple mitigator.

Hence, a small F-Cap can be utilized to replace the bulky and less reliable E-Cap.

Similarly, rather than resorting to a bulky E-Cap to buffer the second-order ripple power, Zhu *et al.* attempted to remove the pulsation power by regulating the voltage waveforms of two small output capacitors [47]. The voltages of the two output capacitors in Figure 2.15 are respectively controlled as follows:

$$v_{c1} = \frac{1}{2}V \sin(\omega t) + M(t) \quad (2-1)$$

$$v_{c2} = -\frac{1}{2}V \sin(\omega t) + M(t) \quad (2-2)$$

where ω and V represent the frequency and amplitude of the output voltage respectively. $M(t)$ is the calculated function to confine the ripple power. The ripple confinement control is realized by having the ac component of load power provided from the two output capacitors. The $M(t)$ is then calculated by equalizing the pulsation power and output capacitor power.

$$P_{\text{load}} = P_{\text{dc}} + P_{\text{ac}} = V \sin(\omega t) I \sin(\omega t) = VI/2 - (VI/2)\cos(2\omega t) \quad (2-3)$$

$$P_{c1} + P_{c2} = P_{\text{ac}} \quad (2-4)$$

The main advantage of this method is that it minimized the power decoupling circuit to only one additional small capacitor. However, as explained previously, the shortcoming of this method is obvious as the calculation assumes constant load and ignores any possible variation of parameters such as capacitance.

Another open-loop control design for the same topology as Figure 2.15 was introduced by Chen *et al* [48]. The main difference is that their design is featured in space vector pulse with modulation (SVPWM) control. Apart from calculating the value of voltage reference, this method also involves the design of ac capacitance which considers the system's current and voltage stress. Similar as [47], the magnitudes of ac capacitor current and voltage are calculated through equalizing the power from the capacitor side to the ripple power of twice the fundamental frequency from the grid side. The results, as stated previously, are subject to the variation of parameters as well as the non-ideal elements on the grid side.

Figure 2.15: Active power decoupling circuit and control system for single-phase full-bridge inverter.

The control diagram, as presented in Figure 2.16, is different from [47], in which three proportional resonant (PR) controllers are employed to control the grid current, ac capacitor current, and voltage, respectively. V_s and I_s are the grid current and voltage, while I_{Cac} and V_{Cac} represent the current and voltage of the ac capacitor. A classical double-loop structure is adopted for the control of ac capacitor, which comprises an

Figure 2.16: Control system for single-phase power conversion and ripple reduction.

outer voltage loop and an inner current loop and. The transfer function of the PR controller adopted in this paper is

$$G_{PR}(s) = K_p + \frac{2k_r \omega s}{s^2 + 2\omega s + \omega^2} \quad (2-5)$$

where K_r and K_p denote resonant and proportional gains, respectively. However, the topology in Figure 2.15 introduces an additional half-bridge for power decoupling. The main issues with these hardware-based active power decoupling methods include increased system complexity, size, cost, and even higher power loss should more switches be included. In light of these issues, software-based active power decoupling methods become more sound and preferred alternatives. These methods force the same type of ripple components to be assimilated by the dc-link capacitors in reduced capacitance through control-based approaches.

2.3.2 Software Power Decoupling Techniques

Software power decoupling refers to the set of methods that manage to achieve the same or even better ripple power suppression effect under the reduced size of capacitors via purely control-based approaches. Apparently, without resorting to any auxiliary circuits or passive electrical components, software power decoupling possesses explicit advantages over those hardware-based approaches at least from system size, cost and topological complexity points of view. Moreover, the circuits implementing software power decoupling generally suffer less power loss since none extra switches are added to the configuration. Finally, from the implementation's perspective, a control-based power decoupling is easier to implement, maintain and even modify should any type of fault occur.

The control-based active power decoupling methods can be broadly categorized into open and closed-loop control. The open-loop control methods are typically applied through calculating either the voltage or current reference for the dc-link capacitors based on derived formulations [49-50]. Despite its simplicity to understand and implement, these methods are particularly sensitive to the variations of parameters in the energy storage components due to aging and wear-out issues. Besides, the calculated-based approaches are only valid under constant and linear load, making it impossible to manage the cases which non-ideal grid or nonlinear loads are involved. Hence, it is challenging to realize either adaptive or accurate active power decoupling via this type of methods, making them the less preferable options for systems that require a high level of accuracy and reliability.

The closed-loop control methods, in contrast, do not necessarily require the sophisticated calculation beforehand and constantly minimize the errors between the values of references and the controlled variables through a feedback mechanism. This group of methods can automatically achieve power decoupling via controlling the ripple components while quickly adapting to any variations of system parameters. Hence, closed-loop control approaches can achieve more accurate and reliable power decoupling as compared to the open-loop ones.

One of the most well-known closed-loop control structure for current ripple reduction is the classical double-loop control diagram as demonstrated in Figure 2.17. The outer voltage loop is tasked at regulating the capacitor voltage, while the inner current loop is dedicated to both controlling capacitor current and reducing current ripple existed in the current [51]. The capacitor voltage open-loop control transfer function is

$$G_{dc_op}(s) = G_v(s)G_i(s)G_C(s) \quad (2-6)$$

where $G_i(s)$, and $G_v(s)$ are current and voltage controllers respectively. $G_C(s)$ represents the transfer function of capacitor impedance. Usually, proportional-integral controllers are employed to regulate dc current and dc voltage. The corresponding closed-loop control transfer function is

$$G_{dc_cl}(s) = \frac{G_{dc_op}(s)}{H_v(s)G_{dc_op}(s) + 1} = \frac{G_v(s)G_i(s)G_C(s)}{H_v(s)G_v(s)G_i(s)G_C(s) + 1} \quad (2-7)$$

where $H_v(s)$ is the feedback gain. However, the main drawback of this control structure is the poor dynamic response caused by the significantly reduced voltage-loop crossover frequency. In addition, there is a possibility of dc voltage overshoot or undershoot in dynamic load scenarios [52].

To improve the dynamic response of the abovementioned double-loop control scheme, a simple approach would be including a notch filter into the outer voltage loop as presented in Figure 2.18 [53-54]. By setting the notch filter's characteristic frequency at the frequency of the particular current ripple component, the voltage controller gain at the targeted frequency can be decreased without lowering crossover frequency in the voltage loop. Thus, the dynamic response of the double-loop control system is notably improved. Nevertheless, the additional notch controller would inevitably introduce a phase shift below its characteristic frequency, which might result in a reduced system phase margin.

Figure 2.17: Basic double-loop control structure of single-phase power converters.

Figure 2.18: Basic double-loop control structure with a notch filter.

Another attempt to achieve excellent current ripple mitigation while not sacrificing control loop dynamic response is discussed in [52]. This tradeoff is realized by tuning the output impedance of the power converter. Shi *et al.* proposed and verified the feasibility of making dc-link capacitors supply all the ripple power [55] in a two-stage single-phase inverter, hence no additional hardware is required for power decoupling. In that paper, dc-link voltage reference is changed by adding the second-order ripple component of the load current via a feedforward loop. The diagram of the feedforward control loop illustrated in [55] is given as Figure 2.19, where the dc bus voltage is controlled to pulsate at twice the line frequency, hence making the dc-link capacitor supply the ripple power and avoiding the oscillating power flowing into the input current. Nevertheless, since the feedforward coefficient is inversely proportional to the capacitance of the dc-link capacitor, any capacitance deviation would impair the capability of current ripple reduction.

Another similar approach that involves the modification of dc voltage reference to accommodate the second order ripple power for standalone PV powered systems is reported in [56]. By allowing the converter control loop to track the modified dc voltage

Figure 2.19: Control diagram of low-frequency current reduction with feedforward loop.

reference, the second-order current ripple the dc-dc converter is significantly reduced. Hence, the main advantage of this method is that it addresses the ripple issue without incurring any extra electrical components or auxiliary circuit. The control diagram of the ripple current reduction method is presented in Figure 2.20.

Note that most of the abovementioned ripple power reduction methods are designed for single-phase two-stage power converters, which require a relatively sizable dc-link capacitor during dc-ac conversion process. Apart from the issue with the size of dc-link capacitors, the effect of the capacitor parameter deviation was usually overlooked by the prior literature. Yao *et al.* investigated the effectiveness of active power decoupling under dc-link capacitance deviation and mismatch in [57-58]. Dc-link capacitance can be expected to drift 10% to 20% away from its rated value over the capacitor's lifespan due to aging and wearout. In addition, the two dc-link capacitors are very unlikely to be aging or worn out at completely the same pace. Hence, capacitance mismatch occurs frequently in practice. By including the consideration of capacitance deviation and mismatch in control scheme design, an even more effective active power decoupling can be achieved. [57] studied the effect of capacitance mismatch on a single-phase differential inverter topology, which requires no additional hardware for power decoupling. The differential inverter comprises two dc-dc converters which share the same dc source and ac output port as shown in Figure 2.21. The differential inverter has two flow paths: the differential path is dedicated to transferring power; the common flow path is committed to removing the second-order pulsating power from the dc source.

Figure 2.20: Control diagram of the second-order ripple current reduction method.

Figure 2.21: Schematic configuration of the single-phase differential inverter.

The capacitance mismatch is found to introduce extra first and third-order ripples at the differential inverter's dc side. In the meantime, additional second and fourth-order ripples are also observed at the ac side. To mitigate and neutralize the effects of capacitance mismatch by eliminating these additional ripples, dc-link capacitor voltage waveforms are reshaped by including the same ripple components into their mathematical expressions. An improved control design with the ac current feedback is proposed in [57] and presented in Figure 2.22. In addition to addressing the practical capacitance mismatch issue, this control scheme is also designed to accommodate non-idea grid conditions, which are featured in additional low-frequency ripple components at 3ω , 5ω , 7ω , and etc. By introducing additional PR controllers with characteristic frequencies set at 3ω , 5ω , 7ω , and etc, those multi-frequency ripple components are effectively compensated. Note that even if the grid is in an ideal condition, RCs are still required to resolve issues with capacitance mismatch. Nonetheless, the main issue with this control approach is that the number of PR controllers required keeps growing as additional low-frequency ripple components appear. And the introduction of additional controllers would weaken system dynamic response and add up to system redundancy.

Figure 2.22: Control diagram of the single-phase differential inverter.

Yao et al. also presented the impact of dc-link capacitance mismatch on power decoupling in [58] along with another control method dedicated to addressing the problem. Specifically, the dc-link capacitor voltage was designed to track a dc offset voltage as well as a ripple component. The dc-link capacitance mismatch was found to have a compromising effect on the power decoupling capability despite not resulting in additional odd-frequency ripple components. The control scheme based on dc-split-capacitor power decoupling is demonstrated in Figure 2.23, which comprises two main control paths. The upper control path is designed for dc voltage regulation, where a simple proportional integral (PI) controller is employed to serve that purpose. The output of the PI controller is multiplied by a grid synchronized sinusoid and forms the reference for grid current. The error of grid current is then fed into a PR controller with its resonant peaks being placed at the fundamental and third-order line frequency. The lower control path commits to achieving the power decoupling with the capacitor voltage references that are formed by feeding the dc voltage ripple to a proportional-resonant controller, whose resonant peaks rest at the second and fourth-order line frequency. Both control paths show excellent dynamic response and compensate the input disturbances promptly.

Most of the power decoupling methods discussed so far are designed to manage the coupling power with double fundamental frequency. And the underlying assumptions of these methods are either ideal power grid or linear loads at the downstream output side. However, with the rapidly growing renewable energy generation worldwide, the

Figure 2.23 Control diagram of dc-split-capacitor power decoupling scheme.

properties of the weak power grid, such as high grid impedance, are gradually shown in the modern power grid. One of the typical characteristics of the weak power grid is that the magnitudes of low-frequency ripple power at the PCC are found to be relatively high. As a result, the instantaneous power coupling between the ac side and the dc bus of a single-phase inverter or rectifier is characterized not only by second-order ripple power but also the ripple components of other frequencies, i.e. 4th, 6th, 8th, and etc. Therefore, it is necessary to incorporate this consideration in power decoupling control design.

Huang et al. designed a power decoupling control to mitigate the multiple low-frequency ripple power components on the dc bus of single-phase grid-connected inverter under nonideal power grid [59]. Through modifying the reference values of dc-link capacitor voltage, they managed to simplify the system control structure as shown in Figure 2.24 and achieve the effective power decoupling for low-order ripple components at periodic frequencies. In [59], a double-line frequency component is added to the dc bus voltage reference instead, which is different from including a line frequency component as proposed in [57]. There are two advantages associated to this modification: grid current is less sensitive to the capacitor parameter deviation, i.e. capacitance mismatch; delay and Park transform modules can be removed from the dc bus voltage control loop. According to Figure 2.24, a closed-loop control structure is adopted in [59]. And the power decoupling is essentially realized through employing a multi-PR controller to force the low-order voltage ripple components at periodic frequencies tend to zero. This power decoupling control works equally well under ideal

Figure 2.24: Control diagram of a multifrequency power decoupling scheme.

grid conditions when the grid voltage at the PCC contains only the second-order ripple component. The multi-PR controller adopted in the outer voltage control loop can be expressed as

$$G_{PRm}(s) = k_{rp} + \sum_{i=2}^n \frac{2k_{ri}\omega_b s}{s^2 + 2\omega_b s + \omega_{hi}^2} \quad (2-8)$$

Where k_{rp} and k_{ri} are the proportional and resonance gains, respectively. The multi-PR controller can generate spiky gains at the specified frequencies and achieve static error-free tracking. Nevertheless, similar to [57], the infinite number of PR controllers is major drawback for this type of control structure. On one hand, it is difficult to anticipate the number of PR controllers required to accommodate the multiple low-frequency ripple components. On the other hand, the stockpile of PR controllers would compromise system dynamic response and increase system complexity.

Another ripple power control method considering the non-idea grid conditions is designed by Ge *et al.* in [60]. The paper introduces a model predictive control to track the direct instantaneous ripple power in a single-phase inverter. It manages to achieve excellent ripple power decoupling despite the highly distorted output voltage and current of the inverter. In addition, the method is capable of compensating the ripple power not only at 2ω but also other frequencies such as 4ω , 6ω , and 8ω , etc. Comparing to the existing art, this method also has several advantages including fast response to load change, minimized capacitance and simple implementation. Nevertheless, the performance of this method is highly subject to the control precision and might be affected by the limited gain of the control loop as well.

To better summarize and compare the different power decoupling methods discussed in this section, a comparison table is provided as in Table 2.2.

Table 2.2: Comparison of different power decoupling techniques

Hardware methods	Power	Capacitor	Decoupling circuit	Efficiency	Merits	Flaws
Fig. 2.6	120W	330 μ F	1L + 1C	82%	no bulky E-Cap	extra L, high current stress
Fig. 2.7	500W	N.A.	4S + 1C + 1L	N.A.	no bulky E-Cap	extra circuit, high power loss
Fig. 2.9	1000W	2*90 μ F	2C	93.5%	min. extra circuit	high dc voltage requirement
Fig. 2.10	480W	90 μ F	2S + 1C	93.3%	high PF, no E-Cap	extra IGBTs required
Fig. 2.11	1500W	180 μ F	1C	95.4%	high efficiency	high voltage stress
Fig. 2.12	1600W	150 μ F	2S + 1L + 1C	97%	high efficiency	extra circuit, power loss
Fig. 2.13	127W	45 μ F	4S + 1C	84.7%	low switching loss	low efficiency, extra circuit
Fig. 2.14	100W	5 μ F	2S + 1L + 1C	93.2%	nonintrusive/hot-swap	extra circuit
Software methods	Power	Capacitor	Decoupling circuit	Efficiency	Merits	Flaws
Fig. 2.18	200W	40 μ F	None	94.4%	good dynamic response	reduced phase margin
Fig. 2.19	2500W	4.08mF	None	N.A.	no extra circuit	bulky E-Cap required
Fig. 2.20	6000W	3.92mF	None	N.A.	no extra circuit	bulky E-Cap required
Fig. 2.21	2200W	2*60 μ F	None	N.A.	Cap mismatch issue solved	slow dynamic response
Fig. 2.23	1000W	2*90 μ F	None	96%	Cap mismatch issue solved	fail on nonideal grid
Fig. 2.24	1500W	330 μ F/120 μ F	None	N.A.	can hand nonideal grid	multiple PR controllers

C:decoupling capacitor; L: decoupling inductor; S: additional swtiches; N.A.: no information found

2.4 Summary and Outlook

Clearly, F-Caps have been widely acknowledged as the better alternative for the dc-link applications as compared to the conventionally used E-Caps. Section 2.1 and 2.2 have systematically compared and evaluated the performances of the two types of capacitors, particularly in terms of reliability, ripple-handling capability, failure mechanisms, and self-healing capability. The analysis suggests that F-Caps are better suited to be utilized as dc-link capacitors in power converter systems owing to their relatively well-rounded performance on all key metrics.

Nevertheless, the F-Cap is not impeccable, it does have its own Achilles' heel which is associated with its volume. Due to its relatively low energy density, the volume of the F-Cap is notably larger than that of E-Caps in the same capacitance. This larger volume of capacitors would inevitably add up to the cost, size, and weight of the power converters, none of which is desirable for industrial applications. Assuming the value of the capacitor's energy density remains unchanged throughout its operational lifetime, there are two ways to potentially reduce the volume of F-Cap according to equation 2-1: scale down the voltage applied to the capacitor or lower the capacitance required.

The first solution is practically infeasible since the high dc-link voltage is required by power converter applications to minimize the risks of overmodulation and reduce power loss, especially those requiring long-distance power transmission. Fortunately, no literature has so far reported any detrimental effect the reduced capacitance requirements might have on dc link applications. Hence, major efforts have been dedicated to investigating the methods to lower the required capacitance at the dc link.

In addition to managing the instantaneous power of fundamental frequency, dc-link capacitors are also responsible for dealing with the second-order ripple power, a common byproduct of dc-ac or ac-dc power conversion. The ripple power is required to be mitigated to an engineering tolerance range [60]. According to the IEEE 1547 standard, the total amount of second to tenth even harmonics has been capped at 1% [61]. Hence, large dc-link capacitors are usually employed to achieve that end. In order to lower the capacitance required by dc link, one of the most straightforward approaches is to separate the ripple power from the fundamental power. This allows

dc-link capacitors to only focus on processing the instantaneous power of fundamental frequency, which can be readily accomplished under significantly reduced capacitance.

Power decoupling methods are capable of separating the ripple power at twice or multiple the fundamental frequency from the instantaneous power of fundamental frequency via advanced control design and auxiliary circuits that possess energy storage capability. Active power decoupling methods are generally preferred over the passive power decoupling techniques primarily due to their lower reliance on additional electrical components and circuits, as well as the higher flexibility and potentials to improve through control-based approaches. Hence, more attentions have been drawn towards studying active power decoupling methods over the past two decades, the most prominent of which are reviewed in this chapter. In this thesis, active power decoupling methods are further categorized into the hardware power decoupling and the software power decoupling depending on whether hardware such as auxiliary circuits and passive electrical components are involved in the design.

Despite hardware power decoupling methods have shown excellent potentials in mitigating ripple power under both idea and non-idea grid/load conditions, boosting power conversion efficiency and even accommodating passive electrical component parameter deviations. Nevertheless, the main drawback associated with this category of methods is the additional hardware introduced to realize the power decoupling. The extra hardware would inevitably increase the cost, size, weight and even the complexity of the system. Moreover, should additional switches be employed, which is commonly seen in hardware power decoupling, the issues with power loss and leakage current have to be considered as well.

In contrast, the software power decoupling is able to suppress the ripple power mainly through controller design and control scheme modification. It possesses insurmountable advantages over the hardware power decoupling as it achieves the same goals without incurring additional circuits or electrical components. However, this type of methods is not flawless either. The main shortcoming will be discussed in the next chapter along with two detailed cases of software power decoupling.

Chapter 3

Capacitor Ripple Reduction for Single-Phase Power Converters

Having illustrated the connections between the reduced dc-link capacitance and the improved system reliability in the first and second chapters, this chapter further demonstrates the approaches to achieving the lowered system requirement on the size of dc-link capacitors. Hence, the more reliable F-Caps can be utilized to replace conventional E-Caps. As discussed previously, one of the main reasons that a bulky capacitor is required at the dc link is due to the ripple power generated during the dc-ac power conversion. In addition to managing the instantaneous power of fundamental frequency, the dc-link capacitor also needs to buffer the second-order ripple power. Therefore, a straightforward approach to reducing the size of dc-link capacitors would be either diverting the ripple power elsewhere or eliminating it through control-based methods. To validate this idea, two thoroughly studied cases are presented in this chapter, both of which manage to reduce the size of dc-link capacitors through active power decoupling approaches.

3.1 Case-I: Grid-Connected Single-Phase Two-Stage Power Converters

3.1.1 Background

Power converters are increasingly deployed in the modern power systems to transmit the electric power generated by renewable energy resources in the context of aggressive penetration of distributed energy generation. Single-phase power converters are commonly adopted for low power grid-connected applications such as PV, fuel cell, wind turbine, energy storage and etc. However, unlike three-phase systems, single-phase power converters can be severely affected by the second-order ripple power generated during the ac-dc/dc-ac power conversion processes. For PV systems, the ripple components in the dc current can compromise the efficiency of maximum power point tracking (MPPT) [47]. Whereas for energy storage systems such as batteries and capacitors, the presence of ripple current is one of the main root causes of the devices' shortened lifespan [62].

To further understand the origin of the current ripple and explore the methods to eliminate it, a single-phase two-stage converter topology shown in Figure 3.1 is adopted by Case-I together with a properly designed control scheme. Note that the circuit configuration below comprises an upstream bidirectional dc-dc converter and a downstream power converter which can be either used as a rectifier or an inverter depending on the direction of power flow. In order to suppress the second-order current ripple appeared at the dc side while maintaining a well-regulated ac current, several

Figure 3.1 Schematic configuration of the two-stage single-phase GCC.

active power decoupling methods have been proposed and discussed in [63-67]. Meanwhile, as illustrated in the previous chapter, due to the growing penetration of distributed generation and widespread utilization of nonlinear electronic loads, the power grid has shown the properties of a weak power grid, where the magnitudes of background harmonics (3ω , 5ω , 7ω , and etc.) at the PCC are non-negligible [68]. Under such circumstance, the control design needs to not only address the issues with the common second-order ripple component but also accommodate the ripple components at higher frequencies. Hence, the dc-link capacitor would solely focus on processing the instantaneous power of fundamental frequency, which can be achieved with much smaller capacitance. The reduced dc-link capacitance allows the replacement of the E-Cap with the more reliable F-Cap, which contributes directly to improving the overall reliability of the system.

To achieve the abovementioned purpose, Case-I introduces a virtual impedance-based control scheme for the grid-connected two-stage power converter system. Particularly, the proposed control design employs repetitive controllers to mitigate the multi-frequency current ripple components in both the dc and grid sides of the power converter system. Compared to bundling multiple PR controllers as in [57-59], the repetitive controller has the advantage of fast dynamic response, simple controller structure, added-in delay module as well as a term to attenuate the gains. More details regarding the design of repetitive controller will be elaborated in the next section. Note that the ripple power is successfully decoupled by the generalized virtual impedance even under the severe penetration of weak grid background harmonics and significantly reduced dc-link capacitance.

3.1.2 System Controller Design for Bidirectional DC-DC Converter

Assuming the bidirectional dc-dc converter operates with a power factor $\cos(\theta)$, the grid voltage and current can be respectively expressed as

$$v_g(t) = \sqrt{2}V_g \sin(\omega t) \quad (3-1)$$

$$i_g(t) = \sqrt{2}I_g \sin(\omega t - \theta) \quad (3-2)$$

where V_g and I_g are the amplitudes of the grid voltage and current, respectively. ω stands for the grid fundamental angular frequency. Assuming the no major power loss during the power conversion process, the grid side ac instantaneous power $P_g(t)$ is expected to be balanced with the dc instantaneous power $P_{dc}(t)$ generated by the dc source that supplies the bidirectional dc-dc converter.

$$P_g(t) = P_{dc}(t) \quad (3-3)$$

As the dc voltage is considered constant in a two-stage power converter system, the dc instantaneous current at the bidirectional dc-dc converter is then derived as,

$$\sqrt{2}V_g \sin(\omega t) \sqrt{2}I_g \sin(\omega t - \theta) = V_{dc} I_{dc} \quad (3-4)$$

$$i_{dc}(t) = \frac{2V_g}{V_{dc}} I_g [\cos(\theta) - \cos(2\omega t - \theta)] \quad (3-5)$$

Apparently, the last term of equation 3-5 shows a second-order ripple component that has the same magnitude as the dc current of the fundamental frequency. The expressions of the 4ω , 6ω , and 8ω ripple components that are resulted from the weak power grid background harmonics (i.e. 3ω , 5ω , and 7ω) can be derived in a similar manner. The existence of these multi-frequency ripple components in the dc current prompt the utilization of a large dc-link capacitor, which is responsible for smoothing the ripples intertwined with the dc-link voltage. In the meantime, the presence of dc-link capacitor changes the previous power equilibrium as shown in equation 3-3. The ac instantaneous power is now balanced by the sum of the dc instantaneous power and the ripple power managed by the dc-link capacitor.

$$P_g(t) = P_{dc}(t) + P_{ripple}(t) \quad (3-6)$$

The multi-frequency ripple components in the dc current have also posed a challenge to the single-phase system, where large capacitance is generally preferred for more effective current ripple compensation. To increase the system reliability, F-Caps are typically more desirable as compared to E-Caps by the virtue of their better ripple-handling capability and longer operational lifespan [19]. However, the main issue with F-Caps is that their low energy density characteristic hinders their way to meet the system requirement on large capacitance. For the same capacitance requirement, F-Caps appear much larger in volume comparing the E-Caps, which may considerably increase the weight and size of the system. Therefore, in order to deploy F-Caps at the

Figure 3.2 Control diagram of the bidirectional dc-dc converter with virtual impedance.

dc link, the required size of dc-link capacitance has to be reduced. This is where the control-based active power decoupling scheme comes in.

The control diagram for dc current regulation in the bidirectional dc-dc converter is presented in Figure 3.2. The main objective of the control design is to compensate the even-order ripple components at periodic frequencies penetrated to the dc current from the grid side. K_p and K_{PWM} respectively represent the gains of a proportional controller and PWM. z^{-1} is the system phase delay, whereas H_i denotes the sensor gain of the dc current. In addition, $G_f(z)$ represents the discrete-time model of the inductor filter, which is calculated via the Zero-Order Hold (ZOH) method, the transfer function of which is

$$G_f(z) = \frac{1}{r_d} \frac{1 - e^{-r_d T_s / L_f}}{z - e^{-r_d T_s / L_f}} \quad (3-7)$$

According to [68], the equivalent continuous-time model of $G_f(z)$ in s domain is

$$G_f(s) = \frac{1}{sL_f + r_d} \quad (3-8)$$

Note that all the controllers are designed in the discrete z -domain since that is closer to what the real systems are like. L_f is the inductance of the dc side inductor, whose equivalent series resistance (ESR) is r_d . T_s denotes the sampling time, the value of which is the inverse of the sampling frequency.

To prevent the multi-frequency even-order current ripple from penetrating into the dc side of the converter, a virtual impedance $Z_{vi}(z)$ is installed in series with the inductive impedance $G_f(z)$ to increase the amplitude of the output impedance only at the corresponding frequencies of the current ripple components. This is because a relatively low amplitude for the output impedance at the other frequencies is more desirable from

a good dynamic response perspective. Based on this theory, a virtual impedance with the following expression

$$Z_{vi}(z) = H_i K_p K_{PWM} z^{-1} G_r(z) \quad (3-9)$$

is implemented in series with the inductor impedance $G_f(z)$. Note that $Z_{vi}(z)$ is characterized by high impedance at 2ω and its multiples and low impedance at the other frequencies. The amplitude of the virtual impedance is $H_i K_p K_{PWM}$, whereas the term $z^{-1} G_r(z)$ represents the transfer function of a phase-lead repetitive controller that is employed to mitigate even-frequency current ripple components. Similar to the PR controller, the repetitive controller introduces spiky gains at the even-order ripple frequencies, which can theoretically suppress all the even-order current ripple components below the Nyquist frequency [69]. The configuration of a repetitive controller for even-frequency current ripple components compensation is demonstrated in Figure 3.3, where the term $e_r(z)$ represents the tracking error of the dc current,

$$e_r(z) = i_{dc}^* - i_{dc} \quad (3-10)$$

K_r is the proportional gain of the repetitive controller, which is selected to achieve desirable damping effects and fast transient response [70]. $Q(z)$ is a zero-phase-shift low pass filter (LPF) featured in a unity gain at low frequencies, the transfer function of which is

$$Q(z) = \frac{z + 2 + z^{-1}}{4} \quad (3-11)$$

The LPF gradually attenuates the magnitude response as frequency increases, which contributes to widening the stability margin of the system. The term $z^{-N/2}$ stands for $N/2$ times of delay, in which N equals the sampling frequency divided by the fundamental frequency. Normally, N times of delay are applied in the design of repetitive controllers [70]. However, $N/2$ times of delay is adequate in this controller design since only even-frequency ripple components are concerned. In practice, a phase-lead term z^{-m} is usually embedded in the forward path to compensate the phase delay resulted from the feedback control loop, PWM process, and digital computation [70]. In this controller design, $m = 5$ is identified to have the most satisfying phase compensation effect. Hence, the

Figure 3.3: Repetitive controller for even-frequency current ripple compensation.

Figure 3.4 Magnitude frequency plot of the bidirectional dc-dc converter output impedance. (a) Output impedance without virtual impedance. (b) Output impedance with virtual impedance.

transfer function of the repetitive controller for even-frequency ripple compensation is expressed as

$$G_r(z) = K_r \frac{Q(z) z^{\frac{-N}{2} + m}}{1 - Q(z) z^{\frac{-N}{2}}} \quad (3-12)$$

Figures 3.4(a) and 3.4(b) present the magnitude responses of the bidirectional dc-dc converter's output impedance before and after the virtual impedance is embedded in the control scheme. Apparently, the effect of adding a virtual impedance composed of the repetitive controller is the spiky gains appeared at all the even multiples of the fundamental frequency. Hence, even-frequency ripple components in the dc current can be effectively compensated. In addition, since the high gains gradually attenuate as frequency increases, a relatively fast dynamic response is maintained for the system.

The control block diagram in Figure 3.5 (a) is implemented in PLECS simulation and it is equivalent to what is presented in Figure 3.2. Basically, by moving the virtual impedance node forward to the input of K_p and making the corresponding changes to the transfer function, a transformed control diagram can be obtained as in Figure 3.5(b).

Figure 3.5 Derivation of the even-frequency repetitive controller with virtual impedance: (a) Control diagram implemented in simulations; (b) Equivalent control diagram one; (c) Equivalent control diagram two; (d) Equivalent control diagram three.

Next, the two feedback nodes including H_i and $H_i G_r(z)$ are combined into one, forming an equivalent control diagram as presented in Figure 3.5(c). Finally, move $1 + G_r(z)$

from the feedback loop to the input of K_p at the forward loop, another equivalent control diagram shown in Figure 3.5(d) can be derived. Since the current reference i_{dc}^* is a dc component, which would not be affected by the repetitive controller. Hence, Figure 5.3(d) is considered equivalent to Figure 5.3(a). This 4-step transformation explains why the control diagram implemented in the simulation is equivalent to the one which a virtual impedance is embedded in the feedback loop.

3.1.3 System Controller Design for Full-Bridge Converter

As discussed previously, the weak grid can be formed due to the presence of nonlinear loads and saturation of transformers, which distort the grid voltage waveforms by introducing low-frequency sinusoidal components. The low-frequency ripple components injected into the grid voltage are normally of odd frequency, i.e., 3ω , 5ω , 7ω , and etc. These odd-frequency voltage ripple components can later be transmitted into the grid current, polluting the current waveform with the ripple components at the same frequencies. The control diagram of the full-bridge converter is demonstrated in Figure 3.6. Most of the control modules are lined up similarly as the one in the bidirectional dc-dc converter. Nevertheless, there are two major differences: a phase-locked-loop (PLL) module is introduced to capture the frequency and phase of the grid voltage, which later are passed on to form the reference value for the grid current regulation; the virtual impedance is in parallel with the capacitive impedance. $G_v(z)$ is a PI controller and $d(z)$ denotes the duty cycle of the converter. $G_f(z)$ and $G_c(z)$ are the transfer functions of an inductive impedance and capacitive impedance respectively. Similar to $G_f(z)$, the transfer function of $G_c(z)$ is

Figure 3.6 Control diagram of the full-bridge converter with virtual impedance.

$$G_c(z) = \frac{1}{C_f} \frac{T_s}{z-1} \quad (3-13)$$

Where C_f is the capacitance of the dc-link capacitor. Note that the equivalent continuous-time model of equation 3-13 is $1/sC_f$. All other modules including K_p , K_{PWM} , z^{-1} , and H_v share the same transfer functions as the ones introduced in the bidirectional dc-dc converter.

The purpose of installing a virtual impedance $Z_p(z)$ in parallel with the dc-link capacitor is to suppress the second-order voltage ripples that are conventionally managed by the dc-link capacitor. The transfer function of the virtual impedance $Z_p(z)$ can be expressed as

$$Z_p(z) = -r \frac{Z_f(z) + Z_s(z)}{H_v G_v(z) K_p z^{-1} K_{PWM} d(z) [1 - G_N(z)]} \quad (3-14)$$

$G_N(z)$ is a notch filter, which is used to further reduce the influence of the second-order voltage ripple, whose function is derived from [71] as

$$G_N(z) = \frac{z^2 + z\omega_n^2 T_s^2 - 2z + 1}{z^2 + (\omega_n^2 T_s^2 + \omega_s T_s - 2)z - \omega_s T_s + 1} \quad (3-15)$$

where ω_n and ω_s represent the filtering frequency and bandwidth frequency, respectively. $Z_s(z)$ is another virtual impedance installed in series with the output inductor.

Similar to Figures 3.5 a-d, Figures 3.7 a-d depict the process of transforming the parallel virtual impedance into the notch filter, which is installed on the left side of the voltage controller in the real control implementation in PLECS.

(a)

Figure 3.7 Derivation of notch filter through virtual impedance: (a) Control diagram with virtual impedance; (b) Equivalent control diagram one; (c) Equivalent control diagram two; (d) Control diagram implemented in the simulation.

Figure 3.8 Repetitive controller for odd-frequency current ripple compensation.

Note that there is another virtual impedance $Z_s(z)$ installed in series with the output inductor, it is employed to suppress the odd-frequency ripple components existed in the grid current. Similar to $Z_{vi}(z)$ discussed in Figure 3.2, $Z_s(z)$ is also a repetitive controller in nature. In the meantime, unlike $Z_{vi}(z)$, $Z_s(z)$ provides odd-frequency periodic signals to track and compensate multiple odd-frequency ripple components in the grid current. The minor difference is also reflected in the configuration of the control diagram as shown in Figure 3.8. Clearly, the structure of the odd-frequency repetitive controller is almost the same as the one presented in Figure 3.3 except the plus signs at the summing node are replaced by the minus signs.

The magnitude responses of the full-bridge converter output impedance without and with the virtual impedance $Z_{vi}(z)$ are shown in Figures 3.9 (a) and 3.9 (b), respectively. Note that this controller introduces the spiky gains at all odd-order frequencies to track and compensate the ripple components at the corresponding frequencies. The key parameters of this controller include K_r , m and N , which are the same set of parameters used in the even-frequency repetitive controllers. Due to the existence of the LPF $Q(z)$, the system magnitude gradually attenuates as frequency increases. This is key to

(a)

(b)

Figure 3.9 Magnitude frequency plot of the full-bridge converter output impedance: (a) Output impedance without virtual impedance; (b) Output impedance with virtual impedance.

Figure 3.10 Control diagram for the full-ridge converter implemented in both simulated and experimental verifications.

preserving system stability according to [72] and becomes an important feature in designing LPF. Similar to $Z_{vi}(z)$, the transfer function of $Z_s(z)$ is derived as

$$Z_s(z) = H_v K_p z^{-1} K_{\text{PWM}} G_{od}(z) G_N(z) G_v(z) \quad (3-16)$$

where $H_v K_p K_{\text{PWM}}$ represents the amplitude, while $z^{-1} G_{od}(z) G_N(z) G_v(z)$ defines the frequency characteristics of the impedance. Through a series of similar transformations, the control diagram shown in Figure 3.10 is implemented in both simulations and experiments for grid current regulation. To further elaborate on the proposed controller design, a flowchart is included in Appendix. The results of simulations and experiments are discussed in the next section.

Table 3.1: System and control parameter values.

Description	Value
Nominal input power P	250 W
Switching frequency f_s	20 kHz
Dc-link capacitor C_f	90 μF
Dc-link voltage v_{dc}	200 V
Grid voltage v_g	115 V
Fundamental frequency f_n	50 Hz
Output inductance	5 mH
Input inductance	5 mH

3.1.4 Simulation Results

The effectiveness of the virtual impedance-based control schemes in suppressing multi-frequency ripple components in both dc and grid current is tested by simulations. The simulations are carried out under the PLECS environment with the circuit parameter values listed in Table 3-1.

The simulation results are demonstrated in Figures 3.11 and 3.12. To simulate the

Figure 3.11 Simulated steady-state results without the proposed current control.

background harmonics under the weak grid conditions, 5% of 3ω , 5ω , and 7ω voltage ripple components were intentionally injected to the grid voltage. Figure 3.11 presents the steady-state results of the grid current and dc current when the designed control is not activated. Clearly, the grid current is intertwined with odd-order ripple components at periodic frequencies, which are obviously resulted from the injection of background harmonics. In the meantime, the waveform of dc current is also severely polluted by the multiple even-frequency current ripples penetrated to the dc side.

As shown in Figure 3.12, by activating the designed control, the grid current immediately turns into a clean sinusoidal despite the grid voltage is still distorted due to the background harmonics injection. At the same time, the even-frequency ripple components are also significantly reduced on the dc side, which is manifested by the much smoother waveform of dc current. Note that due to the existence of switching frequency ripple components, the waveform of dc current still appears to be slightly wavy.

Figure 3.12 Simulated steady-state results with the proposed current control.

3.1.5 Experimental Results

To further validate the effectiveness of the designed control in current ripple mitigation, a 250 W testbed was built in the laboratory for experimental verification. The parameter values used in the experiments are the same as the ones listed in Table 3-1.

The grid voltage is supplied by Chroma 61512 programmable ac power source, which was programmed to contain 5% of 3ω , 5ω , and 7ω voltage ripple components, respectively. The steady-state experimental results are demonstrated in Figures 3.13 and 3.14. Similar to what is observed in the simulated results, both grid and dc current are noticeably distorted due to the existence of multi-frequency ripple components when the designed control is not enabled as shown in Figure 3.13. Likewise, the waveforms of both current become considerably smoother and cleaner when the designed control is enabled as shown in Figure 3.14. Hence, the steady-state

Figure 3.13 Experimental steady-state results without the proposed current control.

experimental results match well with the simulated ones, which further demonstrated

Figure 3.14 Experimental steady-state results with the proposed current control.

Figure 3.15 Experimental transient-state results with the proposed current control.

the validity of the designed control. Moreover, the transient response of the system under a 33% power step down (from 250 W to 167 W) is also studied. The waveforms in Figure 3.15 suggest excellent dynamic response with minor oscillatory transient immediately followed by the step change.

In addition to the experimental results plotted in the oscilloscope, the waveform data are also captured and subsequently imported to MATLAB for Fast Fourier Transform (FFT) analysis. The FFT analysis reveals the proportions of current ripple components at different frequencies before and after the designed control is enabled. The FFT results of the grid current under both traditional and the designed control are demonstrated in Figure 3.16. Clearly, more than the acceptable amount of ripple components at 3rd, 5th and 7th of the fundamental frequency are observed in the FFT plot. The total harmonic distortion (THD) amounts to over 10% due to the existence of the odd-frequency ripple components. In contrast, these ripple components are significantly reduced as shown by the striped bar once the designed control is activated. The THD is lowered to only 3.63%, 70% of which comes from high switching frequency ripple. The suppression of such high-frequency ripple components, nevertheless, is not the objective of this case. Hence, given that the total share of low-frequency ripple components is successfully diminished to less than 1% of the grid current magnitude, the designed current control is thus considered effective.

The FFT analysis on the dc current ripple components is presented in Figure 3.17, which reveals a similar conclusion. By enabling the designed current control, the even-

Figure 3.16 FFT analysis on grid current regulation.

Figure 3.17 FFT analysis on dc current regulation.

frequency current ripple components (particularly the second-order) are substantially decreased.

3.1.6 Summary

In this case, a virtual impedance-based control design is introduced for two-stage single-phase GCCs to compensate multi-frequency ripple components in both dc and grid current. The case adopts the concept of virtual impedance in designing the control scheme and leverages the capability of the repetitive controller in suppressing low-order ripple components at periodic frequencies. Through meticulous design and fine tunes, both types of ripple components are successfully suppressed. In the meantime, the system maintains excellent stability and fast dynamic response. In addition, it is worth to note that only three 30 μF dc-link capacitors were required to achieve these results thanks to the designed control. The considerably reduced requirement on dc-link capacitance prompts the utilization of F-Caps, which further enhances the reliability of the entire system.

Notably, neither additional electrical components nor auxiliary circuits were introduced to achieve current ripple compensation in the two-stage system. However, topology-wise, the single-phase two-stage power converters are still considered voluminous and complicated for certain applications. Besides, the aforementioned high switching frequency harmonics can not be addressed by the control schemes proposed in Case-I.

In the light of these concerns, a single-phase differential inverter that can realize voltage scale up/down and dc-ac conversion all in one stage is discussed in Case-II. In addition to suppressing the low-order current ripple components at periodic frequencies, an interleaved modulation is also introduced to address the issue with high switching frequency harmonics.

3.2 Case-II: Fuel Cell-Powered Single-Phase Differential Inverters

3.2.1 Background

Fuel cell-powered single-phase uninterruptible power supplies are commonly utilized to provide high quality and reliable power for system sensitive loads in the event of power failures. However, a well-known issue with such single-phase systems is that the performance of the dc side may be affected by the second-order current ripple resulting from the double-line frequency component of ac side instantaneous power. Note that the low-frequency current ripple has been proven to have measurable effects on fuel cell's inner chemical reactions and hence, detrimental to fuel cell's reliability and lifespan. In studying interactions between fuel cells and power converters, [73] examines the fuel cell voltage responses to a series of current sinusoidal perturbations and identified a sizable hysteresis at around 100 Hz exclusively. Another paper analyzed the effects of current ripples on fuel cell's performance [74] and concluded that both the presence of hysteric activity and the proximity of ripple frequency to the fuel cell's cutoff frequency can be factored into additional losses of the output power. Moreover, fuel cell's durability and lifespan can also be compromised as a result of the low-frequency sinusoidal disturbances [75-77]. Furthermore, the low-frequency current ripples are found to be the major cause of degradation occurred in the fuel cell's cathode catalyst [78], which can also cripple both system performance and reliability. Similar effects are noticeable in battery-powered systems as well [79]. Despite already serious concerns induced by second-order current ripple, this issue tends to aggravate

Figure 3.18 Schematic circuit of the single-phase boost differential inverter.

when the system supplies nonlinear loads, where the input dc current could be polluted by multiple low-frequency ripple components. Apart from the disastrous effects on fuel cells, the existence of these current ripples leads to the reduced conversion efficiency, nuisance tripping [80] and distorted output voltage in the system.

To mitigate the low-frequency current ripples in the dc side of the single-phase system, a variety of methods have been proposed. Among the ones that have been reviewed so far, differential inverter seems to be the best candidate for this particular task. The differential inverter is typically composed of two identical bi-directional dc-dc converters and it can perform both dc-dc and dc-ac power conversions using the same circuit configuration. A single-phase boost differential inverter topology as shown in Figure 3.18 is discussed in [81]. Instead of using a bulky dc-link capacitor to manage the second-order ripple power, this topology removes the ripple components in the dc current by controlling the voltage waveforms of the two output capacitors. However, the voltage reference of the two output capacitors is derived through mathematic calculations in [81], which is only capable of dealing with linear and constant load conditions. Abeywardana *et al.* introduce a rule-based control to mitigate the second-order current ripple in all four power operating quadrants using the same topology [82]. Nevertheless, this method is also impotent when it comes to handling nonlinear loads since the control schemes are designed to accommodate the second-order current ripple only. An improved voltage waveform control that allows the single-phase boost differential inverter to operate under load variations is proposed in [83]. Despite the output voltage reference is calculated through a more robust closed-loop manner, the ac voltage output from this method is notably distorted when the system supplies nonlinear loads. Yao *et al.* further analyze the operating principles and active power decoupling strategies for single-phase buck, boost and buck-boost differential inverters under nonlinear loads [84]. By adding multiple resonant controllers in parallel to the control loop, the current ripple components at second, fourth, sixth and eighth of the fundamental frequency are effectively reduced. However, both the theoretical analysis and experimental results in [81] have demonstrated that the successful suppression of ripple component at one order might give rise to the ripple component in the next immediate periodic order, i.e., second-order and fourth-order in [81]. Hence, it is difficult to predict the number of resonant controllers that are required to combat the newly formed ripple components in the dc current.

In the light of these issues, Case-II introduces dual-mode operations to the single-phase boost differential inverter, the topology of which is shown in Figure 3.18. The differential mode (DM) operation achieves active power conversion and ac voltage regulation. In the meantime, the common mode (CM) operation focuses on suppressing ripple components in the dc current. Particularly, the current ripple reduction control can work effectively under either linear or nonlinear load conditions. In addition, the control schemes regulate the two operation modes in a closed-loop manner, which guarantees the robustness and preciseness of the output capacitor voltage reference calculation. Furthermore, it is worth to note that this control scheme does not require any auxiliary hardware components for active power decoupling, which contributes to minimizing the cost and size of the inverter system. Apart from suppressing low-frequency current ripple components, the control scheme also manages to reduce the current ripples at switching frequency by adopting interleaved modulation.

3.2.2 Circuit Analysis

The single-phase boost differential inverter comprises two identical boost dc-dc converters that share a common dc source. The output of the boost differential inverter is formed by connecting the upper switches of two dc-dc converters. v_o represents the output voltage, while V_{in} and i_{in} respectively denote the input voltage and current of the boost differential inverter. Conventionally, the two output capacitor voltages v_{C1} and v_{C2} are controlled to be

$$v_{C1} = V_{dc} + \frac{1}{2} V_o \sin(\omega t) \quad (3-17)$$

$$v_{C2} = V_{dc} - \frac{1}{2} V_o \sin(\omega t) \quad (3-18)$$

where V_{dc} is the dc offset voltage of the output capacitor and V_o is the amplitude of the output ac voltage, whose fundamental angular frequency is ω . Assuming the system supplies a simple resistive load R , the input current i_{in} can be derived as

$$i_{in} = i_{L1} + i_{L2} = \frac{1}{1-d_1} i_{s2} + \frac{1}{1-d_1} i_{s4} = \frac{v_{C1}}{V_{in}} (i_{C1} + i_o) + \frac{v_{C2}}{V_{in}} (i_{C2} - i_o) \quad (3-19)$$

where i_{L1} and i_{L2} represent the currents of two inductors with the same inductance L . The two output capacitors C_1 and C_2 also share the same capacitance C , the voltages of

which v_{C1} and v_{C2} , respectively. By replacing v_{C1} , v_{C2} in equations 3-17, 3-18 into 3-19 and making the proper transformation, the input current i_{in} can be reformulated as

$$i_{in} = \frac{V_0 i_o}{2V_{in}} - \frac{V_0 i_o}{2V_{in}} \cos(2\omega t) + \frac{\omega C V_o^2}{4V_{in}} \sin(2\omega t) \quad (3-20)$$

Clearly, the last two terms suggest the existence of second-order current ripple component in the input current. By adding second-order components into the output capacitor voltage references through dc offset voltage regulation, the double line frequency current ripple can be compensated theoretically as in [81]. Nevertheless, the mathematic solution of the unknown amplitudes involves complicated square root and inverse trigonometric calculations as illustrated in [84]. Moreover, the solution might become even more sophisticated should nonlinear loads be supplied by the system. Hence, a more versatile control-based method is required to simplify the process while allowing the system to work under both linear and nonlinear load conditions.

3.2.3 Small-Signal Modeling and Operating Principles

As mentioned previously, the single-phase boost differential inverter can operate in two different modes. The DM operation focuses on delivering power from the dc source to the load while completing active power conversion. In the meantime, the CM operation directs the power to flow around the two dc-dc converters separately, aiming at regulating the dc offset voltages of the two output capacitors and forcing the current ripple to be assimilated by these capacitors. Hence, the dc source would be theoretically free from the low-frequency current disturbance, leaving its efficiency and lifespan unscathed. For the dual-mode operations, there are two differential equations derived from Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) that should always hold true regardless of the operating modes. The two equations also shed the light to the system modeling of the dual-mode operations, which are expressed as

$$L \frac{di_{Lj}}{dt} = V_{in} - (1 - d_j) v_{Cj} \quad (3-21)$$

$$C \frac{dv_{Cj}}{dt} = (1 - d_j) i_{Lj} + (-1)^j i_o \quad (3-22)$$

where j is either 1 or 2 that corresponds to the variable footers of the two dc-dc converters. The output voltage under the DM operation is defined as the difference of the two output capacitor voltages, whereas the dc offset voltage under the CM

operations equals the sum of the same pair of the variables. The system models under the two operating modes are also built based on these two equations. To simplify the analysis, the variables involved in the DM operation are generally expressed as

$$x_{DM} = (x_1 - x_2) / 2 \quad (3-23)$$

where x could either voltage, current or even duty cycle. The variables in the CM operation are defined similarly as,

$$x_{CM} = (x_1 + x_2) / 2 \quad (3-24)$$

By substituting x_{DM} into equations 3-21 and 3-22 and applying small-signal analysis before proceeding with ac equations and dismissing all second-order ac variables, the two equations above are transformed into

$$L \frac{d\hat{i}_{DM}}{dt} = \frac{D_1 \hat{v}_{C1} - D_2 \hat{v}_{C2} + \hat{d}_1 V_{C1} - \hat{d}_2 V_{C2}}{2} - \hat{v}_{DM} \quad (3-25)$$

$$C \frac{d\hat{v}_{DM}}{dt} = \hat{i}_{DM} - \frac{D_1 \hat{i}_{L1} - D_2 \hat{i}_{L2} + \hat{d}_1 I_{L1} - \hat{d}_2 I_{L2}}{2} - \frac{\hat{v}_{DM}}{R} \quad (3-26)$$

The dc components of above control variables are equal at the quiescent operating point due to the symmetry of the two dc-dc converter circuits, i.e., $V_{C1} = V_{C2} = V_C$, $I_{L1} = I_{L2} = I_L$, and $D_2 = D_1 = D$. Hence, the equations above can be further simplified as

$$L \frac{d\hat{i}_{DM}}{dt} = (D-1)\hat{v}_{DM} + V_C \hat{d}_{DM} \quad (3-27)$$

$$C \frac{d\hat{v}_{DM}}{dt} = (1-D)\hat{i}_{DM} - I_L \hat{d}_{DM} - \frac{\hat{v}_{DM}}{R} \quad (3-28)$$

The equivalent small-signal circuits are demonstrated in Figure 3.19. By taking the Laplace transform over the above equations and re-arranging the small-signal model in matrix form, the boost differential inverter's duty cycle-to-current and current-to-voltage transfer functions under the DM operation can be derived by solving the matrix,

Figure 3.19 Small-signal equivalent circuit of the DM operation.

Figure 3.20 Small-signal equivalent circuit of the CM operation.

$$G_{d2i_DM}(s) = \frac{\hat{i}_{DM}(s)}{\hat{d}_{DM}(s)} = \frac{CV_C s + (1-D)I_L + V_C / R}{LCs^2 + L/Rs + (1-D)^2} \quad (3-29)$$

$$G_{i2v_DM}(s) = \frac{\hat{v}_{DM}(s)}{\hat{i}_{DM}(s)} = \frac{(1-D)V_C - LI_L s}{CV_C s + (1-D)I_L + V_C / R} \quad (3-30)$$

By following the same procedures, the small-signal modeling equations of the CM operation can be derived similarly as

$$L \frac{d\hat{i}_{CM}}{dt} = \hat{v}_{in} + V_C \hat{d}_{CM} + (D-1)\hat{v}_{CM} \quad (3-31)$$

$$C \frac{d\hat{v}_{CM}}{dt} = (1-D)\hat{i}_{CM} - I_L \hat{d}_{CM} \quad (3-32)$$

the equivalent small-signal circuit of which is presented in Figure 3.20. By going through similar transforming procedures as illustrated above, the transfer functions under the CM operation can be derived as

$$G_{d2i_CM}(s) = \frac{\hat{i}_{CM}(s)}{\hat{d}_{CM}(s)} = \frac{CV_C s + (1-D)I_L}{LCs^2 + (1-D)^2} \quad (3-33)$$

$$G_{i2v_CM}(s) = \frac{\hat{v}_{CM}(s)}{\hat{i}_{CM}(s)} = \frac{(1-D)V_C - LI_L s}{CV_C s + (1-D)I_L} \quad (3-34)$$

Notably, the transfer functions above demonstrate uncanny resemblance to the small-signal modeling transfer functions of a simple boost dc-dc converter. The only difference is that the resistive load is characterized by the DM operation alone according to the equations above.

3.2.4 System Controller Design

The control scheme employed by this Case comprises three interconnected control block diagrams as presented in Figure 3.21. In a nutshell, the DM control scheme is configured to achieve ripple-free active power conversion under either linear or nonlinear load conditions. Whereas, the CM control scheme regulates dc offset voltage and eliminates ripple components in the input dc current. To obtain a deeper insight into the design of the control scheme, the three control block diagrams are dissembled for the detailed analysis.

a. DM Control Scheme Design

A classic double-loop control structure is employed for the boost differential inverter under DM operation, the control block diagram of which is demonstrated in Figure 3.22. Note that all transfer functions in the control diagram are presented in their respective z domain forms in order to approximate the control model to the real system. For the inner current control loop, z^{-1} represents one sample computational delay in the digital control system. A half sample PWM delay derived from the ZOH method is also integrated through the continuous to discrete conversion. K_{p_DM} is a proportional gain introduced to soothe the LC resonance. $G_{d2i_DM}(s)$ and $G_{i2v_DM}(s)$ are plant models, whose transfer functions are given in equations 3-29 and 3-30, respectively. For the outer voltage control loop, a PR controller loop is conventionally employed to

Figure 3.21 Control scheme of the single-phase differential boost inverter.

Figure 3.22 Proposed closed-loop control for output voltage regulation (DM operation). compensate the voltage ripple when the system only supplies linear load. However, in the case that the nonlinear load is considered, the output voltage could be severely distorted by the outburst of multiple odd-frequency ripple components, such as 3ω , 5ω , 7ω , and etc. As discussed previously, PR controllers can still be utilized under such multi-frequency ripple scenario. However, considering the challenge of dealing with the constant pop-up of new ripple components, repetitive controllers are considered a better alternative. Hence, a plug-in repetitive controller for odd-frequency voltage ripple reduction is employed in the control diagram in Figure 3.22. Note that the structure of the control diagram and the variables are completely the same as the one discussed in Figure 3.8 in Case-I. The only difference lies in the design of one parameter. As illustrated previously, a phase lead term z_{m1} is embedded in the forward path to compensate the phased delay caused by the control feedback, PWM process, and digital computation. Guided by the design principles specified in [70], $m_1 = 5$ is identified to have the best compensation effect for the DM voltage control loop. This parameter value is also validated by the system's Nyquist locus in MATLAB, which will be presented in the next subsection. The transfer function of the repetitive controller is given as

$$G_{rc_DM}(z) = K_{r1} \frac{Q(z) z^{\frac{N}{2} + m_1}}{1 + Q(z) z^{\frac{N}{2}}} \quad (3-35)$$

b. CM Control Scheme Design

Different from the implementation of DM operation, the control design of CM integrates two highly correlated control block diagrams, as presented in Figures 3.23 and 3.24, to achieve two separate goals. One of them is to ensure the two dc-dc boost converters are operating well within the linear modulation range by controlling the dc offset voltages of their respective output capacitors. For this purpose, the block diagram as shown in Figure 3.23 also adopts the classic double-loop control design. Particularly, the inner current loop is configured similarly as its DM counterpart due to the resemblance of their plant models. Note that a difference here is that a CM duty cycle d_{CM2} is added after the delay module before an integrated d_{CM} signal is formed and sent to the next block. For the outer voltage loop, a simple PI controller is employed to force the voltage to approach its reference value since only the dc component is concerned. $G_{d2i_CM}(s)$ and $G_{i2v_CM}(s)$ are plant models, whose transfer functions are given in equations 3-33 and 3-34, respectively.

The other goal of CM control design is to eliminate the ripple components in the input dc current as reflected in the control block diagram in Figure 3.24. By properly controlling the CM voltages of the two output capacitors, the predominant second-order current ripple can be significantly reduced according to the previous analysis. However, should the nonlinear load be supplied by the system, the odd-frequency ripple

Figure 3.23 Proposed closed-loop control for dc offset voltage regulation (CM operation).

Figure 3.24 Proposed closed-loop control for dc current ripple reduction (CM operation).

components would appear in the output voltage and subsequently intertwine with the fundamental component of the modulation signal, forming the even-frequency ripple components in the input dc current, i.e., 2ω , 4ω , 6ω , and etc. The corresponding flowchart can be found in Appendix.

To manage the multi-frequency ripple components in the input dc current, another plug-in repetitive controller $G_{rc_CM}(z)$ is adopted by the CM control scheme to regulate the dc current [85-87]. The control block diagram and variables of $G_{rc_CM}(z)$ are completely the same as the one presented in Figure 3.3. The only modified parameter is the phase-lead term z^{m_2} , where $m_2 = 3$ is adopted for the optimized delay compensation effect. The transfer function of the repetitive controller is expressed as

$$G_{rc_CM}(z) = K_{r2} \frac{Q(z) z^{\frac{N}{2} + m_2}}{1 - Q(z) z^{\frac{N}{2}}} \quad (3-36)$$

In addition, a high pass filter (HPF) $G_{HPF}(z)$ is included in the feedback loop since the implementation of the plug-in repetitive controller may introduce an integral term at 0 Hz frequency in addition to the spiky gains embedded at the even-order ripple frequencies. However, the extra integral term attempts to regulate the mean value of the input dc current, which might hinder the implementation of the DM voltage control. Given the conflicts involved in the different operations, a first-order LPF is also employed to compensate the high gain introduced by the integral term. The respective flowchart is given in Appendix.

c. Interleaved Modulation Design

One of the main issues that Case-I failed to address is the mitigation of ripple components at switching frequency. In Case-II, despite the multiple low-frequency ripple components in the input dc current are considerably reduced by the plug-in repetitive controller, PWM induced ripples whose sidebands are centered around the switching frequency and its multiples are still wildly existed. By employing an *LCL* filter or its more sophisticated ramifications at the output of the boost differential inverter, the PWM induced ripples can be theoretically suppressed [88]. However, the introduction of such additional electrical components would inevitably complicate the circuit configuration and increase both the size and costs of the system.

Fortunately, the symmetrical circuit structure of the boost differential inverter formed by two identical boost dc-dc converters allows switching frequency ripple suppression without resorting to any additional hardware. By integrating interleaved modulation into system control design, the PWM carriers of the two boost dc-dc converters are shifted in 180° . The 180° angular difference between the two PWM carriers results in the opposite changing directions of the two inductor currents i_{L1} and i_{L2} during certain switching periods. Since the input dc current i_{in} equals the sum of i_{L1} and i_{L2} , the increase in i_{L1} is immediately offset by the decrease in i_{L2} . Hence, the switching frequency ripples in the input dc current can be partially cancelled out as shown in Figure 3.25.

Theoretically, if the i_{L1} and i_{L2} have the same peak-to-peak amplitude, the performance of such ripple cancellation then depends on the values of their individual duty cycles. A detailed analysis conducted in [84] suggests the ideal cancellation effect occurs when the duty cycles of both i_{L1} and i_{L2} are set to be 0.6. In this case, nearly all switching frequency ripples in the input dc current are successfully cancelled out. Nevertheless, the peak-to-peak amplitudes of the inductor currents are constantly changing along with the line frequency. Moreover, the values of duty cycles also shift regularly due to the closed-loop control. Thus, only partial cancellation is able to be achieved in the boost differential inverter.

Figure 3.25 Proposed interleaved modulation for switching frequency ripple reduction.

3.2.5 Control System Stability Analysis

a. DM Operation

In studying the system stability under the influence of the plug-in repetitive controller, a proportional controller $G_v(z)$ is temporarily utilized to replace the repetitive controller for voltage control. As presented in Figure 3.26, the open-loop transfer function describing the mathematical relationship between current error e_{i_DM} and i_{DM} can be formulated as

$$G_{i_DMop}(z) = \frac{i_{DM}}{e_{i_DM}} = K_{p_DM} z^{-1} Z_{ZOH} [G_{d2i_DM}(s)] \quad (3-37)$$

The corresponding closed-loop transfer function of the current control can be derived accordingly as

$$G_{i_DMcl}(z) = \frac{i_{DM}}{i_{DM}^*} = \frac{G_{i_DMop}(z)}{1 + G_{i_DMop}(z)} \quad (3-38)$$

Similarly, the open-loop transfer function of the voltage control, according to Figure 3.26, can be expressed as,

$$G_{v_DMop}(z) = \frac{v_{DM}}{e_{v_DM}} = G_v(z) (1 - G_{i_DMcl}(z)) K_{p_DM} z^{-1} Z_{ZOH} [G_{d2i_DM}(s) G_{i2v_DM}(s)] \quad (3-39)$$

The corresponding closed-loop transfer function of the voltage control from v_o^* to v_{DM} is then derived as

$$G_{v_DMcl}(z) = \frac{v_{DM}}{v_o^*} = H_1(z) = \frac{G_{v_DMop}(z)}{1 + 2G_{v_DMop}(z)} \quad (3-40)$$

By incorporating the plug-in repetitive controller $G_{rc_DM}(z)$ into the closed-loop control block diagram in Figure 3.26, the transfer function of the entire control system can then

Figure 3.26 Proposed alternative control block diagram for output voltage regulation.

be derived by feeding a new voltage reference

$$v_{o*}'(z) = v_{o*} + (v_{o*} - 2v_{DM})G_{rc_DM}(z) \quad (3-41)$$

into equation 3-39, which can be reformulated as

$$G_{v_DMop}'(z) = (1 + G_{rc_DM}(z))G_{v_DMop}(z) \quad (3-42)$$

By substituting equation 3-42 into equation 3-40, the closed-loop transfer function of the entire control system for DM operation can be rewritten as

$$G_{v_DMcl}'(z) = \frac{(1 + G_{rc_DM}(z))G_{v_DMop}(z)}{1 + 2(1 + G_{rc_DM}(z))G_{v_DMop}(z)} = \frac{H_1(z)(z^{N/2} + Q(z) - K_{r1}Q(z)z^{m1})}{z^{N/2} + Q(z) - 2K_{r1}Q(z)z^{m1}H_1(z)} \quad (3-43)$$

From equation 3-43, the overall closed-loop control system is stable only if the root or roots of the characteristic function $z^{N/2} + Q(z) - 2K_{r1}Q(z)z^{m1}H_1(z)$ are located inside the unit circle. To simplify the analysis, a sufficient condition for system stability can be expressed as

$$\|Q(z)(1 - 2K_{r1}z^{m1}H_1(z))\| < 1, \forall z = e^{j\omega}, 0 < \omega < \frac{\pi}{T} \quad (3-44)$$

According to the equation 3-44, the system stability can be significantly affected by the values of $Q(z)$, K_{r1} , and $m1$, which makes them the elements of interest in designing a plug-in repetitive controller. The detailed analysis of the three variables above is elaborated in [84]. To test the system stability of the boost differential inverter under the DM operation, a Nyquist plot the equation 3-44 is delineated by MATLAB and presented in Figure 3.27.

Figure 3.27 Nyquist plot of $Q(z)(1 - 2K_{r1}z^{m1}H_1(z))$.

Clearly, the Nyquist locus of $Q(z)(1-2K_{r1}z^{m1}H_1(z))$ is completely encompassed by the unit circle according to the plot. This indicates that the condition in equation 3-44 is well satisfied and the system is considered stable at all frequencies up to Nyquist frequency.

b. CM Operation

For the CM operation, a repetitive controller for even-frequency current ripple suppression is employed in the current control loop to manage the issues with the nonlinear load. However, the introduction of the repetitive controller might cause stability concerns of the entire control system. Hence, it is necessary to investigate the system stability under the CM operation as well. Given the similar plant models utilized for the two operations, the same procedures could be applied to the control stability analysis of the CM operation.

Recall Figure 3.21, the duty cycle of the CM operation d_{CM} equals the sum of d_{CM1} and d_{CM2} . Thus, to simplify the analysis, the two control block diagrams in Figures 3.23 and 3.24 can be combined into a simplified control system for dc current ripple reduction as shown in Figure 3.28. According to Figure 3.28, the open-loop transfer function from the current error e_{i_CM} to the CM current i_{CM} can be written as

$$G_{i_CMop}(z) = \frac{i_{CM}}{e_{i_CM}} = \frac{K_{p_CM} z^{-1} Z_{ZOH} [G_{d2i_CM}(s)]}{1 + G_{HPF}(z) G_i(z) z^{-1} Z_{ZOH} [G_{d2i_CM}(s)]} \quad (3-45)$$

Where $G_i(z)$ and $G_{HPF}(z)$ are the discretized models of the current controller and the HPF with a cutoff frequency at 20 Hz. The corresponding closed-loop transfer function between i_{CM} and i_{CM}^* can be derived accordingly as

Figure 3.28 Proposed simplified control block diagram for dc current ripple reduction.

$$G_{i_CMcl}(z) = \frac{G_{i_CMop}(z)}{1 + G_{i_CMop}(z)} = \frac{K_{p_CM} z^{-1} Z_{ZOH} [G_{d2i_CM}(s)]}{1 + (K_{p_CM} + G_{HPF}(z) G_i(z)) z^{-1} Z_{ZOH} [G_{d2i_CM}(s)]} \quad (3-46)$$

Similarly, the open-loop transfer function of the voltage control loop (from the voltage error e_{v_CM} to the CM voltage v_{CM}) can be expressed as

$$G_{v_CMop}(z) = \frac{v_{CM}}{e_{v_CM}} = \frac{G_{pi}(z)(1 - G_{i_CMcl}(z)) K_{p_CM} z^{-1} Z_{ZOH} [G_{d2i_CM}(s) G_{i2v_CM}(s)]}{1 + G_{HPF}(z) G_i(z) z^{-1} Z_{ZOH} [G_{d2i_CM}(s)]} \quad (3-47)$$

The corresponding closed-loop transfer function from v_{dc}^* to v_{CM} can be derived similarly as

$$G_{v_CMcl}(z) = \frac{v_{CM}}{v_{dc}^*} = H_2(z) = \frac{G_{v_CMop}(z)}{1 + G_{v_CMop}(z)} \quad (3-48)$$

Similar to the control design of the DM operation for output voltage regulation, a plug-in repetitive controller $G_{rc_CM}(z)$ is implanted into equation 3-48. Through the same procedures including combination, substitution, and transformation, the closed-loop transfer function of the overall control system for current ripple reduction can be rewritten as

$$G'_{v_CMcl}(z) = \frac{(1 + G_{rc_CM}(z)) G_{i_CMop}(z)}{1 + (1 + G_{rc_CM}(z)) G_{i_CMop}(z)} = \frac{H_2(z)(z^{N/2} - Q(z) + K_{r2} Q(z) z^{m2})}{z^{N/2} - Q(z) + K_{r2} Q(z) z^{m2} H_2(z)} \quad (3-49)$$

As mentioned previously, a sufficient condition for system stability based on the equation 3-49 can be expressed as

Figure 3.29 Nyquist plot of $Q(z)(1 - K_{r2} z^{m2} H_2(z))$.

$$\left\| Q(z) \left(1 - K_{r2} z^{m2} H_2(z) \right) \right\| < 1, \forall z = e^{j\omega}, 0 < \omega < \frac{\pi}{T} \quad (3-50)$$

The Nyquist locus of the equation 3-50 presented in Figure 3.29 suggests that the stability condition is satisfied since the entire locus is encompassed by the unit circle. The result is also consistent with the simulation results obtained from a piecewise linear electrical circuit simulation. The conclusion is also verified by the experimental results in the next subsection.

c. Overall Control System Stability

Clearly, the overall control system is linearly related to both DM and CM subsystems as demonstrated by the composition of the two output duty cycles in Figure 3.21. In addition, according to the previous analysis, the control of DM and CM signals are mutually independent, whereby no interactions are identified between the two subsystems. Based on the superposition principle, the stability of all subsystems can directly reflect the stability of the overall system provided that the overall system is linearly related to each subsystem and no interaction occurs among subsystems. Since both requirements are soundly met in this case, the stability of the overall control system is thereby confirmed.

Figure 3.30 Testbed for experimental verification.

3.2.6 Experimental Results

In order to further validate the effectiveness of the control schemes introduced in the last subsection, a 500 W prototype of the single-phase boost differential inverter was set up in the laboratory as shown in Figure 3.30. Note that the values of the parameters used in the experiments are in consistence with the ones applied to both simulations and stability analysis. Table 3.2 gives the values of the system parameters.

a. Linear Load Experimental Results

The steady-state experimental results of the single-phase boost differential inverter under the linear load condition are exhibited in Figures 3.31 and 3.32. Clearly, without the current ripple reduction control and interleaved modulation, the input dc current is severely polluted by the second-order current ripple as shown in Figure 3.31. In addition, the input current waveform appears to be thick, which suggests the existence of current ripple components at switching frequency are intertwined with the dc current.

Table 3.2: Boost differential inverter circuit parameters.

Parameters	Value
Nominal input power P_n	500 W
Switching frequency f_s	19.2 kHz
Line frequency f_n	60 Hz
Output capacitance C_1, C_2	60 μ F
Boost inductance L_1, L_2	1.4 mH
Input voltage V_{in}	150 V
Dc offset voltage V_{dc}	260 V
Output voltage V_o	110 V

Figure 3.31 Steady-state experimental results under linear load condition (with neither current ripple reduction control nor interleaved modulation).

Figure 3.32 Steady-state experimental results under linear load condition (with both proposed current ripple reduction control and interleaved modulation).

By enabling both the current ripple reduction control and interleaved modulation, the input dc current immediately becomes smoother and flatter as demonstrated in Figure 3.32. Besides, the waveform of the current also becomes notably slimmer as compared to its previous state, suggesting the switching frequency current ripples are considerably reduced thanks to the interleaved modulation.

Furthermore, the effectiveness of the control design is also confirmed by the results of the FFT analysis on the input dc current as shown in Figures 3.33 and 3.34. The amount of second-order current ripple component drops by an impressive 98.5% as a result of the control design as shown in Figure 3.33. The FFT analysis on the switching frequency current ripples also reveals that the high-frequency ripple components also fall by more than two-thirds in the input dc current as shown in Figure 3.34. Therefore, the effectiveness of the control design on current ripple reduction is duly confirmed by both experimental and statistical results.

Figure 3.33 FFT analysis results on low-frequency current ripple components in the input dc current under linear load condition.

Figure 3.34 FFT analysis results on switching frequency current ripple components in the input dc current under linear load condition.

b. Nonlinear Load Experimental Results

As illustrated previously, the control schemes are equally capable of suppressing the multiple low-frequency current ripples when the system supplies nonlinear loads. To validate this theory, a full-bridge diode rectifier supplying an RLC ($470 \mu\text{F}$, 0.5 mH and 120Ω) load is connected to the output side. The steady-state experimental results under nonlinear load condition are presented in Figures 3.35 and 3.36. When the current ripple reduction control is not enabled, the input dc current is obviously contaminated by a series of low-frequency even-order current ripples as shown in Figure 3.35. The current waveform, however, is in good agreement with the previous analysis. Besides, the current waveform appears to be thick which implies the existence of current ripple components at switching frequency.

As soon as the current ripple reduction control and interleave modulation are enabled, the input dc current becomes significantly less distorted. In the meantime, the switching

Figure 3.35 Steady-state experimental results under nonlinear load condition (with neither current ripple reduction control nor interleaved modulation).

Figure 3.36 Steady-state experimental results under nonlinear load condition (with both proposed current ripple reduction control and interleaved modulation).

frequency ripple components are reduced dramatically as manifested by the much slimmer current waveform. Note that the current peaks are also considerably attenuated, which would otherwise easily surge to a high value and falsely trigger the overcurrent protection should an unexpected oscillation occur.

The results of FFT analysis on the two types of ripple components in the input dc current are respectively presented in Figures 3.37 and 3.38. Apparently, when the current ripple reduction control is activated, the proportions of 2ω , 4ω , 6ω , and 8ω current ripples against dc component decline substantially with a combined reduction over 96% as shown in Figure 3.37. In the meantime, the activation of the interleaved modulation also leads to a major decrease of the current ripple components at switching frequency, the magnitude of which drops by almost 80% according to Figure 3.38.

Figure 3.37 FFT analysis results on low-frequency current ripple components in the input dc current under nonlinear load condition.

Figure 3.38 FFT analysis results on switching frequency current ripple components in the input dc current under nonlinear load condition.

The transient response of the system under nonlinear load is also studied, and the results are presented in Figure 3.39 corresponding to a 50% step down of the resistive component of the nonlinear load (from 120 Ω to 60 Ω). The waveforms suggest excellent dynamic response with minor oscillatory transient immediately followed by the step change. Despite the positive experimental results, it is necessary to note that

Figure 3.39 Nonlinear load experimental results under load step change. (with both proposed current ripple reduction control and interleaved modulation).

Table 3.3: Comparative results of dc current ripple reduction with the proposed control and the waveform control in [81] and [83].

Linear Load Case	Proposed Control	Waveform Control [81]
Second-order current ripple reduction	98.54%	93.69%
Switching frequency current ripple reduction	69.15%	N.A.
Nonlinear Load Case	Proposed Control	Waveform Control [83]
Second-order current ripple reduction	98.05%	92.68%
Fourth-order current ripple reduction	96.09%	83.87%
Sixth-order current ripple reduction	94.91%	86.36%
Eighth-order current ripple reduction	98.08%	38.46%
Switching frequency current ripple reduction	79.45%	N.A.

electrical transients such as instantaneous power fluctuation and overload conditions could result in instantaneous system power imbalance due to the slow dynamic response nature of many dc sources. A solution to this problem is by integrating a supercapacitor module along with the dc source [89].

Finally, Table 3.3 compares the percentage of dc current ripple reduced by the control design introduced in this case with that reported in [81] and [83]. Clearly, the waveform control in [81] is incapable of managing current ripples when the system supplies nonlinear load. Even under a purely resistive load scenario, the control design of this case exhibits a better performance in mitigating second-order current ripple components. As an improved design to [81], the closed-loop waveform control in [83] may allow the system to operate properly under nonlinear load condition. Nevertheless, the effectiveness of its current ripple reduction declines as frequency increases. In contrast, the control design introduced in this case demonstrates a consistently better performance up to Nyquist frequency. Furthermore, the introduction of interleaved modulation allows significant mitigation of current ripples at switching frequency, which is another type of current ripples that was overlooked by both [81] and [83].

3.2.7 Summary and Outlook

In this case, the low-frequency current ripples are identified as one of the root causes of renewable energy sources', i.e., fuel cells declined efficiency, underperformance and reduced lifespan. The analysis reveals the chemical and physical correlations between the low-frequency ripples in the dc current and their impact on the dc source. To address the problem, a dual-mode operated single-phase boost differential inverter was implemented under control schemes characterized by repetitive controllers. The control schemes maintain excellent performance in current ripple suppression regardless of the types of load supplied by the system. The investigation into the control scheme performance in conjunction with repetitive controllers further validates the system design in terms of stability and dynamic response. Besides the successful suppression of the low-frequency current ripples, the current ripple components at switching frequency are also significantly reduced thanks to the interleaved modulation introduced in this case.

Capacitance-wise, the implementation of the control design allows the capacitance of the two output capacitors to be as low as 60 μF , which is substantially less than what was required by the similar topologies in the existing literature. Due to such considerably reduced output capacitance requirement, F-Caps are utilized in the experiments and have demonstrated excellent capability in managing ripple components. As elaborated in previous chapters, the replacement of E-Caps with F-Caps in reduced capacitance contributes to the improved reliability of power converter systems. From that perspective, the dual-mode control design discussed in this case has successfully achieved that goal.

However, moving forward, an interesting question to consider is whether the replacement of reliability-critical electrical components i.e., capacitors, is the only approach to boosting system reliability. The short answer is no. There are plenty of alternative ways to achieve that end by addressing other reliability-oriented issues associated with the system. One promising area would be studying the reliability issues associated with frequency regulation when the grid is connected to the renewable generators through fast response power converters.

Unlike synchronous generators, renewable generators, e.g. PV arrays and wind turbines,

cannot provide rotating inertia when connected to the grid through power converters. As a result, excessive grid frequency deviations are likely to occur in the event of generator tripping and/or load shedding. Apparently, frequency deviations would have a detrimental effect on the grid as well as the downstream power transmission and distribution at large. Fortunately, there is an effective approach to addressing this challenge by properly controlling the power converters. By proportionally associating the dc-link voltage of the GCCs with the grid frequency, the power converters can generate a fixed amount of virtual inertia for frequency support.

The next chapter is dedicated to further developing this idea that allows the power converters to contribute an even higher amount of virtual inertia in the event of frequency deviation. This is achieved by introducing a frequency deadband into the frequency controller, which can increase virtual inertia in shorter time duration, leading to the reduced frequency deviations and output energy of power converters. More importantly, the next chapter also reveals that the introduction of frequency deadband in system controller design also helps improve the reliability of power converter systems.

Specifically, when a frequency deadband is embedded in the controller, the dc-link voltage is found to change only when the maximum frequency deviation exceeds the upper or lower limit of the preset frequency deadband value, i.e. $|f_{\text{dead}}| = 0.1 \text{ Hz}$. Therefore, the unnecessary voltage changes during frequency events can be substantially avoided, which contributes to preserving and even extending the lifespan of dc-link capacitors. Since capacitors are considered one of the top reliability-critical passive electrical components in power converter systems, the preservation and extension of capacitors' lifespan directly contribute to improving the reliability of the entire system. More detailed analysis and descriptions will be elaborated in the next chapter.

Chapter 4

Capacitor Ripple Reduction with Virtual Inertia Control

Another reliability issue with power converters arises in the context of renewable energy grid integration. Since renewable energy generators cannot provide rotating inertia when connected to the grid through power converters, excessive grid frequency deviations are likely to occur in the event of generator tripping and or/load shedding. An effective approach to increasing inertia is associating the dc-link voltage of GCCs with the grid frequency, allowing power converters to generate a fixed amount of virtual inertia for frequency support. However, the downside of this method is that even an insignificant grid frequency deviation could trigger a major voltage change in dc-link capacitors. The voltage ripples are detrimental to the lifespan of capacitors, and hence considered unfavorable from power converter reliability's perspectives. To further improve frequency regulation and enhance the reliability of power converters, this chapter introduces a frequency deadband-based virtual inertia controller for power converters to perform inertia control during frequency events. The controller enables the increment of inertia in a shorter time duration via a frequency deadband, leading to an improved frequency nadir and a reduction of the energy required for emulation. More importantly, the introduction of the frequency deadband allows unnecessary voltage changes under normal system operating conditions to be avoided, thus contributing to suppressing voltage ripples in dc-link capacitors and improving the reliability of power converters.

4.1 Background

Due to their clean and sustainable features, renewable energy resources (RESs) have been increasingly deployed in power systems to replace fossil fuels. As a result, conventional gas/steam turbines and synchronous generators (SGs) are gradually being phased out [90]. Conventionally, RESs are integrated into the grid through fast-response power converters. However, this RES-power converter architecture itself does not generate any rotating inertia, resulting in decreased power system inertia [88], [90-91]. Hence, frequency deviations are very likely to exceed the acceptable range in the event of generator tripping and/or load shedding [92]. Considering the large penetration of RESs in some modern power systems, such excessive frequency deviations could trigger cascaded failure even large-scale blackout [93-94]. For instance, turbine blades might have to bear vibratory stresses as a result of those generating units operating at a low frequency, causing the reduced output of fans [91]. Under such circumstance, under-frequency protective relays are activated by protocol, which ensures generators will be tripped off in the event of excessive frequency decline. Apparently, the incidents like generation tripping, cascaded failure, and even electrical island have a fairly high chance to occur due to the inadequate system inertia. In addition, the occurrence of these incidents would inevitably affect the reliability of the grid-connected power converter system as a whole. Recall the concept of reliability defined in Chapter 1, the reliability of an electronic component is frequently connected to its failure rate, i.e. failures per million hours. In the context of frequency deviation, this concept could also be applied to the entire grid-connected power converter system. Hence, in order to maintain an acceptable level of reliability for the entire system, it is necessary to explore effective approaches to compensating the system inertia so that the incidents resulted from frequency deviation could be duly avoided.

Straightforward approaches for inertia enhancement include employing extra energy storage into power systems to provide frequency support, such as batteries, supercapacitors, and flywheels. Those grid-scale energy storage devices have reportedly been utilized to smooth the output power fluctuations and facilitate the frequency regulation of renewable energy generation systems [95-97]. However, the drawback associated with the employment of is obvious, the limited lifespan, efficiency, and reliability of those devices become the system-wide concerns. Another prevailing

method is to count on the inertia collectively generated by multiple SGs operating at partial load conditions [91]. Nevertheless, the solution introduces additional components to the system, giving rise to elevated costs, increased system complexity, and even safety concerns. Instead of relying on backup synchronous generators, a proven approach refers to the inertia emulation by wind turbines, where speed recovery poses a special challenge and remains under active research [98].

In contrast, dc-link capacitors are integral components of GCCs to maintain stable dc-link voltages and filter out switching harmonics. By associating the dc-link voltage with the grid frequency through a proportional gain, power converters can be controlled to generate virtual inertia for frequency support without incurring any modification of system hardware [17], [99-100]. Unfortunately, dc-link voltages keep varying under the normal operating conditions. In addition, a further improvement of the frequency nadir and reduction of the energy requirement are desired.

In the light of the abovementioned concerns, a deadband-based frequency controller for GCCs is introduced in this chapter. The designed controller can increase virtual inertia and shorter time duration, leading to the reduced frequency deviations and energy supply of power converters. In addition, with the implementation of frequency deadband, the dc-link voltage only changes when the frequency deviation exceeds the preset frequency deadband. Hence, unnecessary voltage changes during frequency events can be largely avoided, which contributes to preserving and even extending the lifespan of dc-link capacitors. In the meantime, it is worth to note that the designed controller does not affect the normal operation of power converters.

4.2 System Configuration

The configuration of a small-scale power system composed of a three-phase virtual synchronous generator (VSG) and a three-phase GCC is demonstrated in Figure 4.1, where the VSG is designed to behave similarly as a synchronous generator for voltage and frequency regulation, while the GCC operates as an ac current source for power regulation [17]. In particular, VSG is employed to corroborate the improvement of frequency regulation made by GCC. Details of the system configuration are thoroughly discussed [17]. Under normal operating conditions, the dc-link voltage v_{dc} of the GCC

Figure 4.1 Configuration of a small-scale power system.

is kept constant by a standard cascaded voltage and current controller, where proportional-integral (PI) controllers are employed in the voltage and current loops. During frequency events, the GCC is expected to provide inertia and reduce frequency deviations through the designed virtual inertia controller.

4.3 Frequency Deadband-Based Virtual Inertia Controller

The control block diagram of the frequency control framework with the designed frequency deadband-based virtual inertia controller is presented in Figure 4.2. The frequency regulation model considers the behaviors of speed governor, reheat turbine, and loads [101]. The prefix Δ and subscript pu denote the changes and per-unit values (the ratios of real values to rated values) of the corresponding parameters, respectively. For the conventional virtual inertia control scheme, the frequency change Δf_r and the power change of the GCC ΔP_{dc} is proportionally associated [17]. Hence, the GCC is able to contribute to frequency regulation by virtual inertia during frequency events. The corresponding virtual inertia coefficient can be expressed as follows according to [17]

$$H_{gcc} = K_{wv} H_c \quad (4-1)$$

where H_{gcc} represents the virtual inertia coefficient of GCC. The inertia coefficient of dc-link capacitors H_c is formulated as the capacitor energy divided by the system base power VA_{base}

Figure 4.2 Frequency control framework with the designed deadband-based virtual inertia controller.

$$H_c = \frac{C_{dc} V_{dc}^2}{2VA_{base}} \quad (4-2)$$

where C_{dc} and V_{dc} denote dc-link capacitance and the rated dc-link voltage, respectively.

K_{wv} stands for the virtual inertia gain, which was organized as follows in [17]

$$K_{wv} = \left(\frac{\Delta V_{dc_max}}{V_{dc}} \right) / \left(\frac{\Delta f_{r_max}}{f_{ref}} \right) \quad (4-3)$$

Where the maximum dc-link voltage ΔV_{dc_max} is formulated as

$$\Delta V_{dc_max} = \frac{(V_{dc_max} - V_{dc_min})}{2} \quad (4-4)$$

V_{dc_max} and V_{dc_min} are the upper and lower threshold values of dc-link voltages. Δf_{r_max} denotes the maximum frequency deviation. Since the system parameter values appeared in Figure 4.2 are in per unit forms. Hence ΔV_{dc_max} and Δf_{r_max} are divided by their respective rated values V_{dc} and f_{ref} .

When a frequency deadband f_{dead} is introduced in the virtual inertia controller, K_{wv} can be reorganized as

$$K_{wv} = \left(\frac{\Delta V_{dc_max}}{V_{dc}} \right) / \left(\frac{\Delta f_{r_max} - f_{dead}}{f_{ref}} \right) \quad (4-5)$$

where f_{dead} represents the upper limit of the frequency deadband. On the basis of the control structure illustrated in [17], an exclusively designed frequency deadband is introduced in the frequency controller. By substituting equations 4-2, 4-5 into equation 4-1, the expression of virtual inertia coefficient H_{gcc} can be updated as:

Table 4.1: System and control parameter values.

Description	VSG	Description	GCC
Droop coefficient R	0.05 s	Rated dc-link voltage V_{dc}	380 V
Speed governor coefficient T_G	0.2 s	Maximum dc-link voltage V_{dc_max}	420 V
Turbine HP coefficient F_{HP}	0.3 s	Minimum dc-link voltage V_{dc_min}	340 V
Time constant of reheater T_{RH}	7.0 s	Maximum voltage deviation ΔV_{dc_max}	40 V
Time constant of main inlet volumes T_{CH}	0.3 s	Dc-link capacitance C_{dc}	2.82
Inertia coefficient of SG H	5.0 s	Virtual inertia coefficient H_{gcc}	10.7 s
Rated frequency deviation f_{ref}	50 Hz	Rated frequency f_{ref}	50 Hz
Maximum frequency deviation Δf_{r_max}	0.2 Hz	Maximum frequency deviation Δf_{r_max}	0.2 Hz
Damping coefficient D	1.0	Frequency controller K_{wv}	26.32
Power rating VA_{base}	500 VA	Frequency deadband f_{dead}	0.1 Hz

$$H_{gcc} = \frac{\Delta V_{dc_max} f_{ref} C_{dc} V_{dc}}{2VA_{base} (\Delta f_{r_max} - f_{dead})} \quad (4-6)$$

The main difference between the above controller design and the fixed inertia control reported in [17] can be observed from the correlations of Δf_r and ΔV_{dc} as revealed in Figure 4.3. Clearly, Δf_r and ΔV_{dc} are linearly correlated in [17] where even an insignificant frequency deviation could trigger a major voltage change. In contrast, when a frequency deadband is embedded in the controller, the voltage only changes when the maximum frequency deviation exceeds the upper or lower limit of the preset frequency deadband value, i.e. $|f_{dead}| = 0.1$ Hz. Therefore, the unnecessary voltage changes during frequency events can be substantially avoided, which contributes to preserving and even extending the lifespan of dc-link capacitors [19]. The system parameters are listed in Table 4.1.

In addition, it is revealed in the analysis that within the range of the maximum frequency deviation, i.e. $\Delta f_{r_max} = 0.2$ Hz [102], the employment of frequency deadband can noticeably increase the value of frequency nadir. Furthermore, a positive correlation between the two parameters can also be observed. The improvement of frequency nadir f_{dead} is another benefit of introducing the frequency deadband f_{dead} into the controller besides extending the lifespan of dc-link capacitors by avoiding unnecessary voltage changes.

Figure 4.3 Correlations between frequency change Δf_r and voltage change ΔV_{dc} .

4.4 Quantitative Analysis of Frequency Nadir

This subsection is dedicated to illustrating and quantifying the influence of the frequency deadband f_{dead} on frequency regulation, particularly for the improvement of the frequency nadir f_{r_nadir} . To achieve this objective, the impact of power system inertia on frequency regulation is discussed first. Referring to Figure 4.2, one can derive the transfer function from the load distribution ΔP_{RL_pu} to the frequency change Δf_{r_pu} as

$$G_{RL-freq}(s) = \frac{\Delta f_{r_pu}}{\Delta P_{RL_pu}} = - \frac{R(1+sT_G)(1+sT_{CH})(1+sT_{RH})}{(2Hs + 2K_{wv}H_c s + D)(1+sT_G)(1+sT_{CH})(1+sT_{RH})R + sF_{HP}T_{RH} + 1} \quad (4-7)$$

According to the analysis conducted in [17], equation 4-7 can be further simplified into

$$\begin{aligned} G_{RL-freq}(s) &= - \frac{R(1+sT_{RH})}{(2Hs + 2K_{wv}H_c s + D)(1+sT_{RH})R + sF_{HP}T_{RH} + 1} \\ &= - \frac{1}{2(H + K_{wv}H_c)} \cdot \frac{s + m_1}{s^2 + 2\zeta\omega_{ud}s + \omega_{ud}^2}, \end{aligned} \quad (4-8)$$

Where $m_1 = 1/T_{RH}$. ω_{ud} and ζ respectively denote the undamped natural frequency and damping ratio, which are expressed as

$$\omega_{ud} = \sqrt{\frac{1 + DR}{2(H + K_{wv}H_c)RT_{RH}}} \quad (4-9)$$

$$\zeta = \frac{2(H + K_{wv}H_c)R + DRT_{RH} + T_{RH}F_{HP}}{4(H + K_{wv}H_c)RT_{RH}} \cdot \frac{1}{\omega_{ud}} \quad (4-10)$$

Under a step-up load change, the grid frequency can be derived in the s domain as

$$\begin{aligned} f_{r_pu}(s) &= f_{ref_pu}(s) + \frac{G_{RL_freq}(s)}{s} \\ &= \frac{1}{s} - \frac{1}{2(H + K_{wv}H_c)} \left\{ \frac{1}{\omega_d} \cdot \frac{\omega_d}{(s + \zeta\omega_{ud})^2 + \omega_d^2} + \frac{m_1}{\omega_{ud}^2} \right. \\ &\quad \left. \cdot \left[\frac{1}{s} - \frac{s + \zeta\omega_{ud}}{(s + \zeta\omega_{ud})^2 + \omega_d^2} - \frac{\zeta\omega_{ud}}{\omega_d} \cdot \frac{\omega_d}{(s + \zeta\omega_{ud})^2 + \omega_d^2} \right] \right\} \end{aligned} \quad (4-11)$$

where the grid reference $f_{ref_pu}(s)$ and frequency deviation $G_{RL_freq}(s)$ are introduced in per unit fashion. ω_d represents the damped frequency, i.e.

$$\omega_d = \omega_{ud} \sqrt{1 - \zeta^2} \quad (4-12)$$

Given the equation of the grid frequency in the s domain, the corresponding expression in the time domain can be simply derived by taking the inverse Laplace transform of equation 4-11:

$$f_{r_pu}(t) = 1 - \frac{1}{2(H + K_{wv}H_c)} \left[\frac{m_1}{\omega_{ud}^2} - e^{-\zeta\omega_{ud}t} J \sin(\omega_d t + \theta) \right] \quad (4-13)$$

where

$$J = \sqrt{\left(\frac{m_1}{\omega_{ud}^2}\right)^2 + \left(\frac{-m_1\zeta + \omega_{ud}}{\omega_{ud}\omega_d}\right)^2}, \theta = \arctan \left[\frac{m_1\omega_d}{(m_1\zeta - \omega_{ud})\omega_{ud}} \right] \quad (4-14)$$

By setting $f_{r_pu}(t) = f_{dead}$ and solving the inverse function of equation 4-13, the breakthrough time t_{bt} when the frequency deviation exceeds the preset frequency deadband f_{dead} can be determined. Following the attainment of equation 4-13, one can obtain several key indices, including peak time t_{peak} and frequency nadir f_{r_nadir} , to further evaluate frequency regulation performances. The peak time t_{peak} is derived as follows:

$$t_{\text{peak}} = \frac{1}{\omega_{ud}} \cdot \left[\arctan\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) - \theta + \pi \right] \quad (4-15)$$

By substituting equation 4-15 into equation 4-13, the equation of peak frequency, also known as the frequency nadir f_{r_nadir} , is obtained as

$$f_{r_nadir} = 1 - \frac{m_1}{2(H + K_{wv}H_c)\omega_{ud}^2} - \frac{Je^{-\zeta\omega_{ud}t_{\text{peak}}}\sqrt{1-\zeta^2}}{2(H + K_{wv}H_c)} \quad (4-16)$$

The relationship between frequency deadband f_{dead} and virtual inertia gain K_{wv} is initially revealed in equation 4-5. Note that the equations of several other variables in equation 4-16 including ω_{ud} , ζ , and t_{peak} , all comprise virtual inertia gain K_{wv} as demonstrated in equations 4-9, 4-10 and 4-15, respectively. Therefore, based on equations 4-5 and 4-16, it is safe to conclude that frequency deadband f_{dead} has a certain influence on frequency nadir f_{r_nadir} , and hence, the frequency regulation. The quantitative relationship between frequency deadband f_{dead} and frequency nadir f_{r_nadir} is presented in Figure 4-4. It is worth to note that the quantitative relationship between frequency deadband f_{dead} and frequency nadir f_{r_nadir} can be derived from equation 4-16 after the maximum frequency deviation exceeds the preset frequency deadband f_{dead} at peak time t_{peak} . Before such a breakthrough, the system inertia frequency regulation provided by VSG alone. In that case, the equation characterizing the relationship frequency nadir f_{r_nadir} and system inertia remain essentially the same as equation 4-16, except the term ' $H + K_{wv}H_c$ ' in the corresponding variables is replaced by simply an ' H '.

As demonstrated in Figure 4-4, within the range of $\Delta f_{r_max} = 0.15$ Hz, the employment of frequency deadband can noticeably increase the value of frequency nadir. Furthermore, a nearly positive correlation between the two variables can also be observed from this figure. The improvement of frequency nadir is another benefit of introducing the frequency deadband f_{dead} into the controller besides extending the lifespan of dc-link capacitors by avoiding unnecessary voltage changes as discussed previously. The accuracy of this quantitative analysis and predicted values is later tested and confirmed by both simulation and experimental results as illustrated in the next subsection.

Figure 4.4 Quantitative relationship between frequency deadband f_{dead} and frequency nadir f_{r_nadir} .

As shown in Figure 4-4, frequency nadir increases almost linearly with frequency deadband up until frequency deadband approaches 0.13 Hz, where it starts to drop. The plot presents the following insights when it comes to selecting the value of frequency deadband:

- The value of frequency deadband should always sit between 0 and Δf_{r_max}
- The relationship between frequency deadband and frequency nadir is nonlinear
- To determine the local optimal of frequency deadband, it is suggested to plot Figure 4.4 using the equations 4-5 and 4-16 as well as the parameters listed in Table 4-1
- Finally, the local optimal of frequency deadband is the value of f_{dead} that corresponds to the peak value of f_{r_nadir} in Figure 4-4

4.5 Simulation Results

In order to validate the effectiveness of the designed frequency deadband-based virtual inertia controller, simulations were carried out under the MATLAB and Simulink environment based on the system parameter values listed in Table 4-1. The simulation results of the systems without virtual inertia, with the fixed virtual inertia reported in [17], and with the frequency deadband-based virtual inertia under a 5% step-up load change at $t_0 = 0$ s are respectively demonstrated in Figures 4-5, 4-6, and 4-7.

Clearly, the frequency deadband-based method allows further reduction of frequency deviation on top of the already impressive performance achieved by the fixed inertia method in [17], as presented in Figure 4-5. Specifically, the observed frequency nadir is improved 10% under the completely same set of parameter values, which further lowers the probability of occurrence for incidents such as generator tripping and/or load shedding. In addition, the waveforms of dc-link voltage are presented in Figure 4-6. Under the frequency deadband-based method, the dc-link voltage only starts to change after a certain period when the maximum frequency deviation exceeds either the upper or lower limit of the preset frequency deadband. The less frequent voltage change encountered by the dc-link capacitor is beneficial to the inner chemical reaction stability of the passive electrical components, which contributes to extending its lifespan. Since

Figure 4.5 Simulated results: grid frequency f_r under a 5% step-up load change.

Figure 4.6 Simulated results: dc-link voltage v_{dc} under a 5% step-up load change.

capacitors are one of the top reliability-critical electrical components in power converter systems, a well-preserved dc-link capacitor does help improve the reliability of the entire system.

In the meantime, this phenomenon can be observed from the different points in time when the voltages start to vary. Besides, the results also indicate that the designed method incurs a smaller overall voltage change as compared to [17]. The reduced

Figure 4.7 Simulated results: output energy ΔE_r under a 5% step-up load change.

voltage change also translates into the lessened energy output from power converters as shown in Figure 4-7. Note that in the steady state, the energy drawn from the frequency deadband-based method drops to the almost a quarter of what is required should the fixed virtual inertia control be implemented instead. Therefore, it is safe to conclude that with the frequency deadband-based method, it is possible to further increase inertia to minimize frequency deviations during frequency events. Meanwhile, it is worth to note that the frequency deadband-based method will not affect the normal operation of power converter systems in the steady state since their respective dc-link voltages are maintained as a constant $\Delta V_{dc_∞}$.

4.6 Experimental Results

To further validate the effectiveness of the frequency deadband-based method, experiments were carried out with the prototype shown in Figure 4.8 using the system parameter values listed in Table 4-1. The control algorithms for both VSG and GCC were executed via a dSPACE control platform. Inductor windings area made of Litz wires with low equivalent series resistance. A TELEDYNE LECROY 8038 oscilloscope was utilized to capture the experimental waveforms before exporting them into MATLAB for further analysis.

Figure 4.9 demonstrates the experimental results of the system frequency deviation when subject to a 5% step-up load change. Without any virtual inertia control, the maximum frequency deviation Δf_{r_max} ($= f_{ref} - f_{r_nadir}$) mounts up to an alarming 0.277 Hz, which dramatically exceeds the normal operating frequency band prescribed by

Figure 4.8 Photo of the experimental prototype.

Figure 4.9 Experimental results: grid frequency f_r under a 5% step-up load change.

international grid codes applied to countries/regions, such as Singapore, Europe and North America [103-105]. Whereas, this value is reduced to less than 0.18 Hz when the frequency deadband-based controller is enabled. In the meantime, the performance of the frequency deadband-based method is unequivocally superior to that of the fixed virtual inertia control discussed in [17], which only manages to reduce this value to around 0.20 Hz as demonstrated in Figure 4.9.

In the meantime, as can be seen from Figure 4.10, the dc-link voltage remains virtually unchanged when none of the virtual inertia controls is activated. This is because the dc-link capacitor is not involved in generating virtual inertia and hence, regulating frequency. In contrast, when either of the virtual inertia control is activated, a sizeable voltage swing can be observed. However, the scale of voltage under the frequency deadband-based method is noticeably smaller than that proposed in [17]. More importantly, under the frequency deadband-based method, the dc-link voltage only starts to change after approximately 0.4 seconds, that is when the maximum frequency deviation Δf_{r_max} exceeds the upper limit of the preset frequency deadband f_{dead} . As

Figure 4.10 Experimental results: dc-link voltage v_{dc} under a 5% step-up load change.

Figure 4.11 Experimental results: output energy ΔE_r under a 5% step-up load change.

mentioned previously, the less frequency voltage change contributes to preserving and even extending the lifetime of dc-link capacitors, which is one of the most reliability-critical components in power converter systems [6], [103]. Hence, the introduction of frequency deadband into the controller design does help improve the reliability of the power converter systems.

Finally, the frequency deadband-based method also manages to significantly reduce the amount of energy required during this operating process. Compared to what is reported in [17], the peak output energy from power converters under the frequency deadband-based method is about 22% less. Whereas, this gap climbs to a whopping 73% when the output energy reaches the steady state as shown in Figure 4.11. Thanks to the frequency deadband-based method, significantly less energy is now required for inertia emulation.

4.7 Summary and Outlook

In this chapter, a frequency deadband-based controller is introduced for GCCs to generate virtual inertia and support frequency regulation during frequency events in the context of the growing penetration of renewable energy generation. As discussed previously, renewable generators cannot provide rotating inertia when connected to the grid through power converters. An immediate consequence of that would be the decreased power system inertia. Under such circumstance, frequency deviations are very likely to exceed the acceptable range in the event of generator tripping and/or load shedding.

A widely acknowledged approach to addressing this issue is by associating the dc-link voltage of GCCs with the grid frequency, allowing power converters to generate a fixed amount of virtual inertia for frequency support. Since dc-link capacitors are integral components of GCCs to maintain stable dc-link voltages and filter out switching harmonics, this solution does not introduce any additional components to power systems.

As compared with the fixed virtual inertia method, the frequency deadband-based control manages to further increase virtual inertia, leading to a 10% improvement on frequency nadir and a whopping 73% reduction on the energy required for inertia emulation at steady state. More importantly, the analysis also reveals that the dc-link voltage only changes when the maximum frequency deviation exceeds the preset frequency deadband. In this way, unnecessary voltage changes under normal system operating conditions can be avoided. Besides, even in the occurrence of voltage change, the scale of voltage swing under the frequency deadband-based method appears considerably smaller than that under the fixed virtual inertia control. Both the reduced frequency of voltage change and dwindled scale of voltage swing directly facilitate the preservation and even lifespan extension of dc-link capacitors as analyzed previously. As a reliability-critical component in power converter systems, a well-preserved dc-link capacitor contributes to enhancing the reliability of the entire system.

Note that the 10% improvement on frequency nadir is clearly not the best possible result. Recall the analysis on the correlation between frequency nadir and frequency deadband as demonstrated in Figure 4.4, the corresponding frequency deadband of the best frequency nadir improvement appears at somewhere between 0.12 Hz and 0.13 Hz assuming other parameters remain unchanged. Hence, it is possible to further improve frequency nadir by adjusting the value of frequency deadband. However, an issue with this approach is that it is difficult to either quantify the improvement on frequency nadir or determine the decisive parameters that contribute to this improvement. Unlike the equations quantifying the relationship between system inertia and frequency nadir illustrated in [17], the presence of frequency deadband introduces a layer of nonlinearity into the series of complicated mathematical equations. For instance, in order to obtain the value of breakthrough time t_{bt} , one needs to solve the inverse function of a polynomial which comprises the product of trigonometric and logarithmic functions as

highlighted in equation 4-13. Moreover, the values of frequency deadband are usually determined via trial and error in the existing literature. This means that the time-consuming simulations and experiments have to be conducted over and over again in order to inch towards a more accurate estimate. Besides, there might be more than one system parameters that contribute to the improvement of frequency nadir.

To address the abovementioned issues, a data-driven approach is introduced in the next chapter to estimate the value of frequency nadir while bypassing the calculations of the sophisticated mathematical relationships between the frequency nadir and different system parameters. Specifically, a forward artificial neural network is employed to act as a fast surrogate model of the GCCs, which is capable of establishing a functional relationship between the frequency nadir and different system parameters. Both the design principles and implementations of the data-driven solution will be elaborated in the next chapter.

Chapter 5

Capacitor Lifetime Extension via Optimization of Frequency Nadir

As discussed in the last chapter, an effective approach to increasing inertia for modern power systems is by using power converters to generate virtual inertia for frequency support. Existing literature has demonstrated its effectiveness in improving frequency regulation in terms of frequency nadir, especially when frequency deadband is included. However, the mathematical relationship between the virtual inertia and frequency nadir is already sophisticated by itself and might become even more complicated due to the nonlinearity introduced by the frequency deadband. Therefore, it is difficult to either quantify the improvement on frequency nadir or determine the decisive parameters that contribute to this improvement. To address this challenge, an artificial neural network (ANN) is employed to act as a computational surrogate model of the GCCs that can map the system design parameters (i.e. frequency deadband, dc-link voltage and etc.) into the variable that characterizes frequency regulation (i.e. frequency nadir). The ANN model is trained by 500 labeled data points and tested by 50 unlabeled ones. The output of ANN is compared against a detailed simulation model in MATLAB and achieves a less than 0.006% error. Finally, the results produced by ANN also show a fourteen times higher accuracy than mathematical calculation.

5.1 Background

As discussed in Chapter 4, power converters can be controlled to generate virtual inertia for frequency support without any modification of system hardware. Virtual inertia contributes to the improved frequency nadir, which is one of the most critical indices used to evaluate the effectiveness of frequency regulation. To further develop this idea, a frequency deadband-based virtual inertia control is introduced in Chapter 4 [103]. This method allows the increase of inertia in a shorter time duration by incorporating a frequency deadband into the virtual inertia controller, leading to an improved frequency nadir. However, an issue with this particular approach is that it is very difficult to determine the value of frequency deadband among other system parameters that lead to such an improvement on frequency nadir. Unlike the equations quantifying the relationship between the system inertia and frequency nadir illustrated in [17], the presence of frequency deadband introduces a layer of nonlinearity into this already complicated mathematical function. Moreover, the values of frequency deadband are mostly determined through trial and error in the existing literature. This means that the time-consuming simulations or experiments have to be conducted all over again in order to inch towards a more accurate estimate. Besides, there might be more than one system parameters that contribute to the improvement of frequency nadir.

In the light of these issues, a forward artificial neural network (ANN) based method is introduced in this chapter to estimate frequency nadir while bypassing the sophisticated mathematical relationship between system parameters and the frequency nadir. Specifically, ANN is deployed as a fast computational surrogate model of the GCCs, which is capable of establishing a functional relationship between the frequency nadir and certain system design parameters. The idea leverages on ANN's strong capability in generalizing nonlinear input and output relationship, hence generating the results with higher precision [104]. Meanwhile, it is worth to note that ANN requires a significantly lower amount of memory than most simulation models, which allows it to experiment with multiple design parameters as the input of the model [105]. In addition, the ANN model completes the estimating process significantly faster than running a detailed simulation model. The estimation of frequency nadir is repeated for a large number of system parameter variations to generate the training data for ANN. After training, the ANN model can generate an explicit functional relationship between the

system parameters and frequency nadir. Finally, given the ANN's nature in generalizing the nonlinear relationship between input and output data, it is capable of providing more accurate and reliable estimates of the frequency nadir than the conventional mathematical calculation approach.

Note that the power system configuration and frequency control framework that are utilized to generate training and testing data for the ANN model in MATLAB are completely the same as the ones elaborated in Chapter 4. For more detailed descriptions, please refer to subsections 4.2 and 4.3 as well as Figures 4.1 and 4.2.

5.2 Frequency Nadir Estimation via Artificial Neural Network-Based Approach

To overcome the difficulties in estimating the value of frequency nadir, this chapter introduces a forward ANN to operate as a more precise, flexible and faster surrogate model of the GCCs. According to [104], ANN is capable of adjusting the weights and biases of its multiple neurons to approximate any nonlinear relationship between input and output data with arbitrary precision. In addition, the excellent generalization capability allows ANN to precisely estimate the corresponding output results for the input examples that are not included in the training dataset [106]. Another advantage of ANN comes from the nonparametric nature of this model [107]. Specifically, ANN is able to learn the relationship between the input and output data on its own during the training process, thereby no prior knowledge of such a relationship is required. This is especially instrumental for the cases in which high dimensional input data or sophisticated nonlinear relationship is concerned. For this particular reason, an ANN-based model is adopted in this chapter to estimate frequency nadir from a set of system parameters including frequency deadband.

5.2.1 ANN Basics

In a nutshell, a forward ANN is composed by an input layer, one or multiple intermediate hidden layers and an output layer. For the input layer, there could be one or multiple dimensions of input data depending on the number of parameters used as input. Similarly, the output layer could also generate one or multi-dimensional data

dictated by the same rule. The intermediate hidden layers are usually considered the brain of the model that processes massive pieces of information in an effective and high-speed manner. Each hidden layer comprises a number of neurons that are responsible for processing the information passed by the neurons in the layer before itself.

At the input layer, x_i^n denotes the i th input parameters' n th example value, assuming there are m input examples and the number of parameters for each input example is I . At the hidden layer, each neuron takes the form of $a_j^{[l]}$, which stands for the j th neuron at the layer l . To calculate the numerical value of $a_j^{[l]}$, the output of all the neurons ($j = [1, \dots, N_{l-1}]$) from the last immediate layer $l-1$ is, at first, multiplied with weights $\omega_{i,j}^{[l]}$ derived from stochastic gradient descent. Then, a bias term $b_i^{[l]}$ ($i = [1, \dots, N_l]$) is added to the product to form $z_j^{[l]}$. Finally, $z_j^{[l]}$ is transformed into $a_j^{[l]}$ through an activation function σ . The most well-known activation functions include sigmoid, tanh, and ReLU [108]. The sigmoid function is frequently utilized for binary classification problems as its output is either 0 or 1 [109]. As a superior alternative to sigmoid, the output values of tanh are evenly distributed between -1 and 1, which centers the output curve at the origin. As a linear activation function, Rectified Linear Units (ReLU) outputs exactly the same value for the positive input data and 0 for the nonpositive input data ($f(x) = x$ for $x > 0$, $f(x) = 0$ otherwise) [110-112]. ReLU has shown higher flexibility in dealing with the output whose value exceeds 1. Considering the value of frequency nadir f_{r_nadir} is not limited to $[-1, 1]$ range, ReLU becomes the natural choice of activation function for the ANN model. The general expression of ReLU activation function is presented as

$$\sigma(z_j^{[l]}) = \begin{cases} 0, & \text{if } z_j^{[l]} \leq 0 \\ z_j^{[l]}, & \text{if } z_j^{[l]} > 0 \end{cases} \quad (5-1)$$

The operating processes of the ANN model are described as follows:

The input layer:

$$X = \begin{bmatrix} x_1^{[1]} & x_1^{[2]} & \dots & x_1^{[m]} \\ x_2^{[1]} & x_2^{[2]} & \dots & x_2^{[m]} \\ \dots & \dots & \dots & \dots \\ x_I^{[1]} & x_I^{[2]} & \dots & x_I^{[m]} \end{bmatrix} \quad (5-2)$$

where x_i^n ($i = [1, \dots, I]$) are the input of the n th example.

The hidden layer(s) l :

$$a_i^{[l]} = \sigma(z_i^{[l]}) = \sigma\left(\sum_{j=1}^{N_{l-1}} \omega_{i,j}^l a_j^{[l-1]} + b_i^l\right) \quad i = 1, \dots, N_l \quad (5-3)$$

Finally, the output layer:

$$y_i = \sigma(z_i^{[L]}) = \sigma\left(\sum_{j=1}^{N_{L-1}} \omega_i^L a_j^{[L-1]} + b_i^L\right) \quad i = 1, \dots, N_L \quad (5-4)$$

where y_i ($i = [1, \dots, N_l]$) denote the output of the i th example.

It is worth to note that both the weights $\omega_{i,j}^{[l]}$ and bias terms $b_i^{[l]}$ are playing critical roles in approximating the complicated and even nonlinear input-output relationship with arbitrary precision. The weights $\omega_{i,j}^{[l]}$ and bias terms $b_i^{[l]}$ in each neuron are tuned automatically through backpropagation algorithm at each epoch during the training process. The backpropagation algorithm is used to calculate the partial derivatives of the cost function C with respect to the weights $\omega_{i,j}^{[l]}$ and bias terms $b_i^{[l]}$ in the neural network [113-116]. The cost function C computes the error between the estimated results and the measured output data at each training iteration [117]. The signs of the partial derivatives determine the directions to which the value of the weights $\omega_{i,j}^{[l]}$ and bias terms $b_i^{[l]}$ should be calibrated. The calibration stops once $\partial C / \partial \omega_{i,j}^{[l]}$ and $\partial C / \partial b_i^{[l]}$ become zero, which indicates the values of weights $\omega_{i,j}^{[l]}$ and bias terms $b_i^{[l]}$ leading to the estimate with the lowest error are achieved.

5.2.2 ANN Structure

While the values of $\omega_{i,j}^{[l]}$ and $b_i^{[l]}$ can randomly initialized or even set to zeros at the beginning [118-120], the structure of ANN requires to be designed and engineered meticulously before the training starts. Specifically, the number of layers and the number of neurons in each layer are two important hyperparameters which directly affect how well the ANN fits the input and output data. If the number of layers or the number of neurons in each layer is set too low, the ANN may fail to capture the most insightful patterns existed in the data, hence underfitting the data and exhibiting huge bias in the estimated results. On the other hand, if the structure comes overly complicated with too many hidden layers and neurons, the ANN may end up overfitting the existing data and perform poorly on the newly acquired data. To solve the overfitting issue, there are half dozens of regularization techniques proposed by data scientists worldwide, which usually involves the design of another hyperparameter λ for regularization [121-123].

A simple way to overcome the overfitting issue is building a relatively simple ANN structure at first, and then gradually adding more neurons or hidden layers onto it by comparing the errors across training, validation and testing datasets. If the variances among the performance of the three datasets are low, then the ANN tends not to overfit on any particular dataset. In the meantime, it is worth to note that the rules of determining either the number of hidden layers or neurons have not been formally discussed in any existing literature. Hence, the values of these hyperparameters used are determined through repetitively evaluating the ANN's performance across training, validation and testing datasets.

The main structure of the ANN employed in this chapter is demonstrated in Figure 5.1. The input layer comprises four different input parameters including frequency deadband f_{dead} , maximum frequency deviation Δf_{r_max} , dc-link voltage v_{dc} , and dc-link capacitance C_{dc} . The rationale behind selecting these four parameters as the input is that they are considered having the highest impact on the value of virtual inertia [17], and thereby frequency nadir. Referring to equation 4-16, virtual inertia gain K_{wv} and inertia

Figure 5.1 Structure of the designed ANN model.

coefficient H_c appear in both the numerator (indirectly) and denominator of the equation. And the value of virtual inertia gain K_{wv} is essentially determined by frequency deadband f_{dead} , maximum frequency deviation f_{r_nadir} , and dc-link voltage v_{dc} according to equation 4-5. Whereas, the value of inertia coefficient H_c is directly related to dc-link voltage v_{dc} and dc-link capacitance C_{dc} as illustrated in equation 4-2. The output layer comprises one neuron, which is the only variable of the interest, frequency nadir f_{r_nadir} . Between the input and output layers, two intermediate hidden layers are empirically chosen to process and identify the patterns among the data. The three hidden layers consist of three, five and two neurons, respectively. This structure is determined by evaluating the ANN's performance across training, validation and testing datasets. It turns out that the ANN yields the lowest mean square errors (MSEs) when operating under this structure with the given datasets. The corresponding cost function is expressed as

$$C = \frac{1}{m} \sum_{i=1}^m \left\| \hat{y}_i - \sigma(z_i^{[L]}) \right\|^2 \quad (5-5)$$

where m is the total number of training examples. $\hat{y}_i$ stands for the output collected from simulations, i.e. expected output, and $\sigma(z_i^{[L]})$ is the vector of activations output from the network, i.e. estimated output. The values of MSEs generated from the same cost function C across training, validation, and testing datasets are strong and robust indicators of ANN's overall performance.

5.3 Design Workflow of the ANN-Based Approach

The complete workflow of the ANN-based design is demonstrated in Figure 5.2. The workflow is split into two stages including training and verification stages. The training stage is composed of two steps. The first step is collecting input data and their corresponding output data by running concurrent simulations in MATLAB for 500 times. The collected data are then preprocessed and organized in an excel file before being imported to the ANN model for training. The data preprocessing stage removes outliers and treats the missing values. By definition, an outlier is something that is outside of the expected response, thereby the existence of which will skew the distribution of the data and potential predictions. Specifically, when the outliers exist, the ANN model tends to overfit and is sensitive to these peculiar data points. Hence, it might predict values either higher or lower than the real future values [124-126]. In contrast, when the outliers are removed, the ANN predicts significantly more accurately with a generalized model that splits the distribution of the data fairly. By plotting the features against the output, it is simple to identify outliers and subsequently remove them.

On the other hand, a missing value is an entry in a column that has no assigned value. This could result from a variety of cases. For instance, a missing value might be the result of an error during the generation of the dataset. This could be a human error, i.e. failure to record the data in a timely manner, or machinery error, i.e. the simulation model fails to produce particular data point(s). Nevertheless, a missing value in certain cases might just mean that a ‘zero’ should be present. When missing values are identified in a dataset, there are generally two options to deal with it. One could delete the entire row or fill the missing entry with an imputed value [127-129]. Apparently, deleting the entire row would reduce the number of training samples available, hence affecting the training of the model. In contrast, filling the missing entry with the mean, median or even the mode of the column would be a better strategy, which preserves the integrity of training data and replaces the missing values with something close enough.

Figure 5.2 Flow diagram of the ANN based design for the estimation of frequency nadir.

Before the training step starts, a divide function is employed to randomly divide the data into training, validation and testing subsets. Out of the 500 data points, 70% of them are empirically assigned to the training set, and the remaining 30% are evenly allocated to validation and testing sets, respectively. The precision of the ANN model shows only negligible variations when operating under different division ratios. As part of the effort to speed up the training, the data across different features are normalized into the same value range through the normalization technique. The Min-Max normalization method is applied to the data of all four input features. Specifically, by

subtracting the minimum value of the feature from each value before having it divided by the difference of the maximum and minimum values of that very feature. As a result, the values of data in that particular feature all end up ranging from 0 to 1.

In addition to collecting and preprocessing the data for training, several other key features of the ANN model need to be defined prior to the start of training. For the designed ANN model, Levenberg-Marquardt backpropagation (LMB) is selected as the network training function to update weight and bias values at each epoch of training [130]. LMB is considered the fastest backpropagation algorithm in MATLAB deep learning toolbox and highly recommended as a supervised algorithm by the virtue of its excellent performance with nonlinear function fitting [131]. The major shortcoming of this algorithm is its higher requirement on memory than other similar algorithms. Fortunately, this would not be an issue for the design ANN model given its relatively small network size. Despite the maximum number of epochs to train is set at 1000, the training process usually ends after 40-80 epochs which limited by the maximum validation failures (set to 6 by default). The maximum validation failures prevent the ANN from underperforming on non-training data by stopping the training when the validation performance degrades for a certain number of consecutive epochs. This is one of the techniques that prevent the ANN from overfitting on the training dataset.

Finally, the trained ANN model is utilized to estimate the frequency nadir f_{r_nadir} from a set of unseen data at the verification stage. The estimated results are then compared against the output of the simulation model fed with the same set of input data. More details regarding the verification process and result analysis are elaborated in the next subsection.

5.4 Simulation Results and Discussion

As discussed previously, 500 data points including input features (f_{dead} , Δf_{r_max} , v_{dc} , and C_{dc}) and output (f_{r_nadir}) are generated by a detailed simulation model in MATLAB. Specifically, the frequency deadband f_{dead} is swept from 0 Hz to 0.04 Hz, 0.09 Hz, 0.14 Hz, and 0.19 Hz with a step of 0.01 Hz when the maximum frequency deviation Δf_{r_max} is set to 0.05 Hz, 0.1 Hz, 0.15 Hz, and 0.2 Hz, respectively. Meanwhile, dc-link capacitance C_{dc} is swept from 1 mF to 5 mF with a step of 1 mF. Whereas dc-link voltage v_{dc} is set to alternate between two different values, i.e. 380 V and 420 V, primarily due to its limited impact on the output. Therefore, the total number of data points required is 500.

The data are then randomly divided into training, validation and testing datasets by the ratio of 70%, 15% and 15% before being fed into the ANN model. The model attempts to generalize the relationship between the input and output data by adjusting the weights and biases of its hidden units at each epoch of training. As a simple way to test the capability of the ANN in generalizing the data, the validation dataset is randomly selected as a statistical representation of the entire dataset but has not been seen by the ANN model. The results of validation dataset are not only a robust indicator of the model's performance with unseen data but also suggest the potential adjustment on hyperparameters that might lead to even better performance. Note that the training and validation datasets have to be labelled properly so that metrics such as loss and accuracy can be obtained at each epoch of training or validation. The testing dataset, however, should not be labelled. This means no output is provided for this set of data, which is the same process the model would experience when deployed in the field. The performance of the designed ANN model is demonstrated in Figure 5.3. Clearly, the ANN achieves excellent performance in generalizing the data as the difference between the values of MSEs for training and validation datasets are insignificant. This indicates that the ANN model is free from overfitting issue. In particular, from the 35th epoch until the maximum validation failures are reached, the validation set scores even lower MSEs than the training set. Even though the results of the testing dataset are slightly worse than that of training and validation datasets, the ANN model is still considered effective and robust, given that the three curves change synchronously and their values of MSEs are mostly distributed within 10^{-3} to 10^{-4} range.

Figure 5.3 Performance of the designed ANN model.

The regression plots in Figures 5.4 – 5.6 reveal the relationship between the output of the network and targets for training, validation and testing datasets. The solid lines in each of these figures represent the best fit linear regression between the output and targets. If the training is perfect, the network output should be equal to the targets, but that rarely occurs in practice. The R -value is a statistical measure of how close the data are to the fitted regression line. A generalized equation to calculate R -value is expressed as

$$R = \sqrt{1 - \frac{\text{MSE of regression line}}{\text{MSE of the mean of the data}}} \quad (5-6)$$

It is generally interpreted as the percentage of variation that can be explained by the linear model. If $R = 1$, it indicates that the model explains all the variability of the output data around its mean. Whereas if R is close to 0, then there is no linear relationship between the output and targets. In this ANN model, the training data indicates an excellent fit, while the R values of validation and testing results are also very close to 1. The scatter plots can also pinpoint certain data points that fit poorly, which is instrumental in determining if these data represent extrapolation. Apparently, the

Figure 5.4 Regression plot of training dataset.

Figure 5.5 Regression plot of validation dataset.

regression plots suggest a relatively good fit between the output and targets.

To further demonstrate the effectiveness and accuracy of the designed ANN model in

Figure 5.6 Regression plot of testing dataset.

estimating frequency nadir f_{r_nadir} , 50 sets of unlabeled data that have not been seen by the ANN previously are fed into the network. The estimated value of frequency nadir f_{r_nadir} by the ANN model are then compared against the output of simulation model with the same set of input data as well as the results obtained from the mathematical calculations in equation 4-16. The result comparison is presented in Figure 5.7. Clearly, the output of ANN not only manifests the same trajectory as the results generated by the simulation model but also achieves an average error as low as 0.0055%. In contrast, the values of frequency nadir f_{r_nadir} calculated by equation 4-16 generally deviate from the simulation results by 0.078%. For certain input data points, the calculated values of frequency nadir f_{r_nadir} even exceed 50 Hz, which is almost impossible in practice. Therefore, the estimated results of the ANN model are not only more accurate than those derived from mathematical calculations but also more reliable in general as they tend not to deviate considerably from the simulation results. Finally, several key statistical parameters featuring the difference between simulation results and the two approaches are presented in Table 5-1. Note that the ANN model excels in all of the key statistics, which further confirms the superiority of this approach in estimating frequency nadir as compared to conventional mathematical calculations.

Figure 5.7 Comparison of frequency nadir estimated by different approaches.

5.5 Summary and Outlook

This chapter introduces an artificial neural network-based approach to estimating the value of improved frequency nadir f_{r_nadir} as a result of virtual inertia generated by the GCCs. The ANN is trained to operate as a surrogate model of the GCCs that maps four different system parameters features (f_{dead} , Δf_{r_max} , v_{dc} , and C_{dc}) into frequency nadir f_{r_nadir} . The ANN-based method has several advantages over the conventional mathematical approach and even simulation models in calculating the value of frequency nadir f_{r_nadir} :

- The ANN-based method is around fourteen times more accurate than mathematical calculations according to Table 5.1.
- The ANN-based method is found to be around four orders of magnitude faster than running a simulation model.
- The ANN-based method is capable of handling sophisticated, high-dimensional and even nonlinear relationship between the input and output data.

Given the relatively high speed of the ANN estimation, numerous system parameter

Table 5.1: Performance in estimating frequency nadir.

Approaches	Comparison with simulation results			
	Mean dev _a	Max dev _a	Min dev _a	MSE
ANN	0.0055%	0.0225%	0.0002%	0.0012%
Eq 4-16	0.0779%	0.4202%	0.0056%	0.5373%

a. Absolute value.

combinations can be tested in a very short period. This lays a solid ground to further investigate the impact of these system parameters on the design goals. Hence, an interesting direction of the future work could be identifying the combination of system parameters that leads to the best improvement on frequency nadir f_{r_nadir} .

Another important performance index when evaluating the influence of virtual inertia on frequency regulation is the rate of change of frequency (RoCoF). Mathematically, RoCoF can be obtained by differentiating equation 4-13 with respect to time:

$$\frac{d}{dt} f_{r_pu}(t) = -\frac{1}{2(H + K_{wv}H_c)} \begin{bmatrix} \zeta \omega_{ud} e^{-\zeta \omega_{ud} t} J \sin(\omega_d t + \theta) \\ e^{-\zeta \omega_{ud} t} J \omega_d \cos(\omega_d t + \theta) \end{bmatrix} \quad (5-7)$$

However, similar to the evaluation of the improvement of frequency nadir, it is difficult to map out the quantitative relationship between system parameters and RoCoF without solving sophisticated mathematical equations. Hence, this is another interesting problem which ANN could be applied to.

Note that despite the introduction of frequency deadband allows further improvement on frequency nadir, RoCoF, on the other hand, has inevitably worsened at the presence of frequency deadband, which is not desirable from frequency regulation point of view. Therefore, the third potential direction would be training an ANN model to identify the optimum values of frequency deadband and other system parameters that lead to the best-improved frequency nadir at the insignificant cost of RoCoF. For instance, a fitness function as below can be defined to conduct a grid search and identify the parameter combination(s),

$$f_{ANN} = (50 - f_{r_nadir})^2 + \omega (\text{RoCoF})^2 \quad (5-8)$$

where ω is the parameter for balancing the importance of the two terms. By experimenting with different values of ω , a Pareto front that characterizes the quantitative correlation between frequency nadir and RoCoF can be plotted in MATLAB. And the global minimum of the plot under different values of ω can be

located by using an exhaustive search algorithm. Once the global minimum is identified from the plot of the fitness function, the corresponding system parameters are revealed as well.

Following the discussion in Chapters 4 and 5, another interesting area to investigate would be quantifying the capacitor lifetime extended as a result of frequency deadband control. In Chapter 4, it was concluded that when a frequency deadband is embedded in the controller, the voltage only changes when the maximum frequency deviation exceeds the upper or lower limit of the preset frequency deadband value, i.e. $|f_{\text{dead}}| = 0.1$ Hz. Therefore, the unnecessary voltage changes during frequency events can be substantially avoided, which contributes to extending the lifespan of dc-link capacitors.

[19] has revealed that reduced voltage ripple did have a positive impact on preserving the lifetime of dc-link capacitors. However, like most other existing literatures, the quantitative correlations between the two remains untouched. In addition, the introduction of frequency deadband adds another layer of complexity in this quantitative analysis, where the ANN might contribute to untangling the correlation. Nevertheless, it is worth to investigating such correlation in order to further assess the benefit of frequency deadband control.

The next chapter concludes the thesis by highlighting the contributions and delineating a few possible directions for future work.

Chapter 6

Conclusions and Future Work

This chapter concludes the major contributions made by the thesis and delineates a few possible directions for future work. Throughout the thesis, efforts are dedicated to investigating various approaches to improving the reliability of power converter systems. In particular, different control-based active power decoupling methods are introduced to facilitate current and voltage ripple suppression, hence reducing the size of dc-link capacitors required to manage the ripple components. Thus, the more reliable F-Caps can replace E-Caps at the dc link of power converters. In addition, virtual inertia produced by GCCs under frequency deadband-based control also contributes to improving power converters' reliability in the context of frequency regulation. The introduction of frequency deadband further improves frequency nadir while reducing voltage ripples in the dc-link capacitors, which plays a tangible role in preserving the reliability of power converters. Finally, an ANN-based approach is introduced to estimate frequency nadir without incurring sophisticated mathematical calculations and identify the system parameters that contribute to such improvement.

6.1 Conclusions

The reliability of power converter systems has shown its tremendous value recently in the context of growing renewable energy generation. As a reliability-critical passive electrical component, dc-link capacitors have drawn particular attention among both academic researchers and industry practitioners worldwide. This is largely driven by the rising cost of unreliability at the later stage of development, increasingly demanding customers as well as the tightened international standard such as IEEE Standard 519-2014 on current ripples. F-Caps have been proven to be more reliable than the widely used E-Caps. However, the main roadblock that prevents the ubiquitous application of F-Caps is their high volume-to-capacitance ratio. For that particular reason, power converter systems typically have to lower their requirements on the size of the dc-link capacitance in order to employ the more reliable F-Caps. A large dc-link capacitor is typically required to buffer the instantaneous ripple power generated during dc-ac/ac-dc power conversion in single-phase power converter systems. Thus, a straightforward idea to lower the size of the dc-link capacitance required is by decoupling the ripple power from the fundamental power and having it compensated elsewhere.

To address the abovementioned issues, Chapter 3 introduces control-based active power decoupling methods for both one-stage and two-stage single-phase power converters to suppress ripple components in dc currents. The polluted dc currents can directly affect the efficiency, reliability and even the lifespan of the upstream renewable generators. For PV systems, the current ripple can compromise the efficiency of MPPT. Whereas for fuel cell systems, the presence of ripple current is one of the main root causes of the devices' shortened lifespan. In light of these potential damages, active power decoupling methods proposed in Chapter 3 consider two worst cases including nonlinear loads and background harmonics in weak grid conditions. Compared to the existing solutions, the proposed methods are capable of dealing with multiple low-frequency current ripple components without stacking PR controllers. Apart from successfully managing the low-frequency current ripples, the proposed control scheme enables suppression of current ripples at the switching frequency, which is commonly overlooked by the existing literature. More importantly, both active power decoupling methods introduced in Chapter 3 allow the single-phase systems to operate at significantly reduced dc-link capacitances. Hence, the more reliable F-Caps can be

employed to replace the conventional E-Caps at dc-link without concerning the volume issue. The substitution of F-Caps contributes to improving the reliability of power converter systems.

Another reliability-oriented issue the thesis attempts to address is related to frequency regulation when the grid is connected to renewable generators through fast-response power converters. Unlike synchronous generators, renewable generators cannot provide rotating inertia when connected to the grid through power converters. As a result, excessive grid frequency deviations are likely to occur in the event of generator tripping and/or load shedding, which poses a major threat to the reliability of the power system. Fortunately, by proportionally associating the dc-link voltage of GCCs with the grid frequency, the power converters can generate a fixed amount of virtual inertia for frequency support. Based on this idea, Chapter 4 introduces a frequency deadband-based frequency controller for GCCs to generate virtual inertia and support frequency regulation. As compared to the fixed virtual inertia in [17], the proposed control manages to further increase virtual inertia, leading to an improved frequency nadir and a reduction of energy required for inertia emulation. More importantly, it is revealed that the dc-link voltage only changes when the maximum frequency deviation exceeds the preset frequency deadband. Thus, unnecessary voltage changes under normal system operating conditions can be considerably avoided. The less frequent voltage changes contribute to preserving and extending the lifespan of dc-link capacitors, a reliability-critical electrical component in power converter systems.

To further explore the relationship between the improved frequency nadir and the values of underlying system parameters, Chapter 5 introduces an ANN-based approach to estimating the improved frequency nadir as a result of the virtual inertia generated by power converters. The ANN is trained to operate as a computational surrogate model of power converters that maps four critical system parameters into frequency nadir. Compared to the conventional mathematical modeling, the ANN-based method achieves fourteen times higher accuracy in calculating the value of frequency nadir with respect to four system parameters. More importantly, it is capable of dealing with complicated, high-dimensional and even nonlinear relationship between the input and output data. In addition, the proposed method is also found to be around four orders of magnitude faster than running a simulation model. Therefore, it is safe to conclude that

the ANN-based approach allows significantly faster and more accurate estimation of frequency nadir, which is one of the key indices when evaluating the performance of frequency regulation.

6.2 Future Work

On the basis of the work completed by the thesis, future efforts can be dedicated to improving the reliability of power converters considering several other critical characteristics of the system. For instance, the thermal-mechanical stress born by reliability-critical electrical components, i.e. semiconductor power devices, is one of the interesting areas to explore.

6.2.1 Active Thermal Control

According to Chapter 1, semiconductor power devices are considered to have an even higher impact on the reliability of power electronic systems than capacitors [6]. Hence, system reliability can be further improved by addressing the issues that affect the operating lifetime and performance of semiconductor power devices, such as thermal-mechanical stress. Insulated gate bipolar transistor (IGBT) and metal-oxide-semiconductor field-effect transistor (MOSFET), are two most widely used semiconductor power devices in power converter systems. However, a notable shortcoming of IGBT is its susceptibility to thermal-mechanical stress. This shortcoming could become a major threat to system reliability when power converters operate under load fluctuations [132].

As a matter of fact, the failures of semiconductor power devices can be mainly attributed to two different causes: high operating temperature and power cycling failure. For instance, when IGBTs/MOSFETs are continuously operating at a temperature that exceeds the highest allowed temperature for the junction, over-temperature failure would typically occur [133-134]. Similarly, the accumulated wearout resulted from the lifetime mechanical stress cycles could also lead to the failures of semiconductor power devices [135]. The correlation among the number of cycles to failure, mean operating temperature T_m , and ΔT_j , a variable that characterizes the thermal-mechanical stress level in IGBT, is demonstrated in Figure 6.1. According to the correlation, the number

Figure 6.1 The correlation among system reliability, operating temperature, and power cycling [132].

of cycles to failure decreases almost linearly as ΔT_j increases. The inverse proportional relationship suggests that higher thermal-mechanical stress prompts the failures of IGBTs. Thus, the reliability of semiconductor power devices could be severely undermined by thermal-mechanical stress.

To address this particular issue, active thermal control can be employed to regulate thermal-mechanical stress in power converter systems. Similar to the idea of power decoupling, by properly controlling the semiconductor power devices' thermal operating performance, the physical stress can be diverted elsewhere. In addition, if the semiconductor power devices can be controlled to operate at their highest allowed temperature continuously, there is a chance to further improve the system power conversion performance. Therefore, active thermal control is considered one of the most meaningful and valuable areas for future work.

6.2.2 Capacitor Condition Monitoring

The other interesting direction would be capacitor condition monitoring, an effective approach to estimating the health status of power electronic components. It is widely adopted in reliability-critical applications, such as electrical aircrafts and wind turbines [136]. As discussed previously, the reliability of dc-link capacitors is considered a critical aspect in control and design of modern power converters. The condition

monitoring of dc-link capacitors can provide a real-time technical guideline for predictive maintenance of those reliability-critical applications. Condition monitoring methodologies are broadly defined as the online measurement of certain electrical component, whereby appropriate actions would be taken should the value of that particular component drift away from its healthy range. Capacitance value is an electrical parameter that indicates the health status and degradation level of a capacitor [137].

Existing technologies to monitor the condition of capacitors rely heavily on hardware and/or voltage/current feedback signal injection [138-140]. Hence, these methods are considered expensive, invasive, inaccurate, and generally less flexible. And they are growing increasingly less favored by today's industries, especially those who are relentless pursuing reduced cost, high accuracy and flexibility.

Traditional methods for capacitance estimation can be classified by DC and AC techniques. The well-known DC techniques include CV (Cyclic Voltammetry) and GPCL (Galvanostatic Cycling with Potential Limitation) [141-142]. However, it is relatively difficult to obtain a purely capacitive current response signal using either of those techniques. In this case, we need to minimize and even remove the contributions of diffusion, ohmic or kinetic. On the other hand, with EIS (Electrochemical Impedance Spectroscopy), the most prominent AC technique, those contributions can be separated, hence achieving more accurate estimation. However, EIS requires the direct measurement of catalyst, and such measurement are realized in stationary method only for the applied potential. Thus, the values are in accordance with the CV capacitance at low scan rate. The accuracy of the abovementioned methods varies a lot depending on scan rate, diffusion phenomena, capacitor materials and system configurations.

These concerns led to the burgeoning interests in studying ANN-based capacitor estimation [136-137, 143-144]. The ANN-based method attempts to estimate the capacitance values based on the available input and output terminal information of the power converter. The input could be the single or multiple different variables that present certain intertwined or even nonlinear correlations to the capacitance value – the output in this case. A few examples of input reported in the literature are input current,

dc-link voltage ripple, dc-link voltage harmonics, load power variation, and etc [143-145].

To exploit the recent breakthroughs made in the field of computer vision, one research topic could be the estimation of capacitance value from thermal images by convolutional neural network (CNN) [146-148]. The thermal images of a capacitor in different capacitances have certain distinguishable features, i.e. unevenly distributed infrared radiation from the bottom to top, heat spots concentrated and/or dispersed in certain area, and changes in shape and size of the thermal image etc. Whereas, different capacitors of the same capacitance might share some, if not all, of those features. On the other hand, CNN is known for its exceptional capability of capturing subtle but distinguishable features in images.

The marriage of thermal imaging and computer vision is not a news and has been successfully applied in various industries. One example is that Apple Inc. attempted to use thermal imaging to improve the accuracy of subject detection when both the camera and the subjects are in motion [149]. Another example is using the thermal imaging techniques for lie detection. The idea is to detect the increase in the surface temperature of the areas around the nose a person when he/she lies. This is also called ‘Pinocchio effect’ [150]. In the field of electrical engineering, a machine learning-based thermal imaging approach is used to detect and measure the thermal anomalies of electrical components [151]. However, this technology has never been used to estimate and monitor dc-link capacitance, which is where the originality of this research sits.

To estimate and monitor the capacitance value in a non-invasive manner, a CNN could be employed to process the thermal images of dc-link capacitors and identify the highly abstract and compact feature representations from raw pixels of images. By learning the representative features in dc-link capacitor’s thermal images under different capacitance values, the CNN is able to generalize the image patterns and hence accurately estimate the corresponding capacitance values based solely on the input thermal images. Therefore, once a CNN is trained by large and random enough datasets of dc-link capacitor thermal images, it is able to estimate the capacitance value in an accurate and unbiased manner.

Since the thermal imaging technologies estimate capacitance based on the thermal characteristics manifested in the form of infrared radiation. Hence, once the neural network is trained by adequately large and diverse datasets, it is able to produce a higher accuracy than the current state of the art. Compared to the traditional methods, the CNN-based thermal imaging approach does not rely on the material, system configuration, scan rate among other variables/phenomena that dictate the accuracy of CV, GPCL and EIS. More importantly, the thermal images are taken through infrared cameras without disturbing the operations of the electrical component. Thus, this method is considered non-invasive and can potentially achieve real-time estimation. In terms of accuracy, CNN has huge potential to outperform traditional methods by a wide margin by leveraging the power of deep learning.

Nevertheless, the major challenge of this research is the availability of large and diverse enough thermal image datasets. In order to train a robust CNN, up to thousands of capacitor thermal images are required. Due to the pioneering nature of the research, the thermal image data might not be widely available. A few research institutions and corporations have studied the thermal images of electrical components, which could be the potential sources of data to begin with.

Publications

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Appendix

Flowchart of the proposed controller design for Case-I in Chapter 3

Flowchart of the proposed controller design for Case-II in Chapter 3

a. Proposed closed-loop control for output voltage regulation (DM operation).

b. Proposed closed-loop control for dc offset voltage regulation (CM operation).

c. Proposed closed-loop control for dc current ripple reduction (CM operation).