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Dielectric Quality of 3D Capacitor Embedded in Through-Silicon Via (TSV)

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Abstract— The concept of 3D capacitor embedded in TSV has been proposed recently to achieve ultrahigh capacitance density (up to 5,621.8 nF/mm²). This paper aims to investigate the effects of trench sidewall roughness and electrode deposition method on the dielectric quality of the 3D capacitor embedded in TSV. The test vehicles of 3D embedded capacitors were designed and fabricated with variations, which were the combinations of: (a) two options of trench sidewall roughness (30 and 290 nm) and (b) three options of electrode deposition methods (sputtering, ALD with air exposure, and ALD without air exposure). For test vehicles with different sidewall roughness but the same electrode deposition method, insignificant change of the leakage current density and dielectric strength can be observed in their *J-E* plots. Despite thicker dielectric layer, the leakage current density of sputtering test vehicles becomes higher than their ALD counterparts at bias greater than 3.5 MV/cm and dielectric strength ends up lower (~ 7.8 vs. >9 MV/cm). Therefore, sputtering is found not suitable for the fabrication of high performance 3D embedded capacitor. Besides, the elimination of air exposure during the process of ALD test vehicles helps suppress the leakage current density when the bias is greater than 4 MV/cm: e.g. it drops from 2.78×10^{-2} to 4.83×10^{-5} A/cm² at 8 MV/cm. Moreover, *C-V* characterization results suggest that the dielectric composition and the total amount of trapped charges become instable for the test vehicles with rough sidewall (290 nm), whereas they are consistent for the test vehicles with smooth sidewall (30 nm). These findings can provide valuable information for performance optimization and long-term reliability assessment of 3D capacitor embedded in TSV.

Keywords—3D IC; TSV; High- κ Dielectric; 3D embedded capacitor; capacitance density;

I. INTRODUCTION

The continuous shrinking of electronic components has been mostly achieved by down scaling of complementary metal-oxide-semiconductor (CMOS) transistors in integrated circuits (ICs). More recently, this approach is becoming technically challenging, as the size of a single CMOS transistor is reaching its physical limitation. This can be potentially a show stopper for further miniaturization and integration of electronic components.

Two alternative approaches have come to rescue. One approach is three-dimensional integrated circuit (3D IC) technology, and the other is the scaling of passive devices. In 3D ICs, different device layers are stacked vertically to realize smaller form factors, lower resistive-capacitive (RC) delay of interconnects and heterogeneous device integration [1]. As for scaling of passive devices, including resistors, capacitors and inductors, it is also impactful on the miniaturization of electronic components, because they usually occupy a much larger portion of the premium silicon

surface area, compared with active devices. Furthermore, the development of these two alternative approaches can benefit each other. One example is 3D capacitor embedded in through-silicon via (TSV) of 3D IC, recently proposed by the authors to achieve ultra-high capacitance [2]. Dedicated trenches for capacitors in Fig. 1(a) may not be necessary if they can be embedded in TSVs, as shown in Fig. 1(b). Therefore, the planar area occupied by trench capacitors is then greatly reduced, and the surface area can be freed up for the integration of other devices.

Figure 1. 3D embedded capacitors occupy less surface area: (a) conventional MIM trench capacitors with TSVs. (b) 3D embedded capacitors with TSVs [2].

So far, the dielectric quality of 3D embedded capacitors has not been discussed when different trench sidewall roughness and electrode deposition methods are applied during fabrication. Thus, this work aims to achieve the following goals:

- To fabricate test vehicles with variations for 3D capacitor embedded in TSV, including the combinations of: (a) two options of trench sidewall roughness (30 and 290 nm) and (b) three options of electrode deposition methods (sputtering, ALD with air exposure, and ALD without air exposure).

- To investigate the effects of the trench sidewall roughness and the electrode deposition methods on the dielectric quality of 3D capacitor embedded in TSV.

In this paper, the process flow of 3D capacitor embedded in TSV and the design of test vehicles are presented in Section II. Then, detailed physical and electrical characterization results are discussed in Section III. Lastly, the conclusion is given in Section IV.

II. EXPERIMENTAL

A. Process Flow

The detailed process flow of 3D embedded capacitor in TSV is illustrated in Fig. 2. A trench with diameter of 40 μm and depth of 60 μm deep was firstly formed on the substrate by deep reactive ion etching (DRIE), as shown in Fig. 2(b). Scallops on sidewalls are inevitable due to the cyclic nature of DRIE process. Two Bosch process recipes were developed to achieve different sidewall roughness, 30 and 290 nm peak-to-valley scallops, by fine tuning of the etching and passivation duty cycles: Then a 10 nm SiO_2 thin layer was grown in O_2 by rapid thermal oxidation (RTO) as an insulation layer between the substrate and the bottom electrode of 3D embedded capacitor, as shown in Fig. 2(c). In this experiment, three electrode deposition methods were also introduced to study their effects on the dielectric quality of 3D capacitor embedded in TSV, including sputtering, atomic layer deposition (ALD) with air exposure, and ALD without air exposure. All the dielectrics in between the electrodes were deposited with the same ALD condition, except that the thickness was 30 nm for the sputtering test vehicles and 10 nm for the other ALD test vehicles. Thus, the stacked layers were:

1. Sputtered 400 nm TiN/ALD 30 nm Al_2O_3 /Sputtered 400 nm TiN
2. ALD 50 nm TiN/ALD 10 nm Al_2O_3 /ALD 50 nm TiN (with air exposure)
3. ALD 50 nm TiN/ALD 10 nm Al_2O_3 /ALD 50 nm TiN (without air exposure)

3D embedded capacitor with sputtered electrodes (option1) has been reported in an earlier publication [3]. Sputtering provides partial coverage of electrodes on the trench sidewalls, thus limited surface area enhancement. The Al_2O_3 thickness in option 1 was set to be 30 nm, thicker than 10 nm Al_2O_3 in option 2 and 3, because sputtering might cause uniformity issues of the dielectric layer. In option 2 and 3, ALD was applied to achieve excellent step coverage of both top and the bottom electrodes of 3D embedded capacitors. The benefit of making integrated capacitors along the third dimension was therefore fully utilised. The difference in option 2 and option 3 lies in the air exposure of the bottom electrodes. In option 2, the test vehicles with TiN bottom electrodes were taken out from the ALD reactor chamber and exposed in air for 8 hours before further Al_2O_3 deposition, whereas in option 3, test vehicles were prepared in a single reactor for all three layers of ALD process, transferred internally between chambers without air

exposure. The oxidation of TiN layer at room temperature was observed and studied in [4], making it a critical variable for 10 nm thin Al_2O_3 in this experiment. However, for relatively thick 30 nm Al_2O_3 in sputtering test vehicles, the effect of bottom electrode oxidation is assumed to be negligible for the overall capacitor performance.

Figure 2. The process flow of 3D embedded capacitor in TSV.

After the deposition of MIM layers, standard TSV process steps should be carried out, including SiO_2 liner

deposition by plasma enhanced chemical vapor deposition (PECVD), Ta and Cu sputtering as diffusion barrier layer and seed layer, Cu electroplating and chemical-mechanical polishing (CMP), as illustrated in Fig. 2(e) to Fig. 2(g). Unfortunately, these processes were not available in our clean room for the time being. Thus, the TSV part was not completed in this work. And, it is assumed that the filling up of TSV has relatively small impact on the performance of 3D embedded capacitors. After that, the test vehicles were etched with patterned photoresists so that the top and bottom electrodes were defined for electrical characterization, as shown in Fig 2(h). Lastly, a 100 nm SiO₂ layer would have been deposited by PECVD as surface passivation layer, with Al pads formed on top of that as contact pads, if TSV processes were completed, as shown in Fig. 2(i) and Fig. 2(j).

In summary, the process flow of 3D embedded capacitors includes metal/insulator/metal layer deposition, standard TSV process and contact pad formation. After fabrication, the various test vehicles were summarized in Table I for easy reference. In this experiment, two options of trench sidewall roughness and three options of electrode process methods results in 6 types of test vehicles in total.

TABLE I. REFERENCE SYSTEM OF TEST VEHICLES

Name	Description
S1	trench with smooth sidewall (30 nm) electrode deposition (option 1)
R1	trench with rough sidewall (290 nm) electrode deposition (option 1)
S2	trench with smooth sidewall (30 nm) electrode deposition (option 2)
R2	trench with rough sidewall (290 nm) electrode deposition (option 2)
S3	trench with smooth sidewall (30 nm) electrode deposition (option 3)
R3	trench with rough sidewall (290 nm) electrode deposition (option 3)

B. Test Vehicle

The design of test vehicle in this work is the same as described in [2]. Figure 3(a) shows the contact window M1 of the bottom electrode and the contact window M2 of the top electrode. The top electrode, 400 μm long and 800 μm wide, contains 9 trenches. Thus, one test vehicle is a planar MIM capacitor with 9 units of 3D embedded capacitors. The planar capacitance is excluded when test vehicles with different sidewall roughness are compared. The probe tips were connected to both top and bottom electrodes for electrical characterization as illustrated in Fig. 3(b).

Figure 3. Design of test vehicles: (a) top view of contact windows M1 and M2. (b) cross-section view for test vehicles under electrical characterization.

III. RESULTS AND DISCUSSION

A. Physical Characterization

Figure 4. SEM images of a R2 test vehicle: (a) a top view of 9 trenches in the test vehicle. (b) zoom-in view of a single trench at a tilted angle.

Firstly, a R2 test vehicle was examined under scanning electron microscope (SEM) for physical characterization. Figure 4(a) shows a SEM image of 9 trenches in the test vehicles. Some artifacts are observed in the vicinity of the three trenches, which are probably photoresist residues. A zoom-in view of a single trench with a tilted angle is shown in Fig. 4(b). Scallop in the trench can be noticed developing along the direction into the substrate. And the top opening of the trench contains zig-zags on the

perimeter, leading to vertical straps on the sidewall of the trench after DRIE.

Then a slice piece was cut from the same sample by focused ion beam (FIB) and sent for sputtering with Pt for TEM analysis. In Fig. 5, multiple layer stacks can be differentiated from the TEM image. From left to right, these layers are considered to be Pt as TEM coating layer, TiN as top electrode layer, Al_2O_3 as high- κ dielectric layer, TiN as bottom electrode layer, SiO_2 as insulation layer and Si as substrate on the right most of the figure. Distinguishable TiN grains in both top and bottom electrode layers demonstrate successful ALD deposition of polycrystalline TiN, which suggests their good electrical conductivity. Moreover, the Al_2O_3 layer by ALD seems stays in amorphous state, suggesting good insulation properties.

Figure 5. TEM image of a R2 test vehicle. Multiple layers can be clearly differentiated from this image.

B. Electrical Characterization

Figure 6. J - E characterization results of all test vehicles: S1, R1, S2, R2, S3, and R3.

In this work, the research focus is to investigate the effect of trench sidewall roughness and electrode deposition

method on dielectric quality of 3D embedded capacitors. Thus, the results of extracted capacitance density and corresponding modeling work will not be discussed here, which can be found in [5]. All test vehicles from S1 to R3 were undertaken current-voltage (I - V) characterization with Keithley 4200scs probe station, because leakage current density and dielectric strength are good indicators of the dielectric quality of 3D embedded capacitors. After that, the I - V characterization results were normalized by the surface area and the dielectric thickness of test vehicles, so that current density-electric field (J - E) plots can be obtained for fair comparison of different test vehicles, as shown in Fig. 6.

At the first glance, one may notice that little difference can be observed from the leakage current densities of test vehicles with the same electrode deposition method, but different sidewall roughness. The dielectric strengths are also very close for each pair of test vehicles: (1) 7.7 vs. 7.9 MV/cm for S1 and R1, (2) 9.4 vs. 9.6 MV/cm for S2 and R2, (3) 9.7 vs. 9.9 MV/cm for S3 and R3. These results are not in agreement with those from previous publications [6], [7], in which higher leakage current densities were observed for deep trench capacitors or nanotubular capacitors implemented in the structures with higher surface roughness. One possible explanation of this discrepancy is the difference in aspect ratio. In those publications, their high aspect ratio of the structures (usually >25) could lead to non-ideal composition of the dielectric layers even if they were deposited conformally by ALD. But in this work, an aspect ratio of only 1.5 was chose for trenches with diameter of 40 μm and depth of 60 μm . It might enable better composition of ALD dielectric layers, thus little change in leakage current densities.

It is worth pointing out that the effect of electrode deposition method is impactful on the leakage current densities and the dielectric strengths. Figure 6 shows significantly lower leakage current densities of S1 and S2 at bias below 3.5 MV/cm due to the thicker dielectric layers, compared with those of S2, R2, S3, and R3: e.g. 2.92×10^{-9} vs. 1.17×10^{-7} A/cm² at 2.5 MV/cm². But their leakage current densities quickly become higher than the other test vehicles at bias greater than 3.5 MV/cm, despite their thicker dielectric layers, and their dielectric strength are lower than the others as reported above. Therefore, it can be concluded that sputtering, as an electrode deposition method, causes more dielectric quality degradation of 3D embedded capacitors than ALD method. Thus, it is not suitable for the fabrication of high performance 3D embedded capacitors. The leakage current densities of S3 and R3 overlap with those of S2 and R2, but are kept much lower at bias greater than 4.5 MV/cm: e.g. at 8 MV/cm, it drops from 2.78×10^{-2} to 4.83×10^{-5} A/cm². Thus, the leakage current densities can be greatly suppressed in high bias region (> 4.5 MV/cm) by the elimination of air exposure. In other words, 3D embedded capacitors should be processed and transferred between chambers within the same ALD reactor for MIM layer depositions.

Figure 7. C - V characterization of 3S and 3R samples.

Although J - E plots of the test vehicles do not imply that the dielectric quality suffer from higher sidewall roughness, some other perspectives can be obtained from capacitance-voltage (C - V) characterization. C - V results of S3 and R3 are shown in Fig. 7 as an example for analysis. These data were extracted from the test vehicles located at 5 different spots across the wafers and the testing condition was set to be bias from -5 V to +5 V at 100 kHz. The lines with black solid symbols represent 3S and 3R de-embedded test vehicles, lying in the lower part of Fig. 7. It shows higher capacitances for R3 test vehicles than those of S3 ones. This is because that higher sidewall roughness in R3 results in larger surface area of capacitors than their S3 counterparts. Besides, it can be seen in Fig. 7 that all C - V curves are not symmetric along the zero bias, shifted towards left by ~ 1.5 V. And C - V curves of R3 test vehicles do not align nicely as those of S3 ones. It is suspected that the trapped charges in the dielectric layer cause this shift.

Some quantitative results of were obtained from second order polynomial curve fittings:

$$C(V) = C_o(\alpha V^2 + \beta V + 1) \quad (1)$$

where C_o is the capacitance at zero bias, α is the quadratic voltage coefficient of capacitance (VCC), and β is the linear coefficient of capacitance. The results are tabulated in Table II: VCC- α was extracted to be $\sim 1.6 \times 10^3$ ppm/V² for and VCC- β to be $\sim 4.8 \times 10^3$ ppm/V for S3 test vehicles, whereas some obvious deviated values are found for both VCC- α and VCC- β of R3 test vehicles, like 2.00×10^3 ppm/V² and 2.99×10^3 ppm/V. The value of VCC- α is correlated with polarization condition of the dielectric layer, and VCC- β is determined by the amount of trapped charges in the dielectric layer [8], [9]. Therefore, these C - V characterization results suggest that the dielectric composition and the total amount of trapped charges in the dielectric layer become instable as trench sidewall roughness becomes higher. S2 and R2 test vehicles

demonstrate similar behaviours and the results are not repeated here. S1 and R1 test vehicles were not sent for C - V characterization, because sputtering method has been found not suitable for the fabrication of high performance 3D embedded capacitor, as discussed earlier. Thus, the effect of sidewall roughness on the dielectric quality of 3D embedded capacitor is revealed with C - V characterization in this experiment. These conclusions can be useful in the performance optimization and future assessment of long-term reliability of 3D embedded capacitors.

TABLE II. VOLTAGE COEFFICIENT OF TEST VEHICLES

Test Vehicle	VCC- α (ppm/V ²)	VCC- β (ppm/V)
S3	1.56×10^3	4.89×10^3
	1.56×10^3	4.99×10^3
	1.61×10^3	5.08×10^3
	1.72×10^3	4.27×10^3
	1.61×10^3	4.76×10^3
R3	1.51×10^3	5.55×10^3
	1.52×10^3	5.45×10^3
	1.75×10^3	3.89×10^3
	1.94×10^3	2.99×10^3
	2.00×10^3	3.32×10^3

IV. CONCLUSION

This paper demonstrates successful fabrication of test vehicles of 3D embedded capacitor with the following variations: (a) two options of trench sidewall roughness (30 and 290 nm) and (b) three options of electrode deposition methods (sputtering, ALD with air exposure, and ALD without air exposure). The test vehicles have been examined to show clearly differentiable layers in SEM and TEM analysis.

The dielectric quality of 3D embedded capacitor has been studied with both J - E and C - V electrical characterizations. For test vehicles with different sidewall roughness but the same electrode deposition method, little change of the leakage current densities and dielectric strengths can be observed in their J - E plots. Despite thicker Al_2O_3 layer, the leakage current densities of S1 and R1 become higher than the others at bias greater than 3.5 MV/cm. Sputtering is found not suitable for the fabrication of high performance 3D embedded capacitor, as it introduces more damage to the dielectric layer than ALD method. Besides, the elimination of air exposure helps suppress the leakage current density at bias greater than 4 MV/cm: e.g. it drops from 2.78×10^{-2} to 4.83×10^{-5} A/cm² at 8 MV/cm. Thus, it advisable for 3D embedded capacitors to be processed and transferred between chambers within the same ALD reactor for MIM layer depositions. Furthermore, further C - V characterization and VCC value extractions of ALD test vehicles suggest that dielectric composition and the total amount of trapped charges in the dielectric layer become instable as trench sidewall roughness becomes higher.

These conclusions drawn from both physical and electrical characterization results can provide valuable information for the performance optimization and future assessment of long-term reliability of 3D embedded capacitors.

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