Dielectric failure mechanisms in advanced Cu/low-k interconnect architecture

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**NANYANG
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UNIVERSITY**

**DIELECTRIC FAILURE MECHANISMS IN ADVANCED
CU/LOW-K INTERCONNECT ARCHITECTURE**

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

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School of Materials Science and Engineering

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TABLE OF CONTENTS

ACKNOWLEDGEMENT	i
TABLE OF CONTENTS	ii
LIST OF FIGURES	v
LIST OF TABLES	xv
ABSTRACT	xvi
CHAPTER 1: INTRODUCTION	1
1.1 Overview	1
1.2 Research Objectives	5
1.3 Scope of Thesis	5
1.4 Organization of Thesis	5
CHAPTER 2: LITERATURE REVIEW	7
2.1 Low- <i>k</i> Dielectric Candidates	7
2.2 Impact of Integration Process on Dielectric Reliability	10
2.2.1 Dielectric etch and plasma damage	10
2.2.2 Dielectric or metal liner barrier deposition	11
2.2.3 Chemical-mechanical polishing (CMP)	13
2.3 Reliability Issues of Cu/Low- <i>k</i> Interconnects	13
2.4 Leakage Current in Cu/Low- <i>k</i> Interconnects	15
2.4.1 Review of conduction mechanisms in dielectrics	15
2.4.2 Leakage conduction in Cu/low- <i>k</i> interconnects	19
2.5 Dielectric Breakdown Mechanisms and Models	21
2.5.1 Review of dielectric breakdown mechanisms	21
2.5.2 Dielectric breakdown models relevant to Cu/low- <i>k</i> interconnects	23
2.5.3 Importance of electric field in dielectric breakdown	33
2.6 Reliability Concepts and Modelling	35
CHAPTER 3: COMB STRUCTURE	39

3.1	Experimental Details	39
3.1.1	<i>Comb test structures</i>	40
3.1.2	<i>Electrical test setup.....</i>	41
3.1.3	<i>Failure analysis tools.....</i>	41
3.2	Statistical Analysis of Dielectric Breakdown in Comb Structures.....	42
3.3	Temperature Dependence of Breakdown Voltage	46
3.4	Type 1 and Type 2 Failure Mode Analysis	47
3.4.1	<i>Observable failures (Type 2)</i>	47
3.4.2	<i>Thermally-induced voltage alteration (TIVA) localization results.....</i>	50
3.4.3	<i>Non-observable failures localized by pulsed-TIVA (Type 1).....</i>	53
3.5	Failure Mechanism Prediction for Type 1 and 2 Failure Modes	57
CHAPTER 4: SINGLE LINE AND CORNER STRUCTURES.....		60
4.1	Experimental Details	60
4.1.1	<i>Description and motivation of the new test structures</i>	60
4.1.2	<i>Electrical characterization techniques</i>	62
4.1.3	<i>Four point bend adhesion test</i>	64
4.2	Electrical Characterization Results	66
4.2.1	<i>Leakage comparison between the new structures and comb structures....</i>	66
4.2.2	<i>Conduction mechanisms in single line and corner structures.....</i>	67
4.2.3	<i>Breakdown strength distribution</i>	69
4.2.4	<i>Time-dependent dielectric breakdown (TDDB) analysis.....</i>	70
4.3	Physical Failure Analysis	73
4.3.1	<i>Failure modes after voltage ramp</i>	73
4.3.2	<i>Failure modes after constant voltage stress</i>	78
4.4	Delamination-induced Breakdown Mechanism	81
4.4.1	<i>Driving forces of delamination</i>	81
4.4.2	<i>Leakage current investigation by electrostatic discharge (ESD) pulse.....</i>	86
4.4.3	<i>Proposed delamination-induced leakage mechanism prior to breakdown</i>	89
4.4.4	<i>Qualitative description of delamination-induced breakdown mechanism</i>	93
4.5	Mechanism of Ta Migration from the Anode Sidewall	94
4.5.1	<i>Electric field as the driving force of Ta migration</i>	94

4.5.2	<i>Thermodynamic and chemical reactivity considerations for Ta migration</i>	99
4.6	TDDDB Degradation Mechanisms in Single Line and Corner Structures	101
CHAPTER 5: STAND-ALONE COWP METAL CAP		104
5.1	Advantages of Stand-Alone CoWP Metal Capped Structures	104
5.2	Test Structures and Test Conditions	105
5.3	Electrical Characterization Results	107
5.3.1	<i>Leakage and conduction mechanisms</i>	107
5.3.2	<i>Breakdown strength performance in asymmetric comb structures</i>	109
5.3.3	<i>TDDDB lifetime performance in symmetric comb structures</i>	110
5.4	Physical Failure Analysis	114
5.5	TDDDB Degradation Mechanism with Stand-Alone CoWP Metal Cap	118
CHAPTER 6: CONCLUSIONS		123
6.1	Comb Structures and Its Failure Analysis Challenges	123
6.1.1	<i>Failure localization methods</i>	123
6.1.2	<i>Failure mechanisms in comb structures</i>	123
6.2	Dielectric Reliability in Single Line and Corner Structures	124
6.2.1	<i>Delamination-induced leakage and breakdown mechanism</i>	125
6.2.2	<i>Ta ionic drift and diffusion and its leakage contributions</i>	126
6.3	Improvements with Stand-Alone CoWP Metal Capped Structures	126
6.4	Research Thesis Contributions and Future Outlook	127
6.5	Recommendations for Future Work	129
BIBLIOGRAPHY		131

LIST OF FIGURES

Figure 1.1 Interconnect RC delay versus gate RC delay [1].	1
Figure 2.1 Structures of silica-based dielectrics which are doped with (a) low and (b) high fluorine concentrations. (c) Structure of the carbon-doped silica-based dielectric (SiOCH).	8
Figure 2.2 (a) Ladder structure of MSQ. (b) Cage structure (T_8 cube) of silsesquioxane-based dielectrics.	8
Figure 2.3 Chemical structures of organic polymers evaluated for low- k dielectrics. (a) Crosslinked polyphenylene (SiLK TM). (b) Fluorinated polyarylene ether (FLARE TM). (c) Benzocyclobutene (BCB).	9
Figure 2.4 Integration process challenges faced with introduction of low- k dielectrics [18].	10
Figure 2.5 Energy filtered-TEM (EFTEM) compositional profile of the microporous SiOC:H low- k dielectric indicating a 20 nm oxidized and carbon-depleted region [20, 21].	11
Figure 2.6 Impact of barrier integrity on breakdown field strength and leakage current in porous MSQ dielectric [20, 23].	12
Figure 2.7 Schematic of a dual-damascene structure illustrating several compelling reliability issues in Cu/low- k interconnects [30].	14
Figure 2.8 Energy band diagrams for (a) Schottky emission and (b) Poole-Frenkel emission with and without an applied electric field.	18
Figure 2.9 Dielectric breakdown process as a function of free energy for the reaction coordinates [68].	25
Figure 2.10 Cu-induced dielectric breakdown model in Cu interconnects. (a) Cross-section of an interconnect structure illustrating the Cu ionization and subsequent migration along the CMP interface with an applied field. (b)	

Energy band diagram depicting the formation of leakage pathway in the dielectric and Cu^+ ion accumulation at the cathode [29].....	30
Figure 2.11 Experimental data obtained from long term TDDB tests matches the $\sqrt{E}$ model [73].....	31
Figure 2.12 (a) Energy band diagram illustrating source of Poole-Frenkel emission before bias-temperature (BT) stress, (b) first stage after BT stress and (c) second stage after BT stress [91].	32
Figure 2.13 (a) Cracking at the low- k /capping barrier interface for low breakdown strength samples. (b) and (c) Cracking at the capping barrier for high breakdown strength samples.....	33
Figure 2.14 Electric field enhancement factors as a function of line-to-line spacing with different line edge roughness sizes [98].	35
Figure 3.1 Flow chart illustrating the sequence of failure analysis steps performed for comb structures.....	39
Figure 3.2 (a) Optical image of several comb structures on a die and (b) a schematic of the single comb structure with a line width/space of $0.18\ \mu\text{m}/0.18\ \mu\text{m}$ and a total test area of $10^{-3}\ \text{cm}^2$	40
Figure 3.3 Cross-section view of the comb structure.	40
Figure 3.4 Schematic diagram depicting the electrical setup for the voltage ramp test.	41
Figure 3.5 V_{BD} distributions obtained at 20°C , 100°C and 150°C	43
Figure 3.6 Logarithm scale of the proposed three distinct I-V leakage characteristics extracted from voltage ramp tests at 20°C	44
Figure 3.7 Breakdown voltage distributions for Type 1, Type 2 and Type 3 failure modes at (a) 20°C , (b) 100°C and (c) 150°C	45
Figure 3.8 Arrhenius plot which shows the temperature dependence of breakdown field strength for Type 1 and Type 2 failure modes.....	46

Figure 3.9 Burn marks observable under an optical microscope for Type 2 and 3 failure modes.....	48
Figure 3.10 SEM top view of (a) bulging and (b) sunken burn marks.	48
Figure 3.11 FIB/SEM cross-sections of the burn mark whereby complete destruction of Cu lines and its surrounding dielectrics are seen.....	48
Figure 3.12 Particle contamination as a possible cause to Type 1 failure mode.	49
Figure 3.13 (a) Frontside TIVA image of comb sample A at 66 mW laser power. (b) Pulsed-TIVA signal image at 66 mW laser power and pulsing frequency of 500 Hz. (c) Optical and pulsed-TIVA overlay image of comb sample A. (d) TIVA and pulsed-TIVA vertical electrical signal line profiles across failure site.....	52
Figure 3.14 (a) Frontside TIVA image of comb sample B at 66 mW laser power. (b) Pulsed-TIVA image at 66 mW laser power and pulsing frequency of 500 Hz. (c) Optical and pulsed-TIVA overlay image of comb sample B. (d) TIVA and pulsed-TIVA horizontal electrical signal line profiles across failure site.	53
Figure 3.15 Optical and pulsed-TIVA overlay image of comb sample A indicating the cross-sectioned sites.....	54
Figure 3.16 SEM cross-section images at (a) AA' displaying dielectric crack paths from Cu top corners and (b) at BB' illustrating Cu extrusion through the crack paths.....	55
Figure 3.17 (a) SEM and (b) TEM cross-section images performed at CC' illustrating dielectric breakdown of the dielectric cap and low- <i>k</i> dielectric. (c) STEM-EDX horizontal line profile across the exploded region, indicated by a dotted line, showing traces of Cu in between the Cu metal lines.	56
Figure 3.18 TEM cross-section for a comb sample which exhibits a combination of dielectric stack burn and dielectric cracking through the Cu top corners.....	57

Figure 4.1 Novel test structures named as (a) S1 for single line structures and (b) S2 for corner structures. Note that the dimensions given are in microns.....	61
Figure 4.2 SEM layout of (a) S1 and (b) S2 test structures after fabrication.	61
Figure 4.3 TEM cross-section image of the novel test structure illustrating the SiC(N) capping layer, USG buried capping layer and SiOCH low- <i>k</i> dielectric.	62
Figure 4.4 (a) Electrical circuit for the Human Body Model (HBM) electrostatic discharge (ESD) pulse and (b) a schematic setup of the ESD and V-ramp tests.....	63
Figure 4.5 HBM ESD waveform output at the (a) zapper and (b) at the probe tips with an applied pulse voltage of 250 V.	64
Figure 4.6 Four point bend configuration illustrating the load application on the multi-layer thin films sandwiched between two elastic Si substrates of same thickness, $h = h_1 = h_2$	65
Figure 4.7 Thin film stacks for four point bend adhesion test with the interface of interest highlighted. (a) SiOCH/USG, (b) USG/SiC(N), (c) SiC(N)/SiOCH and (d) Cu/SiC(N).....	65
Figure 4.8 Interconnect leakage currents measured at room temperature for comb, S1 and S2 structures.	66
Figure 4.9 (a) Schottky emission observed in comb structures. (b) Plot of $\ln(I)-\ln(E)$ yielding a slope of almost 1, indicating Ohmic conduction at low electric fields.	67
Figure 4.10 Three distinct I-V leakage characteristics observed for (a) S1 and (b) S2 structures.....	68
Figure 4.11 (a) & (b) Ohmic conduction at low electric fields and (c) & (d) Poole-Frenkel emission at high electric fields deduced for S1 and S2 structures, respectively.	68

Figure 4.12 Weibull plots of the breakdown voltage conducted at 20°C, 50°C and 100°C for (a) S1 and (b) S2 structures.....	69
Figure 4.13 Arrhenius plot which shows the temperature dependence of breakdown field strength for comb, S1 and S2 test structures.	70
Figure 4.14 General TDDDB leakage current curves for comb, S1 and S2 structures.	71
Figure 4.15 Weibull plot of times-to-failure for comb, S1 and S2 structures stressed at 20°C and 150°C.	71
Figure 4.16 (a) Arrhenius plot of time-to-failure at 63.2%, $F(t_{63.2})$, at 3.33 MV/cm and (b) field dependence at 100°C for comb, S1 and S2 structures.....	72
Figure 4.17 (a) Schematic diagram of S1 indicating locations of cross-sections performed at the horizontal (H) and vertical (V) directions. TEM images of failure mode II in S1 structures after voltage ramp, at the (b) planar, (c) horizontal and (d) vertical directions.	73
Figure 4.18 (a) Schematic diagram of S2 indicating locations of cross-sections performed at the horizontal (H) and vertical (V1 and V2) directions. TEM images of failure mode II in S2 structures after voltage ramp, at the (b) horizontal, (c) vertical V1 and (d) vertical V2 directions.	74
Figure 4.19 (a) The delamination extends to a proportion of the anode terminal with a length of about 1 μm in S1 structure. (b) The delamination in S2 structure extends all the way to the end of anode terminal with a length of about 1.9 μm	75
Figure 4.20 Ta migration (indicated by the arrows) was observed for failure mode III in both the (a) horizontal and (b) vertical directions of S1, apart from the delamination. (c) STEM-EDX line profile along the dotted line shown in figure (b), illustrating Ta migration into the SiOCH low- k dielectric.	76

- Figure 4.21 (a) Discontinuities observed throughout the Ta sidewall barrier due to Ta migration into the SiOCH low- k dielectric. (b) Broken Ta barrier as indicated by the arrows which could be caused by stress generated from thermal expansion mismatch of the various materials at the site..... 77
- Figure 4.22 Ta migration (indicated by the arrows) was observed for failure mode III in the (a) horizontal and (b) vertical directions for S2, apart from the delamination. (c) STEM-EDX line profile along dotted line shown in figure (b), illustrating Ta migration into the SiOCH low- k dielectric..... 77
- Figure 4.23 A sub-surface catastrophic thermal dielectric breakdown after TDDB in S1 structures..... 78
- Figure 4.24 (a) TEM image displaying the Cu particles observed in the low- k dielectric and near the CMP surface after constant voltage stress at 2.33 MV/cm and 20°C. (b) EDX spectrum at position 1 whereby the Cu-K peaks at 8 keV are signals from the Cu grid used and EDX spectrum at position 2 which confirms the presence of Cu in the low- k dielectric due to the existence of Cu-L peaks at 0.93 keV. 79
- Figure 4.25 (a) TDDB failure mode after the abrupt current jump whereby Cu diffusion was seen along a delaminated SiC(N)/SiOCH interface at the anode terminal. Cu-L EDX profile is shown in the inset. (b) A magnification of the TEM image which shows the Cu particles along the delaminated interface. 80
- Figure 4.26 Soft breakdown TDDB failure mode whereby Ta migration into the SiOCH low- k dielectric was seen in addition to the Cu diffusion near the delaminated SiC(N)/SiOCH interface, at the anode terminal, as observed in (a) S1 and (b) S2 structures. 81
- Figure 4.27 Structural damage in the SiC(N) capping layer observed above the Cu anode terminal..... 81

Figure 4.28 Load-displacement trends obtained after four point bend test for the four main interfaces in an interconnect structure. The circled points are loads considered in the calculation of critical strain energy release rate.	82
Figure 4.29 Interfacial adhesion energies of the four main interfaces in the interconnect measured by four point bend adhesion test.....	83
Figure 4.30 Top down schematic of the extent of delamination at SiC(N)/SiOCH interface (shaded) summarized from physical analyses for (a) S1 and (b) S2 structures.	84
Figure 4.31 Electric field simulation of (a) S1 and (b) S2 structures, illustrating electric field enhancements at the end of line and corners.	86
Figure 4.32 Delamination occurred at the (a) Cu anode terminal after +250 V and 6 ESD pulses were applied to the anode while it occurred at the (b) Cu cathode terminal after -250 V and 6 ESD pulses was applied to the anode.....	87
Figure 4.33 Varying extent of delamination or failure severity after (a) 2 ESD pulses, (b) 6 ESD pulses and (c) 8 ESD pulses at the Cu anode terminal after a +250 V was applied.	87
Figure 4.34 (a) Leakage current measured at the anode and (b) absolute leakage current at the cathode with varying number of positive ESD pulses.	88
Figure 4.35 Leakage current at the anode terminal plotted on a linear scale which emphasizes the negative current at $V < 25$ V after +250 V ESD pulses.	89
Figure 4.36 Electric field vector distribution for 0.30 μm metal spacing after 100 V stress.	90
Figure 4.37 Band diagrams depicting the trapping of electrons at the positively charged traps at the delaminated site (at low electric fields) and detrapping of electrons through Pool-Frenkel emission at higher electric fields.....	91

Figure 4.38 (a) Band diagram and (b) schematic diagram of the proposed current leakage path leading to dielectric breakdown in the Cu/low-k interconnect when an interfacial delamination is present.	92
Figure 4.39 Top down schematic of Ta migration (cross-hatched) summarized from physical analyses for (a) S1 and (b) S2 and corresponding electric field distribution simulated for (c) S1 and (d) S2 structures.	95
Figure 4.40 Electric field simulation at the cross-section of the interconnect system, illustrating higher electric fields at the upper and lower corners of the Cu trench.	95
Figure 4.41 Leakage characteristics associated to Ta migration into the SiOCH low- <i>k</i> dielectric for (a) S1 and (b) S2 structures.	97
Figure 4.42 (a) Leakage increase as a result of an increased electron injection from the cathode due to potential lowering. (b) Leakage saturation due to neutralization of Ta ions and Ta oxide formation.	97
Figure 4.43 Temperature dependence of the electric field at which the leakage starts to increase.	98
Figure 5.1 (a) Top view schematic diagram of the asymmetric comb structure whereby the lines with vias are represented by the dotted lines. (b) TEM cross-sections of the structure with conventional SiN dielectric cap and (c) CoWP metal cap.	106
Figure 5.2 (a) SEM top view layout of the symmetric comb structure describing the locations of vertical and horizontal spacing. (b) Schematic diagram of the cross-sections illustrating Cu interconnects with conventional SiN dielectric cap and (c) CoWP metal cap.	106

Figure 5.3 I-V leakage characteristics for interconnect structures with SiN, 20 nm-thick CoWP and 40 nm-thick CoWP cap stressed at 100°C for (a) asymmetric (0.14 μm spacing) and (b) symmetric (0.28 μm spacing) comb structures.....	107
Figure 5.4 (a) Schottky emission and (b) Poole-Frenkel emission in SiN-capped asymmetric comb structures with 0.14 μm metal spacing and stressed at 20°C.	109
Figure 5.5 Breakdown field strength of SiN-capped and CoWP-capped structures for 0.14 μm metal spacing and stressed at 20°C.	109
Figure 5.6 Effects of temperature on the breakdown field strength for SiN dielectric cap and CoWP metal cap at (a) 0.14 μm and (b) 0.18 μm metal spacing.	110
Figure 5.7 General TDDDB leakage current trends for interconnect structures with SiN dielectric cap, 20 nm-thick CoWP and 40 nm-thick CoWP metal caps.	111
Figure 5.8 Weibull plots of TDDDB times-to-failure, taken at failure criterion: 10 μA , for SiN and CoWP-capped structures with the following metal spacing and temperatures: (a) 0.28 μm , 150°C (b) 0.28 μm , 180°C (c) 0.30 μm , 150°C and (d) 0.30 μm , 180°C.	112
Figure 5.9 Arrhenius plot of times-to-failure at 63.2% for interconnect structures with SiN, 20 nm-thick CoWP and 40 nm-thick CoWP caps at an electric field of 4 MV/cm, for (a) 0.28 μm metal spacing and (b) 0.30 μm metal spacing.	113
Figure 5.10 (a) Optical image of the asymmetric structure after voltage ramp stress illustrating burn marks and (b) SEM top view of the burn marks after delayering.	114
Figure 5.11 Optical images of the burn marks observed after TDDDB stress in (a) SiN-capped and (b) 20 nm-thick CoWP-capped structures. The short lines drawn indicate cross-section sites.	114

Figure 5.12 SiN capping layer damage observed in (a) asymmetric structures after voltage ramp and (b) symmetric structures after TDDB stress, is the likely origin of the catastrophic breakdown in SiN-capped structures.....	115
Figure 5.13 Burn at the SiO ₂ /SiO ₂ interface and metallic diffusion along the interface for (a) 20 nm-thick CoWP and (b) 40 nm-thick CoWP-capped structures.....	115
Figure 5.14 Energy dispersive X-ray point analyses at (a) point 1 for 20 nm-thick CoWP and at (b) point 2 for 40 nm-thick CoWP-capped structures. The table in the inset shows the atomic percent of the elements detected.	116
Figure 5.15 (a) Burn near the SiO ₂ /SiO ₂ interface and Co and Cu diffusion at the Cu trench corners for 40 nm-thick CoWP-capped structures with early failure. (b) EDX spectrum of the region highlighted by the white circle, indicating more Co diffusion than Cu.....	117
Figure 5.16 EDX analyses conducted at the SiO ₂ /SiO ₂ interface with the atomic percent of elements tabulated respectively for 40 nm-thick CoWP samples that exhibit (a) long time-to-failure compared to (b) samples that exhibit early failure.....	117

LIST OF TABLES

Table 2.1 Summary of conduction mechanisms in dielectrics.	16
Table 2.2 Conduction mechanisms reported in the literature for carbon-doped silicon oxides.....	20
Table 3.1 Mean V_{BD} (μ) and corresponding standard deviation (σ) for failure types 1, 2 and 3.	46
Table 4.1 Weibull slope (β) obtained from constant voltage stress data.	72
Table 4.2 Standard thermodynamic properties of Ta, Al, Si and Cu oxides [125].....	99
Table 4.3 Leakage characteristics and failure modes observed in single line (S1) and corner structures (S2).....	102
Table 4.4 Voltage ramp parameters, TDDB parameters and failure modes/mechanisms for comb, S1 and S2 structures.....	103
Table 5.1 Constant voltage test temperatures used for the symmetric comb structures. .	107
Table 5.2 TDDB thermal activation energy for SiN, 20 nm-thick CoWP and 40 nm-thick CoWP-capped structures conducted at electric field of 4 MV/cm.	113
Table 5.3 Voltage ramp parameters, TDDB parameters and failure modes/mechanisms for SiN-capped and CoWP-capped structures.....	118
Table 6.1 Interconnect architecture impact on failure mechanisms in advanced Cu/low- k interconnects	128

ABSTRACT

Time-dependent dielectric breakdown (TDDB) reliability is increasingly becoming a critical reliability concern with the introduction of lower dielectric constant materials and shrinking of metal spacing in the back-end-of-line technology. Therefore, there is a need to investigate the factors causing the leakage and dielectric breakdown in advanced Cu/low- k interconnects and understand the failure mechanisms involved. In this research, the effects of interconnect layout and dielectric stack on the leakage current and dielectric breakdown were studied. Failure analysis of traditionally used comb structures is tedious, challenging and unpredictable due to its large test area compared to the failure analysis area. Thus, a pulsed and thermally-induced voltage alteration (pulsed-TIVA) failure localization technique was employed. Although, mechanical cracking followed by Cu extrusion through the SiC capping layer was observed, the catastrophic thermal dielectric breakdown initiating from the upper half of the Cu trench, leaves little evidence for failure analysis.

Therefore, single line (S1) and corner (S2) structures were introduced for efficient failure analysis and also to study the effects of interconnect layout. S1 and S2 test structures revealed delamination at the SiC(N) cap and SiOCH low- k dielectric interface, SiC(N) film degradation and Cu diffusion through the cap and along the delaminated region as factors causing the catastrophic breakdown. The delamination which is caused by bond breaking at weak adhesion interfaces is driven by a field-enhanced thermal process and catalyzed by leakage through the cap. Moreover, it resulted in a lower TDDB activation energy, E_a , (~ 0.20 eV) for S1 and S2 structures as compared to comb structures (0.44 eV) in which delamination was not observed. Despite the difference, the source of catastrophic breakdown is the same, which begins at the cap region. Another factor found, which mainly affects the leakage current, was Ta ionic drift and diffusion from the anode sidewall, which is due to electric field gradient and Ta's oxidation tendency.

Since the capping layer properties and its adjacent interface adhesion quality are the main causes of leakage and dielectric breakdown, the introduction of a stand-alone and self-aligned CoWP metal cap is promising. The elimination of the dissimilar interface between the cap and intra-metal dielectric (SiO_2 in this case) led to a lower leakage current and negligible Poole-Frenkel emission. Moreover, the breakdown strengths and times-to-failure of CoWP-capped structures were found to be comparable to SiN-capped structures if not enhanced. Interestingly, the E_a for CoWP (0.66 – 0.96 eV) were almost two times higher than that for SiN-capped structures (0.47 – 0.58 eV). Hence, the TDDB degradation mechanism for CoWP-capped structures is dominated by the intrinsic properties of SiO_2 due to the similarity of E_a obtained from intrinsic SiO_2 breakdown. In conclusion, interconnect layouts with enhanced electric fields (i.e. S1 and S2) can lead to delamination and thereby lower the E_a . Conversely, dielectric stack without a dielectric capping layer will result in a higher E_a and thus improved TDDB reliability.

CHAPTER 1: INTRODUCTION

1.1 Overview

The minimum feature size in integrated circuits (ICs) is continuously decreasing while the device density per chip increases to keep up with Moore's Law of doubling in the device's speed every 18 months. It is obvious that as the device shrinks, the transistor gate delay reduces and thus improving the device performance. In order to take advantage of the increased device speeds, more complex interconnect schemes involving multilayer metal wirings separated by inter-level dielectrics are required to connect the individual devices. Moreover, the interconnects have to shrink to smaller cross-sectional areas and packed closer to each other to accommodate the increase in device density. Consequently, both the interconnect line resistance and the intra-line capacitance will increase which lead to the increase in signal propagation delay, crosstalk noise and power dissipation of the interconnect. As a result, the interconnect RC delay becomes a limiting factor in performance of IC chips over the gate delay as illustrated in Figure 1.1.

Figure 1.1 Interconnect RC delay versus gate RC delay [1].

Therefore, copper (Cu) became the next suitable candidate replacing traditionally used aluminum (Al) metal interconnects due to its lower resistivity and better electromigration resistance than Al. However, the use of Cu poses several problems such as poor adhesion of Cu to most dielectrics and non-self limiting oxidation behaviour of Cu. Furthermore, Cu can easily diffuse through the silicon dioxide (SiO_2) and subsequently degrade the device. This is because Cu forms deep traps in the forbidden energy gap of Si as well as readily reacts with Si to form conductive Cu_3Si at temperature as low as 200° [2, 3].

Therefore, a liner barrier at the sidewalls and bottom of a Cu trench, as well as a cap barrier at the top of the Cu trench, is required to prevent Cu diffusion into the intra-metal dielectric (IMD) and inter-level dielectric (ILD). The liner barrier is also required to serve as an adhesion promoter to Cu as well as provide suitable texture to promote growth of Cu with a strong texture in the (111) direction. Good diffusion liner barriers should have nano-crystalline or amorphous microstructures. The liner barrier integrity also depends on its chemical or metallurgical reactivity with Cu and dielectric as well as its density. In general, the liner should not react with Cu or dielectric under the thermal, mechanical and electrical stresses encountered during processing or operating conditions. The liner should also be dense enough to eliminate fast diffusion paths which could arise from defects and pinholes. Examples of liner barriers that were most studied and integrated into present interconnect schemes are W-, Ti- and Ta-based binary and ternary alloys [4]. However, the selection of a suitable liner barrier system becomes more challenging when liner thickness reduces to a few nanometers in order to minimize its resistivity contributions to the Cu lines and when porous low- k dielectrics are introduced.

Apart from being a diffusion barrier, the cap layer must protect Cu from corrosion during subsequent patterning steps and act as an etch stop layer. A cap layer is typically a

dielectric which covers both the Cu line and IMD. Examples of dielectric cap layers that have been studied and integrated into the interconnect scheme are SiN, SiC, SiCO and SiCN. However, the dielectric cap layers have relatively weak chemical bonds with Cu, thereby enabling Cu migration at the Cu-cap interface. This in turn limits the maximum current density through the lines due to Cu electromigration. However, as seen in the International Technology Roadmap for Semiconductors (ITRS) roadmap, an increasing current density is essential to support ongoing trends to higher operation frequencies and power consumption. Besides, the dielectric cap layers increase the intra-line capacitance due to its higher dielectric constants compared to IMDs and thus limit the reduction of interconnect RC delay. Therefore, metal cap layers with better interfacial adhesion to Cu are viable candidates for 45 nm generations and beyond. Metal cap layers such as W, Cu_xSi and CoWP have shown improvements in electromigration lifetime [5-8] as well as reduction in the interconnect RC delay by 5% to 12% [9, 10].

The conventional SiO_2 dielectric also needs to be replaced by a lower dielectric constant material, defined as low- k dielectrics, to further meet the signal propagation requirements. The choices of low- k dielectrics are more open in contrast to the choices of metal interconnects. One of the first low- k dielectric used in the 0.13 μm technology node is fluorine-doped SiO_2 (FSG) with a dielectric constant of 3.9. In order to keep pace with the gate scaling beyond the 90 nm technology node, second generation low- k dielectrics were introduced. The low- k ($k < 3.0$) candidates include silica-based (chemical vapor deposited carbon-doped SiO_2) and silsesquioxane-based dielectrics (spin-on deposited hydrogen-silsesquioxane (HSQ) and methyl-silsesquioxane (MSQ)). Ultra low- k dielectrics ($k < 2.4$) such as organic polymers (eg. benzocyclobutene (BCB) and SiLK), porous dielectrics or air gaps are eventually needed for future technology nodes.

Low- k dielectrics have to be robust electrically, thermally and physically. Electrically, low- k dielectrics need to have low dielectric constant, low leakage current and high breakdown field strength. Moreover, the dielectrics need to have high thermal conductivity, low thermal coefficient of expansion (CTE) and high thermal stability. Physically, it has to be mechanically stable to withstand chemical mechanical polishing (CMP) processes and has low moisture absorption. The dielectric constant of low- k materials is lowered by optimization of molecular structure (i.e. by minimizing configurational and dipole polarizability), reduced density and incorporation of porosity into the dielectric structure [11]. However, both approaches degrade thermomechanical properties of the low- k dielectric which includes strength (i.e. hardness and stiffness), adhesion, thermal conductivity and coefficient of thermal expansion. Thus, extensive materials research has been done to improve these inferior properties of low- k dielectric for it to be successfully incorporated into the back-end-of-line interconnect.

The inferior thermomechanical properties of the low- k dielectrics has led to the concern of thermal-mechanical stability of interfaces amongst Cu metal, diffusion barriers and low- k dielectrics which results in line-to-line leakage currents. Other reliability concerns for Cu/low- k interconnect are time-dependent dielectric breakdown (TDDB) in Cu/low- k interconnects, stress migration and electromigration of Cu via and lines. Therefore, besides exploring and improving material properties of the low- k dielectric itself, the electrical properties of an integrated interconnect system needs to be evaluated as well since it will affect the performance of the device directly. Hence, this research work is focused on the leakage current and dielectric breakdown in advanced Cu/low- k interconnect systems to gain more insight on the factors contributing to the leakage and the dielectric breakdown failure mechanisms involved. The objectives and thesis scope are explicitly described in the subsequent sections.

1.2 Research Objectives

The principal objectives of this research are:

- To understand the failure mechanisms responsible for leakage and dielectric breakdown in various advanced Cu interconnect systems
- To investigate the effects of interconnect layout and dielectric stack (generally defined as interconnect architecture) on leakage mechanism, breakdown field strength, time-dependent dielectric breakdown as well as failure modes and mechanisms

1.3 Scope of Thesis

The low- k dielectrics used for the study of interconnect layout will be limited to carbon-doped SiO₂ with dielectric constant of 2.9 whereby the interconnect structures are processed using 0.13 μm technology node. For the dielectric stack studies, the IMD dielectric is chemical vapor deposited SiO₂ with dielectric constant of 3.9. Although this is not a low- k dielectric which is needed for 90 nm technology node and beyond, the metal-capped interconnect structures (CoWP in this case) is likely to be used in replace of the dielectric capping layer due to the requirements in further reducing the interconnect signal propagation.

1.4 Organization of Thesis

The thesis begins with an introduction on the research objectives and scope (Chapter 1), a brief but concise background and literature review (Chapter 2) followed by the main body of the report. The main body of the thesis is divided into three chapters in accordance to the interconnect architecture studied. Therefore, the experimental setup and analysis tools used, results and discussion will be presented in the corresponding chapters. It will be presented in the sequence described in the following paragraphs.

Chapter 3 will give a general picture of the present interconnect dielectric reliability test structure (primarily the comb-comb structure) and testing methodology (primarily voltage ramp). Constant voltage stress or in short TDDB stress on comb structures are used as a reference in the subsequent chapters. An improved failure localization technique is demonstrated apart from the standard failure analysis procedures performed. In spite of that, there are still challenges faced in the failure analysis and understanding of failure mechanisms in the conventional comb test structures.

Hence in Chapter 4, new test structures are proposed to overcome the failure analysis challenges and thus provide an understanding of the failure mechanisms that could occur in Cu/SiOCH interconnect systems. The new test structures also enable the effects of interconnect layout (terminated tips and cornered lines) to be studied which is lacking from the comb structures (which consists of only parallel lines).

The effects of capping layer (or dielectric stack) on TDDB reliability is presented in Chapter 5. CoWP metal cap is known to improve electromigration and also able to reduce the interconnect intra-line capacitance due to absence of a dielectric capping layer. Therefore, the TDDB reliability of interconnects with stand-alone CoWP metal cap is evaluated. Moreover, the leakage and TDDB degradation mechanisms for stand-alone CoWP metal capped structures are investigated and compared to conventional interconnect structures with dielectric capping layers. Last but not least, an overall summary of the thesis as well as recommendations for future work are discussed in Chapter 6.

CHAPTER 2: LITERATURE REVIEW

2.1 Low- k Dielectric Candidates

Traditionally, SiO_2 has been used as an IMD and ILD in the interconnect system. Since the interconnect delay started to dominate the circuit delay at 0.18 μm technology node and beyond, low- k dielectric materials were introduced. One of the first low- k dielectrics used in the 0.18 μm and 0.13 μm technology node was fluorine-doped SiO_2 (also called FSG or SiOF) due to its similar mechanical, chemical and thermal properties to SiO_2 . The addition of fluorine lowers the orientational polarization due to replacement of more polarizable silanol groups (Si-OH bonds) with less polarizable Si-F bonds as shown in Figure 2.1(a) [12, 13]. The dielectric constant can be further reduced by increasing the fluorine concentration, resulting in the destruction of the threefold ring and thus increasing the free volume of the silica structure as shown in Figure 2.1(b). However, a high concentration of fluorine (>10 at %) results in reaction with water which causes adhesion loss and metal corrosion. Thus, the lowest k value that can be obtained with fluorine doping is about $k = 3.6$.

In order to keep pace with the gate scaling beyond the 90 nm technology node, second generation low- k dielectrics were introduced. The low- k candidates include silica-based and silsesquioxane-based dielectrics. Examples of silica-based low- k dielectrics are fluorine-doped SiO_2 as mentioned in the previous paragraph and carbon-doped SiO_2 (also called organosilicate glass (OSG), SiOC or SiOCH). The dielectric constant of carbon-doped SiO_2 dielectrics is lowered by replacement of highly polarizable Si-O bonds with lower polarizable Si-C bonds. Similar to the fluorine-doped SiO_2 , the addition of these methyl groups led to an increase in free volume of the silica structure as shown in Figure 2.1(c). The most common plasma enhanced chemical vapor deposited (PECVD) OSG

materials in the market are the Black Diamond™ ($k < 3$: Applied Materials), Coral™ ($k = 2.85$: Novellus) and Aurora™ ($k = 2.9$: ASM).

Figure 2.1 Structures of silica-based dielectrics which are doped with (a) low and (b) high fluorine concentrations. (c) Structure of the carbon-doped silica-based dielectric (SiOCH).

Silsesquioxane-based (SSQ) dielectrics are organic-inorganic polymers with an empirical formula of $(R-SiO_{3/2})_n$ and are usually spin-on dielectrics. Referring to Figure 2.2, the ladder structure and cage structures of SSQ are illustrated. The chemical formula is derived from the sesquistoichiometry of oxygen bonded to silicon. The two main SSQ dielectrics that are used for microelectronic applications are the hydrogen-silsesquioxane (HSQ) and methyl-silsesquioxane (MSQ) in which $R = H$ and $R = CH_3$, respectively.

Figure 2.2 (a) Ladder structure of MSQ. (b) Cage structure (T_8 cube) of silsesquioxane-based dielectrics.

Besides silica-based dielectrics, organic polymers have also been evaluated. Typical examples are crosslinked polyphenylene (SiLKTM), fluorinated polyarylene ether (FLARETM) and benzocyclobutene (BCB) and are illustrated in Figure 2.3. Although carbon double bonds have higher polarizability (thus, higher dielectric constant) than single bonds, carbon double bonds (with larger bond energies) are introduced in order to increase the thermal stability of the polymer dielectric materials. So far, the low-*k* candidates described are constitutive porous materials [11]. This means that the final structure of the dielectric depends on the original, as-deposited arrangement of the molecules.

Figure 2.3 Chemical structures of organic polymers evaluated for low-*k* dielectrics. (a) Crosslinked polyphenylene (SiLKTM). (b) Fluorinated polyarylene ether (FLARETM). (c) Benzocyclobutene (BCB).

On the other hand, substitutive porous materials are dielectrics whereby certain parts of the original as-deposited structure are selectively removed to create pores. Pores have to be extrinsically introduced in order to meet the ITRS requirement for 45 nm technology node and beyond. Typically, the pores are created through thermal desorption of macromolecular porogens from a multiphase solid or through sol-gel process. Examples of substitutive porous dielectrics made from sol-gel process are aerogel ($k < 2.2$) [14] and

xerogel [15], which are basically porous silica-based dielectrics. Ultimately, to achieve the most idealistic interconnect system with the lowest intra-line capacitance is by introducing air gaps as the IMD dielectric [16, 17].

2.2 Impact of Integration Process on Dielectric Reliability

The slower than projected pace of low- k dielectrics introduction was one of the central issues highlighted in ITRS 2003. The delay in adopting low- k dielectric materials was mainly due to reliability and yield issues associated with integration of the low- k dielectrics into the dual damascene process. The integration process challenges of low- k dielectrics are summarized in Figure 2.4. A few important integration processes that affect the dielectric reliability are briefly highlighted in the following sub-sections.

Figure 2.4 Integration process challenges faced with introduction of low- k dielectrics [18].

2.2.1 Dielectric etch and plasma damage

Dual damascene dielectric patterning is generally used for Cu-based interconnects. There are basically two approaches to the dual damascene process and they are trench-first and via-first processes. The trench-first approach is usually not preferred due to difficulty in

lithography of the via after trench etching. However, via-first approach has issues with residues around the via (i.e. fencing) and over-etching of etch stop layer which were eventually solved by improved integration techniques [19].

Although patterning of SiO_2 and SiOC are conceptually the same, the high carbon content in SiOC makes etch and resist strip more difficult. This is because the oxygen plasmas used for resist removal (also called resist ashing) can oxidize the surface of SiOC and result in an increased effective dielectric constant and thus, intra-line capacitance due to carbon depletion at the sidewalls as shown in Figure 2.5 [20, 21]. The formation of the sidewall damage could be up to a total of 20 nm thick and it was shown to increase the electric field experienced by the undamaged SiOC low- k dielectric as compared to the dielectric without sidewall damage [22]. Porous materials are even more susceptible to the plasma modification because of the ease of diffusion of the reactive species through its porous network.

Figure 2.5 Energy filtered-TEM (EFTEM) compositional profile of the microporous SiOC:H low- k dielectric indicating a 20 nm oxidized and carbon-depleted region [20, 21].

2.2.2 Dielectric or metal liner barrier deposition

As mentioned previously, selection of a suitable liner barrier system becomes more challenging for future generations. In the context of process integration, it becomes more challenging to deposit a conformal and continuous barrier with no fast Cu diffusion paths

through the barrier. The impact of barrier integrity on breakdown and leakage in porous MSQ is illustrated in Figure 2.6 [20, 23]. It was shown that a poor sealing barrier (porous barrier) results in lower breakdown field strength and higher leakage current.

Nonetheless, the barrier integrity can be enhanced by improving the barrier deposition process or by modifying the integration scheme. For non-porous low- k dielectrics such as SiOC, Ar ion re-sputtering after TaN and Ta deposition is suggested to reduce the barrier thickness at the via bottom while improving the coverage at the sidewall [24, 25]. Moreover, the problem of Cu being re-sputtered onto the dielectric sidewall during sputter preclean (i.e. via opening) could be eliminated. On the other hand, for porous low- k dielectrics, a post etch porogen burn-out (PEBO) is suggested whereby pores are created after dielectric etch and ash [26]. This results in a continuous barrier due to the smooth dielectric sidewall as opposed to the conventional process sequence. Pore sealing by dielectric deposition or plasma treatment are also feasible. By implementing these pore sealing techniques, deposition of barrier onto the porous low- k dielectrics will be more uniform and thereby improving the breakdown strength and TDDB lifetime [27].

Figure 2.6 Impact of barrier integrity on breakdown field strength and leakage current in porous MSQ dielectric [20, 23].

2.2.3 Chemical-mechanical polishing (CMP)

Chemical-mechanical polishing is part of the dual damascene process. CMP is done after Cu electroplating, to remove the over-plated Cu and Ta-based barrier at the top surface until it reaches the low- k dielectric surface. Consequently, the low- k dielectric is exposed to chemical slurries with abrasive particles and oxidizing chemicals, which will induce mechanical and chemical damage on the surface of the low- k dielectrics. As a result, reliability issues such as Cu corrosion (Cu oxidation), Cu scratch and Cu or slurry residue arises, apart from the commonly observed Cu dishing and oxide erosion [28]. The Cu contamination after CMP process could lead to metal shorts or open circuit failures if a proper clean is not performed.

The surface of the low- k dielectric is normally treated with NH_3 or H_2 plasma treatment [29]. It was postulated that the hydrogen radicals generated by the NH_3 or H_2 plasma decreased the density of surface defects (dangling bonds) at the Cu and low- k dielectric surface as well as reduced the Cu oxides to Cu. Moreover, NH_3 plasma treatment results in Cu nitridation on the Cu surface, which prevents formation of Cu silicides and subsequently suppress the increase in line resistance. As lower k dielectric materials with pores are introduced, more stringent CMP conditions need to be implemented due to the weaker mechanical properties of the low- k dielectric.

2.3 Reliability Issues of Cu/Low- k Interconnects

As a consequence of poor thermomechanical properties of low- k dielectrics and resultant integration challenges, a range of reliability issues are anticipated. An overall picture of the reliability issues in Cu/low- k interconnects is summarized in Figure 2.7. To illustrate, there is an increase in leakage current and degradation in breakdown field strength as well as the risk of copper ion migration, delamination and moisture absorption. These

reliability issues contribute to TDDB performance of interconnects. In addition, the problem is exacerbated with interconnect scaling, whereby electric fields experience by the intra-metal dielectric increases and line edge roughness becomes important. On the other hand, Cu lines that have to accommodate higher current densities in future technology nodes face stress migration and electromigration issues.

Figure 2.7 Schematic of a dual-damascene structure illustrating several compelling reliability issues in Cu/low-*k* interconnects [30].

Early studies on Cu and its effects on the dielectric was focused on the drift and diffusion kinetics of mobile Cu ions into the bulk SiO₂ [31] and low-*k* dielectrics [32-35]. The effectiveness of the sidewall diffusion barriers (metal barriers) and the cap barriers (dielectric barriers) of preventing Cu diffusion into the dielectric were also addressed [36, 37]. Generally, electrical characterization for these metal-insulator-semiconductor (MIS) structures such as voltage ramp, bias-temperature stress (BTS) or TDDB, and capacitance-voltage (C-V) measurements were performed to evaluate the Cu ion migration and barrier integrity. As the fabrication of low-*k* dielectrics via the dual damascene process became viable, electrical characterization of the integrated interconnect structures with different stack materials is necessary. Therefore, a review on

the leakage current analysis and dielectric breakdown models relevant to Cu/low- k interconnects will be elaborated.

2.4 Leakage Current in Cu/Low- k Interconnects

Leakage between metal lines contributes to the static power of a device. Therefore, the total leakage from the transistor and interconnect during the off state must be as low as possible to minimize power consumption. Hence, there is a need to tackle the increased leakage current caused by the low- k dielectrics through the understanding of the causes of leakage and the leakage conduction mechanisms.

2.4.1 Review of conduction mechanisms in dielectrics

Central to understanding charge-induced damage in dielectrics are several conduction mechanisms such as ohmic or ionic conduction, Fowler-Nordheim (F-N) tunneling, Schottky emission, Poole-Frenkel (P-F) emission and space-charge-limited conduction. They are divided into low and high electric field conductivity as well as electrode-limited and bulk-limited conductivity. These conduction mechanisms will be described briefly but Schottky emission and P-F emission will be reviewed in depth as these are the two major conduction mechanisms reported in Cu/low- k interconnects. Table 2.1 summarizes the various conduction mechanisms aforementioned together with its equations.

Ohmic conduction occurs through thermally excited electrons hopping from one isolated state to the next. This conduction dominates at low fields and at moderate to high temperatures. Meanwhile, the diffusion of ions in a dielectric with assistance from an applied electric field is defined as ionic conduction. One possible source of the ions is from the ionic contamination imposed during wet chemical processes. On the other hand, F-N tunneling is commonly found in gate dielectrics but not likely in low- k dielectrics. F-

N tunneling only occurs if the dielectric is very thin (10 nm range), which means it occurs at high electric fields. It involves quantum mechanical tunneling of electrons from the metal through the triangular energy barrier into the conduction band of the dielectric.

Table 2.1 Summary of conduction mechanisms in dielectrics.

Conduction mechanism	J-E relationship	Additional notes
Schottky emission	$J = A^* T^2 \exp\left(\frac{\beta_s \sqrt{E} - \Phi_s}{k_B T}\right)$	$\beta_s = \sqrt{\frac{q^3}{4\pi\epsilon_o\epsilon_r}}$
Poole-Frenkel emission	$J = J_o \exp\left(\frac{\beta_{PF} \sqrt{E} - \Phi_{PF}}{k_B T}\right)$	$\beta_{PF} = \sqrt{\frac{q^3}{\pi\epsilon_o\epsilon_r}} ; J_o = \sigma_o E$
F-N tunneling	$J = E^2 \exp\left(-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E}\right)$	J = current density A* = Richardson-Dushman constant T = temperature in Kelvin
Space-charge-limited	$J = \frac{8\epsilon_o\epsilon_r\mu\theta V^2}{9d^3}$	E = electric field k _B = Boltzmann constant q = electron charge
Ohmic	$J = E \exp\left(-\frac{\Delta E_{ae}}{k_B T}\right)$	ε _o = permittivity of free space ε _r = relative permittivity Φ _(S, PF or B) = barrier height σ _o = low field conductivity
Ionic conduction (low field)	$J = \frac{E}{T} \exp\left(-\frac{\Delta E_{ai}}{k_B T}\right)$	m* = effective electron mass ħ = Planck’s constant μ = free carrier mobility θ = ratio of free charge to sum of free and trapped charge V = applied voltage d = dielectric thickness ΔE _(ae or ai) = activation energy

Schottky emission is a thermal emission of electrons from a metal electrode into the conduction band of a dielectric, with an image force correction taken into account. The energy band diagram at the metal-dielectric contact with and without an applied electric

field is shown in Figure 2.8(a) while the current density equation is described in equation 2.1.

$$J = A^* T^2 \exp \left[- \frac{q \left(\Phi_s - \sqrt{qE / 4\pi\epsilon_o\epsilon_r} \right)}{k_B T} \right] \dots\dots\dots (2.1)$$

The constant A^* is the Richardson-Dushman constant of thermionic emission given by $A^* = 4\pi q m^* k_B^2 / h^3$; Φ_s is the Schottky barrier height at the metal-dielectric contact; E is the applied electric field, ϵ_o is the permittivity of free space; ϵ_r is the high frequency dielectric constant of the dielectric (i.e. $\epsilon_r = n^2$) and k_B is the Boltzmann constant. Since the emission of electrons from the metal into the dielectric depends on the barrier height at the metal-dielectric interface, thus Schottky emission is an electrode-limited conduction.

On the other hand, P-F emission is a bulk-limited conduction which dominates at high electric fields and high temperatures. The P-F effect is the lowering of a Coulombic potential barrier when an electric field is applied, which results in thermal emission of charge carriers from the Coulombic traps that are in the bulk of a dielectric or semiconductor. Figure 2.8(b) depicts the energy band diagram of a Coulombic trap with and without an applied electric field. The traps must be neutral when filled with an electron and positively charged when electron is emitted, making it a Coulombic trap. The classical P-F equation which was introduced is shown in equation 2.2 [38].

$$J = q\mu n E \exp \left[- \frac{q \left(\Phi_{PF} - \sqrt{qE / \pi\epsilon_o\epsilon_r} \right)}{k_B T} \right] \dots\dots\dots (2.2)$$

The electrical conductivity given by $\sigma_o = q\mu n$ is dependent on the carrier mobility and concentration of free electrons in the conduction band, while Φ_{PF} is the ionization

potential which is the amount of energy required for the trapped electron to escape the influence of the positive nucleus at the trapping center when no field is applied.

Figure 2.8 Energy band diagrams for (a) Schottky emission and (b) Poole-Frenkel emission with and without an applied electric field.

The P-F model was further developed to explain the anomalous P-F effect by considering deep donor levels and shallow neutral traps [39]. It describes the case whereby a bulk-limited conduction is observed in the dielectric but the conductivity is field-dependent in the manner similar to the Schottky emission. In 1968, the model is further extended to include the conductivity dependence on the relative densities of acceptor and donor sites [40]. Therefore, the extended P-F equation shown in equation 2.3 includes an acceptor compensation factor, ξ , which can range between 1 to 2, depending on the position of Fermi level (or amount of acceptor compensation). The P-F relationship which was first proposed by Frenkel in 1938 and is still commonly used now, assumes an acceptor compensation factor of 1 ($\xi = 1$). This applies to the case when the density of acceptor and donor sites are high compared to the free electrons in the conduction band (i.e. $N_a \gg n$, $N_d \gg n$). Meanwhile, $\xi = 2$ when the density of acceptor sites is small compared to the density of donor sites and free electrons (i.e. $N_d \gg N_a$, $n \gg N_a$).

$$J = q\mu \frac{N_c(N_d - N_a)}{2N_a} E \exp \left[- \frac{q(\Phi_{PF} - \sqrt{qE / \pi \epsilon_o \epsilon_r})}{\xi k_B T} \right] \dots\dots\dots (2.3)$$

The electrical conductivity term now includes the effective density of states in the conduction band, N_c , concentration of donor sites, N_d and concentration of acceptor sites, N_a .

The conduction mechanisms can be deduced by fitting the current-voltage (I-V) curves obtained from voltage ramp tests to the most relevant conduction mechanism relationships. Since both Schottky and P-F emissions depend on the exponential of the square root electric field, they are differentiated through the fitted k value. The conduction mechanism that yields a k value close to the dielectric constants of the dielectrics used in the interconnect is the correct conduction mechanism. Apart from the Schottky and P-F emissions that were reported in low- k dielectrics, space-charge-limited conduction was found in an organic low- k dielectric, BCB [41] as well as methylsilsesquiazane (MSZ) low- k dielectric [42]. This temperature independent space-charge-limited conduction is described as the retardation of the incoming charge carriers due to the presence of trapped carriers in the dielectric [43].

2.4.2 Leakage conduction in Cu/low- k interconnects

Some of the reported conduction mechanisms in specific electric field regions for carbon-doped SiO₂ are listed in Table 2.2. It is important to note that there may be more than one conduction mechanism occurring in the same field region and that the effects of temperature on the leakage current is necessary to give more information on the type of conduction mechanism [44]. Thus, the deduced conduction mechanisms that were reported are assumed to be the more dominant conduction mechanism occurring at that field region.

Besides determining the leakage conduction mechanisms in a dielectric, it is imperative to identify the dominant leakage paths. The possible leakage paths in an interconnect system are the bulk of the intra-metal low- k dielectric, the bulk dielectric barrier (i.e. the cap layer) and the interfaces [45]. It is evident that the most probable leakage pathway is at the interface between the low- k dielectric and cap barrier which is the CMP surface [29, 41]. This is due to the mechanical damage imposed on the dielectric surface caused by the slurry used and the downward force applied during the CMP, which results in interfacial defects such as dangling bonds and traps. In addition, the cap barrier plays a significant role in contributing to the failure in an interconnect because the amount of leakage current and the dominating conduction mechanism change with the cap barrier material [46-48]. Moreover, the change in cap barrier material will inadvertently affect the interface bonding quality and the intrinsic film stress as well as the stress distribution in the cap film with respect to its surrounding [49].

Table 2.2 Conduction mechanisms reported in the literature for carbon-doped silicon oxides.

Reference no.	Bulk Dielectric Constant, k	Conduction Mechanisms	Structure Type/ Cap Layer/ Diffusion Barrier
[50]	2.87	1. Ohmic ($<0.2\text{MV/cm}$) 2. Schottky ($0.2\text{-}1.4\text{MV/cm}$) 3. Poole-Frenkel ($>1.4\text{MV/cm}$) 4. F-N tunneling ($1.7\text{-}2.08\text{MV/cm}$)	<ul style="list-style-type: none"> ▪ Comb-comb ▪ 50nm SiC ▪ 25nm Ta
[51]	3.00	Poole-Frenkel ($>1.4\text{MV/cm}$)	<ul style="list-style-type: none"> ▪ Comb-serpentine ▪ 50nm SiC(N) ▪ 15nm Ta/TaN
[52]	3.00	1. Ionic ($<0.25\text{MV/cm}$) 2. Ohmic ($0.25\text{-}0.5\text{MV/cm}$) 3. Poole-Frenkel ($0.5\text{-}1.25\text{MV/cm}$)	<ul style="list-style-type: none"> ▪ Comb-serpentine ▪ 30nmSiCN/20nmSiC ▪ 15nm TaN

A few methods have been employed to improve the leakage between the Cu lines. One method is to add a hard mask or buried capping layer beneath the cap barrier [47, 53].

The SiO₂ (or USG) buried capping layer is deposited on the carbon-doped SiO₂ (SiOC) low-*k* dielectric to protect the low-*k* dielectric from plasma damages during trench patterning and eliminate the CMP-induced damage of the low-*k* dielectric. Thus, the leakage current is reduced with a buried capping layer due to the elimination of process-induced damages, and inherently lower leakage and higher breakdown strength of SiO₂ compared to SiOC, as well as reduced electric field at the interface. Another method is to eliminate the CMP-surface leakage path by using the same material for both the hard mask and cap barrier above it [54].

2.5 Dielectric Breakdown Mechanisms and Models

2.5.1 Review of dielectric breakdown mechanisms

In order to predict the lifetime of a dielectric prior to breakdown and to verify the reliability of the dielectric, electric field acceleration models which relate closely to the dielectric breakdown mechanism need to be established. The theories discussed here were studied on SiO₂ gate dielectric, which has been a technologically important dielectric used in integrated chips. Early electronic breakdown theories were based on impact ionization and electron avalanche effect [55]. The breakdown stages are as follows: (1) initiating stage increasing the electrical conductance which leads to (2) instability causing current runaway and resulting in (3) voltage collapse across the dielectric, with local melting and evaporation. At the initiating stage, electrons are injected into the conduction band of the dielectric and at a critical field, the electrons have sufficient energy to cause impact ionization as well as generate a localized succession of electron avalanche. This leads to occurrence of current runaway instabilities and eventually voltage collapse which is mainly caused by discharge of electrostatic energy stored in the dielectric.

However, fields estimated from impact ionization and avalanche theory is an order of magnitude higher than those observed for large band gap dielectrics (>4 eV) [56]. Therefore, other breakdown mechanisms for SiO_2 such as the ion-induced breakdown model were proposed. The model is based on F-N tunneling at cathodic protuberance, filamentary Joule heating and activation of mobile positive ions such as Na^+ , which enhances the injecting field leading to breakdown. However, this model is no longer applicable to SiO_2 gate dielectrics since the mobile ion contamination is very much reduced with current technology though it may be applicable to low- k interconnect dielectrics as will be discussed under Cu-induced dielectric breakdown model.

Currently, a well accepted intrinsic dielectric wearout mechanism which eventually leads to breakdown for thin SiO_2 gate dielectrics is based on gradual oxide degradation, which is a consequence of trap generation in the oxide [57]. Breakdown is triggered once the accumulated traps reach a critical level. Several indicators of oxide degradation reported are interface trap creation, negative or positive charge trapping, hole fluence, neutral electron trap creation and generation of a stress-induced leakage current (SILC). SILC is leakage current through the gate oxide, which is divided into transient and steady state components [58]. Initially, the transient component exists whereby the leakage decreases with time due to electron trapping (or filling) in the oxide. When equilibrium between trap filling and emptying is reached, a steady state leakage is reached. Thick oxides have a large transient component and a small steady state component.

There are mainly three trap generation mechanisms or models which give rise to oxide degradation, which are the anode hole injection model (i.e. $1/E$ model), electric field energy model (i.e. E model) and hydrogen release model [59, 60]. Moreover, the dielectric breakdown is believed to occur via a percolation model. As the density of

neutral electron traps increases, conductive clusters of traps start to overlap with each other subsequently forming a percolation path between the anode and cathode and ultimately leading to a breakdown path [61].

Therefore, the three main stages of hard breakdown are as follows: (1) defect generation and accumulation which eventually forms a conductive path that leads to (2) dielectric breakdown at the conductive pathway and immediately followed by (3) thermal damage by lateral propagation of the breakdown spot. This has been modeled for oxide thickness of more than 5 nm. However, for sub-5 nm oxides, soft breakdown was included [62]. It is defined as an oxide breakdown without lateral propagation of the breakdown spot due to thermal damage and exhibits anomalous increase in stress-induced leakage current as well as current fluctuations.

Although the SiO₂ gate dielectric and low-*k* dielectric in interconnects are different in terms of the structure (i.e. MIS stack versus a complex interconnect architecture) and dielectric material, many of the concepts and mechanisms gained from gate dielectrics are used to explain the breakdown of low-*k* dielectrics in interconnects as will be elucidated in the ensuing sub-section.

*2.5.2 Dielectric breakdown models relevant to Cu/low-*k* interconnects*

Thermochemical E model

Logically, the thermochemical E model is chosen over the 1/E model for interconnect lifetime extrapolation. This is presumably due to insignificant current injection by F-N tunneling into the low-*k* dielectric because of the much thicker low-*k* dielectric as compared to gate dielectrics. Therefore, the derivation of the model and its corresponding physical mechanism is further discussed here. The linear field model in which the

logarithm breakdown time is linearly dependent on electric field was empirically observed by Crook [63], Anolick [64] and Berman [65]. It was later given a thermochemical foundation by McPherson and Baglee [66, 67]. Thermochemical E model is based on Eyring model to characterize the time-dependent dielectric breakdown data. The Eyring model is a theoretical model based on exponential reaction rate theory and thermodynamic free energy considerations. The thermochemical E model was established to explain the discrepancies in activation energy and field acceleration parameters obtained from different researchers. Quantitatively, the model suggests that the discrepancies were due to activation energy dependence on electric field and field acceleration parameter dependence on temperature.

When the dielectric is stressed at E_{ox} (which is less than the breakdown field, E_B), the breakdown occurs after some time. Assuming a collection of identically processed capacitors, the rate of breakdown of these capacitors may be approximated by a reaction rate constant, k , described by the Eyring model as shown in equation 2.4.

$$k \propto \exp\left(-\frac{\Delta G^*}{k_B T}\right) \dots\dots\dots (2.4)$$

The ΔG^* represents the free energy of activation associated to the breakdown. By treating the surviving capacitors as reactants and the broken down capacitors as products, the time-to-failure (TTF) is related exponentially to the free energy of activation as shown in equation 2.5 and can be described as a free energy diagram shown in Figure 2.9.

$$TTF \propto \frac{1}{k} \propto \exp\left(\frac{\Delta G^*}{k_B T}\right) \dots\dots\dots (2.5)$$

Figure 2.9 Dielectric breakdown process as a function of free energy for the reaction coordinates [68].

After several simplifications and assumptions of the Gibbs free energy, the following relationship is obtained whereby ΔH_o^* is the change in enthalpy required to activate the poly filament growth at breakdown, B and C are constants and $S = E_B - E_{ox}$.

$$\Delta G^* = \Delta H_o^* + k_B T \left[B + \frac{C}{T} \right] S \quad \dots\dots\dots (2.6)$$

The time-to-failure then becomes:

$$TTF(f\%) = A \exp\left(\frac{\Delta H_o^*}{k_B T}\right) \exp[\gamma(T)S] \quad \dots\dots\dots (2.7)$$

The field acceleration parameter, γ , is therefore a temperature dependent parameter given in equation 2.8. γ can be obtained experimentally from the gradient in plot of TTF versus electric field.

$$\gamma(T) = \left(\frac{\partial \ln TTF(f\%)}{\partial S} \right)_T = - \left(\frac{\partial \ln TTF(f\%)}{\partial E_{ox}} \right)_T = B + \frac{C}{T} \quad \dots\dots\dots (2.8)$$

On the other hand, the effective activation energy is a function of the field given in equation 2.9. $(\Delta H)_{eff}$ can also be obtained experimentally from the gradient in a plot of TTF versus temperature.

$$(\Delta H)_{eff} = k_B \left(\frac{\partial \ln TTF(f\%)}{\partial (1/T)} \right)_s = \Delta H_o^* + k_B C(E_B - E_{ox}) \dots \dots \dots (2.9)$$

The model was further given a physical meaning by describing the intrinsic breakdown process as a thermal bond breakage of weak bonding states due to strong dipolar coupling of the intrinsic defect states with the local electric field in the dielectric [69]. The dipole-field coupling results in a lower activation energy that is required to thermally break a bond and thereby accelerating the dielectric degradation process. Moreover, one of the dominant intrinsic defect was established to be an oxygen vacancy, or so called E' center whereby the bonds to break are Si-Si bonds. The formation of an oxygen vacancy is due to the replacement of a highly strained Si-O-Si bond with Si-Si bond. This is because the highly strained Si-O-Si bonds, whereby its bond angles are either greater than 180° or smaller than 120° , were unstable compared to the Si-Si bond with an oxygen vacancy [70]. The stretching of Si-O-Si bond in SiOCH low- k dielectric after an applied electric field was also observed. The Si-O-Si bond angle deviated to angles greater than 144° or less than 144° after an electric field was applied [71]. Therefore, the thermochemical E model is justifiable for TDDB prediction in Cu/low- k interconnects although the breakdown does not only involve the degradation of low- k dielectric but likely includes other factors such as interface and barrier integrity as well as the impact of Cu contamination.

An electron passing through the dielectric will see on average the applied electric field between the anode and cathode terminals. However, each SiO₂ molecule experiences an externally applied field plus a dipolar field caused by polarization, P , due to distortion of the SiO₂ lattice when a field is applied. The sum of the applied field and dipolar field is

called the localized field, E_{loc} . It is best described by Lorentz relation or Mossotti field as shown in equation 2.10 whereby E_{ox} is the applied field, L is the Lorentz factor (usually $L = 1/3$ for cubic symmetry), P is the induced polarization, χ is the dielectric susceptibility and ϵ_0 is permittivity of free space [72].

$$E_{loc} = E_{ox} + L(P / \epsilon_0) = (1 + L\chi)E_{ox} \dots\dots\dots (2.10)$$

Assuming that it requires an amount of energy ΔH_o^* to activate bond breakage in the absence of an electric field, then the activation energy for bond breakage in the presence of field is described in the equation 2.11, which is an updated version to equation 2.9 [68].

$$(\Delta H)_{eff} = \Delta H_o^* - p_{eff} E_{ox} \dots\dots\dots (2.11)$$

This means that the higher the applied field, E_{ox} , the lower the energy to activate the bond breakage and thus, the shorter the time-to-failure. Moreover, equation 2.11 shows that the activation energy obtained from TDDb data depends on the applied electric field. A field dependence of activation energy in SiCOH low- k dielectric used in interconnects was also reported [73]. p_{eff} is the effective molecular dipole moment which depends on the nature of molecular bonding in the SiO_2 dielectric and is related to the field acceleration factor, γ , as shown in equation 2.12. It was demonstrated that p_{eff} ranged from 7 eÅ to 13 eÅ whereby 13 eÅ is associated with a stretched silicon-oxygen bond while 7 eÅ is consistent with a hole-captured silicon-oxygen bond [74].

$$\gamma(T) = - \left[\frac{\partial \ln TTF(f\%)}{\partial E_{ox}} \right]_T = \frac{p_{eff}}{k_B T} \dots\dots\dots (2.12)$$

Copper-induced Dielectric Breakdown Model

In addition to the leakage through the dielectric leading to intrinsic dielectric degradation, Cu contamination at levels more than 10^{12} atoms/cm² could shorten the time-to-failure of

silica-based dielectrics by more than ten times [75]. Cu contamination can be brought about during process integration and further aggravate with application of an electric field and temperature. The critical process steps that could contribute to Cu contamination are during via patterning and Cu CMP. Cu residues can be found outside the diffusion barrier due to re-sputtered Cu onto the via sidewalls induced during via etching [76]. Cu residues can also be found on the low- k dielectric surface due to micro-scratches, arc-scratches or incomplete CMP polishes [77, 78]. An increase in Cu particles at the CMP surface was also found after prolonged exposure to the ambient before cap barrier deposition [79, 80]. This is due to ease of oxidation of the Cu metal surface to form cuprous oxide (Cu_2O) and cupric oxide (CuO) [81, 82], encouraging the ionization of Cu atoms to form Cu ions.

Apart from concentration gradient, the driving force for Cu migration is believed to be due to presence of oxygen (O_2) in the dielectric whereby oxidized Cu provides the source of Cu ions that are transported through the SiO_2 dielectric via diffusion and drift [83]. The Cu ion migration is found at temperatures as low as $200 - 300^\circ\text{C}$ with applied fields ranging from $0.1 - 1.0 \text{ MV/cm}$. A similar mechanism was reported for porous MSQ-based dielectric whereby oxidants from the ambient diffuse through the dielectric pores, driving Cu migration through the diffusion barrier and into the dielectric [84]. Alternatively, Cu ions can migrate through non-uniformities such as pinholes at the sidewall diffusion barrier and into a porous low- k dielectric [85]. A separate study demonstrated that Cu in the form of Cu^+ ions are more stable (in terms of a lower potential energy) in the SiO_2 dielectric as compared to Cu atoms. This further validates the aforementioned mechanism whereby Cu ions are the migrating species [86]. Thermal diffusion of Cu atoms into SiO_2 is possible but at temperatures more than 350°C [87] or in dielectrics that are porous.

The migration can occur by interstitial or substitutional (vacancy) diffusion or through structural imperfections such as grain boundaries, dislocations and free surfaces. For diffusion of Cu atoms through polycrystalline films such as the Ti or Ta-based sidewall barriers, defects such as vacancies, grain boundaries and dislocations provide fast diffusivity paths for Cu. However, for Cu^+ ion drift and diffusion in dielectrics, the molecular structure of the dielectric affects the migration rate. In reference [88], the cross-linking and polarity of functional groups in the organic polymer dielectrics were demonstrated to be factors affecting the Cu^+ ion migration. To illustrate, the increased cross-linking obstructs the interstitial migration of Cu^+ ions due to minimized free volume in the polymer dielectric. On the other hand, the presence of polar functional groups such as $\text{C}=\text{O}$ provides a strong partial negative charge (δ^-) that can attract Cu^+ ions electrostatically, thus enhancing the migration.

In summary, the main driving force for Cu migration into dielectrics is the presence of oxidants (O_2 or H_2O molecules) that are either from the ambient or out-gassed from the dielectric. The oxidized Cu is a source of Cu ions by which Cu^+ ions are formed due to a negative and minimum potential energy generated. Thereafter, the Cu^+ ions drift and diffuse into the dielectric when temperature and field are supplied. Moreover, the molecular structure of the dielectric plays a role in enhancing or reducing the rate of Cu^+ ion migration. They are the free volume density (for non-porous dielectrics), porosity level (for porous dielectrics) and the polarizability (or molecular dipole moment) of the dielectric.

Due to the numerous possibilities of Cu^+ ion drift and diffusion into the dielectrics, the breakdown mechanism caused by Cu generally includes the following: (1) Cu ionization and injection (or migration) of Cu^+ ions from anode into the dielectric followed by (2)

Cu^+ ion migration through the dielectric, and (3) formation of leakage pathways as well as Cu^+ ion accumulation near the cathode leading to increase in leakage current and eventual dielectric breakdown. The energy band diagram of Cu^+ ion migration into the dielectric is generally depicted as shown in Figure 2.10. To further illustrate, the accumulation of Cu^+ ions in the dielectric near the cathode lowers the potential barrier, thus allowing more electron injection into the dielectric. Moreover, Cu^+ ions migrating towards the cathode can recombine with oncoming electrons to form Cu particles in the dielectric. This could lead to the formation of a conductive pathway (or a percolation path) in the intra-level dielectric [80, 89], which leads to a catastrophic dielectric breakdown. One of the physical TDDB models proposed for Cu ion-induced breakdown is consistent with the thermochemical E model [90].

Figure 2.10 Cu-induced dielectric breakdown model in Cu interconnects. (a) Cross-section of an interconnect structure illustrating the Cu ionization and subsequent migration along the CMP interface with an applied field. (b) Energy band diagram depicting the formation of leakage pathway in the dielectric and Cu^+ ion accumulation at the cathode [29].

Square Root E model

Besides the commonly used linear E model for Cu/low-*k* interconnects, a square root E model was proposed and could be a more accurate prediction of the interconnect dielectric lifetime. As illustrated in Figure 2.11, the $\sqrt{E}$ dependence is empirically proven and predicts a less pessimistic TDDB lifetime as compared to the E model [73]. The model was based on the frequently observed Schottky and P-F emission. The linkage

between conduction mechanism and acceleration field model was first brought up for the $1/E$ model in gate oxides whereby F-N tunneling exhibits a reciprocal field dependence.

Figure 2.11 Experimental data obtained from long term TDDB tests matches the $\sqrt{E}$ model [73].

Chen *et al.* [73] describe the breakdown mechanism as being caused by Cu ions and atoms which eventually causes a metallic shorting bridge in between the Cu lines or creates a damage path catalyzing bond breakage at the low- k dielectric and capping layer interface. The Cu ions are postulated to be generated from thermalization of energetic electrons at the anode terminal. The electrons contribute to Schottky emission due to injection of electrons from the cathode terminal and subsequently P-F emission due to traps in the dielectric. A more detailed explanation of the source of P-F emission was given by Suzumura *et al.* [91]. Referring to Figure 2.12(a), a P-F emission from the electron traps in the dielectric is deduced, which is before any constant voltage stress (referred as bias-temperature stress in the figure). In Figure 2.12(b), which is the first stage after constant voltage stress, Cu ions migrate into the dielectric forming deeper electron traps. As a result, the constant voltage leakage current curve initially decreases with time. However, the TDDB leakage current increases gently with longer stress time. This was attributed to the accumulation of Cu ions near the cathode terminal resulting in

modification of the conduction band and thus causing the increased electron injection (Figure 2.12(c)).

Figure 2.12 (a) Energy band diagram illustrating source of Poole-Frenkel emission before bias-temperature (BT) stress, (b) first stage after BT stress and (c) second stage after BT stress [91].

Other Dielectric Breakdown Models

An interesting model proposed by Lloyd *et al.* [92] states that the breakdown failure depends on the probability of an electron gaining sufficient energy to cause impact damage to the dielectric. Therefore, the time-to-failure dependence on the field is mainly dependent on the probability of having sufficient electron energy and not on the precise physical mechanism(s) causing damage, which were described in the previous E and $\sqrt{E}$ models. The time-to-failure (TTF) is then described in equation 2.13, whereby N_f is the number of defects needed to promote breakdown; N_0 is the number of pre-existing defects; A is the pre-exponential term in the P-F emission as depicted in equations 2.2 and 2.3 and α is the electric field necessary for damage creation within the electron mean free path. The first term in the exponential represents the leakage current while the second term represents the electron impact damage.

$$TTF = \frac{N_f - N_o}{AE} \exp\left(-\frac{\beta_{PF}}{k_B T} \sqrt{E} + \frac{\alpha}{E}\right) \dots\dots\dots (2.13)$$

Apart from the field-enhanced thermal bond breakage, Cu-induced dielectric breakdown and electron impact damage, the influence of mechanical forces was also considered. The breakdown mechanism was attributed to mechanical cracking at the low-*k* dielectric and capping layer interface for low breakdown strength samples (Figure 2.13(a)) and cracking in the capping layer for higher breakdown strength samples (Figure 2.13(b) and (c)) [93]. The cracking is believed to be due to electrostatic forces between the metal lines which led to Cu extrusions through the formed cracks. Moreover, weaker interfacial adhesion strength at the dielectric capping layer/Cu interface as compared to the low-*k* dielectric/capping layer interface is the postulated reason for the low-*k* dielectric/capping layer crack.

Figure 2.13 (a) Cracking at the low-*k*/capping barrier interface for low breakdown strength samples. (b) and (c) Cracking at the capping barrier for high breakdown strength samples.

2.5.3 Importance of electric field in dielectric breakdown

From the above discussions, electrical stress (i.e. electric field) is one of the most important driving forces for dielectric degradation. Besides creating a potential difference for electron conduction through the dielectrics, electric field also enhances the Cu⁺ ion drift and diffusion into the dielectrics. At the molecular level, the applied electric field

results in an enhancement of localized electric field caused by polarization of the dielectric molecules. This in turn lowers the activation energy required for bond breaking, thereby accelerating the breakdown reaction rate through a thermal (Boltzmann) exponential process.

Since electric field plays an important role in the dielectric degradation, several studies have shown the significant effects of electric field on dielectric breakdown. One important aspect is the electric field distribution at the CMP interface. Electrical simulations have shown high electric fields at the CMP interface due to contributions from the higher dielectric constant of the cap barrier as well as the shorter distance between the Cu lines at the top of the trench due to sloped profiles [94, 95].

Apart from geometrical dimensions of the Cu trenches, electric field distribution on different structural layout of the Cu lines was simulated. The electric fields were found to increase 2x or 2.5x higher than nominal fields at surrounded corner structures or misaligned vias, respectively [30, 96]. Hence, there is a higher probability of failure at the corners and tips of an interconnect line due to the enhancement in the electric field. Furthermore, asymmetrical via-involved structures demonstrated worse TDDB performance as compared to the conventional line-to-line structures [97].

In addition, the TDDB lifetime decreased with decrease in Cu line width [79]. From MEDICI simulation, the reason for the lifetime decrease is due to stronger electric field interaction from both sides of the same metal line in comb-line capacitors for finer Cu lines regardless of metal spacing, a phenomenon named ‘fine line effect’. Furthermore, it was highlighted that as the metal spacing shrinks with technology node, line edge roughness becomes critical. It was shown that the line edge roughness increases with the

decrease in metal spacing, resulting in an increased spacing variation [98]. This led to shorter time-to-failures and wider spread in the TDDB values (i.e. smaller Weibull slope). This is due to electric field enhancements at the protrusions created from the line edge roughness. As shown in Figure 2.14, the electric field enhancement factor increases with decreasing line-to-line spacing and increasing roughness depicted by the b/a ratio. Hence, the role of the electric field on TDDB degradation is important especially with the decrease in metal spacing to keep in pace with the scaling of devices.

Figure 2.14 Electric field enhancement factors as a function of line-to-line spacing with different line edge roughness sizes [98].

2.6 Reliability Concepts and Modelling

Reliability is defined as the probability that a device or component will perform an intended function under stated conditions for a stated period of time. The study of reliability involves both reliability physics and reliability statistics. The reliability physics is the study of the failure mechanisms which is the physics and chemistry of why things fail and do not fail. The failure mechanisms and proposed models were described in the previous sections. On the other hand, reliability statistics is a means of quantifying the failure data with the use of statistical distributions and thus enables the assessment of the product quality through measuring certain parameters. Moreover, a large number of

devices need to be tested for the failure data to be statistically accurate. A well-known reliability model is the bathtub curve, which is a plot of the failure rate versus the operating time of a device. The three distinct regions in the curve are the infant mortality region (or early life), constant failure region and the wearout region. At the early stages of the device, which is the infant mortality region, the failure rate is high but decreases with time. This is followed by the constant failure region, which has a constant failure rate, and it corresponds to the use lifetime of the device. Beyond the useful life of the device, the device starts to fail at an increasing failure rate due to wearout mechanisms.

Some of the common terms in reliability are the reliability function, $R(t)$, cumulative distribution function (CDF), $F(t)$, probability density function (PDF), $f(t)$, hazard rate, $h(t)$, and mean-time-to-failure (MTTF). The $R(t)$ is the fraction of devices that survive at time t while the $F(t)$ is the fraction of devices that fails up to time t . Besides, the hazard rate, $h(t)$ is the instantaneous failure rate of items having survived to time t . There are mainly two methods to calculate the $F(t)$ for a set of devices. The mean ranking is used for normal distributions while the median ranking is appropriate for skewed distributions. Before calculating the $F(t)$ for each time-to-failure point, the times-to-failure are arranged in an ascending order. Then, the $F(t)$ are calculated according to equation 2.14 for mean ranking and equation 2.15 for median ranking, whereby i is the order of the particular time-to-failure point and n is the total number of devices tested.

$$F(t) = \frac{i}{n+1} \dots\dots\dots (2.14)$$

$$F(t) = \frac{i-0.3}{n+0.4} \dots\dots\dots (2.15)$$

The failure distributions obtained could be fitted to several theoretical probability distributions such as normal, lognormal, Weibull and exponential distributions. Since

lognormal and Weibull distributions are commonly used to fit the reliability failures in interconnects such as electromigration and TDDDB, the mathematics will be described. Both Weibull and lognormal distributions are skewed distributions unlike the normal distribution, whereby the PDF curve is symmetrical. Therefore, the median ranking method is used to calculate the $F(t)$ for each device.

The lognormal distribution is similar to the normal distribution except that all the data points are in the natural logarithm. The PDF of the lognormal distribution is described in equation 2.16. Like normal distribution, the lognormal distribution is a two parameter model. The first is μ , which has a physical significance of representing the time when 50% of the total distribution fail i.e. $\mu = \ln t_{50}$. The other parameter is the shape parameter, σ , which influences the shape of $f(t)$ and $F(t)$ curves and thus determines the hazard rate. Depending on the shape parameter, the lognormal distribution can represent the early failure, steady state and wearout regions in the life of the device.

$$f(t) = \frac{1}{\sigma t \sqrt{2\pi}} \exp \left[-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2} \right] \dots\dots\dots (2.16)$$

Similar to lognormal distribution, the Weibull distribution is generally a two parameter model. The PDF for the Weibull distribution is expressed in equation 2.17 while the CDF is expressed in equation 2.18. β is the shape parameter while η is the scale parameter. Generally, when $\beta < 1$, the failure rate is decreasing and thus, represents the infant mortality region. The Weibull distribution reduces to an exponential distribution when $\beta = 1$ and thus, represents the constant failure rate region. On the other hand, the failure rate fits the wearout region when $\beta > 1$. Clearly, the Weibull distribution can be used to model all three regions of the bathtub curve. Substituting $F(t_{50}) = 0.50$ into equation 2.18, the median-time-to-fail, t_{50} is $\eta[\ln 2]^{1/\beta}$. However, the t_{50} depends on the shape parameter.

Therefore, the time-to-fail in Weibull distributions is usually represented by $F(t_{63.2}) = 0.632$, which is the time when 63.2% of the total population fails. In this situation, the $t = \eta$, and thus η is referred to as the characteristics life parameter.

$$f(t) = \frac{\beta}{\eta} \left(\frac{t}{\eta} \right)^{\beta-1} \exp\left(- (t/\eta)^\beta\right) \dots\dots\dots (2.17)$$

$$F(t) = 1 - \exp\left(- (t/\eta)^\beta\right) \dots\dots\dots (2.18)$$

The various shapes of the PDF curves for Weibull and lognormal distributions appear to be quite similar as can be seen in reference [99, 100]. Therefore, a given set of reliability data may fit both models equally well. However, the suitability of the model depends on how accurate the predictions can be made by extrapolating the fitted curves beyond the data points. In general, the Weibull distribution provides a better fit to short time failures and is suitable for devices that have competing failure mechanisms whereby the weakest link fails first. Examples of cases best described by a Weibull distribution are dielectric breakdown and fracture. On the other hand, lognormal distribution is better at predicting long time failures and thus, more suitable for wearout mechanisms whereby device degradation occurs rather slowly. Hence, lognormal distributions are used for electromigration lifetime predictions while Weibull distributions are used for TDDB lifetime predictions.

CHAPTER 3: COMB STRUCTURE

3.1 Experimental Details

A summary of the experimental procedures performed for the comb structures to investigate the failure mechanisms occurring in the Cu/low- k interconnect is shown in the flow chart of Figure 3.1. A brief description of the test structures, electrical setup and failure analysis tools will be explained in the subsequent sub-sections.

Figure 3.1 Flow chart illustrating the sequence of failure analysis steps performed for comb structures.

3.1.1 Comb test structures

The test structure used was a standard, inter-digitated, comb structure with line width/space of $0.18\ \mu\text{m}/0.18\ \mu\text{m}$ as shown in Figure 3.2. The intra-metal dielectric tested is at the first metal level (M1). The cross-section of the structure shown in Figure 3.3 illustrates the SiC capping layer and the Ta diffusion barrier used to prevent Cu out-diffusion. The low- k dielectric is a carbon-doped SiO_2 (SiOCH) with a measured dielectric constant of 2.9.

Figure 3.2 (a) Optical image of several comb structures on a die and (b) a schematic of the single comb structure with a line width/space of $0.18\ \mu\text{m}/0.18\ \mu\text{m}$ and a total test area of $10^{-3}\ \text{cm}^2$.

Figure 3.3 Cross-section view of the comb structure.

3.1.2 Electrical test setup

A wafer level voltage ramp (V-ramp) was applied to examine the breakdown voltage distributions and I-V leakage trends, using a HP4156C semiconductor parameter analyzer. A linear voltage ramp was used with a step increase of 1 V. The wafer chuck was heated to three different temperatures, 20°C, 100°C and 150°C, to study the effects of temperature on breakdown voltage. The electrical test setup for the wafer level V-ramp is shown in Figure 3.4.

Figure 3.4 Schematic diagram depicting the electrical setup for the voltage ramp test.

3.1.3 Failure analysis tools

Physical failure analysis was conducted first by using an optical microscope and then a scanning electron microscope (SEM) to observe and detect the failure sites on the surface of the dice. Next, focused-ion beam (FIB) milling was used to cut the samples to observe the failures from a cross-sectional view and also to prepare the samples for transmission electron microscopy (TEM). Lastly, SEM, TEM and energy dispersive X-ray (EDX) analysis attached to a scanning TEM (STEM), were used to investigate the failures.

For failures that were not visible from the optical microscope, a failure/fault localization technique was used. One promising approach to localizing resistive and open metallization defects is by using laser-induced fault localization techniques. Laser-induced techniques are usually implemented in a scanning optical microscope with a laser

source to provide carrier or thermal stimulation, depending on the band gap of the material studied and the properties of the defect investigated. For Si devices, a near infrared laser source with 1340 nm wavelength is suitable since it is not entirely absorbed by Si and most back-end-of-line dielectrics and could produce effective conductor heating. The principle of detecting resistive and open metallization defects is by scanning a laser beam across a biased sample to thermally stimulate the defect. A defect will cause a large change in resistance, which will then be collected, amplified and finally translated into a TIVA image. The change in resistance is detected either through a change in current with a constant voltage applied for Optical Beam Induced Resistance Change (OBIRCH) technique [101] or through a change in voltage with constant current supplied for Thermally-Induced Voltage Alteration (TIVA) technique [102]. The TIVA technique is inherently more sensitive with detection of voltage change compared to a detection of current change in the OBIRCH technique.

Therefore, TIVA was used in this research due to its availability and a more sensitive detection method compared to OBIRCH. However, the conventional TIVA is insufficiently sensitive for effective failure localization for comb test structures. Therefore, pulsed-TIVA was used instead. It has been shown that detection sensitivity for TIVA can be significantly enhanced by a gain factor of over 9 times with the use of a pulsed laser with digital signal integration algorithm [103]. The enhanced detection sensitivity allows the localization of two types of subtle failures which are otherwise not detectable by conventional TIVA, as will be demonstrated in sub-section 3.4.2.

3.2 Statistical Analysis of Dielectric Breakdown in Comb Structures

The dielectric breakdown voltage (V_{BD}) is defined as the voltage when the leakage current reached 10 μA , which is also the set compliance level. After the voltage ramp

tests, cumulative V_{BD} distributions at different temperatures were plotted in Figure 3.5. A large spread in the V_{BD} data is seen at low temperatures but the spread tightens at higher temperatures. Moreover, a bi-modal or multi-modal failure trend is apparent for the V_{BD} distribution at 20°C and 100°C. To understand the possible different failure modes and mechanisms, the I-V characteristics corresponding to the V_{BD} values were analyzed.

Figure 3.5 V_{BD} distributions obtained at 20°C, 100°C and 150°C.

Three distinct I-V characteristics were found and were plotted in logarithm scale as shown in Figure 3.6. The I-V characteristics for Type 1 failure mode is recognized as a sudden increase in leakage current up to the set compliance level. The current jump is typically in the range of 1 to 2 orders of magnitude over a 1 V step increase. This trend can be interpreted as a switch from a resistive pathway to an electrical short in the dielectric between the metal lines. Meanwhile, the Type 2 failure mode shows a gradual increase in leakage current up to the compliance level. The leakage pathway remains resistive even at breakdown voltage.

On the other hand, Type 3 failure mode shows a combination of Type 1 and 2 failures. There is an abrupt increase in leakage current but by a smaller amount (3-10 times) compared to that observed in Type 1, followed by a gradual but fluctuated increase in leakage up to the compliance level. Therefore, the V_{BD} for Type 3 failure is defined differently from that for Type 1 and 2 failure modes. The V_{BD} for Type 3 failure is the voltage when the leakage current increased abruptly by a substantial amount (i.e. at least 3 times).

Figure 3.6 Logarithm scale of the proposed three distinct I-V leakage characteristics extracted from voltage ramp tests at 20°C.

The breakdown voltage distribution at each temperature was re-plotted in Figure 3.7, with the V_{BD} grouped according to the type of leakage current characteristics (failure mode) observed. A normal distribution was used and as observed from Table 3.1, the mean breakdown voltage (μ) and standard deviation (σ) is similar to that reported in [104]; except that no bimodal distribution was observed in the reference. Here, a multi-modal failure distribution is apparent. For example, in Figure 3.7(a), the three regions of the multi-modal failure are labeled A, B and C. After grouping the V_{BD} values according to the failure types defined earlier (i.e. I-V characteristics), regions A and C match with

Type 1 and Type 2 failure distributions, respectively. The same matching was found for the V_{BD} distributions at 100°C and 150°C. Also, it can be seen that Type 2 failure mode has higher V_{BD} values compared to Type 1 failure mode at all temperatures. Moreover, from Table 3.1, the standard deviations for the grouped data (i.e. Type 1 and Type 2) are much smaller compared to the ungrouped data. On the contrary, no distinct trend was observed for Type 3 failure mode and thus, Type 3 will not be described from here on.

Figure 3.7 Breakdown voltage distributions for Type 1, Type 2 and Type 3 failure modes at (a) 20°C, (b) 100°C and (c) 150°C.

Table 3.1 Mean V_{BD} (μ) and corresponding standard deviation (σ) for failure types 1, 2 and 3.

Temp. (°C)	All		Type 1		Type 2		Type 3	
	μ	σ	μ	σ	μ	σ	μ	σ
20	52.87	12.50	35.86	3.02	64.77	2.86	49.30	6.93
100	43.21	11.96	34.00	4.39	47.64	6.97	45.83	19.80
150	38.40	7.31	32.93	2.35	41.48	3.45	41.33	16.34

3.3 Temperature Dependence of Breakdown Voltage

Figure 3.8 was plotted to examine the temperature dependence of the three failure modes and to investigate the possibility of a different failure mechanism from the breakdown activation energies. The breakdown field strength, E_{BD} , was estimated by dividing the mean V_{BD} with the designed dielectric spacing, i.e. $0.18 \mu\text{m}$. However, it must be noted that the breakdown field strength could be higher than shown due to a smaller spacing at the top of the Cu trench caused by its sloped profile, as will be shown in Figure 3.12 later.

Figure 3.8 Arrhenius plot which shows the temperature dependence of breakdown field strength for Type 1 and Type 2 failure modes.

Nevertheless, it was observed that V_{BD} decreases with an increase in temperature, with an activation energy of (26 ± 12) meV extracted from the Arrhenius relationship. Specifically, Type 1 failure mode shows very weak temperature dependence with an activation energy of (7.0 ± 0.1) meV. Meanwhile, Type 2 failures show stronger temperature dependence with an activation energy of (37 ± 10) meV. Note that the deviations given for the breakdown activation energy values were calculated from the possible minimum and maximum slopes (within the standard deviations of breakdown values at the 3 temperatures) in the Arrhenius plot. The different activation energy for Type 1 and Type 2 failure modes implies that Type 1 and Type 2 failure experience a different breakdown failure mechanism. This was further investigated from the failure analysis results and will be discussed in section 3.5.

3.4 Type 1 and Type 2 Failure Mode Analysis

3.4.1 Observable failures (Type 2)

Type 2 and Type 3 failure modes show physical damage in the form of burn marks on the test structure as shown in Figure 3.9. The location of burn marks was found to be random due to the random nature of defects. Two main types of burn marks were found from the SEM top view image. Figure 3.10(a) and (b) exhibit bulging burn marks and a sunken burn mark, respectively. The FIB/SEM cross-sections shown in Figure 3.11 illustrate the explosion-like failure, i.e. the complete melting of Cu lines as well as the surrounding low- k dielectric. Besides the melted regions at M1, the low- k dielectric above M1 was also completely destroyed, thus causing a delamination-like failure pattern. Similar burn marks with melted dielectric and Cu lines were also observed elsewhere [23, 105]. These burn marks are believed to be caused by Joule heating, thermal runaway and finally a catastrophic thermal dielectric breakdown.

Figure 3.9 Burn marks observable under an optical microscope for Type 2 and 3 failure modes.

Figure 3.10 SEM top view of (a) bulging and (b) sunken burn marks.

Figure 3.11 FIB/SEM cross-sections of the burn mark whereby complete destruction of Cu lines and its surrounding dielectrics are seen.

Type 1 failure mode does not show any apparent physical damage under the optical microscope and SEM but there may be subtle damages below the surface. However, it is difficult and time consuming to pinpoint the exact failure site for cross-sectioning due to the large comb area (10^{-3} cm^2) as compared to the much smaller failure analysis area for cross-sectional SEM or TEM (10^{-8} cm^2). One possible method to locate the failure site is

by top down polishing or delayering. Any abnormalities could be examined from the plan view of the comb structures. After top down mechanical polishing with assistance from silica slurry, a particle was seen lying in between the Cu metal lines as shown in Figure 3.12(a). Moreover, from the TEM cross-section of a FIB cut at a random location (Figure 3.12(b)), particle contamination is apparent. Therefore, particle contamination could be a contributing factor to the dielectric breakdown. However, the particle seen in Figure 3.12 (a) could be a particle introduced during or after delayering but before SEM imaging. This leads to the uncertainty of the delayering technique without use of any failure localization technique such as TIVA.

In summary, although Type 2 and 3 failures could be easily observed, the failure is catastrophic and thus leaving little evidence for further failure analysis. On the other hand, locating Type 1 failures using conventional methods is tedious, challenging and unpredictable. Hence, newly developed failure localization techniques are required to detect sub-surface failures. The application of TIVA, which is a laser-induced failure localization technique, for Type 1 failure in comb samples is introduced in the following sub-section.

Figure 3.12 Particle contamination as a possible cause to Type 1 failure mode.

3.4.2 Thermally-induced voltage alteration (TIVA) localization results

Although the burn marks of Type 2 and 3 failure modes can be detected by conventional TIVA as demonstrated in reference [106], but it is not needed since the marks can easily be seen under an optical microscope or SEM. However, even for Type 1 failure mode, the conventional TIVA technique cannot effectively localize the failure site. Therefore, a pulsed-TIVA with higher detection sensitivity was employed for localization of Type 1 failures. It will be shown that subtle dielectric defects which are otherwise not detectable with conventional TIVA can be detected with pulsed-TIVA.

Figure 3.13(a) shows the TIVA image collected from the front side of the sample, with the laser scanned in parallel with the comb lines of comb sample A at 66 mW laser power. It shows a weak TIVA signal at the circled defect location and a faint tail artifact at the right end of the leakage site indicated by the arrow. Conversely, an entire current leakage path caused by the resistive short in the comb lines was revealed after a pulsed-TIVA was performed, as illustrated in Figure 3.13(b). The main failure site appears with the highest signal intensity (i.e. largest resistance change) along the leakage path. Note that pulsed-TIVA is operated at the same laser power as TIVA but with an additional 500 Hz pulsing frequency and digital signal integration algorithm incorporated. The failure is then pinpointed by overlaying the optical image of the comb sample and pulsed-TIVA image as shown in Figure 3.13(c). Also, only three separate frame scans are required to cover the entire comb structure in order to locate the failure site.

To explain further, when the laser scans along the leakage path, heat is conducted quickly to the rest of the structure from the laser spot. Thus, as the temperature increases towards steady state, the change in resistance of the shorted Cu lines gradually decays. This converts to slow laser induced voltage change under constant current sourcing. It is

further attenuated by the ac-coupling input of the TIVA detection system acting as a high pass filter. Thus, the leakage path could not be effectively localized by conventional TIVA. On the other hand, pulsed-TIVA amplifies and modulates the laser induced transient response with a pulsed laser at 50% duty cycle. The integration algorithm further accumulates the laser induced response in each laser pulse pixel by pixel, eliminating the tailing artifacts in ac-coupled detection mode. This enhances the detection sensitivity by increasing the electrical signal intensity as shown by the vertical line profiles across the circled failure site for TIVA and pulsed-TIVA in Figure 3.13(d). Therefore, at the same laser power and biasing conditions, pulsed-TIVA is significantly more sensitive than conventional TIVA apart from being free of tail artifacts.

Another sample, comb sample B was examined but with the laser scanning perpendicular to the comb lines. Although the TIVA image in Figure 3.14(a) reveals a faint leakage path, it is not sufficiently sensitive to localize the actual failure site. However, the pulsed-TIVA image in Figure 3.14(b) shows that the leakage path and the failure can be clearly identified. The location of the failure is then revealed from the optical and pulsed-TIVA overlay image in Figure 3.14(c). The horizontal electrical signal line profiles across the failure site, shown in Figure 3.14(d), further exemplify the significant enhancement in electrical signal intensity with pulsed-TIVA as compared to the conventional TIVA. In addition, results of comb sample A and B show that the enhanced detection sensitivity of pulsed-TIVA in defect localization is independent of scan orientation.

Figure 3.13 (a) Frontside TIVA image of comb sample A at 66 mW laser power. (b) Pulsed-TIVA signal image at 66 mW laser power and pulsing frequency of 500 Hz. (c) Optical and pulsed-TIVA overlay image of comb sample A. (d) TIVA and pulsed-TIVA vertical electrical signal line profiles across failure site.

Figure 3.14 (a) Frontside TIVA image of comb sample B at 66 mW laser power. (b) Pulsed-TIVA image at 66 mW laser power and pulsing frequency of 500 Hz. (c) Optical and pulsed-TIVA overlay image of comb sample B. (d) TIVA and pulsed-TIVA horizontal electrical signal line profiles across failure site.

3.4.3 Non-observable failures localized by pulsed-TIVA (Type 1)

From the several comb samples with Type 1 failure mode that were examined by pulsed-TIVA, two kinds of failure were observed. They are dielectric cracking from the top corners of Cu lines and IMD breakdown. The IMD breakdown failure is similar to the burn mark failures observed previously except that the explosion is on a smaller scale and thus non-visible to the optical microscope. For comb sample A, a progressive series of FIB cross-section cuts were performed near the localized failure beginning from the right

as shown by the arrow in Figure 3.15. Note that the comb structure tested is boxed. The cross-sections at the defect were then imaged with a SEM at locations AA', BB' and CC'.

Figure 3.15 Optical and pulsed-TIVA overlay image of comb sample A indicating the cross-sectioned sites.

The SEM cross-section images captured at AA' and BB' are shown in Figure 3.16. In Figure 3.16(a), crack paths through the dielectric are found at the top corners of the Cu lines. At location BB' where the pulsed-TIVA signal intensity is the highest, an additional Cu extrusion along the crack path was observed as shown in Figure 3.16(b). A similar failure mode has been reported as shown in Figure 2.13(b), whereby the crack paths and Cu extrusion are believed to be due to mechanical forces exerted from electrostatic attraction between the comb fingers during the electrical stress. The initiation of these crack paths from the Cu corners are due to high stress concentrations at the Cu corners, generated by the vast differences in coefficient of thermal expansion of the Cu interconnect (16.5 ppm/°C) [107], Ta barrier (6.3 ppm/°C) [107], SiCN:H cap (3.9 ± 0.5 ppm/°C) [108] and SiOC:H low- k dielectric material (14 ± 3 ppm/°C) [108]. Moreover, the shear stress is maximum at the 45° direction [109]. Therefore, the crack paths occur at the direction of maximum shear stress instead of along the interfaces. Subsequently, Cu extrusion occurred through the crack paths, driven by the electrostatic forces.

Figure 3.16 SEM cross-section images at (a) AA' displaying dielectric crack paths from Cu top corners and (b) at BB' illustrating Cu extrusion through the crack paths.

From cross-section line CC', dielectric breakdown of the dielectric cap barrier and the intra-metal low- k dielectric is observed as shown in Figure 3.17(a). The corresponding TEM image in Figure 3.17(b) shows that the breakdown occurred between the upper regions of the Cu lines. This is in agreement with reports on the weakest link in the Cu interconnect/dielectric system, which states that the CMP interface region (i.e. Cu/SiC interface) experiences the highest leakage and electric field and thus is the most probable failure region [45, 94]. Further elemental analysis of the exploded region revealed random Cu traces as shown in the STEM-EDX line profile in Figure 3.17(c).

There are several possibilities for Cu to be present in between the Cu metal lines prior to the explosion. Cu could have diffused from the anode and especially along the CMP interface during electrical stress, or originate from the remains of Cu that extruded due to electrostatic forces. However, the voltage test was conducted within a short time and thus; Cu diffusion is not likely the case. Therefore, the traces of Cu detected could originate from the extruded Cu due to electrostatic forces. On the other hand, Cu could be present even before the electrical stress, whereby Cu residues were left behind after the CMP process step.

Figure 3.17 (a) SEM and (b) TEM cross-section images performed at CC' illustrating dielectric breakdown of the dielectric cap and low- k dielectric. (c) STEM-EDX horizontal line profile across the exploded region, indicated by a dotted line, showing traces of Cu in between the Cu metal lines.

Figure 3.18 shows the TEM image of a localized defect from another comb sample with similar pulsed-TIVA signals as comb sample A and B. It reveals a combination of IMD breakdown and dielectric cracking through the top corners of Cu lines. Since the defects that were localized from the comb samples by pulsed-TIVA are similar to those reported in the literature, the defects are thus not likely caused by the laser source of the system.

Figure 3.18 TEM cross-section for a comb sample which exhibits a combination of dielectric stack burn and dielectric cracking through the Cu top corners.

3.5 Failure Mechanism Prediction for Type 1 and 2 Failure Modes

From the experimental results, the characteristics for Type 1 failure mode can be summarized in the following:

- Low breakdown field strength (1.67 - 2.22 MV/cm);
- Weak temperature dependence (7.0 ± 0.1) meV;
- No visible burn marks but subtle failures such as dielectric breakdown, mechanical cracking and Cu extrusion were observed.

From these observations, Type 1 failure mode is postulated to be caused by extrinsic factors. This is supported by two characteristics in the above-mentioned, and they are the low breakdown strength and the breakdown field strength's temperature independence. Particle contamination and Cu metal residues in between the metal lines are the two probable extrinsic factors identified from the failure analysis results which led to the lowering of breakdown strength. The Cu residue and particles embedded in the dielectric could act as conductive paths which increase the leakage through the dielectric and eventually cause Joule heating, subsequent thermal runaway and finally a catastrophic dielectric breakdown. These factors are similar in a way that they do not require any temperature activation for the breakdown failure to occur because the shorting element is

already present in between the metal lines. This is likely the case since the activation energy was found to be 7 meV, which means temperature independence. Moreover, from pulsed-TIVA failure localization, the mechanical cracking observed is a result of stress concentration at the Cu corners (with maximum shear stress at 45° to Cu surface) and electrostatic forces which are not temperature dependent.

The distinct characteristics for Type 2 failure mode is summarized in the following:

- High breakdown field strength (3.33 - 3.89 MV/cm);
- Stronger temperature dependence (37 ± 10) meV;
- Visible burn marks seen

Type 2 failures are postulated to be due to the intrinsic properties of the SiOCH low- k dielectric and/or the SiC capping layer. This is because the temperature dependence, exemplified by the burn marks, indicates one of the feature characteristics of thermal breakdown in dielectrics [110]. Thermal breakdown occurs at local regions in the dielectric system, called hot spots, which have higher leakage current or poorer thermal conductivity than other regions in the dielectric system. The higher leakage current could be contributed by Cu ion diffusion and/or accumulation of charges at the hot spots, especially at the interfaces of the interconnect. As a result of poor heat removal away from the hot spot or Joule heating in localized resistive paths, thermal runaway occurs and results in melting of the dielectric and Cu metal lines. The Joule heat generated could also cause massive debonding which led to the bulging burn marks observed. Furthermore, Type 2 dielectric breakdown failures depend on temperature with an activation energy of 0.037 eV. This is close to that reported in reference [111], whereby a voltage ramp was done on similar carbon-doped low- k dielectric at different temperatures to extract the breakdown activation energy from an Arrhenius plot.

In summary, particle contamination / metal residues, mechanical cracking and Cu extrusion are some of the extrinsic factors that lead to dielectric failure in the interconnect, apart from the intrinsic factor of the dielectric itself, which leads to thermal dielectric breakdown. Although catastrophic breakdown was observed both in Type 1 and Type 2 failures, the root cause of the breakdown is different. The cause of Type 1 catastrophic breakdown is likely due to Cu residues or particle contamination left behind during process integration which led to the lower breakdown strengths whereas Type 2 failures are due to intrinsic degradation of the dielectric. Nonetheless, the dielectric breakdown or burn is believed to occur first at the top of the Cu metal lines, i.e. near the capping layer and CMP interface, before spreading downwards.

Although some deductions could be made of the failure mechanisms from the statistical data and failures localized by an improved failure localization technique (i.e. pulsed-TIVA), uncontrollable burn marks remain an obstacle to deeper understanding of the failure mechanisms in comb structures as these burn marks can be caused by both extrinsic and intrinsic factors. Furthermore, the comb structures may not completely represent the actual interconnect layout whereby some regions of the circuit have less densely packed parallel lines, terminated tips or corner structures. This leads to the next chapter of the thesis which covers the failure in terminated tips and corners structures.

CHAPTER 4: SINGLE LINE AND CORNER STRUCTURES

4.1 Experimental Details

4.1.1 Description and motivation of the new test structures

As mentioned in Chapter 3, the failures observed after voltage ramp and constant voltage stress show severe burn marks, thus it is difficult to understand the causes of failure in an interconnect due to the catastrophic nature of the breakdown. Moreover, it is difficult and time consuming to pinpoint a subtle failure (i.e. sub-surface failures) in a large, conventional comb structure with typical test area in the order of 10^{-3} cm^2 as compared to failure analysis area for cross-sectional SEM or TEM (10^{-8} cm^2). It is so because these failures can neither be seen under an optical microscope nor SEM. Although pulsed-TIVA was demonstrated to localize the sub-surface defects, the uncontrollable dielectric breakdown which leads to the destruction of the dielectric stack and any subtle evidence is inevitable. In addition, the comb structures do not represent all types of interconnect layout that are used in an IC chip.

Hence, one of the approaches taken to overcome these challenges is by designing test structures suitable for failure analysis as shown in Figure 4.1. There are four advantages with these new test structures. Firstly, it can confine the failure location to one particular site, unlike the conventional comb structures. It is also designed with dimensions suitable for precise TEM analyses such as high resolution imaging and elemental analyses. Inadvertently, failure severity is reduced due to the much smaller leakage area in these test structures. The smaller leakage currents enable control of the catastrophic dielectric breakdown to a certain extent and will be exemplified later in the chapter. Moreover, the structural effects or interconnect layout on the leakage current and dielectric breakdown of the Cu/SiOCH interconnect system can be evaluated. Also, a more stringent reliability assessment can be performed due to the electric field enhancement at the line ends (S1) or

corners (S2) compared to the nominal electric fields occurring in the parallel lines of comb structures.

Figure 4.1 Novel test structures named as (a) S1 for single line structures and (b) S2 for corner structures. Note that the dimensions given are in microns.

Figure 4.2 displays the SEM top view image of S1 and S2 test structures after the fabrication. The average metal spacing measured from the SEM and TEM images (Figure 4.3) for S1 and S2 are $0.30\ \mu\text{m}$ and $0.19\ \mu\text{m}$, respectively. The reference comb structures have a measured spacing of $0.15\ \mu\text{m}$. The low- k dielectric is a carbon-doped SiO_2 (SiOCH) with dielectric constant of 2.9 and the diffusion barriers used in the interconnect scheme are 50 nm-thick SiC(N) capping layer and 25 nm-thick Ta liner. Part of the hardmask (i.e. undoped silicate glass (USG)) deposited on the SiOCH low- k dielectric was retained after the chemical-mechanical polishing (CMP) step and remained as a buried capping layer (BCL) because it improves the leakage and breakdown field strength of the interconnects/dielectric system [53].

Figure 4.2 SEM layout of (a) S1 and (b) S2 test structures after fabrication.

Figure 4.3 TEM cross-section image of the novel test structure illustrating the SiC(N) capping layer, USG buried capping layer and SiOCH low- k dielectric.

4.1.2 Electrical characterization techniques

A standard voltage ramp and constant voltage stress were performed on the samples using the same electrical test setup as described in Chapter 3. A voltage step of 1 V up to a maximum of 200 V was applied. The estimated ramp rate during the voltage ramp is 0.6 V/s. For the voltage ramp, a compliance limit of 0.1 mA and 10 nA was set for the comb and new test structures (S1 and S2), respectively. Meanwhile, a compliance limit of 1 μ A and 100 pA for comb and new test structures, respectively, was fixed during the constant voltage stress to minimize the failure severity. Moreover, the breakdown voltage and time-to-breakdown was read at 10 μ A and 100 pA for the comb and new test structures, respectively, since the breakdown voltage and time-to-breakdown at that level is within the abrupt current jump region.

A separate type of test was conducted using the Human Body Model (HBM) electrostatic discharge (ESD) pulse. It has a very short pulse in the 150 ns range and high current in Amperes, depending on the applied voltage. Figure 4.4(a) shows the HBM ESD circuit with a 100 pF capacitor that charges up in less than 10 ns and a 1.5 k Ω resistor through which the discharged current flows. Meanwhile, Figure 4.4(b) shows the test setup that consists of a Keytek zapper connected through connecting wires to the probe tips and

HP4156C semiconductor parameter analyzer for testing of the wafer placed in the Karl Suss probe station.

Figure 4.4 (a) Electrical circuit for the Human Body Model (HBM) electrostatic discharge (ESD) pulse and (b) a schematic setup of the ESD and V-ramp tests.

The voltage levels used for S1 and S2 were $\pm 250\text{ V}$ and $\pm 200\text{ V}$, respectively. This voltage was chosen based on the ESD failure threshold criteria whereby the threshold is defined as the maximum voltage level that does not cause any failure for a minimum of 3 samples [112]. Note that the voltage levels can only be changed in steps of 50V. The number of pulses was varied from 1 – 8 pulses. Figure 4.5 shows the HBM ESD waveform at the zapper and at the probe tips, respectively, recorded using an oscilloscope. It can be seen that the HBM ESD pulse parameters were changed after it went through the connecting wires and probe tips. There is only a 10% increase in peak current but a large increase in pulse rise time (from 7.7 ns to 35.4 ns). This is due to the resistance and capacitance of the connecting wires used. Thus, the ESD pulse that was used for the experiment is not a standard HBM ESD pulse. However, the results obtained are still applicable because the author intends to use a very short electrical pulse to trigger the failure at progressive stages. The study was mainly done on S1 structures as will be described in sub-section 4.4.2 although similar results were obtained for S2 structures.

Figure 4.5 HBM ESD waveform output at the (a) zapper and (b) at the probe tips with an applied pulse voltage of 250 V.

4.1.3 Four point bend adhesion test

Four point bend adhesion tests were conducted to examine the interfacial adhesion strengths of the various interfaces found in the Cu/low- k interconnect architecture previously shown in Figure 4.3. The technique is based on well established interface fracture mechanics containing the interface of interest sandwiched between two massive elastic substrates (in this case Si substrate) and has been shown to provide a quantitative and reproducible measure of adhesion. Moreover, this technique constrains the relaxation of residual stresses present in thin films which would otherwise contribute to the debond driving force [113].

A load, P , was incrementally applied (at a rate of $0.2 \mu\text{m/s}$) to the sandwiched beam in a manner shown in Figure 4.6 until a plateau is reached. The macroscopic work of fracture (or interfacial adhesion strength) was then calculated in terms of the critical strain energy release rate, G_c (shown in equation 4.1) whereby the P was taken at the start of the plateau region in the load-displacement curve or at the point just after a drop in load occurs. The dimension of the beam used is $46 \text{ mm} \times 7 \text{ mm}$. The thin film stack was glued to a Si substrate with epoxy and cured at 100°C for 1 hour.

$$G_c = \frac{21(1-\nu^2)P^2l^2}{16Eb^2h^3} \dots\dots\dots (4.1)$$

The load, P , is recorded from the load-displacement curve; Poisson ratio of Si, $\nu = 0.28$; elastic modulus of Si, $E = 165 \text{ GPa}$; $l = 4 \text{ mm}$; $b = 7 \text{ mm}$ and $h = 725 \text{ }\mu\text{m}$ (dimensions of samples as illustrated in Figure 4.6).

Figure 4.6 Four point bend configuration illustrating the load application on the multi-layer thin films sandwiched between two elastic Si substrates of same thickness, $h = h_1 = h_2$.

The thin film stacks used for this study are shown in Figure 4.7, with the interface of interest highlighted with dashed lines. Note that the sequence of deposition of the films in the stacks were done in a similar way to that done for the interconnect architecture used. The process parameters were also kept the same. The debonded interfaces were then verified by X-ray photoemission spectroscopy (XPS) and step profiling.

Figure 4.7 Thin film stacks for four point bend adhesion test with the interface of interest highlighted. (a) SiOCH/USG, (b) USG/SiC(N), (c) SiC(N)/SiOCH and (d) Cu/SiC(N).

4.2 Electrical Characterization Results

4.2.1 Leakage comparison between the new structures and comb structures

A comparison of the leakage current levels for the conventional comb structure with S1 and S2 structures is illustrated in Figure 4.8. The applied voltage was converted to electric field by dividing the voltage by the average dielectric spacing. From the graph, it is obvious that the leakage current for comb structure is more than 3 orders of magnitude higher compared to the new test structures. This is because the comb structure has a larger area for leakage (i.e. $2.4 \times 10^{-3} \text{ cm}^2$) as compared to the S1 structure ($9.4 \times 10^{-10} \text{ cm}^2$) and S2 structure ($8.4 \times 10^{-9} \text{ cm}^2$). The leakage area was estimated as the area of the sidewalls along the cathode lines.

Figure 4.8 Interconnect leakage currents measured at room temperature for comb, S1 and S2 structures.

The I-V leakage curve was then fitted to either the Schottky or Poole-Frenkel (P-F) emission conduction mechanism that was reported for carbon-doped silicon oxides. Linear relationships were found in both the $\ln(I)-\sqrt{E}$ plot and $\ln(I/E)-\sqrt{E}$ plot for the comb structure. However, as shown in Figure 4.9(a), the dominant conduction mechanism in the comb structure at electric fields more than 1 MV/cm is found to be Schottky emission since it yields a reasonable k value of 2.29, which is close to the dielectric constant of the

low- k dielectric used. The same conduction mechanism for similar interconnect stack material and comb test structure were reported in [53]. At electric fields less than 1 MV/cm, an Ohmic conduction is observed as shown in Figure 4.9(b).

Figure 4.9 (a) Schottky emission observed in comb structures. (b) Plot of $\ln(I)$ - $\ln(E)$ yielding a slope of almost 1, indicating Ohmic conduction at low electric fields.

4.2.2 Conduction mechanisms in single line and corner structures

From the voltage ramp tests on the S1 and S2 structures, three distinct I-V leakage characteristics were observed and are categorized into three modes as shown in Figure 4.10. Note that each of these leakage modes corresponds to a specific failure mode which will be presented in section 4.3. Mode I shows an abrupt increase in leakage current of at least 2 orders of magnitude up to the compliance level. Modes II and III exhibit lower leakage levels as compared to Mode I and do not show any abrupt increase in current. Furthermore, there is a leakage step increase between 3 MV/cm to 5 MV/cm at room temperature voltage ramp for Mode III, which will be further analyzed in sub-section 4.5.1.

At low electric fields (<5 MV/cm), Ohmic conduction was deduced for S1 and S2 structures with leakage characteristic of failure mode II (Figure 4.11). However, at high electric fields, Poole-Frenkel emission was observed. The calculated dielectric constant, k ,

ranges from 1 to 2 which is neither close to the dielectric constant of SiOCH dielectric nor the SiC(N) cap. The reason for this k value will be discussed in sub-section 4.4.3 after physical failure analysis is performed.

Figure 4.10 Three distinct I-V leakage characteristics observed for (a) S1 and (b) S2 structures.

Figure 4.11 (a) & (b) Ohmic conduction at low electric fields and (c) & (d) Poole-Frenkel emission at high electric fields deduced for S1 and S2 structures, respectively.

4.2.3 Breakdown strength distribution

As seen in the I-V leakage characteristics, the breakdown voltage for S1 and S2 are defined when the leakage current reaches 100 pA. This is reasonable since the leakage at this current level is either in the abrupt increase region or at the region with the steepest leakage slope. The breakdown voltage for the S1 and S2 structures at different temperatures are plotted on a Weibull scale as shown in Figure 4.12. Apparently, the plot exhibits a bimodal or multimodal behaviour. However, there is no direct correlation between Modes I, II and III defined from the I-V leakage characteristics and the breakdown voltage distribution like the one observed in Chapter 3.

Figure 4.12 Weibull plots of the breakdown voltage conducted at 20°C, 50°C and 100°C for (a) S1 and (b) S2 structures.

The breakdown strength decreases with increase in temperature probably due to the increase in the rate of bond breakage of the dielectric. According to Maxwell-Boltzmann probability distribution, there is a larger fraction of molecules having energy higher than the minimum activation energy as the temperature is increased. Hence, with more molecules having high energy, the bonds in the dielectric become easier to break thereby lowering the breakdown strength. The activation energy calculated from the average breakdown field as shown in the Arrhenius plot in Figure 4.13 ranges from 19 meV to 27

meV. This is close to that found in the previous chapter for intrinsic breakdown of a similar carbon-doped SiO₂ low-*k* dielectric as well as those reported in reference [111].

Figure 4.13 Arrhenius plot which shows the temperature dependence of breakdown field strength for comb, S1 and S2 test structures.

4.2.4 Time-dependent dielectric breakdown (TDDB) analysis

The leakage current versus time (*I*-*t*) curves for S1 and S2 as compared to comb structures are shown in Figure 4.14. The curves are similar except for minor fluctuations observed for S1 and S2 structures, and this is likely due to the low leakage current levels measured. There are mainly two types of *I*-*t* curve for S1 and S2 as differentiated by the square and triangle symbols. The curves with a square symbol are *I*-*t* curves that are typically observed in comb structures and documented in the literature whereby the leakage current decreases initially before reaching a steady state, and finally an abrupt increase at the failure time. Curves of this type will be defined as hard breakdown in subsequent discussions. On the other hand, the *I*-*t* curves indicated by a triangle symbol exhibit a minor step leakage current increase between 1 pA to 10 pA (akin to a soft breakdown) prior to the final hard breakdown at 100 pA. Curves with a minor step leakage will be defined as soft breakdown.

Figure 4.14 General TDDB leakage current curves for comb, S1 and S2 structures.

A Weibull plot of the time-to-failure is shown in Figure 4.15. Similar to the breakdown voltage distribution, there is no direct correlation between the two types of I-t curves and the apparent bimodal distribution observed in the figure especially for S1. Thus, the occurrence of soft breakdown is random and does not necessarily result in a lower breakdown strength or shorter time-to-failure. Note that the cause of this pseudo-leakage will be described in sub-section 4.5.1. As summarized in Table 4.1, the Weibull slope, β , ranges from 1 to 2.

Figure 4.15 Weibull plot of times-to-failure for comb, S1 and S2 structures stressed at 20°C and 150°C.

Table 4.1 Weibull slope (β) obtained from constant voltage stress data.

Temperature ($^{\circ}\text{C}$)	Comb	Single line (S1)	Corner (S2)
20	1.09	0.71	2.23
100	0.87	0.51	1.04
150	1.11	0.69	1.08

From the Weibull plot in Figure 4.15, the temperature and electric field dependence of time-to-failure at cumulative probability of 63.2%, $F(t_{63.2})$, were acquired as plotted in Figure 4.16. Since the time-to-failure follows a linear E dependence, the thermochemical E model is adopted. The TDDDB activation energy, E_a , extracted for comb, S1 and S2 structures is 0.44 eV, 0.23 eV and 0.20 eV, respectively. In addition, the field acceleration parameter, γ , measured at 100 $^{\circ}\text{C}$ for comb, S1 and S2 is 2.22 cm/MV, 2.19 cm/MV and 1.31 cm/MV, respectively.

4.3 Physical Failure Analysis

4.3.1 Failure modes after voltage ramp

For failure mode I, the catastrophic thermal breakdown occurred in between the Cu metal lines after voltage ramp. The breakdown frequently resulted in the damage of the dielectric stack and the Cu lines and thus, left little evidence to the causes of failure. However, the more subtle failure modes II and III would be able to give clues to the factors leading to the catastrophic breakdown.

Figure 4.17 (a) Schematic diagram of S1 indicating locations of cross-sections performed at the horizontal (H) and vertical (V) directions. TEM images of failure mode II in S1 structures after voltage ramp, at the (b) planar, (c) horizontal and (d) vertical directions.

Figure 4.18 (a) Schematic diagram of S2 indicating locations of cross-sections performed at the horizontal (H) and vertical (V1 and V2) directions. TEM images of failure mode II in S2 structures after voltage ramp, at the (b) horizontal, (c) vertical V1 and (d) vertical V2 directions.

A schematic description of the location of cross-sections performed and the corresponding TEM images of failure mode II are shown in Figure 4.17 for S1 and in Figure 4.18 for S2. A delamination was found between the SiC(N) capping layer and the SiOCH low- k dielectric above it and consistently occurred directly above the anode terminal. Moreover, the delamination occurs only in the presence of a cathode terminal. In S1, the anode and cathode line faces each other at the end of the line as shown in Figure 4.17(a). Therefore, the delamination in S1 extends away from the cathode up to only a proportion of the anode terminal i.e. about 1 μm out of 1.8 μm total length of the anode, as shown in Figure 4.19. However, the cathode terminal in S2 faces the end of the

anode line and also along the anode line as can be seen in Figure 4.18(a). Thus, the delamination in S2 extends all the way to the end of the anode line.

Figure 4.19 (a) The delamination extends to a proportion of the anode terminal with a length of about 1 μm in S1 structure. (b) The delamination in S2 structure extends all the way to the end of anode terminal with a length of about 1.9 μm.

The delamination was found to occur at voltages higher than 150 V, which is at electric fields of more than 5 MV/cm when conducted at room temperature. This was deduced from the TEM cross-sections performed on samples stressed with a voltage ramp up to 100 V, 150 V and 200 V. No physical damage was observed after V-ramp up to 100 V and 150 V was applied, but a delamination was found after a V-ramp up to 200 V. Apart from the delamination at the SiC(N)/SiOCH interface, occasional voiding was observed near the interface between the USG buried capping layer and the SiOCH low-*k* dielectric below, it especially for S2.

For failure mode III, Ta migration from the anode sidewall and into the SiOCH low-*k* dielectric was observed in both S1 and S2 structures, in addition to the delamination. Figure 4.20(a) and (b) show the horizontal and vertical TEM cross-sections, respectively, indicating the Ta migration for S1 at the upper and lower corners of the Cu trench, after voltage ramp at room temperature (20°C). From the STEM-EDX line profile performed along the dotted lines as indicated in Figure 4.20(b), it is confirmed that the migrated

material is Ta (Figure 4.20(c)). A closer look at the Ta sidewall barrier indicates discontinuities throughout the barrier, which imply that some of the Ta material has migrated into the SiOCH low- k dielectric. This is also clearly seen in Figure 4.21(a) for another sample. Note that more Ta migration was observed at the center of the Cu line for this sample because it underwent voltage ramp at a higher temperature i.e. 100°C. Furthermore, the Ta barriers at the top, indicated by the arrows in Figure 4.21, were broken. This could be caused by the high stress concentration generated by a thermal expansion mismatch of the various materials at the site, namely Cu, Ta, SiOCH, USG and SiC(N). As shown in Figure 4.22, S2 also experiences Ta migration, similar to S1, but the Ta migration occurred mainly at the upper corners of the Cu trench.

Figure 4.20 Ta migration (indicated by the arrows) was observed for failure mode III in both the (a) horizontal and (b) vertical directions of S1, apart from the delamination. (c) STEM-EDX line profile along the dotted line shown in figure (b), illustrating Ta migration into the SiOCH low- k dielectric.

Figure 4.21 (a) Discontinuities observed throughout the Ta sidewall barrier due to Ta migration into the SiOCH low- k dielectric. (b) Broken Ta barrier as indicated by the arrows which could be caused by stress generated from thermal expansion mismatch of the various materials at the site.

Figure 4.22 Ta migration (indicated by the arrows) was observed for failure mode III in the (a) horizontal and (b) vertical directions for S2, apart from the delamination. (c) STEM-EDX line profile along dotted line shown in figure (b), illustrating Ta migration into the SiOCH low- k dielectric.

4.3.2 Failure modes after constant voltage stress

There are several types of hard breakdown failure modes observed for S1 after more than 10 times abrupt increase in leakage up to 100 pA (i.e. I-t curve indicated by a square symbol in Figure 4.14). The most severe failure is the catastrophic thermal breakdown which results in burn marks that are observable under an optical microscope. A less severe failure of a thermal breakdown that is non-observable under an optical microscope is shown in Figure 4.23. It can be seen that the upper part of the IMD i.e. near the SiOCH low- k dielectric and the SiC(N) cap layer were completely damaged. Moreover, the Ta barrier at the sidewalls of the Cu anode was damaged as well, and thus allowing Cu to diffuse into the dielectric from the anode terminal.

Figure 4.23 A sub-surface catastrophic thermal dielectric breakdown after TDDDB in S1 structures.

Another failure mode observed was Cu particles in the low- k dielectric, which almost bridged the Cu anode and cathode as shown in Figure 4.24. This was observed for the sample stressed at a constant field of 2.33 MV/cm for about 27 minutes at room temperature (20°C). The bridging of the Cu metal lines led to the abrupt increase in leakage seen in a typical I-t curve. The Cu particles are expected to cause Joule heating due to the conductive path created, and eventually a catastrophic failure as shown in the previous failure mode.

Figure 4.24 (a) TEM image displaying the Cu particles observed in the low- k dielectric and near the CMP surface after constant voltage stress at 2.33 MV/cm and 20°C. (b) EDX spectrum at position 1 whereby the Cu-K peaks at 8 keV are signals from the Cu grid used and EDX spectrum at position 2 which confirms the presence of Cu in the low- k dielectric due to the existence of Cu-L peaks at 0.93 keV.

The third failure mode observed for TDDB curves with abrupt current jumps is described as follows: Cu particles were found along the delaminated interface (i.e. interface between SiC(N) cap and SiOCH dielectric) and also scattered around the minor explosion mark at the Cu top corner of the anode terminal (Figure 4.25). Therefore, it could be implied that a delamination at the SiC(N) cap and SiOCH low- k dielectric interface had occurred followed by Cu diffusion prior to the catastrophic thermal breakdown of the dielectric stack during TDDB.

Figure 4.25 (a) TDDB failure mode after the abrupt current jump whereby Cu diffusion was seen along a delaminated SiC(N)/SiOCH interface at the anode terminal. Cu-L EDX profile is shown in the inset. (b) A magnification of the TEM image which shows the Cu particles along the delaminated interface.

For soft breakdown failure modes (i.e. I-t curve indicated by a triangle symbol in Figure 4.14), Ta migration from the anode sidewall was observed similar to that observed in samples stressed by voltage ramp. However, as seen in Figure 4.26, the Ta migration after TDDB stress is uniform across the thickness of the Cu trench as opposed to that stressed by voltage ramp, whereby the Ta migrated to further distances at the upper and lower corners of the Cu trench. As deduced from the I-V leakage characteristics and failure analysis, both failure modes II and III exhibit delamination but only failure mode III exhibits the Ta migration and leakage step. The leakage step in the I-t curve was also associated to the Ta migration. Therefore, the Ta migration is believed to contribute to the additional leakage prior to the hard breakdown.

On the other hand, there were samples that do not show any abrupt increase in leakage current up to the maximum test time of three hours, as indicated by the asterisk symbols in Figure 4.14. The TEM cross-section shown in Figure 4.27 shows voiding at the SiC(N) capping layer above the Cu anode. The structural damage in the capping layer led to the fluctuation of leakage current recorded during the constant voltage stress. The capping layer damage could be one of the factors leading to the catastrophic dielectric breakdown.

Figure 4.26 Soft breakdown TDDDB failure mode whereby Ta migration into the SiOCH low- k dielectric was seen in addition to the Cu diffusion near the delaminated SiC(N)/SiOCH interface, at the anode terminal, as observed in (a) S1 and (b) S2 structures.

Figure 4.27 Structural damage in the SiC(N) capping layer observed above the Cu anode terminal.

4.4 Delamination-induced Breakdown Mechanism

4.4.1 Driving forces of delamination

There are several driving forces which could cause delamination in a multi-layered thin film stack. They are stress levels in the films (which includes intrinsic stress due to deposition parameters and residual stress generated from thermal expansion mismatch), thickness of the film, presence of crack nucleation sites and poor film adhesion [114]. From finite element simulations reported in [109], shear stresses at the Cu corners which developed from CTE mismatch is dominant along the 45° direction and not along the

interfaces. Therefore, the tendency for shear stress-induced interface delamination is unlikely and thus, the quality of interface adhesion becomes the main determining factor for the occurrence of delamination.

Four point bend adhesion tests were then carried out to determine the interfacial adhesion strengths of the four main interfaces present in the interconnect scheme used, which are SiOCH/USG, USG/SiC(N), SiC(N)/SiOCH and Cu/SiC(N). The general load-displacement trends for the interfaces are shown in Figure 4.28. The load, P , was read at the circled points shown in the graph, a point at which a drop in load occurs or at the start of the plateau region. Equation 4.1 is then used to calculate the critical strain energy release rate, G_c . A summary of the calculated G_c is plotted in Figure 4.29. It can be seen that the SiC(N)/SiOCH interface exhibits the lowest G_c followed by SiOCH/USG interface. This suggests that debonding at interfaces with SiOCH low- k dielectric is most likely to occur.

Figure 4.28 Load-displacement trends obtained after four point bend test for the four main interfaces in an interconnect structure. The circled points are loads considered in the calculation of critical strain energy release rate.

Figure 4.29 Interfacial adhesion energies of the four main interfaces in the interconnect measured by four point bend adhesion test.

Figure 4.30 illustrates the extent of delamination at the SiC(N)/SiOCH interface in the structures, which was summarized from the cross-sectional TEM taken at the horizontal and vertical directions. It is clear that the delamination will only occur with the presence of a cathode terminal, which means that the applied electric field is the driving force for delamination to occur. Moreover, according to Lorentz relation, the molecules in a dielectric will experience a local field that is higher than the applied field due to contributions from polarization of the dielectric surrounding the molecules. Thus, the local field at the delaminated region (i.e. at the SiC(N)/SiOCH interface) is higher than the applied field, due to the high dielectric constant of the SiC(N) cap. This further alleviates the bond breaking at the already weak interface. Hence, the delamination is caused by a field-enhanced thermal process as described in the thermochemical E model, whereby the dipole-field coupling results in lower activation energy that is required to thermally break a bond, as described in equation 2.11. In addition, the theory of electrons having sufficient energy gained from the field and thus causing damage, proposed in the

electron impact damage model, could also result in the bond breakage leading to delamination.

Figure 4.30 Top down schematic of the extent of delamination at SiC(N)/SiOCH interface (shaded) summarized from physical analyses for (a) S1 and (b) S2 structures.

In addition to the electric field effect, leakage through the capping layer as well as through the IMD could catalyze the bond breakage leading to delamination. It was reported that hole capture serves as a catalyst for thermochemical bond breaking at fields ranging from 8 – 12 MV/cm (i.e. called hole-assisted thermochemical bond breaking) [74, 115]. The delamination found after voltage ramp occurred at applied fields more than 5 MV/cm. Moreover, the fields experienced by S1 and S2 structures are in fact higher than 5 MV/cm due to electric field enhancement, which will be explained later. Therefore, it is likely that the delamination occurs through a hole-assisted thermochemical bond breaking. It also explains the reason for delamination occurring at the anode terminal since energetic holes are generated near the anode terminal.

From the field acceleration parameter obtained from TDDB tests, the calculated effective molecular dipole moment, p_{eff} , using equation 2.12 was found to be 7.05 eÅ and 4.21 eÅ for S1 and S2, respectively. This is close to the $p_{\text{eff}} = 7.00$ eÅ reported for a hole-captured silicon-oxygen bond, whereby a hole (from the leakage current) capture by the silicon-oxygen bond reduces the amount of energy required to thermally break the bond [74]. This further substantiates the fact that bond breaking in both the SiC(N)/SiOCH and

SiOCH/USG interfaces are catalyzed by hole capture near the Cu anode, due to sweeping of free electrons (or leakage) into the Cu anode terminal during an applied bias. The hole capture further weakens the bond strength that was already reduced by the dipole-field coupling.

However, Cu diffusion was observed after TDDB, in addition to the delamination. The introduction of Cu ions into the dielectric could have resulted in the slightly lower p_{eff} value observed (especially for S2 whereby $p_{\text{eff}} = 4.21 \text{ e\AA}$) as compared to the one reported in the literature. Therefore, the Cu ions generated at the anode could be an additional driving force for delamination to occur besides the hole-assisted thermochemical bond breaking, during a constant voltage stress. Furthermore, a smaller extent of delamination was observed after TDDB as compared to that after voltage ramp. The smaller extent of delamination was expected since a field less than 5 MV/cm was used for the constant voltage stress. The observation of Cu diffusion after TDDB stress also implies that the failure mechanism after voltage ramp and TDDB is likely different due to the stress time and applied voltage range.

So far, delamination has not been observed in comb structures and thus it is possible that the delamination is specific to S1 and S2 structures. This is because the activation energies, E_a , derived from TDDB Weibull plots for S1 (0.23 eV) and S2 (0.20 eV) structures are lower as compared to that of comb structures (0.44 eV). The E_a for comb is similar to that reported for silica-based low- k dielectrics [116]. Therefore, the E_a could be related to ease of delamination at the SiC(N)/SiOCH interface, whereby a lower E_a corresponds to an easier delamination. To support this proposition, the adhesion strength has been reported to be lower when the delamination direction is parallel to the comb

lines (as in the case for S1 and S2 structures) as compared to the delamination direction that is orthogonal to the comb lines [117].

Moreover, the S1 and S2 structures experience an electric field enhancement due to the end of line and corner effects, as shown in Figure 4.31. The maximum electric field, $E_{\max}$, was simulated to be 1.59 times (for S1) and 1.90 times (for S2) higher than the nominal applied field, E_{nom} . The nominal field is obtained by dividing the applied voltage by the minimum distance between the Cu lines. Since the delamination is driven by electric field, the delamination in S1 and S2 structures become easier as compared to the comb structures due to the electric field enhancement. Besides the electric field enhancement, the density of Cu lines may affect the ease of delamination. There are many parallel Cu lines in the comb structure as compared to just a single pair of lines in the S1 and S2 structures, thereby making it difficult for delamination to occur in comb structures because of the constrain imposed by its adjacent lines.

Figure 4.31 Electric field simulation of (a) S1 and (b) S2 structures, illustrating electric field enhancements at the end of line and corners.

4.4.2 Leakage current investigation by electrostatic discharge (ESD) pulse

As mentioned, the main purpose of the electrostatic discharge (ESD) pulse is to control the severity of the failure. After application of at least two ESD pulses, delamination was observed at the SiC(N)/SiOCH interface, similar to failure mode II observed after voltage

ramp and constant voltage stress. Furthermore, the delamination was found to occur at the Cu terminal that experienced a higher ESD potential, regardless of whether a positive or negative pulse was applied to the same Cu electrode. This is illustrated in Figure 4.32. This further supports the V-ramp failure analysis results whereby delamination was consistently observed at the anode terminal. Moreover, the delamination extent was found to be dependent on the number of ESD pulses. As the number of pulses increased from 2 to 6, the delamination widened and extended towards the low- k dielectric as illustrated in Figure 4.33(a) and (b). Ultimately, after a critical number of pulses, a catastrophic thermal breakdown occurred as illustrated in Figure 4.33(c).

Figure 4.32 Delamination occurred at the (a) Cu anode terminal after +250 V and 6 ESD pulses were applied to the anode while it occurred at the (b) Cu cathode terminal after -250 V and 6 ESD pulses was applied to the anode.

Figure 4.33 Varying extent of delamination or failure severity after (a) 2 ESD pulses, (b) 6 ESD pulses and (c) 8 ESD pulses at the Cu anode terminal after a +250 V was applied.

Figure 4.34 shows the leakage current measured after varying number of ESD pulses was applied. Note that for the leakage measurements, the maximum voltage ramped is 100 V, whereby delamination was only observed at voltages higher than 150 V as demonstrated in sub-section 4.3.1 previously. Thus, the delamination observed is a result of the ESD pulse and not caused by the V-ramp performed for the leakage measurements. The anode leakage current (I_A) and cathode leakage current (I_C) were observed to increase by at least an order of magnitude after 2 ESD pulses and increased even further with a higher number of ESD pulses. This corresponds with the failure analysis results that show an extension of the delamination with higher number of pulses. Thus, it can be deduced that a larger delamination area led to a higher leakage current. However, the leakage current increase saturated after 4 ESD pulses. It could be an indication that a catastrophic burn was about to occur since a catastrophic burn was observed after 8 ESD pulses.

Figure 4.34 (a) Leakage current measured at the anode and (b) absolute leakage current at the cathode with varying number of positive ESD pulses.

Interestingly, the anode leakage current detected after the +250 V ESD pulses, flowed in the negative direction at voltages below 25 V (~ 0.83 MV/cm), and switched back to the normal positive direction after 25 V (Figure 4.35). Conversely, the cathode leakage current remained in the normal negative direction throughout the V-ramp as shown earlier.

Furthermore, the magnitude of the reverse anode current increased as the number of pulses increased. As a first conjecture, this could mean that the extended delamination at the anode terminal is attracting more electrons to the delaminated region which is filled with trap sites (presumably acceptor sites) created by the dangling bonds. Revisiting equation 2.3, the intercept of the graph of $\ln (J/E)$ versus $\sqrt{E}$ is

$$\left[\ln \left(q\mu \frac{N_c(N_d - N_a)}{2N_a} \right) - \frac{q\Phi_{PF}}{\xi k_B T} \right].$$

It can be seen that the intercept term is related to the density of states as well as the density of donor and acceptor sites. Hence, it can be deduced that the increase in the reverse anode current with higher number of ESD pulses is due to increased density of traps. This is caused by the widening of the delamination region.

Figure 4.35 Leakage current at the anode terminal plotted on a linear scale which emphasizes the negative current at $V < 25$ V after +250 V ESD pulses.

4.4.3 Proposed delamination-induced leakage mechanism prior to breakdown

A delamination-induced leakage mechanism is proposed with analyses from V-ramp and additional observations from the ESD tests. The phenomenon of reverse anode leakage current is first discussed with the help of band diagrams drawn for the region surrounding

the Cu anode terminal. After the ESD pulse, a delamination at the anode is initiated, which gives rise to positively charged traps. As a result, an internal electric field is built in the opposite direction to the externally applied field. The external field direction is from the Cu anode to the SiC(N) cap above, as shown in the circled region in Figure 4.36.

Figure 4.36 Electric field vector distribution for 0.30 μm metal spacing after 100 V stress.

Thus, at low applied fields, the electrons are swept through the SiC(N) cap and towards the delaminated region (i.e. at the SiC(N)/SiOCH interface) as shown in the energy band diagram at the bottom of Figure 4.37. However, at higher applied fields, the internal field is overcome by the externally applied field and therefore leading to leakage. This is illustrated in the band diagram at the top of Figure 4.37. The leakage conduction mechanism is by P-F emission near the delaminated interface as deduced from the leakage curves in sub-section 4.2.2.

Figure 4.37 Band diagrams depicting the trapping of electrons at the positively charged traps at the delaminated site (at low electric fields) and detrapping of electrons through Pool-Frenkel emission at higher electric fields.

One of the main leakage paths is believed to be the SiC(N) capping layer. This could be inferred from the catastrophic burn that is located at the upper half of the dielectric in between the Cu terminals, i.e. near the capping layer, as seen in the comb structures (Figures 3.16 – 3.18) and S1 test structures (Figure 4.23). A possible reason for the higher leakage in the capping layer is due to the smaller energy band gap of SiC(N) as compared to SiOCH low- k dielectric and USG. The energy band gaps reported in the literature for SiC-based dielectric and SiC(N) range from 3.68 eV to 4.5 eV [118, 119]; 3.55 eV to 6.33 eV for carbon-doped low- k dielectrics [120] and 9 eV for USG [121, 122]. Therefore, the electrons would more likely flow in the SiC(N) capping layer which has a lower barrier height to overcome, assuming that the Fermi level of Cu is in the middle of the dielectric band gap. Furthermore, SiC(N) films were found to be electrically unstable due to build-

up of charges in the film even at room temperature and current injection into the film at electric fields as low as 0.4 MV/cm [123].

The injection of electrons into the SiC(N) capping layer is shown as point 1 to 2 in the quasi-three dimensional band diagram in Figure 4.38(a). Then, from point 2 to 3, the electrons slide through the potential gradient across the Cu anode and cathode. At this point, although the leakage occurs dominantly through the SiC(N) capping layer, leakage could also occur at the interfaces of the SiC(N) capping layer with USG and SiOCH. Next, the trapping and detrapping of electrons at points 3 and 4, respectively, occurs as explained previously. Figure 4.38(b) displays a schematic diagram of the leakage flow through the SiC(N) capping layer.

Figure 4.38 (a) Band diagram and (b) schematic diagram of the proposed current leakage path leading to dielectric breakdown in the Cu/low-k interconnect when an interfacial delamination is present.

4.4.4 Qualitative description of delamination-induced breakdown mechanism

The delamination-induced breakdown mechanism in the Cu/SiOCH low- k interconnects, as deduced from the voltage ramp and constant voltage stress analyses, as well as the ESD analysis, is summarized here. The driving force for delamination at the SiC(N)/SiOCH interface is the applied field coupled with hole capture during the electrical stress whereby the mechanism of delamination was proposed to be a hole-assisted and field-enhanced thermochemical bond breaking. Moreover, the delamination will take place at the interface with the weakest adhesion strength, as verified by the four point bend adhesion test. From the ESD experiments, it was deduced that the main leakage path is through the bulk SiC(N) capping layer as well as along its adjacent interfaces. This resulted in the extension of delamination at the SiC(N)/SiOCH interface and eventual damage in the SiC(N) capping layer when the sample is electrically stressed at a higher voltage (in voltage ramp) or for a longer time (in TDDB stress).

In addition to the delamination extension and damage after voltage ramp or TDDB stress, Cu particles were found after TDDB stress. Therefore, Cu diffusion through the structurally damaged capping layer towards the delaminated interface could be an additional driving force for delamination to occur under constant voltage stress conditions. From this observation, the failure mechanism after TDDB and voltage ramp is demonstrated to be different. This makes the voltage ramp to TDDB correlation poor for Cu/low- k dielectric systems, unlike the case for gate oxide whereby voltage ramp data can be converted to TDDB data and thus reduces the test time to evaluate the oxide integrity.

In conclusion, the delamination at interfaces with SiOCH low- k dielectric is the main factor initiating the interconnect dielectric breakdown. After prolonged electrical stress at a constant voltage (i.e. TDDB tests), the delamination widens and eventually leads to the

catastrophic dielectric breakdown. Moreover, structural damage in the capping layer and Cu diffusion through the damaged capping layer are additional factors that would accelerate the breakdown process.

4.5 Mechanism of Ta Migration from the Anode Sidewall

4.5.1 Electric field as the driving force of Ta migration

The Ta migration characteristics as observed in section 4.3 are believed to be electric field driven. First of all, the observed directions of Ta migration from physical analysis (summarized in the top down schematic diagrams in Figure 4.39(a) and (b)) coincide with the simulated electric field vector lines shown in Figure 4.39(c) and (d) for S1 and S2 structures, respectively. Moreover, Ta was observed to migrate more near the upper and lower corners due to electric field enhancement at the corners, as illustrated in Figure 4.40. However, Ta migration is more likely at the upper corners as observed in the S2 structures. An obvious reason would be the slightly shorter inter-metal distance at the top of the Cu trench due to the sloped profile, which resulted in a higher electric field. Another probable contribution is an electric displacement field, D , enhancement (i.e. also called electric flux density). As described in equation 4.2 for linear materials [72], a higher D is a result of a higher dielectric constant, ϵ (or k). Therefore, the D enhancement is contributed by the SiC(N) capping layer and USG buried capping layer, which have higher dielectric constants as compared to the low- k dielectric.

$$D = \epsilon_o E + P = \epsilon_o E + \chi \epsilon_o E = \epsilon E \dots\dots\dots (4.2)$$

Where E is the applied electric field, P is the polarization in the dielectric induced by the electric field, χ is the dielectric susceptibility, ϵ is the dielectric constant and ϵ_o is the permittivity of free space.

Figure 4.39 Top down schematic of Ta migration (cross-hatched) summarized from physical analyses for (a) S1 and (b) S2 and corresponding electric field distribution simulated for (c) S1 and (d) S2 structures.

Figure 4.40 Electric field simulation at the cross-section of the interconnect system, illustrating higher electric fields at the upper and lower corners of the Cu trench.

As mentioned in the earlier sections, the reason for the leakage step in the I-V leakage mode III and pseudo-leakage observed in constant voltage test will be explained here. From physical failure analysis, Ta migration is always observed when the leakage curves contain a leakage step both in voltage ramp and constant voltage tests. As seen in Figure 4.41, the leakage step from voltage ramp consists of two regions, which are the leakage increase region and the leakage saturation region.

The leakage increase region is believed to be contributed mainly by electronic current. The electronic current is proposed to be caused by an increased electron injection from the cathode due to lowering of potential caused by the Ta ions that drifted and diffused into the dielectric, as shown schematically in Figure 4.42(a). As the Ta ions migrated further into the dielectric, more electrons were injected into the dielectric, resulting in the increase in leakage current. At higher temperatures, the onset of the leakage step was shifted to lower voltages. This means the onset of leakage increase caused by Ta ion migration became easier, which also implies that the Ta ionization became easier at higher temperatures. Moreover, the leakage current is higher at higher temperatures due to more Ta ions generated and more electron injection from the cathode terminal.

Subsequently, the leakage will reach a saturation region. The leakage saturation is likely caused by reduction in the amount of Ta ions migrating into the dielectric due to repulsion from existing Ta ions in the dielectric and / or neutralization of the Ta ions to form an oxide compound, as illustrated in Figure 4.42(b). At higher temperatures, the onset of saturation region was also shifted to lower voltages and thus, implying the formation of Ta oxide at lower voltages. It is also observed that the maximum leakage current in the saturation region did not vary significantly with temperature. This could indicate that there is a limited thickness of Ta oxide that can be formed. The Ta oxide

formation and the reason for saturation as well as the possibility of Ta ionization will be further substantiated in the next sub-section.

Figure 4.41 Leakage characteristics associated to Ta migration into the SiOCH low- k dielectric for (a) S1 and (b) S2 structures.

Figure 4.42 (a) Leakage increase as a result of an increased electron injection from the cathode due to potential lowering. (b) Leakage saturation due to neutralization of Ta ions and Ta oxide formation.

Figure 4.43 summarizes the electric field onset of leakage increase region's dependence on temperature for S1 and S2. As mentioned earlier, the electric field at which the leakage starts to increase decreases with an increase in temperature. However, further increase in temperature from 373K to 423K did not decrease the electric field onset further. Therefore, it is deduced that a minimum electric field is required to drive the Ta migration

from the anode sidewall barrier and into the SiOCH low- k dielectric. It is true that temperature alone will not drive the Ta migration since no migration was observed for unstressed samples that underwent the same heating temperature (maximum temperature applied is 150°C).

The minimum electric field required was found to be 2.67 MV/cm and 2.51 MV/cm for S1 and S2 respectively. The lower minimum field for S2 structures is suspected to be due to a larger field enhancement at the corners (1.90 times) as opposed to the terminated tips (1.59 times). Moreover, S2 requires a higher temperature activation as compared to S1. This agrees with the failure analysis results which showed less Ta migration for S2 as compared to S1. The likely reason is the different structure type of S1 and S2 which affects the dielectric etching and Ta deposition uniformity. Hence, Ta migration is electric field driven as observed from the electric field simulations, physical failures and leakage analyses.

Figure 4.43 Temperature dependence of the electric field at which the leakage starts to increase.

4.5.2 Thermodynamic and chemical reactivity considerations for Ta migration

It is not possible for atomic diffusion of Ta into the low- k dielectric at 20°C due to the low temperature condition and also small diffusion coefficient of Ta, considering its high melting temperature of 3017°C. Therefore, Ta needs to be ionized to be able to drift and diffuse into the SiOCH low- k dielectric with an applied electric field. An attempt to explain the possibility of Ta ionization will be discussed here. One such mechanism is the presence of oxygen in the dielectric which sets off the ionization of metal and subsequent drift into the dielectric with an applied field, proposed by a few independent authors. This was also mentioned in Chapter 2 about the driving force for Cu^+ ion diffusion into dielectrics. In references [33] and [124], the amount of charges injected into the dielectric correlated well with the heat of oxide formation, whereby more metal ions drift into the dielectric if the metal has a higher oxidation tendency or more negative heat of oxide formation. Their results show that the amount of charges/cm² entering the organosiloxane polymer follows the following order: $\text{Pt} < \text{Cu} < \text{Ta} < \text{Al}$. As seen in Table 4.2, Ta oxide has a higher formation tendency as compared to Cu oxide or Si oxide due to a higher negative heat of oxide formation, as well as a more negative Gibbs free energy.

Table 4.2 Standard thermodynamic properties of Ta, Al, Si and Cu oxides [125].

	Standard molar enthalpy (heat) of formation at 298.15K, ΔH_f° (kJ/mol)	Standard molar Gibbs energy of formation at 298.15K, ΔG_f° (kJ/mol)
Ta ₂ O ₅	-2046.0	-1911.2
Al ₂ O ₃	-1675.7	-1582.3
SiO ₂ (α -quartz)	-910.7	-856.3
Cu ₂ O	-168.6	-146.0
CuO	-157.3	-129.7

Therefore, Ta ionic drift and diffusion is made possible through the ionization of Ta due to contact with an oxygen source found in the SiOCH low- k dielectric. The source of oxygen could be extrinsically incurred or is inherent to the low- k dielectric. The oxygen could be present at the surface of the dielectric through various ways. It could originate from the moisture absorbed or defects created from plasma damage incurred during photoresist removal. The plasma damage was reported to increase the oxygen content at the low- k dielectric sidewalls directly adjacent to the Cu metal due to carbon depletion as mentioned in Chapter 2 [20, 21].

As observed from the TEM cross-sections, the Ta ionic drift and diffusion occurred initially at the upper and lower corners of the Cu trench. However, after higher temperature or longer stress time, the distance of migrated Ta was observed to saturate to an average thickness of 30 – 60 nm, which spreads uniformly across the anode sidewall barrier. This means that the Ta ionic drift and diffusion increases with voltage / time at the beginning but eventually saturates after a critical drift distance is reached. It is believed that a stable Ta₂O₅ is formed and further Ta ionic drift and diffusion is not possible. This is supported by another experiment described in [126] whereby the Ta ionic drift rate associated to the flat-band voltage shift, saturates with longer bias-temperature-stress (BTS) time. Furthermore, the phenomenon is analogous to the self passivation of Al metals when in contact with SiO₂. Ta also forms a stable and stoichiometric oxide when in contact with SiO₂. However, the SiOCH low- k dielectric has insufficient oxygen to form a dense and stable oxide layer with Ta. Therefore, the drift and diffusion of Ta ions further into the SiOCH low- k dielectric occurred until a dense and stable oxide layer is formed. This led to the leakage saturation region whereby the maximum leakage current did not vary with temperature. The maximum leakage is the

same regardless of temperature because the same amount of Ta ions is required to form the stable and stoichiometric Ta oxide.

In summary, migration of Ta is possible when in contact with a dielectric that contains oxygen and when an electric field is applied. The mechanism of Ta migration was explicitly illustrated in the band diagrams of Figure 4.42, whereby Ta ionic drift and diffusion occurs initially which increases the leakage current at the leakage step. At the same time, a non-stoichiometric Ta oxide is formed. The Ta ionic drift and diffusion as well as the formation of unstable Ta oxide continued until a dense and stable oxide is formed. At this point, the leakage current and the Ta migration region were observed to saturate. Moreover, The Ta ionization and Ta oxide formation occurred at a lower electric field when temperatures are increased.

4.6 TDDDB Degradation Mechanisms in Single Line and Corner Structures

A summary of the I-V leakage characteristics and its corresponding failure modes observed in single line and corners structures are shown in Table 4.3. It can be seen that the two main degradation mechanisms observed in single line and corners structures are delamination at the SiC(N)/SiOCH interface (Mode II) and Ta migration from the anode (Mode III). For Mode II, the delamination is driven by a hole-assisted and field-enhanced thermochemical bond breaking. The condition for delamination to occur is the weak interface adhesion strength. On the other hand, for Mode III, Ta migration is driven by Ta's oxidation tendency and also electric field. The condition for Ta migration to occur is the availability of oxygen molecules in the low- k dielectric.

The failure modes observed after voltage ramp and constant voltage stress are similar, except for the additional Cu diffusion observed and extent of Ta migration after a

constant voltage stress. As mentioned earlier, the additional Cu diffusion observed after constant voltage stress implies that the failure mechanism leading to breakdown is different after voltage ramp and TDDB stress. The Cu diffusion accelerated the breakdown process and therefore is an additional driving force for delamination to occur.

Table 4.3 Leakage characteristics and failure modes observed in single line (S1) and corner structures (S2).

	Voltage ramp		Constant voltage stress (TDDB)	
	I-V leakage characteristics	Failure mode	I-t leakage characteristics	Failure mode
Mode I	<ul style="list-style-type: none"> – Abrupt increase in current – May have leakage hump 	<ul style="list-style-type: none"> – Catastrophic burn and could include Mode II and III 	<ul style="list-style-type: none"> – Abrupt increase in current at breakdown 	<ul style="list-style-type: none"> – Catastrophic burn, upper half of Cu trench
Mode II	<ul style="list-style-type: none"> – Gentle increase and steep slope near breakdown – Poole-Frenkel emission during delamination 	<ul style="list-style-type: none"> – Delamination at SiC(N)/SiOCH interface and at anode – Occasional debonding at SiOCH/USG interface 		<ul style="list-style-type: none"> – Delamination at SiC(N)/SiOCH interface and at anode AND – Cu particles along delaminated region
Mode III	<ul style="list-style-type: none"> – Leakage hump 	<ul style="list-style-type: none"> – Ta migration from anode at top and bottom corners of trench – Delamination as in Mode II 	<ul style="list-style-type: none"> – Leakage step prior to abrupt increase in current 	<ul style="list-style-type: none"> – Ta migration from anode across whole trench – Delamination and Cu particles as in Mode II

Besides the different failure mechanism as a result of the different electrical test (i.e. voltage ramp and TDDB stress), there is also an influence of the interconnect layout on the failure mode and mechanism. Table 4.4 summarizes the failure modes, voltage ramp and TDDB parameters observed in the conventional comb structures, single line (S1) and corner (S2) structures. The factors that differ significantly are the failure mode observed and the TDDB activation energy (E_a) measured. As described in sub-section 4.4.1, the factors affecting the delamination are the delamination direction, electric field enhancement and density of Cu lines. These factors make delamination easier in S1 and S2 structures and therefore resulted in the lower TDDB activation energy measured.

In conclusion, this chapter shows that the S1 and S2 structures are able to reveal the possible failure modes and mechanisms that will occur in Cu/low- k interconnect systems although there is an influence from the interconnect layout on the failure mechanism. More importantly, interfacial adhesion strength and integrity of sidewall barrier as well as the quality of the low- k dielectric adjacent to the liner barrier are the two important factors that will affect the Cu/low- k dielectric reliability and therefore, should be taken into consideration during process integration of the low- k interconnects.

Table 4.4 Voltage ramp parameters, TDDB parameters and failure modes/mechanisms for comb, S1 and S2 structures.

Parameter	Comb	Single line (S1) / Corner (S2)	Remarks
Conduction mechanism	<1MV/cm: Ohmic >1MV/cm: Schottky	<5MV/cm: Ohmic >5MV/cm: P-F	Schottky emission with $k = 2.3$ in comb while P-F emission with $k = 1-2$ in S1 and S2
Nominal breakdown field (E_{BD})	3.6 – 7.9 MV/cm	S1: 3.3 – 6.6 MV/cm S2: 3.8 – 7.8 MV/cm	Similar E_{BD} range
Vramp temperature dependence	23 meV	S1: 19 meV S2: 27 meV	Similar temperature dependence as compared to Type 2 failure in Chapter 3
TDDB beta (β)	0.87 – 1.11	S1: 0.51 – 0.71 S2: 1.04 – 2.23	Slightly lower β for S1 but higher β for S2 compared to comb
TDDB field acceleration, gamma (γ)	2.22 cm/MV	S1: 2.19 cm/MV S2: 1.31 cm/MV	Similar field acceleration parameters
TDDB activation energy (E_a)	0.44 eV	S1: 0.23 eV S2: 0.20 eV	Lower E_a for S1 and S2
Failure mode/mechanism observed	Thermal dielectric breakdown initiating at the SiC(N) cap region	Thermal dielectric breakdown, delamination, Cu diffusion, Ta migration	Delamination is the main difference in failure mode observed and thus, the main cause for lower E_a observed

CHAPTER 5: STAND-ALONE COWP METAL CAP

5.1 Advantages of Stand-Alone CoWP Metal Capped Structures

It is known that Cu needs to be enclosed with metal barriers at the sidewall and bottom of the Cu line and protected at the top with a dielectric capping layer in order to prevent Cu diffusion into the surrounding low- k dielectric. However, it was shown from the previous chapter that delamination is likely to occur at the interface between the dielectric capping layer and the low- k dielectric, especially in interconnect layouts with terminated tips or corners. Moreover, the lower activation energy mainly contributed by the delamination will lead to a shorter projected TDDb lifetime. Therefore, a plausible alternative is to replace the capping layer with a self-aligned barrier (SAB) on Cu which eliminates the interface between the capping layer and low- k dielectric between the Cu interconnects.

The initial motivation for SAB is to maintain electromigration reliability in order to accommodate the increasing current density needs for future technology nodes. There are two ways to incorporate the SAB, which are by replacing the dielectric capping layer with a SAB or through a more complex bilayer stack (which keeps the capping layer). Comparing the two methods, the stand-alone SAB would be more beneficial in terms of intra-line capacitance due to the absence of a dielectric capping layer and thus, able to improve the RC delay at least by 5 to 12% [9, 10, 127]. Furthermore, stand-alone SAB is essential in CMOS image sensor applications whereby the absence of the SiN dielectric capping layer eliminates light reflectivity issues [128].

The SAB can be deposited via chemical vapor deposition (CVD) or electroless plating. Examples of CVD-based barriers examined are tungsten [5], Cu_xSi [6] and CuSiN [10], while Co(P) and CoWP are electroless-deposited [7, 8]. These barriers were shown to exhibit significant improvements in Cu electromigration lifetime, which is correlated to

the improvement in adhesion between a Cu-metal barrier as compared to a Cu-dielectric barrier [129]. The improved adhesion with Cu also improves the breakdown strength due to less occurrences of Cu diffusion and Cu extrusion at the CMP interface [93]. In addition, the metal cap barriers such as CoWP have good diffusion barrier properties due to solute effects of W and P blocking Cu diffusion along the grain boundaries [130]. Extensive investigation and development has also been performed so that the line resistance is not compromised by the metal cap barriers. However, in terms of the TDDB reliability of interconnects with metal cap barriers, not much has been studied. Therefore, in view of the importance of stand-alone and self-aligned barriers in achieving the desired interconnect performance and reliability, CoWP-capped structures are investigated and presented in this chapter.

5.2 Test Structures and Test Conditions

Three cap splits: conventional SiN dielectric cap, 20 nm-thick CoWP and 40nm-thick CoWP metal cap at the metal 2 (M2) level were studied. The IMD and ILD used were both SiO₂. The comb test structures used were the asymmetric and symmetric comb lines. The asymmetric structures contain a via on alternate comb lines as shown in Figure 5.1(a) by the dotted lines. These lines with the via were stressed with a negative voltage while the lines without the via which are at the M2 level were stressed at a positive voltage. Figure 5.1(b) and (c) shows the cross-section of the asymmetric comb structure. The metal spacing used was 0.14 μm and 0.18 μm as highlighted in the figure. Voltage ramp with a ramp rate of 1 V/s and at temperatures 20°C, 100°C and 150°C was performed on these asymmetric structures. Breakdown voltage, V_{BD} , was defined at the point where an abrupt increase or drop in leakage current occurred while the breakdown field strength, E_{BD} , was obtained by dividing V_{BD} with the measured metal spacing.

Figure 5.1 (a) Top view schematic diagram of the asymmetric comb structure whereby the lines with vias are represented by the dotted lines. (b) TEM cross-sections of the structure with conventional SiN dielectric cap and (c) CoWP metal cap.

Figure 5.2 (a) SEM top view layout of the symmetric comb structure describing the locations of vertical and horizontal spacing. (b) Schematic diagram of the cross-sections illustrating Cu interconnects with conventional SiN dielectric cap and (c) CoWP metal cap.

On the other hand, TDDB studies were done on the symmetric structures which consist mainly of cornered tips as shown in the SEM image in Figure 5.2(a). The metal lines are at the M2 level. The vertical spacing between the Cu lines was fixed at 0.28 μm but the horizontal spacing between the tip and corner was varied. The horizontal distances used were 0.28 μm and 0.30 μm . Figure 5.2(b) and (c) shows the cross-section of the symmetric structures with SiN dielectric cap and CoWP metal cap, respectively. Wafer-level voltage ramp and package-level constant voltage tests were conducted on these symmetric structures. Voltage ramp was performed at a ramp rate of 1 V/s. Meanwhile,

the structures were stressed at a field of 4 MV/cm and at oven temperatures as shown in Table 5.1 for package level TDDB. The failure criterion for the constant voltage tests was defined when the current level reaches 10 μA .

Table 5.1 Constant voltage test temperatures used for the symmetric comb structures.

Capping layer	Oven temperature			
	100°C	130°C	150°C	180°C
SiN dielectric cap	X		X	X
CoWP metal cap		X	X	X

5.3 Electrical Characterization Results

5.3.1 Leakage and conduction mechanisms

The leakage characteristics of SiN-capped and CoWP-capped structures are shown in Figure 5.3, and behave similarly for both asymmetric and symmetric comb structures. It can be seen that the leakage for CoWP-capped structures were comparable to SiN-capped structures at fields <2.5 MV/cm and lower than SiN-capped structures at fields >2.5 MV/cm.

Figure 5.3 I-V leakage characteristics for interconnect structures with SiN, 20 nm-thick CoWP and 40 nm-thick CoWP cap stressed at 100°C for (a) asymmetric (0.14 μm spacing) and (b) symmetric (0.28 μm spacing) comb structures.

The conduction mechanism found for both the asymmetric and symmetric SiN-capped comb structures is similar to that reported in [45]. Ohmic, Schottky and P-F conduction were found to occur in the SiN-capped structures at increasing applied fields. At low electric fields, Ohmic conduction occurred. A Schottky emission into the interface between the SiO₂ dielectric and SiN cap was observed at electric fields higher than 2.4 MV/cm with calculated k value of 4.23 for both 0.14 μm and 0.18 μm metal spacing, as shown in Figure 5.4(a).

At fields higher than 3.4 MV/cm, P-F emission is predicted to be in the SiN capping layer, near the SiN/SiO₂ interface, with calculated k value of 6.81, as shown in Figure 5.4(b). However, at 100°C, the calculated k value dropped to about 4.77 for symmetric structures and an average of 4.63 for asymmetric structures. This implies that P-F emission occurred both at the SiN capping layer as well as at the adjacent interfaces (i.e. SiN/SiO₂). The occurrence of P-F emission indicates the presence of a large density of traps and is likely contributed by the interfacial traps at the dissimilar SiN/SiO₂ interface as compared to CoWP-capped structures with only similar SiO₂/SiO₂ interfaces. The higher leakage current contributed by dissimilar interfaces has been demonstrated before for carbon-doped oxides with SiN capping layers as compared to SiC capping layers [48, 131]. However, it cannot be ruled out that the higher leakage and P-F emission observed could also be contributed by the bulk SiN capping layer. It was reported in references [132, 133] that the SiN dielectric conducts by P-F emission.

On the other hand, neither Schottky emission nor the P-F emission accurately fit the CoWP-capped structures. There is a possibility that the leakage is caused by electron hopping in the dielectric. Since P-F emission was not observed, thus it can be said that

CoWP-capped structures have insignificant trap density due to absence of interfacial traps originating from the dissimilar SiN/SiO₂ interface.

Figure 5.4 (a) Schottky emission and (b) Poole-Frenkel emission in SiN-capped asymmetric comb structures with 0.14 μm metal spacing and stressed at 20°C.

5.3.2 Breakdown strength performance in asymmetric comb structures

A Weibull plot of the E_{BD} for the three cap splits with 0.14 μm metal spacing and stressed at room temperature is shown in Figure 5.5. Clearly, the CoWP-capped structures showed a higher E_{BD} as compared to the SiN-capped structure. Moreover, the thicker CoWP-capped structure exhibited a slightly lower E_{BD} as compared to the thinner CoWP-capped structure as will be discussed later.

Figure 5.5 Breakdown field strength of SiN-capped and CoWP-capped structures for 0.14 μm metal spacing and stressed at 20°C.

However, the E_{BD} for CoWP-capped structures became almost comparable and even lower than SiN-capped structures when subjected to higher temperatures as shown in Figure 5.6. Note that the data points for 20 nm-thick CoWP and 40 nm-thick CoWP were intentionally shifted to the right for a clearer view. Furthermore, it can be seen that the E_{BD} for 20 nm-thick CoWP and 40 nm-thick CoWP-capped structures degrade more rapidly with temperature as compared to the SiN-capped structure regardless of metal spacing. In other words, the failure mechanism of CoWP-capped structures is more dependent on temperature as compared to that of SiN-capped structures.

Figure 5.6 Effects of temperature on the breakdown field strength for SiN dielectric cap and CoWP metal cap at (a) 0.14 μm and (b) 0.18 μm metal spacing.

5.3.3 TDDB lifetime performance in symmetric comb structures

From the TDDB leakage current curves shown in Figure 5.7, most of the CoWP-capped structures exhibited anomalous and fluctuated increase in leakage up to the failure current at 10 μA , akin to the soft breakdown phenomena observed for SiO_2 gate oxides. This is unlike the SiN-capped structures, whereby only the stress-induced leakage current (SILC) was observed. Although most of the CoWP samples exhibited fluctuated and leaky currents, there are a few which showed SILC whereby the leakage was found to be at similar levels or even up to an order of magnitude lower than SiN-capped structures at the

same applied voltage. This implies that the density of existing traps or stress-generated traps in the IMD for CoWP-capped structures are less than that in SiN-capped structures.

Figure 5.7 General TDDDB leakage current trends for interconnect structures with SiN dielectric cap, 20 nm-thick CoWP and 40 nm-thick CoWP metal caps.

Furthermore, the time-dependent dielectric breakdown was improved by about 15% (equivalent to about 1 decade of increase) when 20 nm-thick CoWP metal cap is used instead of the conventional SiN dielectric cap as illustrated in the Weibull plots of Figure 5.8(a) and (c). However, the improvement became marginal at higher temperatures, similar to the breakdown field strength behavior observed for asymmetric comb structures after voltage ramp. In spite of that, its time-to-failure remained comparable to SiN-capped structures as shown in Figure 5.8(b) and (d).

In addition, a bimodal distribution was observed for 40 nm-thick CoWP-capped structures and a minority of 20 nm-thick CoWP-capped structures, whereby a small number of samples (which are circled in the graphs) exhibited short time-to-failures while the rest had comparable or longer time-to-failures as compared to that of SiN-capped structures.

These so-called early failures could be due to Co contamination deposited during plating because the dielectric surface is also exposed to the plating solution. Early failures leading to low breakdown voltages which was attributed to Co contamination were also inferred in similar symmetric comb structures [128]. Moreover, the loss of selectivity was reported to increase with the thickness of CoWP deposited [134], which explains the higher occurrence of early failures for 40 nm-thick CoWP as compared to 20 nm-thick CoWP-capped structures. This could also explain the slightly shorter overall time-to-failures of 40 nm-thick CoWP-capped structures as compared to 20 nm-thick CoWP-capped structures.

Figure 5.8 Weibull plots of TDDb times-to-failure, taken at failure criterion: 10 μ A, for SiN and CoWP-capped structures with the following metal spacing and temperatures: (a) 0.28 μ m, 150°C (b) 0.28 μ m, 180°C (c) 0.30 μ m, 150°C and (d) 0.30 μ m, 180°C.

From the variation of times-to-failure with temperature extracted at 63.2% percentile, CoWP-capped structures exhibited TDDB thermal activation energy, E_a , almost two times larger than that for SiN-capped structures (Figure 5.9). The E_a for SiN-capped structures are 0.47 eV – 0.58 eV for 0.28 μm and 0.30 μm spacing, while the E_a for CoWP-capped structures ranged from 0.84 eV – 0.96 eV for 20 nm-thick CoWP and 0.66 eV – 0.88 eV for 40 nm-thick CoWP, as summarized in Table 5.2. By excluding the early failures for 40 nm-thick CoWP-capped structures, the E_a calculated was slightly lower compared to 20 nm-thick CoWP-capped structures, which will be discussed in section 5.5. On the other hand, the vast difference in E_a between SiN and CoWP-capped structures imply a difference in TDDB degradation mechanism. A comparison of the E_a and failure mechanism is described in section 5.5.

Figure 5.9 Arrhenius plot of times-to-failure at 63.2% for interconnect structures with SiN, 20 nm-thick CoWP and 40 nm-thick CoWP caps at an electric field of 4 MV/cm, for (a) 0.28 μm metal spacing and (b) 0.30 μm metal spacing.

Table 5.2 TDDB thermal activation energy for SiN, 20 nm-thick CoWP and 40 nm-thick CoWP-capped structures conducted at electric field of 4 MV/cm.

Metal spacing (μm)	TDDB thermal activation energy at 4 MV/cm (eV)		
	SiN	20 nm CoWP	40 nm CoWP
0.28	0.47	0.84	0.66
0.30	0.58	0.96	0.88

5.4 Physical Failure Analysis

Several burn marks were observed both in SiN-capped and CoWP-capped structures after voltage ramp and TDDDB stresses as shown in the optical images of Figure 5.10 and Figure 5.11, respectively. Cross-sections were performed near the burn marks to observe the probable failure initiation locations in the interconnect structure which led to the catastrophic breakdown. As seen in Figure 5.12 for SiN-capped structures, the initial site of failure is most likely the SiN capping layer near the CMP surface. The SiN capping layer was seen to be completely damaged. This was similarly observed in comb structures with SiC-based capping layer with carbon-doped oxide in the previous chapters.

Figure 5.10 (a) Optical image of the asymmetric structure after voltage ramp stress illustrating burn marks and (b) SEM top view of the burn marks after delayering.

Figure 5.11 Optical images of the burn marks observed after TDDDB stress in (a) SiN-capped and (b) 20 nm-thick CoWP-capped structures. The short lines drawn indicate cross-section sites.

Figure 5.12 SiN capping layer damage observed in (a) asymmetric structures after voltage ramp and (b) symmetric structures after TDDDB stress, is the likely origin of the catastrophic breakdown in SiN-capped structures.

CoWP-capped structures also showed burn marks at the CMP interface but at the interface between the SiO₂ IMD and the SiO₂ ILD (Figure 5.13). This is expected due to the shorter distance between interconnect lines at the top and weaker strength of the interface although it is an interface between the same dielectric. Moreover, Cu and some Co diffusion along this interface were observed as confirmed by EDX analyses performed at the circled locations, as shown in Figure 5.14. The atomic percent of Co relative to Cu was found to be higher in 40 nm-thick CoWP as compared to 20 nm-thick CoWP-capped structures, as shown in the inset of Figure 5.14.

Figure 5.13 Burn at the SiO₂/SiO₂ interface and metallic diffusion along the interface for (a) 20 nm-thick CoWP and (b) 40 nm-thick CoWP-capped structures.

Figure 5.14 Energy dispersive X-ray point analyses at (a) point 1 for 20 nm-thick CoWP and at (b) point 2 for 40 nm-thick CoWP-capped structures. The table in the inset shows the atomic percent of the elements detected.

On the other hand, for early failures of 40 nm-thick CoWP-capped structures, Co extrusions from the corners of the trench are observed. This is likely due to high stress concentrations at the top corners, similar to that discussed in Chapter 3. The atomic percent of Co was found to be higher or at least more than 10 at% as compared to Cu in the early failure samples, as shown in Figure 5.15. EDX was performed at the white circled region shown in the inset of Figure 5.15(a) and the atomic percent for the K peaks are tabulated in Figure 5.15(b). A small amount of phosphorus (P) was also detected. This implies that Co and P extruded into the SiO₂, leading to failure of the CoWP diffusion barrier and thereby allowing Cu out-diffusion into the SiO₂ dielectric.

In addition, an EDX analysis was performed at the CMP surface, whereby the intra-metal SiO₂ and inter-level SiO₂ meet, to check for any Co contamination. EDX was conducted on the region circled in black as shown in Figure 5.15(a) for 40 nm-thick CoWP sample that failed early and on another sample that have a longer time-to-failure. As shown in Figure 5.16, a small atomic percentage of Co was found in the sample that failed early. Therefore, Co contamination at the CMP surface is no doubt the main reason for the early failures. The low EDX counts collected for Co contamination is probably due to the

minute amounts of Co that could be detected from a very thin TEM sample. Also note that the Cu-K signal came from the Cu grid used to hold the TEM samples.

Figure 5.15 (a) Burn near the $\text{SiO}_2/\text{SiO}_2$ interface and Co and Cu diffusion at the Cu trench corners for 40 nm-thick CoWP-capped structures with early failure. (b) EDX spectrum of the region highlighted by the white circle, indicating more Co diffusion than Cu.

Figure 5.16 EDX analyses conducted at the $\text{SiO}_2/\text{SiO}_2$ interface with the atomic percent of elements tabulated respectively for 40 nm-thick CoWP samples that exhibit (a) long time-to-failure compared to (b) samples that exhibit early failure.

5.5 TDDDB Degradation Mechanism with Stand-Alone CoWP Metal Cap

A summary of the voltage ramp parameters, TDDDB parameters and failure modes are presented in Table 5.3. As observed from the table and in Figure 5.8, CoWP-capped structures show improvement in breakdown fields as well as times-to-failure as compared to SiN-capped structures. Although these properties of CoWP-capped structures degrade more rapidly with temperature, they remain comparable with SiN, at least up to 180°C. There were a few early failures, especially for 40 nm-thick CoWP-capped structures, which were attributed to Co contamination at the SiO₂/SiO₂ interface due to increased loss of selectivity with thicker CoWP deposition. The Co contamination could also explain the slightly lower breakdown strength and shorter time-to-failure for 40 nm-thick CoWP as compared to 20 nm-thick CoWP-capped structures. This was also reflected in the slightly lower TDDDB thermal activation energy of the thicker CoWP-capped structures. Despite the Co contamination and selectivity issue, the TDDDB activation energies for CoWP-capped structures remain much higher than that for SiN-capped structures.

Table 5.3 Voltage ramp parameters, TDDDB parameters and failure modes/mechanisms for SiN-capped and CoWP-capped structures.

Parameter	SiN-capped	CoWP-capped	Remarks
Conduction mechanism	<2.4MV/cm: Ohmic >2.4MV/cm: Schottky >3.4MV/cm: P-F	Possibility of electron hopping in dielectric	Schottky and P-F emission in SiN-capped structures mainly at SiN/SiO ₂ interface
Nominal breakdown field (E_{BD})	1.5 – 8.4 MV/cm	20nm: 3.0 – 10.0 MV/cm 40nm: 2.2 – 9.0 MV/cm	Similar E _{BD} range
TDDDB beta (β)	0.65 – 2.13	20nm: 0.61 – 1.01 40nm: 0.67 – 0.94	Similar spread of time-to-fails
TDDDB activation energy (E_a)	0.47 – 0.58 eV	20nm: 0.84 – 0.96 eV 40nm: 0.66 – 0.88 eV	Higher E _a for CoWP-capped structures
Failure mode/mechanism observed	Thermal dielectric breakdown at the SiN cap	Thermal dielectric breakdown at SiO ₂ /SiO ₂ interface; Co and Cu diffusion	Different failure mechanism observed

Since the main difference between the SiN-capped and CoWP-capped structures is the SiN capping layer, it is the main cause of TDDDB degradation for SiN-capped structures. This was also verified from the failure mode observed, which is a thermal dielectric breakdown initiating at the SiN cap. There are two factors that can result in the poorer dielectric performance for SiN-capped structures. First, is the weaker adhesion strength between SiN dielectric cap and Cu as compared to the adhesion strength between the CoWP metal cap and Cu. The adhesion strength with Cu may play a role in the ease of extrusion and thus have an influence on the breakdown strength as reported in [93]. However, the extrusions at 45° to Cu surface are usually related to early failures. This has been established in Chapter 3 (compare Type 1 failure mode with Type 2 failure mode). Moreover, a similar extrusion is observed for the early failure samples in 40 nm CoWP-capped structures (Figure 5.15). Therefore, Cu extrusion is not the failure mechanism dominating the normal failure samples.

For the normal failures, leakage and subsequent dielectric breakdown are the main failure mechanism (i.e. thermal dielectric breakdown). Thus, the factor for the poorer dielectric performance of SiN-capped structures is the interface between the SiN capping layer and the SiO₂ IMD. It is shown that P-F emission occurred with the presence of the SiN/SiO₂ dissimilar interface. The existence of P-F emission in SiN-capped structures could be due to two reasons. One obvious reason is the presence of higher density of interfacial traps at a dissimilar SiN/SiO₂ interface as compared to a similar SiO₂/SiO₂ interface in stand-alone CoWP-capped structures. The higher density of traps in the IMD for SiN-capped structures is also reflected in the higher SILC seen in the I-t curves. Another reason for the P-F emission would be the contribution of a higher dielectric constant by the SiN cap which leads to a higher local electric field at the CMP surface based on the Lorentz relation. A higher resultant field in the SiN-capped structures will then cause easier de-

trapping of the electrons as compared to that for CoWP-capped structures since P-F emission is electric field dependent. Hence, the presence of the dielectric cap could either increase the density of interfacial traps or increase the resultant local electric field experienced by the molecules in the IMD, both of which will increase the leakage current and degrade the breakdown strength as well as the time-to-fail.

On the other hand, SiO₂ dielectric degradation (at the SiO₂/SiO₂ interface and also in the bulk SiO₂) is expected to be the main TDDB degradation mechanism in CoWP-capped structures due to absence of the SiN capping layer. Nevertheless, Co and Cu diffusion into the IMD could accelerate the dielectric breakdown and also cause leakage fluctuations. Hence, the TDDB degradation mechanism in CoWP-capped structures is dominated either by the drift and diffusion of Co and Cu into the SiO₂ dielectrics or degradation of the SiO₂ dielectric. In order to determine which mechanism is dominant, an evaluation based on the TDDB activation energy was carried out. The TDDB activation energy obtained for SiN-capped structures is consistent with other reported dielectric cap-IMD systems [116]. On the other hand, the TDDB activation energies obtained for CoWP-capped structures are close to the Cu or Co diffusion activation energies into SiO₂ dielectric but closer to the TDDB activation energy for intrinsic SiO₂ degradation reported in the literature.

To further illustrate, the activation energy for Co diffusion into SiO₂ dielectric is 1.70 eV while it is 2.36 eV for large Co concentration [135]. Meanwhile, Cu ion drift into PECVD SiO₂ dielectric is found to be 1.13 eV [31]. Moreover, Cu is able to diffuse out from the CoWP cap barrier partially due to the loss of the CoWP efficiency as a diffusion barrier caused by the out-diffusion of Co and even P element. Besides, Cu could also diffuse through the grain boundaries of the CoWP cap with a required activation energy of 1.25

eV as measured in [136]. As can be seen, the activation energies required for Cu or Co drift and diffusion are somewhat higher than the experimentally observed TDDB activation energies. Therefore, it is likely that SiO₂ dielectric degradation occurs first prior to the Co or Cu diffusion since the TDDB activation energy measured is close to TDDB activation energy reported for SiO₂ gate oxides, which are between 0.70 – 0.95 eV for applied fields less than 9 MV/cm [137]. Moreover, the degradation would occur first at the SiO₂/SiO₂ interface followed by the bulk SiO₂ degradation.

Nonetheless, the Co and subsequently Cu diffusion into the SiO₂ dielectric play an important role in the dielectric breakdown. It was shown that the presence of Co contamination prior to the TDDB stress caused the early failures and led to the lower breakdown strengths and shorter times-to-failure in 40 nm-thick CoWP-capped structures. Therefore, in order to obtain a reasonable TDDB reliability, a compromise must be made between having a thick CoWP cap to increase its diffusion barrier properties and having a thin CoWP cap to minimize Co contamination during plating. Definitely, effective clean procedures after CoWP deposition need to be developed to eliminate the Co contamination.

In conclusion, the results of this chapter show that incorporating a metallic stand-alone self-aligned CoWP barrier and eliminating the dissimilar interface between the dielectric cap and intra-metal dielectric could improve TDDB reliability of interconnects in both symmetric structures (line-to-line configuration) as well as asymmetric structures (line-to-via configuration). In terms of the failure mechanism, TDDB degradation without the dielectric cap is dominated by a similar material interface (i.e. SiO₂/SiO₂ interface in this thesis) and intrinsic properties of the IMD, as opposed to the conventional dielectric cap

architecture whereby TDDB degradation is controlled by the dielectric cap properties and its associated dissimilar interface.

CHAPTER 6: CONCLUSIONS

6.1 Comb Structures and Its Failure Analysis Challenges

6.1.1 Failure localization methods

Localization of failure sites in standard comb test structures is undoubtedly tedious, challenging and unpredictable especially for sub-surface failures which may be more important than gross failures. This is due to the large comb structure area (10^{-3} cm^2) as compared to the much smaller failure analysis area for cross-sectional SEM or TEM (10^{-8} cm^2). As a result, the failures could only be analyzed from the plan view through the use of optical microscopy; top down polishing or delayering to reveal the affected layer and subsequent cross-section analysis using FIB. This method has its limitations since polishing could destroy the failure site unknowingly and optical microscopy has its own resolution limits.

Therefore, failure localization techniques such as the laser-induced failure localization technique have proven to be useful. Thermally-induced voltage alteration (TIVA) technique is one of the techniques used to localize resistive and open metallization defects although it was ineffective in localizing the sub-surface failure sites in this research project. Instead, pulsed-TIVA was applied due to its enhanced sensitivity features as demonstrated in the failures that were localized and summarized in the ensuing subsection.

6.1.2 Failure mechanisms in comb structures

The failure modes and mechanisms observed in comb structures were similar to those reported in the literature. They were mainly mechanical cracking through the capping layer followed by Cu extrusion through the crack paths, as well as catastrophic thermal dielectric breakdown which manifests as visible and non-visible burn marks. The cause of

mechanical cracking and subsequent Cu extrusion is attributed to electrostatic forces during the electrical stress. The crack paths were at 45° from the Cu surface due to the high stress concentration at the corners of the Cu trench whereby the maximum shear stress is at 45° from the Cu surface. On the other hand, the catastrophic thermal dielectric breakdown is due to Joule heating and subsequent thermal runaway.

The failures were mostly catastrophic in nature and thus, the factors leading to the catastrophic dielectric breakdown cannot be identified, thereby making it difficult to rectify or improve the TDDB reliability. Nevertheless, the observation of the non-visible burn marks, at which a catastrophic burn occurred at the region near the dielectric capping layer and CMP surface (i.e. at the upper half of the Cu trench), revealed an important evidence to aid the understanding of failure mechanism(s) in interconnects other than the mechanical cracking. From the comb structures, it could be inferred that the dielectric capping layer and its adjacent interface quality are the main factors contributing to the dielectric breakdown.

6.2 Dielectric Reliability in Single Line and Corner Structures

As a result of the challenges faced in using comb structures for failure mechanism investigations, new test structures were designed to facilitate the failure analysis procedure. The advantages of having these structures are described in the following. It can confine the failure to one particular site, unlike the comb structures and designed with dimensions suitable for precise TEM analyses such as high resolution imaging and elemental analyses. Inadvertently, the failure severity is reduced due to a much smaller leakage area. Moreover, the interconnect layout effects on the leakage current and dielectric breakdown in Cu/low-*k* interconnects could be evaluated. In addition, a more stringent reliability assessment could be performed due to electric field enhancement at

the line ends (S1) and corners (S2) as compared to the nominal electric fields occurring in the parallel lines of comb structures.

6.2.1 *Delamination-induced leakage and breakdown mechanism*

From the S1 and S2 test structures, delamination mainly at the interface between the SiC(N) capping layer and SiOCH low- k dielectric and occasionally at the SiOCH/USG interface, followed by SiC(N) capping layer damage as well as Cu diffusion through the capping layer and into the delaminated region were physically observed. These aptly explain the catastrophic dielectric breakdown near the capping layer region. The delamination is due to weak interface adhesion (confirmed by four point bend adhesion experiment) whereby bond breaking at the interface is driven by a field-enhanced thermal process and catalyzed by leakage current through the capping layer as well as the IMD (verified from the calculated effective molecular dipole moment values). Moreover, leakage current was deduced to be mainly through the SiC(N) capping layer due to a lower electron barrier height as well as its reported electrical instability. In addition, the conduction mechanism observed during the delamination was Poole-Frenkel emission of the trapped electrons at the delaminated region.

With leakage through the capping layer and delaminated interface, the delamination widened with time and the capping layer gradually degraded structurally. At the same time, Cu diffusion through the cap and along the interface accelerated the dielectric breakdown process. The delamination was not observed in comb structures mainly due to its structure orientation which makes it more difficult for delamination to occur, thereby explaining the higher TDDB activation energy of comb structures as compared to the S1 and S2 structures. Nevertheless, the initial failure site is similar to that in comb structures, which is at the upper half of the Cu trench. Therefore, it can be concluded that the leakage

and dielectric breakdown in Cu/low- k interconnects is dominantly affected by the dielectric capping layer properties and its interface adhesion quality with adjacent dielectrics.

6.2.2 Ta ionic drift and diffusion and its leakage contributions

The integrity of the sidewall barrier is another factor that affects the dielectric reliability in Cu/low- k interconnects. Specifically, Ta migration from the anode sidewall and into the SiOCH low- k dielectric was found to cause a leakage step, as observed from the I-V and I-t curves. The driving force of Ta migration is Ta's oxidation tendency which resulted in the formation of Ta ions. This was attributed to the presence of oxygen in the SiOCH low- k dielectric adjacent to the sidewall barrier. Subsequently, the Ta ions drifted and diffused into the SiOCH low- k dielectric with the aid of an applied electric field. The leakage current increase at the start of the leakage step is due to the Ta ionic drift and diffusion but the eventual leakage saturation is due to the formation of a dense and stable Ta oxide.

6.3 Improvements with Stand-Alone CoWP Metal Capped Structures

The dielectric capping layer was shown to be one of the key factors that degrades the dielectric reliability in interconnects resulting in interface delamination and lower TDDB activation energy, especially in structures that experience electric field enhancements such as S1 and S2 structures. Therefore, the introduction of stand-alone and self-aligned CoWP metal caps is promising in terms of the TDDB reliability of interconnects. In this research, the leakage current, dielectric breakdown and time-to-failure performance of asymmetric and symmetric comb structures with CoWP cap were found to be better than conventional SiN-capped structures.

Specifically, the leakage in CoWP-capped structures is comparable to SiN-capped structures at low fields but became lower at high fields. Moreover, CoWP-capped structures show negligible P-F emission. On the other hand, SiN-capped structures exhibited P-F emission due to interfacial traps at the dissimilar SiN/SiO₂ interface and experienced a higher local electric field due to the higher dielectric constant of SiN.

In addition, the breakdown strength and time-to-failure were found to be enhanced with CoWP-capped structures although it became comparable to SiN-capped structures at higher temperatures. More interestingly, the TDDB activation energy for CoWP-capped structures is almost twice of that of SiN-capped structures and even other structures that are conventionally capped with dielectric barriers. The TDDB degradation mechanism for CoWP-capped structures is then postulated to be dominated by the SiO₂/SiO₂ interface and intrinsic properties of the intra-metal dielectric, failure of which led to Co and Cu diffusion. This is in contrast with TDDB degradation in dielectric cap architectures whereby presence of the dielectric cap and its associated dissimilar interface increases the leakage, lowers the breakdown strength, shortens the time-to-failure as well as lowers the TDDB thermal activation energy.

6.4 Research Thesis Contributions and Future Outlook

In a nutshell, the failure mode and mechanisms for the different interconnect architecture, i.e. different interconnect layout (S1 and S2) and different dielectric stack (SiN versus CoWP capping layer), presented and discussed in chapters 3 to 5 as well as reviewed in this chapter are summarized in Table 6.1. The numbers or roman numerals indicated in bold are the failure modes defined as specified in the relevant chapters.

Table 6.1 Interconnect architecture impact on failure mechanisms in advanced Cu/low-*k* interconnects

Dielectric Stack Type	Dielectric-Capped Structures				Self-aligned Metal-Capped Structures
Cap Material	SiC or SiC(N)			SiN	CoWP
Interconnect Layout	Comb	Comb	Single line (S1) and corner (S2)	Comb	Comb
Failure Mode & Mechanism	1: Cu extrusion & mechanical cracking caused by electrostatic forces	2: Thermal dielectric breakdown at the cap	I: Thermal dielectric breakdown; II: Delamination (>5MV/cm) & Cu diffusion; III: Ta migration (>2.5MV/cm)	Thermal dielectric breakdown at the cap	Thermal dielectric breakdown at SiO ₂ /SiO ₂ interface; Co and Cu diffusion
Breakdown Strength (MV/cm)	1.7 – 2.2	(3.3 – 3.9)/ (3.6 – 7.9)	3.3 – 7.8	1.5 – 8.4	2.2 – 10
TDDB Activation Energy (eV)	N.A.	N.A./ 0.44	0.20 – 0.23	0.47 – 0.58	0.66 – 0.96
Location of Results/ Discussion	Chapter 3	Chapter 3/4	Chapter 4	Chapter 5	Chapter 5

As can be seen from the table, failure Type 1 is caused by extrinsic-like factors which could be related to high defect density and low yield of the wafer used. The breakdown strengths are seen to improve for wafers used in Chapter 4 whereby Type 1 failures are believed to be eliminated.

The interconnect layout also has an impact on the failure mode and mechanism, breakdown strength as well as TDDB activation energy. For S1 and S2 structures which are common in actual interconnect circuits, the observed delamination at the SiC(N)/SiOCH interface demonstrates the importance of interface adhesion strength in the interconnect system. For 32 nm technology nodes and beyond, interface adhesion strength will definitely be one of the main focuses due to introduction of ultra low-*k* dielectrics which are more porous than the current low-*k* dielectrics and therefore more likely to have poorer adhesion strengths. Hence, new materials or intelligent process

manipulation is required to ensure that the interfacial adhesion strengths of the various interfaces do not degrade the dielectric reliability performance. One of the viable solutions is by implementing self-aligned CoWP metal cap to improve the adhesion strength with Cu while eliminating dissimilar interfaces at the IMD region. It was shown in the thesis that the TDDB reliability was improved.

Furthermore, the integrity of sidewall barrier and the quality of low- k dielectric adjacent to the sidewall barrier should not be neglected. Ta migration from the anode was shown to be possible due to Ta's high oxidation tendency and availability of oxygen molecules in the low- k dielectric. Therefore, new barrier materials that do not react readily with oxygen or low- k dielectric candidates that do not contain oxygen could be considered for future generation interconnects. Moreover, for future generation interconnects, the likelihood for Ta migration to occur increases due to the increase in electric field caused by shrinking of line space as well as the increased occurrence of line edge roughness.

On the other hand, new testing methodologies other than the voltage ramp and constant voltage stress may become necessary for future technology nodes to further understand the failure mechanisms. It was demonstrated here that the ESD stress was able to control the delamination failure severity and thus, yielded information on the leakage mechanism. These led to the recommendations for future work described in the next section.

6.5 Recommendations for Future Work

Standard electrical tests (i.e. voltage ramp and constant voltage stress) have been used to investigate the conduction mechanisms and TDDB parameters for the comb structure and new test structures in this research. Furthermore, ESD pulses have been used to trigger failure at progressive stages and thus, enable further understanding of the leakage and

failure mechanism. Recently, pulsed voltage tests (unipolar) and alternating voltage tests (bipolar) are implemented to estimate a more realistic TDDB lifetime since most interconnects carry pulsed DC or AC in actual circuits. Therefore, it would be of significant interest to investigate the differences, if any, in the leakage and failure mechanisms under pulsed DC or AC test conditions for comb, S1 and S2 test structures as well as stand-alone CoWP-capped structures.

In this research project, delamination has been observed in between the SiC(N) cap and the SiOCH low- k dielectric above the cap, which is the interface with the weakest adhesion strength. If the interconnect structure does not have a USG buried capping layer, the delamination is predicted to shift to the interface between SiC(N) cap and intra-metal SiOCH low- k dielectric below it, which is at the CMP interface. Hence, S1 and S2 structures with varying dielectric stacks (for example, with and without a buried capping layer) could be studied to validate the location of delamination. Furthermore, apart from asymmetric and symmetric comb structures for CoWP metal cap, characterizing the S1 and S2 type of test structures could further establish the current understanding of the TDDB degradation mechanism and also enable the study of the effects of interconnect layout in metal-capped structures.

In addition, the impact of process integration in terms of improving the interface adhesion strength, especially at interfaces with low- k dielectric could be investigated. It was recently reported that the interface adhesion strength between SiC(N) and SiOCH could be improved by H₂ and NH₃ plasma treatment at that interface [138] or by inserting an adhesion promoter layer in between. Therefore, by varying the process steps and using the specifically designed S1 and S2 test structures, the impact could be physically established.

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