Design of transmitter front-end for WLAN 802.11ax application

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Design of Transmitter Front-End for WLAN 802.11ax Application

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2020

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Date Liu Bei

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Summary

As the successor to current IEEE 802.11ac, the emerging IEEE 802.11ax will increase the efficiency of wireless local area network (WLAN) networks, especially in the high-density WLAN deployment scenario, and the data rate is expected to reach 10 Gbps. Carrier aggregation (CA) will be a key feature of 802.11ax system to boost data rate. Voltage-controlled oscillator (VCO) pulling and crosstalk between RF channels are two main problems related to carrier aggregation due to the inevitable coupling and leakage between different signal transmitting channels in one complementary metal-oxide silicon (CMOS) chip, which introduce severe impacts on adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). To address these two problems, high isolation between signal transmitting channels is required, but may not be realizable in some practical cases due to the constraint of layout. Firstly, this thesis proposes a new transmitter architecture using parallel direct-conversion and double-conversion configuration, which can address the problems of crosstalk and VCO pulling simultaneously without large physical isolation. Based on the proposed transmitter architecture, a transmitter front-end supporting two-carriers aggregation for 5-GHz WLAN 802.11ax application is designed and implemented in TSMC 40-nm CMOS technology. For contiguous intra-band carrier aggregation with two VHT80, MCS9 signals (80-MHz bandwidth, 256-quadrature amplitude modulation (QAM) and 11.25-dB peak-to-average power ratio (PAPR)), the transmitter front-end delivers an average output power of 5.3+4.8 dBm for two carriers with the EVM ≤ -32 dB, and the EVM can reach -36.1 dB.

802.11ax's systems are designed to operate in the existing 2.4-GHz and 5-GHz (4.9-5.9 GHz) spectrums, requiring a 2.4/5-GHz dual-band transmitter front-end. A single

transmitter supporting reconfigurable 2.4/5-GHz dual-band operation is superior to the dual-band architecture using two transmitters channels in terms of lower cost. Currently, no reconfigurable dual-band transmitter using only one transmitting channel is available in academia and industry. Therefore, another effort of this thesis is to design such a reconfigurable 2.4/5-GHz dual-band transmitter front-end for 802.11ax application. As a core block in a transmitter, the power amplifier (PA) should also operate in the 2.4- and 5-GHz bands. This thesis presents a new design methodology of the reconfigurable dual-band output matching network to extract high passive efficiency. A 2.4/5-GHz dual-band PA is designed to validate the proposed matching methodology. In the 2.4-GHz and 5-GHz WLAN bands, the PA achieves a saturated output power (P_{sat}) of 23 dBm and 21.9-22.4 dBm with power-added efficiency (PAE) of 27% and 24.2-28.2%, respectively. Then, a transmitter front-end supporting the 2.4/5-GHz dual-band operation for WLAN 802.11ax application is designed. The measurement results verify that the transmitter front-end can support the 802.11ax signal with 1024-QAM modulation both in the 2.4- and 5-GHz bands. Since only one RF channel is used, the proposed transmitter front-end has the advantages of simpler design, smaller chip size and lower cost, in comparison with other state-of-the-art dual-band WLAN transmitters.

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List of Acronyms

ACLR	Adjacent Channel Leakage Ratio
AWG	Arbitrary Waveform Generator
BPF	Band-Pass Filter
CMOS	Complementary Metal-Oxide Silicon
CA	Carrier Aggregation
CML	Current-Mode Logic
CPW	Coplanar Waveguide
DAC	Digital-to-Analog Convertor
DPD	Digital Pre-Distortion
EM	Electromagnetic
EVM	Error Vector Magnitude
GMSK	Gaussian Minimum Shift Keying
ISM	Industrial, Scientific, and Medical
IF	Intermediate Frequency
LPF	Low-Pass Filter
LO	Local Oscillator
OFDMA	Orthogonal Frequency-Division Multiple Access
OQPSK	Offset Quadrature Phase-Shift Keying
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PGA	Programmable-Gain Amplifier (PGA)
PLL	Phase-Locked Loop

PPA	Pre-PA Amplifier
P_{sat}	Saturated Output Power
QAM	Quadrature Amplitude Modulation
SNR	Signal-to-Noise Ratio
VCO	Voltage-Controlled Oscillator
VGA	Variable-Gain Amplifier
V-I	Voltage-to-Current
VSG	Vector Signal Generator
WLAN	Wireless Local Area Network
5G	Fifth-Generation

Chapter 1

Introduction

1.1 Motivation

Recently, the accelerating growth of smartphones and mobile devices is propelling the wireless communication to evolve towards higher data rate. Currently, the development of new IEEE 802.11 standards, driven by the increasing demand on the broadband wireless local area network (WLAN), becomes a hot research topic in recent years. As the main 5-GHz WLAN standards, IEEE 802.11ac system utilizes a wider bandwidth and more complex modulation scheme, and thus can provide up to 866 Mbps date rate. As the successor to current IEEE 802.11ac, the emerging IEEE 802.11ax introduces orthogonal frequency-division multiple access (OFDMA), utilizes smaller sub-carrier spacing and employs 1024-quadrature amplitude modulation (QAM) to improve overall spectrum efficiency and boost the data rate. Besides, carrier aggregation (or channel bonding) technique is a key feature of 802.11ax standard to increase the data rate significantly. By introducing carrier aggregation, the data rate of 802.11ax is expected to reach 10 Gb/s, in order to meet the tremendous demand for high data rate applications, such as interactive and high-definition video.

Carrier aggregation (CA), originating from LTE-Advanced, combines multiple contiguous or non-contiguous frequency bands together, to form a wider frequency band to increase the transmission data rate. There are three kinds of carrier aggregation: intra-band contiguous aggregation, intra-band non-contiguous aggregation, and inter-band non-contiguous aggregation [1], as shown in Figure 1.1. In the 5-GHz band, three discontinuous frequency bands are allocated for 802.11ax: 5.17 GHz ~ 5.33 GHz, 5.49 GHz ~ 5.71 GHz, and 5.735 GHz ~ 5.835 GHz [2], as shown in Figure 1.2. In practical

application, all three carrier aggregation modes will be supported in 802.11ax transceiver.

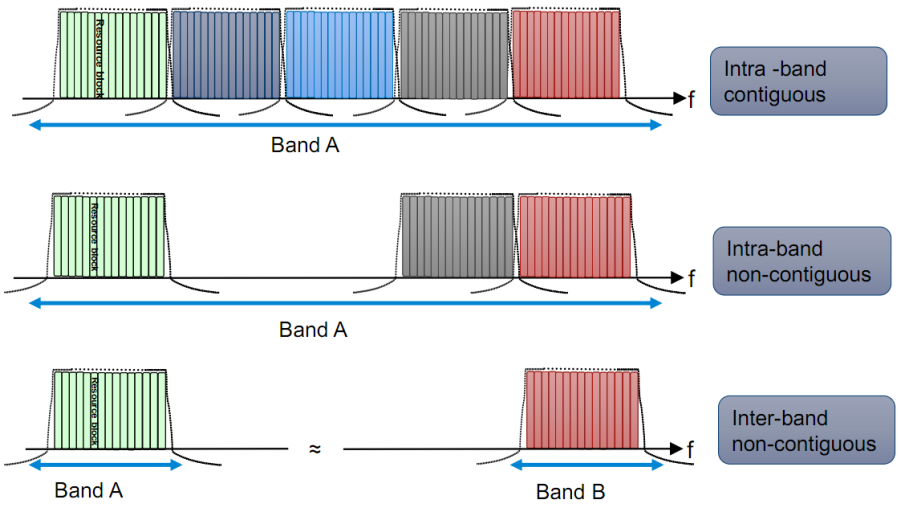


Figure 1.1. Carrier aggregation scenarios.

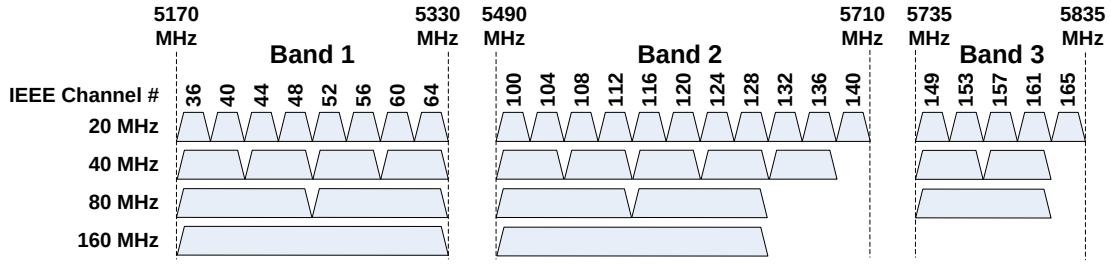


Figure 1.2. 5-GHz WLAN frequency allocation for 802.11ax.

Some transmitter architectures have been introduced and discussed in [1] and [3]. The main difference between these proposed architectures lies in where the carriers are combined in the transmitter. To support intra-band contiguous carrier aggregation, a single transmitter chain with all carriers aggregated at digital baseband is feasible [4]. Since the aggregated signals are processed in only one RF transmitter chain after generated from digital-to-analog convertor (DAC), this architecture is the least complex architecture in terms of the number of RF blocks required. In practice, this architecture can further support non-contiguous carrier aggregation with a small frequency spacing. However, in 802.11ax application scenario where the frequency spacing between carriers is quite large, the sampling rate of DAC has to be extremely high accordingly, causing

considerable power consumption and intensifying the complexity of DAC.

To support inter-band carrier aggregation, the architecture with carriers combined in RF part can be utilized. However, the conventional architecture for carrier aggregation in RF part has inherent problems of crosstalk and voltage-controlled oscillator (VCO) pulling caused by the interaction between transmitter channels in RFIC implementation [5]-[9], which introduce severe impacts on adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). To address these two problems, high isolation between the transmitter channels is required. In order to increase the isolation and reduce the interaction between the transmitter channels, a sufficiently large physical separation between transmitter channels is required. However, in practice, large physical separation between transmitter channels requires a large chip size, and may not be achieved due to the constraint of layout in some cases. Thus, one motivation of the work in this thesis is to propose a new carrier aggregation transmitter architecture that can effectively mitigate the problems of crosstalk and VCO pulling simultaneously without a large physical isolation required on-chip.

Besides the 5-GHz WLAN band, 802.11ax will also operate in the existing unlicensed 2.4-GHz band. Therefore, 802.11ax's devices will be designed with the dual-band operation, requiring a dual-band transmitter or a broadband transmitter covering both the 2.4- and 5-GHz bands. In the literature and commercial products, two separate RF transmitting channels with different operating frequencies are integrated together to enable the 2.4/5-GHz dual-band operation [10]-[20]. Although the architecture using two RF channels can meet the requirement of the dual-band operation for 802.11ax, the chip size will be large and the cost will be high due to two RF channels used. In terms of low cost, a single transmitter supporting reconfigurable 2.4/5-GHz operation is superior to the dual-band architecture using two transmitters. Currently, no reconfigurable dual-band

transmitter using only one transmitting channel is available in academia and industry. Therefore, the other motivation of the thesis is driven by the requirement for such a reconfigurable 2.4/5-GHz dual-band transmitter front-end.

As a core block in a transmitter, the power amplifier (PA) should operate in dual bands or in a broadband to cover both the 2.4- and 5-GHz bands. There are two general approaches that have been proposed to implement dual-band or multi-band and broadband PAs in complementary metal-oxide silicon (CMOS) technology. The first approach is based on using distributed configurations [21]-[23] and various broadband matching techniques such as reactive filter synthesis [24]-[28]. Nevertheless, no matter using the distributed configurations or the broadband matching techniques, PAs inherently suffer from low power efficiency and large size, making them unsuitable for low cost application. The other approach is based on using reconfigurable components in the matching networks, such as switches [29]-[31]. However, in the relevant publications, the passive efficiency of the reconfigurable dual-band matching network is quite low, having a significant impact on PAs' final efficiencies. Therefore, one more effort of this thesis is to design such a reconfigurable 2.4/5-GHz dual-band PA with high efficiency in the dual-band transmitter front-end.

1.2 Major Contribution

The major contribution of this thesis is summarized as follows.

1. Crosstalk and VCO pulling are two main problems related to carrier aggregation, which are caused by inevitable coupling or leakage though low-resistance Si substrate and electromagnetic radiation. In this thesis, the effect of crosstalk between different signal paths on signal-to-noise (SNR) and EVM for 802.11ax signal is thoroughly analysed. Besides, VCO pulling is investigated, and the impact of VCO pulling on ACLR is demonstrated. Furthermore, the coupling strength between different signal paths in

practical layout is explored, indicting a large physical separation between transmitter channels is required to guarantee a low coupling strength.

2. In some practical cases, due to the constraint of layout, high isolation between signal transmitting channels may not be realized to address the problems of crosstalk and VCO pulling. A new transmitter architecture using parallel direct-conversion and double-conversion configuration is proposed to solve the problems of crosstalk and VCO pulling simultaneously without a large physical isolation requirement. The proposed transmitter architecture can support arbitrary mode of carrier aggregation for 802.11ax in the 5-GHz WLAN band. A 5-GHz transmitter front-end supporting two-carriers aggregation is designed to verify the effectiveness of the proposed transmitter architecture.

3. Besides the 5-GHz WLAN band, 802.11ax systems operate in the 2.4-GHz WLAN band, requiring a 2.4/5-GHz dual-band PA and dual-band transmitter front-end. A new design methodology of a reconfigurable dual-band output matching network with high passive efficiency is proposed. A 2.4/5-GHz dual-band PA is designed to validate the methodology, and the synthesis procedure of the reconfigurable output matching network is described in detail, providing a guideline for other researchers to employ the proposed methodology. Based on the implemented standalone PA, a 2.4/5-GHz dual-band transmitter front-end is designed and implemented, which is the first published design for dual-band WLAN 802.11ax application in the literature and industry.

1.3 Thesis Organization

This thesis is organized as follows.

Chapter 2 firstly gives a brief review on the transmitter architectures for single carrier and some possible transmitter architectures for carrier aggregation. Secondly, these transmitter architectures for carrier aggregation are compared in terms of their applicability, cost and system's complexity. Finally, the prevalent dual-band WLAN

transmitter architectures in commercial products are discussed.

In Chapter 3, firstly, the problem of crosstalk related to carrier aggregation is introduced, and the impact of crosstalk on EVM for different modulation schemes including 64-QAM and 256-QAM is theoretically investigated. Then, the degradation of ACLR caused by VCO pulling is analysed. Finally, to explore the isolation between two practical RF channels, the coupling strength between active devices and between the passive signal traces in TSMC 40-nm technology are simulated.

Chapter 4 presents a novel carrier aggregation transmitter architecture using parallel direct-conversion and double-conversion configuration to solve the problems of crosstalk and VCO pulling, and explicitly explains the mechanism of crosstalk and VCO pulling mitigation. Based on the proposed architecture, a transmitter front-end is designed and implemented in TSMC 40-nm technology. The implemented transmitter front-end consists of LO generator, mixer, driver and PA, and the design of these circuit blocks are described. The transmitter front-end is measured using two 802.11ax signals with 80-MHz bandwidth and 256-QAM, and the measurement results are reported in Chapter 4.

In Chapter 5, a new design methodology of a reconfigurable dual-band output matching network to achieve high passive efficiency is introduced. By employing the proposed methodology, a 2.4/5-GHz dual-band standalone PA and transmitter front-end are designed and fabricated, and the experimental results are presented.

Finally, Chapter 6 concludes the work in this thesis and gives some recommendations for the future works.

Chapter 2

Review of transmitter

The transmitter is the building block of the communication systems, and it is the physical layer of the system and the actual device that sends the modulated signal through wireless channel. Thus, the transmitter plays a key role in the performance of wireless communication systems. In this chapter, to better understand transmitter architecture, we firstly introduce some conventional transmitter architectures for single carrier [32]-[35]. Then, a brief review on some transmitter architectures applicable for carrier-aggregation is given, and the design challenges in terms of their applicability, cost and complexity of system are discussed for these transmitter architectures. In addition, two dual-band transmitter architectures used in the commercial 2.4/5-GHz dual-band WLAN products are reviewed.

2.1 Conventional transmitter architecture

2.1.1 Direct up-conversion transmitter

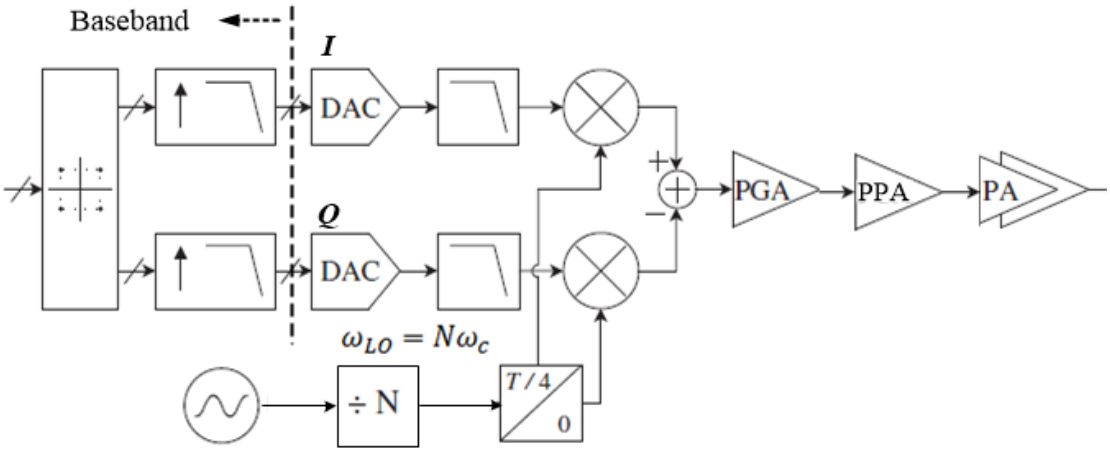


Figure 2.1. Direct up-conversion transmitter [34].

The direct up-conversion transmitter shown in Figure 2.1 is the most common

transmitter architecture, and this topology directly converts the baseband spectrum to the RF carrier. The up-conversion mixer is followed by the amplification blocks including a programmable-gain amplifier (PGA) or variable-gain amplifier (VGA), a Pre-PA amplifier (PPA) and a PA. The analog baseband I and Q signals are filtered by a low-pass filter before being applied to the up-conversion mixer. To avoid oscillator pulling, local oscillator (LO) frequency f_{LO} is chosen sufficiently far from carrier frequency f_c. Mostly, f_{LO} is chosen as twice f_c. However, this architecture cannot fully eliminate injection pulling, since PA's nonlinearity produces a finite power at the second harmonic of the carrier. Besides injection pulling, this architecture suffers from other drawbacks: IQ mismatch, DC offset, LO leakage. In order to compensate these drawbacks, the digital assisted calibrations are employed.

2.1.2 Heterodyne transmitter

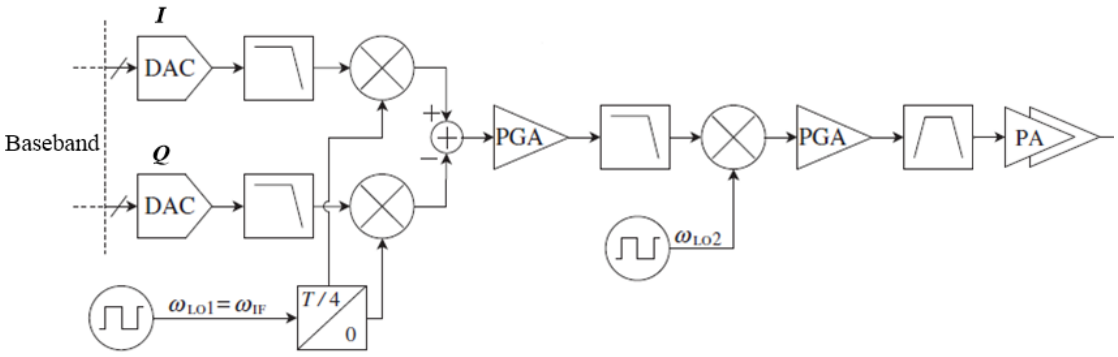


Figure 2.2. Heterodyne transmitter [34].

To avoid injection pulling, another transmitter architecture is proposed, named two-step architecture or heterodyne architecture, as shown in Figure 2.2. The up-conversion is performed in two steps: the baseband I and Q signals are first up-converted to an intermediate frequency (IF) ω_1, and then the IF signal is translated to a carrier frequency $\omega_1+\omega_2$. As a result, the LO frequency remains far from the PA output spectrum. Since the quadrature modulation is performed at lower frequency, IQ matching is superior to

that in the direct up-conversion architecture. In this architecture, a passive bandpass filter is required to reject the unwanted sideband. Compared with the direct up-conversion architecture, this architecture has a higher complexity of implementation and larger chip area, resulting in a higher cost. In addition, the power consumption is also higher due to more circuit blocks used in the transmitter.

2.1.3 Real-IF transmitter

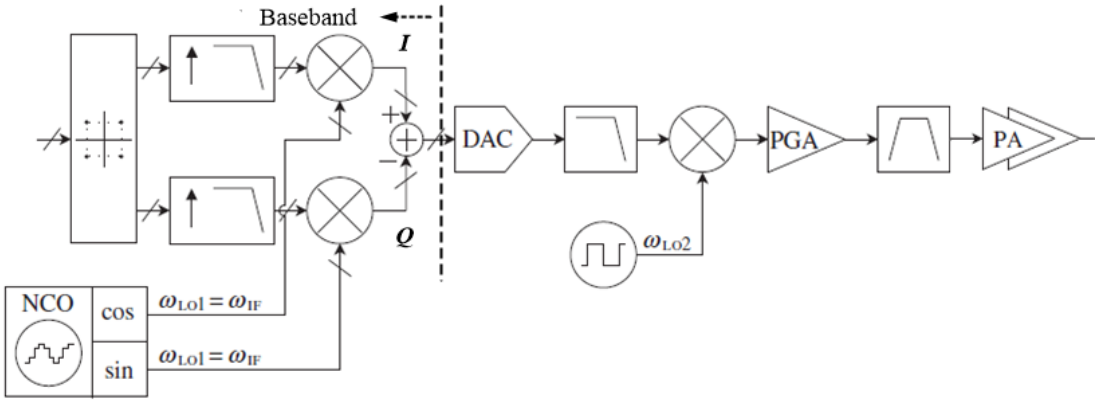


Figure 2.3. Real-IF transmitter [34].

Real-IF transmitter architecture is presented in Figure 2.3. In this architecture, the modulated IF signal is generated in digital domain. Due to the high accuracy associated with the digital signal processing, the imbalance between I and Q signals is negligible. Besides, no LO leakage exists in the transmitter, and in-band image signal is also negligible. Moreover, the digital implementation allows for great agility in phase or frequency jump of the LO waveforms, thus, this architecture could be used in the application involving frequency hopping. Another advantage of this architecture is that only one DAC is used along the signal path. While, since the IF modulation is realized in digital domain, the sampling rate in the digital signal processing is quite high, inducing a high power consumption.

2.1.4 PLL modulation transmitter

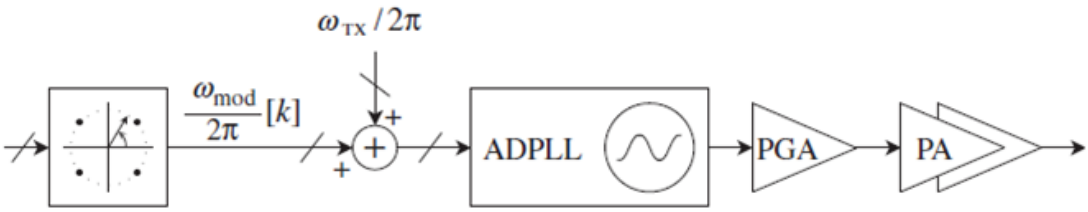


Figure 2.4. PLL modulation transmitter [34].

Phase-locked loop (PLL) modulation transmitter architecture shown in Figure 2.4 is suited to the systems with constant-envelope or pure phase/frequency modulation, such as offset quadrature phase shift keying (OQPSK), pi/4QPSK, Gaussian minimum shift keying (GMSK), PSK. In practice, this architecture is often used in Bluetooth. The main benefit of this architecture is that the minimum set of the processing blocks are required to generate phase/frequency modulation. This architecture also suffers from oscillator pulling. The intrinsic limitation of this architecture is that it cannot be used in the systems with non-constant envelope modulation, such as QPSK and QAM in WLAN and LTE applications.

2.2 Transmitter architecture for carrier aggregation

In order to support carrier aggregation, the baseline transmitter for single-carrier operation can be extended in several ways. The topology of transmitter architecture depends on where the aggregated carriers are combined in the transmitter. Here, four main possible transmitter architectures for carrier aggregation are introduced [1], [3].

2.2.1 Architecture with parallel fully separated chains

This architecture includes multiple separated transmitters, and each transmitter consists of a baseband chain, an up-conversion mixer, an amplification unit, an output bandpass filter and an antenna, as shown in Figure 2.5. In practice, this topology is well suitable for inter-band carrier aggregation. While, due to multiple passive filters and

antennas used, this architecture is not economically efficient, and it can only be implemented in the case where there is no constraint by the cost. Practically speaking, this architecture is not feasible for the system where the cost is limited, such as mobile phone. Although it has potential to be used in 5-GHz WLAN 802.11ax access points if the overall size and cost are not concerned, using too many antennas will become troublesome in mobile phone when supporting more than two carriers.

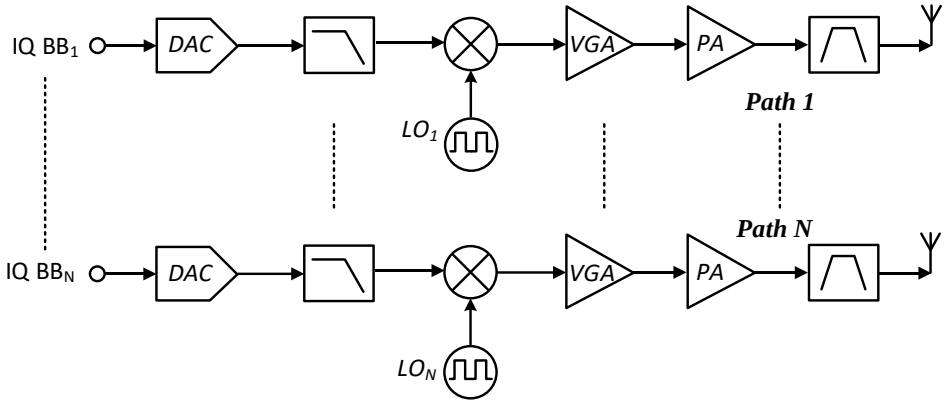


Figure 2.5. Parallel separated chain architecture [1], [3].

2.2.2 Architecture with carriers combined after PAs

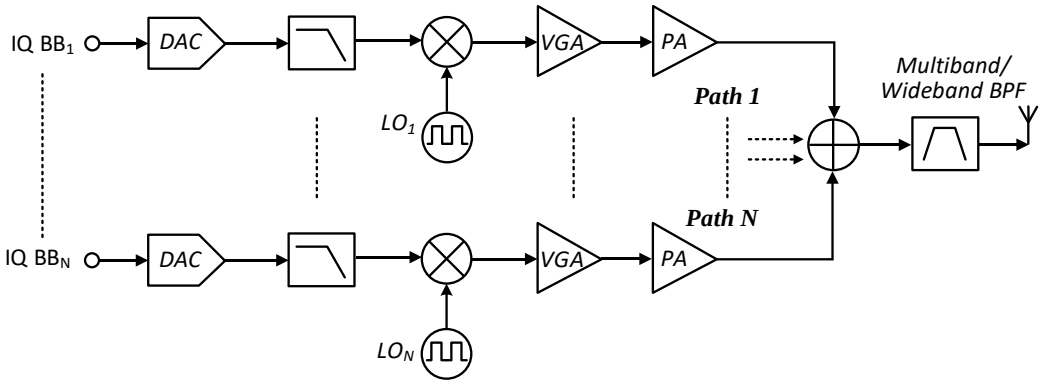


Figure 2.6. Architecture with carriers combined at output of PAs [1], [3].

In order to reduce the number of the passive components (filters and antennas), another candidate architecture is proposed for carrier aggregation [1], [3], as shown in Figure 2.6. In this architecture, the RF output signals from the PAs are combined through a RF combiner or multiplexer. For inter-band carrier aggregation, if the frequency

spacing between the aggregated carries are too large, all the passive components including RF combiner or multiplexer, filter and antenna are required to have a wideband or multiband performance. In practice, it is a great challenge to design such wideband or multiband passive components.

Besides, the PAs may affect each other, causing the load modulation effect, which has a drastic impact on the linearity of the output signal from the PAs and leads to an extreme degradation on EVM performance. In order to avoid load modulation effect between the PAs, the port isolation of the combiner or multiplexer should be sufficiently high, which further intensifies the difficulty in designing RF combiner or multiplexer. In CMOS technique, RF combiner or multiplexer with high port isolation is unavailable. For this reason, off-chip RF combiner or multiplexer is required, bringing in an external cost besides the cost of the filter and antenna.

2.2.3 Architecture with carriers combined before PA

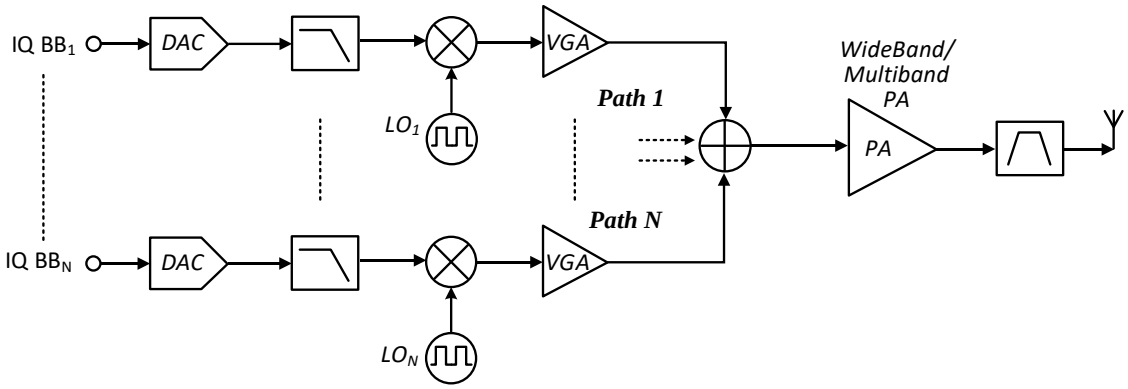


Figure 2.7. Architecture with carriers combined before PA [1], [3].

An alternative architecture is shown in Figure 2.7 [1], [3], [8]. In this architecture, the RF signals are combined before the power amplifier, and only one PA with multi-band or broadband performance is utilized. Since the transistor size of the VGAs is much smaller than that of the PAs, the load modulation between the VGAs is negligible. Therefore, no isolation is required associated with the combination of the carriers.

After combination, the PA processes multiple carriers concurrently, and the total bandwidth of the signals processed in the PA is the sum of all carriers' bandwidth. In this case, the adjacent channels emission of one carrier will decrease the SNRs of other carriers and will further impact the EVMs of other carriers. Thus, the requirement of the linearity is more stringent for the PA processing multiple carriers, compared to the PA processing only one carrier. Consequently, the main practical challenge for this architecture is designing a multi-band/broadband power amplifier with high linearity and high efficiency.

2.2.4 Architecture with carriers combined in baseband

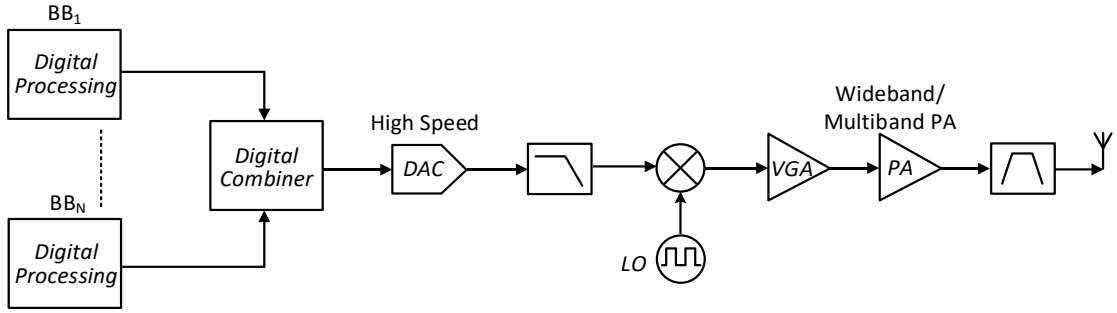


Figure 2.8. Architecture with carriers in digital baseband [1], [3].

Different from the architectures with the carriers combined in the RF part, another possible architecture with the carriers aggregated in digital baseband is presented in Figure 2.8. In this architecture, the aggregated signals from the DAC are processed in only one transmitter chain. As a result, this architecture is the least complex architecture in terms of the number of RF blocks required. While, since the aggregated baseband signal is converted from digital domain to analog domain through a single DAC, the bandwidth of the aggregated signal is constrained by the sampling rate of the DAC. Hence, this architecture is suitable for contiguous intra-band CA or non-contiguous CA with a small frequency spacing between the carriers. For the scenario where the frequency spacing between the carriers is quite large, the sampling rate of the DAC has

to be at least twice the frequency spacing, and will be extremely large, causing considerable power consumption and intensifying the complexity of the DAC. For example, the sampling rates of the DAC are 3.9 GS/s and 1.14 GS/s in [4] and [37], respectively. In order to support inter-band carrier aggregation in the 5-GHz WLAN bands, the sampling rate of the DAC will exceed 1.2 GS/s. Besides, since the carriers are combined in the digital baseband, the complexity of the baseband digital processing will drastically increase, and more digital hardware resources will be occupied and more power will be consumed.

2.2.5 Summary of different architectures

Table 2-1. Comparison of different transmitter architectures for CA.

Architecture	Suitable for cellphone	RF Complexity	Cost of RF Part	Inter-band CA	Intra-band CA
1	No	Low	High	Yes	Yes
2	Yes	High	High	Yes	Yes
3	Yes	Low	Medium	Yes	Yes
4	Yes	Low	Low	No	Yes

Architecture 1, 2, 3 and 4 are the architectures discussed in section 2.2.1-2.2.4, respectively.

To summarize, the comparison of the above mentioned transmitter architectures for carrier aggregation is listed in Table 2-1. Due to the high cost caused by using multiple filters and antenna, Architecture-1 with multiple separated transmitter chains is not suitable for low cost WiFi application in cellphone. Although Architecture-2 with the carriers combined after the power amplifier uses only one filter and one antenna, a broadband combiner with high port isolation is required to alleviate the load modulation between the power amplifiers, which will intensify the complexity of the RF part and increase the cost of the whole transmitter. As for Architecture-4 with the carriers aggregated at digital baseband, it features the lowest complexity of RF part, though, it is not suitable for inter-band carrier aggregation due to extremely high sampling rate of

baseband signal processing. Therefore, considering the feasibility and cost of the RF part, Architectue-3 with the carriers combined before the power amplifier is prior to other architectures to support arbitrary carrier aggregation mode for 5-GHz WLAN 802.11ax application in cellphone.

2.3 Dual-band WLAN Transmitter

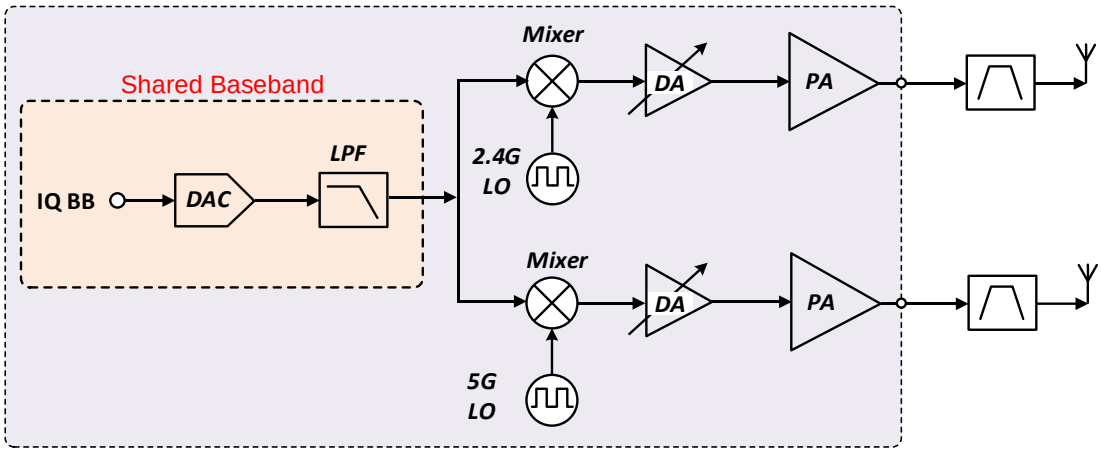


Figure 2.9. Diagram of the dual-band transmitter architecture with shared baseband.

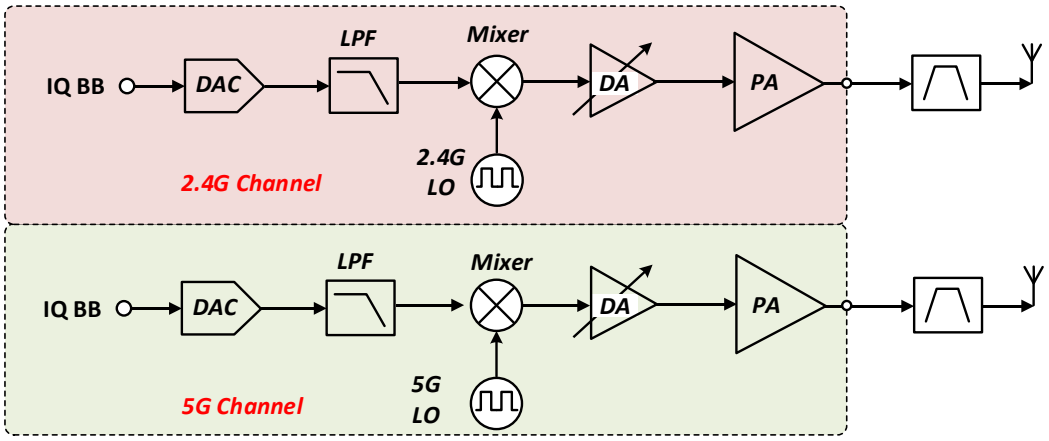


Figure 2.10. Diagram of the dual-band transmitter architecture enabling concurrent dual-band operation.

Currently, WLAN standards have two operation bands: 2.4-GHz ISM band and 5-GHz band. Due to the 2.4-GHz ISM band is shared by WLAN, Bluetooth, Zigbee and

other more applications, it is very crowded in the 2.4-GHz band. Sometimes when other applications occupy the 2.4-GHz band, it is difficult for WLAN to transmit and receive data with a high data rate in the 2.4-GHz band. On the other hand, the existing 5-GHz WLAN band (5.18 to 5.825 GHz) has more available channels and has a flexibility in channel bandwidth. It is much less crowded in the 5-GHz band, and wider bandwidth can be utilized to improve data rate. Therefore, as the main standard of WLAN, 802.11ac operates in the 5-GHz band and is backward compatible with the previous 802.11a. While, since the path loss of link is smaller in the 2.4-GHz band than in the 5-GHz band, the transceivers operating in the 5-GHz band will consume more power to achieve the same coverage range, compared with the transceiver operating in the 2.4-GHz band. Thus, although the 2.4-GHz band may not provide enough bandwidth for WLAN devices in some cases, the function of the 2.4-GHz operation is still necessary for low-to-moderate applications and 2.4-GHz WLAN standards 802.11b/g are still commonly used today.

In practice, most commercial WLAN transceivers are designed to have a 2.4/5-GHz dual-band operation [10]-[17], such that the transceivers can support all existing WLAN standards (802.11a/b/g/n/ac). In some scenarios, the WLAN devices have to toggle from the 2.4-GHz operation to the 5-GHz operation if there is not enough available bandwidth in the 2.4-GHz band, or have to toggle from the 5-GHz operation to the 2.4-GHz operation when the required data rate is no longer high. The dual-band WLAN transceivers proposed in [10]-[17] can meet the requirement of the switching operation modes. Since this thesis focuses on transmitter design, the receiver part of the RF transceivers in [10]-[17] are not involved. In these dual-band transceivers, the transmitter parts use the similar architecture, and the block diagram of the dual-band transmitter architecture is shown in Figure 2.9. In the architecture, there are two separated RF channels including direct up-conversion mixer, driver and power amplifier. A single

analog baseband block including DACs and low pass filters is shared between the 2.4-GHz and 5-GHz channels to reduce the complicity and chip area. At one time, only one RF channel works, and the operation mode can be switched between the 2.4-GHz and 5-GHz modes.

In [18]-[20], another transmitter architecture is presented to support the 2.4-GHz and 5-GHz simultaneous operation, as shown in Figure 2.10. Different from the architecture shown in Figure 2.9, this architecture has two fully separated channels, and each RF channel has its own baseband block. The main benefit of this dual-band transmitter architecture is simultaneous dual-band operation capability, which enables full throughput by utilizing the bandwidths both in the 2.4-GHz and 5-GHz bands. On the other hand, the complexity of this architecture is significantly increased due to the two baseband signal processing units and the baseband analog blocks required in the whole system.

In CMOS implementation, the chip size of the RF transceiver is dominated by the passive components used in the matching networks including inductors and transformers. In the transmitter, the inter-stage matching networks between the mixer and the driver, and between the driver and the PA are required. Besides, the output matching network for the PA is also required. In general, the inductors and transformers are utilized in the inter-stage and output matching networks, which occupy most of the chip area. Therefore, the two architectures shown in Figure 2.9 and Figure 2.10 both have a large size due to the two separated RF channels used. For the architecture in Figure 2.9, if two RF channels can be merged into one RF channel with a dual-band function, the number of the matching networks will be the half and the chip size will be considerably reduced. In terms of low cost, a single transmitter supporting reconfigurable 2.4/5-GHz dual-band operation is superior to the dual-band architecture in Figure 2.9 using two transmitter

channels. Currently, no reconfigurable dual-band transmitter using only one transmitting channel is available in academia and industry. Therefore, one part of the effort in this thesis is to design such a reconfigurable 2.4/5-GHz dual-band transmitter front-end for WLAN 802.11ax application.

Chapter 3

Crosstalk and VCO pulling

To support carrier aggregation, more carrier signals have to be processed concurrently in one CMOS transceiver chip. Due to the low-resistance silicon substrate, coupling or leakage between different signal processing paths is unavoidable, leading to two main problems, namely crosstalk and VCO pulling. Besides, in CMOS transceiver, since the physical spacing between signal processing paths is very small and is even in μm-level, the electromagnetic radiation is another major contributor to the near-filed coupling and leakage, and the coupling strength caused by the electromagnetic radiation is dependent with the operating frequency, which will be discussed in the following parts of this chapter. Among the transmitter architectures for carrier aggregation introduced in Chapter 2, except for the architecture with carriers aggregated in digital domain, all other architectures have the intrinsic problem of crosstalk and VCO pulling in CMOS implementation. Practically speaking, the coupling or leakage between signal processing paths should be minimized to reduce the effect of crosstalk and VCO pulling on the transceiver's performance, which is the main consideration in designing a transceiver supporting carrier aggregation, especially for 5-GHz 802.11ax with wide bandwidth and high order modulation scheme. In this thesis, we only focus on transmitter design for carrier aggregation, and how the performance of transmitter is affected by crosstalk and VCO pulling will be investigated in this chapter. While, the effect of crosstalk and VCO pulling on receiver is not involved and discussed in this thesis. In additional, to explore the strength of interaction between two signal processing channels in practical layout, the coupling factor between active devices and between the passive signal traces are simulated in this chapter.

3.1 Crosstalk

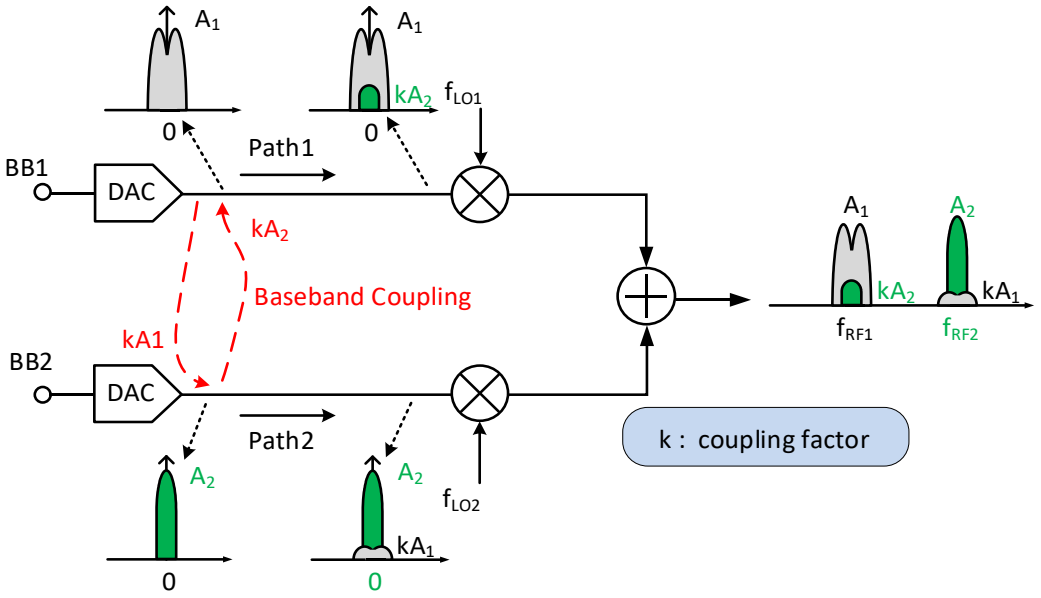


Figure 3.1. Effect of crosstalk caused by baseband coupling on SNR.

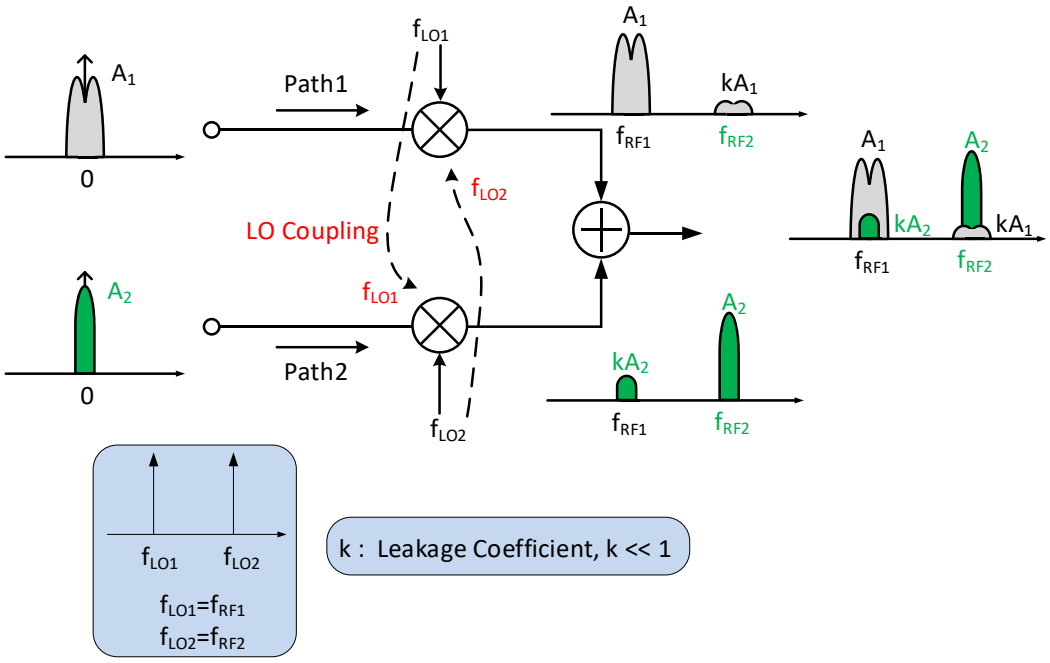


Figure 3.2. Effect of crosstalk caused by LO coupling on SNR.

In general, crosstalk is mainly caused by the baseband coupling and the LO coupling [8], [9], and crosstalk has a significant impact on the signal-to-noise ratio (SNR) of the transmitted signals. Figure 3.1 demonstrates the effect of the baseband coupling on the transmitted signals. In Figure 3.1, two RF transmitting paths both use a direct-conversion

mixer, and two carriers are combined after the mixer. The coupling signal from BB1 falls on top of BB2 and vice versa. As a result, before injected into the mixer, both the signals BB1 and BB2 are interfered by the coupling signal from the other path. Consequently, the SNR of each baseband signal is degraded. In Figure 3.1, the bandwidth of the baseband signal BB1 is assumed to be larger than that of the signal BB2, so only the SNR of the signal BB1 is affected by the interference. Whereas, as for the signal BB2, not only the SNR is degraded, but also the ACLR is degraded. However, in practical carrier aggregation scenario, all carriers have the same bandwidth; thus, in this thesis, the degradation of the ACLR caused by the baseband coupling or the LO coupling is only demonstrated in figures, but not considered in the further analysis.

The effect of crosstalk caused by the LO coupling in direct-conversion transmitter is demonstrated in Figure 3.2. LO signal couples from one path to the other, and there are two LO signals for the mixer in each path. As a result, there are two mixing products of the mixer, and one is the desired RF signal, and the other interference exists at the same frequency of the desired signal in the other path. After combination, the SNR of each transmitting signal is degraded by the resulted interferences. Hence, the LO coupling has the similar impact on the SNR of the RF signals as the baseband coupling does.

As demonstrated in above Figure 3.1 and Figure 3.2, crosstalk have an impact on the SNR, and the degradation of the SNR then affects the EVM performance, which is the most widely adopted standard in the industry to quantify the performance of the signal in the transmitter. Regardless of the impairments of transmitter, such as AM-AM and AM-PM distortion of PA, IQ mismatch, DC offset and phase noise of LO, EVM is a function of SNR [38], expressed by

$$EVM = 100\% \cdot \sqrt{\frac{\sqrt{M}+1}{3 \cdot SNR \cdot (\sqrt{M}-1)}} \tag{3.1}$$

where *M* is the order of modulation. A calculation has been performed to show how EVM is affect by SNR for four modulations, QPSK, 16-QAM, 64-QAM and 256-QAM, and the calculated results are shown in Figure 3.3. Seen from Figure 3.3, when SNR is 50 dB, the values of EVM are nearly 0.3% for all four modulations.

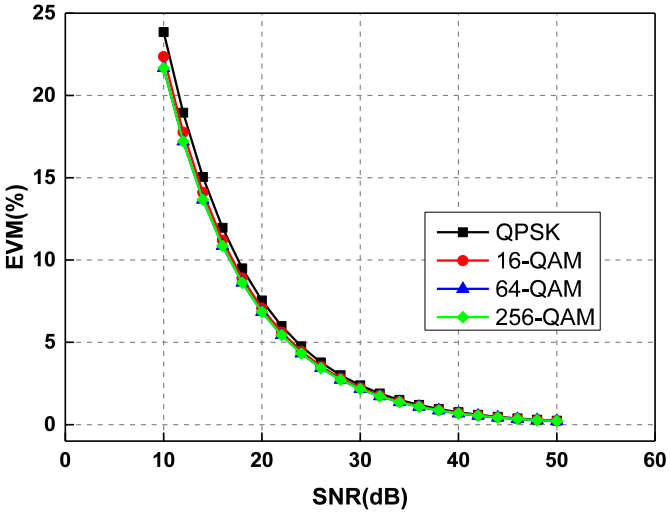
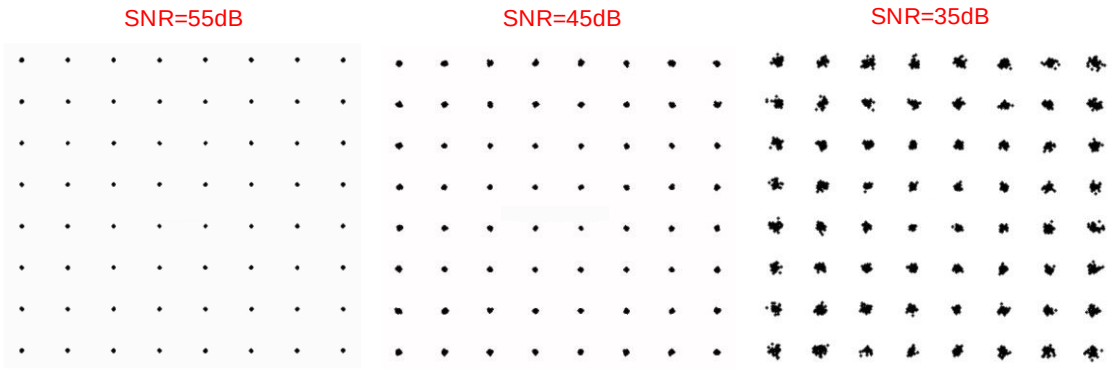


Figure 3.3. EVM versus SNR.

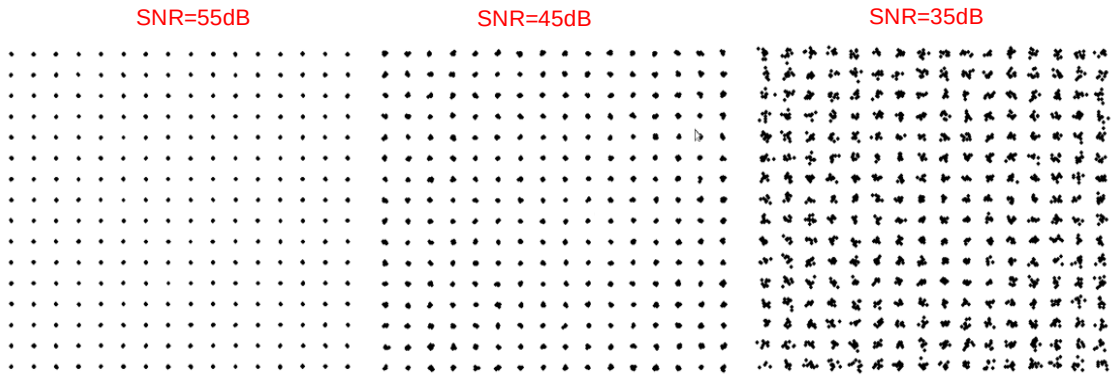
While, in practice, $EVM_{rms,avg}$ is measured instead of EVM through a vector signal analyzer. As an alternative definition of EVM, $EVM_{rms,avg}$ normalizes the error vector to the average symbol energy [39], [39], only depending on SNR, expressed by

$$EVM_{rms,avg} = 100\% \cdot \sqrt{\frac{1}{SNR}} \cdot \tag{3.2}$$

In the following part of this thesis, EVM refers to $EVM_{rms,avg}$. In order to explore the impact of SNR on EVM for practical WLAN signals, a simulation has been performed to calculate the constellation and EVM using 802.11ac signals with different SNRs. Since 802.11ac signal has the same modulation as 802.11ax signal does, 802.11ac signal can be an alternative of 802.11ax signal when simulating the constellation and EVM. In the simulation, 80-MHz 802.11ac signals with 64-QAM and 256-QAM modulation are used. The simulated constellations versus different SNRs are illustrated in Figure 3.4. From



(a)



(b)

Figure 3.1. Simulated constellation for 802.11ac signals. (a) 64-QAM. (b) 256-QAM.

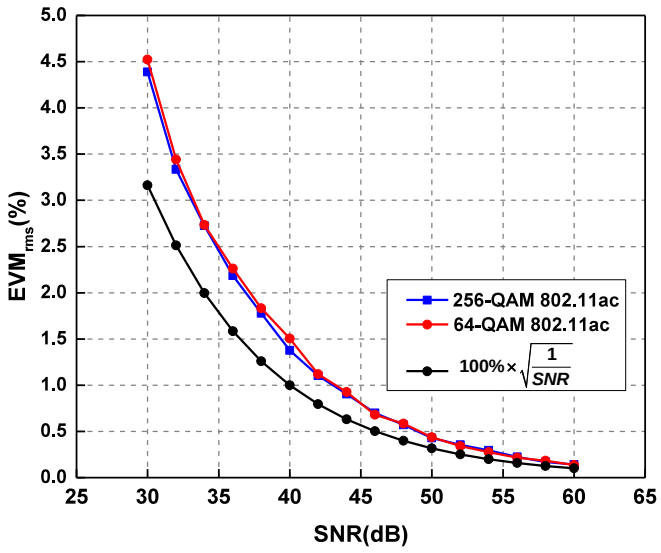


Figure 3.2. Simulated $EVM_{rms,avg}$ versus SNR.

the simulated results, when SNR is higher, the demodulated data points are more concentrated to the ideal points in the constellation, and better EVM can be achieved.

Figure 3.5 plots the simulated EVM with respect to SNR. In Figure 3.5, the EVM curves for 64-QAM and 256-QAM almost overlap, showing that EVM ($EVM_{rms,avg}$) is independent of the modulation, which is in accordance with (3.2). In addition, the simulated EVM for 802.11ac signals is slightly higher than that predicted from (3.2), but has the same tendency with SNR. From Figure 3.5, the 50-dB SNR results in the EVM of 0.42%. Considering the stringent EVM requirement of 2.5% (-32 dB) for 256-QAM modulation, the deterioration of the EVM by 0.42% has a severe impact on system performance, which will intensify the noise and linearity requirement for the circuit blocks in the transmitter. Therefore, for the 802.11ax system employing 256-QAM and 1024-QAM modulation, an SNR of better than 50 dB is required. While, for LTE-Advance, the EVM requirement for 16-QAM is 12.5%, and thus 30 dB SNR is high enough to meet such loose EVM requirement. Compared with LTE-A, it deserves much effort to increase the isolation between signal paths to achieve a high SNR for the 802.11ax system operating in the carrier aggregation mode.

We have thus far analysed the impact of SNR on EVM, and now turn to study how SNR is affected by the coupling in layout. In Figure 3.1 and Figure 3.2, the SNR of the transmitting signal in Path1 can be simply defined as follows:

$$\text{SNR\_dB} = 20\log\frac{A_1}{kA_2} \tag{3.3}$$

where k is the coupling factor between the signal paths, which is dependent on the operating frequency, the length of the signal paths and spacing between the paths. Assuming the transmitting signals in Path1 and Path2 have the same amplitude and bandwidth,

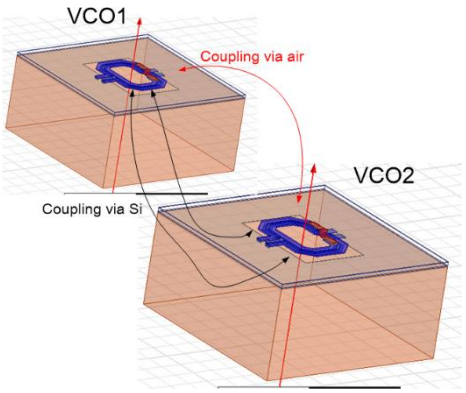
$$\text{SNR\_dB} = -20\log k\,. \tag{3.4}$$

Then,

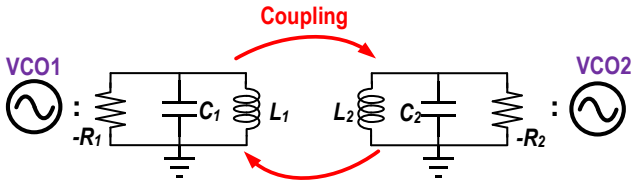
$$EVM_{rms,avg} = 100\% \cdot \sqrt{\frac{1}{SNR}} = 100\% \cdot \sqrt{k} \,. \tag{3.5}$$

Thus, without considering the amplitude of the transmitting signals, EVM is mainly dependent with the coupling factor between the signal paths, and crosstalk is a dominant contributor to EVM. As analysed in above, for 802.11ax system, to ensure a good EVM performance, the SNR should be above 50 dB, which means the coupling factor is required to be lower than 50 dB (0.0032).

3.2 VCO pulling



(a)



(b)

Figure 3.6. Coupling between two VCOs.

In transmitter supporting multiple carriers, two or more PLLs are integrated on the same substrate and operate concurrently. Due to the coupling between VCOs through the substrate and electromagnetic radiation, as shown in Figure 3.6, the oscillators undergo a mutual interaction between each other, resulting in unwanted sidebands or spurs at the oscillators' output, which is called VCO pulling [5]-[7], [40], [41]. These resulted

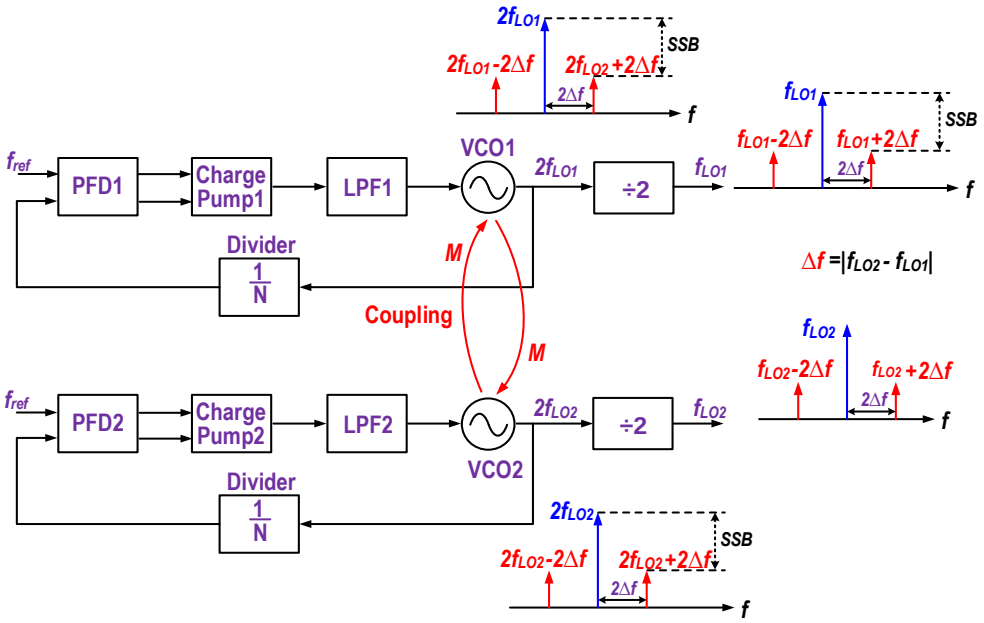


Figure 3.3. VCO pulling between PLLs.

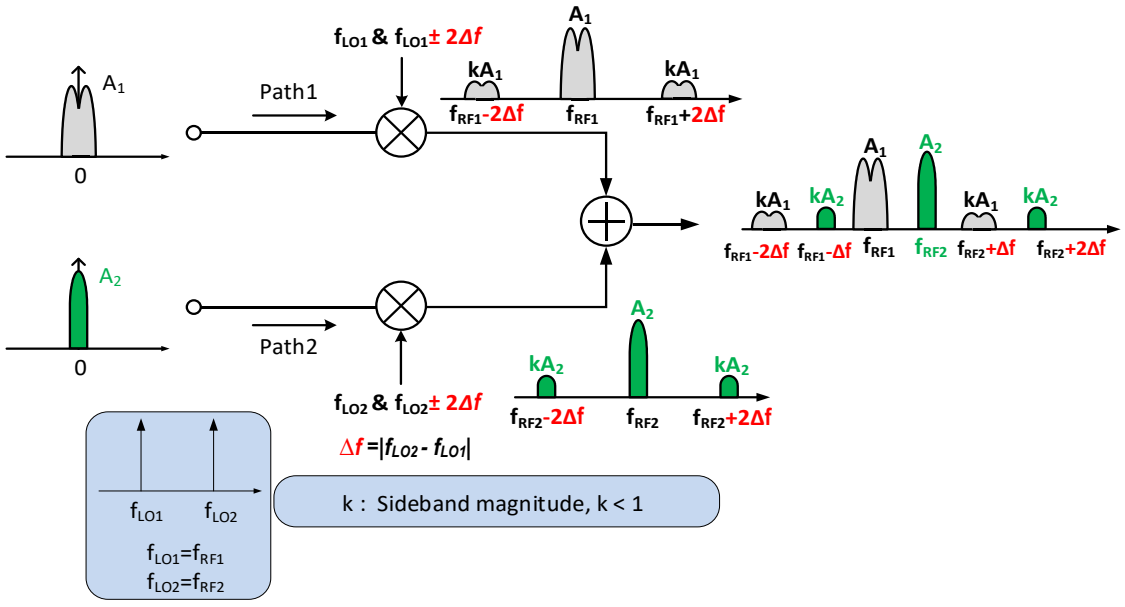


Figure 3.4. Effect of VCO pulling on transmitter for carrier aggregation.

sidebands or spurs are at an offset equal to the frequency spacing between the PLLs' outputs, as shown in Figure 3.7. As a result, for the mixer in each path, there are three LO signals, one desired LO, and two interferences caused by VCO pulling. Then, these three LO signals will produce three RF output signals after the mixer, one desired RF output and two interferences, as illustrated in Figure 3.8. Due to these interferences, the

requirement of emission mask for 5-GHz 802.11ax may not be satisfied. For contiguous carrier aggregation, these two resulted inferences will be located in the lower and upper adjacent channels of the desired carriers, thus ACLR will degrade, which is the worst case for the effect of VCO pulling on transmitter's output spectrums.

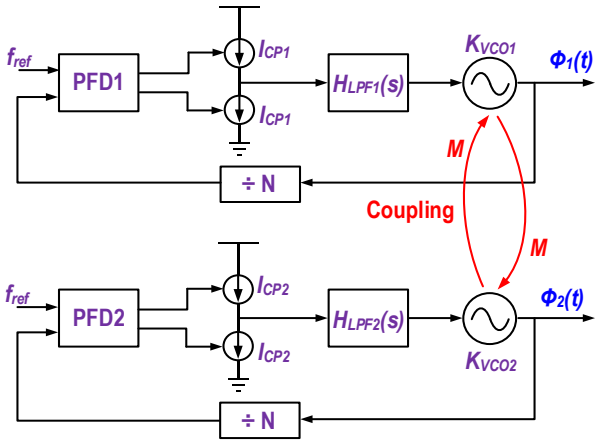


Figure 3.9. Model of VCO pulling between two PLLs.

To evaluate the effect of VCO pulling, it is critical to estimate the magnitude of the sidebands. In Figure 3.9, the output phases of the PLLs in time domain, $\Phi_1(t)$ and $\Phi_2(t)$ can be expressed as [7]

$$\Phi_1(t) = \omega_1 t + \theta_1 + \Delta\Phi_1(t) \tag{3.6}$$

$$\Phi_2(t) = \omega_2 t + \theta_2 + \Delta\Phi_2(t) \tag{3.7}$$

where ω_1 and ω_2 are the desired angular frequencies of the two PLLs' outputs, θ_1 and θ_2 are dictated by the phases of the reference clocks as well as the delays caused by the charge-pump and divider, and $\Delta\Phi_1$(t) and $\Delta\Phi_2$(t) represent the phase perturbations caused by VCO pulling, respectively.

The differential forms of (3.6) and (3.7) are as follows:

$$\frac{d\Phi_1(t)}{dt} = \omega_1 + \frac{d\Delta\Phi_1(t)}{dt} \tag{3.8}$$

$$\frac{d\Phi_2(t)}{dt} = \omega_2 + \frac{d\Delta\Phi_2(t)}{dt}. \tag{3.9}$$

$\frac{d\Delta\Phi_1(t)}{dt}$ and $\frac{d\Delta\Phi_2(t)}{dt}$ can be derived as:

$$\frac{d\Delta\Phi_1(t)}{dt} = -K_{VCO1}\frac{I_{CP1}}{2\pi}\frac{\Delta\Phi_1(t)}{N_1} * h_{LPF1}(t) + \frac{k\omega_1}{2Q_1}\sin\left(\Delta\omega t + \theta_2 - \theta_1\right) \quad (3.10)$$

$$\frac{d\Delta\Phi_2(t)}{dt} = -K_{VCO2}\frac{I_{CP2}}{2\pi}\frac{\Delta\Phi_2(t)}{N_2} * h_{LPF2}(t) - \frac{k\omega_2}{2Q_2}\sin\left(\Delta\omega t + \theta_2 - \theta_1\right) \quad (3.11)$$

where $\Delta\omega = \omega_2 - \omega_1$, K_{VCO1} and K_{VCO2} are the gains of the VCOs, Q_1 and Q_2 are the *LC* tank's quality factors in the VCOs, k is the coupling factor between the VCOs, I_{CP1} and I_{CP2} are the magnitudes of the charge-pump currents, N_1 and N_2 are the division ratios of the dividers, $h_{LPF1}(t)$ and $h_{LPF2}(t)$ are the transfer functions of the loop filters in the two PLLs, respectively. The closed form solutions of (3.10) and (3.11) are derived by the following equations:

$$\Delta\Phi_1(t) = \frac{-jk\omega_1 e^{j(\theta_2-\theta_1)}}{2Q_1} \times \left.\frac{e^{st}}{s + \frac{I_{CP1}}{2\pi}\frac{K_{VCO1}}{N_1}H_{LPF1}(s)}\right|_{s=j\Delta\omega} \quad (3.12)$$

$$\Delta\Phi_2(t) = \frac{jk\omega_2 e^{j(\theta_2-\theta_1)}}{2Q_2} \times \left.\frac{e^{st}}{s + \frac{I_{CP2}}{2\pi}\frac{K_{VCO2}}{N_2}H_{LPF2}(s)}\right|_{s=j\Delta\omega}. \quad (3.13)$$

For simplicity, assuming the two PLLs have the same parameters, the sidebands' magnitude can be approximately predicted by

$$M_{SB}(\Delta\omega) = \frac{k\omega_0}{2Q}\left.\frac{1}{s + \frac{I_{CP}}{2\pi}\frac{K_{VCO}}{N}H_{LPF}(s)}\right|_{s=j\Delta\omega}. \quad (3.14)$$

According to (3.14), increasing the quality factor Q of the *LC* tank can reduce the VCO pulling effect. However, in a bulk CMOS technology, the quality factor of the inductor cannot be very high. Thus, it is not feasible to alleviate VCO pulling mainly through

increasing the quality factor of the VCOs. In addition, reducing the coupling factor between two VCOs can effectively lower the unwanted sidebands, which can be done by increasing the physical spacing between two VCOs, placing ground shielding around the *LC* tank and using separated DC supply and ground for each VCO [7], [8]. Moreover, the sidebands' magnitude becomes lower with the increase of the frequency spacing between the VCOs.

To roughly evaluate the sidebands' magnitude for practical mutual pulling PLLs, a calculation has been performed according to (3.14), based on a reasonable assumption of the PLL parameters. The parameters of the PLLs are assumed: K_{VCO} = 50 MHz/V, I_{CP} = 50 μA, N = 275, f_0 = 11 GHz, Q = 15. The parameters of the loop filter in the PLLs are assumed: C_1 = 20 pF, R_1 = 150 kΩ, R_2 = 1.5 pF, and its' transfer function is

$$H_{LPF}(s) = \frac{1 + sC_1R_1}{s^2C_1C_1R_1 + s(C_1 + C_2)}. \tag{3.15}$$

With these assumed parameters, the -3-dB closed loop bandwidth of the PLL is 405 kHz, and the loop phase margin is 60.3°. The coupling factor between the two VCOs is assumed to be -50 dB, which is also a reasonable value for practical cases. The calculated result is plotted in Figure 3.10 for Δf varying from 1 MHz to 200 MHz. Obviously, increasing the frequency spacing between the VCOs can significantly reduce the sideband magnitude. For 80 + 80 MHz contiguous carrier aggregation in the 802.11ax system, the sidebands' magnitude is -42.8 dB from Figure 3.10. Considering the effect of VCO pulling, the spectrum for 80 + 80 MHz contiguous carrier aggregation is illustrated in Figure 3.11. Referring to the spectral mask for 80 + 80 MHz contiguous carrier aggregation shown in Figure 3.12, -42.8-dB sideband can satisfy the spectral mask, though, there is almost no margin of the noise and non-linearity for circuits in transmitter. To ensure good ACLR performance, the isolation between the VCOs has to be lower

than -50 dB, requiring a large physical isolation in practical layout.

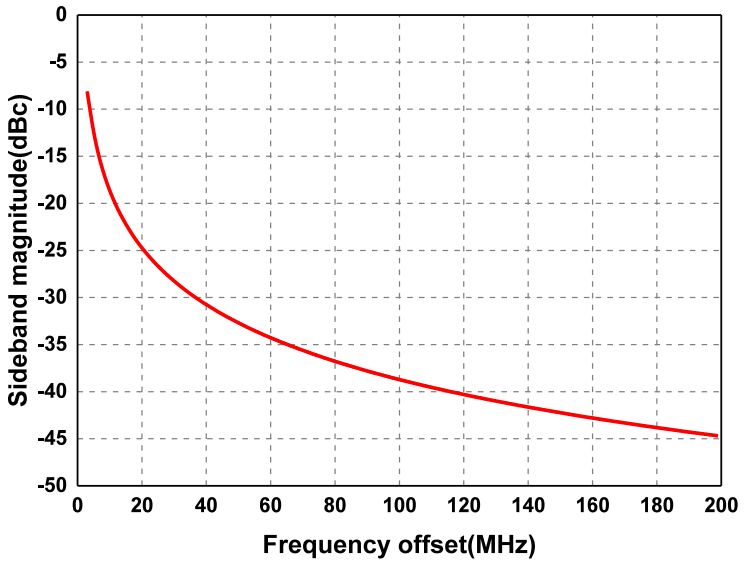


Figure 3.10. Simulated magnitude of sideband for pulling PLLs' output with frequency offset.

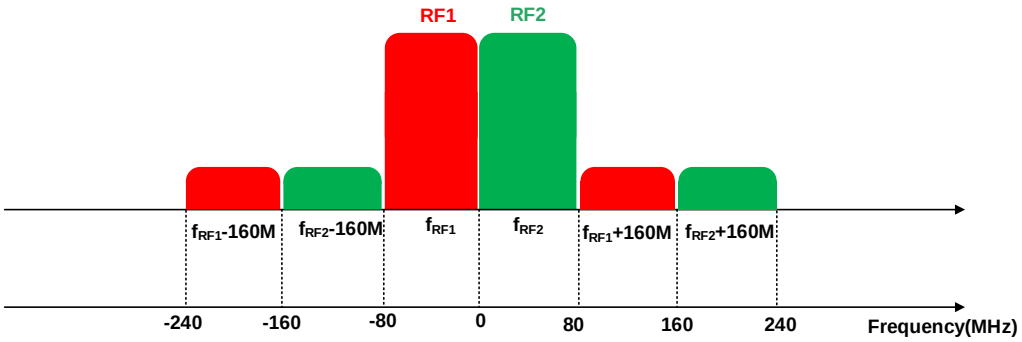


Figure 3.11. Spectrum for 80 + 80 MHz contiguous carrier aggregation.

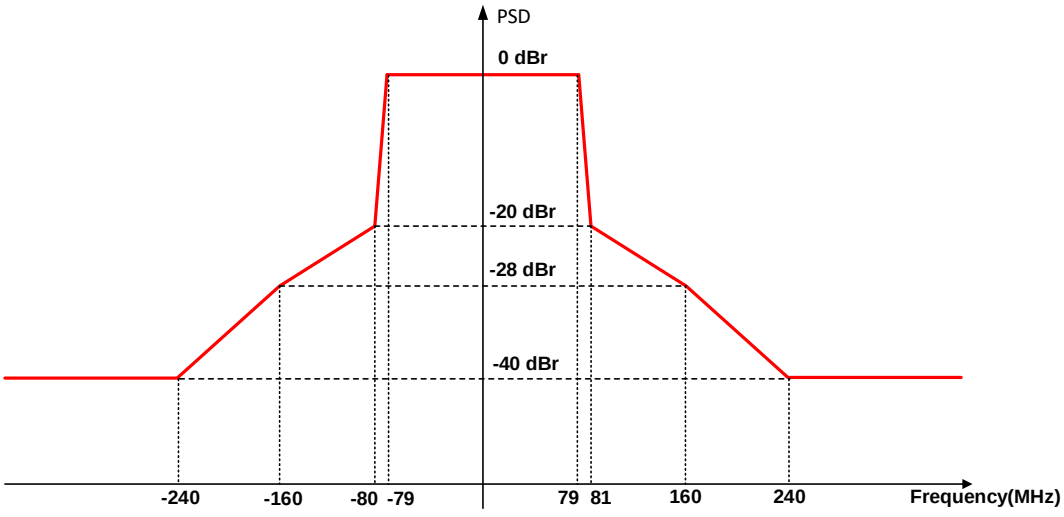


Figure 3.12. Spectral mask for 80 + 80 MHz contiguous carrier aggregation.

In some practical cases where a large physical isolation cannot be achieved, increasing the frequency spacing between two VCOs is an effective approach to solve the problem of VCO pulling. In [8], the division ratio of the divider in one path is the double of the division ratio of the divider in the other path. Accordingly, one VCO operates at twice the operating frequency of the VCO in the other path. In this way, a large frequency separation can be obtained when supporting contiguous carrier aggregation. Although the approach used in [5] to achieve a large frequency separation is feasible for LTE-A with the operating frequency below 3 GHz, it is not suitable for 802.11ax in the 5-GHz WLAN band of 5.17-to-5.835 GHz. Such approach will require a PLL with the frequency as high as 23.34 GHz, which drastically intensifies the PLL's design complexity. Besides, the power consumption of the PLL and divider operating in such high frequency from 20.68 to 23.34 GHz will be higher.

3.3 Coupling factor between two channels in layout

3.3.1 Coupling factor between two active devices

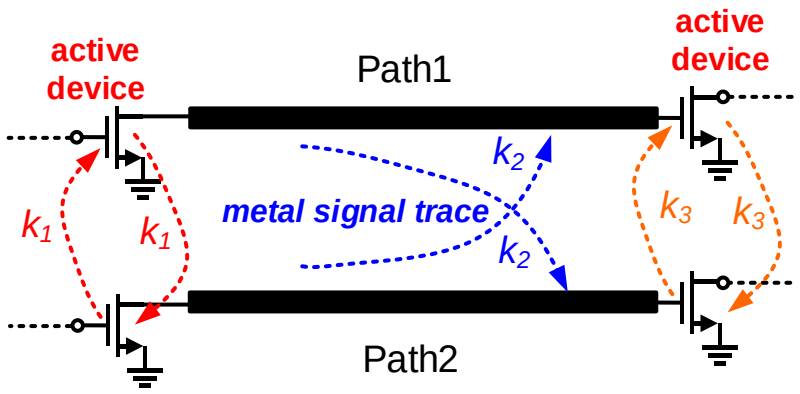
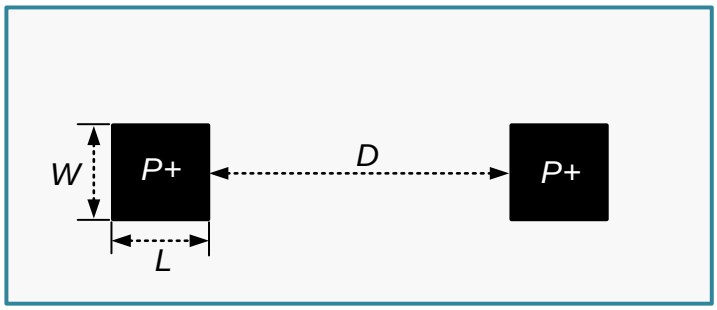


Figure 3.13. Coupling between active devices and between metal signal traces.

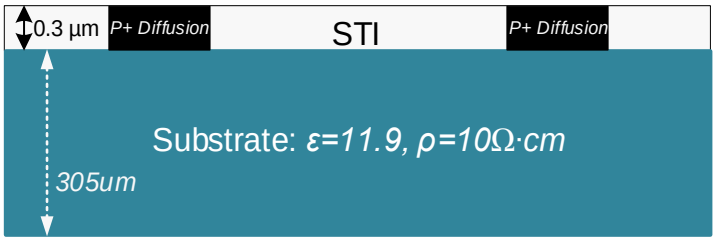
To characterize the coupling factor in practical layout, some physical models are created to simulate the coupling factor in TSMC 40-nm CMOS 1P10M technology. The coupling exists between the devices and between the metal signal traces in practical

layout, as shown in Figure 3.13. Thus, the coupling factor is categorized into two types to investigate: the coupling factor between the active devices and the coupling factor between the metal signal traces.

First of all, we investigate the coupling factor between the two actives with different sizes and spacings [42]-[47]. In practice, one transistor may have a large number of fingers, then the width or length of one transistor's layout may reach 100 μm or even become larger than 100 μm, thus it is not feasible to accurately model the transistors in simulating the coupling factor. On the other hand, if the coupling exists between the two RF channels through the active devices, all the transistors used in the two channels will undergo the coupling. Take the LO coupling for example, all the transistors used in the mixers and LO generation circuits will undergo the coupling. In general, it is not easy to simulate the coupling factor for a practical transmitter layout accurately. For simplicity, the active devices are modelled as a rectangle shape with P+ diffusion in the simulation, and Figure 3.14 demonstrates the model of the two active devices in TSMC 40-nm CMOS technology. In this technology, the thickness of the substrate is 305 μm, and the relative dielectric constant and resistivity of Si substrate are 11.9 and 10 Ω·cm, respectively. Shallow trench isolation (STI) is used to prevent the electric current leakage and increase the isolation between the adjacent active devices in horizontal direction. Although STI can provide isolation in some degree, the coupling through the substrate underneath the active devices is still unavoidable, shown in Figure 3.15.



(a)



(b)

Figure 3.14. Model of two active devices in TSMC 40-nm CMOS technology. (a) Top view. (b) Cross-sectional view.

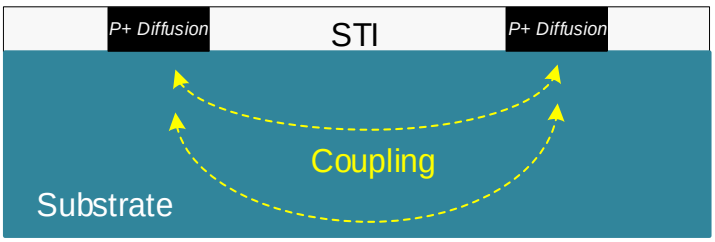


Figure 3.15. Coupling through substrate between active devices.

The simulation has been performed in the EM simulation software HFSS V15. The screenshot of the simulation model in HFSS is shown Figure 3.16. The solution type is 'Driven Terminal', and the excitation is 'waveport'. The simulated coupling factors for some cases with different width, length and spacing are plotted in Figure 3.17. Seen from

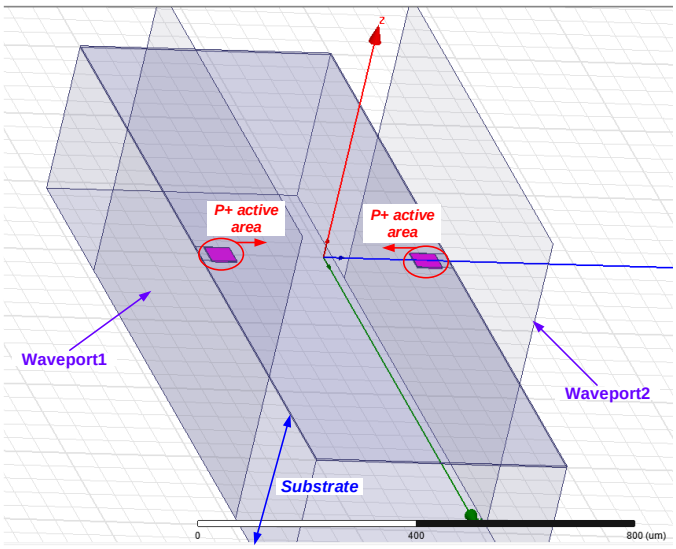


Figure 3.16. Simulation model in HFSS.

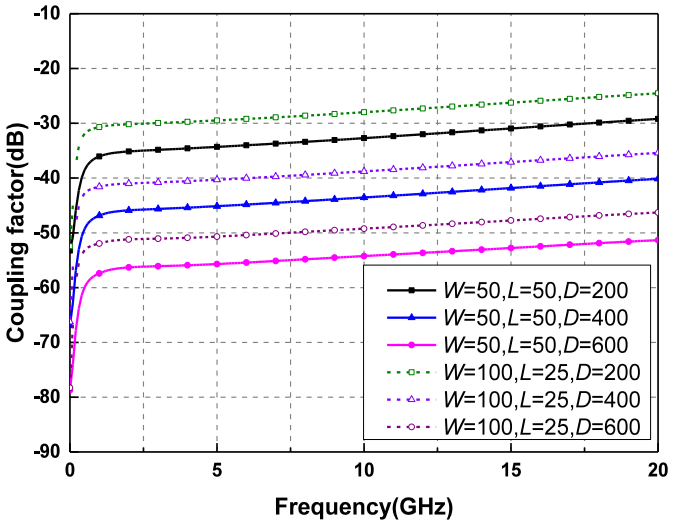
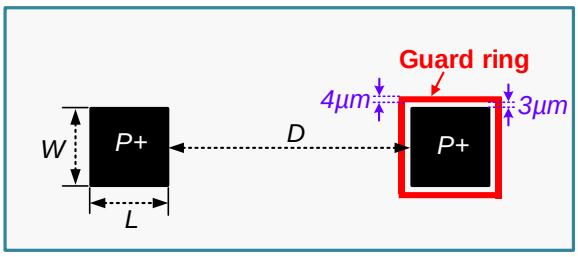


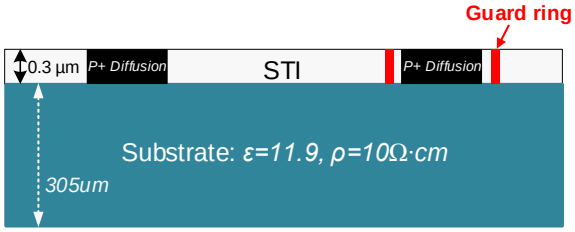
Figure 3.17. Simulated coupling factor between two active devices.

Figure 3.17, the coupling factor is dependent on the area of the active device and the spacing between the devices. Besides, the coupling factor becomes a slightly higher as the frequency increases, showing the portion of the coupling caused by the near field electromagnetic radiation increases when the frequency becomes higher. Obviously, increasing the physical spacing between the active devices is an effective approach to reducing the coupling. For the active device with a length of 25 μm and a width of 100 μm, the physical spacing is required to be larger than 400 μm to ensure the coupling factor below -50 dB. If accounting for the active devices in the whole transmitter path, the total equivalent size of all active devices undergoing coupling will become quite large. Consequently, in order to guarantee low coupling to achieve a good EVM performance, the physical isolation may be required to be larger than hundreds of micrometres, when only considering the coupling between active devices. While, the spacing of hundreds of micrometres may not be realizable in some practical cases due to the constraint of layout.

In general, the guard rings used in various places in CMOS circuit design may provide electrical isolation of circuit functions and prevent undesirable interaction between devices and circuits. In addition, it is also believed that the guard rings improve layout



(a)



(b)

Figure 3.5. Model to simulate coupling factor with one active is surrounded by a guarding ring. (a) Top view. (b) Cross-sectional view.

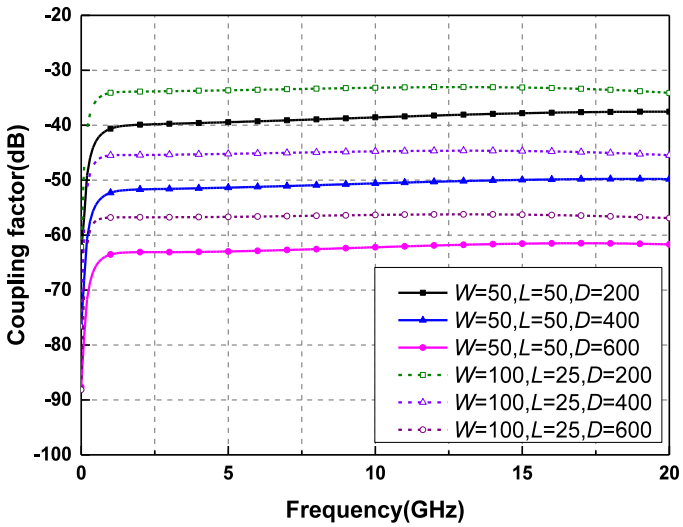
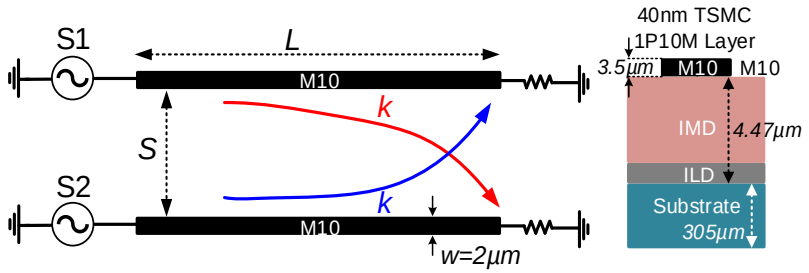


Figure 3.6. Simulated coupling factor between one active device and the other active device with guard ring.

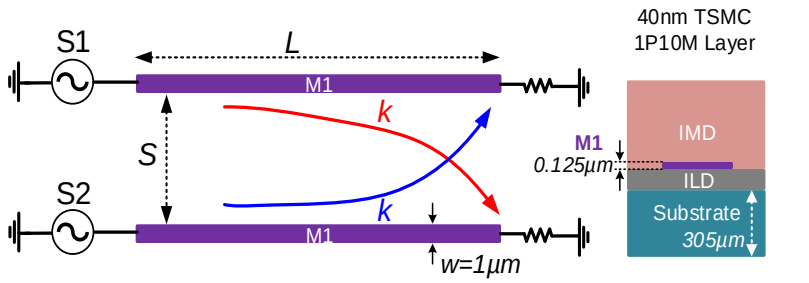
matching as well. Thus, it is desirable to investigate the effect of the guard ring on improving the isolation. We have simulated the coupling factor for the case that one active device is surrounded by a P+ guard ring, and Figure 3.18 shows the physical model

in the simulation. Here, only one active is surrounded by the guard ring in order to investigate how much isolation one guard ring can provide. In Figure 3.18, the width of the guard ring is 4 µm and the spacing between the active device and the guard ring is 3 µm, and these two parameters are reasonable in practical layout. The simulated coupling factors are reported in Figure 3.19. Compared with the simulated coupling factors shown in Figure 3.17, the guard ring can provide 7-10 dB isolation. Although adding a guard ring can help to increase isolation, it cannot ensure sufficiently high isolation in some practical cases.

3.3.2 Coupling factor between two metal signal traces



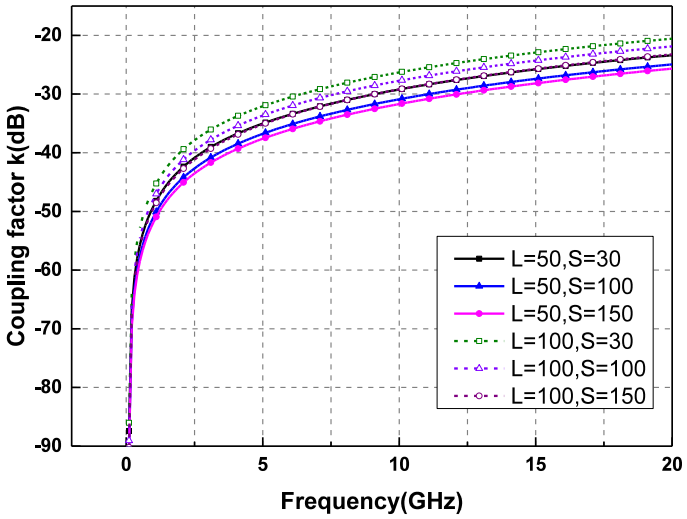
(a)



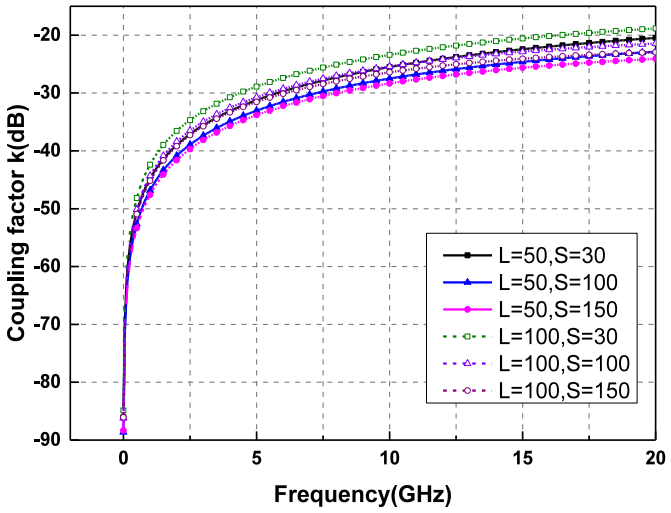
(b)

Figure 3.7. Model to simulate coupling factor for single ended signal traces. (a) Top metal M10. (b) Bottom metal M1.

Besides the coupling between the active devices through the substrate, it is critical to analyze the coupling between the metal signal traces, which is another main contributor to crosstalk. In practical layout, single ended and differential signal traces are both used.



(a)

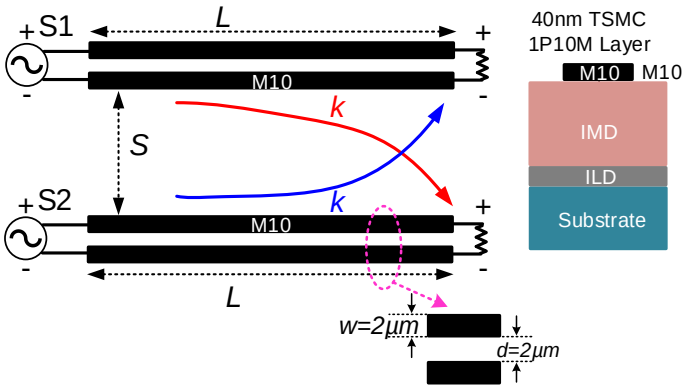


(b)

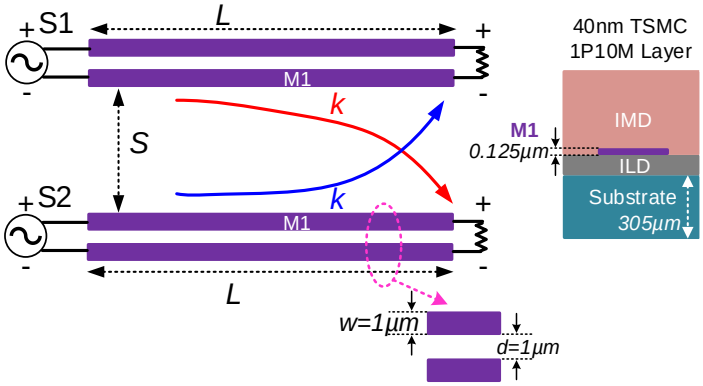
Figure 3.8. Simulated coupling factor with different length and spacing for single ended. (a) Top layer metal M10. (b) Bottom layer metal M1.

Thus, the simulations are performed for these two types of signal traces.

In the simulation, the signal traces using the top metal and bottom metal are both considered in the simulations. The physical models of the single ended signal traces are depicted in Figure 3.20. In Figure 3.20(a), the thickness and the width of the top layer (M10) metal are 3.5 μm and 2 μm, respectively; In Figure 3.20(b), the thickness and the width of the bottom layer (M1) metal are 0.125 μm and 1 μm, respectively. In practice,



(a)

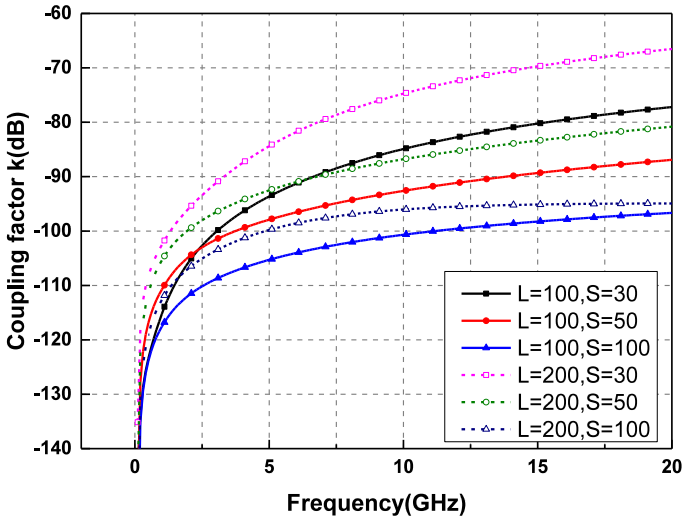


(b)

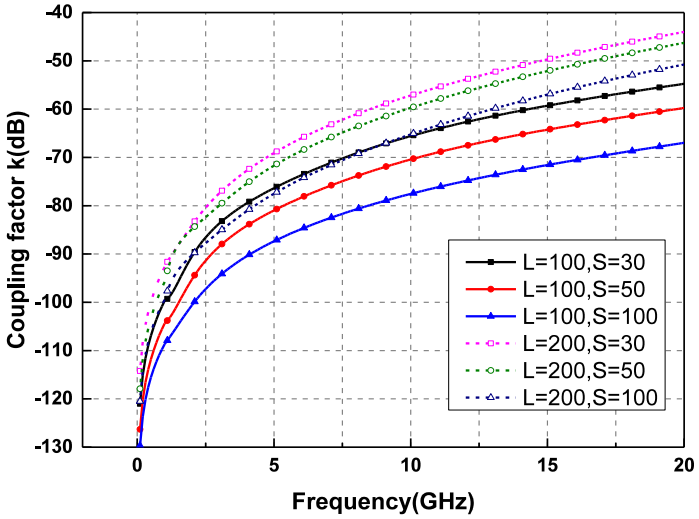
Figure 3.9. Model to simulate coupling factor for differential signal traces. (a) Top layer metal M10. (b) Bottom layer metal M1.

to reduce the parasitic capacitance as much as possible, no ground metal is placed under the metal signal traces in most cases. Hence, there is no ground under the simulated signal traces in the model shown Figure 3.20(a). Figure 3.21 plots the simulated coupling factors with the frequency for different length *L* and spacing *S*. Obviously, longer coupling path and smaller spacing produce higher coupling factor. More importantly, the coupling factor is proportional to the frequency, since the electromagnetic coupling becomes strong and dominant in high frequency. Comparing the simulated results in Figure 3.21(a) and the simulated results in Figure 3.21(b), the signal traces using the top metal layer have a coupling factor lower than the signal traces using the bottom metal layer by 3-5 dB. The reason for that is the bottom layer is closer to the substrate and it is

easier for the signal to leak into the other path through the substrate. Therefore, practically speaking, upper layer metal is recommended for signal trace, rather than lower layer metal, based on the consideration of leakage or coupling.



(a)



(b)

Figure 3.23. Simulated coupling factor with different length and spacing for differential signal traces. (a) Top layer metal M10. (b) Bottom layer metal M1.

In practical circuits, differential signal traces are more widely used than single-end signal traces. The coupling factor between two differential traces are simulated, and the model used for the simulation is shown in Figure 3.22. The simulation results are

illustrated in Figure 3.23. Compared with the simulated results for the single-ended traces shown in Figure 3.21, the differential signal traces have a remarkable anti-interference ability. The reason is that the polarity of the two metal lines in one differential pair is opposite, their external electromagnetic fields can cancel each other out and much less electromagnetic energy is leaked to the outside. Moreover, it is worth noting that the differential signal traces using the top layer metal can significantly improve the isolation by 20 dB, in comparison with the differential signal traces using the bottom layer metal. Thus, the differential signal traces using the top layer metal are superior to other types of the signal traces in the performance of isolation.

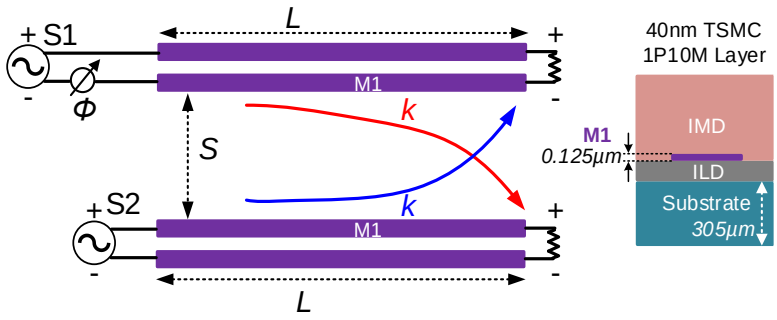


Figure 3.24. Model to simulate coupling factor for non-ideal differential signal traces.

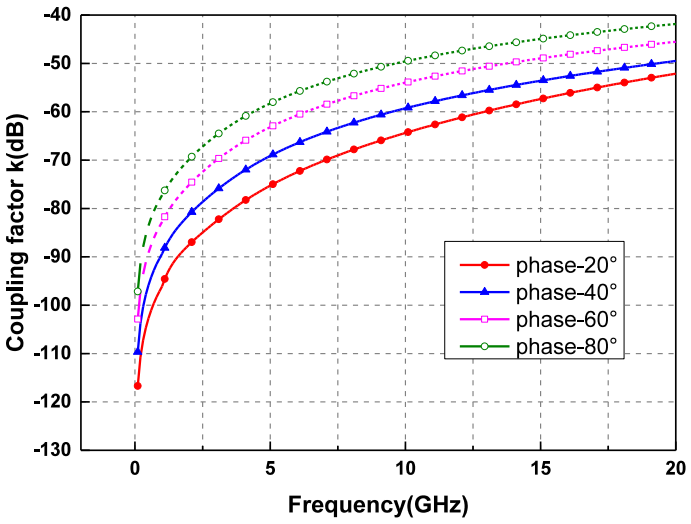


Figure 3.25. Simulated coupling factor for L=200, S=100 μm with different phase deviation.

On the other hand, due to the inevitable mismatch and asymmetry in practical layout,

the signals cannot keep ideally differential along the whole signal path. Here, considering the signals are non-ideally differential, a phase-shifter is introduced to the model to emulate the phase deviation, as shown in Figure 3.24. The simulated coupling factors for L = 200 μm, S = 100 μm with different phase deviations are illustrated in Figure 3.25. As observed, the phase deviation from the ideal differential case has a significant impact on the coupling factor, since the electromagnetic fields leaked to the outside cannot be perfectly cancelled out when the polarity of the two lines in the differential pair is no longer ideally opposite. Therefore, using differential signal traces with less phase deviation can effectively minimize the interference between metal signal traces.

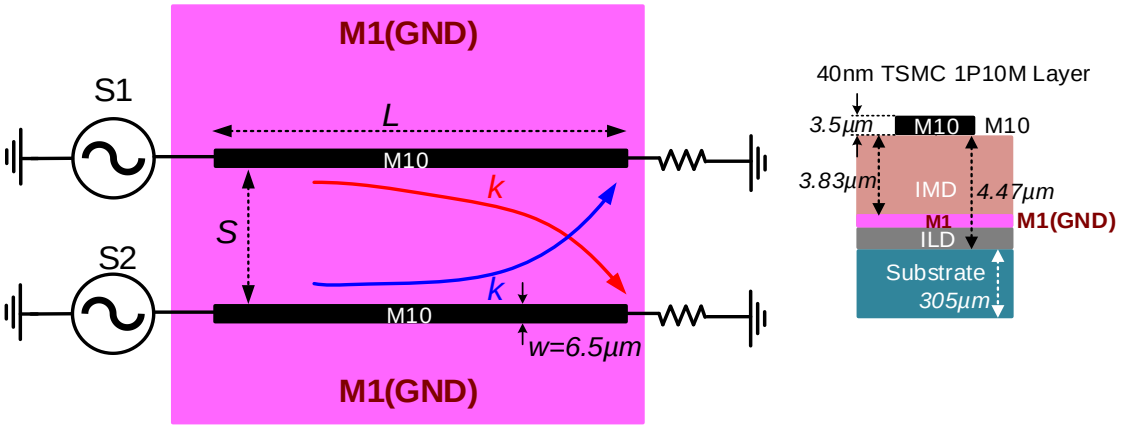


Figure 3.26. Simulation model for coupling factor between two microstrip lines.

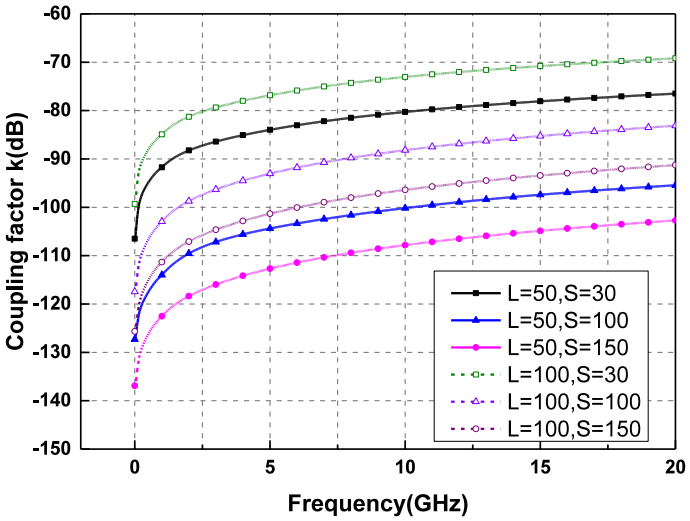


Figure 3.27. Simulated coupling factor between two microstrip lines (unit: μm).

Besides, in high frequency and milli-meter wave circuits, microstrip line and coplanar waveguide (CPW) are another two types of signal traces, which are widely used in the input\output matching networks and signal transmitting path. As the operating frequency of 802.11ax is below 6 GHz and the corresponding frequency of PLL is below 12 GHz, microstrip line and CPW are seldom employed in layout due to the large size in such low frequency. Though, the coupling factor between the signal traces using microstrip line and CPW is still included into the scope of the research of this thesis. In the emerging fifth-generation (5G) communication, carrier aggregation is also an important feature to boost date rate. Thus, 5G CMOS transceiver will encounter the same problem of crosstalk when the function of carrier aggregation is supported. Since the 5G FR2 operates in the 28-GHz and 39-GHz bands, the microstrip line and CPW may be utilized in circuits design, and it is meaningful to simulate the coupling factor between the signal traces using the microstrip line and CPW.

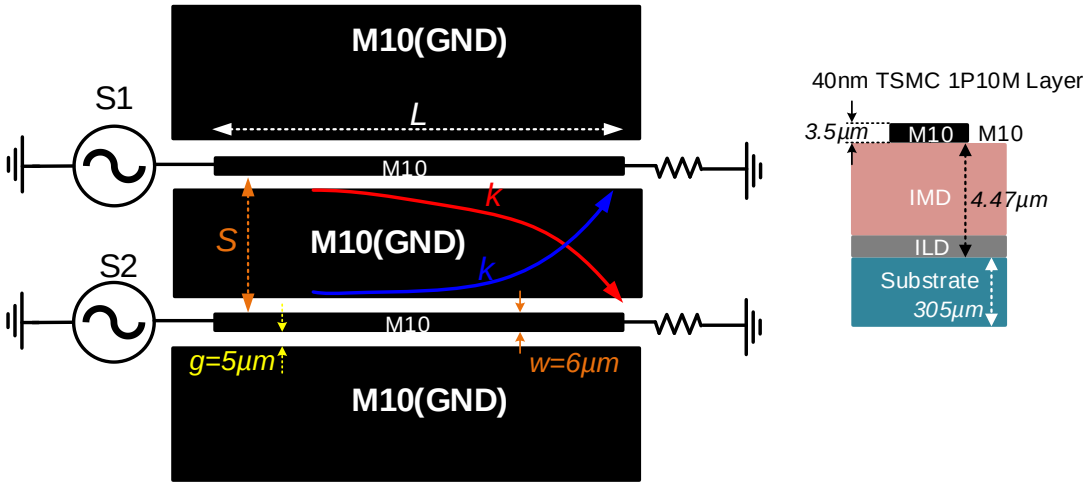


Figure 3.28. Simulation model for coupling factor between two CPWs.

Thus, we have performed two more simulations, one for the coupling between two microstrip lines, and the other for the coupling between two CPWs. Here, for simplicity, we only consideration a general case for the microstrip line with a 50-Ω standard characteristic impedance. The simulation model for the coupling between two microstrip

lines is shown in Figure 3.26. The width of the microstrip lines is 6.5 μm, and the characteristic impedance is 48-52 Ω from 1 GHz to 20 GHz. The simulated coupling factor between these two microstrip lines is plotted in Figure 3.27. The simulation model for the coupling between two CPWs is shown in Figure 3.28. The width of the CPW is 6 μm, and the gap between CPW and GND is 5 μm, and the simulated characteristic impedance of the CPW is 49.5-52.5 Ω from 1 GHz to 20 GHz. Figure 3.29 plots the simulated coupling factor between two CPWs. Seen from Figure 3.27 and Figure 3.29, the coupling factor between the microstrip lines or CPWs are much lower and far below -50 dB even with a large length and a small spacing at high frequency, showing microstrip lines and CPWs have a distinct advantage in anti-interference. However, the large physical size of microstrip line and CPW limits their application in circuits design for low frequency applications including 5-GHz 802.11ax.

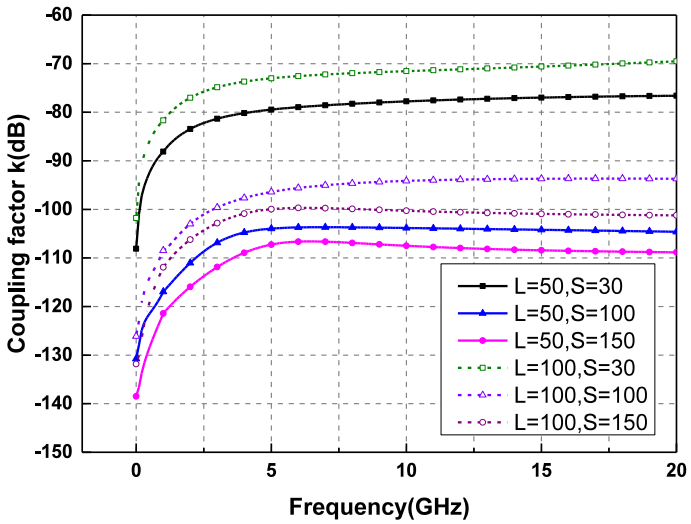


Figure 3.29. Simulated coupling factor between two CPWs (unit: μm).

3.4 Summary

In this chapter, crosstalk and VCO pulling caused by the interaction between two RF channels when the two signals are processed concurrently in one CMOS chip are introduced. Then, the impact of crosstalk on the EVM and the impact of VCO pulling on

the ACLR of the transmitted signals are analyzed. To achieve a good EVM performance for an 802.11ax signal with 256-QAM modulation, at least 50-dB isolation between RF channels is required. For 80 + 80 MHz contiguous intra-band carrier aggregation, 60-dB isolation may be required to minimize the effect of VCO pulling and meet the spectral emission mask. Moreover, to investigate the isolation between two practical RF channels, the coupling strength between the active devices and between the passive signal traces are simulated. The simulation results indicate the physical separation of hundreds of micro-meters is required to ensure a sufficiently high isolation between two RF channels.

Chapter 4

Design of a Transmitter for Carrier Aggregation

In the previous chapters, some transmitter architectures for carrier aggregation are introduced together with their merits and drawbacks, and two intrinsic problems of crosstalk and VCO pulling related to carrier aggregation are discussed, which are caused by the inevitable coupling existing between the signal transmitting channels. The impacts of crosstalk and VCO pulling on EVM and ACLR have been theoretically investigated, proving the isolation between the signal transmitting channels is required to be higher than 50 dB for 5-GHz 802.11ax carrier aggregation. Meanwhile, we have investigated the coupling factor between the active devices and between the metal signal traces, showing a large physical separation is required to ensure a 50-dB isolation. While, in some practical cases, large physical isolation may not be realized by the constraint of layout.

In this chapter, to address the problems of crosstalk and VCO pulling without a high on-chip isolation, a novel transmitter architecture using parallel direct-conversion and double-conversion configuration is proposed. The proposed transmitter architecture can support two-carriers aggregation with arbitrary mode for 5-GHz 802.11ax application, and the corresponding mechanism of crosstalk and VCO pulling mitigation is thoroughly analysed. Based on the proposed architecture, a transmitter front-end is designed and implemented in TSMC 40-nm CMOS technology, and the details on the circuits design and the measured performances are included in this chapter.

4.1 Proposed transmitter architecture

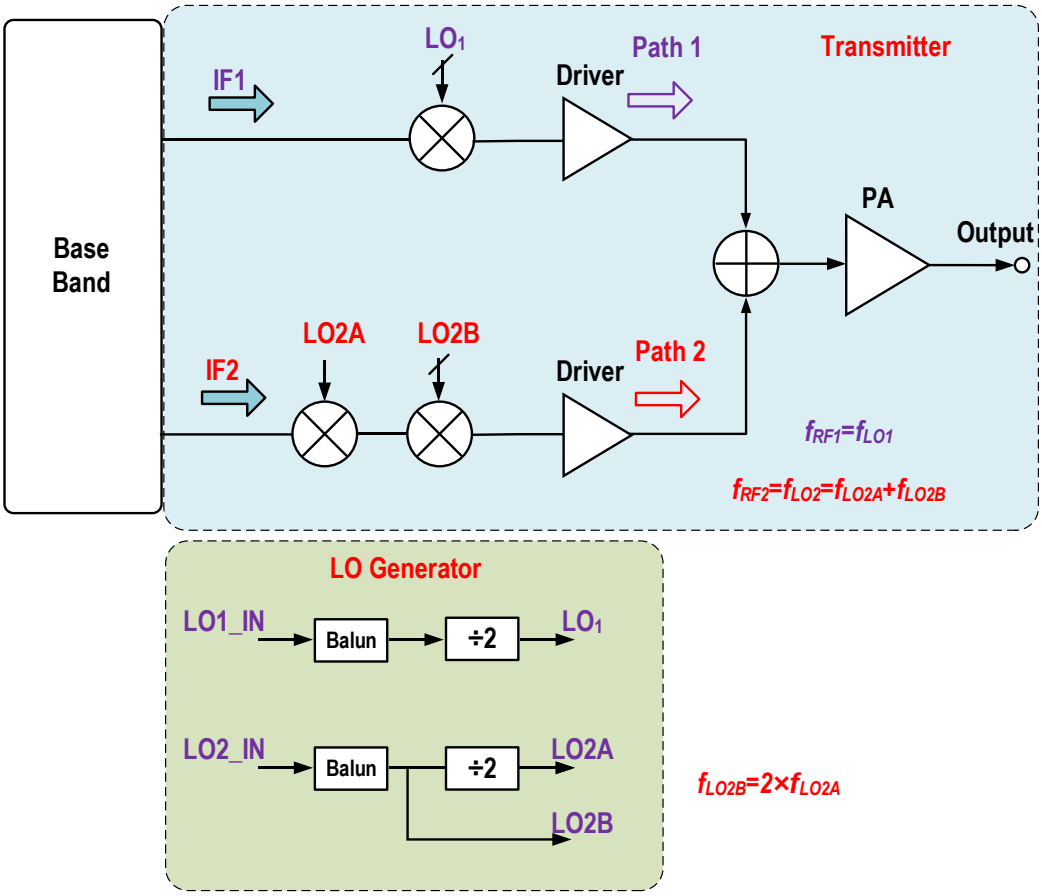


Figure 4.1. Proposed parallel direct-conversion and double-conversion transmitter architecture

The block diagram of the proposed transmitter is shown in Figure 4.1 [9]. This transmitter has two parallel paths, one direct-conversion path and one double-conversion path, thus, two carriers can be processed at the same time. In this architecture, the two carriers are combined after the driver and before injected into the PA. While in [8] and [9], the carriers are combined directly after the up-conversion mixer, and the output ports of the mixers are connected together, leading to no isolation between the mixers in different paths. In the proposed transmitter, a driver is added before the combination of carriers to increase the isolation between the mixers in two paths. Three LO signals (LO1, LO2A and LO2B) are generated from two corresponding LO input signals (LO1_IN and

LO2_IN) to feed the mixers in the two paths. Among these LOs, the frequency of LO2A is half of the frequency of LO2B. The two LO input signals can be provided from external signal sources or from integrated on-chip PLLs.

4.2 Mechanism of VCO pulling mitigation

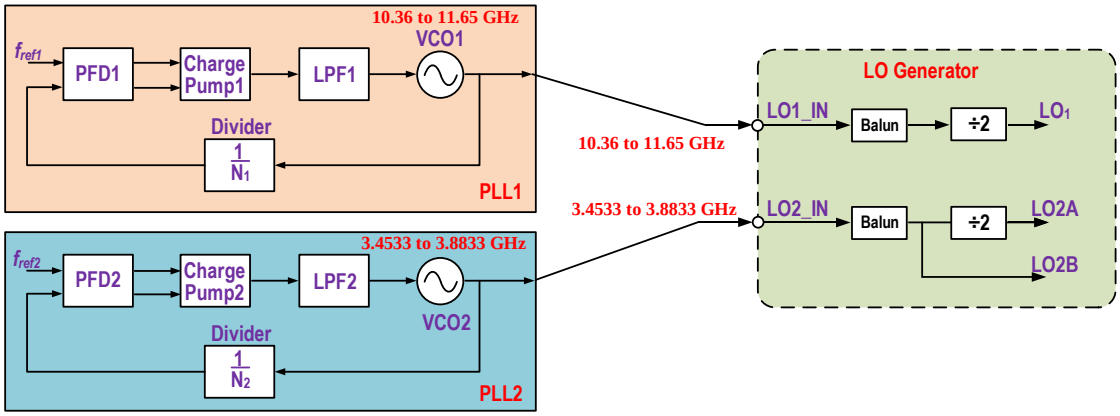


Figure 4.2. Diagram of LO generator with PLLs integrated on-chip.

Frequency planning is critical in the proposed transmitter to avoid the problem of crosstalk and VCO pulling. In order to determine an elaborate frequency plan, two objectives need to be fulfilled. Firstly, all frequencies of VCOs or LO_INs and their harmonics should be kept outside the 5.17-to-5.835 GHz RF band of interest, thus the crosstalk caused by the leakage of VCOs and LO_INs can be avoided. Secondly, the frequency of one VCO or LO_IN and its harmonics are not close to the other VCO's frequency in order to obtain large frequency separation, so that VCO pulling can be suppressed as much as possible. In the proposed transmitter architecture, since

$$f_{LO1} = \frac{f_{LO1\_IN}}{2}$$
$$f_{LO2} = \frac{3 f_{LO2\_IN}}{2}, \tag{4.1}$$

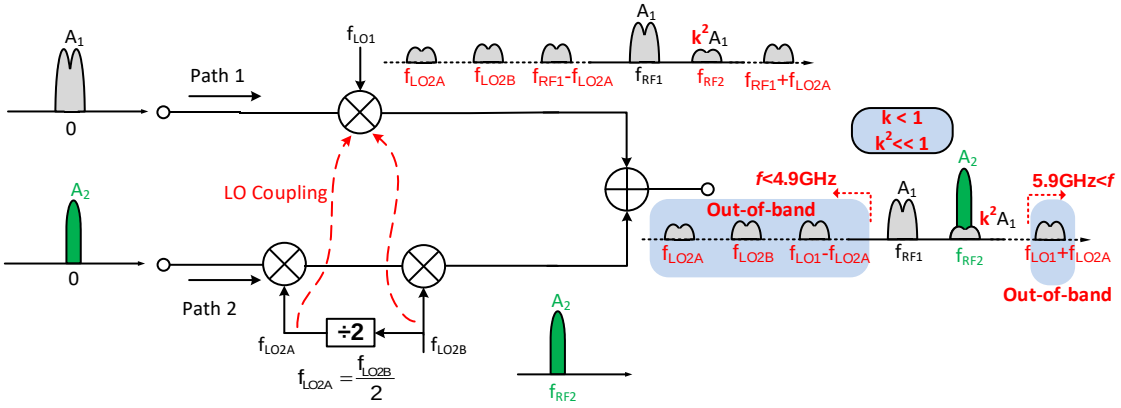
referring to the 5GHz WLAN frequency allocation depicted in Figure 1.2, the frequency of LO1_IN is from 10.36 to 11.65 GHz, the frequency of LO2_IN is from 3.4533 to

3.8833 GHz, respectively. If these two LO input signals are provided from two internal integrated PLLs, the operating frequencies of the VCOs in the two PLLs will be 10.36-11.65 GHz and 3.4533-3.8833 GHz, respectively, as shown in Figure 4.2. In such case, the frequency spacing between the operating frequencies of the two VCOs is 6.4767 GHz at least. Since the frequency ranges of these two VCOs are far apart from each other, according to the equation (3.15), the effect of VCO pulling is negligible if the two PLLs are integrated on-chip. Therefore, VCO pulling is no longer an issue for the proposed architecture. In [9], we have demonstrated a 3-carriers aggregation transceiver, in which the transmitter architecture is similar to the architecture proposed in this chapter. The measurement results in [9] have verified the problem of VCO pulling can be solved due to a large frequency spacing between the VCOs. In [8], one VCO operates at twice the operating frequency of the VCO in the other path. Thus, the approach to minimize VCO pulling in [8] is increasing the frequency spacing between the two VCOs, which is the same as the approach in our proposed architecture. For the proposed transmitter front-end in this chapter, the two LO input signals are provided from external signal sources, not from internal PLLs. Though, it is undeniable that the proposed transmitter front-end is immune to VCO pulling if the two PLLs are integrated on-chip.

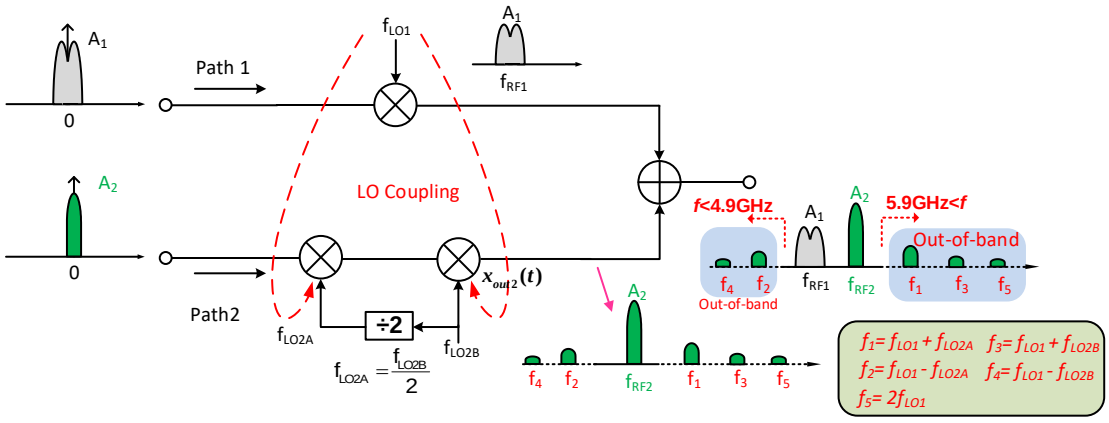
4.3 Mechanism of crosstalk mitigation

From the simulated coupling factors between the active devices and between the passive signal traces in Chapter 3, the coupling factor in the frequency range below 100 MHz is much smaller than that at frequency higher than 5 GHz. For 80 MHz 802.11ax signal, the maximum analog frequency of the baseband signal is only 40 MHz, and it is easy to achieve an isolation above 50 dB for the baseband within 40 MHz even with a long metal signal trace and small spacing between the traces. As a result, in comparison with the LO coupling, the baseband coupling has negligible effect on SNR.

Hence, the baseband coupling is not taken into consideration in the transmitter front-end design in this chapter, and only the crosstalk caused by the LO coupling is considered.



(a)



(b)

Figure 4.3. Mitigation of crosstalk between Path1 and Path2

To explicitly explain the mechanism of mitigation of crosstalk caused by the LO coupling for the proposed transmitter architecture, we firstly consider the LO coupling from Path2 to Path1, as shown in Figure 4.3(a). In Figure 4.3(a), the unwanted signals of LO2A and LO2B both leak from Path2 to the mixer in Path1. As a result, there are three LO signals for the mixer in Path1, f_{LO1}, f_{LO2A} and f_{LO2B}. Then, these three LO signals produce three mixing products with the baseband signal by the direct up-conversion in Path1. Among the resulted mixing products, there are one desired signal and two

interferences with the frequency of f_{LO2A} and f_{LO2B}. Obviously, these two interferences are far away from the 5-GHz WLAN band, having no impact on the SNR of the transmitted signal in Path2. Besides, the three LO signals will mix with each other, resulting in six more mixing products. Among these mixing products, there is only one product falling into the 5-GHz WLAN band, which is the mixing product of LO2A and LO2B. The frequency of this interference is f_{LO2}, the same frequency of the transmitted signal in Path2. After combination, the SNR of the desired signal in Path2 will be affected by this interference, while, the amplitude of this interference is considerably reduced and the impact on the SNR of the transmitted signal can be ignored. Besides the above intuitive analysis, theoretical analysis has to be made to validate that the crosstalk caused by the LO coupling from Path2 to Path1 can be mitigated.

To facilitate the analysis, the two baseband signals and three LO signals are assumed to be:

$$\begin{aligned} BB_1 &= A_1 \cos(\omega_{BB1} t + \varphi_{BB1}) \\ BB_2 &= A_2 \cos(\omega_{BB2} t + \varphi_{BB2}) \\ LO_1 &= \cos(\omega_{LO1} t + \varphi_1) \\ LO_{2A} &= \cos(\omega_{LO2A} t + \varphi_{2A}) \\ LO_{2B} &= \cos(\omega_{LO2B} t + \varphi_{2B}) \end{aligned} \quad . \tag{4.2}$$

Then, the up-converted signal in Path1 can be written as follows:

$$\begin{aligned} x_{out1}(t) = {} & G_1 A_1 \cos((\omega_{BB1} + \omega_{LO1})t + \varphi_1 + \varphi_{BB1}) \\ & + kG_1 A_1 \cos((\omega_{BB1} + \omega_{LO2A})t + \varphi_{2A} + \varphi_{BB1}) \\ & + kG_1 A_1 \cos((\omega_{BB1} + \omega_{LO2B})t + \varphi_{2B} + \varphi_{BB1}) \\ & + kG_1 A_1 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2A})t + \varphi_1 \pm \varphi_{2A} + \varphi_{BB1}) \\ & + kG_1 A_1 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2B})t + \varphi_1 \pm \varphi_{2B} + \varphi_{BB1}) \\ & + k^2 G_1 A_1 \cos((\omega_{BB1} + \omega_{LO2A} \pm \omega_{LO2B})t + \varphi_{2A} \pm \varphi_{2B} + \varphi_{BB1}) \end{aligned} \quad . \tag{4.3}$$

where, G_1 is the gain of the mixer and is assumed to be independent with frequency, k is the coupling factor, and A_1 is the amplitude of the baseband signal BB1. Among $x_{out1}(t)$, the interferences caused by the unwanted LO signals coupling from Path2 exist at

frequencies: $f_{LO1} \pm f_{LO2A}$, $f_{LO1} \pm f_{LO2B}$ and $f_{LO2B} \pm f_{LO2A}$, respectively.

Since
$$\begin{cases} 5.17G \le f_{LO1} \le 5.835G \\ 1.723G \le f_{LO2A} \le 1.945G \\ 3.447G \le f_{LO2B} \le 3.89G \end{cases},$$

$$\begin{cases} 6.893G \le f_{LO1} + f_{LO2A} \le 7.78G \\ 3.225G \le f_{LO1} - f_{LO2A} \le 4.112G \\ 8.617G \le f_{LO1} + f_{LO2B} \le 9.725G \\ 1.28G \le f_{LO1} - f_{LO2B} \le 2.388G \\ 1.723G \le f_{LO2B} - f_{LO2A} \le 1.945G \\ 5.17G \le f_{LO2B} + f_{LO2A} \le 5.835G \end{cases}.$$

Obviously, these interferences at $f_{LO1} \pm f_{LO2A}$, $f_{LO1} \pm f_{LO2B}$ and f_{LO2B}- f_{LO2A} will fall into out-of-band. Only one in-band interference exists at $f_{LO2B} + f_{LO2A}$, and its amplitude is $k^2 G_1 A_1$. Then, the SNR of the transmitted signal in Path2 can be defined as follows:

$$SNR_2 = 20\log\frac{A_2}{k^2 A_1} = 20\log\frac{A_2}{kA_1} + 20\log\frac{1}{k} \tag{4.4}$$

Compared with SNR expressed in (3.3), SNR_2 is increased by $20\log\frac{1}{k}$. Since the coupling factor k is smaller than 1, $20\log\frac{1}{k}$ will be a large positive value and SNR_2 becomes very large. Hence, the LO coupling has a negligible impact on the SNR of the transmitted signal in Path2.

In general, the inter-stage matching networks between the mixer and the driver, and between the driver and the PA form resonant tanks operating within the desired band and have a bandpass filter function. Therefore, in the proposed transmitter architecture, the out-of-band interferences caused by the LO coupling will be suppressed by the following resonant tanks. Besides, the out-of-band interferences can be easily filtered out by external SAW filter.

Secondly, the LO coupling from Path1 to Path2 is considered, as shown in Figure

4.3(b). In Figure 4.3(b), the LO1 leakages from Path1 to Path2, correspondingly, there are two LO signals for each stage mixer in Path2 (LO2A and LO1 for the first-stage mixer, and LO2B and LO1 for the second-stage mixer). Then, these LO signals produce a series of mixing products in the output of the mixer in Path2. As demonstrated in Figure 4.3(b), among all the mixing produces, there is no in-band interference and all interferences fall into out-of-band.

Then, the output signal of the mixer in Path2 can be derived as:

$$\begin{aligned} x_{out2}(t) = {} & G_2 A_2 \cos((\omega_{BB2} + \omega_{LO2A} \pm \omega_{LO2B})t + \varphi_{2A} \pm \varphi_{2B} + \varphi_{BB2}) \\ & + kG_2 A_2 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2A})t + \varphi_1 \pm \varphi_{2A} + \varphi_{BB2}) \\ & + kG_2 A_2 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2B})t + \varphi_1 \pm \varphi_{2B} + \varphi_{BB2}) \\ & + kG_2 A_2 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2A} \pm \omega_{LO2B})t + \varphi_1 \pm \varphi_{2A} \pm \varphi_{2B} + \varphi_{BB2}) \\ & + k^2 G_2 A_2 \cos((\omega_{BB1} + 2\omega_{LO1})t + 2\varphi_1 + \varphi_{BB2}) \\ & + k^2 G_2 A_2 \cos((\omega_{BB1} + \omega_{LO1} \pm \omega_{LO2A} \pm \omega_{LO1})t + \varphi_1 \pm \varphi_{2A} \pm \varphi_1 + \varphi_{BB2}) \end{aligned} \quad (4.5)$$

Among $x_{out2}(t)$, the interferences caused by the LO coupling from Path1 are all out-of-band, indicating that the LO coupling from Path2 has no impact on the transmitted signals.

In conclusion, the proposed parallel direct-conversion and double-conversion configuration can push the interferences caused by the LO coupling into out-of-band; consequently, the transmitter front-end is essentially immune to the problem of crosstalk caused by the LO coupling.

4.4 Transmitter front-end design

Based on the proposed transmitter architecture, a transmitter front-end is designed and implemented in TSMC 40-nm CMOS technology. The block diagram of the transmitter front-end is shown in Figure 4.4, including the LO generator, mixers, drivers and PA. In the transmitter front-end, a 500-bit SPI controller is designed to control the state of the circuit blocks, such as tuning the gain of the mixer, turning on or off the LO balun or divider, and changing the bias of the driver and the PA. To provide the biases for the

mixer, driver and PA, a series of 7-bit DACs using a simple R-2R structure are designed to generate the corresponding bias voltages, which are controlled by the SPI.

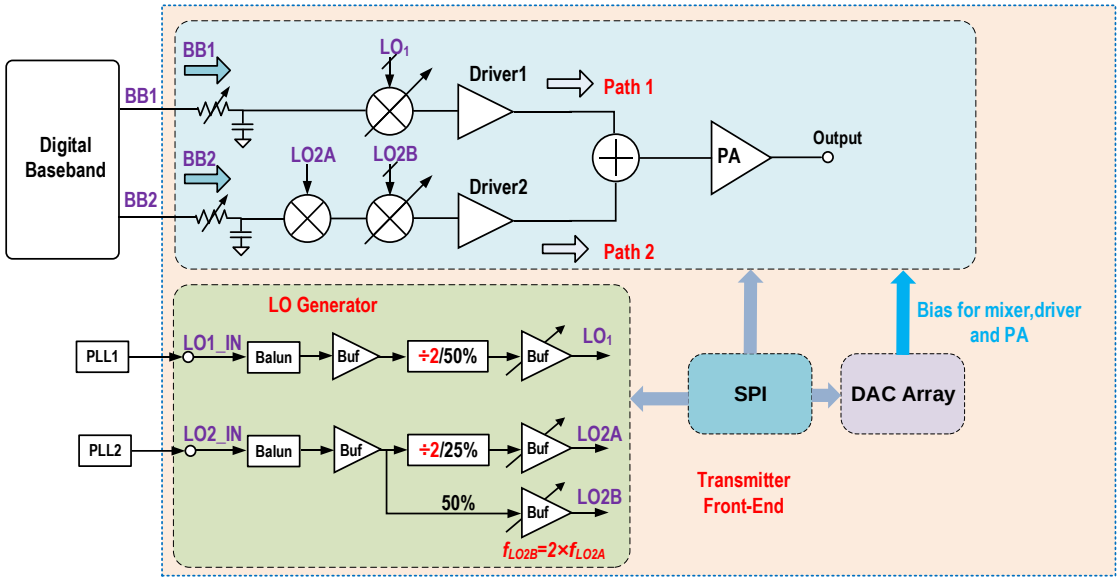


Figure 4.4. Diagram of the proposed transmitter front-end.

4.4.1 Mixer design

Mixers are generally classified as active and passive mixers. Active mixers can provide higher conversion gain and higher port isolation, and requires lower LO power, but have higher noise than their passive counterparts [48], [49]. Passive mixers, on the other hand, typically show conversion loss but exhibit high linearity and low noise at the expense of high LO power requirement and poor port isolation [33]. To overcome conversion loss, passive CMOS mixers are usually followed by gain stages in integrated CMOS transceivers [8], [50]-[55].

Mixer design requires many compromises among different figure of merit such as conversion gain, LO power, linearity, noise figure, port-to-port isolation and total power dissipation. Every type of mixer has its own advantages and drawbacks, so the choice of which type of mixer depends on which performance is priority in design. In the following part, two types of mixer are introduced and their noise performance are analyzed.

4.4.1.1 Active mixer

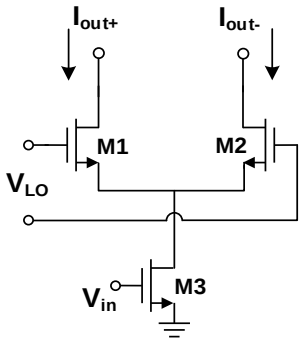


Figure 4.5. Single-balanced mixer.

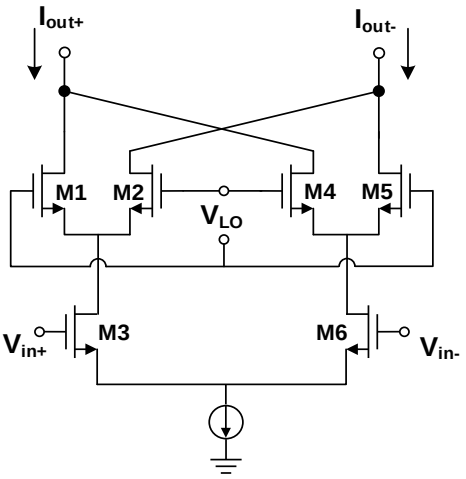


Figure 4.6. Double-balanced mixer.

A single-balanced active mixer is shown in Figure 4.5. In the mixer, the incoming baseband voltage signal is firstly converted into a current signal and then multiplied in current domain. The transistors M1 and M2 are biased slightly above their threshold level. This results in the LO alternatively switching M1 and M2 on and off. Consequently, one LO transistor is always on, while the other LO transistor is ideally off. Since the LO signal can be considered as a square wave consisting of only odd harmonics of the LO frequency, the baseband input current signal is multiplied by the odd-order harmonics of the LO signal, resulting in mixing products to appear at the output RF port. The major disadvantage of this single-balanced mixer is the presence of LO component and unwanted side-band image in the output port. In order to cancel the LO component and

side-band image in the output port, two single-balanced mixers are combined to form a double-balanced mixer. The active double-balanced current switching mixer is also termed as Gilbert mixer as shown in Figure 4.6, which is more widely used in the integrated transceivers than the single-balanced mixer.

In practice, most of the noise of the active mixer is generated by the voltage to current (V-I) conversion circuit. Without considering the noise in the switches, the noise can be approximated as [50]

$$\begin{aligned} N^2 &\approx \left(\frac{4}{\pi}\right)^2 4KT\gamma g_m R_p^2 + 4KT\gamma g_m \\ &= 4KT\gamma \frac{G^2}{g_m} + 4KT\pi \frac{G}{g_m} \\ &= 4KT\left(\gamma \frac{G^2}{g_m} + \frac{\pi G}{g_m}\right) \end{aligned} \tag{4.6}$$

where $G = 4/\pi g_m R_p$, G is the voltage gain of the mixer. To lower the noise in the active mixer, the only approach is to increase g_m and lower the load impedance, leading to lower conversion gain and increased power consumption. In real implementation, in order to meet the requirement of noise floor, tens of mA current have to be consumed.

4.4.1.2 Passive mixer

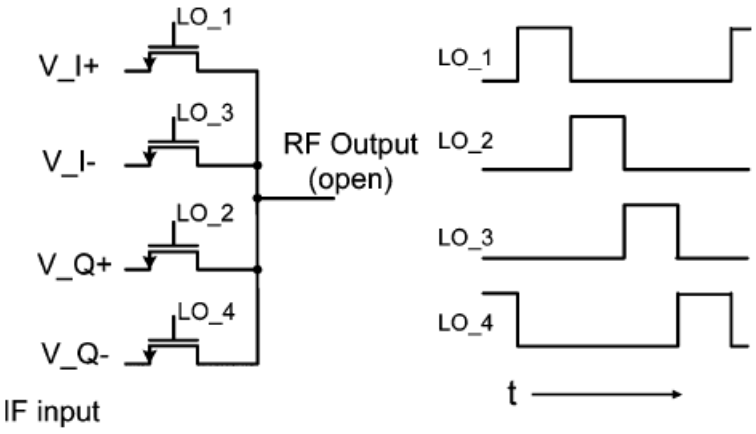


Figure 4.7. Passive mixer [50].

The passive voltage mode mixer consists of four switches which are driven by 25%-

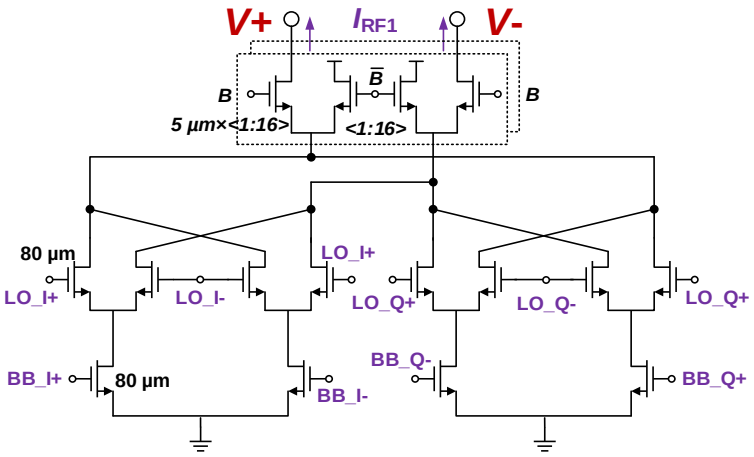
duty-cycle LO [50], [51], as shown in Figure 4.7. By switching on/off the switch transistors through the quadrature-phase LO, the IF quadrature input voltage V_I+, V_I-, V_Q+, V_Q- are sequentially sampled to the voltage mixer output, which sees an open load. Such operation leads to a direct quadrature voltage modulation. Because of the high impedance at the RF output, ideally there is no AC or DC current, and the passive mixer does not consume any power. Without V-I conversion, the thermal noise of the switches' on-resistance mainly contributes to the noise generated in the passive mixer [50], given by

$$\begin{aligned} N^2 &= 4 \cdot 4KTR_{on} \cdot 25\% \\ &= 4KTR_{on} \\ &= \frac{4KT}{u\mathrm{C}_{\mathrm{ox}} \frac{W}{L}(V_{GS} - V_{TH})} \end{aligned} \tag{4.7}$$

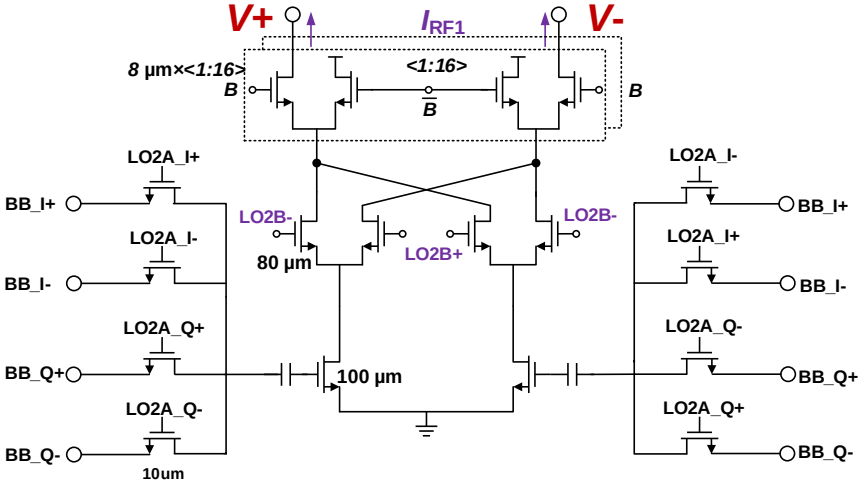
In practical implementation, the on-resistance R_{on} is much smaller than $\gamma \frac{G^2}{g_m} + \frac{\pi G}{g_m}$ in (4.6), thus the passive mixer has better noise performance. Besides, the passive mixer has other superior performance to the active mixer in terms of linearity, LO leakage and linearity. However, the passive mixer has two main problems. First, when the duty cycle of LO is not accurate at 25% or LO has overlap, the I and Q paths crosstalk with each other as a result of the lack of reverse isolation between RF output and baseband input. Second, in order to achieve high SNR of baseband signal, the swing of the baseband should be as high as possible, which requires the mixer switches must bear a very large voltage swing while maintaining high linearity.

4.4.1.3 Proposed mixer circuit design

Considering both advantage and disadvantage of active and passive mixers, the



(a)



(b)

Figure 4.1. Schematic of the proposed mixer. (a) Path1. (b) Path2.

proposed double-conversion mixer in Path2 employs a passive mixer as the first stage and an active mixer as the second stage based on the tradeoff between the conversion gain and the noise performance. If the two stage mixers both employ the passive mixers, the conversion loss will be very large. While, if the two stage mixers both employ the active mixers, high noise will be a problem. The mixer in Path1 uses an active mixer mainly based on the consideration of the conversion gain and the port isolation. The schematics of the proposed mixers are shown in Figure 4.8. The passive mixer is driven

by a 25%-duty-cycle clock, while the active mixers are driven by a 50%-duty-cycle clock. A 5-bit current-steering gain control unit is used in each mixer, and the range of the control gain is around 24 dB [58], [59]. In order to keep sufficient voltage headroom, the supply voltage for the mixers is chosen to be 1.8 V.

Since the second stage active mixer in Path2 is not IQ mixer, there are two identical mixing products at the output of the second stage active mixer: one required signal at the frequency of $f_{LO2B}+f_{LO2A}$ (5.17 to 5.835 GHz) and one unwanted image at the frequency of $f_{LO2B}-f_{LO2A}$ (1.7266 to 1.9417 GHz). This image increases the power consumption of the second stage active mixer, which is the main impact on the second mixing stage. In the transmitter, the mixer is followed by the driver and the PA, and there are three transformers after the mixer, forming three resonant tanks, which can suppress the magnitude of the unwanted image.

4.4.2 LO input balun design

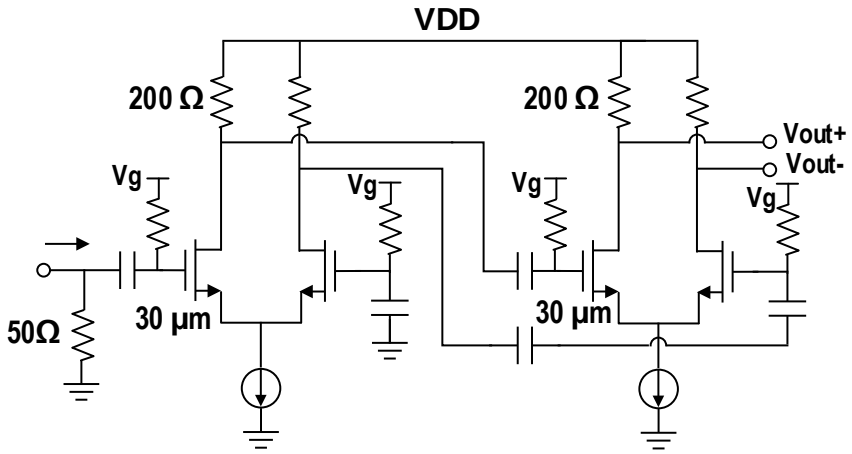


Figure 4.9. Schematic of the active balun.

Since the LO input signal is provided from external signal source, a balun is required to convert the single-ended LO input signal to the differential signals. Passive baluns are the most popular choice, which are often implemented by a passive transformer or coupler. However, in the frequency range below 11 GHz, passive baluns may not have a

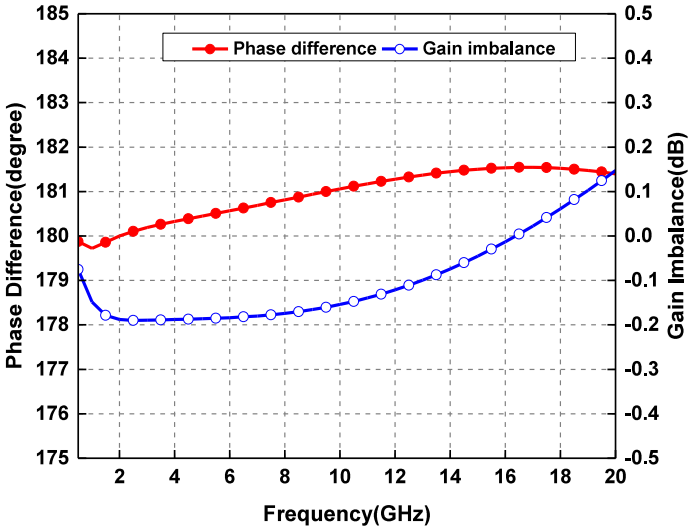


Figure 4.2. Simulated phase difference and gain imbalance of the active balun.

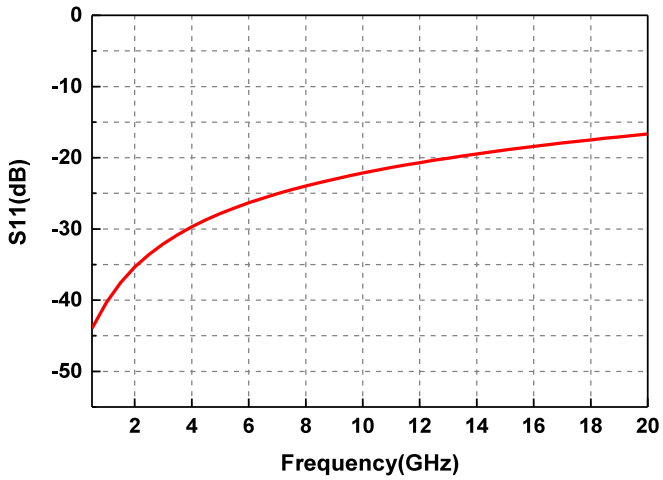


Figure 4.3. Simulated S_{11} of the active balun.

small size. In the proposed transmitter front-end, the frequency of LO2_IN is from 3.4533 to 3.8833 GHz. At such low frequency, the size of passive baluns will be very large. Moreover, passive baluns suffer from high insertion loss, thus necessitating high power level of the input signal. In CMOS implementation, the loss of a passive balun is even higher due to the low quality factor of the passive components caused by the lossy substrate. While, active baluns are superior to passive baluns in terms of size and loss. Therefore, an active balun is used in this design mainly considering small size and low loss [57]-[64], and the schematic of the active balun is shown in Figure 4.9 [63]. The

balun consists of two stage differential pairs with common source configuration. For the first stage differential pair, one input is the single ended LO input signal, and the other is AC grounded through a large bypass capacitor. In order to achieve a good input matching, a 50-Ω resistor is introduced parallel to the input port.

The simulated performance of the balun is reported in Figure 4.10 and Figure 4.11. The simulated gain imbalance is less than 0.2 dB, and the simulated phase difference is 180 ± 1.5° from 0.5 to 20 GHz, showing the balun exhibits a good differential output performance. Besides, the simulated S_{11} is below -15 dB, showing a good input matching. The phase noise of the active balun should be low enough, such that the phase noise of the input signal should not be degraded by this balun. For 11-GHz input frequency, the simulated phase noise of the balun is -134.1 dBc/Hz and -142.4 dBc/Hz at 0.1- and 1-MHz offset, respectively, indicating the balun exhibits quite low phase noise.

4.4.3 Divider design

1. Divider with 50%-duty-cycle clock

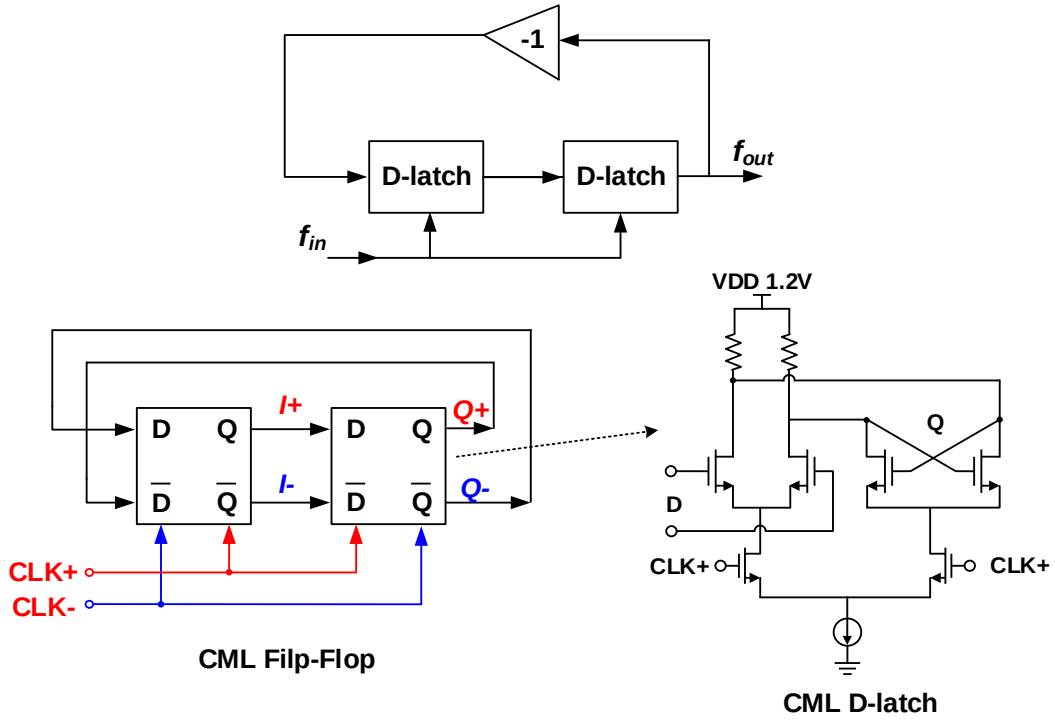


Figure 4.12. Divider-by-2 with CML flip-flop.

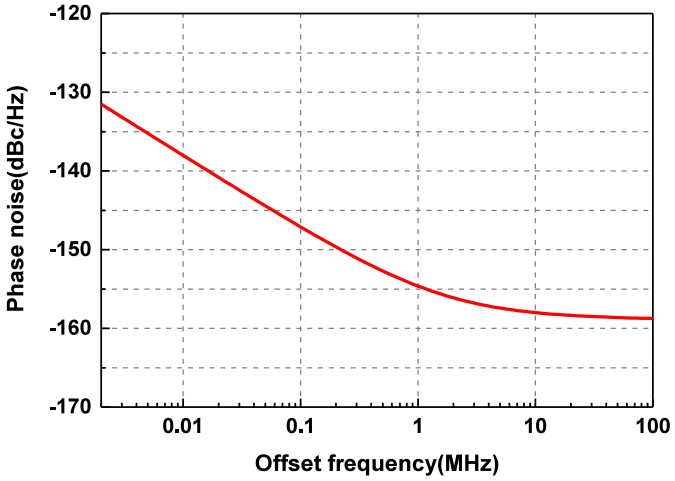


Figure 4.13. Simulated phase noise of the divider for LO1.

The divider-by-two to generate 50%-duty-cycle clock for LO1 uses current-mode logic (CML) D-latch filp-flop topology [33], [65], [66]. A simple structure of CML filp-flop divider, shown in Figure 4.12, consists of two cascaded D-latches with a negative feedback. The advantage of this type of divider is high speed since the signal only propagates through two CML gates per input cycle. In the transmitter front-end, the frequency of the input clock is as high as 11.67 GHz, which is reason why we choose CML D-latch filp-flop divider. Another advantage of CML divider is that a common-mode input voltage is accepted. Here, we have designed a divider with the operating frequency reaching 20 GHz. For 5.5-GHz output with 11-GHz input, the simulated phase noise is shown in Figure 4.13. The simulated phase noise is -147 dBc/Hz and -154.6 dBc/Hz at 0.1- and 1-MHz offset, respectively. The power consumption of the divider is 3.6 mW. Compared with other types of divider, one disadvantage of CML divider is the dissipation of static power.

2. Divider with 25%-duty-cycle clock

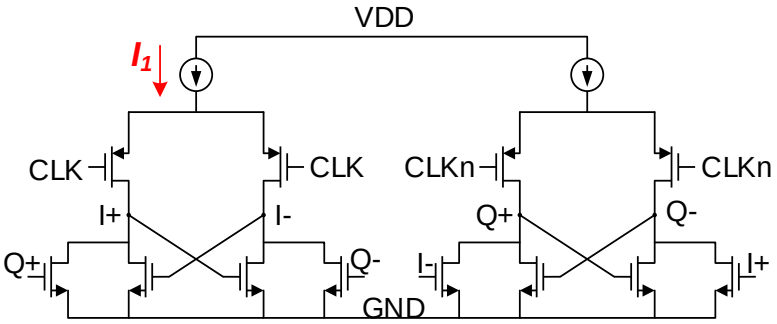


Figure 4.14. Schematic of 25%-duty-cycle divider in Razavi's paper [67].

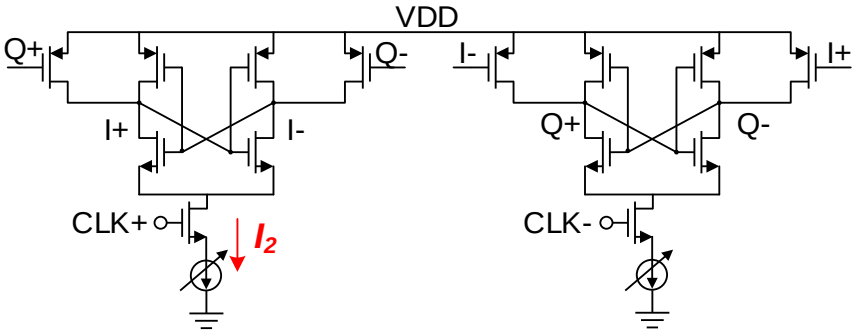


Figure 4.15. Schematic of the proposed divider.

Since the first stage of the mixer in Path2 uses a passive mixer, 25%-duty-cycle LO signal is required to feed this passive mixer. Correspondingly, a divider-by-two is required to generate 25%-duty-cycle LO signal. Razavi proposed a divider to generate 25% duty-cycle clock in [67], shown in Figure 4.14, and this divider is widely used in the transmitters with passive mixers.

In this work, we have proposed a novel divider-by-two to generate 25% duty-cycle clock, which originates from Razavi's structure in [67]. In the proposed divider, the NMOS cross-couple pair in Razavi's divider is replaced with a CMOS cross-couple pair to reduce the power consumption and improve the phase noise. In Razavi's divider, due to the ratioed low output voltage, all the transistors in the current path from VDD to ground will turn on simultaneously in a long period, which increases the power consumption, and the output waveform will flip gradually, which is harmful to the phase

noise. Thanks to the CMOS cross-couple pair in the proposed divider, all the transistors in the current path from VDD to ground will turn on simultaneously in a much shorter period. As a result, the power consumption is reduced, and the output waveform will flip quickly and sharply, thus, the phase noise is lower. The disadvantage of the proposed divider is that its maximum operation frequency is lower due to its large parasitic capacitance at output nodes, compared with Razavi's divider, but its operation frequency still can meet the requirement of this work. In order to compare the performance between the proposed divider and Razavi's divider, we have performed TRAN and PNOISE simulations for these two dividers with 4-GHz input and 2-GHz output. The simulated current waveforms of I_1 and I_2 are shown in Figure 4.16. As observed from the simulated current waveform, there is a current flow (I_1) in the half period of the clock for Razavi's divider. While, there is no current flow in the most part of a period for the proposed divider. As a result, the proposed divider reduces the power consumption. The simulated power consumptions of Razavi's structure and the proposed structure are 2.1mW and 0.38 mW, respectively. The simulated phase noises of the proposed divider and Razavi's divider are plotted in Figure 4.17, showing the phase noise of the proposed divider can be improved by around 12 dB in comparison with Razavi's divider.

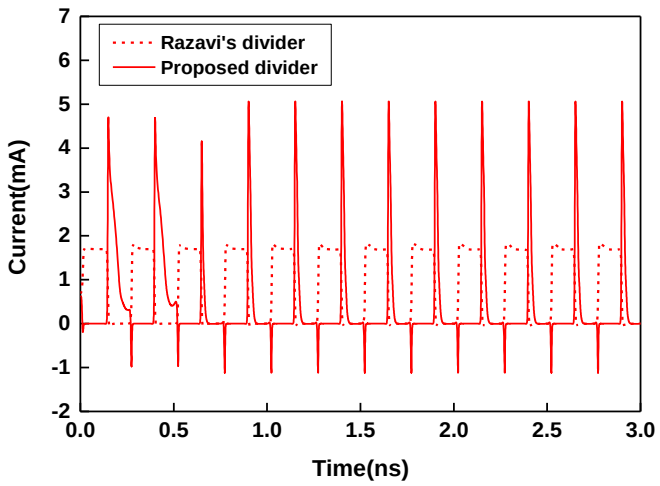


Figure 4.16. Simulated current waveforms of Razavi's divider and the proposed divider.

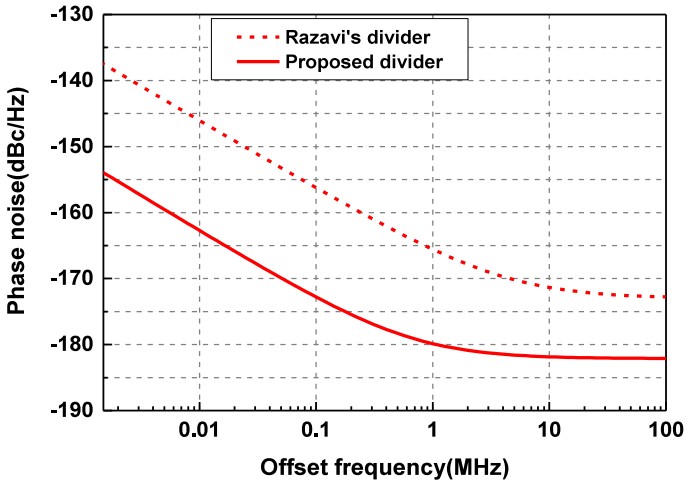


Figure 4.17. Simulated phase noises of Razavi's divider and the proposed divider.

3. Jitters of LO1, LO2A and LO2B

The LO phase noise causes a frequency spreading of the carrier frequency, thus impacting EVM. The EVM degradation is defined by [38], [39]

$$EVM_{rms} = 100\% \cdot \sqrt{2 - 2e^{-\sigma^2/2}} \tag{4.8}$$

where σ is the phase error in radians and is derived from the integrated phase noise. In practice, jitter is often used to quantify integrated LO phase noise in broadband communication systems. Since the relationship between jitter and phase error is

$$J = \frac{\sigma}{2\pi f_c} \tag{4.9}$$

EVM can be derived as

$$EVM = 100\% \cdot \sqrt{2 - 2e^{-(2\pi f_c J)^2/2}} \tag{4.10}$$

To achieve lower than 0.5% (-46 dB) EVM, the jitters are required lower than 144.7 fs at 5.5-GHz. The simulated jitters of the LO generator including the balun, divider and buffer are 18.14 fs for LO1 at 5.5 GHz, 29 fs for LO2A at 1.8333 GHz, and 19.57 fs for LO2B fs for LO2B at 3.6667 GHz, respectively. The simulated jitters for the three LO signals indicate the phase noises produced by the LO generator have a negligible impact on EVM of the transmitted signal.

4.4.4 Driver and Power Amplifier Design

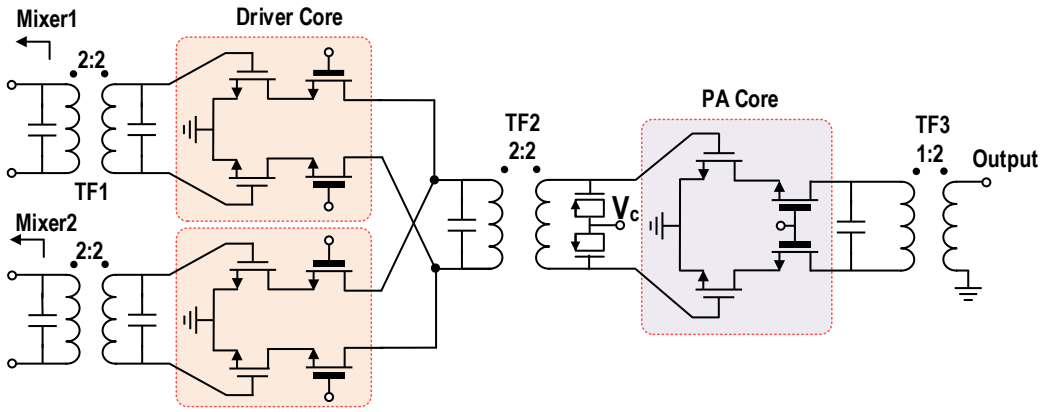


Figure 4.18. Schematic of the driver and the PA.

In the proposed transmitter front-end, the two aggregated carries are amplified by the driver and the PA, following the up-conversion mixers. The linearity of the amplification block is critical to the transmitter's performance, and the performance of EVM and ACLR will deteriorate due to the degradation of the linearity. For 5-GHz WLAN application, the wide bandwidth of 80 MHz and the 256-QAM modulation of 802.11 ac/ax signal result in a very high peak-to-average power ratio (PAPR), which can be over 10 dB. Thus, a large power back-off is required for the driver and the PA to satisfy the stringent EVM and ACLR requirements of 802.11 ac/ax. The design of the driver and the PA with high linearity is a key issue for carrier aggregation to reduce power back-off and improve power efficiency. For this reason, the linearity is given priority among some key performances in designing the amplification block. The linearity is determined by AM-AM and AM-PM distortion, and flat AM-AM and AM-PM characteristics are desired [39].

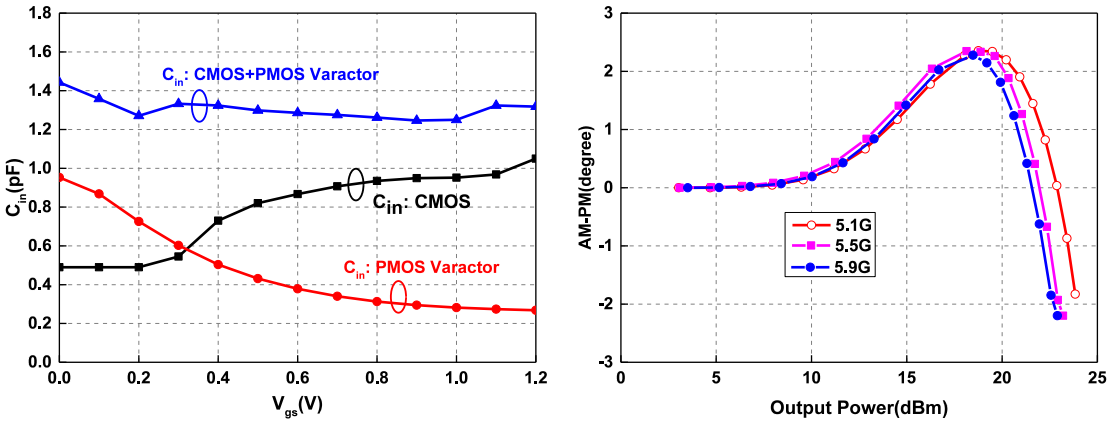
In practice, flat AM-AM performance can be achieved through optimizing bias or employing the multi-gate biasing technique. In [68]-[71], the multi-gate biasing technique is used to achieve a flat gain over a wide range of input, and thus improve the AM-AM performance. While, this technique requires three bias voltages, resulting in

high complexity. For convenience, the back-off technique is often used to improve the AM-AM performance other than the multi-gate biasing technique at the expense of power efficiency. In our design, the bias voltages are optimized to obtain the AM-AM performance as flat as possible.

In CMOS implementation, when input signal changes towards high power level, the input transistor of the PA is driven from the cutoff state to the saturation and triode regions. Consequently, the effective input capacitance of the PA changes with different power levels, leading to the AM-PM distortion, which is another major contributor to EVM degradation. Currently, the capacitance compensation technique is an effective technique for the PA to enhance the AM-PM performance. Auxiliary PMOS transistor or varactor is adapted to compensate the gate-source capacitance (C_{gs}) of NMOS transistor with different input levels [25], [72]-[74]. PMOS device has an inverse capacitance with different power levels as compared to its NMOS counterpart. As a result, when attaching a PMOS devices with an appropriate size, the total capacitance can be flattened with a little variation, reducing the AM-PM distortion. For the driver, the variation of the gate-source capacitance is not large due to its' small transistor size. Thus, the capacitance compensation technique is only adopted for the PA.

The schematic of the driver and the PA is shown in Figure 4.18. The driver and the PA both employ cascode structure, in which the thick-oxide devices are used in the common gate device to sustain gate-drain voltage stress in high output power level under a supply voltage of 2.5 V. The size of the transistors in the driver and the PA are selected mainly based on the total gain, saturated output power and efficiency. In our design, the PA is targeted to deliver an average output power of 10 dBm for VHT80, MCS9 802.11ax signal. Based on high PAPR of VHT80 MCS9 signal, which is at least 10 dB, to meet the requirement of the average output power of 10 dBm, the saturated output

power of the PA should be larger than 22 dBm. Accordingly, the transistor sizes of the common source and the common gate devices are set to 0.896 mm/40 nm and 1.536 mm/270 nm, respectively, so that the PA can deliver a maximum output power of around 24 dBm. In order to make sure the driver operates in linear state even when the following PA enters the compression region, the P_{1dB} or saturated power of the driver should have 3-5 dB margin. Based on this consideration, the transistor size of the driver's common source and common gate devices are set to 0.256 mm/40 nm and 0.512 mm/270 nm.



(a) (b)

Figure 4.19. (a) Input capacitance compensation. (b) Simulated AM-PM distortion of the PA.

As evident in [25], compared with PMOS transistor, PMOS varactor can more effectively compensate the non-linear input capacitance of input NMOS transistor by virtue of larger ratio of C_{max}/C_{min}. Therefore, PMOS varactor is utilized in the PA's input. Figure 4.19(a) depicts the variation of the input capacitance versus input voltage with and without PMOS varactor. Compared to a counterpart without capacitance compensation, the variation of the total capacitance is below ±0.08pF, improving the AM-PM performance significantly. In addition, the simulated AM-PM performance of the PA at different frequencies are plotted in Figure 4.19(b), showing the AM-PM

distortion of <±2.3° across the 5-GHz WLAN band.

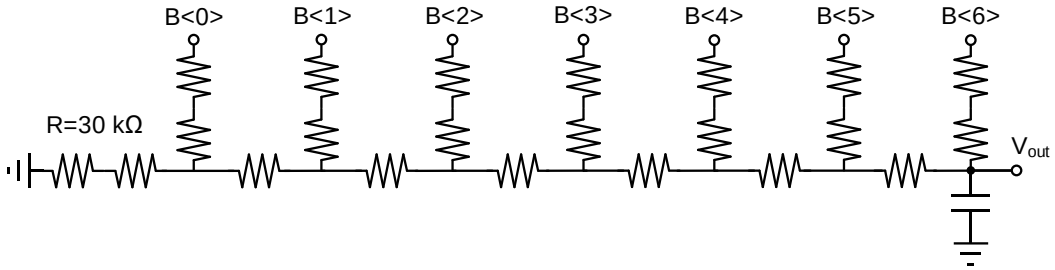
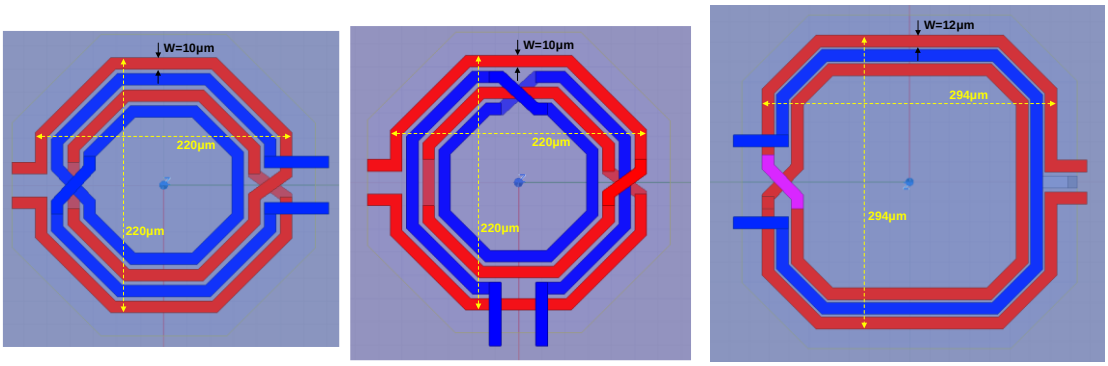


Figure 4.20. Schematic of the DACs to provide bias voltage.

The driver and the PA both operate in class-AB mode, based on the trade-off among power gain, PAE and linearity. The supply voltages are 2.5 V for both the driver and the PA. For the PA, the bias voltages are optimized to 0.5 V and 2.2 V for the common source transistor and the common gate transistor, respectively; For the driver, the bias voltages are set at 0.52 V and 2.2 V. In the design, every bias voltage is controlled by one 7-bits DAC, which employs a simple R-2R structure [75], as shown in Figure 4.20. The resolution of the DAC's output voltage is 0.094 and 0.0195 V for the gate bias for the common source devices and the common gate devices, respectively.



(a) (b) (c)

Figure 4.21. Physical structure of the transformers (a) between the mixer and the driver. (b) between the mixer and the PA. (c) output.

In order to achieve wideband performance from 5 GHz to 6 GHz, the inter-stage matching networks between the driver and the PA, and between the mixer and the driver

are designed using transformers; The output matching network is also designed using transformer. The gate bias for the common source devices and DC supply voltages for the drivers and PA are all provided through the center tap of the transformers. The transformers are designed in EM simulation software HFSS V15, and they are implemented using the top layer metal with a thickness of 3.5 μm. Figure 4.21 shows the physical structures of the transformers. Two inter-stage transformers TF1 and TF2 both have a turn ratio of 2:2, and the equivalent parameters of these two transformers are: L_p = 0.85 nH, L_s = 0.78 nH, k = 0.718, Q_p = 11.5, Q_s = 15.3 for TF1; L_p = 0.9 nH, L_s = 0.78 nH, k = 0.7, Q_p = 11.6, Q_s = 15.3 for TF2, respectively. The output transformer has a turn ratio of 1:2, and it also works as a differential-to-single-ended output balun. The equivalent parameters of the output transformer are: L_p = 0.51 nH, L_s = 1.52 nH, k = 0.71, Q_p = 12.6, Q_s = 15.5.

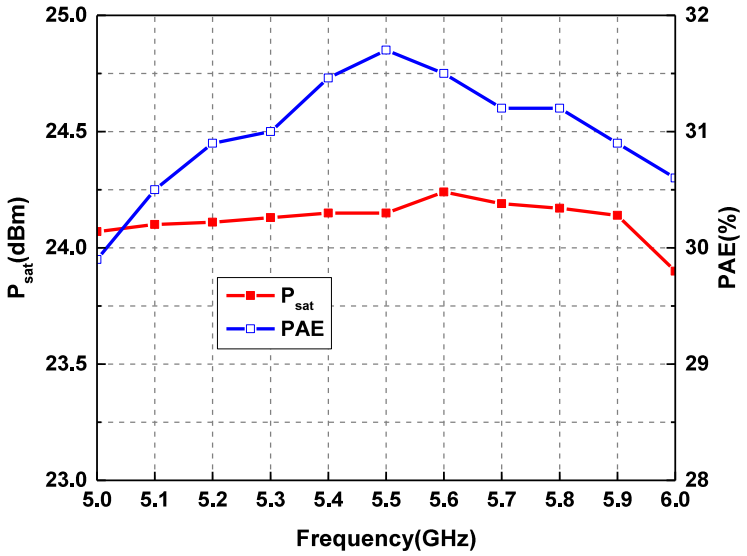


Figure 4.22. Simulated P_{sat} and PAE at different frequencies.

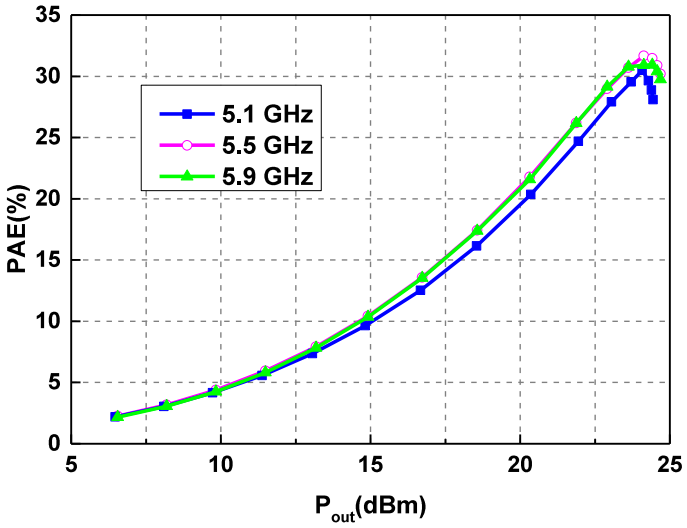


Figure 4.23 Simulated PAE versus output power at 5.1, 5.5 and 5.9 GHz.

Figure 4.22 depicts the simulation results of the PA, in terms of the P_{sat} and PAE. The PA delivers an output power of 23.6-24.3 dBm with a PAE of 29.9-31.7% from 5 to 6 GHz. In addition, the simulated PAE versus the output power at 5.15, 5.5 and 5.9 GHz are depicted in Figure 4.23.

Since the outputs of the two drivers are added through the transformer, the two outputs of the drivers are directly connected. Similarly, in [8] (from Broadcom), the two outputs from mixers are also directly connected. However, in this case, the inter-stage matching between the driver and the PA is affected. The output capacitance C_{out} of the driver is related to the output power of the driver, as shown in Figure 4.24. When the output power of the one driver changes, its output capacitance will change accordingly. Then, the inter-stage matching network between the driver and the PA will change, and the performance for the other driver will be affected. The variation of the output capacitance C_{out} depends on the transistor size. In this transmitter front-end, the transistor size of the driver is not too large, so the interference between the drivers can be accepted.

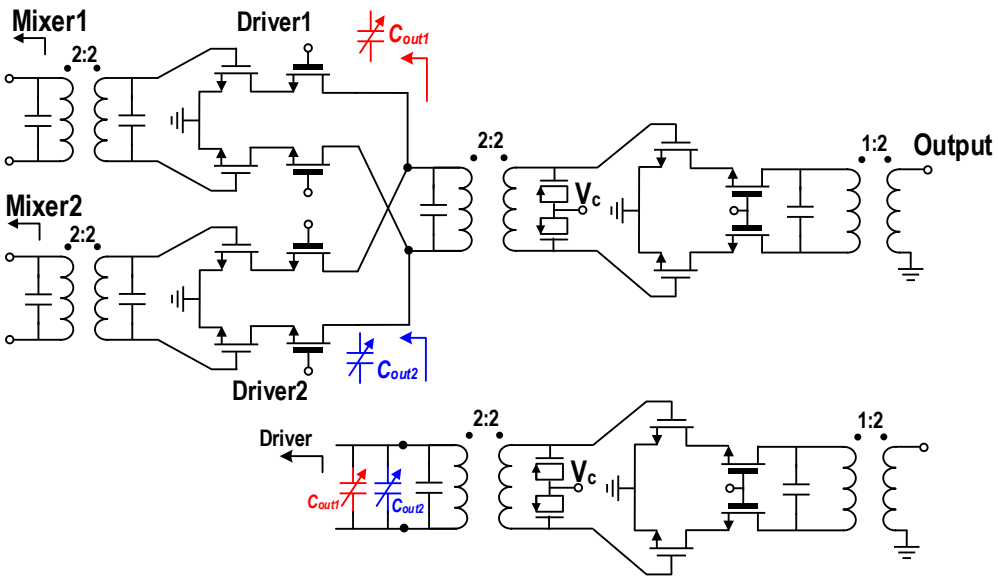


Figure 4.24. Output capacitance of the two drivers.

4.5 Transmitter measurement results

The transmitter front-end was fabricated in TSMC 40-nm CMOS technology, and bonded on the testing PCB. Figure 4.25 depicts the die microphotograph of the transmitter front-end, and the die area is 1.1×1.3 mm^2.

The measurement setup is shown in Figure 4.26. The two baseband signals are first created in Matlab, then downloaded to the arbitrary waveform generator (AWG: 81180A) and the vector signal generator (VSG: E8267D). In the measurement, the RF output signal is directly sampled by using Keysight DSOZ634A oscilloscope at a sampling rate of 160 Gsps, and then the sampled data is sent to PC via Ethernet and demodulated in

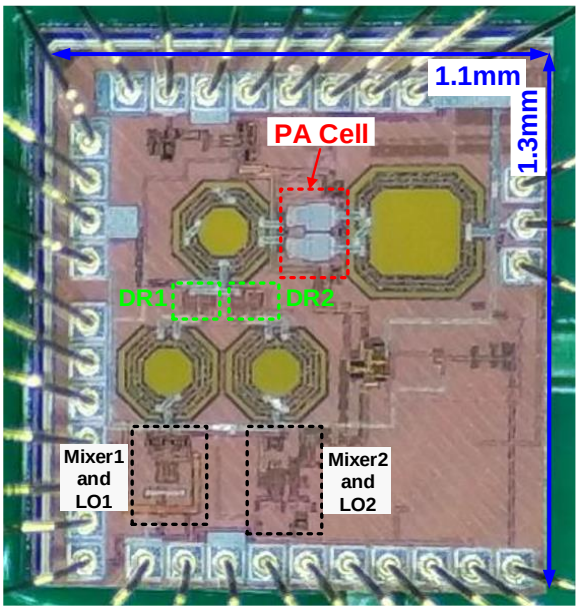


Figure 4.4. Die photograph of the proposed transmitter front-end.

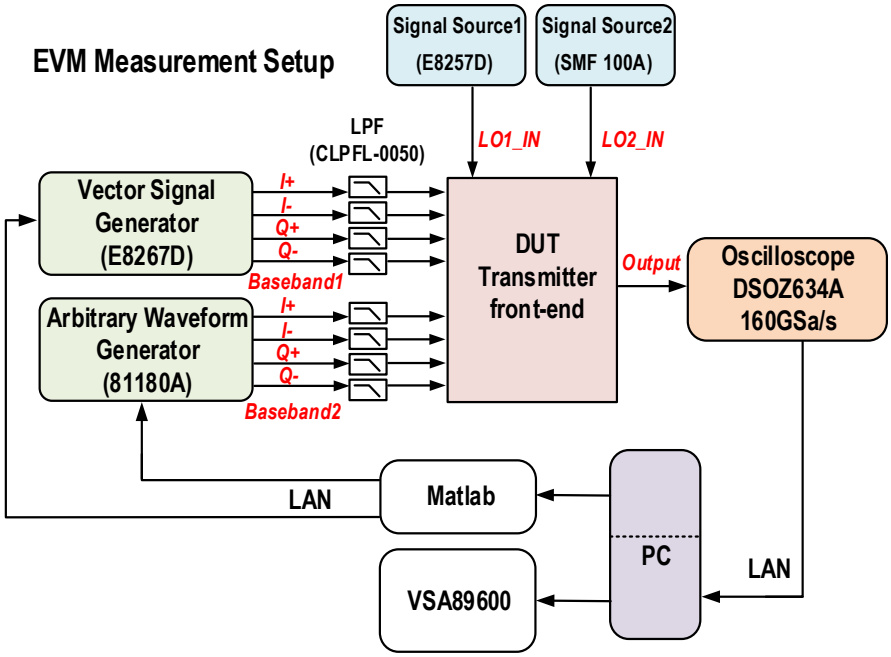


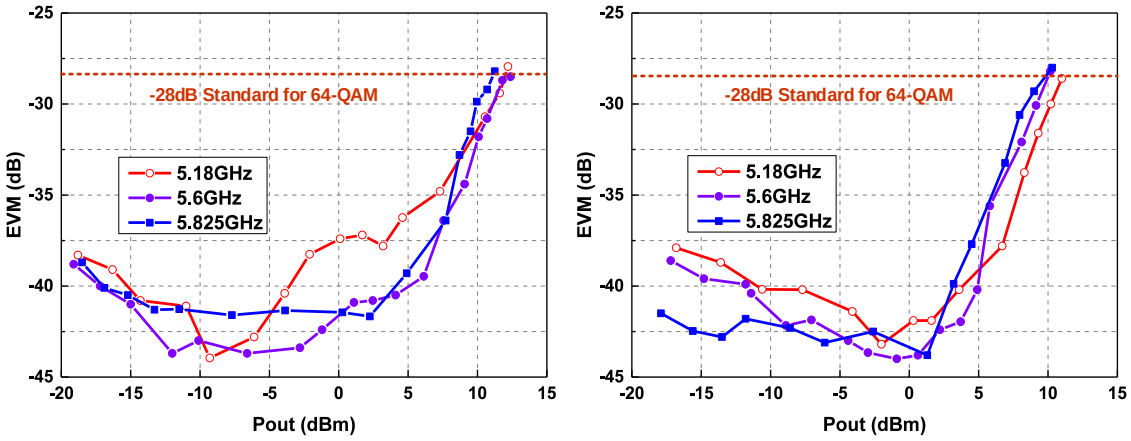
Figure 4.5. EVM measurement setup.

Keysight VSA 89600B software. In generating the analog baseband signal, the sampling rates of the DACs in both AWG and VSG are both set to 100 Msps. As a result, a series of images caused by the DACs exist at the frequencies of N×100 MHz. If these images are up-converted to RF, the corresponding interferences will fall into the 5-GHz WLAN band. In order to suppress these images, low pass filter is necessary. In the proposed

transmitter front-end, only one second-order R-C filter is used, while, it cannot provide enough suppression to filter out the images. Therefore, external low pass filters are used to suppress the images, and the used filters are CLPFL-0050 from Crystek. The filter has a seventh-order Chebyshev response with 58-MHz 3-dB bandwidth, and it can provide a suppression higher than 80 dB at the frequency above 150 MHz.

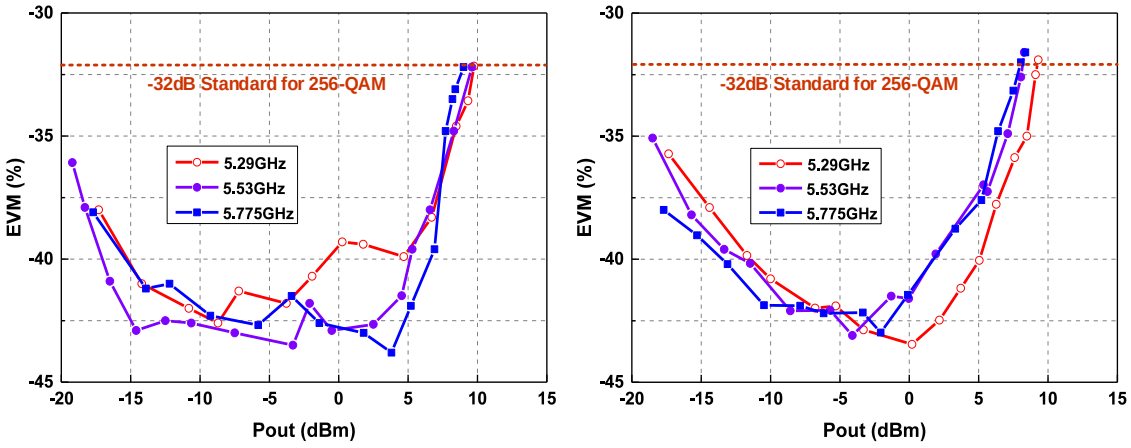
4.5.1 Single Carrier Performance

Before evaluating the transmitter front-end's practical performance for carrier aggregation, each path was tested by using a VHT20, MCS5 (20-MHz bandwidth, 64-QAM modulation, 3/4 code rate) and a VHT80, MCS9, 802.11ax signal (80-MHz bandwidth, 256-QAM modulation, 5/6 code rate) without digital pre-distortion (DPD) [76]. EVM was first measured by using the VHT20, MCS5 signal at 5.18, 5.6 and 5.825 GHz, in Channels 36, 120 and 165. The PAPR of this signal is 9.49 dB. The measured EVMs of the two paths in different average output power levels are reported in Figure 4.27. When the specification of the EVM of ≤ -28 dB is satisfied for 64-QAM modulation, Path1 delivers an average output power of 12.2, 12.4 and 11.3 dBm, and Path2 delivers an average output power of 11.2, 10.2 and 10.3 dBm, at 5.18, 5.6 and 5.825 GHz, respectively.



(a) (b)

Figure 4.27. Measured EVM with VHT20, MSC5 802.11ax signal for single carrier mode. (a) Path1. (b) Path2.



(a) (b)

Figure 4.28. Measured EVM with VHT80, MSC9 802.11ax signal for single carrier mode. (a) Path1. (b) Path2.

Then, EVM was measured by using the VHT80, MCS9 signal at 5.29, 5.53 and 5.775 GHz, in Channels 58, 106 and 155. The measured EVM with respect to the average output power level are plotted in Figure 4.28. When satisfying the specification of the EVM below -32 dB, Path1 delivers an average output power of 9.75, 9.5 and 9 dBm, and Path2 delivers an average output power of 9.1, 8.3 and 8.37 dBm, at 5.29, 5.53 and 5.775 GHz, respectively. The best EVM achieved can reach -43.3 dB and -43.64 dB for Path1 and Path2, respectively. Since the PAPR of the VHT80, MCS9 signal is as high as 11.25 dB, large back-off is required for the PA to meet the stringent EVM requirement of -32 dB for 256-QAM modulation without using DPD. In this design, we do not focus on the PA design with a large output power; thus, the average output power of this transmitter front-end for 802.11ax signal is lower than that of some other commercial transceivers with integrated PA. In addition, the measured constellation, spectrum and EVM at 5.53 GHz for Path1 are demonstrated in Figure 4.29.

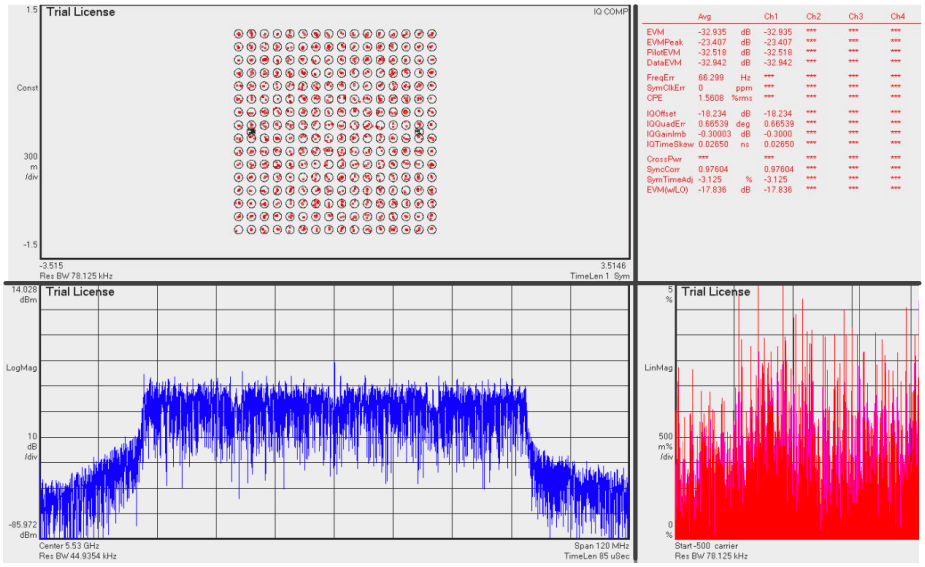
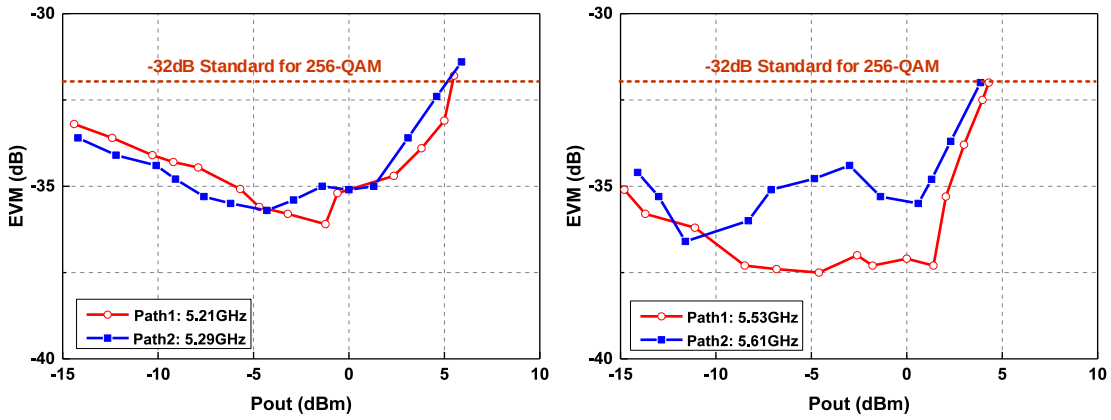


Figure 4.29. Measured constellation and EVM for Path1 at 5.53 GHz.

4.5.2 Carrier Aggregation Performance

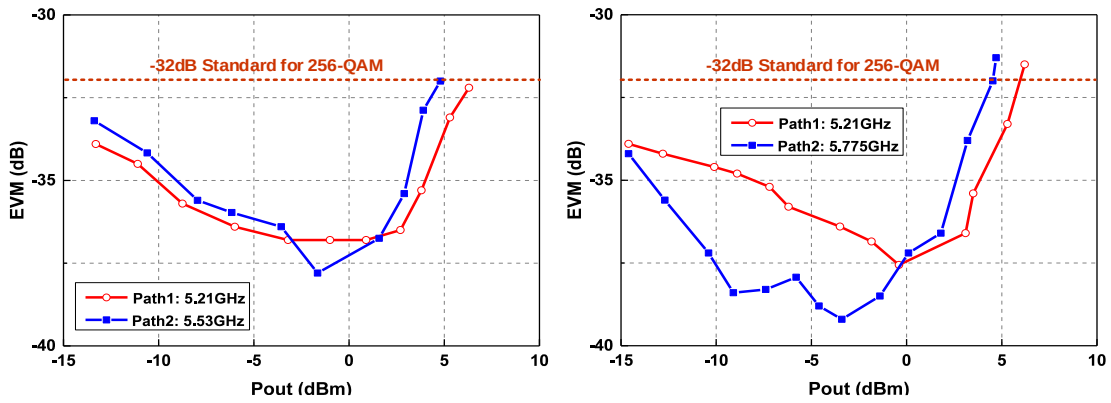
We measured EVM using two VHT80, MCS9, 802.11ax signals for intra-band and inter-band carrier aggregation modes. The measured EVM of each carrier for two contiguous intra-band carrier aggregation cases (5.21 + 5.29 GHz and 5.53 + 5.61 GHz) are plotted in Figure 4.30. For non-contiguous inter-band carrier aggregation, EVM was measured for three cases: 5.21 + 5.53 GHz, 5.61 + 5.775 GHz, and 5.21 + 5.775 GHz, and the measured results are shown in Figure 4.31. Besides, the measured constellation and EVM for contiguous carrier aggregation (5.53+5.61 GHz) are depicted in Figure 4.32. Compared with the measured results for single carrier operation, 2-3 dB more back-off is required to meet the linearity requirement in terms of the total output power of the two carriers. It is reasonable that the linearity of the PA degrades when processing two wideband signals concurrently. If DPD is employed, the average output power will be increased by a large degree, and it is beyond the scope of this thesis.



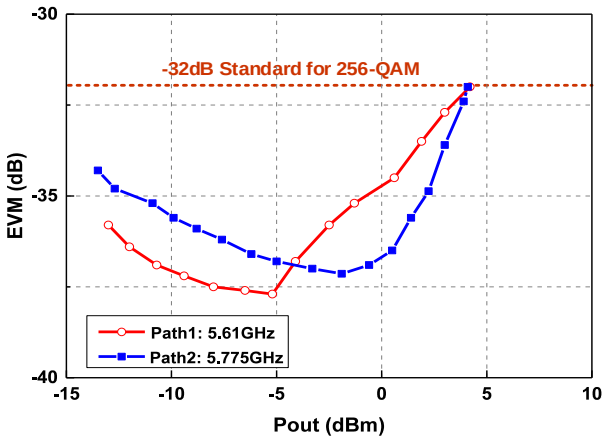
(a) (b)

Figure 4.30. Measured EVM performance for contiguous carrier aggregation mode. (a) 5.21+5.29 GHz. (b) 5.53+5.61 GHz.

Meanwhile, the measured performance is summarized and compared with other recent works listed in Table 4.1. From Table 4.1, the EVM floor achieved in this work has the same level as that in other state-of-the-art works, verifying a good EVM performance can be achieved even without high physical isolation between RF signal paths. Compared with some other works, the power consumption is high and the transmitter's power efficiency is low. One reason for the low power efficiency is that the circuit blocks are not optimal regarding the power consumption and efficiency. In addition, when the PA concurrently processes two carriers using VHT80, MCS9 802.11ax signals, large back-off results in lower efficiency of the PA and drivers.

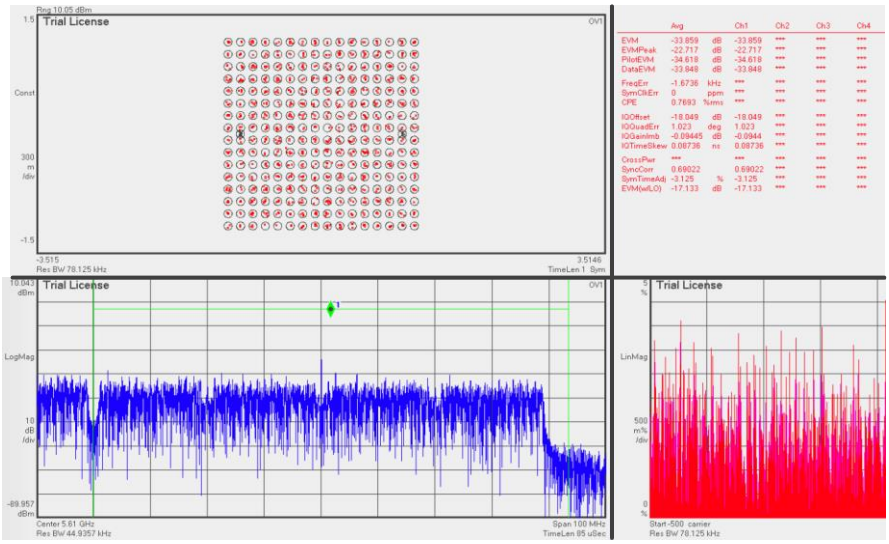


(a) (b)

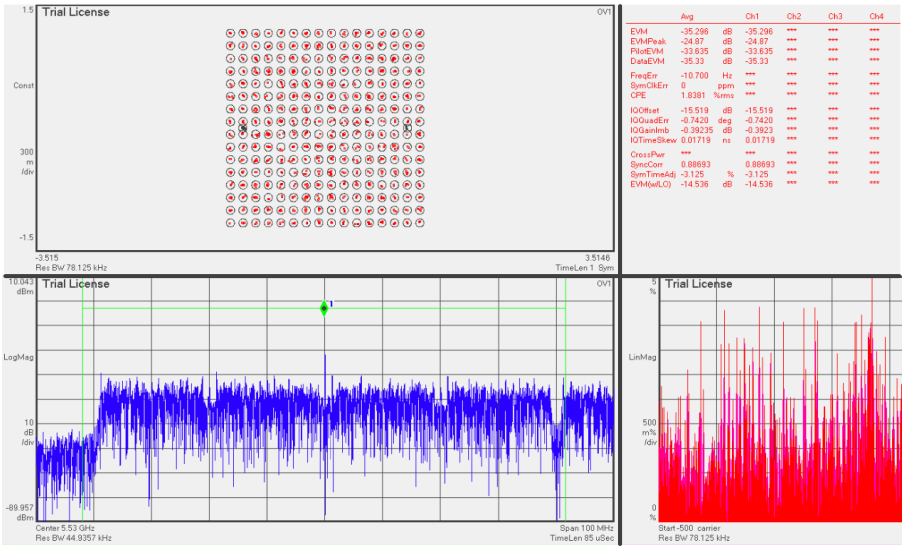


(c)

Figure 4.31. Measured EVM performance for non-contiguous carrier aggregation. (a) 5.21+5.53 GHz. (b) 5.21+5.775 GHz. (c) 5.61+5.775 GHz.



(a)



(b)

Figure 4.32. Measured constellation, EVM and spectrum for contiguous carrier aggregation. (a) 5.61 GHz. (b) 5.53 GHz.

During the measurement, the power level difference between the two carriers is kept within ± 1.5 dBm, aiming to avoid EVM degradation by the emission from the adjacent channel in the contiguous carrier aggregation mode. When the output power level has a large difference between the two carriers, the carrier having lower power will suffer from considerable adjacent channel emission from the other carrier having larger output power, thus leading to SNR deterioration and EVM degradation, as illustrated in Figure 4.33 [20]. In order to gain insight into the impact of the power level difference on EVM for the contiguous carrier aggregation mode, we measured the EVM of Path2 at 5.61 GHz with a fixed output power, while tuning the output power of Path1 at 5.53 GHz. The measured EVM versus the power level difference is reported in Figure 4.33. When the output power of Path2 is much larger than that of Path1, better EVM of Path2 is achieved and vice versa.

In addition, the measured spectrum for contiguous carrier aggregation (5.53+5.61 GHz) is depicted in Figure 4.35(a), showing that the requirement of the emission mask

is satisfied in the 5-GHz band. From the wideband spectrum shown in Figure 4.35(b), the two unwanted signals caused by the LO coupling fall into out-of-band at the frequencies of 3.66 and 7.4 GHz ($f_{LO1}\pm f_{LO2A}$), as previously predicted in Chapter 4.3. Besides, there are two more unwanted signals at 3.74 and 7.48 GHz, which are caused by the double-conversion mixer in Path2. Although the resonant tanks in the transmitter front-end can suppress the magnitude of these unwanted out-of-band signals, some signals are still quite strong and violate the emission mask. Therefore, in practical application, one external bandpass filter is required to suppress these unwanted signals.

Table 4-1 Measured performance summary and compassion with state-of-the-art 802.11ac/ax transmitters.

		This work		ISSCC2018 [15]	ISSCC2017 [20]	JSSC2017 [14]
WLAN standards		11a/ac/ax		11abgn/ac/ax	11abgn/ac	11abgn/ac
Process (nm)		40		28	40	40
Integrated PA		Yes		No	Yes	Yes
Non-contiguous CA		Yes		Yes	Yes	No
Contiguous CA		Yes		No	Yes	No
Measured Signal		VHT80, MCS9, 11ax		VHT80, MCS10, 11ax	VHT80, MCS9, 11ac	VHT80, MCS9, 11ac
EVM Floor (dB)	Single Carrier	**-42.5**		-38.1	-36.5	-38
	CA	**-37.6** non-contiguous	**-36.1** contiguous	-36.5	-36.8 non-contiguous	N.A
P_{sat}(dBm)		21.9		N.A	27	29
Power Consumption (mW)		428@(5.3+4.8 dBm) (2 Streams without PLL)		832@(-5 dBm) (4 Streams +2 PLLs)	4164@(19+19 dBm) (2 Streams +2 PLLs)	1750@(17 dBm) (2 Streams +1 PLL)
Transmitter efficiency (%)		1.5		0.156	3.81	5.73

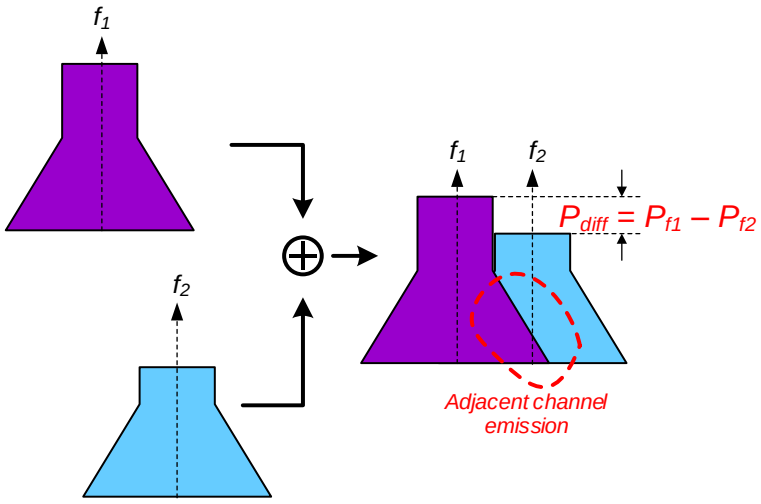


Figure 4.33. Spectrum for contiguous carrier aggregation with power difference between two carriers.

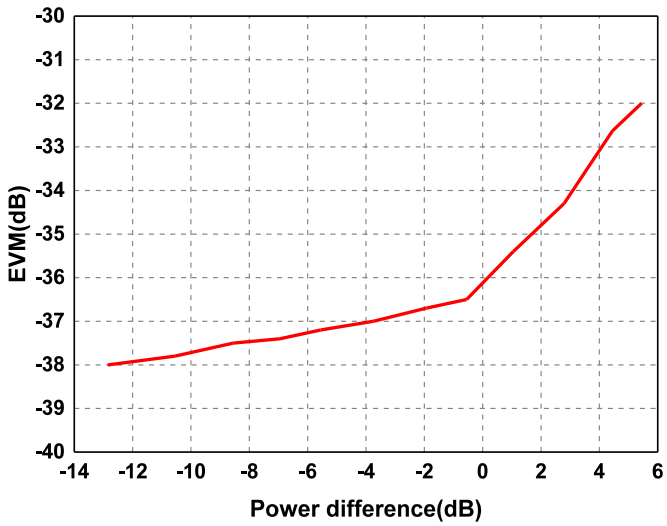
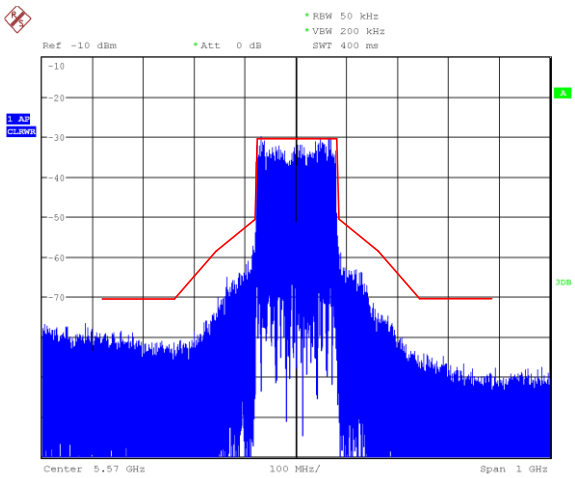
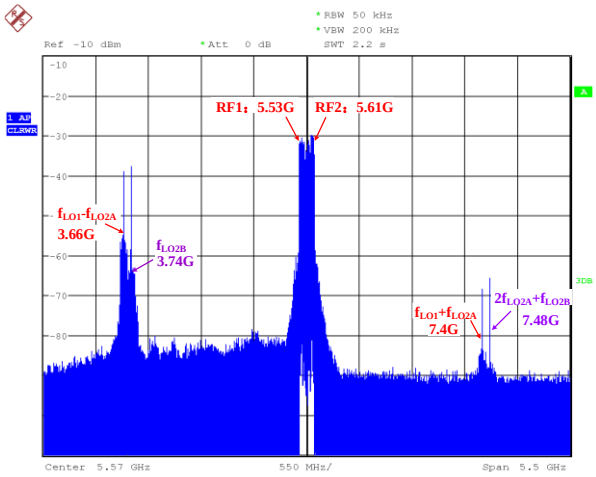


Figure 4.34. Measured EVM versus power difference.



(a)



(b)

Figure 4.35. Measured spectrum for contiguous carrier aggregation. (a) 1-GHz span. (b) 5-GHz span.

4.6 Summary

In this chapter, we propose a new transmitter architecture to address the problems of crosstalk and VCO pulling simultaneously without large physical isolation required on-chip. Based on the proposed architecture, a transmitter front-end is designed and implemented in TSMC 40-nm CMOS technology, and the circuit design of the main blocks in the transmitter front-end is presented in detail. For 80+80 MHz contiguous carrier aggregation using 802.11ax signals with 256-QAM modulation, the measured EVM reaches -36.1 dB, validating the proposed architecture can effectively address the problem of crosstalk without large physical isolation on-chip. Although, two LO inputs signals are provided from the external signal sources, not from the internal PLLs, it is still convinced that the proposed architecture can address the problem of VCO pulling if using internal PLLs due to large frequency spacing between two VCOs.

Chapter 5

Reconfigurable 2.4/5-GHz Dual-band Transmitter Front-End

802.11ax's devices are designed to operate in the existing 2.4- and 5-GHz (4.9-5.9 GHz) spectrums, requiring a dual-band transmitter or a broadband transmitter covering both the 2.4- and 5-GHz bands. As previously mentioned in Chapter 2, a single transmitter supporting reconfigurable 2.4/5-GHz dual-band operation is superior to the dual-band architecture using two transmitters channels in terms of lower cost. Currently, no reconfigurable dual-band transmitter using only one transmitting channel is available in academia and industry. Therefore, the effort of this chapter is to design such a reconfigurable 2.4/5-GHz dual-band transmitter front-end for 802.11ax application. As a core block in a transmitter, the power amplifier should operate in dual-band or in a broadband to cover both the 2.4- and 5-GHz bands. In this chapter, firstly, we review the dual-band and broadband PAs in the literature, and find low efficiency caused by the output matching network is a main drawback both for the published dual-band and broadband PAs. Then, a new design methodology of the reconfigurable output matching network is proposed to extract high passive efficiency, and the synthesis procedure is described in detail. Since the on-resistance of switches significantly impact the passive efficiency of the output matching network, how the on-resistance affects the efficiency has been investigated theoretically, providing a foundation to pursue high efficiency in designing reconfigurable dual-band output matching network. Based on the proposed design methodology of high efficiency dual-band matching, a 2.4/5-GHz dual-band PA and transmitter front-end are designed and implemented in TSMC 40-nm CMOS technology.

5.1 Background of dual-band or broadband PAs

In the literature, there are two general approaches to implement dual-band or multi-band and broadband PAs. The first approach is based on using reconfigurable components in the matching networks, such as switches [29]-[31], varactors [77], and p-i-n diode [78]. The operating frequencies of the PAs are changed or tuned through changing the values of the reconfigurable components in the matching networks by the use of the reconfigurable components. The other approach is based on using distributed configurations [21]-[23] and various broadband matching techniques such as reactive filter synthesis and real frequency techniques [24]-[28].

In [29], the operating frequency of the PA can be tuned at 2.4/3/3.5 GHz through changing the status of the two switches in the output matching network, but the achieved maximum drain efficiency is below 16.5%. In [30] and [31], two S/X band PAs using the same switchable transformer are presented, and the efficiency of the PAs in X band is only 12.5% due to the large resistance of the switch in series with the transformer. In these proposed PAs, the switches are all realized using CMOS transistor, and the on-resistances of the switches may not be very small. While, in [29]-[31], the on-resistances of the switches are not taken into consideration in the design procedure, thus, the passive efficiencies of the output matching networks are significantly impacted by the switches.

[77] proposes a multi-band multi-mode power amplifier with the efficiency of 30-55% using off-chip high quality varactors. However, these high-quality varactors are realized in silicon-on-glass technology, resulting in high cost in practical applications. If realized in CMOS technology, the quality factor of varactors will drop rapidly, leading to a significant decrease of efficiency of PA. Besides, the ratio of C_{max}/C_{min} of varactor limits the achievable frequency tuning range. In [78], a multi-band PA is proposed using p-i-n diodes to control the inductor value. Although p-i-n diode has a lower on-resistance, it is

unavailable in CMOS technology.

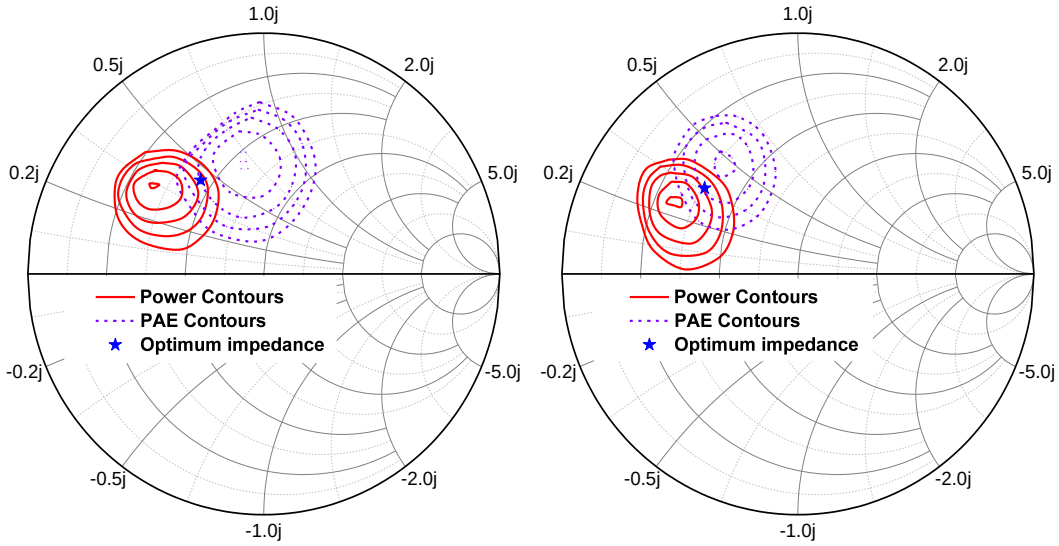
Compared with the PAs using reconfigurable components, the distributed PAs have a distinct advantage in the performance of return loss and wideband. However, they inherently suffer from low power efficiency and large size, making them unsuitable for low cost application. [24] and [25] present the broadband PAs using the third-order bandpass matching networks. Although the PAs using filter-based matching network have better efficiency in comparison with the distributed PAs, the power efficiency is still limited by the large loss of the complex high order output matching network, and the size of the output matching network is also quite large due to the inductors used. Thus, with the main considerations of high efficiency and low cost, the current broadband PAs no matter using distributed configurations or using filter-based broadband matching networks are not suitable for the transmitter designed to cover both 2.4- and 5-GHz WLAN bands.

5.2 2.4/5-GHz Dual-band PA

5.2.1 Optimum Load Impedance Analysis

CMOS PAs often use a pseudo-differential pair, cascode devices to provide a high output power [14], [27]. Thick-oxide devices are used in the common gate device to sustain gate-drain voltage stress in a high output power level. In this design, the cascode structure with thick-oxide common gate devices is employed. Considering the 10-dB PAPR of VHT80, MCS10 802.11ax signal (80-MHz bandwidth, 1024-QAM and 3/4 coding rate), the saturated output power of PA should be larger than 22 dBm in order to deliver an average output power of 10 dBm. Given a 23-dBm saturated output power for the design target, accounting for the estimated loss of output matching network of around 1.5 dB, the PA core should deliver a 24.5-dBm saturated output power. Here, we have

performed load-pull simulations in Keysight Advanced Design System (ADS) at 2.4 and 5.5 GHz to optimize the transistor sizes of the PA core. The transistor sizes are set at 0.896 mm/40 nm for the common source devices, and 1.536 mm/270 nm for the common gate devices, respectively. With these transistor sizes, the PA core can achieve the highest efficiency when delivering a 24.5-dBm output power under 2.5-V DC supply.



(a) (b)

Figure 5.1. Load-pull simulation results. (a) 2.4 GHz. (b) 5.5 GHz

For the differential cascode devices, the optimum load impedance is given by a load resistance in parallel with an equivalent negative output capacitance [24], as

$$Z_{opt} = R_{opt} \| \left(\frac{-1}{j\omega C_{out}} \right). \tag{5.1}$$

In practice, the optimum load impedance is normally determined through load-pull simulation. The simulated power contours and PAE contours for the fundamental at 2.4 and 5.5 GHz are demonstrated in Figure 5.1. For practical PA design, PAE and output power are two critical performances that should be considered concurrently. In general, rather than to only pursue maximum PAE or maximum output power, a trade-off between output power and PAE is normally made. In view of this point, the optimum load

impedances are determined as 22.1+j22 Ω and 17.3+j17.8 Ω at 2.4 and 5.5 GHz, respectively, as marked in Figure 5.1. The corresponding R_{opt} and C_{out} are 44 Ω and 1.5 pF at 2.4 GHz, and are 35.6 Ω and 0.82 pF at 5.5 GHz, repectively.

5.2.2 Dual-band Output Matching Network Design

The basic prototype of the reconfigurable dual-band output matching network using switchable capacitors is shown in Figure 5.2. In this matching network, the transformer is fixed, while the values of two capacitor C_1 and C_2 are tunable or switchable to adjust the load impedance seen into the matching network to target at the optimum impedances in the two bands of interest. In order to facilitate analysis and design, the equivalent circuit of the output matching network is utilized [79], as shown in Figure 5.3.

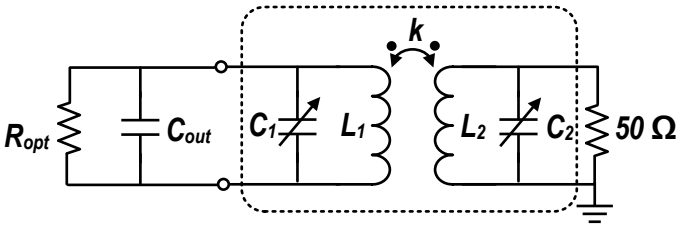


Figure 5.2. Prototype of the reconfigurable dual-band output matching network.

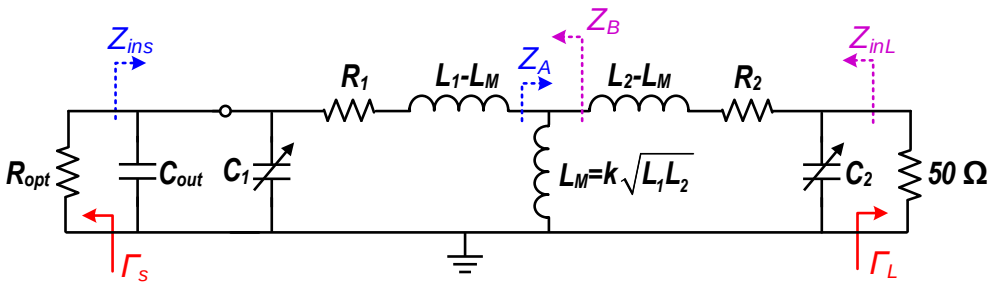


Figure 5.3. Equivalent circuit of the dual-band output matching network.

For ideal matching network, the target of matching is equivalent to achieving reflection coefficients $\Gamma_s = 0$ and $\Gamma_L = 0$ simultaneously. In practice, the ideal matching network is unachievable. Hence, we set $|\Gamma_s| \leq$ -20 dB and $|\Gamma_L| \leq$ -15 dB as the target for the output matching network to be designed in this work. $|\Gamma_s|$ and $|\Gamma_L|$ can be derived as

$$\Gamma_s = 20\log\left|\frac{R_{opt} - Z_{ins}}{R_{opt} + Z_{ins}}\right| \tag{5.2}$$

$$\Gamma_s = 20\log\left|\frac{50 - Z_{inL}}{50 + Z_{inL}}\right|, \tag{5.3}$$

where

$$Z_{ins} = \frac{Z_A + R_1 + j\omega(L_1 - L_M)}{1 + j\omega(Z_A + R_1 + j\omega(L_1 - L_M)) \cdot (C_1 + C_{out})} \tag{5.4}$$

$$Z_{inL} = \frac{Z_B + R_2 + j\omega(L_2 - L_M)}{1 + j\omega C_2(Z_B + R_2 + j\omega(L_2 - L_M))} \tag{5.5}$$

and

$$Z_A = \frac{j\omega L_M(-\omega(L_2 - L_M + 50R_2C_2) + 50(1 - (L_2 - L_M)C_2))}{50(1 - (L_2 - L_M)C_2) + j\omega(L_2 + 50R_2C_2)} \tag{5.6}$$

$$Z_B = \frac{-\omega^2 L_M(L_1 - L_M + R_{opt}C_1' + j\omega L_M R_{opt}(1 - (L_1 - L_M)C_1'))}{R_{opt}(1 - (L_1 - L_M)C_1') + j\omega(L_1 + R_{opt}C_1')} \tag{5.7}$$

$$C_1' = C_1 + C_{out} \tag{5.8}$$

$$R_1 = \frac{\omega L_1}{Q_1}, R_2 = \frac{\omega L_2}{Q_2}. \tag{5.9}$$

Now, in the equivalent circuit shown in Figure 5.3, there are four main parameters (L_1, L_2, C_1, and C_2) to be determined. Given the matching target at 2.4 and 5.5 GHz, first, we sweep the value of L_1 and L_2, and explore the range of L_1 and L_2, where C_1 and C_2 have the solutions. In this procedure, the quality factor of the primary and secondary windings of the transformer are both assumed to be 15, which is a normal value for practical transformers. Besides, the solutions of C_1 and C_2 are constraint in the range of 0-6 pF, and the solutions of C_1 and C_2 above 6 pF are regarded as unreasonable and are abandoned. Here, we investigate the range of L_1 and L_2, assuming the coupling factor of 0.67, which is a reasonable value when the primary and secondary windings are

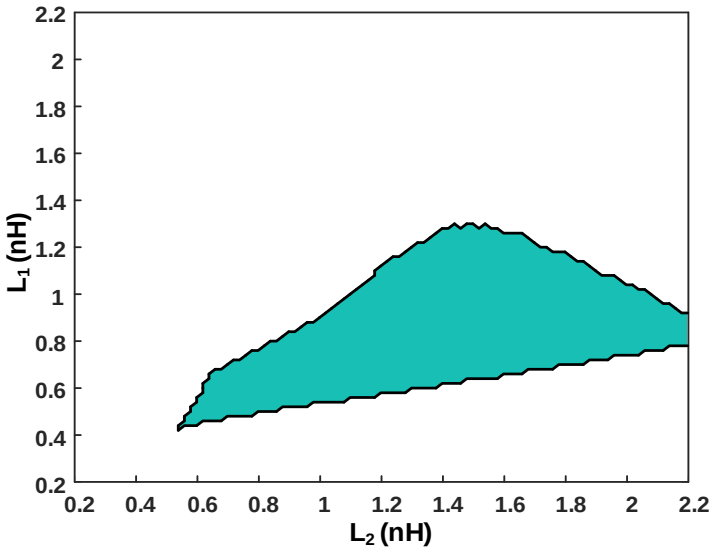


Figure 5.1. Range of L_1 and L_2 where optimum impedances can be achieved at 2.4 and 5.5 GHz.

implemented in the same top metal layer.

The calculated range is plotted in the region in Figure 5.4. This range of L_1 and L_2 can guarantee that C_1 and C_2 have the solutions such that the matching targeted ($|\Gamma_s| \leq$ -20 dB and $|\Gamma_L| \leq$ -15 dB) are achieved at the two specific frequencies. To extract the optimum value of L_1 and L_2 regarding efficiency, it is desirable to investigate the efficiency of the transformer in the achieved range of L_1 and L_2. Assuming that the quality factors of the capacitors are high enough, the efficiency η can be expressed as [80]

$$\eta = \frac{R_L' \omega^2 L_M^2}{R_1\left[\left(R_2 + R_L'\right)^2 + \omega^2\left(L_2 - \frac{50^2 C_2}{1+(50\omega C_2)^2}\right)\right] + \omega^2 L_M^2\left(R_2 + R_L'\right)} \tag{5.10}$$

where

$$R_L' = \frac{50}{1+\left(50\omega C_2\right)^2}. \tag{5.11}$$

The calculated efficiency η from (5.10) in the achieved range of L_1 and L_2 at 2.4 GHz and 5.5 GHz is illustrated in Figure 5.5. Obviously, the selection of L_1 and L_2 has a

significant impact on the transformer's efficiency. Figure 5.5 can provide a rough guidance on the selection of L_1 and L_2 to maximize the transformer's efficiency.

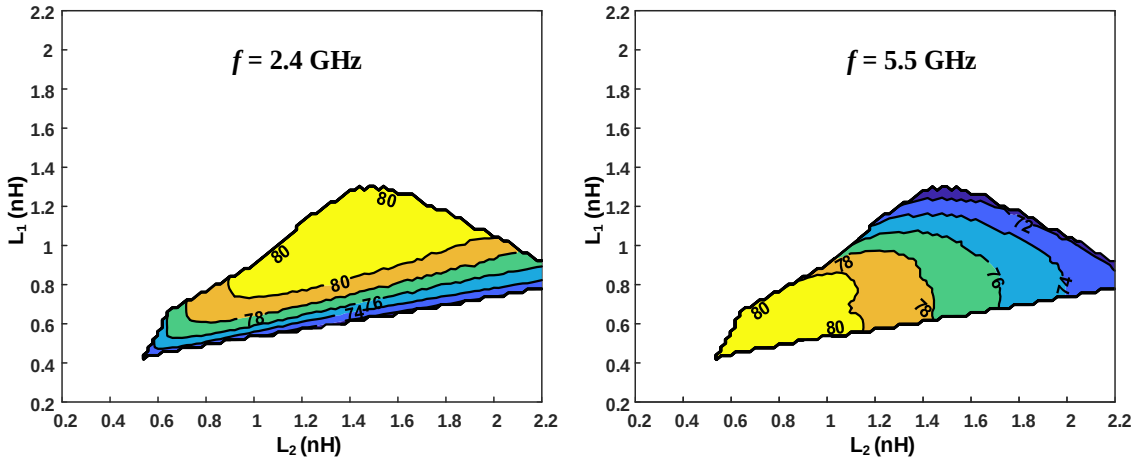


Figure 5.5 Efficiency contours of output matching network in achieved range, and unit in contours is %.

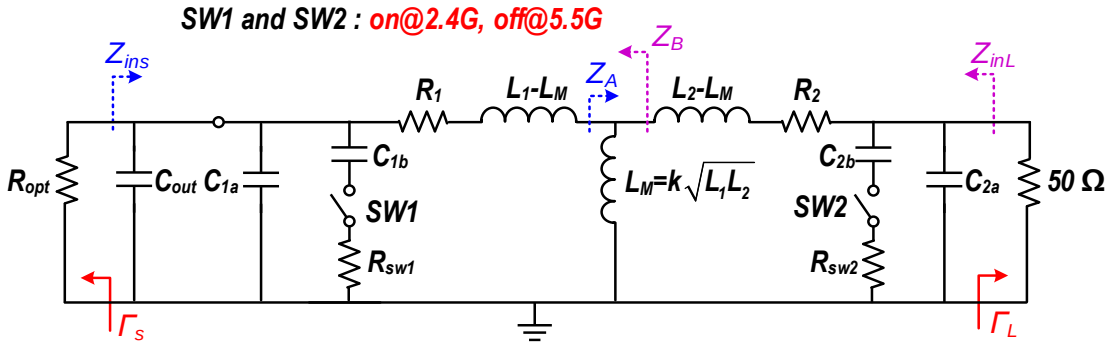


Figure 5.6. Equivalent practical circuit of dual-band output matching network.

While, in practical circuits, the values of C_1 and C_2 are switched by turning the switches on and off, as shown in Figure 5.6. When the switches are turned on to increase the value of C_1 and C_2 at 2.4 GHz, the on-resistances of the switches will decrease the quality factors of C_1 and C_2 and reduce the efficiency of the output matching network. Consequently, to determine the optimum value of L_1 and L_2, it is indispensable to take the on-resistance of the switches into account in estimating the efficiency of the output matching network at 2.4 GHz. The details on the calculation of the efficiency η' with the consideration of the on-resistance of the switches is presented as follows.

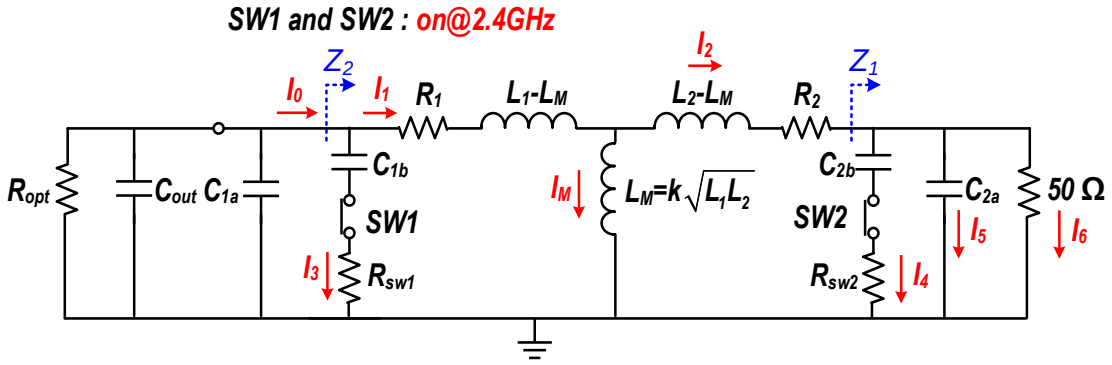


Figure 5.7. Model used to calculate efficiency of output matching network.

The output matching network's efficiency η' is defined as the ratio of the power P_{load} dissipated in the output termination load (50 Ω) and the total power P_{total} dissipated in all the resistors (R_1, R_2, R_{SW1} and R_{SW2}) and the output termination load [80], given by

$$\eta' = \frac{P_{load}}{P_{total}} = \frac{|I_6|^2 \cdot 50}{|I_1|^2 R_1 + |I_2|^2 R_2 + |I_3|^2 R_{SW1} + |I_4|^2 R_{SW2} + |I_6|^2 \cdot 50}. \tag{5.12}$$

To facilitate the calculation of the efficiency η', two impedances Z_1 and Z_2 seen from different planes are employed, as shown in Figure 5.7, which can be derived as follows:

$$Z_1 = \frac{1 + j\omega R_{SW2} C_{2b}}{\left(\frac{1}{50} - \omega^2 R_{SW2} C_{2a} C_{2b}\right) + j\omega\left(\left(C_{2a} + C_{2b}\right) + \frac{R_{SW2} C_{2b}}{50}\right)} \tag{5.13}$$

$$Z_2 = \frac{j\omega L_M \left(Z_1 + j\omega\left(L_2 - L_M\right) + R_2\right)}{Z_1 + j\omega\left(L_2 - L_M\right) + R_2 + j\omega L_M} + j\omega\left(L_1 - L_M\right) + R_1. \tag{5.14}$$

Based on Kirchhoff equations, the relationship between the currents I_1, I_3, I_4, I_6 and the current I_2 can be written as

$$I_1 = I_2 \frac{j\omega L_2 + R_2 + Z_1}{j\omega L_M} \tag{5.15}$$

$$I_3 = I_2 \frac{Z_2 C_{1b}\left(j\omega L_2 + R_2 + Z_1\right)}{\left(1 + jQ_{1b}\right) L_M} \tag{5.16}$$

$$I_3 = I_2 \frac{Z_2 C_{1b}\left(j\omega L_2 + R_2 + Z_1\right)}{\left(1+ jQ_{1b}\right) L_M} \tag{5.17}$$

$$I_4 = I_2 \frac{jQ_{2bL}}{\left(1+\frac{jQ_{2bL}}{1+jQ_{2b}} + jQ_{2aL}\right)\left(1+ jQ_{2b}\right)} \tag{5.18}$$

where

$$Q_{1b} = \omega C_{1b} R_{SW1} \tag{5.19}$$

$$Q_{2aL} = \omega C_{2a} \cdot 50 \tag{5.20}$$

$$Q_{2b} = \omega C_{2b} R_{SW2} \tag{5.21}$$

$$Q_{2b\mathrm{L}} = \omega C_{2b} \cdot 50\,. \tag{5.22}$$

Substituting (5.15) to (5.18) into (5.12), the efficiency η' can be obtained as

$$\eta' = \frac{\dfrac{50}{\left|1+\frac{jQ_{2bL}}{1+jQ_{2b}} + jQ_{2aL}\right|^2}}{\dfrac{\left|j\omega L_2 + R_2 + Z_1\right|^2 \cdot R_1}{\omega^2 L_M^2} + R_2 + \left|\dfrac{Z_2 C_{1b}\left(j\omega L_2 + R_2 + Z_1\right)}{\left(1+ jQ_{1b}\right) L_M}\right|^2 R_{SW1} + \dfrac{Q^2{}_{2bL} \cdot R_{SW2}}{\left|1+\frac{jQ_{2bL}}{1+jQ_{2b}} + jQ_{2aL}\right|^2 \left|1+ jQ_{2b}\right|^2} + \dfrac{50}{\left|1+\frac{jQ_{2bL}}{1+jQ_{2b}} + jQ_{2aL}\right|^2}} \tag{5.23}$$

The on-resistance of the switches R_{SW1} and R_{SW2} depends on the transistor size of the switches, which will be discussed in the next section. Here, the on-resistance R_{SW1} and R_{SW2} are both set at 1.5 Ω, which is a reasonable value for a practical switch transistor. Given the value of R_{SW1} and R_{SW2}, the calculated efficiency contours from (5.23) at 2.4 GHz in the determined range of L_1 and L_2 are plotted in Figure 5.8 (a). Considering the efficiency both at 2.4 GHz and 5.5 GHz, the optimum selection of L_1 and L_2 is marked in Figure 5.8. From Figure 5.8, the optimum values of L_1 and L_2 are 1 nH and 1.38 nH, respectively, and the calculated efficiencies are both above 76% at 2.4 and 5.5 GHz. Accordingly, the solutions of C_1 and C_2 are 1.6 pF and 2.08 pF at 2.4 GHz, and 0 pF and 0.62 pF at 5.5 GHz, respectively. Then, the achieved $|\Gamma_s|$ and $|\Gamma_L|$ are both below -20 dB

at 2.4 GHz and 5.5 GHz.

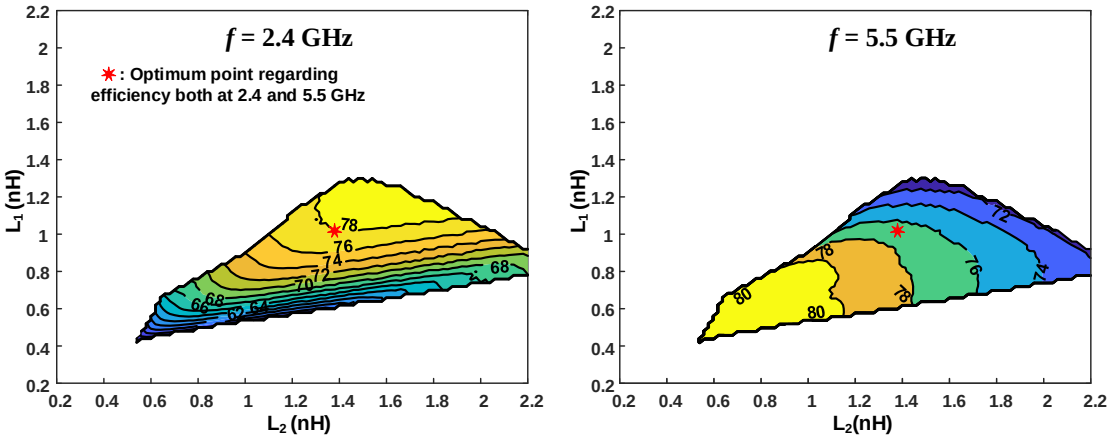


Figure 5.8. Efficiency contours of output matching network with considering on-resistance of switches, and unit in contours is %.

5.2.3 Implementation of output matching network

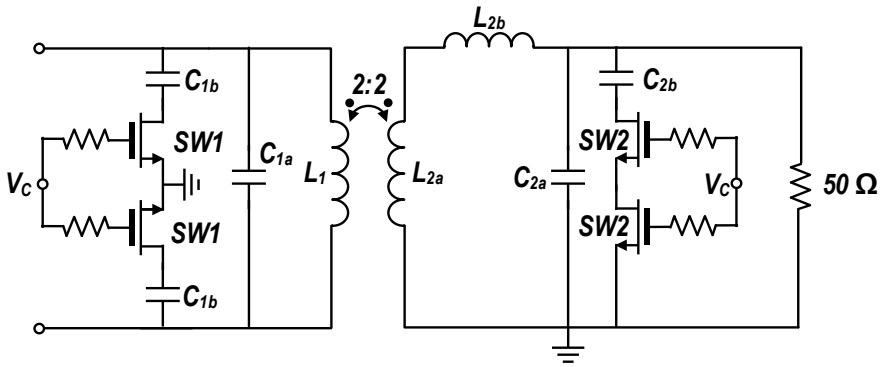


Figure 5.9. Implemented the dual-band output matching network.

We have so far determined the optimum values of the components in the reconfigurable dual-band matching network; now, we step to implement the matching network with these values. The detailed schematic of the matching network is presented in Figure 5.9. In practical implementation, L_1 of 1nH and L_2 of 1.38 nH cannot be realized by a transformer with a coupling factor of around 0.67. To solve this problem, a series connection of a transformer with the winding ratio of 2:2 and an inductor with the inductance of around 0.35 nH are utilized to form a new equivalent transformer with the desired value of L_1, L_2 and k [81]. For the transformer in series with the inductor, the

inductance L_1 and L_{2b} are both around 1 nH, the quality factors Q_1 and Q_{L2b} are 14.7-18.2 and 13-16, and the coupling factor k' between the two windings is 0.74-0.78 from 2.4 to 6 GHz, respectively. The equivalent parameters L_2, k, and Q_2 of the new equivalent transformer are given by [81]

$$L_2 = L_{2a} + L_{2b} \tag{5.24}$$

$$Q_2 = \frac{\omega L_2}{\frac{\omega L_{2a}}{Q_{2a}} + \frac{\omega L_{2b}}{Q_{2b}}} \tag{5.25}$$

$$k = \frac{k'\sqrt{L_1 L_{2a}}}{\sqrt{L_1 + L_2}}. \tag{5.26}$$

Consequently, the parameters of the new transformer are: L_1 = 0.978 nH, L_2 = 1.375 nH, k = 0.656, Q_1 = 14.74, Q_2 = 12.07 at 2.4 GHz; L_1 = 1.035 nH, L_2 = 1.42 nH, k = 0.69, Q_1 = 18.1, Q_2 = 15.1 at 5.5 GHz.

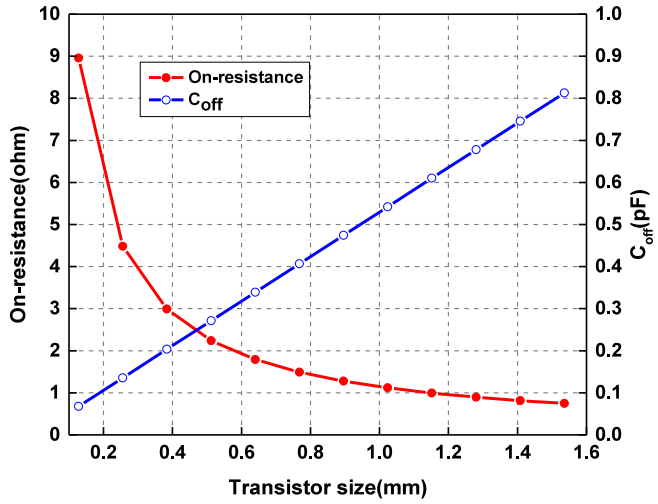


Figure 5.10. On-resistance and C_{off} of the switch transistor versus size.

The switches SW1 and SW2 are implemented using two-stacked thick gate-oxide transistors, mainly based on the consideration of reliability in the OFF-state [82]-[87]. To reduce the loss caused by the on-resistance of the switch, the transistor's size should be as large as possible since the on-resistance is inversely proportional to the transistor

size. On the other hand, the large transistor size of the switch results in large parasitic capacitance in the OFF-state, which cannot be ignored in practical design. In the procedure of determining the optimum values of components in the matching network, the capacitance of the switch in the OFF-state is not taken into account. The on-resistance of the switches R_{SW1} and R_{SW2} depends on the transistor size of the switches. Thus, the on-resistance (R_{on}) and the capacitance (C_{off}) in the OFF-state have been simulated for different transistor sizes, as shown in Figure 5.10. In this design, the transistor sizes of SW1 and SW2 are both 1.536 mm/270 nm. Under this size, the transistor has R_{on} of 0.75 Ω and C_{off} of 0.77 pF. Correspondingly, the on-resistance R_{sw} and OFF-capacitance $C_{sw\text{-}off}$ of the switches consisting of two stacked transistors are 1.5 Ω and 0.385 pF. In above section, the calculated optimum values of C_2 are 2.08 pF and 0.62 pF when the switches are in the 'ON' and 'OFF' states, respectively. Accounting for $C_{sw\text{-}off}$ of 0.385 pF, the C_{2a} and C_{2b} are 0.235 pF and 1.69 pF in the implemented circuit. Since the desired C_1 are 1.6 and 0 pF at 2.4 and 5.5 GHz, respectively, C_{1a} and C_{1b} are set at 0 and 3.2 pF. In the 'OFF' state, the final C_1 is 0.31 pF rather than 0 pF at 5.5 GHz due to $C_{sw\text{-}off}$. Consequently, the resulted load impedance is 25.6 + j12.6 Ω at 5.5 GHz when the switches are off and is 21+ j18.1 Ω at 2.4 GHz with the switches turned on. As shown in Figure 5.11, the deviation between the achieved load impedance and the optimum impedance results in the PAE degradation by 3% at 5.5 GHz, which is acceptable in practice. Finally, the loss of the implemented output matching network is 1.45 and 1.25 dB at 2.4 and 5.5 GHz, and the efficiency of the implemented output matching network is 71.6% and 75% at 2.4 and 5.5 GHz, respectively. In comparison, the passive efficiency of the matching network in [29] is ~70%, and that in [31] is 64.2% and 68.5% at 3 and 9 GHz. Furthermore, to verify the matching performance in the whole 5-GHz band, the achieved load impedance at 4.9 and 5.9 GHz are also demonstrated in Figure

5.11 together with the load-pull simulation results. Across the 5-GHz band, PAE will degrade by 3%, and the output power will decrease by at most 0.3 dBm due to the deviation between the achieved impedances and the optimum impedances. Thus, the impedance matching network can be designed in the whole 5-GHz band with a little performance degradation.

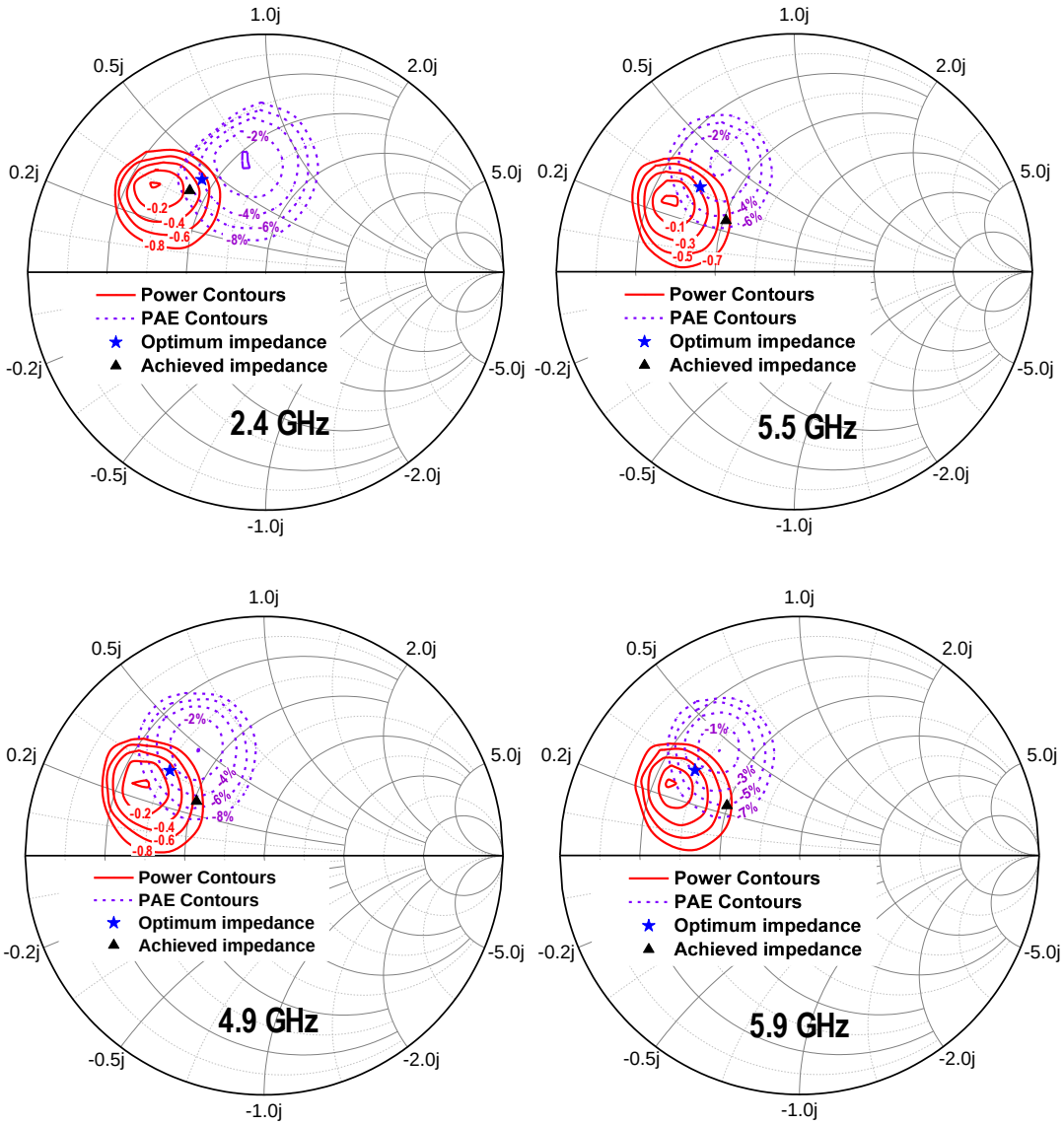


Figure 5.11. Achieved load impedance of implemented output matching network in 2.4- and 5-GHz bands.

5.2.4 Implementation and measurement of dual-band PA

Based on the proposed output matching network, a reconfigurable dual-band PA is

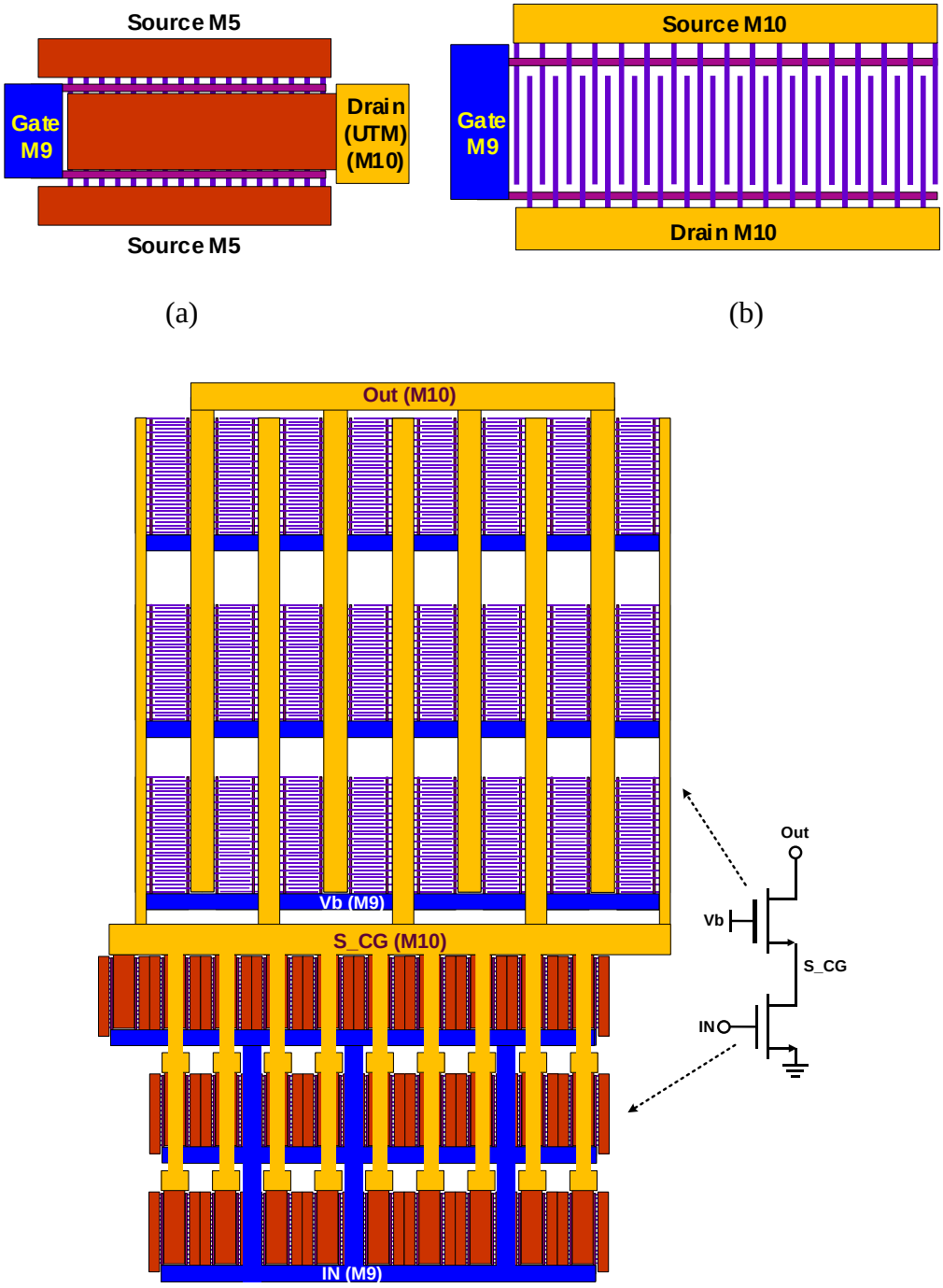


Figure 5.2. Layout of the cascode structure in the PA core.

designed and implemented in TSMC 40-nm RF CMOS technology. Figure 5.12 (a) shows the proposed layout of the unit transistor cell in the common source device in the PA core. This unit transistor cell consists of 32 fingers with a finger width of 1 μm (size: 32×1 μm/40 nm), occupying an area of 6.6×2.5 μm^2. Figure 5.12 (b) shows the proposed

layout of unit transistor cell for the common gate device in the PA core. It consists of 32 fingers with a finger width of 2 μm (size: 32×2 μm/270 nm), occupying an area of 17.6×8.5 μm^2. Thus, the common source device has 28 transistor cells and the common gate devices has 24 transistor cells. The proposed layout of the cascode structure in the PA core is shown in Figure 5.12 (c), and the areas of the common source device and the common gate device are 44×27 μm^2 and 60×56 μm^2, respectively.

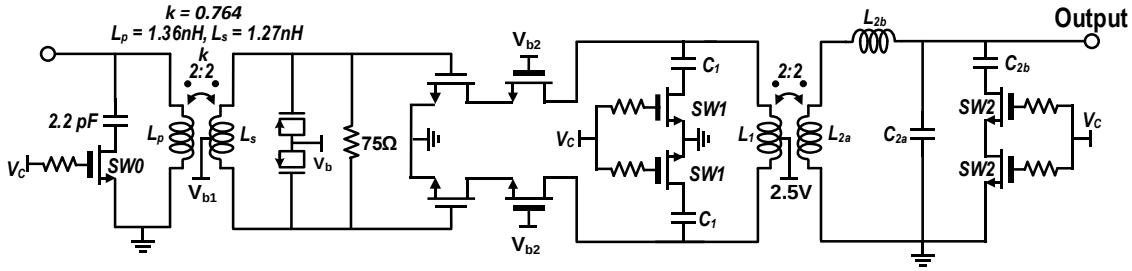


Figure 5.13. Schematic of the dual-band PA.

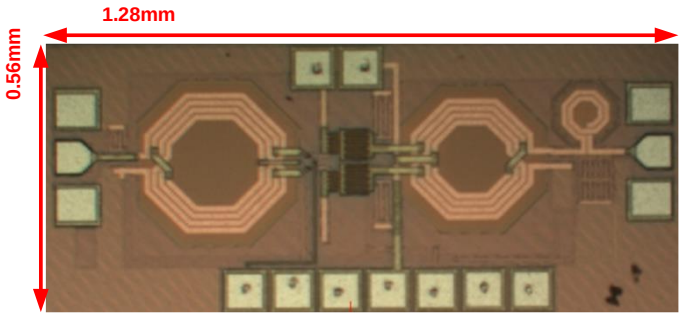
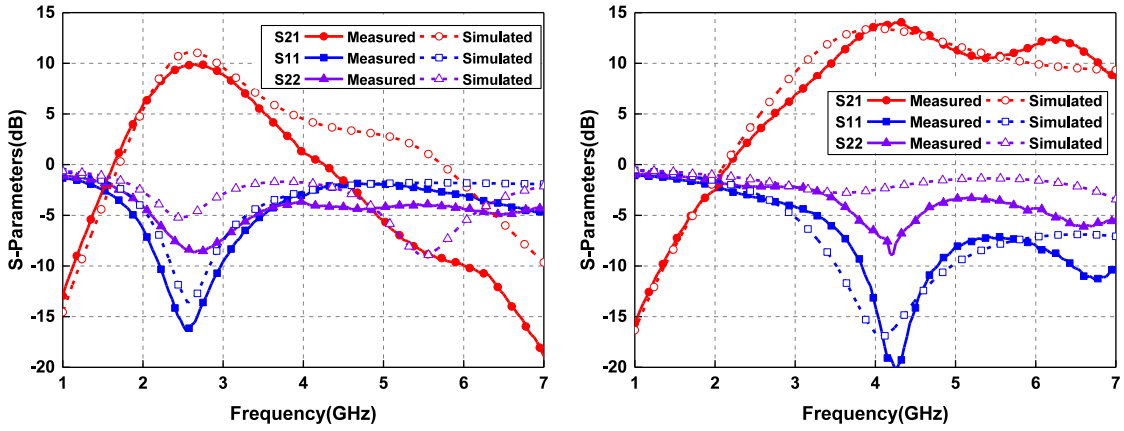


Figure 5.14. Micrograph of the fabricated PA.

The schematic of the PA is shown in Figure 5.13. In the PA, the capacitance compensation technique is also employed to minimize the variation of the input capacitance of the common source transistors. After the compensation, the total capacitance of the PMOS varactors and input capacitance of the common source transistors is 1.25-1.44 pF with different input voltage. A switchable input matching network using a transformer is designed to change the operating frequency. The parameters of the components in the input matching network are given in Figure 5.13. Compared with the switches in the output matching network, the on-resistance of the

switch in the input matching network is not an important issue. The transistor size of the switch in the input matching network is 0.768 mm/270 nm, and the on-resistance of this switch is 1.5 Ω. Figure 5.14 shows the micrograph of the fabricated PA with a die area of 1.28×0.56 mm^2. To evaluate the performance of the implemented PA, different types of measurements have been carried out as follows.

A. Performance with single-tone continuous wave (CW) signal



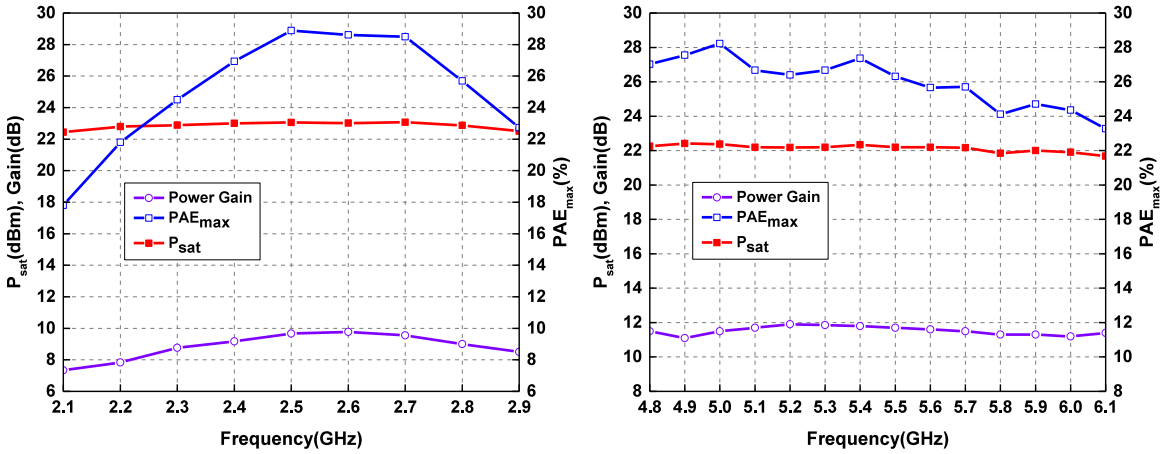
(a) (b)

Figure 5.15. Measured S-parameters. (a) 2.4-GHz mode. (b) 5-GHz mode.

The PA is biased in class-AB condition with a quiescent current of 41 mA (5% × I_{max}), under a supply voltage of 2.5 V, based on the trade-off between linearity and efficiency. For class-AB mode, the linearity of PA is superior to that in class-B mode, and the efficiency is higher than that in class-A mode [25], [72]. Small-signal S-parameters were measured to validate the basic amplification function. The measured S-parameters are plotted in Figure 5.15.

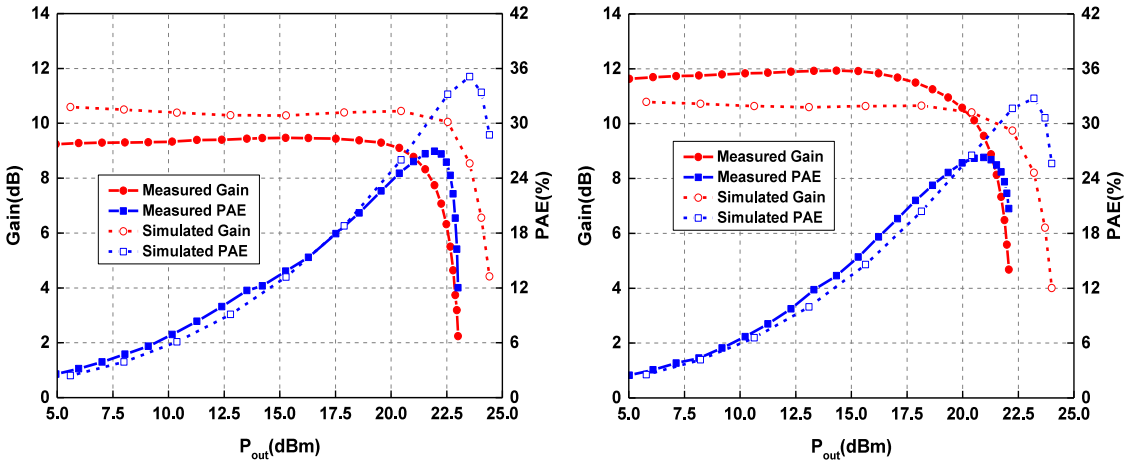
To characterize the power gain, output power and efficiency of the PA, CW signals were employed as the stimulus to the PA from 2.1 to 2.9 GHz and from 4.8 to 6.2 GHz. Figure 5.16 depicts the measurement results, in terms of maximum PAE, saturated output power (P_{sat}) and power gain. In the interested 2.4- and 5-GHz bands, P_{sat}'s are 23 and 21.9-22.4 dBm, and PAEs are 27% and 24.2-28.2%, respectively. Besides, the power

gain of the PA is 9.2 dB and 11.3-11.9 dB at 2.4 GHz and in 5-6 GHz, respectively. Moreover, the measured power gain and PAE versus output power at 2.4 and 5.5 GHz are depicted in Figure 5.17 together with the simulated results. In addition, the main single-tone CW performance of the proposed PA is summarized and compared with other broadband PAs and reconfigurable dual-band PAs in Table 5-1, illustrating that the proposed PA outperforms other broadband and dual-band PAs in PAE.



(a) (b)

Figure 5.16. Measured P_{sat}, power gain and PAE_{max} at different frequencies.



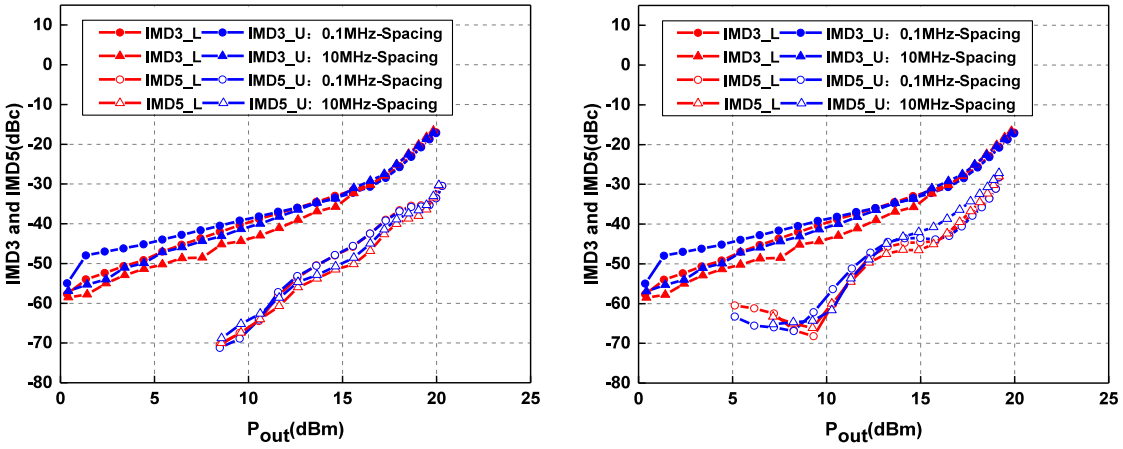
(a) (b)

Figure 5.17. Measured power gain and PAE versus output power. (a) At 2.4 GHz. (b) At 5.5 GHz mode.

Table 5-1. Performance comparison with other broadband and dual-band PAs.

Ref.	Freq (GHz)	Gain (dB)	P_{sat} (dBm)	PAE (%)	Technology
[29]	2.5/3/3.5	~15	22.5/21.5	16.5/15 (DE)	65nm CMOS
[30]	3.1/8	17/7.5	24.3/21.2	33.4/7.7	180nm CMOS
[25]	2-6	22.8-24.4	20.1-22.4	19-28.4	65nm CMOS
[88]	2.6/4.5	24-27	28.1/26	35.2/21.2	65nm CMOS
This work	**2.4/ 4.9-5.9**	**9.2/ 11.3-11.9**	**23/ 21.9-22.4**	**27/ 24.2-28.2**	**40nm CMOS**

B. Two-Tone Characterization



(a) (b)

Figure 5.18. Measured IMD3 and IMD5. (a) At 2.4 GHz. (b) At 5.5 GHz.

To evaluate the linearity of the PA, inter-modulation distortion (IMD) measurement was performed using two-tone signals. Figure 5.18 demonstrates the measured third-order and fifth-order inter-modulation (IMD3 and IMD5) with respect to the output power with 0.1- and 10-MHz tone spacings at 2.4 and 5.5 GHz, respectively. The results indicate the PA is linear with IMD3 lower than -30 dBc at up to 16.5-dBm single tone output power.

C. Performance with modulation signals

To verify the PA's practical performance for 802.11ax application, the PA was tested using a VHT20, MCS5 signal (20-MHz bandwidth, 64-QAM modulation, 3/4 code rate), a VHT40, MCS10, signal (40-MHz bandwidth, 1024-QAM, 3/4 code rate, 10.3-dB PAPR), and a VHT80, MCS10 signal (80-MHz bandwidth, 1024-QAM, 3/4 code rate, 11-dB PAPR). The measurement platform is shown in Figure 5.19, and no digital pre-distortion (DPD) is used in EVM measurement.

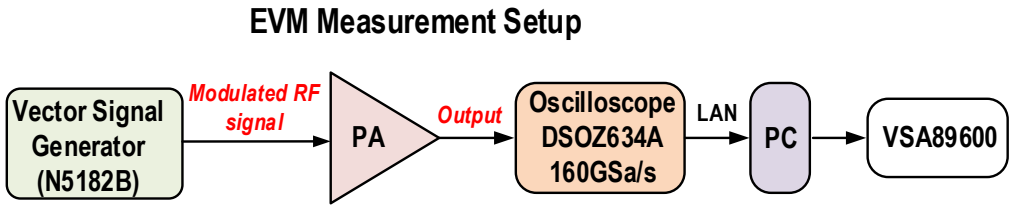
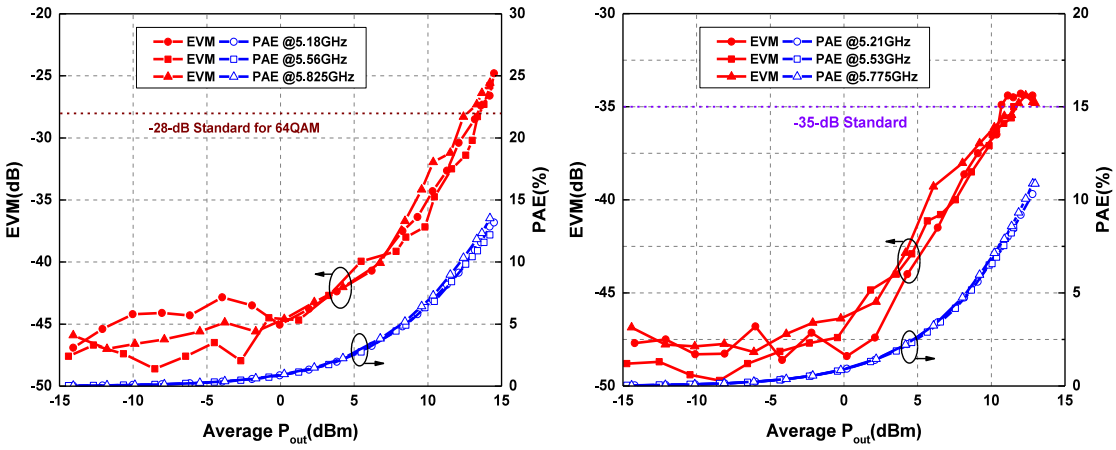


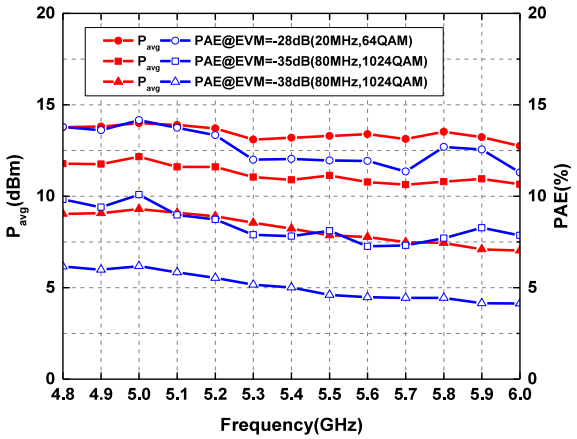
Figure 5.19. PA's EVM measurement setup.

EVM was first measured across the 5-GHz band, and the measured results are reported in Figure 5.20. For the VHT80, MCS10 signal, when EVM is -35 dB, the PA delivers an average output power of 10.95-12.16 dBm and achieves a PAE of 7.3-10.1% in the 5-GHz band. Although the standard EVM requirement for the 1024-QAM modulation is -35 dB, the PA should have a more stringent EVM requirement, and at least, the 3-dB margin of EVM is necessary for the PA [89]-[91]. At -38-dB EVM, the PA delivers an average output power of 7-9.3 dBm with 4.1-6.2% PAE in 5-GHz band.

Then, EVM was measured at 2.442 GHz (Channel-7), and the measured EVM in different output power levels and the corresponding PAEs are plotted in Figure 5.21 (a). For the VHT40, MCS10 signal, the PA delivers 12.8-dBm average output power with 9% PAE when EVM is -35 dB. When satisfying -38-dB EVM, the PA delivers 10.2-dBm average output power with 5.7% PAE. Besides, EVM was measured from 2.1 to 3 GHz, and the results are reported in Figure 5.21 (b). Finally, a detailed comparison between the performance of the proposed dual-band PA and other PAs designed for 5-GHz WLAN 802.11ac/ax is given in Table 5-2.

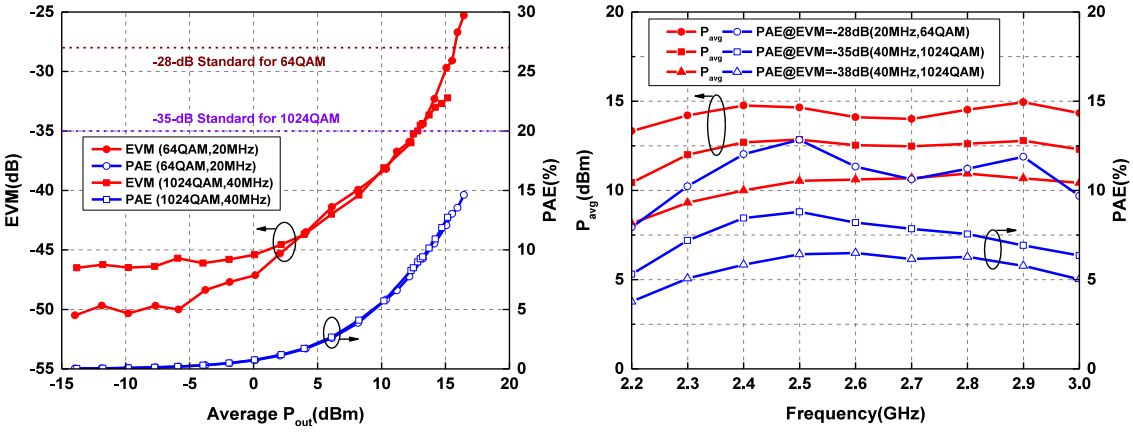


(a) (b)



(c)

Figure 5.20. Measured EVM performance in 5-GHz band. (a) EVM and PAE in different average output power levels for 20MHz, 64-QAM signal. (b) For 80MHz, 1024-QAM signal. (c) P_{avg} and PAE versus frequencies when EVM requirements are satisfied.



(a) (b)

Figure 5.21. Measured EVM performance in 2.4-GHz mode. (a) EVM and PAE in different average output power levels at 2.442 GHz. (b) P_{avg} and PAE versus frequencies when EVM requirements are satisfied.

Table 5-2. Performance comparison of state-of-the-art 802.11ac PAs

Ref.	Technology	Modulation	Bandwidth (MHz)	Pout (dBm)	EVM (dB)	PAE (%)	VDD (V)	Area (mm^2)
This work	**40nm CMOS**	**11ax 1024-QAM**	**80**	**12.1**	**-35**	**10.1**	**2.5**	**0.72**
		11ax 64-QAM	**20**	**14**	**-28**	**14.1**		
TMTT'2017 [92]	0.13µm CMOS	11ac 256-QAM	80	15.6	-35	7.5	3.6	0.62
JSSC'2015 [93]	40nm CMOS	11ac 64-QAM	40	15.3	-28	13.6	2.5	1.07
RFIC'2015 [19]	40nm CMOS	11ac 256-QAM	80	14.8	-32	9.3	2.4	N.A
RFIC'2015 [94]	SiGe BiCMOS	11ac 256-QAM	80	17	-35	7.8	3.3	1.6
RFIC'2012 [95]	SiGe BiCMOS	11ac 64-QAM	80	17.7	-34	10.1	3.3	2.4

5.3 2.4/5-GHz Dual-band Transmitter Front-End

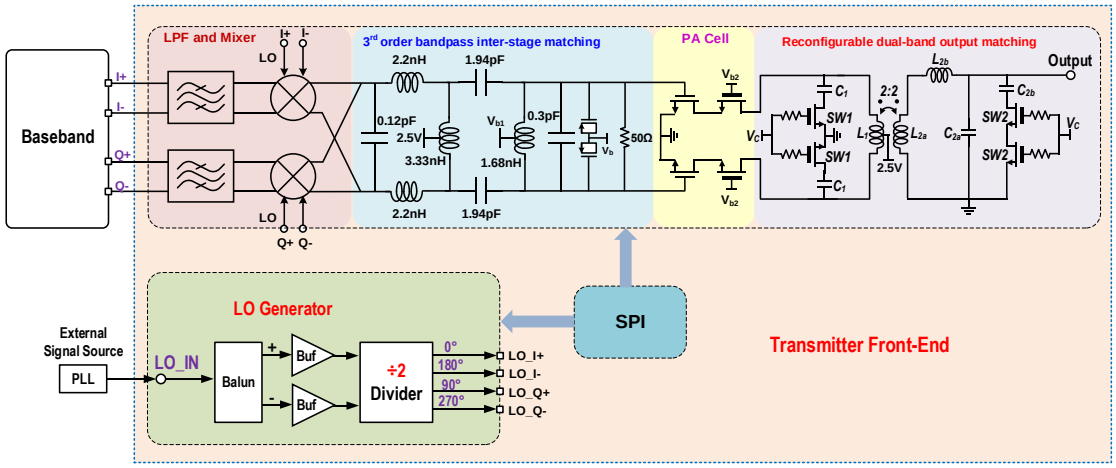


Figure 5.22. Diagram of the transmitter front-end.

A reconfigurable power amplifier operating in 2.4- and 5-GHz WLAN bands has been proposed in the proceeding section. This section presents a reconfigurable 2.4/5-GHz dual-band transmitter front-end designed based on the proposed PA. The diagram of the proposed transmitter front-end is shown in Figure 5.22, including LO generator, tunable lowpass filter (LPF), active mixer, broadband inter-stage matching, and PA stage. The PA stage has the same cascode devices and the same reconfigurable dual-band output matching network as the proposed PA has. Here, we skip the details of the design of the PA stage. The design of the circuit blocks including LPF, mixer and LO generator will be presented in this section, as well as the inter-stage matching network between the mixer and the PA stage.

5.3.1 LPF and Mixer

Since 802.11ax signals have different bandwidths, the cut-off frequency of the analog baseband LPF is required to be adjustable accordingly. In the proposed transmitter front-end, the Tow-Tomas biquad filter is used [48], [96], [97], as shown in Figure 5.23. In order to tune the filter's cutoff frequency, a programmable capacitor network is used, and the cutoff frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{R_2 R_3 C_1 C_2}} \tag{5.27}$$

Since the analog bandwidth of 802.11ax baseband signal is half of the bandwidth of the signal, the tunable 3-dB cutoff frequencies of the filter are set to 15, 30, and 60 MHz for 802.11ax signal with 20-, 40-, 80-MHz bandwidths, respectively.

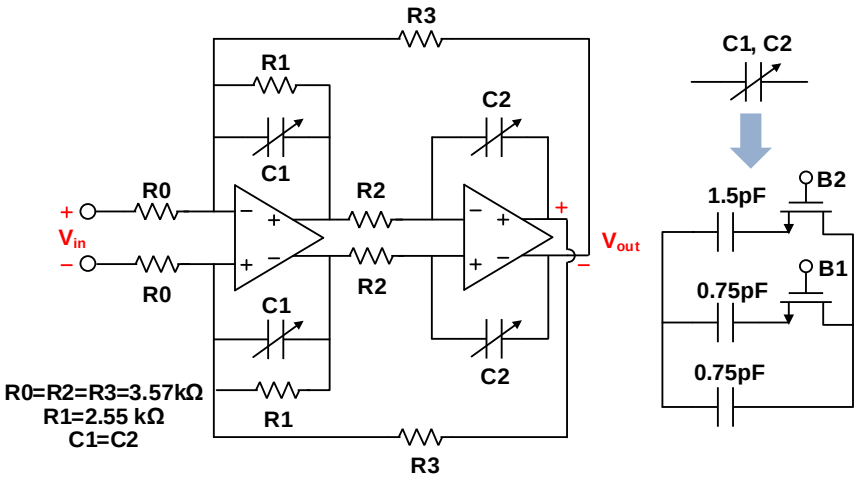


Figure 5.23. Schematic of the LPF.

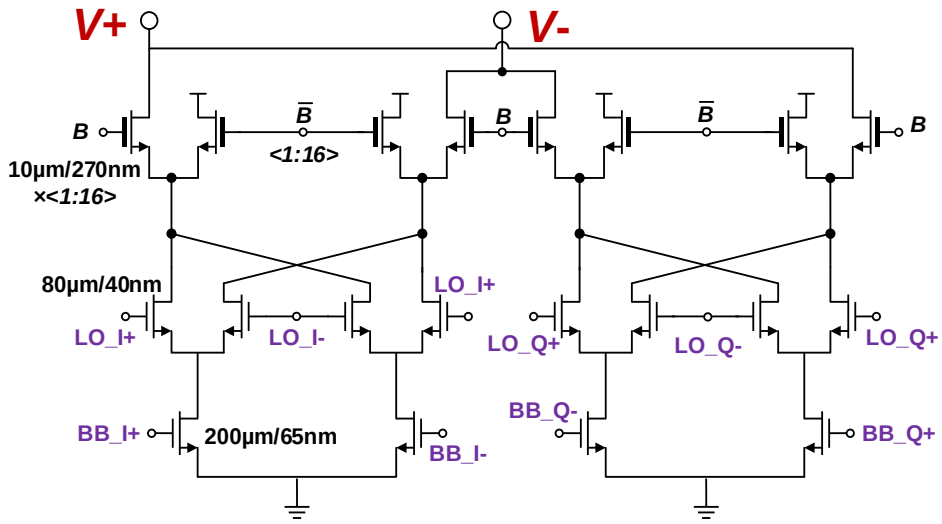


Figure 5.24. Schematic of the mixer.

Mixer design requires many compromises among different figures of merit, such as conversion gain, LO power, linearity, noise figure, port-to-port isolation and total power dissipation. In this work, an active mixer is used rather the counterpart passive mixer, by virtue of high conversion gain and large port isolation, and the proposed mixer is shown

in Figure 5.24. The mixer is driven by a quadrature 50%-duty-cycle clock, which is generated from the LO generation block. A 5-bit current-steering gain control unit is stacked on the mixer, and the range of the control gain is around 24 dB. In order to keep sufficient voltage headroom and deliver a high output power to the PA, the supply voltage for the mixer is chosen to be 2.5 V, and thick-gate-oxide transistors are used in the current-steering gain control unit.

5.3.2 Inter-stage matching between mixer and PA stage

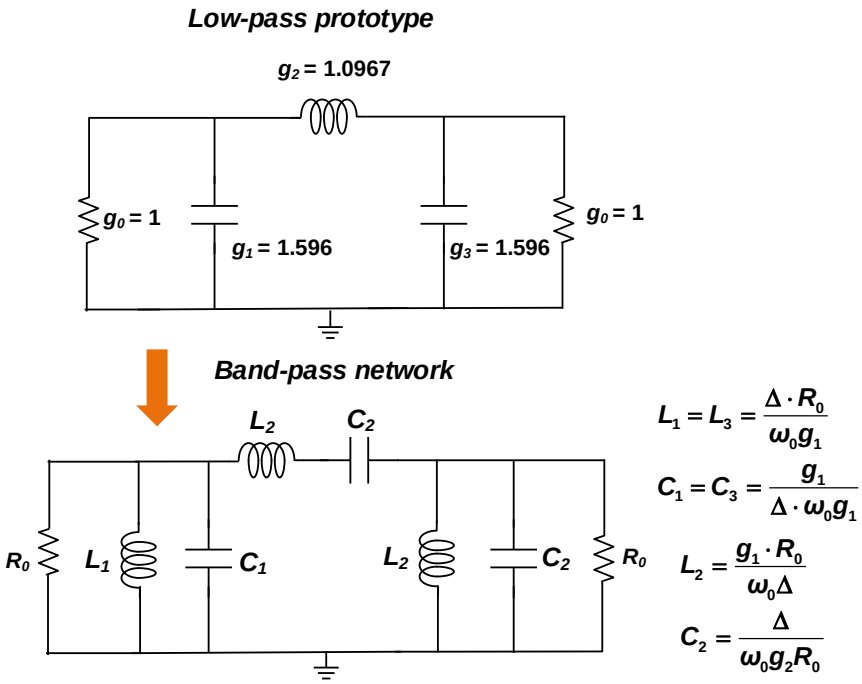


Figure 5.25. Low-pass prototype and band-pass network.

The inter-stage matching is designed as a third-order bandpass matching [24], [25], [98], which can cover the frequency range from 2 to 6 GHz. Since the mixer can be approximated as the current source, the bandpass matching can achieve a constant transimpedance transfer function, providing flat driving power to the following PA across a broad operating band. The inter-stage matching is designed based on the third-order Chebyshev lowpass network prototype with a 0.5-dB ripple. Figure 5.25 shows this lowpass network prototype with the coefficients g_1, g_2 and g_3 and its bandpass

configuration [99], [100].

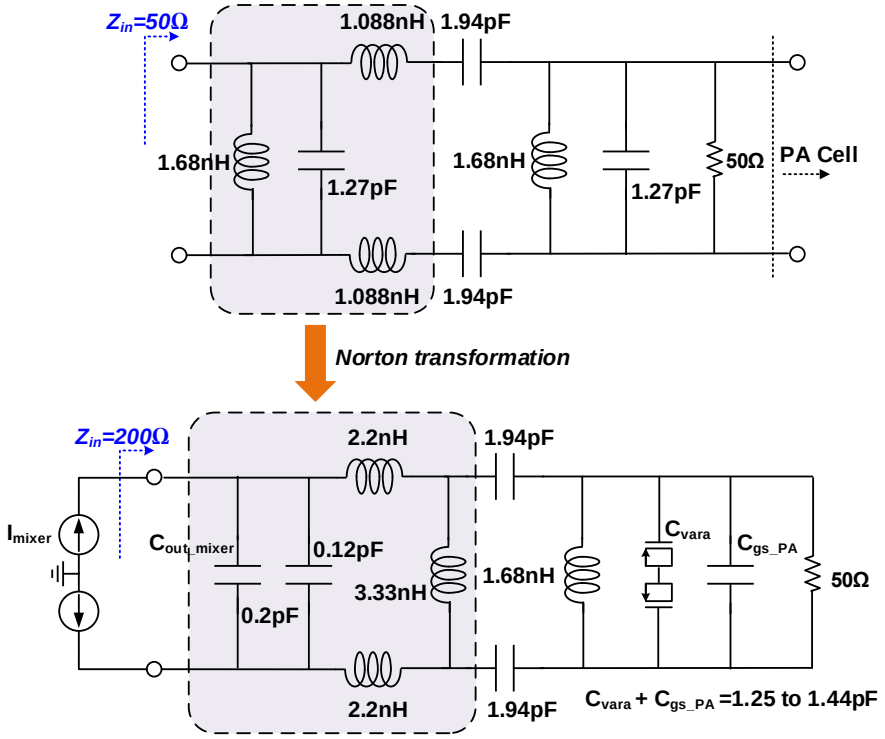


Figure 5.26. Inter-stage matching network and Norton transformation.

In the PA's input side, a 50-Ω resistor is used to reduce G_{max} and ensure stability. Since the input impedance of the PA cell is high, the 50-Ω resistor can be viewed as the load R_0 shown in Figure 5.25. Then, the parameters of the components in the bandpass network are: $L_1 = L_3 = 1.68$ nH, $C_1 = C_3 = 1.27$ pF, $L_2 = 1.088$ nH, and $C_2 = 1.94$ pF. In the proposed transmitter front-end, the mixer drives the PA directly without any driver between the mixer and the PA. Otherwise, one more inter-stage matching between the driver and the PA is required, which will intensify the design complexity and increase the chip size. Therefore, the load impedance for the mixer should be large enough to ensure a sufficient transmission gain from the mixer to PA. A generic double-termination third-order bandpass network has equal impedances at two terminations; thereby, the mixer will have a low load impedance due to the 50-Ω resistor used in the PA's input. In general, the mixer's output can be assumed as a current source, thus, a large load

impedance will produce a large output voltage. While, in this case, the low load impedance will cause a low transmission gain and an insufficient power from the mixer to drive the PA. To address this issue, a Norton transformation is employed to boost the load impedance from 50 Ω to 200 Ω for the mixer and increase the mixer's output power [24], [101]. Here, we follow the procedure of Norton transformation demonstrated in [24]. Figure 5.26 shows the details of the final inter-stage matching network. In the matching network, the total capacitance of the PMOS varactors and the input capacitance of the PA cell is from 1.25 to 1.44 pF, which is around the desired value of 1.27 pF for C_2. Thus, this total capacitance serves as C_2. Besides, the output capacitance of the mixer also serves as one part of capacitance in the matching network.

5.3.3 LO generator

Since PLL is not integrated on-chip and an external signal source will be used to provide the LO input signal, a balun is required to convert the single-ended input signal from the external source to a differential signal. In this work, the same balun presented in Chapter 4 is used, since the previous simulation results have proved this balun has an excellent differential performance.

The divider to generate 50%-duty-cycle clock uses current-mode logic (CML) latch [65], [66], which is also the same divider used in the carrier aggregation transmitter front-end proposed in Chapter 4. For 2.4-GHz and 5.5-GHz output, the simulated phase noises are -147.2 dBc/Hz and -149.2 dBc/Hz at 0.1-MHz offset, and are -154.7 dBc/Hz and -156.5 dBc/Hz at 1-MHz offset, respectively.

5.3.4 Implementation and measurement of dual-band transmitter front-end

The transmitter front-end was fabricated in the same TSMC 40-nm RF CMOS technology, Figure 5.27 shows the micrograph of the fabricated transmitter front-end chip with a dimension of 1.94×0.54 mm^2. In the measurement, the transmitter front-end

chip was bonded on the PCB implemented using RO4350 substrate with the thickness of 20-mil and the dielectric constant of 3.5.

Figure 5.27. Micrograph of the fabricated dual-band transmitter front-end.

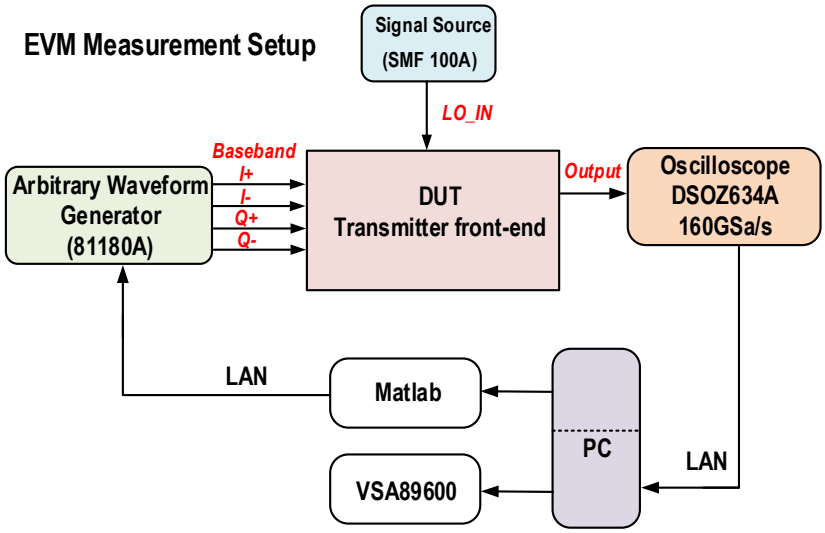


Figure 5.28. EVM measurement setup.

The measurement setup is shown in Figure 5.28. EVM was first measured in the 5-GHz mode, by using the VHT20, MCS5 signal at 5.18, 5.56 and 5.825 GHz, in Channels 36, 112 and 165, and then measured by using the VHT80, MCS10 signal at 5.21, 5.53 and 5.775 GHz, in Channels 42, 106 and 155. The measured EVM in different average output power levels are reported in Figure 5.29. For the VHT80, MCS10 signal, when satisfying the standard specification of EVM ≤ -35 dB, the transmitter delivers an average output power of 6.72, 6.91 and 6.95 dBm at 5.21, 5.53 and 5.775 GHz, respectively.

Then, the transmitter was measured at 2.442 GHz, and the measured EVM and PAE

with respect to the average output power are reported in Figure 5.30. The transmitter delivers 10.8- and 8.1-dBm average output power when EVM ≤ -28 dB for the VHT20, MCS5 signal and EVM ≤ -35 dB for the VHT40, MCS10 signal, respectively. Since the PAPR of the VHT80, MCS10 signal is as high as 11 dB, a large back-off is required for the transmitter to meet the stringent EVM requirement of -35 dB for 1024-QAM modulation without using DPD. If DPD is employed, the average output power will be increased by a large degree, while it is beyond the scope of this work.

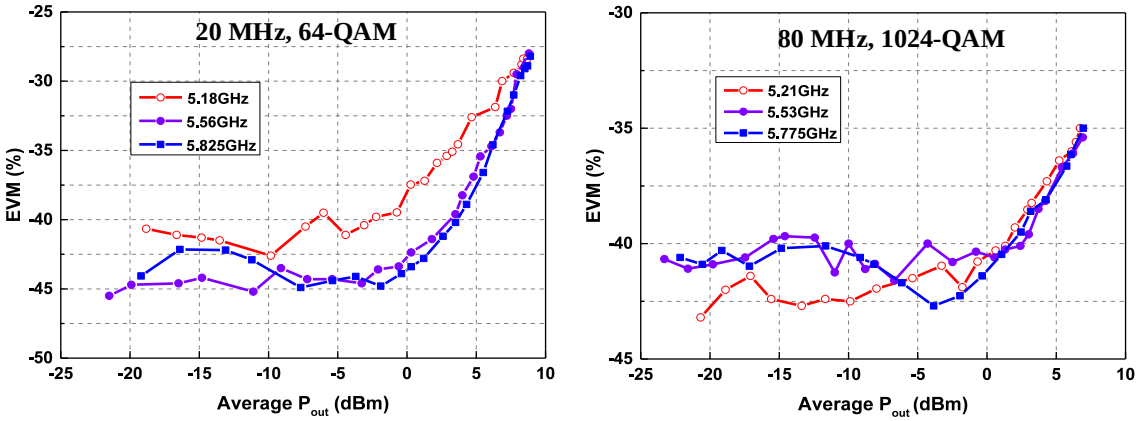


Figure 5.29. Measured EVM versus output levels for different modulation signals in 5-GHz mode.

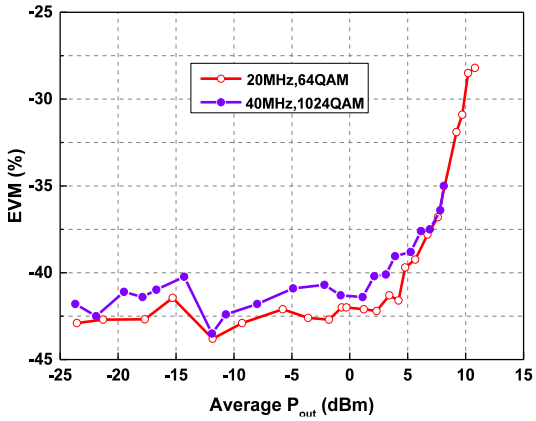


Figure 5.30. Measured EVM in different output levels for modulation signal at 2.442 GHz.

In addition, the measured 1024-QAM constellation for theVHT80, MCS10 signal

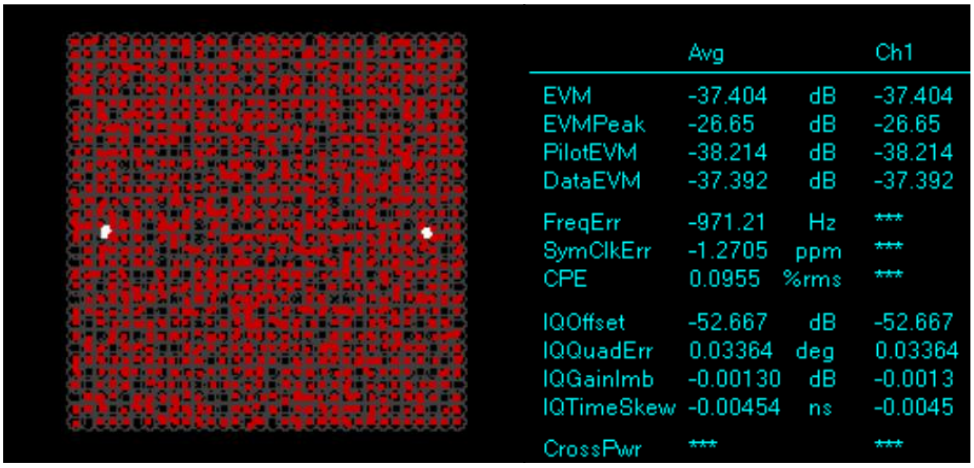
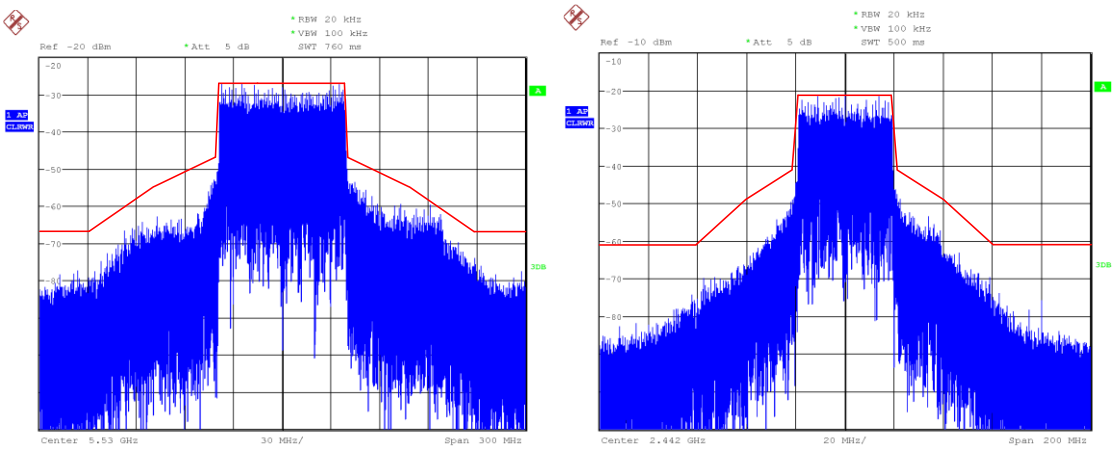


Figure 5.3. Measured 1024-QAM constellation at 5.53 GHz.



(a) (b)

Figure 5.4. Output spectrum from transmitter front-end. (a) VHT80, MCS10 signal at 5.53 GHz. (b)VHT40, MCS10 signal at 2.442 GHz.

with -37.4-dB EVM at 5.53 GHz is illustrated in Figure 5.31. Besides, the output spectrum with -35-dB EVM for the VHT80, MCS10 signal at 5.53 and the VHT40, MCS10 signal at 2.442 GHz are depicted in Figure 5.32 shows that the requirement of the emission mask is satisfied both in the 2.4-GHz mode and 5-GHz mode. Meanwhile, the measured performance is summarized and compared with other recent 2.4-/5-GHz dual-band WLAN transceivers in Table 5-3. In these dual-band WLAN transceivers, two RF channels are employed to realize a 2.4-/5-GHz dual-band operation, while the dual-

Table 5-1. Transmitter front-end performance summary and comparison with state-of-the-art 802.11ac/ax transmitter.

		This work	ISSCC2018 [15]	ISSCC2017 [20]	JSSC2017 [14]
WLAN standards		11abgn/ac/**ax**	11abgn/ac/**ax**	11abgn/ac	11abgn/ac
Process (nm)		40	28	40	40
2.4/5G Dual-band		Yes	Yes	Yes	Yes
Configuration		**Single Transmitter**	Multiple Transmitter	Multiple Transmitter	Multiple Transmitter
Modulation signal	2.4G	VHT40, MCS10,11ax	VHT40, MCS10,11ax	LG54M	LG54M
	5G	VHT80, MCS10,11ax	VHT80, MCS10,11ax	VHT80, MCS9,11ac	VHT80, MCS9,11ac
1024-QAM		**Yes**	Yes	No	No
TX Pout (dBm) @ EVM=-35dB	2.4G	8.1	-5	21.3 (EVM=-28dB)	23.5 (EVM=-28dB)
	5G	6.95	-5	19	17
EVM floor	2.4G	**-42.5**	-42.5	N.A	-40
	5G	**-40**	-38.1	-36.8	-38
RF Power Consumption (mW)	2.4G	206 @(8.1 dBm)	844 @(-5 dBm)	3863 @(21.3 dBm)	1460 @(20 dBm)
	5G	195 @(6.95 dBm)	832@(-5 dBm)	4161@(22 dBm)	1750@(17.5 dBm)
Transmitter Efficiency (%)	2.4G	3.13	0.156	3.49	6.85
	5G	2.54	0.156	3.81	3.21

band operation can be achieved in the proposed transmitter front-end using only one transmitter channel. Compared with the transmitters using two RF channels, the main

advantage of the proposed transmitter front-end is that only one channel is used to achieve a dual-band operation. To authors' knowledge, the proposed transmitter front-end is the first design for dual-band WLAN 802.11ax application in the literature.

5.4 Summary

In this chapter, a new reconfigurable dual-band output matching methodology is proposed. In the proposed methodology, the on-resistance is taken into consideration to optimize the passive efficiencies of the output matching network at both 2.4 and 5.5 GHz. Based on the proposed methodology, a standalone PA supporting the 2.4/5-GHz dual-band operation was firstly designed for WLAN 802.11ax application. A step-by-step design procedure of the output matching network is demonstrated. The measurement results validate the proposed matching methodology. Besides, the PA exhibits a promising performance in comparison with other broadband PAs and reconfigurable dual-band PAs in the literature. The PA was measured using the 802.11ax signals with 1024-QAM modulation, and the measurement results shows the PA features a good linearity. Secondly, a 2.4/5-GHz transmitter front-end was designed from the standalone PA. The measurement results verify the transmitter front-end can operate both in the 2.4- and 5-GHz modes, and the transmitted signals can meet the requirement of the emission mask for 802.11ax when the measured EVM is -35 dB. Since only one RF channel is used, the proposed transmitter front-end has a distinct advantage in less complexity, small chip size and low cost, in comparison with other state-of-the-art dual-band WLAN transmitters using two RF channels.

Chapter 6

Conclusion and Future Works

In this chapter, the conclusions of the whole thesis will be drawn and some recommendations for the future work will be discussed.

6.1 Conclusions

The research work in the thesis is focused on the CMOS transmitter front-end for 802.11ax application.

In Chapter 2, different transmitter architectures for carrier aggregation are reviewed and compared in terms of their applicability, cost and complexity of system. Besides, the state-of-the-art WLAN 2.4/5-GHz dual-band transmitter architectures reviewed.

In Chapter 3, two inherent problems of crosstalk and VCO pulling related to carrier aggregation caused by the interaction between RF channels are discussed. Theoretical analysis indicates that EVM is vulnerable to crosstalk and ACLR is seriously affected by VCO pulling. To explore the strength of the interaction between two signal processing channels, the coupling factor between the active devices and between the passive signal traces are simulated. The simulation results show large physical isolation is required to achieve sufficiently low coupling such that the coupling has negligible on EVM and ACLR.

In Chapter 4, considering large physical isolation may not be realizable in some practical cases due to the constraint of layout, a new transmitter architecture using parallel direct-conversion and double-conversion configuration is proposed to solve the problems of crosstalk and VCO pulling simultaneously without large physical isolation requirement. A prototype transmitter front-end supporting 2-carrier aggregation for 5-GHz WLAN 802.11ax application is implemented in TSMC 40-nm CMOS technology

to verify the proposed architecture. For the contiguous carrier aggregation, the measured EVM reaches -36.1 dB for the VHT80 MCS9 signals, verifying a good EVM performance is achieved without large physical isolation on-chip.

In Chapter 5, a new reconfigurable dual-band output matching methodology is proposed to extract high passive efficiency. Based on the proposed methodology, a standalone 2.4/5-GHz dual-band PA and a transmitter front-end are designed to meet the requirement of the dual-band operation for WLAN 802.11ax systems. The implemented output matching network achieves a passive efficiency of 71.6% and 75% at 2.4 and 5.5 GHz, respectively. In the 2.4- and 5-GHz WLAN bands, the implemented PA achieves a P_{sat} of 23 and 21.9-22.4 dBm with power-added efficiency (PAE) of 27% and 24.2-28.2%, respectively. The PA exhibits a promising performance in comparison with other broadband PAs and reconfigurable dual-band PAs in the literature. At 2.442 GHz, the transmitter delivers 8.1-dBm average output power for 40-MHz, 1024-QAM 802.11ax signal, while EVM $\leq$ -35 dB. In the 5-GHz operating mode, the transmitter achieves an average output power of 6.72-6.95 dBm with the EVM of -35 dB for 80-MHz, 1024-QAM 802.11ax signal. These measurement results validate the function of the transmitter front-end in the dual-band operation.

6.2 True power detector

In modern communication systems, such as LTE-Advance, WLAN and etc, to optimize the power consumption, it is required to monitor the transmitted RF power accurately and adjust the RF power according to the channel quality. For this reason, a highly accurate power detector is required to detect the RF PA's output power in the power control loop, which is critical in a high-performance mobile system.

Hence, many power detection techniques have been proposed, and most of these techniques only detect the voltage or current to determine the RF output power [102]-

[104]. The accuracy of these techniques can be ensured only when the load impedance of the antenna is fixed. However, in practice, the load impedance of the antenna may not be fixed and may change even for one same antenna with different output power levels. Therefore, it is difficult to use the conventional power detectors to accurately measure the true RF output power under antenna load impedance variations. In theory, output power is defined as the product of the voltage and current, and the product is defined by

$$\begin{aligned} P_{out}(\mathrm{t}) &= v_{out}(t) \times i_{out}(t) \\ &= V_{out}\cos(\omega t) \times I_{out}\cos(\omega t + \varphi) \end{aligned} \tag{6.1}$$

where φ is the phase difference between the voltage and current. In LTE-A and WLAN systems, since the envelope of RF signal is not constant, the average output power is more important in the power control loop, which is defined as the time average of the instantaneous output power by

$$\begin{aligned} P_{out}(\mathrm{t}) &= \frac{1}{\tau}\int_0^{\tau} v_{out}(t) \times i_{out}(t) \\ &= \frac{1}{2} V_{out} I_{out}\cos(\varphi) \end{aligned} . \tag{6.2}$$

Based on the definition of the average output power in Equation 6.2, a true power detector is proposed in [105], as shown in Figure 6.1. This power detector detects both the output voltage and current simultaneously and uses a multiplier to obtain a product of the voltage and current. The current is sensed through a coupling coil in the output transformer in the PA without affecting the output matching [105], [106], shown in Figure 6.2. In this coupled transformer, the magnetic field created by the current flow through the first coil is coupled to the sense coil, inducing a voltage in the sense coil depending on the load impedance of the sense coil.

6.3 Transmitter with true power detector for carrier aggregation

In carrier aggregation transmitter, the output power of each carrier is required to be

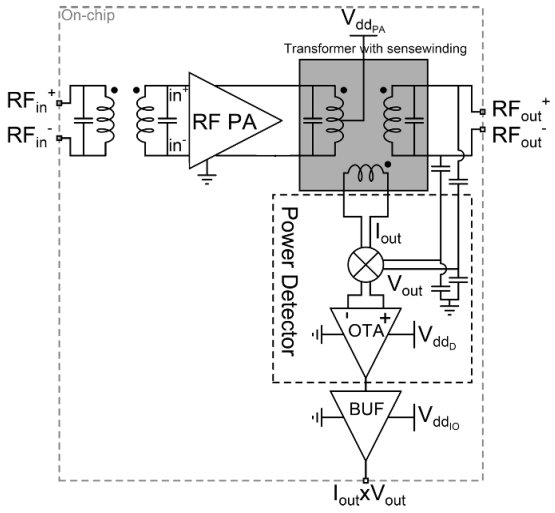


Figure 6.1. True power detector [105].

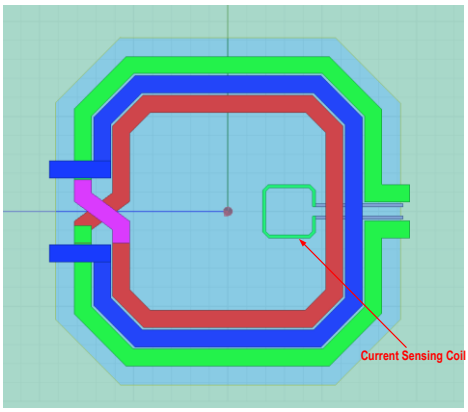


Figure 6.2 Transformer with current sense coil

detected separately in the power control loop. In our proposed transmitter architecture, the PA's output contains all the carriers. For this reason, the proposed true power detectors in the literature only can detect the total output power, but cannot detect the output power for each carrier.

In order to solve this problem, the output voltage and current to be detected have to be separated for each carrier in frequency domain, so that the output power for each carrier could be determined by the separated voltage and current. With this concept, a new transmitter with a true power detector for carrier aggregation is recommended for future work, as shown in Figure 6.3. Firstly, the current is sensed by the method as

discussed in [105], and the voltage is captured by a simple capacitor voltage divider. Secondly, the sensed voltage and current are down converted using the mixers driven by the same LOs in the transmitter chain to separate two carries in frequency domain. This down-conversion process is inverse to the up-conversion process in the transmitter chain. And then, the down-converted voltage and current are filtered by a low pass filter to filter out the interference from other carriers. After that, two multipliers are used to generate the product of the voltage and current for each carrier, and two amplifiers are used following the multipliers to amplify the product of the voltage and current.

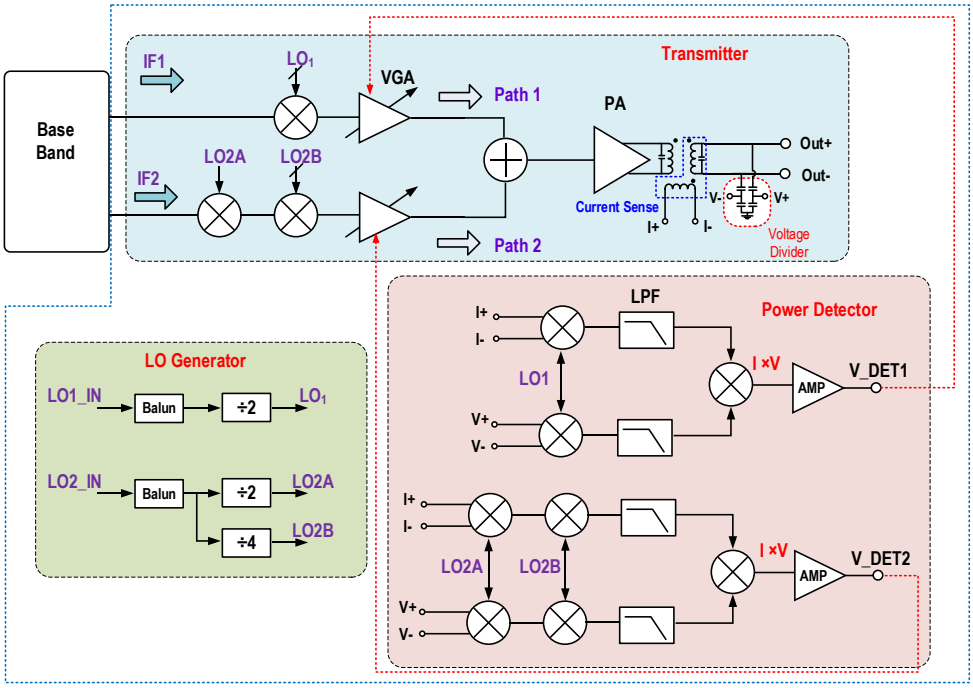


Figure 6.3. Possible transmitter architecture with power detector for carrier aggregation.

6.4 Transmitter supporting 2.4/5-GHz dual-band operation and 5-GHz carrier aggregation

In this thesis, we have presented a 5-GHz carrier aggregation transmitter front-end and a 2.4/5-GHz dual-band transmitter front-end for 802.11ax application. Practically, an 802.11ax transmitter supporting both the 2.4/5-GHz dual-band operation and 5-GHz

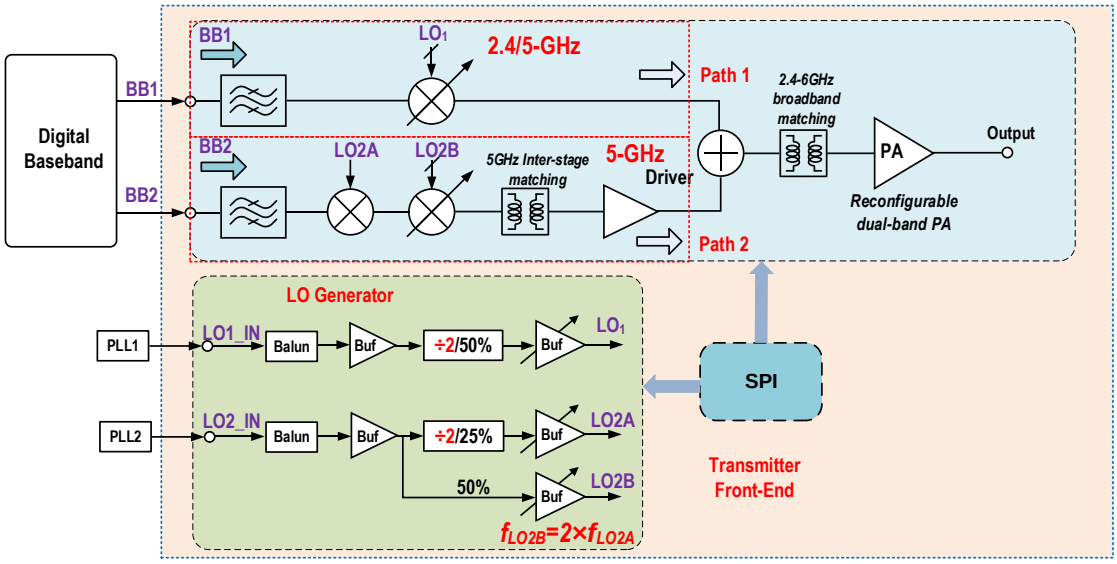


Figure 6.3. Transmitter architecture supporting dual-band and carrier aggregation.

carrier aggregation may be desired. While, our proposed two transmitter front-ends cannot satisfy such requirement. Therefore, one improvement of the research work achieved in this thesis is to combine the proposed two transmitter front-ends into a new transmitter front-end enabling carrier aggregation and dual-band operation capabilities. Thus, we propose a new transmitter architecture based on the two already implemented transmitter front-ends for further work, as shown in Figure 6.4. Similar to the architecture proposed in Chapter 4, this architecture also has one direct-conversion path and one double-conversion path, and the two carriers are combined before the reconfigurable dual-band PA. The reconfigurable dual-band PA can be designed following the methodology proposed in Chapter 5.

When the Path2 and the corresponding LO generation blocks are turned off, the new transmitter front-end will become a dual-band transmitter front-end, almost the same as the transmitter front-end proposed in Chapter 5. On the other hand, when the PA and Path1 both work in the 5-GHz mode, the new transmitter front-end will support 5-GHz carrier aggregation. Hence, the new transmitter front-end will have the both function of the dual-band operation and carrier aggregation, which is the main benefit of this new

transmitter front-end.

Author's Publications

1. **B. Liu**, X. Yi, K. Yang, Z. Liang, G. Feng, P. Choi, C. C. Boon, and C. Li, "A carrier aggregation transmitter front end for 5-GHz WLAN 802.11ax application in 40-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques,* vol. 68, no. 1, pp. 263-275, Jan. 2020.
2. **B. Liu**, X. Quan, C. C. Boon, D. Khanna, P. Choi, and X. Yi, "Reconfigurable 2.4/5-GHz dual-band transmitter front-end supporting 1024-QAM for WLAN 802.11ax application in 40-nm CMOS," Accepted, *IEEE Transactions on Microwave Theory and Techniques*, 2020.
3. **B. Liu**, M. Mao, D. Khanna, C. C. Boon, P. Choi, and E. A. Fitzgerald, "A novel 2.6-6.4GHz highly integrated broadband GaN power amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 1, pp. 37-39, Jan. 2018.
4. **B. Liu**, M. Mao, C. C. Boon, P. Choi, D. Khanna, and E. A. Fitzgerald, "A fully integrated Class-J GaN MMIC power amplifier for 5-GHz WLAN 802.11ax application," *IEEE Microwave and Wireless Components Letters,* vol. 28, no. 5, pp. 434-436, May 2018.
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10. X. Yi, G. Feng, Z. Liang, C. Wang, **B. Liu**, C. Li, K. Yang, C.C. Boon, and Q. Xue, “A 24/77 GHz dual-band receiver for automotive radar applications,” *IEEE Access,* vol. 7, pp. 48053-48059, Mar. 2019.
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