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Leakage current conduction mechanism of three-dimensional capacitors embedded in through-silicon vias

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Leakage current conduction mechanism of three-dimensional capacitors embedded in through-silicon vias has been investigated for two sets of test vehicles, namely “sputtering samples” and “atomic layer deposition (ALD) samples”. Schottky emission, hopping conduction, Poole-Frenkel emission, and Fowler-Nordheim tunneling have been identified for these samples, respectively. Self-consistent parameters are extracted through the analysis of leakage current conduction mechanisms: (1) optical dielectric constant (1.98-3.69), and (2) Schottky barrier height (1.66-2.21 eV). In terms of leakage current density, the ALD process is preferred over the sputtering process during the fabrication because the sputtered electrodes result in more traps in the vertical dielectric layers.

Over the past few years, integrated capacitor is getting considerable attention due to its potential applications in three-dimensional integrated circuits (3D ICs), such as decoupling capacitor, integrated voltage regulator, and others.¹⁻⁴⁾ We have recently proposed a novel approach to implement integrated capacitors, termed “3D embedded capacitors”, to achieve ultrahigh capacitance density.⁵⁻⁶⁾ They are realized by embedding metal-insulator-metal (MIM) layers into the trenches of through-silicon vias (TSVs). As evident from Fig. 1, the premium silicon surface area can be freed up for transistor fabrication if MIM capacitors are implemented in the TSV trenches, instead of their dedicated trenches. Furthermore, as the layer stack in MIM capacitor is typically much thinner than that of TSV diameter (e.g., 0.1 vs 10 μm), 3D embedded capacitors in TSV do not alter the TSV properties significantly. An extremely high capacitance density of up to 5,621.8 nF/mm² is envisioned for 3D embedded capacitor according to our model, and up to 3,776.6 nF/mm² has been demonstrated in our early stage prototypes.⁷⁾ In addition to capacitance density, leakage current density is another key figure of merit (FOM) for integrated capacitors. Low leakage current density is desired to minimize unnecessary power dissipation of the capacitors. Conventional trench capacitors were reported to have higher leakage current density than their planar counterparts due to their vertical structures.⁸⁾ However, leakage current density has not been studied for 3D capacitors embedded in TSVs so far. In this paper, we report our investigation of leakage current conduction mechanism of 3D capacitors embedded in TSVs based on our recent measurement results.⁹⁾ Understanding of these conduction mechanisms is essential in material and process selection of 3D embedded capacitor to optimize the design for manufacturing yield and long-term reliability.

Fig. 1. (Color online) Illustrations of integrated capacitors and TSVs: (a) stand-alone MIM trench capacitors with TSVs and (b) 3D embedded capacitors with TSVs.

Two sets of test vehicles with different layer stacks were designed and fabricated: (1) 400 nm sputtered TiN/30 nm ALD Al_2O_3 /400 nm sputtered TiN, and (2) 50 nm ALD TiN/10 nm ALD Al_2O_3 /50 nm ALD TiN. The fabrication flow is similar to our early report in Ref. 6. The first set of test vehicles are addressed as “sputtering samples”, and the second set of test vehicles are addressed as “ALD samples”. For sputtering samples, their electrodes were designed to be much thicker than those of ALD samples (i.e. 400 vs 50 nm) because the sputtering process can only provide limited step coverage of the electrode layers. To ensure uniform film deposition on rough sputtered bottom electrodes, the thickness of Al_2O_3 layers in sputtering samples was also set to be higher than that in ALD samples (i.e. 30 vs. 10 nm). In this experiment, each set of test vehicles also contains three structures for comparison: (1) planar capacitors as de-embedded structures, (2) 3D embedded capacitors with rough sidewalls (290 nm scallops), (3) 3D embedded capacitors with smooth sidewalls (30 nm scallops). Thus, the combination of layer stack and structure variations results in six types of test vehicles: sputtering-planar, sputtering-rough, sputtering-smooth, ALD-planar, ALD-rough, and ALD-smooth.

An ALD-rough sample was cross-sectioned and examined under scanning electron microscope (SEM) and transmission electron microscopy (TEM) for physical integrity.

Figure 2(a) shows the cross-sectional SEM image of 3D capacitor embedded in a trench of TSV, and TiN/Al₂O₃/TiN layers can be differentiated in a TEM image of Fig. 2(b). Their thicknesses were measured to be 57.0, 10.8, and 51.9 nm, respectively, which were close to the intended design parameters mentioned above.

Fig. 2. (Color online) SEM and TEM cross-sectional images of a 3D capacitor embedded in a trench of TSV.

Subsequently, electrical characterizations were conducted with Keithley 4200SCS semiconductor characterization system to obtain the current density-electric field (J - E) results for both sputtering and ALD samples. For sputtering samples, Fig. 3(a) shows a major overlap between the leakage current density of the sputtering-rough sample and that of the sputtering-smooth sample, both of which are higher than that of the sputtering-planar sample (e.g., 1.1×10^{-6} vs 3.6×10^{-8} A/cm² at a field of 4 MV/cm). As for ALD samples, Fig. 3(b) shows a major overlap between the leakage current densities of the ALD-planar, the ALD-rough, and the ALD-smooth samples. These observations suggest: (1) the sputtered electrodes have a negative effect on the leakage current density of the test vehicles with the trench structures, but it is not the case for the ALD electrodes, and (2) the effect of sidewall roughness is negligible on the leakage current density for both sputtering and ALD samples. Therefore, the dielectric degradation of the sputtering-rough and the sputtering-smooth samples is unlikely due to the thinning of dielectric layers deposited on the vertical trench sidewalls, which was conceived previously as the root cause for trench capacitors.⁸⁾ Additionally, Al₂O₃ layers in ALD samples also show a higher breakdown field than those in sputtering samples (~ 9.5 vs ~ 8.0 MV/cm). It demonstrates that despite their thinner dielectric layers (10 vs 30 nm), ALD samples can withstand a higher electric field than sputtering samples.

Fig. 3. (Color online) J - E plots of (a) sputtering samples. (b) ALD samples.

More physical insights can be obtained from the analysis of leakage current conduction mechanisms for 3D embedded capacitors. It was made based on the conduction models reviewed in Ref. 10, including both electrode-limited and bulk-limited conduction mechanisms.¹¹⁻¹⁵⁾ Firstly, Schottky Emission is fitted as shown in Figs. 4(a) and 4(b) for sputtering and ALD samples, respectively. Optical dielectric constants greater than 100 were extracted for sputtering samples, which is too high compared with the value of 3.1 reported in literature.¹⁶⁾ Nevertheless, reasonable physical parameters are extracted from ALD samples: 2.16 as optical dielectric constant and 2.12 eV as Schottky barrier height, respectively. Thus, Schottky emission is identified in the low bias region for ALD samples. Secondly, Fowler-Nordheim (FN) tunneling is fitted as shown in Figs. 5(a) and 5(b) for sputtering and ALD samples, respectively. Both sputtering and ALD samples show good linear fitting, and the extracted barrier heights ranging from 1.66 to 2.21 eV are consistent with the values from Schottky emission analysis. Therefore, FN tunneling can be identified for all samples in the high bias region, while an energy barrier is confirmed at TiN/Al₂O₃ interface with a height of ~ 2.0 eV. Thirdly, Poole-Frenkel (PF) emission is fitted as shown in Figs. 6(a) and 6(b) for sputtering and ALD samples, respectively. PF emission can be identified in the middle bias region because the extracted optical dielectric constants range from 1.98 to 3.69, which are close to the reported value of 3.1.¹⁶⁾ Lastly, hopping conduction is fitted as shown in Figs. 7(a) and 7(b) for sputtering and ALD samples, respectively. However, this conduction mechanism can only be identified for ALD samples, because the evaluated mean hopping distance is much smaller than the reported value by an order of magnitude for sputtering samples.¹⁶⁾

Fig. 4. (Color online) Schottky emission fitting of (a) sputtering samples and (b) ALD samples.

Fig. 5. (Color online) FN tunneling fitting of (a) sputtering samples and (b) ALD samples.

Fig. 6. (Color online) PF emission fitting of (a) sputtering samples and (b) ALD samples.

samples.

Fig. 7. (Color online) Hopping conduction fitting of (a) sputtering samples and (b) ALD samples.

All the analytical results of conduction mechanism have been summarized in Table I for comparison with bias conditions and extracted physical parameters. One observation is that the onset points of FN tunneling are consistent for all samples, implying relatively uniform thickness of the dielectric layers. It confirms that the leakage current degradation of the sputtering-rough and the sputtering-smooth samples is not due to the thinning of the dielectric layers deposited on the vertical sidewalls. It is also worth noting that PF emission is observed at a lower field for the sputtering-rough and the sputtering-smooth samples than the sputtering-planar one. It suggests that the sputtered electrodes cause more traps in the dielectric layers on the trench sidewalls than in the planar dielectric layers. Therefore, the higher leakage current density is attributed to the sputtering process. Since the ALD-rough and the ALD-smooth samples do not suffer from leakage current density degradation, ALD process is preferred over sputtering process as an electrode deposition method during the fabrication of 3D embedded capacitors.

Table I. Summary of the analysis of leakage current conduction mechanisms.

Sample		Schottky emission	FN tunneling	PF emission	Hopping conduction
400 nm TiN 30 nm Al ₂ O ₃ 400 nm TiN	Planar		[4.1,7.2] MV/cm $\Phi_B=2.1$ V	[3.7,5.2] MV/cm $\epsilon_r=1.98$	
	Rough		[3.9,6.5] MV/cm $\Phi_B=1.66$ V	[3.2,5.4] MV/cm $\epsilon_r=3.59$	
	Smooth		[4.0,6.7] MV/cm $\Phi_B=1.66$ V	[3.0,5.3] MV/cm $\epsilon_r=3.69$	
50 nm TiN 10 nm Al ₂ O ₃ 50 nm TiN	Same	[0,1.2] MV/cm $\Phi_B=2.12$ V $\epsilon_r=2.16$	[4.1,7.2] MV/cm $\Phi_B=2.21$ V	[3.7,5.2] MV/cm $\epsilon_r=2.22$	[0,1.2] MV/cm a=1.71 nm

To conclude, two sets of 3D embedded capacitor test vehicles have been successfully fabricated, characterized and analyzed to study their leakage current conduction mechanisms in this work. For sputtering samples, FN tunneling and PF emission have been identified from mid to high bias regions. For ALD samples, Schottky emission, hopping conduction, PF emission and FN tunneling have been identified from low to high bias regions. Physical parameters extracted from curve fittings are found to be self-consistent: (1) optical dielectric constant ranging from 1.98 to 3.69, and (2) Schottky barrier height ranging from 1.66 to 2.21 eV. The higher leakage current density found in sputtering samples with trench structures is attributed to more traps, caused by sputtered electrodes, in the dielectric layers on the vertical sidewalls than those in the planar dielectric layers. It has been confirmed by the early onsets of PF emission. Therefore, in terms of leakage current density, the ALD process is preferred over the sputtering process as an electrode deposition method for 3D embedded capacitors.

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