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Characterization of SiC Power Devices for Dual-active Bridge Converter

Yeo Howe Li, Venkata Ravi Kishore Kanamarlapudi
Autonomous Vehicles and Electro-mobility (AVEM) group,
Energy Research Institute at Nanyang Technological University (ERIAN),
Singapore
Email: hlyeo@ntu.edu.sg

Abstract— Double pulse testers are required for extraction of switching energies and waveforms of power devices. With the increasing adoption of wide bandgap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) comes an increasing need for the creation of double pulse testers and associated procedures capable of testing fast switching speeds. To date, many papers involving double pulse test setups have been published. However, these papers tend to focus on the results of the characterisation rather than the technical aspects of the experimental setup itself. In this paper, the characterisation procedure and practical considerations of a double pulse tester are presented in detail. Practical considerations involving the testing of fast switches like SiC MOSFETs are also reviewed and highlighted.

Keywords—Double pulse tester, silicon carbide schottky diode, silicon carbide MOSFET, dual-active bridge converter

I. INTRODUCTION

Nowadays, there is an increasing need for more efficient, faster-switching power devices. This need is being driven by a need for efficient converters with higher power densities in various applications such as grid-tied applications [1-2], traction applications [3-5] and aerospace applications.

Wide bandgap power devices realised from GaN and SiC are able to exhibit low switching times [6] and low switching losses [7-12]. However, their high cost compared with presently existing silicon technology requires designers to assess whether or not the gain in power density and efficiency is worth the increased cost of the switches.

Device characterization, often involving double pulse tests, is necessary in order to assess this tradeoff. To date, many authors [13-16] have published work with regards to characterisation of wide bandgap semiconductors however few [17-20] highlight the practical considerations required for accurate testing of these switches at such short switching times.

In this paper, the technical considerations, equipment and work procedure required for extraction of switching energies with a double pulse tester are presented. A dual-active bridge (DAB) with a 3-level NPC leg on the primary side and a H-bridge on the secondary side as shown in Fig. 1 is chosen as an example of a power converter which uses the characterized switches.

The devices used for characterization are C2M0045170D and C3D10170H. For protection purposes, the MOSFETs for both high and low sides were overrated. Hence the C2M0045170D was selected for both sides. The C3D10170H SiC schottky diode was selected as the clamping diode for the NPC leg to minimise reverse recovery losses.

Fig. 1. Dual-active bridge converter with input and output voltage ratings

II. OVERALL PROCEDURE

The overall procedure for extraction is presented in Fig. 2. Switching conditions are first identified by considering the relevant current and voltage waveforms of the converter while it operates in steady-state. This can be done by simulation and in this paper, the converter is outputting 6 kW and operates at a switching frequency of 100 kHz. The switching waveforms for one period is presented in Fig. 3, where the top two waveforms are primary side voltage, V_p , and primary side current, I_p , of the high frequency transformer and the bottom two graphs are the secondary side voltage, V_s , and current, I_s , respectively.

Fig. 2. Overall procedure for switching energies extraction

Fig. 3. Steady-state waveforms of high frequency transformer

After identifying the voltage and currents imposed across the switches at the various points of switching, the switching energies can be extracted using a double pulse tester under a variety of test conditions. These switching energies can be used to create a lookup table that is then inputted into the simulation to calculate the switching loss of the converter while it is in operation.

III. PRACTICAL CONSIDERATIONS FOR DOUBLE PULSE TESTER

In this section, the dependent and independent variables associated with the double pulse test are identified. The hardware required for testing is also elaborated upon in parts and the model numbers of various parts are given at the end of this section.

A. Dependent and Independent Variables

The various dependent variables of the double pulse test are as follows:

- Switching energies
- di/dt and dv/dt
- Gate charge
- Current and voltage waveforms

The independent variables that control them are as follows:

- Voltage across drain-to-source or collector-to-emitter terminals
- Current through drain-to-source or collector-to-emitter terminals
- Junction temperature of switch

- Positive and negative rail voltages of gate driver
- Turn-on and turn-off gate resistances
- Gate drivers
- Commutating switch
- Circuit layout

It is important to record down these variables when using or referencing switching energy data. In cases where the experimenter intends to examine the effect of different circuit layouts on switching behavior, the commutation and gate driver loop inductances for each layout should be noted as well.

B. Double pulse test module

Fig. 4. Double pulse tester configuration for testing active devices

The double pulse test module may be configured to test either active switches or power diodes. In Fig. 4, the schematic of a typical double pulse tester is depicted. This configuration is used to test active transistors. The double pulse tester may be reconfigured into the configuration shown in Fig. 5. It is used for characterization of diodes.

Fig. 5. Double pulse tester configuration for diode characterization

The commutation and gate driver loop inductances for any double pulse tester module should be designed to be as small as reasonably possible in order to ensure that the switches can be tested at higher switching speeds. Reduction of commutation inductance has been highlighted in various papers [7], [15]. Excessive parasitic inductance in either loop can lead to ringing and overvoltages that destroy the device. In this paper, a commercial evaluation board as shown in Fig. 6 was chosen to serve as the double pulse tester module. This module is meant for testing TO-247 packages and has not been optimised for reduced parasitic inductances. It will be replaced with a more optimal module in future works.

Fig. 6. Double pulse test layout depicting commutation loop (red) and gate driver loop (yellow)

In this paper, the partial inductances of the printed circuit board (PCB) tracks of the commutation and gate driver loops are approximated using (1) and (2). These equations are for calculating the inductance of a rectangular coil where N stands for number of turns, W stands for width of the coil, H stands for height of the coil, d stands for diameter of the coil's wire and μ_R stands for the relative permeability of the core enclosed by

the coil. In the test setup, d has been approximated as 1 mm, N and μ_R are taken as 1.

$$L = \frac{\mu_0 \mu_R}{\pi} [-2(w + h) + 2\sqrt{h^2 + w^2} + k] \quad (1)$$

$$k = -h \ln \left(\frac{h + \sqrt{h^2 + w^2}}{w} \right) - w \ln \left(\frac{w + \sqrt{h^2 + w^2}}{h} \right) + h \ln \left(\frac{4h}{d} \right) + w \ln \left(\frac{4w}{d} \right) \quad (2)$$

In order to approximate the parasitic inductance of both loops, the partial inductance of the switches involved in both the gate driver loop and the commutation loop must be considered and added to the partial inductance of the PCB tracks. In order to approximate these inductances for the case of a TO-247 package, the LT-SPICE netlist of C2M0045170D SiC MOSFET is examined and values of inductances in the netlist model are used. In Table I, the values of N , W , H , d and μ_R are noted in addition to the values corresponding to the partial inductances of the PCB tracks and switches in the gate driver and commutation loops.

TABLE I. PARASITIC INDUCTANCE CONSIDERATIONS

Loop	Rectangular loop parameters		Inductances (nH)		
	$W(\text{mm})$	$H(\text{mm})$	PCB	Switch(es)	Total
Gate driver	17	10	26.5	24	50.5
Commutation	29	26	72	30	102

C. Oscilloscope measurement system

The oscilloscope measurement system consists of one low voltage probe for measuring the gate signal, one high voltage differential probe for measuring the drain-to-source or collector-to-emitter voltage, one current shunt for measuring the drain-to-source or collector-to-emitter current and the oscilloscope itself. The trigger signal may be inputted into the remaining channel of the oscilloscope.

For each quantity to be measured, a measurement chain consisting of measurement elements is required. For each measurement chain used to measure either voltage or current, the total rise time must be low enough such that the error in measured switching time is minimised. The bandwidth BW , of an instrument such as a low voltage probe is related to its rise time t_r , according to (3).

$$t_r = \frac{0.35}{BW} \quad (3)$$

Assuming that the measurement chain consists of n elements, then the measured switching time t_m , and the actual switching time t_{sw} , are related by (4) where t_{rn} represents the rise time of the n^{th} element in the chain. It can be seen from (3) and (4) that it is desirable to have instruments with high bandwidth so as to minimise the error in between the measured and actual switching times.

$$t_m = \sqrt{t_{sw}^2 + t_{r1}^2 + t_{r2}^2 + \dots + t_{rn}^2} \quad (4)$$

In this paper, the rise time of the instruments involved have been noted in Table II. The system rise time, t_{sys} , corresponding to the measurement chains for the gate-source voltage V_{gs} , drain-source voltage V_{ds} , and drain-source current I_{ds} have been recorded. t_{sys} is calculated using (5).

$$t_{sys} = \sqrt{t_{r1}^2 + t_{r2}^2 + \dots + t_{rn}^2} \quad (5)$$

TABLE II. RISE TIMES

Equipment	Measurement chain rise times(ns)		
	V_{gs}	V_{ds}	I_{ds}
500MHz oscilloscope	0.7	0.7	0.7
500MHz passive probe	0.7	-	-
120MHz differential probe	-	2.9	-
2GHz current shunt	-	-	0.2
t_{sys}	1.0	3.0	0.7

For SiC MOSFETs, the switching times have been estimated in datasheets [21] to be as low as 9ns. This translates to a rise time error in the V_{ds} waveform of about 5 percent according to (4). This translates to an increase in measured switching energy of about 5 percent.

Fig. 7. Thermal measurement of switches on hot plate

D. Temperature control

In general, implementation of temperature control while simultaneously ensuring low commutation inductance in the double pulse tester is difficult as conventional hot plates are large and may force the designer to adopt unoptimal circuit layouts in order to accommodate the hot plate. In this paper, temperature control is implemented using a UC150 hot plate as seen in Fig 7.

E. Safety system

As high dc voltages are present, it is important that sufficient safety precautions are taken to protect the experimenter and are outlined as follows:

- Enclosure with safety interlock relays that sense when the doors are closed or open
- A single-pole double-throw (SPDT) switch used in conjunction with resistors and the door interlock relays to disconnect the supply and discharge the capacitor bank when the door is open.
- Remote control of the double pulse test module, oscilloscope and high voltage dc supply during test. It is done through the use of fibre optic cables, Ethernet and RS232 communication

Of particular importance is the SPDT switch, which is used to discharge the capacitor bank. As the capacitor bank can possess large capacitance values as high as 2mF and has a voltage rating of 1500V, it is important that it has to be discharged before the experimenter touches it. The SPDT switch may be implemented with two relay-controlled circuit breakers as shown in Fig. 8. Alternatively, the SPDT switch can be implemented using semiconductor switches.

Fig. 8. SPDT switch with discharge resistor R1

F. Pulse generator

The pulse generator is an field programmable gate array (FPGA) with a signal for controlling switching of power transistors (Sig[1]) and another signal for triggering the oscilloscope (Sig[0]) as shown in Fig. 9. Turn-off energy is measured at the rising edge of the trigger signal whilst turn-on energy is measured at the falling edge of the signal. In Fig. 8, the time quantities t_1 , t_2 , t_3 and t_4 are adusted by controlling the number of clock cycles in each state.

The pulse generation is implemented using the moore state machine depicted in Fig. 10 and the duration of the various pulses is adjusted by the number of clock cycles that it in each state. The number of clock cycles corresponding to each state is given by t_{1_cycles} , t_{2_cycles} , t_{3_cycles} and t_{4_cycles} respectively. t_{count} is the number of clock cycles that have elapsed.

Fig. 9. Gate signal (Sig[1]) and trigger signal (Sig[0])

Fig. 10. Moore state machine

In Fig. 11, the double pulse tester experimental setup is presented along with its salient parts. In Table III, the list of equipment the setup are detailed.

Fig. 11. Double pulse tester experimental setup

TABLE III. EQUIPMENT MODELS

Equipment category	Equipment model(s)
Measurement	HDO6054 oscilloscope 2 PP018 passive voltage probes HVD3106 differential voltage probe SDN-414 current shunt
Double pulse test circuit	KIT8020-CRD-8FF1217P-1 0.59 mH air-core inductor (custom-wound) 12 MAL209639152E3 0.5mF capacitors
Safety system	2 NM12VZA-M interlock relays HFBR-RNS010Z fibre optic cable AFBR-1624Z fibre optic transmitter AFBR-2624Z fibre optic receiver Enclosure
Pulse generator	DE0-Nano FPGA kit based on EP4CE22F17C6N
Power supplies	XR10000-0.8/415 Magna power supply GPD-3303S benchtop power supply

IV. POST-PROCESSING

It is important to be able to save and refer to the measured data. It is also important to implement deskewing to compensate for the delay in between the current shunt and high voltage probe. In this section, the principles behind the deskewing are presented for the cases of transistor turn-on, transistor turn-off, diode turn-on and diode turn-off. In the following sections, the post-processing of results obtained under the conditions specified in Table IV are presented. It should be noted that for testing of the C3D10170H diode, the gate driver parameters are related to gate driver of the commutating switch.

TABLE IV. TEST CONDITIONS

Parameters	Primary side MOSFET	Primary side diode	Secondary side MOSFET
Device under test	C2M0045170D	C3D10170H	C2M0045170D
Positive rail voltage	20V	20V	20V
Negative rail voltage	-5V	-5V	-5V
Turn-on gate resistance	73Ω	73Ω	73Ω
Turn-off gate resistance	5Ω	5Ω	5Ω
Gate driver	ACPL-W346	ACPL-W346	ACPL-W346
Commutating switch	C3D10170H	C2M0045170D	C2M0045170D
Circuit layout	KIT8020-CRD-8FF1217P-1	KIT8020-CRD-8FF1217P-1	KIT8020-CRD-8FF1217P-1
Drain-source voltage	730V	730V	400V
Drain-source current	10A - 20A in increments of 2A	10A - 20A in increments of 2A	20A - 30A in increments of 2A
Junction temperature	25°C, 90°C	25°C, 90°C	25°C, 90°C

A. Transistor turn-on

During the initial current rise of the turn-on period, an initial voltage drop is observed in V_{ds} . This voltage drop is caused by the current shunt resistance, R_{sh} , as well as the commutation inductance, L_{COM} . L_{COM} is approximated in section 3B to be 102nH. The value approximated from the alignment results is 100nH. Hence, I_{ds} and V_{ds} may be aligned using V_{align} which has been defined in (6). V_{DC} refers to the applied dc voltage at turn-on.

$$V_{align} = V_{DC} - L_{COM} \frac{dI_{ds}}{dt} - I_{ds}R_{sh} \quad (6)$$

In Fig. 12, V_{align} is superimposed over V_{ds} in order to ensure alignment. As observed by Fig. 12, voltage dip in V_{align} overlays with the initial voltage dip in V_{ds} . A similar method is also employed in [16] and by other authors. If needed, L_{COM} can be scaled until the required voltage dip is achieved.

Fig. 12. Alignment of waveforms – V_{align} (pink, 100V/div), V_{ds} (blue, 100V/div), I_{ds} (green, 5A/div), V_{gs} (red, 5V/div)

B. Transistor turn-off

(6) can also be used for aligning the voltage waveforms for transistor turn off as depicted in Fig. 13.

Fig. 13. Alignment of waveforms – V_{align} (pink, 100V/div), V_{ds} (blue, 100V/div), I_{ds} (green, 5A/div), V_{gs} (red, 5V/div)

C. Diode turn-on

During diode turn-on, the cathode-to-anode capacitance of the diode is being discharged. Hence, during the turn-on period, the diode can be treated as a capacitance and a current, I_{align} , as defined by (7) which can be used for aligning the voltage and current waveforms. In (7), C_{ak} is the capacitance of the anode-to-cathode capacitance of the switch and V_{ak} is the anode-to-cathode voltage of the switch. I_{align} can then be

superimposed onto the anode-to-cathode current, I_{ak} , such that the two align during the discharge period as observed in Fig. 14.

$$I_{align} = C_{ak} \frac{dV_{ak}}{dt} \quad (7)$$

Fig. 14. Alignment of waveforms – I_{align} (pink, 5A/div), V_{ak} (blue, 100V/div), I_{ak} (green, 5A/div)

D. Diode turn-off

During diode turn-off, the diode experiences reverse recovery losses. (6) is slightly modified to yield (8) which describes $V_{align,d}$. This is aligned with the voltage oscillations seen in V_{ak} as observed in Fig. 15 to ensure proper deskewing.

$$V_{align,d} = -V_{DC} - L_{COM} \frac{dI_{ak}}{dt} - I_{ak}R_{sh} \quad (8)$$

Fig. 15. Alignment of waveforms – I_{align} (pink, 5A/div), V_{ak} (blue, 100V/div), I_{ak} (green, 5A/div)

V. RESULTS

The turn-on and turn-off energies for C2M0045170D and C3D10170H are extracted. The C2M0045170D and C3D10170H are used for the NPC leg of the primary side as depicted in Fig. 1. On this side, it is expected that T1 and T2! will experience hard turn-on and hard turn-off and that these switches will commute with Dc-h and Dc-l respectively. On the secondary side, C2M0045170D switches are used. Switches on this side are expected to achieve zero-voltage switching (ZVS). Hence, only the turn-off energies are extracted and the stored output capacitance energy must be subtracted from these energies in order to reflect soft-switching. The extracted switching energy values for the cases of a junction temperature of 25°C and 90°C are used to create the lookup tables. As the pulses in the experiments are typically

less than 1ms, it is assumed that the self-heating of the switches during the pulse duration is negligible and that the temperature throughout the switch is uniform. Under such conditions, the junction temperature T_j , is assumed to be the same as the case temperature. In Tables V to VII, the switching energies are given. It should be noted that for the C2M0045170D, a large turn-on gate resistance of 73 ohm is used to suppress the ringing in the turn-on waveforms.

TABLE V. SWITCHING ENERGIES OF C2M0045170D AT 730V

Energy	T_j	Current					
		10A	12A	14A	16A	18A	20A
Turn-on (mJ)	25°C	0.85	1.00	1.15	1.30	1.47	1.64
	90°C	0.82	0.95	1.10	1.24	1.39	1.54
Turn-off (mJ)	25°C	0.22	0.23	0.24	0.25	0.26	0.27
	90°C	0.25	0.26	0.26	0.27	0.28	0.30

TABLE VI. SWITCHING ENERGIES OF C3D10170H AT 730V

Energy	T_j	Current					
		10A	12A	14A	16A	18A	20A
Turn-on (mJ)	25°C	-0.12	-0.13	-0.13	-0.13	-0.13	-0.13
	90°C	-0.13	-0.13	-0.12	-0.12	-0.12	-0.12
Turn-off (mJ)	25°C	0.16	0.15	0.16	0.17	0.17	0.17
	90°C	0.14	0.14	0.13	0.14	0.13	0.13

TABLE VII. SWITCHING ENERGIES OF C2M0045170D AT 400V

Energy	T_j	Current					
		20A	22A	24A	26A	28A	30A
Turn-off (μJ)	25°C	119	129	138	150	167	181
	90°C	118	127	139	152	170	193

From Table V results it can be observed there is a general trend that turn-on energy decreases with increase in temperature and turn-off energy increases with increase in temperature. One of the possible reasons for that could be the threshold voltage of SiC MOSFETs which is decreases with increase in junction temperature as observed in datasheets [21]. The decreased threshold voltage pulls down the miller-plateau voltage which opposes gate driver voltage during turn-on and turn-off. A reduced miller voltage means a higher gate current can enter the gate during the miller period of turn-on, leading to faster switching and reduced turn-on energy. A reduced miller voltage also results in a lower gate current leaving the gate during the miller period of turn-off, leading to slower switching and an increased turn-off energy.

From Table VI results, the turn-on energies of the diode are negative. This is because the device's junction capacitor is discharging during turn-on. This energy is not expected to vary as much as device's junction capacitance is a weak function of temperature. During turn-off, reverse recovery of the diode occurs and the device's junction capacitor is recharged. Hence, it is expected that the magnitude of turn-off energy exceeds that of turn-on energy as the former is inclusive of the energy of the device's junction capacitor and any resistive losses that occur during switching. It should also be noted that at higher junction temperatures, the turn-off energy of the switch

increases. This is because the commutating MOSFET is switching slower due to reduced miller plateau voltage.

The switching energies are compiled into a lookup table which is then inputted into PLECS. Devices on both the primary side and secondary side were assumed to be forced cooled with separate cooling systems each with a thermal resistance of 0.5K/W. The switching loss breakdown for the converter operating at 100 kHz switching frequency and 6 kW output is shown in Table VIII.

TABLE VIII. SWITCHING LOSS BREAKDOWN OF DAB CONVERTER

Switching loss component	Loss/W
C2M0045170D MOSFETs on primary side	231.7
C3D10170H diodes	5.0
C2M0045170D MOSFETs on secondary side	59.3
Total:	296

CONCLUSION

In this paper, the practical considerations for device characterization have been presented and SiC devices have been characterized for a dual-active bridge converter. The results of the characterization have been discussed and the switching loss breakdown of the converter have been presented.

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