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Practical Guidelines for Device Characterization and Power Converter Design involving SiC MOSFETs

Howe Li Yeo

*Autonomous Vehicle and Electro-mobility group
Energy Research Institute @ NTU
Singapore
hlyeo@ntu.edu.sg*

Venkata Ravi Kishore Kanamarlapudi

*Autonomous Vehicle and Electro-mobility group
Energy Research Institute @ NTU
Singapore
kanamarlapudi@ntu.edu.sg*

Abstract—SiC MOSFETs offer significant advantages over Si IGBTs in terms of power density and efficiency for power converter design. However, their fast switching speeds and limited short circuit current capability lead to issues during device characterization and converter design. In this paper, guidelines for overcoming the practical issues of characterizing and designing with SiC MOSFETs are presented. A double pulse test setup and a SiC-based dual-active bridge are developed by incorporating the guidelines. Experimental results are obtained where applicable to illustrate the benefits of these guidelines.

Index Terms—SiC MOSFETs, Gate drivers, Double pulse test

I. INTRODUCTION

The rate of adoption of SiC devices for commercial applications has been steadily increasing. This technology has been considered for potential use in transport [1]–[3], renewable energy [4], [5] and solid-state transformers [6], [7]. The interest in SiC MOSFETs is brought about by the improved power density and efficiency they offer over Si IGBTs for converter design. However, adopting SiC MOSFETs poses several challenges in converter design.

First of all, their fast switching speeds lead to oscillations in voltage or current that can potentially destroy or degrade device performance and hence ways of modelling and suppressing these oscillations have been investigated by various authors [8], [9]. Authors have also investigated and proposed ways of mitigating issues like crosstalk [10], [11] and electromagnetic compatibility (EMC) [12], [13] which arise as a result of fast switching speed.

Secondly, their short circuit current capability is lower than that of Si IGBTs [14], [15]. This has raised concerns over their robustness and necessitates the use of short-circuit protection.

Thirdly, it is presently difficult to predict the lifetime of SiC MOSFETs due to the phenomenon of threshold voltage shift [16]. Authors have looked into ways of power cycling SiC devices [17], [18] and this is still on-going. This makes it difficult to use them for applications that are expected to last several decades.

These challenges have implications on the design of SiC-based power converters as well as the device characterization procedure for SiC MOSFETs. In this paper, these implications

are discussed in detail and guidelines for overcoming practical issues in these areas are put forth. A double pulse test setup and a SiC-based dual-active bridge are developed and experimental results are obtained to better illustrate the benefits of using the proposed guidelines where possible.

II. DEVICE CHARACTERIZATION

One of the key instruments required for device characterization is the double pulse tester. It is used for measuring the switching energies of power devices. The results can be used to select the right power devices and to tune the gate drive so that the switching energies can be reduced without compromising the reliability of the switch. In this section, general guidelines are provided for the selection of measuring equipment. Further details regarding implementation are mentioned in [19], [20]. The effect of various independent variables on switching energy, overshoot, $\frac{di}{dt}$ and $\frac{dv}{dt}$ are also examined in detail.

The choice of oscilloscope and voltage probes can impact rise and fall times of voltage and current measurement. This consequently impacts the switching energy. Of particular importance is the bandwidth of the measurement system. This fact has been highlighted by various authors [20]–[22]. A typical measurement system is depicted in Fig. 1, consists of the oscilloscope as well as probes for of current and voltage measurement. The probe and oscilloscope channel for each quantity measured form a measurement chain. The bandwidth of individual components in each measurement chain influences the observed rise and fall times on the oscilloscope. In general, a higher bandwidth is recommended for observing the switch transition times of wide band-gap semiconductors. However, measurement systems with higher bandwidth cost more. Hence it is important to assess the required bandwidth before setting up the double pulse tester.

The bandwidth, BW , is related to the instruments rise time, t_r , according to (1).

$$t_r = \frac{0.35}{BW} \quad (1)$$

The measured rise time of the voltage or current, t_m , is related to the rise times of the components in the measurement chain according to (2) where $t_{v,i}$ represents the actual rise time of the measured voltage or current, t_p represents the

Fig. 1. Typical measurement system with measurement chains

rise time of the probe and t_{osc} represents the rise time of the oscilloscope. It can be seen from (2) that the rise times of the probe and oscilloscope incur an error in between the measured rise time and the actual rise time. For accurate measurements, it is recommended that the values of t_p and t_{osc} be selected such that $t_m \leq 1.05 \cdot t_{v,i}$.

$$t_m = \sqrt{t_{v,i}^2 + t_p^2 + t_{osc}^2} \quad (2)$$

In order to ensure that the correct equipment is selected, the rise and fall time of voltage and current must be considered. The rise time and fall time of the currents can be read from datasheets and are dependent on maximum ratings of the device and the conditions under which it is switched. The rise times and fall times are defined as the times taken for the current to rise from 10 percent to 90 percent of its final value and fall from 90 percent to 10 percent of its final value respectively based on IEC 60747-9 [23]. These times vary from about 15ns for the case of smaller devices to about 70ns for the case of large modules. Voltage rise and fall times are not stated in datasheets and hence must be approximated. This can be done through simulation but in cases where simulation models are not available, a simple way will be to multiply the current rise and fall times by 2. Based on the Table I, the required bandwidths of measuring equipment can be approximated and consequently, suitable equipment can be selected for measurement as shown in Table II.

In addition to the bandwidth requirement, there is a requirement on recommended driving voltages. The recommended driving voltages of various devices vary widely between manufacturers as seen in Table III. Hence, when constructing a double pulse test setup for testing various SiC devices, a gate driver with variable positive and negative rail voltage is required. An example of such a driver was presented in [24].

In order to mitigate the voltage overshoots at the drain and the gate during tests, it is important to minimise the parasitic inductances of the gate driver and commutation loops depicted in Fig. 2. For the case of the commutation loop, the voltage overshoot is affected by the commutation inductance and rate of change of current through the D.U.T. according to (3). The drain-to-source voltage, V_{ds} , across the device

TABLE I
RISE TIMES AND FALL TIMES OF SWITCHES AS SEEN IN DATASHEETS

Voltage rating	Device	Current rating (A)	T_{rise} (ns)	V_{fall} (ns)	T_{fall} (ns)	V_{rise} (ns)
1200V	IMZ120R045M1	52	18	36	13	26
	FF11MR12W1M1_B11	100	16.4	32.8	31	62
	WAS300M12BM2	300	68	136	43	86
1700V	C2M0080170P	40	9	18	18	36
	C2M0045170P	72	13	26	10	20
	CAS300M17BM2	300	72	144	56	112

TABLE II
RECOMMENDED PROBES AND OSCILLOSCOPES BASED ON DEVICES

Device	Oscilloscope model	Voltage probe	Current probe
IMZ120R045M1	HDO9104 (1GHz)	HVP120 (400MHz)	SDN414 (2GHz)
FF11MR12W1M1_B11			
C2M0080170P			
C2M0045170P	Yokogawa DLM4038 (350MHz)	Yokogawa 701927 (150MHz)	Iwatsu S285A (30MHz)
CAS300M17BM2			
WAS300M12BM2			

TABLE III
DRIVING VOLTAGES OF VARIOUS DEVICES

Vendor	Devices	V_{gs-on} (V)	V_{gs-off} (V)
CREE	C2M0080170P	20	-5
	C2M0045170P		
Infineon	IMZ120R045M1	15	-5
	FF11MR12W1M1_B11		
Rohm	BSM180D12P2E002	18	0
	SCT3160KLHR

Fig. 2. Gate driver and commutation loops

during switching is described using (4) where V_k , V_R and V_{dc} represent cathode-to-anode voltage, current shunt resistor voltage and dc supply voltage respectively.

$$V_{com} = L_{com} \cdot \frac{di_{ds}}{dt} \quad (3)$$

$$V_{ds} = V_{dc} - L_{com} \cdot \frac{di_{ds}}{dt} - V_k - V_R \quad (4)$$

For the case of the gate driver loop, the gate resistance, R_g , parasitic inductance, L_g and input capacitance, C_{iss} form an LCR circuit and the characteristic equation is given by (5). Damping factor, ζ , is given by (6).

$$\frac{d^2 i_g}{dt^2} + \frac{R_g}{L_g} \cdot \frac{di_g}{dt} + \frac{i_g}{L_g C_{iss}} = 0 \quad (5)$$

$$\zeta = \frac{R_g}{2L_g} \quad (6)$$

In order to minimise overvoltages at the gate, the damping factor must be increased to reduce the ringing. Ideally, a critically damped response is desired but in practice, there may be variations in L_g due to manufacturing tolerances in the conductor geometry. Hence, it is advisable to target an overdamped response by setting $\zeta = 1.2$. It can be seen from (6) that there exists two ways to increase damping factor. The first is through increasing R_g which is not desirable as it slows down switching speed. The second is through reduction of L_g which is preferable.

In order to reduce L_{com} and L_g , it is important to assess the paths of the currents in order to find the area enclosed by the current loops. This area should be reduced as much as possible in order to ensure low values of parasitic inductance. Current loops may be characterised into two broad categories, vertical loops, where cross-sectional area of the loop is a plane perpendicular to the conducting planes containing the forward and return currents, and lateral loops, where the cross-sectional area of the loop is parallel to the plane containing the forward and return paths. Examples of commutation loop realised using both types of loops can be seen in Fig. 3 and Fig. 4. It is possible to design a vertical loop with extremely low parasitic inductance provided if the distance between the plane containing the forward path and the plane containing the return path is sufficiently small. This was demonstrated in [25] through the design of an optimal power loop which used an inner layer of copper as its return path. However, in practice, it may not always be possible to adopt such an optimal loop due to various constraints such as device packaging, part placement and the number of available conducting layers. Hence it is important for designers to understand the how geometrical parameters affect L_{com} and L_g so that these parasitic inductances can be quickly estimated for an initial design.

If the dimensions of the loop are known, the parasitic inductance can be approximated with basic formulae. For the case of vertical loops, (7) is used for approximation.

Fig. 3. Vertical loop

Fig. 4. Lateral loop

As suggested by the equation, the vertical loops parasitic inductance, L_v , is influenced by thickness of printed circuit boards (PCBs) dielectric, t , length of the forward or return current path, l , and conductor width w seen by the current path. The product of t and l is the area enclosed. It can be seen from (7) that for the case of vertical loops, it is preferable to have short current paths, thin dielectric layers and wide trace widths for parasitic inductance minimization. In this work, a vertical loop was employed for the gate-drivers loop. The forward and return paths of the driver were presented in [24] and are presented here in Fig. 5 alongside the vertical loop. The driver is benchmarked against a commercial driver in [24] and found to yield significantly improved performance. The estimated partial inductance of the gate driver loop path in Fig. 5 is about 6.2nH.

$$L_v = \frac{\mu_0 t l}{w} \quad (7)$$

For the case of lateral loops, their geometry can generally be approximated by a rectangular loop as depicted in Fig. 4. The four sides of the rectangle can be thought of as two pairs of parallel wires. The lateral loop inductance, L_l , can therefore be approximated using (8) where s_1 and s_2 are the distances between two opposite sides in the rectangular loop, w_1 and w_2 are the widths of the conductor in the corresponding side of the rectangle and μ_0 is permeability of free space.

Fig. 5. Gate driver loop

$$L_l = \frac{\mu_0}{\pi} \left(s_2 \cosh^{-1} \frac{s_1}{w_1} + s_1 \cosh^{-1} \frac{s_2}{w_2} \right) \quad (8)$$

The estimated value of the commutation loop with and without the current shunt is presented in Table IV. A double pulse test is conducted to verify the commutation inductance of loop with the current shunt. The commutation inductance of the PCB is estimated using the math functions on current channel input of the oscilloscope. During the turn-off event, drain-to-source voltage, V_{ds} , can be described by (4). However, after the current across the device under test has fallen to close to zero, the diode in Fig. 2 can be considered as turned-on completely and hence V_k can be approximated as zero during this time. V_R may also be approximated as zero as the current is very low and the value of shunt resistance is low as well. Hence, during the time when device is almost turned-off, (4) may be approximated as (9). (9) can then be used to program a math function on the oscilloscope for alignment of overshoot. Des skew time between current and voltage may be adjusted for this alignment. The initial voltage spike and subsequent oscillations of the alignment function should align with V_{ds} as depicted in Fig. 7 if it is properly adjusted. After aligning the overshoot, the scaling parameter corresponding to L_{com} can be adjusted until the observed overshoot magnitude and the overshoot magnitude of the math function aligns as seen in Fig. 7.

$$V_{ds} = V_{dc} - L_{com} \cdot \frac{di_{ds}}{dt} \quad (9)$$

For the double pulse tester of this paper, the PCB layout is presented in Fig. 6, a jumper resistor pad was incorporated to bypass the coaxial shunt resistor in case the module needed to be used as a conventional half-bridge. The path of the commutation current with the jumper resistor by pass is depicted in Fig. 6 along with values of s_1 and s_2 . For w_1 and w_2 , the width of the narrowest part of the copper trace on the PCB was used. This value is 3mm and corresponds to the traces near the drains of the devices as they taper off slightly before the drains. It should be noted that the value approximated in (8) is expected to be an underestimate as the narrowest width along the path is used.

Fig. 6. Commutation loop in double pulse test module

Fig. 7. Verification of commutation inductance via oscilloscope measurement during double pulse test

It should be also noted that devices with kelvin source connections significantly reduce the parasitic inductance of the gate driver loop and should be adopted if possible to reduce switching losses. In Table V, the IMW120R045M1 device without kelvin connection is compared with IMZ120R045M1 device with kelvin connection to give a sense of the reduction in switching energy. Tests were conducted at a d.c. voltage of 750V. As seen in Table V, the turn-on energy, E_{on} , is significantly reduced by the presence of the kelvin connection but the turn-off energy, E_{off} , is not as significantly reduced. In order to account for this behaviour, Fig. 8 is considered. , the C_{oss} capacitance sees the channel resistance and hence the rate of discharge of this capacitance is solely influenced by the rate of reduction of channel resistance during turn on as depicted in

TABLE IV
RECOMMENDED PROBES AND OSCILLOSCOPES BASED ON DEVICES

	Inductance value (nH)
Commutation path without current shunt (estimated)	33
Current shunt	7
Commutation path with current shunt (estimated)	40
Commutation path with current shunt (measured)	35

TABLE V
COMPARISON OF SWITCHING ENERGIES WITH AND WITHOUT KELVIN
CONNECTION @ 750V

	Switch	Current							
		2A	4A	6A	8A	10A	12A	14A	16A
E_{on} (μJ)	IMW120R045M1	128	166	208	252	298	342	387	435
	IMZ120R045M1	126	152	181	209	243	272	302	334
E_{off} (μJ)	IMW120R045M1	58.4	65.3	67.2	72.4	74.9	76.1	82.1	90.1
	IMZ120R045M1	59.4	65.3	69.5	71.1	73.1	72.3	79.2	81.0

Fig. 8. Turn-on and turn-off of MOSFET

Fig. 8. The rate of reduction of channel resistance is influenced by how fast the gate voltage rises. However, during turn-off, the drain-to-source current, I_{ds} , goes through both the channel and the C_{oss} capacitance. Usually, the channel turns off quickly as V_{gs} decreases quickly. However, voltage does not rise immediately to final value as the C_{oss} capacitance takes time to charge. In short, turn-off energy is also strongly dependent on load current and a kelvin connection has limited effect on turn-off energy as it only speeds up turn off of channel but not charging of C_{oss} .

The switching behaviour of SiC MOSFETs is dependent on various independent variables presented in [24]. These variables are V_{ds} , I_{ds} , T_j , rail voltages of the driver, R_g , L_g , L_{com} and the complementary switch. For the most part, the influence of these variables on switching behavior is the same for both SiC MOSFETs and Si MOSFETs. Their effects are not discussed further in this paper as various application notes are available in literature.

Device lifetime is also of great concern for practitioners. The long-term wear and tear of power devices is primarily caused by the mismatch in between the coefficient of thermal expansion of the semiconductor die and any interfaces it is attached to such as the substrate or electrical contacts. Over time, the variations in temperature cause the semiconductor die and these interfaces to expand and contract at different rates and this eventually causes problems like delamination or bond-wire lift-off. Presently, device lifetime is characterised through the use of the power cycling method which is a form of highly accelerated stress test that accounts for this failure mechanism. In Fig. 9, the setup required for this method is depicted. A large power supply is required for supplying the high current needed to achieve the desired heating effect whilst a smaller supply is required to supply the measurement cur-

Fig. 9. Power cycling setup

rent required to measure the associated temperature sensitive electrical parameter (TSEP). A suitable cooling system for the device under test is also required to quickly cool it down to simulate periods of expansion and contraction. Power cycling has been used successfully on silicon IGBTs [26] and involves measuring the number of cycles, N_f , to failure while varying the mean temperature, T_m , and the temperature variance, ΔT_j . A suitable lifetime indicator, such as on-resistance, must also be chosen to indicate the point of failure of the power device. For a typical silicon device, the lifetime is modelled by (10) where k_b and E_a represent Boltzmann's constant and activation energy respectively. A and α are constants that depend on the packaging and the materials used.

$$N_f = A \cdot \Delta T_j^\alpha \cdot e^{\frac{E_a}{k_b \cdot T_m}} \quad (10)$$

In the case of SiC MOSFETs however, difficulties arise in terms of lifetime prediction and characterisation due to the phenomenon of gate threshold voltage shift [16]. This effect is more prominent in SiC MOSFETs compared to Si MOSFETs or IGBTs and makes it difficult to use conventional lifetime indicators as they are dependent on threshold voltage.

III. GATE DRIVER DESIGN

In general, the following features are desirable for an ideal gate driver.

- High driving capability
- Low gate driver loop inductance
- Short circuit protection
- Miller clamping
- Sufficient insulation rating
- Low coupling capacitances between high and low sides
- Low cost
- Small footprint
- Low power consumption

At present, there are plenty of driver ICs and evaluation boards are commercially available. However, it is typically very difficult to find a commercially available solution with all the above-mentioned features. Often, designers have to resort to using more than one part to meet the requirements. For instance, one driver IC can be used for protection function in cascade with another driver IC with high driving capability. It

is important to understand the requirements so that a custom-made driver can be designed in efficient manner.

The fast switching speed of SiC MOSFETs compared with Si IGBTs lead to special gate drive requirements. The driver must possess high current driving capability in addition to a low parasitic inductance in the gate driver loop so as to minimise voltage overshoot at the gate and improve the switching speed of the driver. Generally, the internal resistances, R_{on-i} and R_{off-i} , of the driver seen by the current is different for turn-on and turn-off of the switch. The turn-on resistances and turn-off resistances may be approximated from the datasheet using the output peak source current, I_{OH} and peak sink current I_{OL} respectively. Turn-on and turn-off resistances can be approximated using (11) and (12) where V_{cc} is the supply voltage to the driver. The driver IC can be modelled as shown in Fig. 10 where diodes depicted are ideal.

$$R_{on-i} = \frac{V_{cc}}{I_{OH}} \quad (11)$$

$$R_{off-i} = \frac{V_{cc}}{I_{OL}} \quad (12)$$

Fig. 10. Driver loop

Often, the cost of driver ICs with high driving capability is high. Hence, it is important to assess the overall performance of the driver through either theoretical calculations or experiment. For approximate theoretical calculations, the driver loop may be modelled as shown in Fig. 10. The parasitic inductance can be approximated using (7) and (8). The gate drivers external resistance and the gate driver will then have to be selected such that the damping factor as mentioned in (6) is sufficiently high. It should be noted that in theory, a driver IC with lower driving capability but lower external gate resistance can perform as well as a driver IC with higher driving capability but higher gate resistance.

The fast switching speed of SiC MOSFETs can also cause cross-talk between two complementing devices which can lead to accidental turn on and, shoot through in consequence. Hence, a suitable way of suppressing this cross talk must be chosen. Presently, there are a few ways of suppressing this cross-talk. A more comprehensive explanation of the various solutions are presented in [20]. In this paper, the mechanism for cross talk is briefly reviewed and two of the more commonly used methods for suppressing cross talk, miller clamping and negative turn-off voltage, are discussed.

Fig. 11. Cross-talk mechanism and effect of miller clamping

The mechanism of cross-talk is depicted in Fig. 11. The turn-on of the lower device causes a $\frac{dv}{dt}$ to appear across the miller capacitance of the upper switch which in turn causes a current to flow through the gate driver loop along the path depicted by the solid line and consequently, a spurious gate voltage to appear across the gate of the upper switch. The peak of this spurious voltage, $V_{gs-u(max)}$, was determined [27], [28] to be related to the $\frac{dv}{dt}$, R_{g-u} , C_{gd-u} , C_{gs-u} and V_{dc} according to (13). As seen by (13), an increase in $\frac{dv}{dt}$ increases the peak of the spurious voltage. This is the main reason why SiC MOSFETs are more prone to cross-talk compared with Si IGBTs.

$$V_{gs-u(max)} = \frac{dv}{dt} \cdot R_{g-u} C_{gd-u} \cdot \left(1 - e^{-\frac{V_{DC}}{\frac{dv}{dt} \cdot R_{g-u} C_{gs-u}}}\right) \quad (13)$$

One of the ways accidental turn-on due to cross talk is prevented is through the use of a negative gate turn-off voltage. This is typically recommended by various SiC device manufacturers. The negative turn-off voltage increases the noise margin of the gate signal as depicted in Fig. 12.

Another popular way is to use miller clamping. It is a feature integrated into many modern gate driver ICs and the basic concept behind it is to create another path of low resistance for the gate current to flow as depicted by the dotted path in Fig. 11. By creating this low resistance path, the gate and source terminals are effectively shorted, hence, in theory, the magnitude of the spurious gate voltage is reduced to zero. In reality, however, the low resistance path has a finite amount of resistance associated with it. Hence, according to (13), the magnitude of spurious voltage is reduced but not eliminated. Hence, it is important to be able to assess the magnitude of spurious voltage through either experiment or theoretical calculations.

The short circuit capability of SiC MOSFETs is well-known [14], [15], [29] to be lower than Si IGBTs. It is hence important to have short-circuit protection that can respond within about $3\mu s$ to $4\mu s$ and to ensure that sufficient overrating

Fig. 12. Noise margin

TABLE VI
COMPARISON OF HARD AND SOFT TURN-OFF ENERGIES @ 750V

	T_j	Current							
		2A	4A	6A	8A	10A	12A	14A	16A
E_{off} (μJ)	25°C	107	117	125	130	136	135	143	146
	100°C	110	119	128	132	137	140	146	148
$E_{off}(ZVS)$ (μJ)	25°C	12	22	30	35	41	40	48	51
	100°C	15	24	33	37	42	45	51	53

current is set for the device. In this work, the ADuM4135 gate driver IC with a fault response time of $2.2\mu s$ was used for protecting IMZ120R045M1 SiC MOSFETs.

Insulation must also be implemented in the driver in the form of creepage and clearance distances. A typical standard used for this is the IEC 60664 [30].

IV. CONVERTER DESIGN

SiC MOSFETs are well-known for their lower switching energies compared with silicon devices. However, this does not eliminate the need for soft-switching techniques. Converters such as the dual-active bridge (DAB) and the LLC converter employ soft-switched SiC MOSFETs to reach high efficiencies and power densities. Hence, it is beneficial and advisable to soft-switch SiC devices in converters.

Zero-voltage switching (ZVS) eliminates turn-on switching energy and recovers the stored E_{oss} energy in the C_{oss} capacitance during the soft turn-on of the switch. In Table VI, a list of hard turn-off switching energies is presented for the case of IMZ120R045M1 with an anti-parallel SCS240KE2. The measured E_{oss} energy corresponding to the combination is $95\mu J$. In a soft-switched converter with ZVS, the switching energy dissipated by the switch over one switching period, $E_{off}(zvs)$, can be calculated using (14). In Table VI, the values of $E_{off}(zvs)$ are presented. Comparing the switching energies for both hard-switching and soft-switching, it can be seen that the energies dissipated under soft-switching are significantly lower than those obtained under hard switching. Hence, for designs where high switching frequency is required, soft-switching is recommended.

$$E_{off}(ZVS) = E_{off} - E_{oss} \quad (14)$$

After obtaining data on the switching energies for various load current and temperature conditions, the energies may

be input into a lookup table for simulation and design. The process for predicting the device losses was highlighted in [19]. In this paper, the hardware for the dual active bridge with topology seen in Figure 16 is briefly presented. The power module PCB, high frequency transformer and inductor laboratory prototypes are shown in Fig. 13. It should be noted that in this work, an external inductor is used in series with the secondary side transformer winding. This inductance can also be implemented as transformer leakage inductance if required. The power modules on both sides use the same driver. On the primary side, the power module is an NPC leg. On the secondary side, the power module is an H-bridge. The waveforms corresponding to converter operation at 3.8kW of output power and 50kHz switching frequency are also presented in Fig. 14. The waveforms depicted are primary side current, I_p , primary side voltage, V_p , secondary side voltage, V_s and H-bridge output V_{hb} . Efficiency at this condition was measured to be 97.5 percent. Voltage spikes on both primary and secondary side are minimal as seen in Fig. 14 due to optimized commutation inductance.

Fig. 13. Prototype DAB

Fig. 14. Waveforms under operation

V. CONCLUSION

Practical guidelines for device characterization and prototyping with SiC MOSFETs have been presented in this paper. Device characterization, gate driver design and converter design have been discussed and various practical guidelines have been highlighted. It was found that the parasitic inductance of a commutation loop can be estimated to a reasonable degree and that application of the various guidelines yielded a SiC converter with a reasonably good efficiency of 97.5 percent.

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