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2018

Ye, J., Gooi, H. B., Wang, B., & Zhang, X. (2019). A new flexible power quality conditioner with model predictive control. IEEE Transactions on Industrial Informatics, 15(5), 2569-2579. doi:10.1109/TII.2018.2874159

<https://hdl.handle.net/10356/143391>

<https://doi.org/10.1109/TII.2018.2874159>

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A New Flexible Power Quality Conditioner with Model Predictive Control

Jian Ye, *Member, IEEE*, Hoay Beng Gooi, *Senior Member, IEEE*, Benfei Wang, *Member, IEEE*, and Xinan Zhang, *Member, IEEE*

Abstract—This paper presents the topology, analysis, and control implementation of a new single-phase flexible power quality conditioner (FPQC), which can be used for handling voltage and current related power quality (PQ) problems. Different from other PQ compensating devices, the FPQC can work under two compensating modes, i.e., parallel connection mode (PCM) and series connection mode (SCM). When the source voltage is unpolluted, the FPQC is working under the PCM so that the load harmonic current and reactive power can be compensated. When the source voltage is polluted, the FPQC is switched to the SCM to mitigate the impact caused by the polluted voltage. In this way, a desired voltage can be maintained at the load side to protect the critical load. The mode switching between PCM and SCM is realized by two relays. To ensure fast dynamics response and smooth transient operation, the model predictive control (MPC) method is applied to regulate the developed FPQC. Both the simulation platform and laboratorial prototype are built to validate the effectiveness of the system. The simulation and experimental results are presented and discussed.

Index Terms—Active filter, power quality (PQ), PQ conditioner, model predictive control (MPC).

I. INTRODUCTION

IN the modern microgrids, the distributed generation (DG) systems are penetrating [1], [2]. Due to the intermittent nature of the DG and the various interfaces with power converters, the power quality (PQ) problems become critical in the microgrids [3]–[5]. The intermittent power supply by the DG may generate voltage sag and swell at the source side. It can cause irreparable damages to the critical loads. The nonlinear load and the interfaces with power converters can draw nonlinear current at the load side [1], [2]. It will further pollute the upstream power grid. The heavy inductive load can decrease the power factor (PF) of the system [1], [2]. To deliver the same amount of active power, the generator needs to generate more power under a low PF. This will also increase the copper losses in the generator. The electric utility companies usually impose a penalty on the customer of a low PF. Thus, it is essential to mitigate the PQ problems in the microgrids. Among the aforementioned PQ problems, the voltage sag is the most cru-

cial one. The critical loads, e.g., the semiconductor processing machines are more sensitive to the voltage sag. Thus, the semiconductor manufacturing requires a higher level of PQ. According to the thresholds recommended by SEMI F47 [6], [7], the semiconductor processing machines should tolerate sags to 50% of the nominal voltage for duration of up to 0.2 s, sags to 70% for up to 0.5 s, sags to 80% for up to 1.0 s, and work continuously under sags to 90%. In order to satisfy the SEMI F47 standard, the dynamic voltage restorer (DVR) is widely applied to handle the voltage sag in the microgrids [8]–[13]. By injecting a compensating voltage in series with the distribution line, the load voltage can be maintained at the desired magnitude [8]–[13]. The IEEE 519 standard recommends that the THD of the source current should be within 5% [14]. To eliminate the load harmonic current and increase the PF, the distribution static compensator (DSTATCOM) can be installed at the distribution line [15]–[19]. By injecting a parallel current, the source current can be sinusoidal and in phase with the source voltage [15]–[19].

Unfortunately, the DVR and DSTATCOM can only handle the voltage and current related PQ problems, respectively. For the newly developed microgrids where all these PQ problems exist, they may lose their efficacy. Under these circumstances, it is required that all these devices should be installed in order to solve the PQ problems, which is obviously cost prohibitive. Additionally, managing and maintaining these individual components can be complicated and expensive. In order to overcome this drawback, the unified power quality conditioner (UPQC) is developed to deal with the PQ problems [20]–[25]. The UPQC is an integration of series and parallel converters and has the ability of improving PQ at both the load side and source side of the microgrids [20]–[25]. Even though the UPQC has been studied for twenty years and already has the ability of handling almost all PQ problems in the microgrids, it still facing great challenge on commercialization. The main reason is that UPQC consists of two sets of high frequency power converters. This leads to a higher capital and maintenance cost compared with that of other PQ compensating devices. The critical loads require voltage PQ compensation at the distribution level. This generates a strong thrust on the installation of the DVR along the distribution lines for maintaining the desired voltage magnitude.

As it is known, the DVR only needs to be activated when the source voltage is polluted. If the source voltage is at the rated magnitude, the DVR has to inject a zero magnitude voltage through the series transformer. This will introduce harmonic

This work is supported by the Energy Innovation Programme Office through the National Research Foundation and Singapore Energy Market Authority. Project LA/Contract No.: NRF2014EWT-EIRP002-005.

J. Ye, H. B. Gooi, B. Wang, and X. Zhang are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore (e-mail: JYE007@e.ntu.edu.sg; EHBGOOI@ntu.edu.sg; BWANG7@e.ntu.edu.sg; ZHANG0342@e.ntu.edu.sg).

voltage, which is generated by the high frequency converter, in the unpolluted source voltage. One solution is to place a bypass switch in parallel with the series transformer, thus the DVR will not introduce harmonic voltage during the voltage steady state [8]. It is noted the DVR will not operate during the voltage steady state, which means that the DVR is not fully utilized. If the DVR can compensate the load harmonic current and reactive power under the steady state, it will alleviate the burden of the upstream flexible AC transmission systems based compensating devices and further increase the utilization rates of the power converters in the DVR. Thus, equipping DVR with harmonic current and reactive power compensation capability contributes to improve the efficiency of the microgrids.

In this paper, we intend to develop a flexible power quality conditioner (FPQC). The FPQC can work under the current compensating mode to recoup the load harmonic current and reactive power during the voltage steady state. When the voltage is polluted, the FPQC can be switched to the voltage compensating mode to deal with the nonsinusoidal voltage. If the voltage PQ problem no longer exists, the FPQC can be switched back to the current compensating mode. The mode switching is accomplished by the relays, which is not high frequency switches. They will only operate under the mode switching conditions and their on-state resistance is very low. Therefore, the operating losses of the relays are relatively lower compared with the high frequency switches. Additionally, the manufacturing cost of the relays is lower than the high frequency switches. As a result, the manufacturing cost of the proposed FPQC is lower than the UPQC system [20]-[25]. We also propose to use a series connected capacitor to handle the injecting voltage so that the series transformer is not necessary in the FPQC system. In this way, the manufacturing cost of the system is further reduced. The detailed topology of the FPQC will be introduced in Section II. The discrete-time models of the FPQC are also derived in Section III. Based on the derived discrete-time models, the model predictive control (MPC) method is applied to realize the online implementation of the developed FPQC. The MPC has the advantages of offering fast dynamics response and smooth transient performance [26]-[32]. By applying the MPC, controller gain tuning, which is required by conventional proportional-integral (PI) controller, is not needed. The MPC based controller is described in Section IV. The simulation study is conducted on MATLAB/SIMULINK platform in Section V. A laboratorial prototype is built to test the developed FPQC in Section VI. Section VII concludes this paper.

II. SYSTEM TOPOLOGY

Fig. 1 shows a single-phase FPQC topology, where i_L , i_S and i_f are the load current, source current and inductor current, respectively; v_L , v_S , v_f and V_{dc} represent the load voltage, source voltage, series compensation voltage and DC-link voltage, respectively. v_p , v_n , i_p and i_n are the upper arm and lower arm voltages and currents, respectively. As illustrated in Fig. 1, the single-phase FPQC consists of a half-bridge converter (HBC) (S1 and S2), a DC power supply (V_{dc}), two neutral-point-clamped DC capacitors (C_{dc1} and C_{dc2}), a parallel

Fig. 1. Topology of FPQC system.

Fig. 2. PCM of FPQC system.

Fig. 3. SCM of FPQC system.

inductor (L_f), a series capacitor (C_f) and two relays (Relay1 and Relay2). C_{dc1} and C_{dc2} have the same capacitance that they can equally share the DC link voltage. When the contacts of Relay1 and Relay2 are switched between normally open (NO) and normally closed (NC), the FPQC can work under two different modes, i.e., parallel connection mode (PCM) and series connection mode (SCM).

When v_S is unpolluted, the contacts of Relay1 and Relay2 are NO. The FPQC is working in PCM, which is presented in Fig. 2. In PCM of the FPQC system, the parallel injected i_f can compensate the undesired current i_L from the critical nonlinear load. In this way, i_S can be sinusoidal and in phase with v_S .

When v_S is polluted, the contacts of Relay1 and Relay2 are

NC. The FPQC is working in SCM as illustrated in Fig. 3. In SCM of the FPQC system, the series injected v_f can mitigate the undesired voltage v_s from the source. Therefore, v_L can be maintain as the desired sinusoidal waveform.

III. DISCRETE-TIME MODEL

A. Discrete-Time Model for PCM

The equivalent circuit of the PCM of the FPQC system is illustrated in Fig. 4. The switches S1 and S2 of the HBC are controlled by the signals G1 and G2. The output voltage of the HBC can be expressed as follows:

$$v_{con1} = u_1 \frac{V_{dc}}{2} \quad (1)$$

where u_1 is the switching variable. When S1 is ON and S2 is OFF, $u_1 = 1$. When S1 is OFF and S2 is ON, $u_1 = -1$.

Based on Fig. 4, and by applying Kirchhoff's voltage and current laws, the equations describing the dynamics of the PCM are as follows:

$$v_{con1} + L_f \frac{di_f}{dt} - v_s = 0 \quad (2)$$

$$i_L + i_f - i_s = 0 \quad (3)$$

Based on the theory of MPC, (2) can be discretized when $t = k + 1$ using the forward-Euler method as follows:

$$i_f(k+1) = i_f(k) + \frac{T_s}{L_f} v_s(k) - \frac{T_s}{L_f} v_{con1}(k) \quad (4)$$

where T_s is the sampling time. As T_s is relatively small, the sensed signals v_s and i_L can be considered as constant values during two the subsequent sampling instants. The following equations can be obtained.

$$v_s(k+1) = v_s(k) \quad (5)$$

$$i_L(k+1) = i_L(k) \quad (6)$$

According to (3), we have

$$i_s(k+1) = i_f(k+1) + i_L(k+1) \quad (7)$$

By substituting (4) and (6) into (7), (7) can be rewritten as follows:

$$i_s(k+1) = i_f(k) + \frac{T_s}{L_f} v_s(k) - \frac{T_s}{L_f} v_{con1}(k) + i_L(k) \quad (8)$$

As illustrated in Fig. 1, it can also be derived that

$$i_p = i_f \quad (9)$$

$$i_n = -i_f \quad (10)$$

Then the dynamics of the DC link voltage can be described as follows:

$$C_{dc1} \frac{dv_p}{dt} = i_f \quad (11)$$

$$C_{dc2} \frac{dv_n}{dt} = -i_f \quad (12)$$

We discretize (11) and (12) in the following

$$v_p(k+1) = v_p(k) + \frac{T_s}{C_{dc1}} i_f(k) \quad (13)$$

Fig. 4. Equivalent circuit of PCM of FPQC system.

Fig. 5. Equivalent circuit of SCM of FPQC system

$$v_n(k+1) = v_n(k) - \frac{T_s}{C_{dc2}} i_f(k) \quad (14)$$

Based on (4), (5), (6), (8), (13) and (14), the discrete-time state-space model of the PCM can be derived as

$$x_1(k+1) = A_1 x_1(k) + B_1 u_1(k) \quad (15)$$

$$y_1(k) = C_1 x_1(k) \quad (16)$$

where

$$A_1 = \begin{bmatrix} 1 & \frac{T_s}{L_f} & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & \frac{T_s}{L_f} & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ \frac{T_s}{C_{dc1}} & 0 & 0 & 0 & 1 & 0 \\ -\frac{T_s}{C_{dc2}} & 0 & 0 & 0 & 0 & 1 \end{bmatrix}; \quad B_1 = \begin{bmatrix} -\frac{T_s V_{dc}}{2L_f} \\ 0 \\ -\frac{T_s V_{dc}}{2L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix};$$

$$C_1 = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix};$$

$x_1(k) = [i_f(k) \ v_s(k) \ i_s(k) \ i_L(k) \ v_p(k) \ v_n(k)]^T$ is the state variable vector; $u_1(k)$ is the control input, i.e., the switching variable in

(1); and $y_1(k) = [i_s(k) \ v_p(k) \ v_n(k)]^T$ is the process output. $i_s(k)$ is regulated to track the source current reference. $v_p(k)$ and $v_n(k)$ are utilized to balance the DC-link voltage between C_{dc1} and C_{dc2} .

B. Discrete-Time Model for SCM

The equivalent circuit of the SCM of the FPQC system is shown in Fig. 5. The signals G1 and G2 control the switches S1 and S2 of the HBC. The output voltage of the HBC can be presented as follows:

$$v_{con2} = u_2 \frac{V_{dc}}{2} \quad (17)$$

where u_2 is the switching variable. When S1 is ON and S2 is OFF, $u_2 = 1$. When S1 is OFF and S2 is ON, $u_2 = -1$.

In Fig. 5, the dynamics of the SCM are described by the following equations.

$$C_f \frac{dv_f}{dt} + i_f - i_s = 0 \quad (18)$$

$$v_{con2} + L_f \frac{di_f}{dt} - v_f = 0 \quad (19)$$

$$v_s - v_f - v_L = 0 \quad (20)$$

When $t = k + 1$, (18) and (19) can be discretized using the forward-Euler method as follows:

$$v_f(k+1) = v_f(k) - \frac{T_s}{C_f} i_f(k) + \frac{T_s}{C_f} i_s(k) \quad (21)$$

$$i_f(k+1) = i_f(k) + \frac{T_s}{L_f} v_f(k) - \frac{T_s}{L_f} v_{con2}(k) \quad (22)$$

The sensed signals i_s and v_s are still considered as constant values during two subsequent sampling instants, thus,

$$i_s(k+1) = i_s(k) \quad (23)$$

$$v_s(k+1) = v_s(k) \quad (24)$$

From (20), we have

$$v_L(k+1) = v_s(k+1) - v_f(k+1) \quad (25)$$

By substituting (21) and (24) into (25), (25) is rewritten as

$$v_L(k+1) = v_s(k) - v_f(k) + \frac{T_s}{C_f} i_f(k) - \frac{T_s}{C_f} i_s(k) \quad (26)$$

The dynamics of the DC link voltage have already been described in (11) and (12). The discrete-time functions of the DC link voltages are given in (13) and (14). Based on (21), (22), (23), (24), (26), (13) and (14), the discrete-time state-space model of the SCM can be derived as follows:

$$x_2(k+1) = A_2 x_2(k) + B_2 u_2(k) \quad (27)$$

$$y_2(k) = C_2 x_2(k) \quad (28)$$

where

$$A_2 = \begin{bmatrix} 1 & -\frac{T_s}{C_f} & \frac{T_s}{C_f} & 0 & 0 & 0 & 0 \\ \frac{T_s}{L_f} & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ -1 & \frac{T_s}{C_f} & -\frac{T_s}{C_f} & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & \frac{T_s}{C_{dc1}} & 0 & 0 & 0 & 1 & 0 \\ 0 & -\frac{T_s}{C_{dc2}} & 0 & 0 & 0 & 0 & 1 \end{bmatrix}; \quad B_2 = \begin{bmatrix} 0 \\ -\frac{T_s V_{dc}}{2L_f} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix};$$

$$C_2 = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix};$$

$x_2(k) = [v_f(k) \ i_f(k) \ i_s(k) \ v_L(k) \ v_s(k) \ v_p(k) \ v_n(k)]^T$ is the state variable vector; $u_2(k)$ is the control input, i.e., the switching variable in (17); and $y_2(k) = [v_L(k) \ v_p(k) \ v_n(k)]^T$ is the process output. $v_L(k)$ is regulated to track the load voltage reference. $v_p(k)$ and $v_n(k)$ are used to achieve the DC link voltage balancing between C_{dc1} and C_{dc2} .

IV. MPC BASED CONTROLLER DESIGN

As the MPC method exhibits superior dynamic and steady state performances in power electronic applications [26]-[32], it is employed to regulate the developed FPQC. Based on the derived discrete-time modes in Section III, the MPC based controller is designed for the PCM and SCM of the FPQC system.

A. Generation of Source Current Reference

In Fig. 6, the generation of the source current reference is presented at the left-hand side. Based on the single-phase p-q theory [33], v_L is considered as the α -axis quantity $v_{L\alpha}$, whereas the β -axis quantity $v_{L\beta}$ is obtained by $\pi/2$ lag of v_L . Similarly, the $\alpha\beta$ -axis quantities $v_{s\alpha}$, $v_{s\beta}$, $i_{L\alpha}$ and $i_{L\beta}$ are obtained from v_s and i_L . By using Akagi's p-q theory [34], the load active power is calculated as follows:

$$p_L = \frac{1}{2} (v_{L\alpha} \cdot i_{L\alpha} + v_{L\beta} \cdot i_{L\beta}) \quad (29)$$

A low pass filter (LPF) is utilized to track the fundamental load active power $\bar{p}_L$. As the source only supports the fundamental load active power during the PCM of the FPQC system, $\bar{p}_L$ is utilized to compute the $\alpha\beta$ -axis quantities of i_s as follows:

$$\begin{bmatrix} i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} = \frac{2}{v_{s\alpha}^2 + v_{s\beta}^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} \bar{p}_L \\ 0 \end{bmatrix} \quad (30)$$

Then $i_{s\alpha}^*$ gives the required reference source current signal, i.e., $i_s^* = i_{s\alpha}^*$.

B. Generation of Load Voltage Reference

As presented at the right-hand side in Fig. 6, v_s is sent to a phase-locked loop to obtain the synchronization angle ωt . The load voltage reference can be expressed as follows:

Fig. 6. Block diagram of MPC method for FPQC system.

$$v_L^* = \sqrt{2}v_{L,rms} \sin(\omega t) \quad (31)$$

where $v_{L,rms}^*$ is the root-mean-square (RMS) value of the nominal load voltage v_L .

C. Cost Function and Minimization for PCM and SCM

On one hand, the predictive current control scheme aims at maintaining the source current at the desired sinusoidal waveform during the PCM of the FPQC system. Hence, the error between the predicted source current and the reference source current should be minimized. On the other hand, the predictive voltage control scheme should minimize the error between the predicted load voltage and the reference load voltage to maintain the load voltage at the nominal magnitude during the SCM of the FPQC system. Furthermore, the error between the voltages of the DC link capacitors C_{dc1} and C_{dc2} is also minimized to ensure that the DC link voltage is balanced during the PCM and SCM. In the MPC method, the cost functions are implemented to determine the optimal control actions for output regulation under PCM and SCM [31]. In the cost functions, the predict horizon N_p and control horizon N_c are utilized. It means with the measured variables $x_i(k)$, $i = 1, 2$ in (16) and (28), the future output variables ($y_i(k+1)$, $y_i(k+2)$, $\dots$, $y_i(k+N_p)$), $i = 1, 2$ are predicted for N_p number of samples using N_c number of control variables ($u_i(k)$, $u_i(k+1)$, $\dots$, $u_i(k+N_c-1)$), $i = 1, 2$. The cost function J_i is defined as follows:

$$J_i = (Y_{i1} - R_i)^T (Y_{i1} - R_i) + \lambda_i (Y_{i2} - Y_{i3})^T (Y_{i2} - Y_{i3}), \quad i = 1, 2 \quad (32)$$

where $Y_{11} = [i_s(k+1) \ i_s(k+2) \ \dots \ i_s(k+N_p)]^T$; $Y_{21} = [v_L(k+1) \ v_L(k+2) \ \dots \ v_L(k+N_p)]^T$; $Y_{12} = Y_{22} = [v_p(k+1) \ v_p(k+2) \ \dots \ v_p(k+N_p)]^T$; $Y_{13} = Y_{23} = [v_n(k+1) \ v_n(k+2) \ \dots \ v_n(k+N_p)]^T$; $R_1 = \underbrace{[11 \dots 1]^T}_{N_p} i_s^*(k)$, $i_s^*(k)$ is the source current reference;

$R_2 = \underbrace{[11 \dots 1]^T}_{N_p} v_L^*(k)$, $v_L^*(k)$ is the load voltage reference; and

λ_i , $i = 1, 2$, is the weighting factor, which is used to decide the trade-off between the reference signal tracking and DC link voltage balancing. We assume $Y_1 = [i_s(k+1) \ v_p(k+1) \ v_n(k+1) \ i_s(k+2) \ v_p(k+2) \ v_n(k+2) \ \dots \ i_s(k+N_p) \ v_p(k+N_p) \ v_n(k+N_p)]^T$ and $Y_2 = [v_L(k+1) \ v_p(k+1) \ v_n(k+1) \ v_L(k+2) \ v_p(k+2) \ v_n(k+2) \ \dots \ v_L(k+N_p) \ v_p(k+N_p) \ v_n(k+N_p)]^T$. Y_i can be calculated as follows [32]:

$$Y_i = F_i x_i(k) + \Phi_i U_i, \quad i = 1, 2 \quad (33)$$

where $U_i = [u_i(k) \ u_i(k+1) \ \dots \ u_i(k+N_c-1)]^T$, $i = 1, 2$;

$$F_i = \begin{bmatrix} C_i A_i \\ C_i A_i^2 \\ C_i A_i^3 \\ \vdots \\ C_i A_i^{N_p} \end{bmatrix}, \quad i = 1, 2;$$

$$\Phi_i = \begin{bmatrix} C_i B_i & 0 & 0 & \dots & 0 \\ C_i A_i B_i & C_i B_i & 0 & \dots & 0 \\ C_i A_i^2 B_i & C_i A_i B_i & C_i B_i & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ C_i A_i^{N_p-1} B_i & C_i A_i^{N_p-2} B_i & C_i A_i^{N_p-3} B_i & \dots & C_i A_i^{N_p-N_c} B_i \end{bmatrix},$$

$i = 1, 2$

As u_i , $i = 1, 2$, has two possible control actions (1 and -1), all possible control actions of U_i are $(U_i^1, U_i^2, \dots, U_i^N)$, $i = 1, 2$, where $N = 2^{N_c}$. Using (33) and all the possible control actions of U_i , all possible future output $(Y_i^1, Y_i^2, \dots, Y_i^N)$, $i = 1, 2$, can be predicted. After that, $(Y_i^1, Y_i^2, \dots, Y_i^N)$, $i = 1, 2$, $i_s^*(k)$ and $v_L^*(k)$ are substituted into the cost function J_i to obtain a series values of $(J_i^1, J_i^2, \dots, J_i^N)$, $i = 1, 2$. The minimal value $J_{i,min}$ can be found among $(J_i^1, J_i^2, \dots, J_i^N)$, $i = 1, 2$. Then, the corresponding U_i is the optimal control action $U_{i,op}$, which can achieve the minimal error. The first control action of $U_{i,op}$, i.e., $u_{i,op}(k)$, is utilized as the present control action. The aforemen-

tioned procedure is illustrated in Fig. 6.

D. Mode Switching Logic

Initially, the FPQC system is working in the PCM (Relay 1 and Relay 2 are NO, $i = 1$). According to the SEMI F47 curve [6], [7], the no interruption in function region is 90%-110% for the percentage of the nominal voltage. According to the standard of the IEEE 519 THD limitation [14], the THD of the voltage $v_{S,THD}$ should be within 5%. At each sampling instant, the proposed control algorithm checks if the RMS value of the source voltage $v_{S,rms}$ is within the range of (90% 110%) and the THD of the source voltage $v_{S,THD}$ is within 5%. If it is true, the FPQC system is working in the PCM (Relay 1 and Relay 2 are NO, $i = 1$). If it is false, the FPQC system is working in the SCM (Relay 1 and Relay 2 are NC, $i = 2$). It is noted that the mode switching only happens at the beginning of the next cycle. The reason is at least one cycle is needed to determine the RMS value of the source voltage. As the critical load should tolerate sags to 50% of the nominal voltage for duration of up to 0.2 s (10 cycles) [6], [7], one cycle polluted voltage will not damage the critical load. After one cycle, the FPQC is switched to the SCM so that the voltage can be compensated. It is pointed out that the tolerated range and THD limitation can be updated according to the practical requirement of the critical load. The mode switching logic is summarized in Fig. 7.

V. SIMULATION RESULTS

In order to validate the FPQC system, the simulation is conducted on the MATLAB/Simulink platform. The system parameters in the simulation are listed in Table I. The configuration of the nonlinear load is presented in Fig. 8. The simulation scenarios are arranged as follows: The system is operating under the nonlinear load condition. Before $t = 0.2$ s, v_s is not polluted. During $t = 0.2-0.3$ s, v_s is polluted with sag, swell or harmonic. At $t = 0.3$ s, v_s is back to unpolluted condition.

The simulation results of the FPQC system during the voltage sag condition are presented in Fig. 9. Before $t = 0.2$ s, as v_s is not polluted, the FPQC system is in PCM. i_f is injected to compensate the nonlinear load current i_L . The THDs of i_L and i_s are listed in Table II. After compensation, the THD of i_s is within the IEEE 519 THD limitation. During $t = 0.2-0.3$ s, v_s is polluted with a 30% sag. The FPQC system is switched into SCM at $t = 0.22$ s (1 cycle after the sag occurs). By injecting v_f into the system, v_L can be maintained at the nominal magnitude. At $t = 0.3$ s, v_s is back to unpolluted condition. The FPQC system is switched back to PCM at $t = 0.32$ s (1 cycle after the sag is dismissed) for the load current compensation. It can be observed that v_p and v_n can be maintained at 500 V during the operation of the system.

The simulation results of the FPQC system during the voltage swell condition are illustrated in Fig. 10. Before $t = 0.2$ s, the FPQC system is also in PCM. i_f is injected to compensate i_L . After compensation, the THD of i_s is within the IEEE 519 THD limitation. In $t = 0.2-0.3$ s, a 30% voltage swell occurs in v_s . The FPQC system is switched to SCM at $t = 0.22$ s (1 cycle after the swell is measured). By injecting v_f into the system, v_L is maintained at the nominal magnitude. At $t = 0.3$ s, v_s is back to

Fig. 7. Block diagram of mode switching logic for FPQC system.

TABLE I
FPQC SYSTEM PARAMETERS

Source nominal voltage and frequency	$v_s = 230$ V $f_s = 50$ Hz
DC-link voltage	$V_{dc} = 1000$ V
Nonlinear load	$R_1 = 10$ Ω $L_1 = 6.5$ mH $R_2 = 20$ Ω $C_1 = 3900$ μ F
Parallel inductor	$L_f = 13$ mH
Series capacitance	$C_f = 30$ μ F
DC-link capacitance	$C_{dc1} = 2200$ μ F $C_{dc2} = 2200$ μ F
Sampling time	$T_s = 20$ μ s
Predict horizon and control horizon	$N_p = 4$ $N_c = 2$
Weighting factors	$\lambda_1 = 10$ $\lambda_2 = 30$
LPF cut-off frequency	$f_c = 30$ Hz

Fig. 8. Configuration of nonlinear load.

TABLE II
THDs OF SOURCE AND LOAD VOLTAGE AND CURRENT

Nonlinear load	THD (%)			
	i_s	i_L	v_s	v_L
FPQC	3.6	41.8	25.0	2.9

Fig. 9. Simulation results of FPQC system during voltage sag condition.

Fig. 10. Simulation results of FPQC system during voltage swell condition.

unpolluted condition. The FPQC system is switched back to PCM at $t = 0.32$ s (1 cycle after the swell is dismissed). v_p and v_n can also be maintained at 500 V during the voltage swell condition.

Fig. 11 shows the simulation results of the FPQC system under the voltage harmonic condition. A 25.0% voltage harmonic happens in v_s during $t = 0.2$ - 0.3 s. Thus, the FPQC system is originally in PCM. i_s is compensated to satisfy the standard of the IEEE 519 THD limitation. The FPQC system is switched to SCM at $t = 0.22$ s (1 cycle after the harmonics are measured). By injecting v_f , v_L is maintained at the desired value. The THDs of v_s and v_L are listed in Table II. After compensation, the THD of v_L is 2.9%, which is within the IEEE 519 THD limitation. At $t = 0.3$ s, v_s is back to steady state. The FPQC system is switched back to PCM at $t = 0.32$ s (1 cycle after the harmonic is dismissed). A balanced 500 V can be maintained for v_p and v_n during the voltage harmonics.

VI. EXPERIMENTAL RESULTS

A laboratorial prototype is built to validate the performance of the developed FPQC. Fig. 12 shows the laboratorial prototype of the FPQC. The SEMIKRON IGBT based inverter is applied as the HBC. The diode bridge rectifier is connected to the RLC load to work as nonlinear load. Two DC capacitors are used as the upper and lower arm DC link capacitors. The programmable DC source is used to support the DC capacitors. The programmable AC source is applied as the supply of the

Fig. 11. Simulation results of FPQC system during voltage harmonic condition.

Fig. 12. Prototype of FPQC: (a) programmable DC source, (b) solid-state relays, (c) DC capacitors, (d) series AC capacitor, (e) parallel inductor, (f) V/I sensors, (g) dSPACE, (h) oscilloscope, (i) SEMIKRON IGBT based inverter and diode bridge rectifier, (j) RLC load.

Fig. 13. Experimental results of FPQC when source voltage changes from steady state to voltage sag: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

Fig. 14. Experimental results of FPQC when source voltage changes from voltage sag to steady state: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

system. The solid-state relays are utilized to realize the mode switching of the FPQC. The dSPACE is utilized as the digital signal processor to realize the control of the FPQC. The experimental results are presented in Figs. 13-18.

As shown in Fig. 13, when v_s is under steady state, the FPQC is operated in PCM. i_s is regulated to sinusoidal waveform by injecting i_f through L_f . When a 30% voltage sag happens in v_s , the FPQC is able to switch to SCM for voltage compensation. Thus, v_f starts to inject in series with the distribution line via C_f . v_L can be maintained at the desired magnitude during the sag condition.

In Fig. 14, when v_s changes from voltage sag to steady state, the FPQC is switched from SCM back to PCM for current compensation. i_f is able to maintain i_s as sinusoidal waveform.

In Fig. 15, v_s changes from steady state to 30% voltage swell. The FPQC is switched from PCM to SCM. When the FPQC is

operated in PCM, i_s can be corrected to sinusoidal waveform. When the FPQC is in SCM, the 30% voltage swell is eliminated.

In Fig. 16, when v_s changes from 30% voltage swell to steady state, the FPQC is switched back to PCM. v_f will not inject in the line. i_s is compensated by injecting i_f .

Fig. 17 shows the transient performance of the FPQC when v_s changes from steady state to voltage harmonic. When voltage harmonic occurs, the FPQC is switched from PCM to SCM. When the FPQC is operated in PCM, i_s is able to be compensated. When the FPQC is switched to SCM, the voltage harmonic can be mitigated by injecting v_f .

In Fig. 18, when v_s changes from voltage harmonic to steady state, the FPQC is switched from SCM back to PCM. The magnitude of v_f changes to 0, as voltage compensation is not required during the steady state. In PCM, i_s is regulated to

Fig. 15. Experimental results of FPQC when source voltage changes from steady state to voltage swell: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

Fig. 16. Experimental results of FPQC when source voltage changes from voltage swell to steady state: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

Fig. 17. Experimental results of FPQC when source voltage changes from steady state to voltage harmonic: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

Fig. 18. Experimental results of FPQC when source voltage changes from voltage harmonic to steady state: time (20 ms/div), (a) source voltage v_s (300 V/div), load voltage v_L (300 V/div), series compensation voltage v_f (300 V/div); (b) source current i_s (20 A/div), load current i_L (20 A/div), inductor current i_f (20 A/div); (c) upper arm DC-link capacitor voltage v_p (200 V/div), and lower arm DC-link capacitor voltage v_n (200 V/div).

sinusoidal waveform.

In Fig. 13-18, it can be observed v_p and v_n are balanced and maintained at 500 V. It is also noted that the mode switching of

the FPQC happens after one cycle when the voltage sag, swell and harmonic occurred or dismissed. The reason is that one cycle is needed to determine the state of v_s .

Finally, we would like to discuss the differences of DVR, UPQC, and FPQC. The DVR can only solve the voltage PQ problem. Thus, the power converter of the DVR cannot be utilized when the source voltage is in steady state. The DVR tends to cause additional power losses in steady state. The UPQC can handle both voltage and current related PQ problems concurrently. However, the capital cost of UPQC is much higher as it consists of two sets of high switching frequency power converters (series part and shunt part). The series part of UPQC will also cause additional power losses when the source voltage is in steady state. The FPQC consists of one set of high switching frequency converter (20 KHz to 2 MHz) and one set of low switching frequency relay (switch only once in each fundamental supply cycle at most). The capital cost of FPQC is greatly reduced compared to that of UPQC. The priority of FPQC is to handle the voltage related PQ problem. When the source voltage is in steady state, the FPQC can deal with the current related PQ problem to alleviate the burden of the upstream STATCOM.

From the viewpoint of the load, with a lower capital cost the FPQC increases the acceptability of installing a PQ conditioner by satisfying the voltage compensation when the source voltage is polluted and providing additional current compensation when the source voltage is in steady state.

VII. CONCLUSION

In this paper, a new single-phase FPQC has been developed to solve the PQ problems in microgrids with significantly reduced cost. The developed FPQC system can be operated under the PCM and SCM to handle the current and voltage related PQ problems respectively. An MPC based controller has also been designed to effectively regulate the FPQC to obtain fast dynamics and smooth transient performance. The simulation study and the experiment are also conducted to validate the performance of the developed FPQC based on the MATLAB/Simulink platform and laboratorial prototype, respectively. It was demonstrated that when the sag/swell of the source voltage is detected within one cycle, the FPQC system can be switched from the PCM to the SCM at the beginning of the next cycle. Thus, the load voltage can be regulated at the desired magnitude to protect the critical load. When the sag/swell of the source voltage no longer exists, the FPQC system can be switched back to the PCM for the current compensation. In this way, the load harmonic current and reactive power can be compensated if the source voltage is unpolluted.

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Benfei Wang (S'12, M'17) received the B.Sc. degree in Electronic Information Science and Technology from University of Science and Technology of China, China, in 2011. He received the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2017. He is currently a Research Fellow at the Energy Research Institute at NTU. His research interests include model predictive control, multi-port DC-DC converter, hybrid energy storage system and microgrids.

Xinan Zhang (S'10, M'14) received the B.E. degree in electrical engineering and automation from Fudan University, China, in 2008. He received the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2014. Then, he worked as postdoc researcher in NTU and the University of New South Wales from 2014 to 2017. He joined NTU as Lecturer in June 2017. His research interests include electrical machine drives, control and modulation of power electronic converters and management of hybrid energy storage systems.

Jian Ye (S'15, M'18) received the B.Eng. degree in electrical engineering and automation from Wuhan University, Wuhan, China, in 2012, and the M.Sc. and PhD degrees in power engineering from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2013 and 2018, respectively.

His research interests include power electronics for various applications such as connecting renewable energy sources, energy devices to microgrids, and

power quality compensation.

Hoay Beng Gooi (SM'95) received the B.S. degree in EE from National Taiwan University in 1978; the M.S. degree in EE from the University of New Brunswick in 1980; and the Ph.D. degree in EE from Ohio State University in 1983.

From 1983 to 1985, he was an Assistant Professor with Lafayette College, Easton. From 1985 to 1991, he was a Senior Engineer with Empros (now Siemens), Minneapolis, where he was responsible for the design and testing coordination of domestic and

international energy management system projects. In 1991, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, as a Senior Lecturer, where he has been an Associate Professor since 1999. He was the Deputy Head of Power Engineering Division during 2008-2014. His current research interests include microgrid energy management systems, electricity markets, spinning reserve, energy efficiency, and renewable energy sources.