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A Generic Gate Driver for SiC MOSFETs with adjustable Positive and Negative Rail Voltage

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Abstract—SiC MOSFETs are well known for possessing lower losses compared with silicon MOSFETs or IGBTs. In order to drive them efficiently, suitable drivers must be designed. However, most commercially available drivers and drivers in literature are suitable for only a limited range of SiC MOSFETs due to limitations on the MOSFET's gate voltage ratings. Hence, the drivers do not allow the designer to easily experiment with different SiC MOSFET models. In this paper, a generic SiC gate driver with adjustable positive and negative voltage rail is presented. The performance of the proposed driver is compared with a commercially available driver through experiment and it is shown that the proposed gate driver is able to drive the chosen SiC MOSFET more efficiently.

Keywords—SiC MOSFET, gate driver

I. INTRODUCTION

SiC devices have been known to possess significantly lower losses compared with silicon devices [1-6]. However, in order to attain such low losses, the devices must be switched quickly and this leads to problems such as increased electromagnetic interference (EMI) [7-9] and voltage or current overshoots [10-13] which can potentially destroy or reduce the health of the device. In addition to this design issue, designers using SiC MOSFETs often consider more than one device from a variety of manufacturers. It is therefore important to have a suitable gate driver that can be optimized and yet simultaneously adapted to drive different SiC MOSFETs. To date, many guidelines and application notes for design of conventional MOSFET gate drivers exist [14-16] alongside less conventional designs proposed in research [17-20]. However the drivers for these papers are often targeted at one specific model of MOSFET and do not allow for adjustment of their rail voltages should a change in device be required.

In this paper, a driver design with adjustable positive and negative rail voltages is presented. Double pulse tests are performed on a SiC MOSFET using the proposed driver and a commercial driver to compare improvement in switching energies. The proposed driver's key parts and design parameters are also presented to aid the designers with their gate driver design.

II. HARDWARE SETUP

A. Proposed driver

The block diagram of the proposed driver is shown in Fig. 1 and the driver board top side and bottom side is shown in Fig. 2. The component list of key parts of the driver are given in Table I. The driver board is of 15cm in length and 2.5cm in width. The proposed driver is modified version of MSCSICMDD/REF1 gate driver from Microsemi and it is capable of driving MOSFETs at different values of positive and negative rail voltage. The schematic of the Microsemi driver is available in [21]. SiC MOSFETs from various manufacturers with their corresponding gate drive voltage specifications are mentioned in Table II. The Common recommended gate drive voltages include +15V/-5V, +20V/-5V and +18V/0V. The proposed driver is capable of outputting these voltages as seen in Fig. 3.

Fig. 1. Block diagram of the proposed gate driver

TABLE I. KEY COMPONENTS OF GATE DRIVER

Block	Main components
Isolated supply	LT3999 push-pull integrated circuit, CSMH1-200HE TR13 schottky diodes, transformer with RM core
3.3V output regulator	LD1086DT33TR
Optical isolation	AFBR-1624Z fibre optic transmitter AFBR-2624Z fibre optic receiver ADuM4135
Variable voltage reference	LT1172 switching regulator, TL1431 current reference, 84WR10KLF potentiometer
Driver	IXRFD630

Fig. 2. Gate driver

(a) Driver outputting voltages at +15V/-5V

(b) Driver outputting voltages at +20V/-5V

(c) Driver outputting voltages at +18V/0V

Fig. 3. Gate driver output at different voltages

TABLE II. GATE VOLTAGES OF VARIOUS SiC MOSFETs

Voltages	Compatible switches	
	Manufacturer	Switch models
+15V/-5V	Infineon	IMW120R045M1, IMZ120R045M1
+20V/-5V	CREE	C2M0160120D, C2M0045170D, C2M0280120D, C2M0080120D, C2M0040120D, C2M0025120D
+18V/0V	Rohm	SCT3160KL, SCH2080KE, SCT2120AF, SCT2160KE, SCT3060AL, SCT3080KL

A general schematic of a gate driver with its gate driver loop and corresponding parasitic loop inductance, L_{gate} , is presented in Fig. 4. It is important to minimize L_{gate} in order to drive switches more quickly and prevent overvoltage oscillations at the gate. In order to improve driving capability, the IXRFD630 from IXYS was chosen as it possess a high current output capability of 28A and the wide pin connections allowed for reduction of parasitic inductance in the gate driver loop. The forward and return paths are placed on opposite layers so as to minimize the overall parasitic inductance of the loop as seen in Fig. 5. Unlike most commercial drivers, where traces are usually kept thin due to size constraints, the traces in the proposed gate driver's loop have been made wide to further reduce the inductance in the gate driver loop. Turn-on gate resistance of the driver is set to be 10Ω and turn-off gate resistance is set to be 5Ω .

Fig. 4. Schematic depicting gate driver loop

(a) Forward path during turn-on

(b) Return path during turn-on

Fig. 5. Forward and return paths of gate driver

The proposed gate driver's performance is compared with a commercial gate driver. Both drivers are used in the double pulse tester. The extracted switching energies for the turn-on and turn-off of the chosen SiC MOSFET for each driver are compared to verify the effectiveness of the proposed gate driver.

In addition to low parasitic inductance in the gate driver loop, it is important to ensure the proper creepage and clearance distances in order to prevent insulation failure. A suitable guide for this can be found in [23]. For a voltage of 1200V in a laboratory environment, the recommended creepage and clearance distances according to [23] are 6.3mm and 1.5mm respectively. Isolation between high and low voltage sides is ensured through the use of a high frequency transformer, an opto-isolator and suitable spacing in between the high and low voltage sides as seen in Fig. 6. In many drivers, short circuit protection is incorporated by sensing the voltage at the drain which may be as high as 1200V for a typical commercial MOSFET. It is hence important to incorporate a routing slot in between the drain connection and other points which may take a lower potential with respect to it

such as the gate and source connections. Such a routing slot is shown in Fig. 7. It should be noted that in order to test the driver for this paper, the short-circuit protection has been bypassed through the use of a jumper resistor as seen in Fig. 7. The jumper resistor must be removed before protection can be used.

Fig. 6. Spacing in between high and low voltage sides

Fig. 7. Routing slot for isolation and jumper resistor

B. Commercial driver

The commercial driver used is SKHI 10/12 from semikron is shown in Fig. 8. This driver is typically used for driving IGBTs but can also be used to drive SiC MOSFETs.

Fig. 8. Semikron SKHI 10/12 driver

C. SiC devices

The SiC MOSFET and SiC schottky diode chosen for characterization are IMW120R045M1 and the C4D15120D. The SiC MOSFET is first characterized with the body diode of another SiC MOSFET acting as the commutation partner. The characterization is repeated with the SiC schottky diode as the commutation partner.

D. Double pulse test module

In order to minimize voltage overshoots, it is important to reduce the commutation inductance. The double pulse tester's schematic is depicted in Fig. 9. The design board of the double pulse test module is presented in Fig. 10. The commutation inductance, L_{com} , of the test module is estimated to be 35nH.

Full details on how the tester was implemented was presented in [22]. Device voltage across Q1 during switching is set using voltage source V_{dc} . During operation, two pulses are fed to the gate of Q1 to switch the device. During the first pulse, current is through inductor L is ramped up to the desired level before the device is turned off. At the falling edge of the first pulse, turn off energy is measured. It is during this turn-off where voltage overshoot can occur as a result of L_{com} . During the rising edge of the second pulse, turn-on occurs and the turn-on energy is measured.

Fig. 9. Schematic of double pulse tester with commutation loop

Fig. 10. Double pulse tester module

III. RESULTS

The SiC devices are tested at a voltage of 750V for a range of current values from 2A to 16A and temperature values of 25°C and 90°C. Alignment of drain-source voltage and drain-source current is done in the same manner as in [22] with a deskew time of 8ns. The switching energies are post-processed using MATLAB scripts. The switching waveforms for some conditions are shown in Fig. 11. In Fig. 11, the scope integration function is used to show the switching energies during turn-on and turn-off. The switching energies can be read from the Δy value under channel F3.

In Fig. 12, Fig. 13, Fig. 14 and Fig. 15, the switching energies are presented at applied voltage of 750V. It can be seen from these results that for the various switching conditions, the proposed driver exhibits lower loss. This is especially so for turn-off energies as seen in Fig. 13 and Fig. 15

where turn-off energies were reduced by about a factor of 3 at higher current values.

(a) Turn-on waveforms of IMW120R045M1 MOSFET with IMW120R045M1 body diode as commutation partner and proposed gate driver. Waveforms are gate-source voltage (green), drain-source voltage (red), drain-source current (blue), cumulative switch energy (purple)

(b) Turn-off waveforms of IMW120R045M1 MOSFET with IMW120R045M1 body diode as commutation partner and proposed gate driver. Waveforms are gate-source voltage (red), drain-source voltage (blue), drain-source current (orange), cumulative switch (green)

Fig. 11. Turn-on and turn-off waveforms for IMW120R045M1 MOSFET at 750V/16A

Fig. 12. Turn-on energies of IM120R045M1 MOSFET with IM120R045M1 body diode at 750V

Fig. 13. Turn-off energies of IM120R045M1 MOSFET with IM120R045M1 body diode at 750V

Fig. 14. Turn-on energies of IM120R045M1 MOSFET with C4D15120D diode at 750V

Fig. 15. Turn-off energies of IM120R045M1 MOSFET with C4D15120D diode at 750V

IV. CONCLUSION

A generic gate driver for SiC MOSFETs with adjustable positive and negative rail voltages has been presented in this paper. The driver possesses wider traces in the gate driver loop compared with commercial drivers and this helps minimize the

parasitic inductance so that SiC switches can be driven more quickly. The block diagram and key parts of the driver have also been presented. The experimental results for different positive and negative rail voltages have been shown for the effectiveness. The performance of the proposed gate driver has been compared with a commercially available driver. The results indicate that the proposed driver can drive SiC devices more efficiently than a commercial driver. Readers are encouraged to contact the authors for full details on schematics and parts list if interested.

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