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DESIGN AND ANALYSIS OF A LOW-NOISE REGULATED NEGATIVE VOLTAGE GENERATOR SYSTEM

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

2-Aug-2020

Date

(Assoc.) Prof. Boon Chirn Chye

Authorship Attribution Statement

This thesis contains material from papers published in the following peer-reviewed journal in which I am listed as an author.

(1) Chapter 4 to Chapter 6 is published as: **D. Khanna**, C. C. Boon, P. Choi, L. Siek, B. Liu and C. Li, “A Low-Noise, Positive-Input, Negative-Output Voltage Generator for Low-to-Moderate Driving Capacity Applications,” in *IEEE Tran. on Circuits and Sys.-I, Regular Papers*, vol. 66, no. 9, pp. 3423 - 3436, July 2019.

The contribution of the co-authors is as follows:

1. **(Assoc.) Prof. Boon Chirn Chye** provided the initial research direction and was involved in detailed review and editing of the manuscript.
2. **Dr. Pilsoon Choi** introduced me to the concept of negative voltage generation and provided with inputs regarding improving the quality and content of the manuscript, throughout the course of its preparation, from its initial draft till its final submission.
3. **(Assoc.) Prof. Liter Siek** helped with a detailed review of the finalized manuscript and provided valuable suggestions for improving the quality and presentation of its technical content.
4. **Bei Liu** coordinated with the application verification of proposed Negative Voltage Generator with Gallium-Nitride High Electron Mobility Transistor (GaN-HEMT) based RF power-amplifier. He also assisted with review and submission of draft manuscript.

5. **Chenyang Li** assisted with the initial system verification on the probe station setup, and helped in the review and preparation of final manuscript.

2-Aug-2020

Date

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Devrishi Khanna

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Summary

This thesis presents the design and analysis of a generic, low-noise regulated negative voltage generator, with wide tuning range and moderate driving capability. The highly integrated solution comprises of a multi-phase clock generator, fully-integrated charge-pump and a regulator block while requiring only one off-chip capacitor that can be shared with supply decoupling capacitors. A novel analysis of the charge-pump module incorporating the effect of non-zero switch resistance and finite on-time of switches, is proposed, and a closed form expression of its output impedance is derived. The resulting frequency dependent charge-pump linear model is included in the regulator setup and utilized for the system level analysis and verification from both small and large signal prospective. This includes ascertaining the stability of the feedback loop, quantifying the charge-pump noise rejection by the regulator module and analysis of the complete settling profile from power-up till steady-state. In addition, the system level performance is further verified through rigorous transient co-simulation of the charge-pump and regulator modules. The overall solution is powered from a single 3.3V DC input and provides an output tuning range from -4.4V to +2.1V for biasing applications. The design also supports a maximum load current of $250\mu\text{A}$, $550\mu\text{A}$ and $800\mu\text{A}$ for regulated output voltage at -3.0V, -1.5V and 1.5V respectively. The measured steady-state ripple is under $3mV_{PP}$ while the noise voltage at the charge-pump operating frequency harmonics is below $130\mu V_{RMS}$ and the noise-floor is under $5\mu V_{RMS}$. The design is also application verified with a Gallium-Nitride power amplifier, thus further confirming its low-noise performance. Implemented in CMOS 180nm process, the prototype chip occupies an area of $0.55mm^2$.

A systematic design methodology, supplemented with an in-depth analysis of CP and regulator modules, ensures robust implementation with reliable performance

output. An on-chip negative generator can facilitate the integration of alternate technologies with mainstream CMOS, besides allowing the designer to experiment with much wider range of circuits and applications. In this regard, the proposed negative voltage generator with low-noise output, wide-tuning and moderate driving capacity can cater to a wide range of integrated applications over multiple circuit design domains. Moreover, the design and analysis carried out in this work is useful towards the evolution of an on-chip negative voltage source that can be potentially included as a generic IP in future SOCs.

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List of Abbreviations

BW	Bandwidth
CMOS	Complimentary Metal-Oxide Semiconductor
CP	Charge-Pump
DAE	Differential-Algebraic Equations
ESR	Equivalent Series Resistance
FOM	Figure-of-Merit
FSC	Fast Switching Condition
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IP	Intellectual Property
LDO	Low Dropout Regulator
NVG	Negative Voltage Generator
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PM	Phase-Margin
PWM	Pulse Width Modulation
SC	Switched-Capacitor
SOC	System-On-Chip

SSC	Slow Switching Condition
TR	Tuning Range
UGB	Unity Gain Bandwidth
WC	Worst Case

Chapter 1

Introduction

1.1 Motivation

Negative voltage supply was ubiquitously employed in early analog integrated circuits, such as instrumentation-amplifiers, fully-differential operational-amplifiers (Op-Amp), etc., which commonly utilized a split-rail power supply configuration, with equal positive and negative supply rail magnitude, referenced to a common ground potential. This balanced 3-way input supply (positive, negative and ground) was readily derived from the output of a centre-tapped transformer, whereby each of its two out-of-phase outputs were followed by linear regulators, to derive the respective positive and negative voltage rails. This dual-rail power supply input gradually gave way to single supply input (positive supply and ground), as it was more compatible with the battery powered operation and resulted in significantly simpler power management implementation. The previous generation split-rail circuits, although not as widely-utilized as before, are still implemented for certain niche applications, such as low-distortion audio amplifiers, zero-voltage detection data converters, and other similar high-performance industrial and automotive applications requiring, a wide input and output voltage range.

Apart from CMOS, negative voltage supply has been a key enabler of certain specific applications and technologies, such as EEPROM (Flash) memory (Fig.1.1(a)) and biasing of III-V depletion mode device, for circuits such as gallium-nitride (GaN) based RF power-amplifier. The use of negative voltage for EEPROM memory application was firstly reported in [17], where it was utilized to implement a low-voltage

Fig. 1.1: Negative voltage Applications: EEPROM memory (a) Nand-Flash memory devices (b) Floating gate cell utilizing negative voltage for erase operation [17, 41]

source-side erase operation, resulting in denser memory implementation improved reliability for the floating-gate devices used within such memories. In earlier EEPROM implementations, the erase operation required placing a high voltage at the source terminal (in excess of 10V), while maintaining the corresponding control-gate at ground, in order to induce Fowler-Nordheim tunneling, for removing the charges stored within floating gate. By utilizing an internally generated a high negative voltage magnitude at the gate terminal (Fig.1.1(b)), the required source potential for erase operation could be reduced proportionally, and thus allowed the use of single standard positive supply rail for the complete implementation.

Along the same lines, the biasing of III-V depletion mode device, for circuits such as gallium-nitride (GaN) based RF power-amplifier, as depicted in Fig. 1.2(b), is also a well-established application of negative voltage supply. The depletion mode devices such as GaN high-electron mobility transistor (HEMT), have significantly superior device characteristics as compared to bulk CMOS process, primarily in terms of having a high breakdown voltage, ultra-low on-resistance, a high $f_{t,max}$, and the ability to handle very high power densities. This intrinsic device properties have made them ideally suited for almost all high-frequency, high-power applications, such RF power-amplifier, DC-DC converter, switching-mode power supplies, etc. Moreover, due to their clear power-performance advantage over bulk CMOS process, the circuits and system utilizing these devices, have already witnessed large scale deployment in several commercial and military applications, despite the implementation overhead involved in their integration with rest of the system, usually implemented using low-cost CMOS technology. However, due to the depletion mode

Fig. 1.2: Negative voltage Applications: Depletion-mode device biasing (a) Depletion Mode I-V characteristics (b) GaN-HEMT based RF power-amplifier utilizing negative gate voltage [21]

operation, these devices are in default on-state, and thus manifest a negative threshold voltage ($-|V_{TH}|$) in their I-V transfer characteristics, as shown in Fig. 1.2(a). Consequently, their operation mandates the use of precisely controlled negative gate voltage, in order to bias them in the intend region of operation, as required for maximum performance extraction.

To further accelerate the development and adoption of depletion mode devices, several on-going research efforts [42–47] are focused towards the fabrication of these devices on the same silicon substrate, as that used for the mature CMOS process. The larger goal is directed towards developing a process integration technology, similar to a CMOS or a III-V only foundry process, that would be utilized for the large scale manufacturing of monolithic III-V/CMOS integrated circuits. In this

Fig. 1.3: Negative voltage Applications: Biomedical implants (a) Illustration of Cochlear implant (b) High-impedance biphasic electrical tissue stimulation

attractive eco-system, CMOS and III-V circuits operating alongside each other on the same chip, will be able to interface effectively, and will thus be able to deliver the highest levels of performance, while achieving the smallest form-factor. In this regard, a low-noise, regulated CMOS negative voltage generator solution, can play a vital role in this foreseeable integration of Depletion mode devices and other related technologies, with the mainstream CMOS, in the near future.

In addition to its traditional applications, in recent times, negative voltage supply also being explored for a wide-range of novel and upcoming applications. The minimum specifications and the desired performance of the required negative supply, is determined primarily by its end application. An overview of the emerging application landscape of negative voltage and its requirements is briefly introduced as follows.

The biomedical circuit frequently employ electrical stimulation of various body tissues and implants, through placement of a pair of electrodes, and passing a charge across them. In this case, the use of negative voltage has been explored [18, 22] to accommodate the large headroom generated through the constant current stimulation of high-impedance ($\sim 150\text{k}\Omega$) electrode-tissue junction (Fig. 1.3). The negative voltage anode terminal is therefore required to reach mid-to-high voltage magnitude, while supporting load currents in hundreds of micro-amperes.

Another important and emerging application area of negative voltage is static-leakage reduction and adaptive threshold voltage modulation, especially for large system-on-chip (SOC) related implementation. As the device feature size continues

Fig. 1.4: Negative voltage Applications: Static leakage reduction [23]

to shrink with technology scaling, the static leakage power is starting to occupy a significant and increasing proportion of the total power consumption budget of the system. In this regard, negative voltage can be applied for biasing the devices and circuits in deep cut-off region and can thus lead to orders of magnitude of improvement in leakage current, even at high operating temperatures, as depicted in Fig. 1.4. In [23], a similar locally generated negative voltage source was utilized for enabling completely turn-off of large RF front-end devices of a Bluetooth transmitter, and thus resulted in significant improvement in the overall transmitter efficiency. In such applications, the emphasis is on the efficiency of negative voltage source, such that the power invested in its generation should be significantly lower than the power gains derived from its implementation. Similarly, for digital circuits, negative voltage supply can be utilized for adaptively varying the threshold voltage of digital devices, by implementing dynamic body biasing of various sub-modules, used within a digital SOC implementation. This allows the system to make dynamic trade-off between speed and power, as per the instantaneous requirements of its environment, thus resulting in a highly-efficient yet responsive system implementation.

In RF circuit design domain, other than RF power-amplifier and static leakage reduction application, use of negative voltage supply has also been explored with high performance Class-C VCOs, as was recently reported in [24], [25]. In [24], negative voltage was used to bias and thus completely turn off NMOS cross-couple

Fig. 1.5: Negative voltage Applications: Class-C VCO [24] (a) VCO schematic (b) Class-C operation in PMOS only mode

pair, while the VCO was operating in the high-performance PMOS-only mode (Fig. 1.5). Eliminating the momentarily conducting path through NMOS pair, resulted in an at least 10% improvement in the LC tank quality factor, which directly translates into better phase-noise performance for the VCO. Thus for this application, the required negative voltage should have high regulation accuracy with moderate tuning range, while the negative voltage source should exhibit high power efficiency.

Lastly, the GaN-HEMT based RF PA, as a subset of depletion mode biasing application, is of particular interest [20, 21, 27], as it places the most stringent requirements on the regulated negative voltage, used for gate biasing of the PA. The required negative voltage should have high regulation accuracy to have a precisely controlled gate voltage magnitude, which can be fine tuned for biasing the PA in the intended region of operation. It should have wide tuning range (typically -4V to -1V), in order to cater to a wide range of PAs, with large variation in their negative threshold voltage magnitude and the resulting I-V transfer characteristics. It should also support moderate driving capacity ($< 1\text{mA}$), since the gate leakage current can have wide variation across temperature and can reach up to hundreds of micro-amperes for large PA device dimensions. Most importantly, the required negative voltage should be a low-noise input, with a high-degree of spectral purity, so that noise from the biasing terminal is not up-converted to RF frequencies, that can potentially lead to the corruption of RF output spectrum.

Fig. 1.6: I-V Specifications of Negative voltage applications

The required I-V specifications of the above mentioned applications, over multiple circuit design domains, is captured in Fig. 1.6, along with operating limits for the negative voltage generator (NVG) proposed in this work. This thesis thus aims to present the design of a generic, negative voltage generator solution, that can cater to multiple of such existing and emerging applications, while meeting the requirements of most demanding applications. Such an integrated negative voltage source will be able open new avenues for the designers to experiment with a much wider range of circuits, devices and technologies. Its implementation will facilitate the integration of alternate technologies with mainstream CMOS, besides accelerating the adoption of negative voltages supply and the development of novel applications based on its utilization. With the use of regulated negative voltage supply gaining momentum, a small on-chip negative voltage generator (NVG) module, can also be envisioned to be included as a generic intellectual-property (IP) in future SOC implementations.

1.2 Objectives

The principal objective of this work is to realized a generic, low-noise, regulated NVG system, that can support a wide range of application, while being suitable from an integration prospective. In addition, the design should deliver high regulation accuracy and superior low-noise performance, such that regulated negative

Fig. 1.7: Negative Voltage Generator: System level implementation

output voltage should be suitable for all precision voltage biasing and noise sensitive applications.

The intended system level implementation, along with an end application, is as shown in Fig. 1.7. The overall NVG system, while being powered from a single positive DC input supply, should be able to deliver a tunable, regulated and low noise, negative voltage output. The NVG system will typically comprise of CP driver circuit, a switched-capacitor (SC) based negative voltage charge-pump (CP) and post-regulation stage. The CP driver circuit receives an input periodic signal and splits into the multi-phase switching inputs, used for driving the capacitive loads within the SC-CP. The SC-CP produces a noisy, unregulated negative voltage output, which is filtered by the post-regulator stage to derive the required low-noise, regulated output at the desired magnitude.

Considering GaN-HEMT PA as a representative application, the regulated output voltage driving the gate of PA device, should be able to accurately bias the PA in the intended region of operation. As a test for the realistic noise-performance and regulation accuracy of the design, the PA should exhibit no variation in its efficiency or linearity performance with the given regulated input, as compared to the reference derived using external negative input source.

In terms of the required specifications of the regulated output, the most important aspect of the performance is the high regulation accuracy and low-noise

performance of the design, to ensure it can be utilized for the most demanding applications, requiring a precisely controlled voltage magnitude with minimal noise injection through the biasing terminal. The regulation accuracy can be assessed in terms the load and line regulation values while the low-noise performance can be evaluated by measuring the transient steady-state ripple in the time domain and the spectral analysis of the regulated output in the frequency domain. In addition, the design should provide a wide-tuning range ($-4V$ to $-1V$), while supporting moderate load driving capacity ($< 1mA$), in order to maximize its application potential for multiple existing and emerging negative voltage applications.

At the system level, the design should be implemented as a highly-integrated solution, requiring minimal number of off-chip components, such that it can readily utilized under varying application scenarios. Moreover, the overall system must be efficient in terms of area utilization and power consumption. Finally, the design effort should result in a robust NVG implementation with repeatable performance output which is immune to the vulnerabilities (possible forward biasing of parasitic p-n junction, latch-up, ESD) associated with the operation involving negative voltage.

1.3 Major Contributions of the Thesis

This work presents the design and analysis of the proposed low-noise, regulated negative voltage generator system. The highly integrated solution, provides regulated negative output voltage with high regulation accuracy, low transient steady-state ripple and high degree of spectral purity, while requiring only one off-chip capacitor, that can be shared with the supply decoupling capacitor of the end application. The regulated output magnitude can be further derived over a wide tuning range, including positive output voltages, while the design also supports moderate driving capacity of load currents up to $800\mu A$. In addition, the low-noise performance is extensively verified through measurement results and the overall performance is verified by operating it within a practical application environment. A summary of the major ideas introduced through this work, are presented as follows.

Firstly, the proposed NVG is a first-of-its-kind implementation of a fully-integrated

switched-capacitor (SC)charge-pump (CP) driving a linear regulator module, to derive the required low-noise, regulated negative output. The resulting configuration provides a high degree of integration and results in higher CP noise rejection, which translates into better noise performance at the output. The given design also validates the feasibility of low-power linear regulator being powered by a high output impedance source, such as a fully-integrated CP, to deliver low-noise, regulated output.

Secondly, the proposed NVG system is implemented under a systematic design framework, encompassing complete design and verification cycle, starting from derivation of CP and regulator specifications, till the overall, multi-dimensional, system-level verification. This structured design flow ensures a stable and robust system implementation, which is tolerant to PVT variations. It also lends scalability to the proposed design principles, such that they can be extended for the design of other switched-capacitor based regulated voltage generators.

Thirdly, a novel switched-capacitor CP operational analysis, incorporating the effect of non-zero switch resistance and finite on-time of the switches, is presented and used to derive a closed-form expression for CP output impedance. The analytical results are further utilized to derive the circuit level equivalent of required negative voltage CP, by optimizing its design parameters for minimum area utilization. Furthermore, the CP output transfer characteristic, predicted by the analytical model, is closely co-related with the counterpart derived from post-layout simulations and silicon measurement.

Fourthly, the system level functionality and performance is rigorously verified using both small and large-signal perspectives. In this regard, the stability of the regulator feedback loop is rigorously verified across its operating range, while incorporating the effect of CP linear model parameters on the feedback loop transfer function. The AC analysis of the CP noise rejection provided by the given regulator topology is presented and an equivalent noise-transfer function is derived and contrasted with corresponding simulation results. In addition, a detailed quantitative analysis of the complete settling characteristics is presented and verified with the corresponding large-signal transient simulation of the regulator. Moreover, to establish system stability and realistically assess the system performance, the pro-

posed NVG system is verified through transient co-simulation of CP and regulator modules.

Lastly, the low-noise performance of the design and other performance features are experimentally verified using a prototype chip fabricated in GlobalFoundries CMOS 180nm BCDlite process. The measured transient steady-state ripple is under $3mV_{PP}$ and the performance is only limited by the accuracy of external reference input. Moreover, the design is application verified with a state-of-the-art GaN-HEMT RF power-amplifier (PA), whereby the PA is verified to deliver identical performance as that obtained from the external negative voltage source. This further confirms the superior noise performance of the design, and clearly highlights its suitability for precision voltage biasing and noise-sensitive applications.

The novel analysis introduced in this work, at both the module and system level, is consistently contrasted and validated with the corresponding simulation and measurement results. For instance, the CP linear model, as obtained through analysis and simulation, is closely co-correlated with its counterpart extracted from measured CP performance characterization curves. Similarly, the measured settling profile and total settling times are accurately matched with ones derived through large-signal simulations and the proposed quantitative analysis, under varying operating conditions. This two-step verification of analytical findings, first by simulation and then through silicon verification, adds further credibility to the equivalent analytical models used for their derivation, and facilitates their use for other similar implementations and application scenarios.

1.4 Organization of the Thesis

The organization of this thesis is as follows.

In this chapter, an overview of the existing and emerging applications of negative voltage supply is presented and the central motivation for undertaking this work, is highlighted.

Chapter 2 presents a detailed review of the operation, design and optimization of the fully-integrated switched-capacitor charge-pumps. The known CP operational analysis techniques are examined and the design and operation of various fully-

integrated SC-CPs is quantitatively analyzed.

In chapter 3, the known regulation techniques that have been employed to derive regulated negative voltage output are reviewed.

Chapter 4 presents a detailed discussion on the design and circuit level implementation of the proposed NVG system. In this chapter, a systematic design methodology is outlined which is followed by transistor level implementation and operational analysis of SC-CP and negative voltage regulator modules.

In chapter 5, the system level functionality and performance is verified using both small and large-signal analytical techniques. This includes verification of regulator's feedback loop stability, CP noise rejection analysis, and a quantitative analysis of the initial settling transients.

Chapter 6 presents and analyses the measurement results obtained from the detailed experimental verification of the fabricated prototype of the proposed NVG system.

In chapter 7, the major analysis, design and implementation effort is summarized and some promising research directions for extending this work are recommended.

Chapter 2

Review of Switched-Capacitor Based Charge-Pump

2.1 Introduction

The term ‘charge-pump’ is used interchangeably to describe the CP module utilized within the analog PLL sub-system, and also for the switched-capacitor based charge-pump (SC-CP) implementation. The former operates by sourcing or sinking a fixed magnitude of current into or from the PLL loop filter, whereas the latter is utilizes capacitive charge-transfer to obtain boosted output voltage magnitude with same or inverted polarity. In context to a negative voltage generator system, an inverting SC-CP is employed to generate unregulated negative voltage at its output, as input for the following regulator stage. In this thesis, we focus on the design of the fully-integrated variant of such a switched-capacitor based CP circuit with inverting configuration so as to achieve an optimized implementation of this integrated negative voltage source.

The voltage multiplier circuits have been traditionally employed for applications such as non-volatile memories and lcd display drivers, whereby a high voltage magnitude is utilized to implement the erase operation in flash memory devices or improve the contrast ratio of the display panels. However, due to scaling down of input power supplies, such circuits have been (explored and) utilized for a wide range of applications including..(Moreover, to compensate for the performance degradation associated with lower operating headroom, these circuit have also been explored for

applications including ..Op-Amps, voltage regulators) ..In this regard, the switched capacitor based charge-pump offers a simple and cost-effective solution to derive the required on-chip boosting of input potential.

The SC-CPs operate by utilizing multi-phase (2-phase / 4-phase) periodic switching signals such that the average node voltage magnitude is increased by the switching signal amplitude, each time charge is shared across its charge-pumping stages, before being finally deposited on the output load capacitor. Unlike their switching regulator counterparts, these circuits do not require any inductive elements, which makes them well-suited for integration and for applications such as display panel, where the height of the components on the final PCB is tightly constrained. Moreover, such an implementation alleviates any EMI radiation concerns for the system level implementation and in general, results in lower on-chip or off-chip implementation space. Although the driving capacity of these circuits is lower than the inductor based dc-dc converters, variants of such CPs with off-chip pumping capacitors have been designed for a driving capacity of up to 150mA while providing over 90% efficiency for a wide range of load currents. The fully-integrated SC-CP variant with integrated charge-pumping capacitors utilizes a higher switching frequency (10MHz - 300MHz) to support load currents in hundreds of micro-amperes and offers moderate power efficiency up to 60%. Such an implementation is ideally suited for integrated applications requiring a internally generated high voltage magnitude with a large input-to-output voltage conversion ratio.

2.2 Charge-Transfer in a Switched Capacitor Charge-Pump

2.2.1 Principle of Operation

The charge-transfer involved in the SC-CP operation can be explained using the simplest voltage-doubler and inverter configurations, depicted in Fig. 2.1(a) and 2.1(b), respectively. With reference to Fig. 2.1(c), in the first phase (Φ_1) of the 2-phase input clock, switches S_1 and S_2 are closed and the pumping capacitor (C_P) is charged to supply potential. In the next phase the top plate is connected to GND

Fig. 2.1: Switched-Capacitor (SC) Charge-Pump (CP) based (a) Voltage Inverter (b) Voltage Doubler (c) Non-overlapping switching input

via switch S_3 , which causes the bottom plate potential being instantaneously pulled down to $-V_{DD}$ potential. At the same time, the bottom plate is connected to the load capacitor via switch S_4 , and the resulting charge-transfer between the C_P and C_L results in lowering of V_{OUT} .

If the switch resistance is neglected ($R_{SW} \approx 0$), then the bottom plate of C_P and output voltage acquire the same potential at the end of this switching phase. For the voltage doubler shown in Fig. 2.1(b), the first phase of input clock is identical, while in the second phase, the bottom plate is connected to the input potential, which results in top plate potential being boosted to $2 \cdot V_{IN}$, and thus the subsequent charge-sharing between the C_P and C_L causes the C_P to be raised.

For the sake of simplicity, it is initially assumed that switches are ideal ($R_{SW} \approx 0$) and no load is connected, then the V_{OUT} at the end of each cycle, can be evaluated using charge-conservation, obtained by equating the charge lost by the C_P (Q_{Lost}) to the charge gained by C_L (Q_{Gain}), as given by (2.1) -(2.3).

$$Q_{=Lost}(= C_P \cdot (V_1(i) - V_{OUT}(f))) = Q_{Gain}(= C_L \cdot (V_{OUT}(f) - V_{OUT}(i))) \quad (2.1)$$

$$V_{OUT} = V_1(i) \cdot \left[\frac{C_P}{C_P + C_L} \right] + V_{OUT}(i) \cdot \left[\frac{C_L}{C_P + C_L} \right] \quad (2.2)$$

$$\Delta V_{OUT} = (V_1(i) - V_{OUT}(i)) \cdot \left[\frac{C_P}{C_P + C_L} \right] \quad (2.3)$$

where ΔV_{OUT} is the change in the output voltage magnitude, at the end of a given switching cycle. The corresponding settling transient for V_{OUT} is as shown in Fig. 2.2. The change in V_{OUT} magnitude decreases with each subsequent cycle, since it is directly proportional to the difference between the initial potentials on the C_P and C_L , at the beginning of each cycle, as expressed in (2.3). Therefore, V_{OUT} follows an approximate exponential response during its initial transient and (over some finite cycles), eventually saturate at $-V_{DD}$ for inverting, and at $2 \cdot V_{DD}$ for boosting configurations respectively.

For the general case, when a finite load current is sourced from, or injected into the CP, the settling profile is similar, with V_{OUT} settling with a steady-state ripple, as shown in Fig. 2.3. Considering the inverting configuration, without loss of generality, in steady-state operation, during the charging phase C_P is isolated and the load current sinks into C_L , thus resulting in a linear increase in V_{OUT} magnitude. In the discharging phase, almost twice the magnitude of load current is injected into the bottom plate of C_P , thus discharging C_L and lowering V_{OUT} to its initial level. In this way steady-state ripple is generated and sustained on V_{OUT} . The current flowing through the switches S1 and S4 in the discharging phase can be evaluated using (2.4).

$$I_{S1} = I_{S4} = I_L \cdot \frac{T_{PRD}}{T_{ON}} = I_L \cdot \frac{1}{F_{IN} \cdot T_{ON}} \quad (2.4)$$

where T_{ON} is the on-time of the switches and $F_{IN} = (1/T_{PRD})$ refer to the switching frequency of the CP. This charge-balance ensures that the average current flowing into and out of C_P is maintained equal to the load current, and thus the average V_{OUT} remains constant during steady-state operation. The steady-state V_{OUT} magnitude in presence of a finite load current can be estimated in terms of the effective CP output impedance (R_{CP}), as given by (2.5).

$$V_{OUT} = -V_{DD} + I_L \cdot R_{CP} \quad (2.5)$$

The presumed linear characteristic of the CP in (2.5), will be verified through a detailed quantitative analysis, simulation and measurement results, as presented in the following sections of this report. As a qualitative estimate, the variation of

Fig. 2.2: Settling transient of CP output voltage (no-load)

Fig. 2.3: Settling transient of CP output voltage ($I_L > 0A$)

R_{CP} and steady-state ripple magnitude V_{RIPPLE} , in terms of CP parameters, can be made using (2.6) - (2.7).

$$R_{CP} \propto \frac{T_{PRD}}{C_P} \quad (2.6)$$

$$V_{RIPPLE} \propto \frac{I_L \cdot T_{PRD}}{C_L} \quad (2.7)$$

The various sources of non-idealities involved in a charge-transfer process are as depicted in Fig. 2.4. This primarily includes the switch resistance (R_{SW}) and the

Fig. 2.4: Sources of non-idealities in a SC-CP based charge-transfer process (a) External capacitor C_P (b) Fully-integrated C_P s

parasitics associated with the C_P , C_L capacitors. For a discrete CP realization, with large off-chip C_P and C_L , the parasitic effect is mainly contributed by the capacitor's inherent equivalent-series-resistance (R_{ESR}) and equivalent-series-inductance (ESL). The parasitic resistances R_{SW} and R_{ESR} cause the charge-transfer response to be over damped, thus ensuring that at the end of each switching cycle, the output settles to its steady-state value without ringing. For CPs employing integrated C_P/C_L , the non-linearities mainly originate due to the parasitic capacitance on the top and bottom plate of these caps. In this case, the R_{CP} exhibits a strong dependence on C_P , R_{SW} , while CP output at no-load is determined primarily due the impact of parasitics. It should be noted, that irrespective of the CP implementation, the parasitic resistances play a vital role in limiting the current peaking occurring at the instant a charge-transfer switches are turned on.

2.2.2 External versus Internal Capacitor Charge-Pumps

The basic SC-CP structure, as shown in Figs. 2.1(a) and 2.1(b), and as elaborated in the previous section, is ubiquitously employed in commercial products, to obtain an inverted or boosted output voltage directly, or to be derived as low-noise output post-regulation. A number of other design modifications, relating to efficiency improvement or additional functionality, have been explored for discrete SC-CPs [1–3], utilizing an external pumping capacitor. The large charge-transfer switches, oscillator, and switch driver circuits are integrated, while the CP requires at least 2 and typically 3 large off-chip capacitors, including the de-coupling capacitor for the input voltage, other than the pump (C_P) and load (C_L) capacitors. The required

Fig. 2.5: Dickson charge-pump (first integrated SC-CP realization)

switching frequency is relatively low, however due to the large sizing of off-chip caps, these CPs can support large load currents from 4mA to (up-to) 150mA. Moreover, the low operating frequency suppress the impact of parasitics and helps to minimize the power consumption in digital circuits. This allows such CPs to deliver high efficiency for a wide-range of load currents. However, due to practical limits on pin-count and number of off-chip components, such CPs are implemented in a single-stage voltage inverter or doubler configurations and are mainly are utilized for industrial or discrete applications such as with high load current requirements.

The first integrated realization of a SC-CP was proposed in 1976 in [4]. A N-stage implementation of this CP, in inverting configurations, is as shown in Fig. 2.5. The structure commonly referred to as 'Dickson CP', after the name of the inventor, consists of a series of diodes and integrated pump capacitances driven by alternating phase of the input clock. An 'N-stage' CP comprises of N-inverting (or boosting) stages each comprising of a pair diode and C_P , and an output stage connecting the C_L and load to the last inverting stage through the N+1th diode. The diodes acting as valves, block the flow of negative charge towards input potential (gnd), while providing a low resistance path as its shared towards output load capacitor. Thus, by enforcing uni-directional flow of charge, the average node voltage magnitude is increased by switching amplitude of the input clock, as the charge is pumped across each of the inverting stages.

If the diodes are initially assumed to be ideal switches, then for the steady-state operation, the charge pumped into and out of each C_P per cycle, must be equal to the total charge injected into the CP in one cycle ($Q_{TOT} = I_L \cdot T_{PRD}$). Thus, by using the principle of charge-conservation, then the node voltage magnitude corresponding with high (V_{nH}) and low (V_{nL}) phase of the input clock, can be derived using (2.8)

- (2.10).

$$V_{1H} = 0(gnd) \quad (2.8)$$

$$V_{1L} = V_{2H} = V_{1H} - V_{DD} + \frac{Q_{TOT}}{C_P} = -V_{DD} + \frac{I_L \cdot T_{PRD}}{C_P} \quad (2.9)$$

$$V_{2L} = V_{3H} = V_{2H} - V_{DD} + \frac{Q_{TOT}}{C_P} = -2 \cdot V_{DD} + 2 \cdot \frac{I_L \cdot T_{PRD}}{C_P} \quad (2.10)$$

Extending (2.8) - (2.10) to the generic N-stage inverting CP, the V_{OUT} and R_{CP} can be deduced using (2.11), (2.12).

$$V_{OUT} = -N \cdot V_{DD} + N \cdot \frac{I_L \cdot T_{PRD}}{C_P} \quad (2.11)$$

$$R_{CP} = \frac{N \cdot T_{PRD}}{C_P} \quad (2.12)$$

Thus, from this simplistic analysis, it can be concluded that both the CP output and its output impedance is increased by a factor of N , even while considering ideal charge-transfer and without incorporating the effect of parasitics and other CP non-idealities.

In addition to this integrated SC-CP, a number of fully-integrated CP architectures, utilizing MOS devices as switches, have been proposed and analyzed. A brief review of these CP topologies and the resulting difference in CP output transfer characteristics is covered at the end of this chapter.

The size of integrated C_P and C_L is highly constrained due to its large silicon area utilization and typically varies from few tenths of a pF to tens of pF for practical design purposes. Moreover, since it is at-least three order of magnitude smaller than its off-chip counterpart ($> 0.1\mu F$), these CPs employ significantly higher switching frequency to achieve driving capacity in hundreds of micro-amperes, such that they can be utilized for multiple low-power integrated applications. The CP efficiency is lower as compared to external capacitor variants, since the effective R_{cp} is significantly higher and digital power consumption is increased significantly due to higher F_{in} . In spite of the higher switching losses and relatively lower driving strength, such CPs can be optimized to yield peak efficiency values in excess of 50%. The main advantage for such CP implementation is that it can be readily extended to multiple stages without incurring a significant design and resource overhead. This

Table 2.1: Qualitative comparison between typical Discrete and Integrated CP implementation

Parameters	Discrete CP	Integrated CP
No. of CP stages	1 to 2	1 to 10
Pump Capacitance per stage	$0.1\mu\text{F}$ to $10\mu\text{F}$	10pF to 100pF
Operating Frequency	100kHz to 1MHz	10MHz to 100MHz
Max. load current	$< 150\text{mA}$	$< 1\text{mA}$
Peak Efficiency	up to 95%	up to 60%

makes such CPs well suited for applications requiring a high output voltage magnitude, or for applications where a large output-input voltage conversion ratio is required.

An overview of the differences between typical discrete (external capacitor) and integrated CP implementations, as mentioned in this section, is captured in Table 2.1.

2.3 Modelling and Analysis of Charge-Pump Operation

2.3.1 Analytical Modelling of SC-CP

In order to provide a framework for the modelling and quantitative analysis of SC-CP structures, this section first identifies the various CP designs and operating parameters, and then discuss the CP figure-of-merits which can be utilized as design specification and for benchmarking its performance. Following this, the CP operation under slow and fast switching condition is differentiated and the generic design and optimization flow is elaborated.

2.3.1.1 Charge-Pump Design and Operating Parameters and SC-CP FOMs

A simplified equivalent functional model for an inverting switched-capacitor charge-pump (SC-CP) implementation is presented in Fig. 2.6. This model can be utilized directly for the Dickson CP (shown in Fig. 2.5) and Dickson-like CPs, which operate by implementing a cascade of charge-pumping stages. Such CP architectures,

Fig. 2.6: Simplified functional model for the integrated SC-CP implementation

commonly referred to as linear CPs, result in linear increase in average node-voltage and output voltage magnitude with each additional CP stage. The equivalent circuit models the charge-transfer switch using a finite switch resistance (R_{SW}), and includes a pair of top and bottom plate parasitic capacitance for the integrated pump capacitance C_P , to model the loss of charge of at the switching instants and also during the charge-transfer phase. This model can well be extended to other non-linear SC-CPs implementations, such as the Fibonacci CP [5], by incorporating similar pair of top and bottom plate parasitic capacitance for the C_P and utilizing a similar R_{SW} in place of each charge-transfer device.

With reference to Fig. 2.6, the SC-CP main design and operating parameters, SC-CP FOMs are listed as mentioned in Table 2.2.

Table 2.2: Design, Operating Parameters and FOMs of integrated SC-CPs

	Parameters	Description/Symbol
Design Parameters	CP Topology	Linear/Non-Linear CPs
	Number of CP Stages	N
	Pump Capacitor per stg.	C_P
	CP Load Capacitor	C_L
Operating Parameters	Load Current	I_L
	Operating Frequency	$F_{IN} (1/T_{PRD})$
	Switch Turn-on Time	T_{ON}
CP FOMs	Voltage Gain	V/V
	Output Impedance	R_{CP}
	Power Efficiency	η_{Eff}
	Area	mm^2
	Power Density	$mWatt/mm^2$
	Ripple	mV_{PP}

In addition to the above listed parameters, the rise/fall time ($t_{rise}/t_{fall} \approx t_r$) of the input switching signals has significant impact on the total current consumption and thus on the overall power efficiency of the CP. It is primarily determined by the strength of the clock buffers driving the large capacitive loads within the CP,

and therefore . Moreover, the t_r also has an observable effect on the output voltage magnitude (and thus the CP output impedance), whereby V_{OUT} magnitude can decrease rapidly if the ratio of (t_r/T_{PRD}) is increased beyond a certain threshold by reducing the buffer size or by utilizing a higher operating frequency. Therefore, t_r can also be regarded as an additional operating parameter, thus must be taken into consideration to achieve an optimized CP implementation.

As is the case with silicon implementation of any other circuit module, the CP performance is mainly evaluated on the basis of it area utilization and power efficiency. Due to the relatively much smaller size of CP MOS switches, with respect to the integrated C_P ($1\text{pF} < C_P < 50\text{pF}$), the CP silicon footprint is directly linked to the total integrated capacitance including the load capacitance C_L , as given by (2.13).

$$A_{TOT} = k \cdot (N \cdot C_P + C_L) \quad (2.13)$$

where k is the proportionality constant based on the integrated capacitor density ($fF/\mu m^2$), dependent on the given technology. The load capacitor C_L is sized to be large enough to limit the steady-state ripple on the CP output for maximum load current, within acceptable bounds. The analysis of CP efficiency is much more involved and depends on both the design as well as the operating parameters of the CP. The CP efficiency evaluated as the ratio of power delivered at the output to the total power consumed by CP, can be derived in terms of the effective CP output impedance as given by (2.14).

$$\eta_{Eff} = \frac{V_{OUT} \cdot I_L}{V_{DD} \cdot I_{TOT}} = \frac{(N \cdot |V_{DD}| \cdot \gamma - I_L R_{CP}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{PAR})} \quad (2.14)$$

where γ captures the loss of charge due combined effect of CP parasitics and I_{PAR} represents the additional spurious current drawn from the supply during the CP steady-state operation. The total power consumption includes the power consumed within the multi-phase clock generators and clock driving buffer cells. The R_{CP} itself, is independent of the instantaneous load current I_L , and is dependent on the remaining design and operating parameters primarily including the charge-pumping capacitance per stage C_P , number of stages N , switch resistance R_{SW} , the operating frequency F_{IN} and the given SC-CP topology.

The CP output impedance therefore captures the overall effect of all the input parameters with respect to CP output voltage magnitude, and can therefore be interpreted as a more fundamental SC-CP FOM. The CP power consumption depends on the total current drawn from the supply and increases linearly with the input load current, as mentioned in (2.14). From (2.14), it can be observed that the parasitic component of the total current I_{PAR} is one causing addition increase in input power and therefore resulting in degradation of CP efficiency. The I_{PAR} , mainly arising from the power consumed in digital gates, increases linearly with operating frequency, while also increasing rapidly as size of buffers is increased or as their corresponding capacitive load is increased.

The total effective parasitic capacitances on the top and bottom plates can be approximated in terms of C_P through the technology dependent parameters α and β as given by (2.15).

$$C_{PAR_TOP} = \beta \cdot C_P \quad C_{PAR_BOT} = \alpha \cdot C_P \quad (2.15)$$

The parameters α and β includes contribution from both technology and design choices, as represented by (2.16).

$$\alpha = \alpha_C + \alpha_S \quad \beta = \beta_C + \beta_S \quad (2.16)$$

The terms α_C and β_C arise due to the inherent stray capacitance between the top/bottom plate and the CMOS substrate, and is primarily dependent on the technology node and layout drawing. The terms α_S and β_S model the parasitics contributed by the large charge-transfer switch and various interconnections among them. The values for α_S and β_S show strong dependence on operating frequency, switch-size and its placement and therefore majority of the design effort is concentrated towards minimizing their impact. In a typical CMOS process the overall α and β values are observed to exhibit a wide-variation from 0.02 to 0.5, with their corresponding magnitude reduced with lower technology nodes using advanced fabrication process.

2.3.1.2 Slow Switching vs Fast Switching Condition

For a given set of specifications, a SC-CP can be designed to operate in the slow switching condition (SSC) or the fast switching condition (FSC). In the SSC, the charge transfer between a pair of CP capacitors is if fully completed, within the on-time of the charge-transfer switches. In other words, the node voltage across the CP switches are equal (or almost equal) at the end of each charge-transfer phase. In contrast, the SC-CP operation in FSC implies that the on-time of the switches T_{ON} is significantly is comparable (or smaller) to the RC time constant ($\tau = R_{SW} \cdot C_P$) associated with the charge-transfer occurring across the switching devices. Therefore, in FSC operation the node voltages across the CP switches at the end of each switching cycle remain un-equal, even though the charge pumped through each C_P is same ($I_L \cdot T_{PRD}$), as required for the CP to maintain equilibrium at its steady-state operation.

The pioneering work in [6] provides a detailed analysis for the evaluation and optimization of CP output impedance in SSC and FSC operating regimes. In general, for any given SC-CP topology with a given set of design parameters (N, C_P, R_{SW}), as operating frequency is increased, the CP output impedance follows a smooth transition from SSC to FSC region, as illustrated in Fig. 2.7. Quantitatively, the effective CP output impedance (R_{CP_EFF}) can be expressed as (2.17)-(2.18).

$$R_{CP_EFF} = \sqrt{(R_{CP_SSC}^2 + R_{CP_FSC}^2)} \quad (2.17)$$

$$\text{where: } R_{CP_SSC} \propto \frac{N}{C_P \cdot F_{IN}} \quad (2.18)$$

$$\text{and: } R_{CP_FSC} \propto N \cdot (T_{PRD}/T_{ON}) \cdot R_{SWs} \quad (2.19)$$

As shown in (2.18), the term R_{CP_SSC} is inversely proportional to the product of ($C_P \cdot F_{IN}$) and occurs due to the finite rate of charge transfer for a given pump capacitor (C_P) magnitude. The term R_{CP_FSC} is found to be directly proportional to switch resistance (R_{SW}) [6] and is independent of both C_P and F_{IN} . It essentially represents the losses occurring across the switches due to charge-transfer process.

In SSC regime, the effect of finite switch resistance is effectively suppressed and thus the effective CP output impedance can be considered equal to the first term ($R_{CP_EFF} \approx R_{CP_SSC}$). It is to be noted that suppression of switch resistance is in

Fig. 2.7: CP output impedance transition from SSC to FSC regime ($N : 2, C_P : 15pF, R_{SW} : 500\Omega, T_{ON} : 0.5 \cdot T_{PRD}$)

terms of the evaluation of R_{CP_EFF} and not in terms of the power loss across switches, which regardless of the SSC operation will degrade the CP efficiency. Conversely, in FSC domain the term R_{CP_SSC} is significantly smaller in magnitude as compared to R_{CP_FSC} due to high operating frequency and thus R_{CP_EFF} can be approximated as equal to the second term ($R_{CP_EFF} \approx R_{CP_FSC}$).

The overall CP output impedance is thus restricted within the asymptomatic bounds set by R_{CP_SSC} and R_{CP_FSC} , as shown in Fig. 2.7. It also follows that SSC and FSC operating boundaries cannot be clearly demarcated as there exists a wide range of operating frequencies where both R_{CP_SSC} and R_{CP_FSC} would have comparable magnitude. However, considering a first-order charge transfer across switching devices ($V_o = V_f + (V_i - V_f) \cdot \exp(-T_{ON}/\tau)$), a ballpark estimate of CP operating regime can be inferred from the ratio of switch on-time (T_{ON}) to the default RC time constant across switching devices ($\tau = R_{SW} \cdot C_P$), as mentioned in (2.20)–(2.22).

$$\text{SSC: } T_{ON} > 4 \cdot \tau \quad (2.20)$$

$$\text{Transition: } 0.1 \cdot \tau < T_{ON} < 4 \cdot \tau \quad (2.21)$$

$$\text{FSC: } T_{ON} < 0.1 \cdot \tau \quad (2.22)$$

As mentioned in (2.20), for $T_{ON} > 4 \cdot \tau$, implying more than 98% charge-transfer efficiency, the CP can be interpreted to be operating under deep SSC regime. Similarly, CP operation under FSC can be assumed for $T_{ON} < 0.1 \cdot \tau$, corresponding to under 10% of charge-transfer efficiency. It follows that for the relatively large range of intermediate operating frequencies for which $0.1 \cdot \tau < T_{ON} < 4 \cdot \tau$, the CP can be considered to operating in the transition region between SSC and FSC, in which both R_{CP_SSC} and R_{CP_FSC} have comparable magnitude.

The SSC and FSC operating regimes directly translates into the area-power trade-off, intrinsic to any CP design and optimization process. As clearly established through numerous prior works [7–9], the SSC operation is essential to maximize the CP power efficiency. This hold true since for a given set of design (N, C_P, R_{SW}) and operating (F_{IN}, I_L) parameters, the SSC operation corresponds to minimum output impedance (R_{CP_MIN}) and thus maximum power delivered to the load. For linear CPs, as relevant to this work, this R_{CP_MIN} is as given by (2.23) and the related CP efficiency (for inverting configuration) is re-iterated in (2.24).

$$R_{CP_MIN} = R_{CP_SSC} = \frac{N}{C_P \cdot F_{IN}} \quad (2.23)$$

$$\eta_{MAX} = \frac{(N \cdot |V_{DD}| - I_L \cdot R_{CP_MIN}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{PAR})} \quad (2.24)$$

The relatively low operating frequency (F_{IN}) required for this condition can result in large C_P for a given load requirement, which can lead to higher area utilization. Alternatively or additionally, for the SSC feasibility, the size of CP switches can be increased to lower R_{SW} and thus reduce the associated RC time constant. However this comes at a higher area cost and results in increased parasitics associated with the charge-transfer switches, captured through the factor α_S , as shown in (2.16).

As operating frequency is increased and the CP transitions into FSC region, the CP output impedance is reduced, as illustrated in Fig. Fig. 2.7. However the parasitic power consumption ($V_{DD} \cdot I_{PAR}$) also increases linearly with F_{IN} . In general, the FSC operation is essential to minimum area utilization for a given load current requirement, as it leads to minimum C_P and R_{SW} magnitude required to meet a given R_{CP} specification. From Fig. Fig. 2.7 it can also be observed that as F_{IN} is increased further, the incremental advantage of reducing R_{CP} magnitude is lost as R_{CP} saturates to its asymptomatic bound in FSC region, while the parasitic power loss continues to increase linearly. It thus follows that, in general, for a given set of fixed design parameters (N, C_P, R_{SW}) the optimum area-power trade-off corresponds to the CP operating in transition region between SSC and FSC operating bounds. However, the actual CP operating region can be tailored to the requirements of the end application.

2.3.1.3 SC-CP Design Specification and Optimization Process

For all practical applications implementing, the CP design and optimization is primarily dictated by its design specifications. The CP design specification typically only specify the input voltage magnitude V_{IN} , output voltage magnitude V_{OUT} (or min. V_{OUT} magnitude) for a given load current I_L or for a range of load currents. The main design objective is to meet or exceed the design specifications while maximizing CP FOMs, mainly including the area utilization in terms of the total integrated pump capacitance, and the derived power efficiency for the specified load current range. Alternatively the design effort can be targeted at arriving at the most acceptable trade-off between these CP FOMs, which is suitable for the requirements of the given application.

The first step towards achieving an optimized CP implementation is to decide if the given CP needs to operated in slow-switching (SSC) or fast-switching conditions. As stated earlier, the SSC is essential towards maximizing the attainable CP efficiency, however it can result in significant increase in silicon area in terms of higher pump capacitance size, as required for the given load current requirements. For the CP operation in FSC regime, the driving capacity is higher for a given pump capacitance magnitude (C_P), but the CP output characteristics shows strong

dependence on switch resistance (R_{SW}) and the operating frequency (F_{IN}). In addition, it exhibits greater sensitivity towards the switching parasitics, thus resulting in reduced CP efficiency.

From a circuit designer's prospective the CP optimization variables include: (1) SC-CP topology (2) Number of CP (inverting or boosting) stages N , (3) Pumping capacitance per stage C_P (4) switch resistance R_{SW} , evaluated in terms of switching device size and lastly (5) operating frequency F_{IN} of the CP. In SSC, the typical CP optimization flow is initiated with selecting the appropriate CP topology which is most suitable to meet the requirements of the given application. For instance, the Fibonacci CPs offer the maximum voltage gain for a given number of CP stages, however the effect of CP parasitics increase more rapidly than other CP topologies, as number of CP stages are increased. Therefore, such CPs are employed when a relatively large voltage conversion ratio is desired, while employing less number of CP stages. This selection is followed by evaluating the optimum number of CP stages to achieve the most area or power efficient implementation for the given CP topology. It is to be noted, that this optimum N_{OPT} can be different from the minimum N_{MIN} deduced from the ratio V_{OUT} to V_{IN} , as mentioned in (2.25) and (2.26), for the inverting and boosting configurations.

$$\text{Inverting: } N_{MIN} = \frac{|V_{OUT}|}{V_{IN}} \quad (2.25)$$

$$\text{Boosting: } N_{MIN} = \frac{|V_{OUT}|}{V_{IN}} - 1 \quad (2.26)$$

Finally, for the selected optimum N_{OPT} value, the pump capacitance C_P is evaluated for the given load current specification and an independently selected F_{IN} , which is low enough to ensure CP operation in SSC. This design flow is thus executed under the assumption, that in SSC, the CP output response and efficiency is independent of the R_{SW} and F_{IN} .

For the CP operating in FSC regime, the optimization involves deriving the CP output in terms of its output impedance R_{CP} , which itself captures the combined effect of all the design and operating parameters including R_{SW} and F_{IN} . In this work, a novel operation analysis, deriving the CP output impedance function for an integrated CP structure operated under strong FSC regime, is proposed and

elaborated in chapter 3.

2.3.2 Operational Analysis of SC-CP

In past, the SC-CP operation has been rigorously analyzed [7,8,10–13] to accurately predict the CP initial transients and its steady-state response, for a given set of design parameters (CP topology, N , C_P , C_L) and specified operating conditions for load current and switching frequency. Such analyses is also utilized to achieve most optimized SC-CP implementation for given set of design specifications, while also assist in understanding the theoretical limits of a given CP topology in terms of CP FOMs.

The general principle followed for such analysis is to derive an equivalent CP circuit model obtained by replacing the switching devices with an ideal switch, and including the parasitic capacitance on each integrated capacitance, as was shown earlier in Fig. 2.6. In this section, we present a brief overview of two such CP analytical model, which provide the tools and techniques that can be used analyze and optimize both linear and non-linear integrated CP architectures.

For a given set of design specifications, the results obtained from the different proposed analytical approaches [7,8,11,12], can be closely co-related in terms of no. CP stages N and pump capacitance per stage. However the same can vary slightly based on the given CP topology, its equivalent circuit model, the assumptions used in the analysis (effect of R_{SW}/F_{IN} ignored for SSC) and parasitic effects ignored or incorporated in the given CP analysis.

2.3.2.1 Simplified Linear Model

The CP operational analysis presented in [7,8] provides a simplified technique for area and power efficiency optimization of linear SC-CP implementations such as. In the given approach, firstly the optimum number of CP stages for most area/power efficient implementation is derived, and the result is then used for subsequent evaluation of required C_P per stage for the given load current requirement. Assuming the CP operation in SSC regime, the effect of R_{SW} and F_{IN} on the CP transfer characteristics is neglected and only the effect bottom plate C_{PAR} is taken into consideration. The equivalent circuit model is therefore same as presented in Fig. 2.6,

with the exclusion of top plate C_{PAR} . The optimization methodology proposed in, can be readily extended to inverting CP configurations, as briefly described here and the resulting expressions for optimum CP stages are used as first estimate for the design of negative voltage CP used in this work.

Considering the CP input voltage V_{IN} equal to the input switching signal amplitude, and reusing the results derived in section 2.2.2, the CP output magnitude for any linear SC-CP implementation, operating in SSC regime, can be derived in terms of the load current, as given by (2.11), and re-presented here in (2.27) for convenience.

$$|V_{OUT}| = N \cdot V_{DD} - N \cdot \frac{I_L \cdot T_{PRD}}{C_P} \quad (2.27)$$

Rearranging (2.27), the expression for C_P is given by (2.28).

$$C_P = \frac{N \cdot I_L \cdot T_{PRD}}{N \cdot V_{DD} - |V_{OUT}|} \quad (2.28)$$

The total area utilization can be considered proportion to the total integrated pump capacitance $N \cdot C_P$, as given by (2.29).

$$A_{TOT} = k \cdot N \cdot C_P \quad (2.29)$$

where k is a technology dependent process parameter. The load capacitor C_L is not included in (2.29), since it is employed used to limit the CP ripple and can thus be varied based on a given design's tolerance to output ripple as seen at maximum load current setting. Using (2.28) in (2.29), and setting $(dA_{TOT}/dN) = 0$, the expression for the optimum number of CP stages for area efficient implementation (N_{Area}) can thus be derived, as mentioned in (2.30).

$$N_{Area} = \frac{|V_{OUT}|}{V_{DD}} \quad (2.30)$$

For a SC-CP operating under SSC regime, the total power-loss (P_L) is primarily contributed by the periodic charging discharging of the bottom-plate parasitic ca-

pacitance (C_{PAR_BOT}) as given by (2.31).

$$P_L = I_{PAR} \cdot V_{DD} = N \cdot C_{PAR_BOT} \cdot V_{DD}^2 \cdot F_{IN} \quad (2.31)$$

$$\Rightarrow I_{PAR} = N \cdot (\alpha \cdot C_P) \cdot V_{DD} \cdot F_{IN} \quad (2.32)$$

where I_{PAR} is resulting parasitic current and $\alpha = (C_{PAR_BOT}/C_P)$ is the bottom-plate parasitic capacitance coefficient. For any linear N-stage SC-CP, the total current drawn from the supply is as mentioned in (2.33)

$$I_{VDD} = N \cdot I_L + I_{PAR} \quad (2.33)$$

Using (2.28) in (2.32) and re-inserting in (2.33), the total drawn current from supply (I_{VDD}) can be expressed in terms of load current and technology dependent parameters α , as mentioned in (2.34).

$$I_{VDD} = \left[N + \frac{\alpha N^2 V_{DD}}{N \cdot V_{DD} - |V_{OUT}|} \right] \cdot I_L \quad (2.34)$$

The I_{VDD} expression in (2.34) can be minimized by setting $(dI_{VDD}/dN) = 0$, to yield the resulting expression for optimum number of CP stages for most power-efficient implementation (N_{Eff}), as derived in (2.35).

$$N_{Eff} = \frac{|V_{OUT}|}{V_{DD}} \left(1 + \sqrt{\frac{\alpha}{1 + \alpha}} \right) \quad (2.35)$$

It is worth noting that the optimum value of N-stages (N_{Area} or N_{Eff}) is independent of load current I_L and operating frequency F_{IN} and is only determined by the ratio of required CP output voltage magnitude ($|V_{OUT}|$) to input voltage magnitude (V_{DD}), and the process dependent parameter α . The selected N value is re-inserted in (2.20) to estimate pump-capacitance C_P per stage, for a given load current I_L specification as required for a given application. As stated before, the operating frequency can be selected independently, given that the on-time of the switches is sufficiently larger than the default RC time constant ($R_{SW} \cdot C_P$), such that the CP operation under SSC regime is ensured.

Fig. 2.8: Two-Port analytical model for SC-CP Operational analysis

2.3.2.2 Two-port Charge-Pump Model

The work in [12], presents a more generic optimization methodology obtained through a unique representation the SC-CP as a 2-port circuit element. The analysis is specifically applied for power efficiency optimization within the constraints of a given set of design specifications. It can be utilized for both linear and non-linear CP typologies by taking into account the differences arising from various CP topologies and incorporating the effect of both top and bottom plate parasitics on the CP output response.

Utilizing the fact that once the steady-state is attained, the average CP output voltage and the input current drawn from the supply is in equilibrium with the input parameters, then any SC-CP can be represented using a 2-port model, as shown in Fig. 2.8.

The independent input parameter are the CP input voltage v_{in} and the load current i_l as given by the design specifications, and the dependent output parameters are the CP output voltage v_{out} and the total input current drawn i_{in} from the supply. The corresponding pair of charge-transfer equations as derived from this 2-port model are as mentioned in (2.36), (2.37).

$$i_{in} = G_{in} \cdot [v_{in}] + A \cdot [i_l] \quad (2.36)$$

$$v_{out} = A \cdot [v_{in}] - R_{out} \cdot [i_l] \quad (2.37)$$

The terms G_{in} and R_{out} denote the input conductance and output impedance of the CP, while the term A represent the nominal gain offered by the given CP topology. It is to be noted that the model assigns same gain A for the the input current i_{in}

with respect to load current i_l , and for the the output voltage v_{out} with respect to the input voltage v_{in} , as is the case for the actual CP implementation and as observed from equations (2.11) and (2.23).

The CP power efficiency η , defined as the ratio of power delivered (P_{out}) to the power consumed (P_{in}) by CP, can be expressed in terms of CP transfer parameters: A , G_{in} and R_{out} using (2.36) and 2.37), as given by (2.38).

$$\eta_{Eff} = \frac{P_{out}}{P_{in}} = \frac{A v_{in} i_l - R_{out} i_l^2}{G_{in} v_{in}^2 + A v_{in} i_l} \quad (2.38)$$

Using i_l from (2.36) in (2.38), the CP efficiency can be obtained in terms of ratio of output to input voltage (v_{out}/v_{in}), as mentioned in (2.39).

$$\eta_{Eff} = \frac{v_{out}/v_{in}}{A + (G_{in} R_{out}/A) - (v_{out}/v_{in})} \quad (2.39)$$

The gain term A only depends on only the CP topology and the number of CP stages N , whereas the CP output impedance R_{out} and the input conductance G_{in} are a function of N based on the CP topology and also vary with both the operating frequency F_{IN} and size of pump-capacitance C_P . Specifically, for any CP topology (in SSC regime) R_{OUT} decreases with the increase in operating frequency or with the increase in pump capacitance magnitude. In contrast G_{in} can be considered directly proportional to both F_{IN} and C_P magnitude. Therefore, R_{out} and G_{in} can be normalized to the product of $(F_{IN} \cdot C_P)$ as shown by (2.40) and (2.41).

$$R_{out} = \frac{r_{out}(N, \alpha, \beta)}{F_{IN} \cdot C_P} \quad (2.40)$$

$$G_{in} = g_{in}(N, \alpha, \beta) \cdot (F_{IN} \cdot C_P) \quad (2.41)$$

The terms r_{out} and g_{in} represents the fundamental input conductance and the output impedance of a given CP topology that are independent of both operating frequency and the pump capacitance magnitude . Thus for a given CP architecture, the terms A , r_{out} and g_{in} can be evaluated as function of N and the the top and bottom plate parasitic coefficients β and α , respectively. For instance, for linear CP implementation, the nominal gain A_{lin} , output impedance $r_{out.lin}$ and input conductance $g_{in.lin}$ have been analyzed in [4, 10], and the corresponding expression for these terms are

evaluated, as mentioned in (2.42) - (2.44).

$$A_{lin} = \frac{N}{1 + \beta} + 1 \quad (2.42)$$

$$r_{out,lin} = \frac{N^2}{1 + \beta} \quad (2.43)$$

$$g_{in,lin} = \frac{\alpha + \beta\alpha\beta}{1 + \beta} \quad (2.44)$$

Now using (2.40) and (2.41) in (2.39), the CP efficiency in terms of A , r_{out} and g_{in} , can be obtained as mentioned in (2.45).

$$\eta_{Eff} = \frac{v_{out}/v_{in}}{A + (g_{in} r_{out}/A) - (v_{out}/v_{in})} \quad (2.45)$$

Since the product term $F_{IN} \cdot C_P$ cancel out from the the product of $R_{out} \cdot G_{in}$ in (2.30), the resulting efficiency expression in (2.36) can be verified to be independent of both the operating frequency and pump capacitance magnitude. The power efficiency expression in (2.36) can now be minimized, to obtain the optimum number of CP stages for maximum efficiency implementation, in presence of finite top and bottom plate parasitics. The optimum N value is re-inserted in (2.34), and by using (2.28) and (2.34) in (2.31), the pump-capacitance per stage can be estimated for any given operating frequency.

2.3.2.3 Limitations of Existing SC-CP Models

The currently available SC-CP models have helped to acquire a deep understanding of the CP operation that can be utilized to obtain an optimized CP implementation for various CP topologies and for varying set of design specifications. However the existing SC-CP models, such as the ones elaborated in the previous sections, are largely based on the CP operation in SSC regime. This implies that these models do not incorporate the effect of (i) non-zero switch resistance R_{SW} of charge-transfer switches and (ii) finite on-time of the switches T_{ON} , which can be well below the RC time constant ($\tau = R_{SW} \cdot C_P$) of typical charge-transfer occurring in the steady-state CP operation.

It is to be noted that the SSC cannot be readily assured for any SC-CP implementation, optimized within the constraints of a given set design specification,

Moreover, there exists an inherent trade-off between driving capacity, and CP operation within SSC regime. For instance, assuming CP is initially operated in SSC, if the CP is now required to support a higher load current, either of the two approaches can be followed: (i) Operating frequency F_{IN} is increased, leading to lower on-time of the switches. (ii) Pump capacitance C_P magnitude is increased, which significantly increases the CP area utilization besides the increase in the RC time constant of the charge-transfer across switches.

In either case the ratio of switch on-time to the RC time constant T_{ON}/τ is increased, which forces the CP to operate outside SSC. To facilitate CP operation in SSC, the switch-resistance R_{SW} can be reduced by utilizing larger sized switches, however, at relatively high load currents, it can lead to very large switching devices, especially for integrated CPs, which are usually implemented within tight constraints of area utilization. Moreover, such approach also results in a proportional increase in parasitics associated with the switching devices, which further contributes towards CP performance degradation.

Another major limitation of the proposed SC-CP is that certain deductions obtained from the related analysis does not agree with the corresponding circuit level CP implementation. This contradiction is apparent if a real switch (with finite switch resistance) is used in CP equivalent model, even though the CP operation in SSC is ensured. For instance, in [7, 8], the assumption of an ideal switching characteristic ($R_{SW} = 0$), leads to an oversimplified prediction of CP output impedance ($R_{CP} \approx (N \cdot T_{PRD})/C_P$), as mentioned in (2.12). This leads to a rather imprecise deduction for the additional current term I_{PAR} , considering it to be directly proportional to the load current I_L and independent of the operating frequency $F_{IN}(= 1/T_{PRD})$. However, for transistor level CP implementations, I_{PAR} is observed to be almost independent of the load and strictly linear with the F_{IN} .

A detailed analysis of the linear CP transfer characteristics for linear CPs, incorporating the effect of both top and bottom plate parasitic capacitance, is presented [9]. In this work, accurate closed-form expressions for both CP output (V_{CP}) and efficiency (η) are derived and the efficiency function is maximized in terms of a single optimization variable $\delta (= \frac{I_L}{F_{IN} \cdot C_P \cdot V_{IN}})$, which relates pump-capacitance (C_P), load current (I_L) and operating frequency (F_{IN}) while assuming number of stages

(N) is fixed. The suggested constrained optimization strategy for the practical case in which the final conversion ratio ($M = |V_{OUT}|/V_{IN}$) is fixed, is identical to [7, 8], whereby the first step is to derive the optimum number of CP stages (N_{OPT}), followed by selection of F_{IN} and derivation of C_P , for a given load current. In this work, although accurate formulations of V_{CP} and η are presented, the results are not linked to actual circuit level implementation using MOS transistor as switches. An estimation of the assumed switch resistance and the corresponding aspect ratio of MOS device is also not discussed. In addition, the power loss in driving the switches is also not included in the efficiency computation and optimization. Moreover, like [7, 8], the scope of this work is limited to CP operation under SSC regime.

The classic work in [6] presents a detailed analysis on the evaluation of CP output impedance in both SSC and FSC domain while also suggesting an optimization strategy for a given area budget, in terms of total pump-capacitance or total power loss across switches. The results can be utilized for any CP topology through the evaluation of its corresponding state charge vectors or switch resistance vectors. In addition, the work also elegantly highlights the difference across various equivalent SC-CP topologies, clearly establishing that linear CPs are best suited for integrated CP implementation operating under FSC regime. However, in this work the parasitic capacitance losses, which are crucial in determining the CP transfer characteristics and efficiency, are not considered in the analysis. Moreover, in FSC condition, only switch resistance losses are considered while assuming the capacitor state voltage to be constant. This assumption cannot be substantiated since the capacitance node voltage change is required to ensure finite unidirectional transfer of charge. This leads to inaccuracy in the evaluation of R_{CP} at high switching frequencies.

In [12], the CP model is more involved, correctly capturing the effect of CP operating frequency on the input power consumption and CP output impedance R_{out} . However, the proposed 2-port CP model, inherently involves a number of assumptions, which cannot be substantiated universally. Firstly, the current gain and the voltage gain are assumed to exactly the same, which may not be the case, as observed from circuit simulations. Secondly, the input current is considered to be linearly related to the CP input voltage ($i_{in} = G_{in} \cdot v_{in}$), which is also not consistent

with its circuit counterpart. Lastly, the model presumes directly linear and inversely linear proportionality of input conductance and output impedance with respect to total integrated pump capacitance $N \cdot C_P$, as mentioned in (2.31) and (2.32). In this regard, even though the trend of variation of R_{out} and G_{in} with respect to C_P is correct, the actual R_{out} and G_{in} variation as a function of C_P is not identical with this simplified approximation.

To address the current limitations of the existing SC-CP models, in this work, a new CP model, invariant to the CP operating regions (SSC or FSC), is proposed in Chapter 4. The given model incorporating the effect of non-zero switch-resistances and finite on-time of the switches, closely mimics the actual circuit level operation, and thus facilitates a more generic CP operational analysis.

2.4 Fully-Integrated Linear Charge-Pump Implementations

This section briefly introduces some of the most well-known and widely utilized fully-integrated linear SC-CP topologies including the Dickson-CP [4, 14], Latched CP [15, 16] and the Bootstrap CP [17, 18] topologies. Apart from the standard linear SC-CPs, a variant of the full-integrated SC-CPs involving non-linear transfer of charge, such as the Fibonacci CP [5] and the exponential CP [19] implementations, have also been explored and analyzed in previous works. Such non-linear CP implementation have the advantage of providing the highest voltage gain for a given number of stages and can also be operated with simple 2-phase switching input, thus resulting in higher efficiency. However, relative to other SC-CP structures, the effect of parasitics on the CP performance is more pronounced and the parasitic losses tend to add very rapidly with addition of CP stages. Moreover, as shown from extensive prior CP analysis [6], [9] the linear CPs are the best candidate for fully-integrated SC-CP implementations, in terms of both area and power efficiency. Therefore, scope of review of fully-integrated CPs is only limited to linear CP implementations, as relevant for the design of negative voltage CP used in this work.

For a given SC-CP implementation, firstly the CP operation is discussed qualitatively by elaborating on the charge-transfer mechanism as implemented at the

device level. This is followed by a brief review on the merits and shortcomings of each CP structure, which is useful in determining its possible application space. Finally, the CP output response and the related performance metrics are compared across two equivalent (same N and C_P) linear fully-integrated CP structures, thus highlighting the difference arising solely due to the topological factors related to a SC-CP implementation.

2.4.1 Dickson Charge-Pump

The Dickson charge-pump represents the first integrated implementation of switched-capacitor based voltage-multiplier circuit. A diode based implementation of this structure, in inverting configuration is as shown in Fig. 2.9. An N -stage CP is a cascade of N -inverting stages and one output stage, with inverting stage comprising of a diode and pump capacitance pair, as marked in Fig. 2.9.

As briefly elaborated earlier in section 2.2.2, the CP operates by implementing unidirectional transfer of charge through the integrated diode devices, which restrict the flow of negative charge towards input, while providing a low-resistance path towards output. In Fig. 2.9, in the positive phase of CLK, diode $D1$ is forward biased, and therefore node 1 acquires a voltage equal to the forward voltage drop ($V_{FD} \approx 0.7V$) of the diode. In the following phase, as CLK goes low, node 1 is pulled down by approximately the switching signal amplitude, thus turning off $D1$ and turning on diode $D2$. Consequently, the negative voltage generated at node 1 is isolated from the gnd node, while it is connected to node 2, with its corresponding clock input in the positive phase. The cycle repeats across each pair of CP node voltages and as charge is pumped across each inverting stages, the average node voltage magnitude increases proportionally to the input switching amplitude. The increase in node voltage magnitude $|\Delta V_n|$ at the switching instant (with its corresponding clock in low phase) can be represented using (2.46)-(2.47).

$$|\Delta V_n| = V_{DD} \cdot \gamma \quad (2.46)$$

$$\gamma = \frac{C_{PAR}}{C_{PAR} + C_P} \quad (2.47)$$

where the supply voltage V_{DD} represents the switching signal amplitude and the pro-

Fig. 2.9: N-stage Dickson charge-pump using PMOS diode connected switches

cess dependent parameter γ model the loss due to the top and bottom plate parasitic capacitance C_{PAR} included with the integrated pump capacitance C_P . Considering a fixed diode voltage drop of V_{FD} across N-stages, and accounting for the loss of charge due to parasitic capacitance, the simplified CP linear model presented in (2.11), can be modified for Dickson CP structure as shown in (2.48).

$$|V_{OUT}| = N \cdot (V_{DD} \cdot \gamma - V_{FD}) - I_L \cdot R_{CP} \quad (2.48)$$

The given CP structure, utilizing standard p-n junction diodes and a simple 2-phase switching inputs can be readily implemented with large number of charge-pumping stages. Due to its relatively simple implementation, it has been widely employed for high magnitude voltage generation for flash EEPROM and other integrated circuits. However, as seen from (2.411) the major bottleneck associated with it's implementation arises due to diode forward voltage drop, which can lead to significant reduction in CP output magnitude $|V_{OUT}|$, especially at low supply inputs. To enhance the compatibility with standard CMOS process, a variant of this CP utilizing diode connected MOS switches has also been proposed [14]. The inverting configuration of such a CP, employing PMOS switches, is as depicted in Fig. 2.9. In this modified implementation, although the diode voltage drop is avoided, a similar limitation arises due to the threshold voltage (V_{TH}) drop of MOS devices, whereby a given MOS device is only turned for the duration for which its respective source-gate potential is higher than its respective V_{TH} . Another major limitation arise due to the increase in V_{TH} of theses device due to the body effect. The V_{TH} of MOS devices steadily increases with each additional CP stage, as their respective source-body potential is increased. This leads to saturation of CP output voltage magnitude as number of CP stages are increased. It is worth noting that

due to the given CP operation, the realization of MOS devices in isolated well, with locally connected source-body junction, is not feasible, and therefore the loss due to body-effect cannot be avoided. Due to such practical implementation and the resulting high switching losses, such CP topologies are not suitable for low input supply voltages and are therefore no longer implemented in current systems and applications.

2.4.2 Latched Charge-Pump

The cross-coupled or the latched CP is also one of the widely utilized linear SC-CPs topologies, often adapted due to its high power efficiency [15], [16]. The inverting configuration implementation of the same with N-stages is as depicted in the Fig. 2.10. Each CP stage comprises of two complimentary pair of mosfets switches in crossed wire configuration as that implemented in a latch cell. The pump capacitance per stage is split into two halves each driven by complimentary phases of input switching signal. The tied up sources of the first pair serve as the input node while the output is derived from the common source terminal of the complimentary pair. Since the input and output are embedded within each CP stage, the N-stage configuration is simple cascade N such CP stages.

For the inverting configuration, the input pair of the first CP stages are the PMOS devices P_0 and P_1 with their respective source terminals tied to gnd, while the output derived from the common source of the NMOS device N_0 and N_1 , serves as the input for the following CP stage. In the positive phase of the CLK, node V_{1A} is pulled down, thus turning on PMOS P_1 and forcing gnd potential at node V_{1B} . In the next phase, as CLK goes low, node V_{1B} is pulled to negative voltage proportional to input switching amplitude ($V_{DD} \cdot \gamma$), thereby turning on PMOS P_0 and thus forcing gnd potential at node V_{1A} . The opposite phase of node voltages V_{1A}/V_{1B} oscillating between gnd (0V) and $-V_{DD} \cdot \gamma$, alternatively turn on NMOS devices N_0 and N_1 to transmit the negative voltage generated at the intermediate nodes to output.

The given CP topology utilizes the simplest 2-phase clocking inputs and the crossed configuration maintains large overdrive potential across switching device, thus turning them on completely and reducing the effective switch resistance en-

Fig. 2.10: N-stage Latched charge-pump

countered in the charge-transfer process. Thus, for a given C_P magnitude and operating frequency F_{IN} , the latched CP offers the lowest output impedance R_{CP} of any other SC-CP structure, thus resulting in higher driving capacity and improved area and power efficiency for the overall implementation.

However, it should be noted that each CP stage requires 4 large charge-transfer switches as compared to one main switching device for bootstrap configuration. Moreover, for the inverting configuration, the nwell of the PMOS devices is tied to gnd to prevent possible forward biasing p-substrate to nwell p-n junction diode, even if the common p-substrate is tied to the output of the CP as the contact for most negative potential of the circuit. This results in the familiar V_{TH} degradation along CP stages due to body effect, and therefore somewhat restricts utilization of this circuit when large no. of CP stages are required.

2.4.3 Bootstrap Charge-Pump

The bootstrap CP is a widely employed SC-CP topology that can be implemented with a large number of CP stages, thus generating high voltage magnitude in both inverting and boosting configurations. It was first introduced in [17], as an integrated negative voltage source, facilitating low-voltage erase operating in Flash EEPROM memory applications. In its early implementation, it utilized PMOS devices for inverting configuration which resulted in the increase in the threshold voltage V_{TH} of these device due to the body effect, similar to that encountered for the Dickson CP topology. To avoid such losses, a variant of this CP using deep-n-well devices was proposed in [18], as shown in Fig. 2.11(a).

Fig. 2.11: (a) N-stage Bootstrap charge-pump using deep-n-well devices (b) 4-phase switching input

Similar to the Dickson CP structure, the N-stage implementation consists of a cascade of N inverting stages followed by one output stage. The CP inverting stage, as highlighted in Fig. 2.11(a), comprises of charge-transfer switch (SW_{nA}), a bootstrap switch (SW_{nB}) connecting the source-gate terminals of the main switching device, a pump capacitor C_P and a small gate capacitor C_G connected directly to the gate of charge-transfer switch. The output stage is identical to the the inverting stage with the exclusion of pump capacitor. The 4-phase input switching sequence as required for the CP operation is as seen from Fig. 2.11(b), where CLK-1A and CLK-2A drive the large charge-pumping capacitor and CLK-1B and CLK-2B are used to turn on the respective switching devices SW_{NB} , through C_G , during the charge-transfer phase.

For a given i^{th} inverting stage, when the switching input driving the pump capacitor C_{Pi} is in positive phase, the bootstrap switches in the following and preceding stages are turned on, thereby turning off their respective charge-transfers switches. This is followed by low phase transition of the complimentary clock input driving the pump capacitor in the $i - 1^{th}$ stage, which pulls down the node voltage V_{i-1} and

results in the bootstrap switch (SW_{iB}) in the i^{th} stage being turned off. Finally the charge-transfer switch SW_i stage is turned on through the positive transition of the clock input connected to its corresponding gate capacitor C_{Gi} , allowing negative charge transfer across its source-drain terminals. In this way the negative voltage generated at node voltage V_{i-1} is connected to V_i through SW_i while it remains isolated from V_{i-2} by maintaining SW_{i-1} turned off. In the next phase of the same period, the other set of charge-transfer switches ($SW_{i-1}, SW_{i-3}, \dots, SW_{i+1}, SW_{i+3} \dots$) driven by complimentary clock input signal are turned on, such that each charge-transfer switch is tuned on once every period, for a duration T_{ON} , less than half of time period T_{PRD} of the input switching signal, as shown in Fig. 2.11(b). Thus the CP operates by restricting the direction of negative charge transfer towards output load capacitor, resulting in boosting of average node voltage magnitude as charges are pumped across across its inverting stages.

The bootstrap CP does not have the lowest output impedance per unit pump-capacitance magnitude C_P and input switching frequency F_{IN} ($R_{CP}/C_P \cdot F_{IN}$), and requires a 4-phase switching input, which adds complexity to the overall implementation. However, the switching scheme ensures that the switching devices are turned on completely during the charge-transfer phase. This reduces the effective switch resistance, thus facilitating its design for moderate driving capacity applications with optimal area utilization. Moreover its inverting configuration implemented using deep-n-well NMOS switches, with local source-body contact, does not suffer from V_{TH} degradation along CP cascaded stages and therefore is better suited for negative voltage generation.

2.5 Performance Comparison Across Linear Charge-Pump Topologies

In this section, we present a performance comparison analysis of two most widely adopted linear CP topologies namely the Latched or the Cross-coupled pair CP and the Bootstrap CP. The analysis also forms the basis for the selection of the negative voltage CP used in the design of the proposed low-noise negative voltage generator system. For the purposes of the comparison, 2-stage and 4-stage implementations

with same pump capacitance magnitude per stage are utilized for the two CP structures. Furthermore, to make an accurate comparison, similar area utilization is ensured by maintaining the total width of CMOS devices per inverting stage, same across the two CP topologies. Thus the total width of switching devices in Bootstrap CP, including the main deep-n-well charge transfer switch and the smaller Bootstrap switch, is evenly distributed across the PMOS and NMOS pairs of the Latched CP's inverting cell, with PMOS devices sized twice the NMOS counterparts, due to their lower transconductance.

The other CP design and operating parameters kept common across the two CP topologies, are as listed in Table 2.3.

Table 2.3: CP Design and Operating parameters utilized for performance comparison

	Parameters	Value
Design Parameters	No. of CP stages	2-stg./4-stg
	Pump Cap. per stage (C_P)	15pF
	CP Switch dimension ($(W/L)_{Tot}$) per stage	11.25 μ /0.6 μ
Operating Parameters	V_{IN}	3.3V
	Operating Frequency	50MHz
	Load Current	0 to 1mA

The CP performance metrics selected for the comparison are the CP output voltage and power efficiency across load current, for the fixed operating frequency of 50MHz. The selected F_{IN} is high enough to ensure CP operation in FSC regime, thus the results drawn from the analysis are applicable to generic SC-CP operation. The CP output versus load current curve is used to extract its equivalent linear model expressions as given by, and thus estimate CP output at no-load and its output impedance. The CP power efficiency results includes the power consumed in the multi-phase (2-phase/4-phase) switching signal generators and buffer cell employed for driving large capacitive loads within CP, thereby capturing a realistic picture of actual CP operation. The results presented henceforth are obtained using the SPICE simulations for the two CPs implemented in CMOS 180nm technology node using GlobalFoundries BCDlite process.

For the 2-stage implementation, the CP output voltage and power-efficiency variation with respect to load current is as shown in the Figs. 2.12(a) and 2.12(b), respectively. The linear interpolation of the CP output response as shown by the

Fig. 2.12: 2-stage SC-CP (a) Output voltage (b) Power-efficiency versus load current

dotted line and the corresponding linear model is also depicted in the Fig. 2.12(a) alongside. It can be observed that the CP output magnitude at no-load is higher for Latched CP, while CP output impedance is slightly lower for the Bootstrap 2-stage implementation. In general, CP output magnitude remains higher for the Latched CP till -2.5V, beyond which the Bootstrap CP V_{OUT} magnitude cross-over to exceed the Latched CP V_{OUT} , due to its lower R_{CP} . The power efficiency of Latched CP is significantly higher than its counterpart across the entire load current range, with peak CP efficiency as high as 47% at $560\mu A$. The substantial difference in the power efficiency levels of the two CPs arises primarily due to significant power consumed in the 4-phase clock generator circuit generating the required 4-phase periodic input for the Bootstrap CP, as compared to minimal power expended in generating simple 2-phase input required for the Latched CP. It is to be noted that almost same amount of power is consumed in the equal sized buffer cells driving the same magnitude of pump capacitance in the two CPs, however for the Bootstrap CP, additional power is consumed in driving the other two phases of input signal connected used to drive the small gate capacitance of charge-transfer switches. Moreover, higher CP magnitude for Latched structure also contributes towards its higher efficiency.

The equivalent performance characterization curves for the 4-stage implementation are presented in Figs. 2.13(a) and 2.13(b). A comparison with 2-stage implementation indicates that output impedance has increased substantially due to

Fig. 2.13: 4-stage SC-CP (a) Output voltage (b) Power-efficiency versus load current

higher switching losses encountered due to additional CP stages. The main difference for this case is that the Latched CP output impedance is substantially higher than Bootstrap CP, which results in higher CP magnitude for the latter, for almost the entire load current range. This difference arises due to the stronger effect of the body-effect for the 4-stage implementation, whereby for the inverting configuration implementation of the Latched CP, the threshold voltage of the input PMOS devices increases along the cascaded CP stages due to increase in their respective source-body potential. It is to be noted that in spite of the lower CP output magnitude for the Latched CP, its power efficiency still exceeds its Bootstrap counterpart, although the difference in the power efficiency level for the two topologies is reduced from that occurring for their respective 2-stage implementations. This is again due to the significantly lower power consumed in the simple 2-phase signal generation and lesser number of buffer cells required for Latched CP. The average and peak power efficiency of Bootstrap CP in this case is higher as compared to 2-stage variant, since the increase in its CP output magnitude is higher than the corresponding increment in the parasitic current consumption arising from driving a higher total pump capacitance.

In summary, it can be concluded that the Latched CP is clearly a more power efficient topology and relatively easier to implement due to a simpler switching scheme. However its implementation as an inverting CP is somewhat restricted due

to 'body-effect', which increases progressively and substantially with the addition of CP stages. In contrast, the Bootstrap CP employing only deep-n-well switches, with local source-body contact does not suffer from body-effect. Therefore it can be regarded as well suited for negative voltage generation, however it does not lend itself as the most power efficient implementation. It can be added that the Bootstrap CP efficiency can be enhanced further by optimizing the multi-phase clock generator and buffer cells for minimal internal power consumption along with the optimization main CP cell to achieve the lowest output impedance.

2.6 Chapter Summary

This chapter presented a detailed review of the design, operational analysis and optimization strategies employed for the fully-integrated switched-capacitor charge-pumps (SC-CP). In this chapter, firstly, the SC-CP design and operating parameters were identified, along with a brief description of the key CP performance indicators. Following this, the SC-CP's different operating regimes (slow switching (SSC) and fast-switching (FSC) conditions) were defined and the general optimization sequence followed for deriving the CP design parameters is described.

This is followed by a detailed review of the known CP analytical techniques which have been used for the fully-integrated SC-CP operational analysis and optimization of CP's Area and power-efficiency. The limitation of the existing analytical models, in terms of their application for generic the SC-CP operation is clearly highlighted.

Finally, the design and operation of some of the well-known and widely-utilized fully-integrated CP topologies is described. In order to clearly highlight the impact of CP architecture, two equivalent (same no. of stages and pumping capacitance per stage), fully-integrated, linear SC-CP structures (Latched CP and Bootstrap CP) are implemented and their performance is contrasted based on their corresponding simulation results.

The analysis and results presented in this chapter are also utilized in selection of appropriate CP topology and also to derive the initial estimate of the number of CP stages, for the required inverting SC-CP, used in the given design.

Chapter 3

Review of Regulation Techniques for SC-CPs

3.1 Introduction

The SC-CP output is characterized with large steady-state ripple and high noise-content. Furthermore, the steady-state ripple magnitude and the noise power increases proportional with the total current injected into the CP output node. In addition, the fully-integrated SC-CP implementation results in high-output impedance ($R_{CP} \approx 1k\Omega$ to $10k\Omega$) in its linear transfer response, thus resulting in large variation in the CP output magnitude with input load current. Thus, the CP output necessarily requires some form of post-regulation, before it can be utilized for multiple applications. In this regard, a number of regulation techniques have been proposed earlier, and are designed to deliver a specific performance for the regulated output as dictated by the requirements of the end application. In this chapter we will review some of such known regulation techniques that have been utilized to derive the required regulated negative voltage output from a fully-integrated negative voltage CP.

Similar to a SC-CP implementation, the regulator performance can be analyzed on the basis of certain FOMs set for both, the stand-alone regulator modules and its performance at the system level. In the following section, we first identify and elaborate on the key performance metrics which form the basis of the qualitative and quantitative analysis of the regulator operation. This is followed by a detailed

review of three broad categories of regulation strategies that have been adopted for the obtaining the regulated negative voltage output.

To provide and coherent quantitative analysis, each regulation technique is explained by means of an application circuit, implemented in the same technology node (GF CMOS 180nm BCDlite process) as utilized for the proposed NVG. The performance of test circuits is evaluated with actual 2-stage bootstrap CP (or its equivalent linear model) as employed in the final NVG system implementation. In addition, the regulator sub-circuits including OTA and Bias-gen are re-utilized, in order to facilitate an accurate comparison among various techniques. This is followed by a detailed analysis of the key advantages and major drawback associated with each technique. Lastly, various regulation techniques are compared with respect to the established regulator FOMs and the basis of selection of linear regulator approach for proposed NVG is highlighted.

3.2 Figure-of-Merits for Regulator Performance Evaluation

The performance of the regulated output voltage determines its suitability for a particular application and therefore aids with selection of appropriate regulation technique. Although the operating conditions such as regulated voltage magnitude, load current, supply input etc. can widely vary across various implementations, the overall regulator performance can still be bench marked against a common set of FOMs. The key performance metrics quantifying the regulator operation, can be broadly classified into two categories, including, firstly, the performance indicators for the stand-alone regulator module, and secondly, the system level performance indicators, determined for a given combination of SC-CP and regulator implementation.

As stated, the regulator specific performance parameters are independent of the SC-CP implementation and therefore, if required, they are evaluated assuming an ideal CP input. These can be identified and explained as follows:

1. **Regulation Accuracy:** This is evaluated in terms of the percentage drift in the regulated output voltage magnitude in response to a given variation in the

unregulated input voltage or across the supported load current range. The former is termed as line regulation and the latter as load regulation, and can be expressed as in (3.1), (3.2).

$$LineRegualtion : \frac{\Delta V_{REG}}{\Delta V_{IN}} * 100\% \quad (3.1)$$

$$LoadRegualtion : \frac{\Delta V_{REG}}{\Delta I_L} * 100\% \quad (3.2)$$

where ΔV_{IN} and ΔI_L denotes the total change in input voltage and load current respectively, and ΔV_{IN} represent the resulting change in regulated output voltage.

2. Power consumption: This is the power consumed by the stand-alone regulator module. At low-loads when the regulator quiescent current is lower or comparable to the load current, it can have sizable contribution towards reduction of system efficiency.

4. Area utilization: This refers to the silicon area required for the integrated implementation of a given regulator topology.

3. Off-chip components: This refers to the number of off-chip components including capacitors, feedback resistor-dividers etc. required for a given regulator implementation.

The other performance parameters for the regulated output are determined by both (1) the transfer characteristics of SC-CP and (2) the response of the regulator module. These implementation-specific performance parameters are listed and elaborated as follow:

1. Maximum load current: This is maximum load current supported for a given regulated output voltage. In this case, the regulated output is fixed, and load current is varied to identify the maximum allowed load for which the output is regulated. The load current variation results in wide variation in the unregulated CP output magnitude due to relatively high output impedance of the SC-CP. Thus, this parameter is strongly dependent on the CP output transfer characteristics, besides the given regulator specifications.

2. Output Tuning Range: This is the total available output voltage range for the regulated output for a given maximum load current specification. In the case, the load current is fixed and the regulated output is varied to identify the range of

regulated output magnitude across which the regulation remains effective. The fixed load current, also fixes the unregulated CP output magnitude provided as input to the regulator input, and determines the lower bound of the regulated output, along with regulator specification. The upper bound of the regulation is determined by the regulator topology itself. Thus, it can also be regarded as dependent on the CP output response with respect to input load current, as captured by its extracted linear model expression.

3. Output Impedance: This refers to the effective output impedance offered at the regulated output node and is evaluated as the ratio of change in regulated output voltage magnitude ΔV_{REG} to the corresponding input variation in load current ΔI_L . Thus it can be considered identical to 'Load Regulation' parameter mentioned earlier, with the conceptual difference that this parameter incorporates the effect of finite output impedance of SC-CP and thus indicates the extent to which the regulator feedback loop is able to suppress the same.

4. CP Noise Rejection: This refers to the small-signal AC rejection offered by a regulator topology to the noise injected from the SC-CP input. It is estimated by including the CP linear model in the regulator simulation setup and considering the dc-source representing the CP output at no-load as the input noise source. It is quantified by noting the rejection magnitude offered at DC (low-frequency) and at CP operating frequency.

5. Power Supply Rejection Ratio (PSRR): This refers to the small-signal AC rejection offered by a regulator topology to the noise present on the positive rail or the power source to the regulator. In this case, the CP linear model is included by replacing the dc-source representing the CP output at no-load with ground potential.

6. Settling Time: This is the time required for the regulated output to reach within certain percentage limit of its corresponding steady-state magnitude, and is strongly influenced by CP output transfer characteristics.

7. Steady-state ripple: This is evaluated in terms of the transient voltage ripple magnitude at the CP switching frequency, once the steady-state has been attained. Its magnitude depends on the ripple of the unregulated input provided by the CP and is therefore evaluated at the maximum load current setting.

8. Noise Power: This is evaluated using the spectral analysis of the regulated

output at maximum load current. It is measured in terms of rms noise voltage at the harmonics of CP switching frequency F_{IN} . It is also estimated in terms of the integrated rms noise voltage obtained across a range of frequencies from DC till N^{th} order harmonics of F_{IN} .

9. System Efficiency: This refers to the end-to-end system efficiency derived for a given regulated output at a given load current, by modifying the CP efficiency expression to as expressed in (3.3).

$$\eta_{sys.Eff} = \frac{V_{REG} \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{PAR} + I_{Q_REG})} \quad (3.3)$$

where $V_{DD} \cdot I_{Q_REG}$ represents the regulator quiescent power consumption. For any given operating condition, the inclusion of post-regulator stage results in lowering of the system efficiency as compared to the efficiency derived for the stand-alone CP. There two main factors contributing towards this efficiency loss are, firstly the possible reduction in CP output magnitude due to the potential drop required across the regulator stage and secondly due to the quiescent power consumption within the regulator.

The regulator efficiency can be interpreted in terms of the difference between the CP and overall system efficiency, whereby a smaller difference indicates a more power efficient regulator implementation.

3.3 Digital Feedback Loop Using Hysteresis Comparator

In this regulation technique the CP is operated within a digital feedback loop, such that its output is bounded within a comparator's hysteresis range. A typical implementation of this regulation technique is as depicted in the Fig. 3.1. It comprises of a comparator with a finite hysteresis range, which compares the scaled CP output to an external reference input and accordingly provides a control signal (EN) which toggles the CP state to turn 'on' or 'off', such that average CP output is obtained at the required potential.

During the steady-state operation, when the scaled CP output falls below the

Fig. 3.1: Negative voltage regulation: Digital feedback-loop utilizing hysteresis comparator [18]

lower tipping threshold (V_{TL}), the comparator outputs a logic low signal which disables the multi-phase generator, clock buffer cells and the CP, causing the circuit to enter a low-power sleep state. As a consequence, the CP output increases linearly due to the finite output load current, till it reaches the upper threshold (V_{TH}) of the comparator. At this crossover potential the comparator output toggles its state to logic high, thus enabling the CP operation and causing the regulated output (V_{REG}) being lowered, till it again falls below V_{TL} , at which point the comparator again toggles its output stage, and the cycle continues indefinitely. Thus a finite steady-state ripple sustained on the regulated output, with its magnitude proportional to the comparator's hysteresis range and independent of the CP design and operating parameters. The resulting PWM type operation for the CP maintains the average magnitude of the scaled CP output (V_{FB}) equal to the external reference input (V_{REF}), thus regulating the CP output itself, to a first degree approximation.

The application circuit of this regulation technique along with the representative values for supply voltage ($V_{DD} : 3.3V$), reference input ($V_{REF} : 2.2V$) and load-current range ($0\text{-to-}600\mu A$), as used for its performance evaluation, is as shown in Fig.3.1. Noticeably, the CP output (V_{CP}) and regulated output (V_{REG}) nodes are shared. The hysteresis comparator is formed as a combination of an OTA and

Fig. 3.2: Transient settling profile for regulated output (V_{REG} : -3.5V, I_L : 400 μ A, V_{REF} : 2.2V)

Fig. 3.3: Steady-state ripple for regulated output (V_{REG} : -3.5V, I_L : 400 μ A, V_{REF} : 2.2V)

inverter buffer chain, sized at 8x the unit inverter sizing to provide fast (< 5 ns) rise/fall times for the EN signal. The performance is evaluated through transient simulations while utilizing the actual bootstrap negative voltage CP employed () in the proposed NVG system implementation, as mentioned before.

The settling profile obtained from the transient simulation of this representative circuit, at a standard operating point (V_{REG} : -3.5V, I_L : 400 μ A, V_{REF} : 2.2V), is as shown in Fig. 3.2. The selected load current (I_L : 400 μ A) is well within the bounds the maximum supported load current (I_{L_MAX}), at the given regulated out-

put voltage magnitude. The zoom-in view of the transient steady-state ripple is depicted in the Fig. 3.3. As indicated in Fig. 3.2, 3.3, for the given application circuit, steady-state is obtained within 2 μ s, with the feedback (V_{FB}) and regulated output voltage (V_{REG}) nodes settling with a relatively large steady-state ripple magnitude ($< 150mV_{PP}$). The steady-state average magnitude of V_{FB} settles at external reference input potential (V_{REF}), thus allowing average regulated output to be stabilized at desired negative voltage magnitude. From Fig. 3.3, it can be observed that V_{REG} increases linearly in presence of charging by the constant load current, while the CP and clock driver circuits are disabled through EN signal, at logic low level. When the EN returns to logic high, the CP (along with switching signal drivers) resumes operation and causes the regulated output to be reduced in a series of charge-discharge sequence at CP operating frequency, identical to free-running CP operation in presence of a constant load current. It can thus be noted that for this regulation technique, the steady-state ripple magnitude is primarily determined by the effective hysteresis magnitude of the given comparator implementation and remains fairly independent of the instantaneous loading conditions.

The steady-state average V_{REG} magnitude and the steady-state ripple magnitude variation for the regulated output (V_{REG}) and the feedback node (V_{FB}), across load current, is presented in the Fig. 3.4. It can be observed that the ripple magnitude for V_{FB} is within $30mV_{PP}$, which is limited by the effective hysteresis magnitude of the comparator, and this bounds the ripple magnitude for V_{REG} within $210mV_{PP}$, across load current. The variation of the duty-cycle and the frequency of the enable signal (EN) with respect to the increasing load current, for the given required regulated output voltage magnitude (V_{REG} : -3.5V), once the steady-state is attained, is as shown in Fig. 3.5. It can be observed that the duty-cycle of the EN signal increases almost linearly from 8.5% at 50 μ A to 86.7% at 600 μ A, while its frequency is bound between 2.4MHz - 4MHz, which is sufficiently below the typical CP operating frequency (F_{IN} : 30MHz - 70MHz) for the given fully-integrated CP implementation. The maximum supported load current range for the given regulated output magnitude can be identified as 600 μ A, corresponding with EN signal duty-cycle reaching almost 100%. For further increase in load current, the EN signal is always on, indicating the CP is always turned on, thus implying that the circuit is completely

Fig. 3.4: Steady-state average regulated output magnitude and the steady-state ripple magnitude versus load current (V_{REG} : -3.5V, V_{REF} : 2.2V)

Fig. 3.5: Enable signal duty-cycle and frequency versus load current (V_{REG} : -3.5V, V_{REF} : 2.2V)

out of regulation. This maximum load current operating point (I_{L_MAX}) can also be verified from Fig. 3.4, as the average V_{REG} magnitude exhibits sharp linear increase for $I_L > I_{L_MAX}$ at 600 μ A.

This regulation technique has been utilized for both full-integrated SC-CPs [18] and external capacitor CPs, including its application in commercial IC products

[28, 29]. It facilitates a simple regulator implementation with minimum implementation overhead. Moreover, the periodic disabling of the CP and buffer cells in its operation results in substantial efficiency enhancement for the CP, especially at low-load currents. However, the regulation accuracy is rather limited due to a number of inherent limitations associated with its operation. A brief review of such limitations is discussed as follows.

Firstly, the technique is effective at only low-load currents as the system reduces to having 'no-regulation' once the load current is increased. This also indicates the trade-off between the obtained CP efficiency and the instantaneous loading conditions, given that the CP is turned on more frequently as load is increased. Even at low-loads, the output is characterized by large steady-state ripple magnitude, determined by the comparator's hysteresis range. Moreover, the ripple magnitude cannot be reduced arbitrarily by reducing the hysteresis range as this can potentially compromise the stability of the feedback loop.

Secondly, the CP output exhibits poor load and line regulation and the CP noise is not suppressed adequately, as the regulated output is directly derived from the CP output node itself. Thirdly, to ensure effective regulation, the CP operating frequency must be well matched to the instantaneous load current, so as to obtain comparable rise and fall times for the regulated output ripple during steady-state operation. Such load dependent frequency variation can significantly add to the design complexity and is not possible to achieve across the entire load current range.

In general the given regulation topology provides a first degree of regulation for the SC-CP unregulated output. However, its poor regulation accuracy, and high noise content restrict its application for precision voltage biasing and noise sensitive applications such as GaN power amplifier and Class-C VCOs. etc. It is well suited for fixed load current application with a high tolerance for transient ripple or spectral purity of the regulated output. Although, the intermittent CP operation does result in further boosting of its derived power efficiency at low-to-mid load current range.

3.4 Analog Feedback Loop Using Zener Diodes

This regulation technique employs a high-gain analog feedback loop which adjusts the total current injected into the CP to derive the regulated CP output at the required potential. An implementation of this technique utilizing the low reverse breakdown potential of zener diodes, is proposed in [26]. The application circuit of this regulation technique along with the representative values for supply voltage ($V_{DD} : 3.3V$), reference input ($V_{REF} : 1.5V - to - 2.5V$), zener diode breakdown voltage ($V_Z : 6V$) and CP linear model parameters ($V_{CP,0} : -5V$, $R_{CP} : 3.5k\Omega$, $C_L : 260pF$), as used for its performance evaluation, is as shown in Fig. 3.6. The test circuit employs the default CP equivalent linear model is to analyze the DC, AC and stability related performance parameters, while the actual transistor level CP implementation is utilized for its transient performance analysis.

The regulation circuit, as shown in the Fig. 3.6, comprises of a high-gain operational transconductance amplifier (OTA), a current source PMOS transistor P1 and a zener diode biased in the reverse breakdown region, with their positive terminal connected towards negative voltage of the inverting CP output. Similar to the previous technique, the CP output (V_{CP}) serves as the regulated output node V_{REG} , as marked in Fig. 3.6. The OTA output provides the gate bias for PMOS P1 such that its drain is maintained at approximately the external reference potential (V_{REF}) due to the high-gain of the feedback loop. In normal operating range, the drop across the zener diode is high enough to bias in its reverse breakdown region. Since the resistance offered by the zener diodes ($R_Z < 120\Omega$) in the reverse breakdown region is minimal, the CP output is thus maintained at zener voltage drop (V_Z) below the reference potential. In other words, the feedback loop action adjusts the total current injected into the CP, by modulating the current through P1, such that the CP output is regulated at zener voltage drops below the reference potential.

In the reverse breakdown region, as shown in Fig. 3.6, the zener diode can be modeled as series combination of DC source equal to V_Z and a small resistance R_Z , which accounts for the additional drop across the diode due to the current flowing across it. Utilizing the well-established linear model expression for the CP ($V_{CP} = V_{CP,0} + I_L \cdot R_{CP}$), the regulated CP output and the current through zener

Fig. 3.6: Negative voltage regulation: Analog feedback-loop utilizing zener diodes [26]

diodes can be derived using (3.4), (3.5).

$$V_{REG} = V_{CP,0} + I_{TOT} \cdot R_{CP} \quad (3.4)$$

$$\text{where } I_{TOT} = I_Z + I_L \quad (3.5)$$

where I_{TOT} represents the total current injected into the negative voltage CP, can be expressed as the sum of load current (I_L) and the current driven through zener-diodes (I_Z). The regulated CP output (V_{REG}) can also be derived in terms of the reference input and zener-diode model using (3.6).

$$V_{REG} = V_{REF} - V_Z - I_Z \cdot R_Z \quad (3.6)$$

Solving (3.4)-(3.6), the current through zener diodes I_Z can be readily derived using (3.7) and the regulated output can be derived in terms of load current using this result in (3.6).

$$I_Z = \frac{V_{REF} - V_Z - (V_{CP,0} + I_L \cdot R_{CP})}{R_{CP} + R_Z} \quad (3.7)$$

Since the (average) regulated output is simply derived as one V_Z below the V_{REF} , the effective output tuning range of V_{REG} is equal to the input common mode range of the OTA. The pass-transistor (MP1) is sized such that it operates at the

Fig. 3.7: Regulated output (V_{REG}) and total CP current (I_{TOT}) vs. reference input (V_{REF})

dropout condition ($V_{DS_PT} = V_{GS_PT} - V_{TH}$) for max. reference input (V_{REF_MAX}), corresponding with the maximum total current (I_{TOT}) injected into the CP. In this limiting case, it is assumed that no-load is connected, thus implying that the total current injected into the CP is provided through pass-transistor itself.

The analog feedback loop is stabilized through the dominant pole formed through CP load capacitor (C_L) and the output load (R_L). The pass-transistor sizing is relatively small to maintain the parasitic pole at its gate outside the unity-gain BW of the loop. The test circuit is verified to remain stable while maintaining a PM $>50^\circ$, within its identified operating envelope.

The (average) regulated output and the corresponding I_{TOT} is determined solely by the V_{REF} potential, as shown in Fig. 3.7. The practical operating bounds and regulation effectiveness can thus be determined by examining the variation of DC operating point and feedback loop's stability parameters (DC gain, Phase-margin

Fig. 3.8: Feedback loop stability parameters vs reference input (V_{REF})

(PM) and unity-gain BW (UGB)) with respect to V_{REF} , as shown in Fig. 3.8. In these analyses (DC and loop-stability) no-load is connected since the I_{TOT} is independent of the loading conditions and is maintained constant by the feedback loop, as required to derive the required V_{REG} magnitude. The practical operating region can be identified as the range of V_{REF} for which DC Gain is above 55dB, while PM is maintained above 50deg. In context of this test circuit, this criteria implies that the permissible V_{REF} range is from 1.2V to 2.6V, corresponding with V_{REG} range from -4.8V with I_{TOT} of $92.7\mu\text{A}$ to -3.5V with an I_{TOT} of $473\mu\text{A}$, as highlighted in Fig. 3.7. The regulation effectiveness can be estimated by contrasting the V_{REG} magnitude (obtained from DC-opt simulation) with the $(V_{REF} - V_Z)$ line, as shown in Fig. 3.9. The difference between the ideal $(V_{REF} - V_Z)$ and real V_{REG} curves depicted in Fig. 3.9 occurs due to the finite breakdown resistance ($R_Z \sim 100\Omega$) of zener diodes, which results in larger variation for lower V_{REG} values, corresponding with lower current through passing through zener diode(s).

The load regulation and AC analysis of CP noise rejection are evaluated at maximum load by setting V_{REF} at maximum input, thus corresponding with the maximum V_{REG} and I_{TOT} magnitude. The supported load current range for a given V_{REG} magnitude is determined using similar criteria of maintaining DC gain above 55dB and PM above 50deg, as that used to identify permissible V_{REF} range. In the

Fig. 3.9: Regulated output (V_{REG}) and ($V_{REF} - V_Z$) curve vs. reference input (V_{REF})

given test-circuit, for the max V_{REG} at $-3.5V$ the corresponding maximum load is determined as $357\mu A$. As per simulation results, the load regulation provided by the given regulation technique, varies from $118\mu V/\mu A$ to $130\mu V/\mu A$, while the small-signal (AC) CP noise rejection is evaluated at around $\sim -24dB$ at DC and $\sim -48dB$ at CP operating frequency.

The complete transient settling profile, evaluated using actual transistor level implementation of the CP, is as shown in Fig. 3.10, along with zoom-in view of the steady-state transient ripple. It can be observed that, likewise the previous regulation technique, the steady-state for this regulator is also attained within $2\mu s$, however the steady-state ripple magnitude is now reduced to under $50mV_{PP}$. The steady-state ripple magnitude is still relatively large, despite the high unity-gain BW ($UGB > 20MHz$) of the feedback loop. It can be further verified that the steady-state ripple magnitude remains constant across the load current range, since the I_{TOT} is invariant of the instantaneous loading condition.

The given regulation technique implementing an always-on, analog feedback loop results in a significant improvement in both the regulation accuracy and efficacy as compared to the previously introduced technique employing digital feedback loops. In steady-state, the high loop gain allows to make fine adjustments into the injected correction current (I_Z), as fast as possible for a given loop bandwidth, thus resulting

Fig. 3.10: Transient settling profile and steady-state ripple for regulated output (V_{REG} : -3.V, I_L : 400 μ A, V_{REF} : 2.6V)

in low-ripple, well regulated CP output. However, the regulator topology encounters a number of design challenges that limit the performance of regulated negative voltage output. The major drawbacks associate with the application of this technique for regulation SC-CP outputs, can be briefly examined as follows.

Firstly, the regulation accuracy and CP noise suppression offered by this technique is limited and may not be acceptable to meet the stringent specifications of RF circuits and other precision biasing applications. This is because, even with a high-gain, high-bandwidth feedback loop, while the drain of current-source P1 is well-regulated to approximately the reference potential c , the final regulated output is derived indirectly from V_{REF} , as mentioned in (3.6). Moreover, for practical implementation, the non-zero zener diode resistance R_Z in the breakdown region can be expected to cause further variation of V_{REF} magnitude across varying load current.

Secondly, the tuning range for the regulated output is very limited as it is derived from varying the external reference input potential. The variation of V_{REF} is not convenient as it is restricted by the limited input common model range of the OTA. In addition, V_{REF} variation is also restricted by the drain-source potential V_{DS_P1} that must be maintained across current source P1 to ensure its operation in the saturation region. The maximum regulated output V_{REG_MAX} and the corresponding maximum injected CP current I_{TOT_MAX} , supported by the given regulator topology,

can thus be derived for the limiting case when P1 in the dropout condition (operating at the onset of linear region) and no load is connected, implying that the total current injected into the CP is driven through PMOS P1 itself. The corresponding design equations are as given by (3.8)-(3.10).

$$V_{REG_MAX} = V_{CP_0} + I_{TOT_MAX} \cdot R_{CP} \quad (3.8)$$

$$V_{REF_MAX} \approx V_{REG_MAX} + V_Z \quad (3.9)$$

$$V_{DS_P1} = V_{DD} - V_{REF_MAX} = \sqrt{\frac{2 \cdot I_{TOT_MAX}}{k'_n(W/L)_{P1}}} \quad (3.10)$$

In (3.9) the effect of zener diode resistance (R_Z) is not considered for simplification. Solving (3.8)-(3.10), the maximum regulated output V_{REG_MAX} and the corresponding maximum supported load current I_{TOT_MAX} can be derived in terms of the CP linear model and current-source P1 design parameters.

Thirdly, to ensure effective regulation, the given technique requires that a minimum magnitude of current to be drive through PMOS P1, such that feedback loop remain active with high loop gain. This implies that for a given regulated output, the maximum allowed load current is a subset of the total current injected into the CP, which as seen from (3.4), solely depends on the CP linear-model parameters namely the charge-pump output at no-load V_{CP_0} and the charge-pump output impedance R_{CP} . Since the CP noise and ripple increases proportionally to the total current sinking into (or sourced from) its output node, it follows that for this technique, there exists an inherent trade-off between the maximum supported load current and the regulated output noise content and transient ripple magnitude.

Lastly, the technique exhibits high sensitivity towards process, voltage and temperature variation as normally occurring in a standard CMOS process. The same can be verified from (3.6) and (3.7), whereby the derived regulated output voltage is directly proportional to the process sensitive breakdown potential of zener diodes, and total current injected into the CP shows strong dependence on the CP output impedance.

3.5 Linear Regulator

In this regulation technique the CP output is followed by a standard linear regulator arrangement to derive a very well regulated, low noise output. The high-gain of the regulator feedback loop effectively suppresses the CP noise and transient ripple, while also lowering the effective output impedance at the regulated output node. The output thus obtained has excellent regulation characteristics and therefore can be directly utilized for almost all negative voltage based applications. However, the technique requires that the stability of the regulator loop is ascertained for the SC-CP input with high output impedance and high load-dependent noise content. This causes significant increase in complexity and implementation overhead related to the design on the given regulator module.

The application circuit of this regulation technique along with the representative values for supply voltage ($V_{DD} : 3.3V$), reference input ($V_{REF} : 2.2V$), CP linear model parameters ($V_{CP,0} : -5V$, $R_{CP} : 3.5k\Omega$, $C_L : 260pF$) and external capacitor ($C_{EXT} : 220nF$), as used for its performance evaluation, is as shown in Fig.3.11. Similar to previous technique, the CP linear model is used to analyze the small-signal performance (DC, AC and stability), while the actual transistor level CP implementation is utilized for its transient performance analysis.

The topology mainly comprises of an error amplifier and the large pass-transistor which separates the noisy CP output (V_{CP}) with regulated output (V_{REG}) node. The regulator module typically also includes the bias-generator circuit (not shown in Fig. 3.11) for the supply-independent, constant current biasing of various branches within the error-amplifier. The error-amplifier, operating within a high-gain negative feedback loops, dynamically adjusts the on-resistance of the pass-transistor such that the feedback node is forced equal to reference potential. The CP output is thus regulated and is derived at the required potential by varying the ratio of feedback resistor divider. Based on the location of dominant loop, the high-gain of the regulator feedback loop therefore actively filters the CP noise and ripple to generate low-ripple, low-noise output with lowered output impedance and precise output magnitude.

The typical settling profile obtained for the linear regulator implemented along with the actual SC-CP implementation, is as shown in Fig. 3.12. The zoom-in view

Fig. 3.11: Negative voltage regulation: Linear regulator arrangement [28, 29]

of the transient steady-state ripple for both CP and regulated output is also depicted in the Fig. 3.12 alongside. The system simulation results presented in Fig. 3.12 are derived with a single minimum sized off-chip capacitor ($C_{EXT} > 220\text{nF}$), which is required to stabilize the regulator feedback loop by determining the location of the dominant pole. As shown in Fig. 3.12, the steady-state is obtained within 2ms, while the regulated output exhibits ultra-low steady-state ripple magnitude of under 250nV, thereby implying that for practical implementation, transient ripple or noise performance of V_{REG} will only be limited by the reference input. In addition, the relative ripple magnitude of CP and regulated outputs indicates high CP noise rejection magnitude resulting in minimal residue of the CP noise contained within regulated output.

However, despite its evident performance advantages over other regulation techniques, the implementation of the linear regulator along with a SC-CP structure results in some major design concerns and implications for overall system implementation. Firstly, the stability of the regulator's negative feedback loop is impacted by the finite output impedance of the SC-CP. This effect has the restricted application of this technique to commercial IC solutions, employing external capacitor CP implementations. Such CPs easily achieve very high driving capacity, supporting up-to 150mA of load currents, and therefore the resulting impact of finite CP output impedance on the loop-stability characteristics is minimal. Secondly, the finite voltage drop required across the pass-transistor translates to reduced load current

Fig. 3.12: Transient settling profile and steady-state ripple for regulated output (V_{REG} : -3.0V, I_L : 250 μ A, V_{REF} : 2.2V)

limit for a given regulated output and results in lower power efficiency for the overall system implementation. Lastly the regulator feedback loop may necessitate the use of an off-chip capacitor to ensure its un-conditional stability. This may not be suitable for integration standpoint, besides result in longer settling times for the regulated output.

3.6 Performance Comparison of Negative Voltage Regulation Techniques

The performance of various regulation techniques can be quantitatively assessed and contrasted using their representative circuits, as introduced in the previous sections. A comparison of the fundamental regulator FOMs, derived as simulation results from these test circuits, is captured in Table 3.1. The performance metrics for the linear regulator arrangement are derived from the its actual implementation utilized in the proposed NVG. To ensure an accurate comparison among various regulator topologies, the regulator circuits are implemented in the same technology node as the proposed NVG. In addition, these test circuits are simulated with actual fully-integrated SC-CP, as employed in the NVG system and identical regulator sub-circuits, including Bias-gen and OTA are re-used across the three regulator

Table 3.1: Comparison of Negative Voltage Regulation Techniques

Parameters	Hysteresis Comparator [18]	Zener Diodes [26]	Linear Regulator (This work [40])
# Off-Chip Cap.	-	-	1
V_{REG} Range	-5.1V to 0V	-5.1V to -3.5V	-4.4V to 2.1V
Max. Load (V_{OUT} : -3.5V)	600 μ A	357 μ A	150 μ A
Load Regulation*	120 μ V/ μ A	118 μ V/ μ A	20 μ V/ μ A
CP Noise Rejection	- - -	-24 dB (at DC) -48 dB (at CP F_{IN})	-65dB (at DC) >-100dB (at CP F_{IN})
Settling Time	< 2 μ s	< 2 μ s	< 2ms
Steady-state Ripple	< 210mV $_{PP}$	< 50mV $_{PP}$	< 250nV $_{PP}$

*Based on (DC-Opt.) Simulation

topologies, either for implementing hysteresis comparator's first stage or as error-amplifier for latter two regulator implementations.

As observed from Table 3.1, the linear regulator topology typically requires at least one off-chip capacitor in order to ascertain unconditional stability of the regulator's feedback loop. In contrast, the other two regulation techniques can be fully-integrated and therefore might be better suited for certain SOC related applications, with less stringent noise and ripple requirements. Furthermore, the linear regulator offers the widest tuning range, however the maximum supported load current for a given V_{REG} magnitude is lower than two counterpart regulation strategies. This is because the linear regulator arrangement has to account for the drop across the pass-transistor, while for the other two regulation techniques, the regulated output is derived directly at the output node of the CP and is therefore only limited by the CP output impedance. In addition, the linear regulator delivers better load regulation and offers significantly higher CP noise rejection, due to the low frequency dominant pole set by the off-chip capacitor. The latter directly translates into high degree of spectral purity and ultra low steady-state ripple for V_{REG} . However, utilizing a large C_{EXT} also incurs large settling times for the regulated output to attain steady-state. In summary, the linear regulator clearly outperforms other negative voltage regulation techniques in terms of transient ripple and low-noise performance while offering better regulation accuracy in terms of load and line regulation. However, its implementation indispensably requires an off-chip, loop stabilizing capacitor, which also

results in longer settling times.

In general, the first two regulation techniques, employing a comparator based digital feedback loop or utilizing an analog feedback loop with zener diodes, operate by directly conditioning the CP operation to derived the required regulated output from the CP output node itself. These techniques offering a simpler regulator implementation also result in higher system efficiency since the additional potential drop across the CP magnitude is avoided. However, the regulator feedback loop is not able to adequately suppress the CP output impedance and noise, since the CP and regulated output nodes are shared. In general, the overall regulation effectiveness is compromised, resulting in poor regulation accuracy, limited tuning range and large steady-state ripple at the CP switching frequency. However due to ease of implementation and higher efficiency, such techniques may well be utilized for several less demanding application with relaxed specification for the required negative voltage input.

The third regulation technique implements a separate linear regulator cell, operating independently of the SC-CP operation. The high-gain of the regulator loop effectively suppress the CP non-linearities to obtain a low-ripple, low noise output with high regulation accuracy. However the output impedance of the SC-CP raises concerns regarding the unconditional stability of the regulator loop. In addition, the potential drop occurring across pass-device further limits the attainable power efficiency for the system level implementation. In general, due to superior regulation performance, the technique can be utilized for multiple applications, provided design concerns associated with its implementation are adequately addressed. In addition, output impedance, as seen at the output node is significantly lower than the CP output impedance, due to high-gain of the feedback loop. Owing to superior regulation characteristics, the regulated negative output, as obtained from this topology, can be directly utilized even for the most demanding applications, requiring precisely controlled voltage magnitude with high degree of spectral purity.

In contrast to the two regulation techniques introduced earlier, the given linear-regulator topology offer clear performance advantage in terms of higher regulation accuracy, significantly lower steady-state ripple and noise content, and wider output tuning range. Due to such superior regulation characteristics, its implementation

is explored within the proposed regulated, low-noise NVG system, while designing it to operate with a fully-integrated SC-CP. The resulting system implementation, despite its limitations (in terms of requirement of off-chip capacitor, longer settling times, lower efficiency) is most suitable for deriving regulated negative voltage source for precision voltage biasing and low-noise application, as is the central objective of this work. In its current implementation within the proposed NVG system, the implications arising much higher output impedance of fully-integrated SC-CPs are identified and addressed. The feedback loop-stability is rigorously verified from both small and large signal prospective. In addition, complete system level performance is further verified through transient co-simulation of CP and regulator modules. The detailed design, analysis and verification of the proposed NVG system is elaborated in the following chapters.

3.7 Chapter Summary

This chapter discusses the design, operation and implementation of various regulation strategies that have been explored for deriving a regulated negative voltage output. In this chapter, firstly the regulator related performance metrics are defined and discussed, in order to aid with the detailed comparative analysis of various regulation techniques.

This is followed by a detailed review and discussion of the three known regulation techniques that have been employed for negative voltage regulation. To facilitate a quantitative examination, a representative test circuit is implemented for each technique and the relevant simulation results are presented to highlight its operation and performance limitations.

Lastly, a detailed performance comparison analysis of various regulation strategies is presented. The regulator FOMs derived from simulation results of its test circuits are contrasted and analyzed. Finally, the design principle and implementation concerns associated with each regulation strategy are outlined.

Chapter 4

Design of Highly-Integrated, Low-Noise, Regulated Negative Voltage Generator

4.1 Introduction

This chapter discusses the circuit level design and silicon implementation of the proposed low-noise, regulated NVG. This highly integrated solution, integrates three main modules, including a multi-phase clock generator, an optimized fully-integrated SC-CP in inverting configuration, and a negative voltage regulator. The periodic square wave input for driving the CP at the varying frequencies, is provided externally, while the feedback resistor divider and the stabilizing capacitor for the regulator, are also implemented off-chip, due to their large magnitude, and are not suitable for integration. An in-depth analysis of the design, operation and transistor level implementation of each of the integrated modules is presented along with a discussion on the practical aspects related to silicon realization of the complete NVG system. The system level analysis and performance verification is presented in the following chapter.

In this chapter, firstly, the functional model of the design is presented and the central idea introduced through this work is clearly highlighted. Following this a systematic design methodology is introduced, which provides a structured flow, starting from derivation of the CP and regulator specifications, till the complete

system level verification, for the given NVG system implementation. This is followed by the details on the implementation of the multi-phase clock generator and the design and optimization of the inverting SC-CP, used in the given design. A novel CP operational analysis is presented and is utilized to derive the required circuit level CP implementation, by way of optimizing the design parameters for minimum area utilization. In addition, a detailed analysis of the CP power efficiency is presented, and the techniques for maximizing its magnitude, under various operating scenarios, are discussed in detail. This is followed by a detailed review of the design, operation and implementation of the negative voltage regulator and regulator sub-circuits, including bias-generator and error-amplifier. Finally, details related to the complete system level implementation and its silicon realization are discussed.

4.2 Low-Noise Negative Voltage Generator Architecture

This work presents the design and analysis of a generic negative voltage generator (NVG) system, that can cater to wide range of applications while being suitable from an integration prospective. The highly-integrated solution is powered from a single positive DC input supply, and generates low-noise, regulated negative voltage output that can be derived over a wide tuning range with high regulation accuracy. The design integrates all the essential circuit modules, and requires only one-off chip capacitor to ensure the stability of the feedback loop.

The functional diagram of the proposed NVG system is as shown in Fig. 4.1. The design essentially comprises of a highly-optimized SC-CP implementation in inverting configuration, and low-power a linear regulator module to derive the required low-noise, regulated negative voltage output. The integrated implementation also includes the Multi-Phase clock generator and buffers for internally generating the periodic input switching signals for driving the capacitive loads within CP. The primary two inputs required for the system level operation are the positive 3.3V DC input supply and input periodic signal (square or sine wave) with frequency range from 20MHz - 70MHz. The default low-noise reference input for the regulator can be set at or below 2.5V, and in case a secondary input voltage source is not available,

Fig. 4.1: Functional diagram of proposed Negative Voltage Generator (NVG) System

it can be derived through a simple resistor divider arrangement from the primary 3.3V input or substituted with a low noise ground rail input. In terms of the off-chip components, the system requires only one off-chip capacitor (C_{EXT}) greater than 220nF, to ensure unconditional stability of the regulator feedback loop. In addition, a feedback resistor, referenced to the 3.3V DC input is utilized to tune the regulated negative voltage output magnitude. The two outputs for this design are the unregulated output of SC-CP and the regulated negative voltage as output from the regulator. The CP output is required for the SC-CP performance characterization and is measured directly from the output pad without requiring an additional load capacitors. In contrast the regulated output is derived as charge stored on the external capacitor, placed in close proximity of the corresponding pad.

The main design idea explored in this work is to utilize a fully-integrated SC-CP, with limited driving capacity, to power a linear regulator module, comprising of a low-power error amplifier and a bias-generator sub-circuit. As shown in Fig. 4.1, the positive rail of the regulator block is shared with the nominal 3.3V supply input, while the CP output is connected to its negative supply rail, along with the source-terminal of the deep-n-well of the pass-transistor. The unregulated CP output therefore serves as both power source for the regulator module and input to the pass-transistor. As mentioned previously, the fully-integrated SC-CP output, is characterized with high-noise content and exhibits high-output impedance resulting in large variation in the CP magnitude across load current. The regulator is designed to withstand the resulting input variation across its supply headroom for the supported range of load currents. The given system level configuration fa-

cilitates effective suppression of CP ripple and noise content, thus generating the required low-noise, regulated negative voltage output. It can be noted, that the CP output being the most negative potential of the entire circuit, all the current from the regulator module and output load sinks into this node

The high-gain of the regulator feedback loop actively filters the CP noise and ripple and suppress its high output impedance to derive regulated negative voltage output with low-steady ripple, minimal CP noise and high regulation accuracy. The reduced output impedance at the regulated output node significantly improves the usability for applications involving large variation in load current. It is also essential in reducing the settling time for the regulated output voltage to reach its steady-state magnitude. Moreover, the regulated output can be conveniently obtained over a wide tuning range, by adjusting the ratio of the feedback resistor divider, whereby the upper bound of the regulated output potential is limited by the reference potential. Therefore, the given design can provide both positive and negative regulated output potentials from the same output node, thus further enhancing its targeted scope of application.

The proposed design encounters a number of system and circuit level design challenges arising primarily from employing the fully-integrated SC-CP as unregulated input source for the regulator. Firstly, the wide variation in CP magnitude across load current dictate that the regulator must be able to withstand large variation in its available headroom. Moreover, due to limited driving capacity of fully-integrated CP, the regulator must be a low power design, with minimum variation in its operating current across its operating range. Secondly, the CP output exhibits high sensitivity towards the parasitic effects, involved in its silicon realization, and can thus be observed to have substantial variation (10% to 20%) across simulation and measurement results, with a larger variation expected for CP operation under FSC regime. Therefore, sufficient design margin must be allocated for the variation in CP output magnitude at the system level, such that the regulator is able to absorb this variation and continues to operate normally. Thirdly, the high output impedance of the fully-integrated CP structure can introduce potential instability within the regulator feedback loop. To further complicate the matter, the instability may not become apparent in small-signal simulation, but may still manifest at the system

level. Therefore, a robust and reliable implementation for such design mandates that the feedback loop stability is rigorously verified, using multiple circuit-analysis techniques.

In spite of the above mentioned design challenges, the proposed design derives its integration advantage and superior low noise performance through the adaption of a fully integrated charge-pump structure. This is because, the noise rejection offered by the linear regulator circuit at typically high switching frequencies (10MHz to 300MHz) employed by the fully-integrated CPs, is 50dB to 90dB higher than that obtained at low frequencies (100kHz to 900kHz) utilized by CPs employing external capacitors. Since the charge-pump ripple is mostly centered around the switching frequency and its harmonics, the given topology results in low noise output with moderate driving capacity, as per the operating limits of the CP. Moreover, the choice of charge-pump implies that the overall design utilizes only one off-chip capacitor, which can be shared with the supply decoupling capacitor, thus leading to high degree of integration for the overall system.

For the given design, implemented with an input power supply at 3.3V and reference input at 2.2V, the regulated output has a tuning range from -4.4V to +2.1V for biasing applications. The design also supports load currents of 250 μ A, 550 μ A and 800 μ A for the regulated output voltage at -3.0V, -1.5V and 1.5V respectively. The regulated output is verified for very low steady-state ripple magnitude and minimal CP noise content for worst-case operation at maximum load current setting. Furthermore, design is application verified with a state-of-the-art GaN-HEMT power-amplifier to demonstrate its suitability for precision negative voltage biasing and noise-sensitive application.

4.3 Design Methodology

In order to ensure a reliable operation along with repeatable performance, a systematic design procedure is adapted for the design of the proposed negative voltage generator system. The present design methodology, besides facilitating a robust implementation, and also serves another important purpose of lending scalability to the given design implementation. The given design flow involves proceeding along

Fig. 4.2: Flowchart of Design Methodology

the steps as depicted in the flowchart presented in the Fig. 4.2.

The scope of this chapter is limited to circuit level implementation and optimization of CP and regulator modules. The system level performance evaluation, analysis and verification, are addressed in detail, in the following chapter. The remainder of this section elaborates on the first two steps as listed in the Fig. 4.2, providing directions for deriving the pass-transistor sizing, and deducing the SC-CP specification, in terms of estimating the optimum number of CP inverting stages and the required CP output impedance.

In terms of designing a generic NVG system, the key performance bottleneck for regulated output voltage arises from noise-sensitive precision voltage biasing applications, such as GaN-HEMT based RF power amplifiers. Therefore, considering such RF circuits and applications as the key target application, the initial design specification is set as $200\mu A$ of minimum load current (I_{L_MIN}) for regulated output (V_{REG_MIN}) greater than $-3.0V$. This specification also aims to maximize its usability for other relevant application areas such as static leakage reduction, constant current stimulation etc., as mentioned in section 1.2 of chapter 1. For the given operating requirement of I_{L_MIN} and V_{REG_MIN} , the deep-n-well pass transistor is sized with a dropout voltage (V_{DO}) of $0.6V$, as given by (4.1).

$$(W/L)_{PT} = \frac{2 \cdot I_{L_MIN}}{k'_n \cdot (V_{DO})^2} \quad (4.1)$$

where k'_n and $(W/L)_{PT}$ represent the output transconductance and required aspect ratio of the deep-n-well pass-transistor, respectively. As seen from (4.1), the relatively large dropout voltage results in significantly smaller sizing of the pass-transistor. This vastly simplifies the regulator implementation and directly contributes in alleviating the concerns associated with the stability of the regulator feedback loop, which is affected due to the high-output impedance of the fully-integrated CP.

To ensure that the regulator feedback loop remains active with high-loop gain, the pass-transistor device must operate in saturation region, thus implying that the required CP output at minimum load current should well exceed the minimum regulated output by the dropout voltage of the pass-device. It is to be noted that even the detailed post-layout simulations consistently underestimate the effect of parasitics on the CP transfer characteristics. To ensure effective regulation performance a 10% design margin is reserved to absorb the possible variation in CP output magnitude. Therefore, the required CP output (V_{CP_REQ}) corresponding to the minimum load current can be estimated to be at least $1V$ below the given minimum regulated output, as shown in (4.2).

$$V_{CP_REQ} = V_{REG_MIN} - V_{DO} - 0.1 \cdot (V_{REG_MIN} - V_{DO}) \approx V_{REG_MIN} - 1V \quad (4.2)$$

The CP output for a given load current can be derived using its extracted linear model, as mentioned in (4.3).

$$V_{CP} = V_{CP,0} + I_{TOT} \cdot R_{CP} \quad (4.3)$$

$$I_{TOT} = I_L + I_{REG} \quad (4.4)$$

where $V_{CP,0}$ is the CP output at no load condition, R_{CP} is the effective CP output impedance, at the a given CP operating frequency. The terms I_{TOT} , representing the total current injected into the CP, is the sum of load current (I_L) and the current consumed within the regulator module (I_{REG}), as mentioned in (4.4). The presumed linear CP characteristic, assuming constant CP output impedance, independent of the injected current, is well established through a detailed quantitative analysis in the following section, and is further verified through simulation and measurement results.

Assuming a linear SC-CP implementation, the charge-pump output at no-load ($V_{CP,0}$) can be expressed in terms of the number of CP inverting stages (N), the switching amplitude (V_{DD}), assumed to be same as the DC input supply magnitude, and the loss factor (γ), as shown in (4.5).

$$V_{CP,0} = -(N \cdot V_{DD} \cdot \gamma) \quad (4.5)$$

The factor γ is a technology dependent parameter which captures the lumped effect of top-plate parasitic capacitance, as given by (4.6).

$$\gamma = \frac{C_P}{C_P + C_{PAR_TOP}} = \frac{1}{1 + \beta} \quad (4.6)$$

where β ($= C_{PAR_TOP}/C_P$) is the top-plate parasitic capacitance coefficient. Based on the sample simulation for transistor level CP implementation operated under FSC regime (such as those presented in Sec. 2.5), the magnitude of γ is estimated to be within 0.72-to-0.76.

The required CP output impedance R_{CP_REQ} for the given SC-CP implementation, can be readily derived in terms of the number of CP inverting stages, by using (4.5) and (4.4) in (4.3), and equating the resulting linear model expression to the

required CP output magnitude V_{CP_REQ} mentioned in (4.2), as given by (4.7).

$$R_{CP_REQ} = \frac{(N \cdot V_{DD} \cdot \gamma) - |V_{CP_REQ}|}{I_L + I_{REG}} \quad (4.7)$$

The required optimum number of CP inverting stages is estimated by extending the analysis for the boosting charge-pumps in [7, 8] for the inverting CP configuration used in this implementation. It should be noted that this analysis is based on the CP operation in slow-switching-condition (SSC) regime, implying that it does not incorporate the effect of switch resistance (R_{SW}) or the on-time (T_{ON}) of the switching devices within CP operation. However it can be still be utilized to arrive at a first estimate for the number of charge-pumping stages, for a given design specification, defined in terms of the output voltage magnitude at a specified load current, for a given input voltage magnitude. Furthermore, for this analysis, pumping capacitance per stage (C_P) is evaluated as function of load current and the derived value of optimum number of CP stages (N_{OPT}). However, in this work, this estimation of C_P is not followed, since it is strictly based on the assumptions resulting from the CP operation in SSC regime. Instead, a novel SC-CP operation analysis, independent of the CP operating regime (FSC or SSC), is proposed and utilized for the derivation of C_P along with switch resistance R_{SW} , as is elaborated in the following section.

The resulting expression of optimum CP inverting stages, were derived in section 2.3.2.1, and re-adapted here in (4.8), (4.9).

$$N_{Eff_opt} = \frac{|V_{CP_REQ}|}{V_{DD}} \left(1 + \sqrt{\frac{\alpha}{1 + \alpha}} \right) \quad (4.8)$$

$$N_{Area_opt} = \frac{|V_{CP_REQ}|}{V_{DD}} \quad (4.9)$$

where N_{Eff_opt} and N_{Area_opt} are the optimum number of CP inverting stages for maximum efficiency and minimum area implementation respectively, and the term α ($= C_{PAR_BOT}/C_P$) is technology dependent parameter representing bottom-plate parasitic capacitance coefficient. In the technology node utilized for this work (GlobalFoundries 180nm BCDlite process), the magnitude of α is within 0.1-to-0.5, including CP operation in FSC region.

For the given implementation, with required CP output (V_{CP_REQ}) at -4V as

mentioned in (4.2) and input supply at 3.3V, N_{Area_opt} is derived as 1.21 while N_{Eff_opt} varies from 1.57 to 1.91. This suggests 2-stage CP implementation. The required CP output impedance can now be estimated using (4.7), for the minimum load current operation (I_{L_MIN} : $200\mu A$) and typical regulator current is assumed to be constant at $50\mu A$. Thus with N set at 2 and with the loss factor γ variation estimated from 0.72-to-0.76, the CP output impedance is estimated to be in the range of $3.0k\Omega$ to $4k\Omega$.

The design methodology presented thus far, provides an outline for the SC-CP structure (in terms of number of CP inverting stages) and the required output transfer characteristics (in terms of the required CP output impedance). It is followed by a novel CP operation analysis, which is used to derive the remaining CP design parameters as needed to arrive at an optimized SC-CP implementation. The frequency dependent CP linear model extracted using this analysis is further utilized in the regulator simulation setup for a realistic evaluation of the system level functionality, including feedback loop stability, CP noise rejection and settling characteristics.

4.4 Design and Optimization of Negative Voltage Switched Capacitor Charge-Pump

4.4.1 Selection of Fully-Integrated SC-CP Topology

A brief overview of the various fully-integrated linear SC-CP architectures was presented in section 2.4. With regards to selecting the appropriate topology for this work, the Dickson CP was avoided due to its primitive implementation resulting in large diode voltage drop in the CP output magnitude. Thus, the CP topologies considered for possible application, were the the Latched CP and the Bootstrap CP. To provide a quantitative basis for selection, a performance comparison analysis between these two linear SC-CP topologies was also presented in section 2.5.

The Latched or the cross-coupled pair CP, utilizes a simple 2-phase input switching signal and typically delivers high power efficiency, precisely due to the lower power consumed in generating the input signals required for its operation. However, its inverting configuration implementation requires that, within any inverting stage,

the n-well of the PMOS pairs is tied to ground, to prevent instability caused due to the possible forward biasing of p-substrate to n-well p-n junction diode. This results in an increased threshold voltage (V_{TH}) for the PMOS devices due to the body-effect manifesting from the subsequent increase in their respective source-body (V_{SB}) potential, along the cascaded CP stages. Consequently, for the inverting configuration, the CP output impedance increases rapidly as number of CP stages are increased, thus resulting significantly lower CP output magnitude and reduced power efficiency. Therefore, despite its default high power-efficiency, the V_{TH} degradation due to body-effect, restricts the application of Latched CPs for negative voltage generation, especially when a large number of CP stages are required.

In contrast, the Bootstrap CPs require more power hungry 4-phase input switching signal, resulting in lower power efficiency. In terms of its implementation for the inverting configuration, the given CP only utilizes deep-n-well devices for both the charge-transfer and the bootstrap switches. The deep-n-well devices with local source-to-body contact, do not suffer from body-effect related V_{TH} degradation along the CP stages, thus facilitating CP implementation with higher number of inverting stages. The CP output impedance still increases with no. of stages, due to the higher switching losses incurred in the signal path. In general, despite the lower efficiency, the Bootstrap CP can be considered as a reliable alternative for negative voltage generation, due to the absence of body-effect. The given CP is therefore utilized for applications requiring a high negative output voltage magnitude, or when a large voltage conversion ratio is desired. Moreover, the use of such CPs is also relevant for applications employing a higher power supply domain, implying that the body-effect related V_{TH} degradation can be much pronounced, even for lesser number of CP inverting stages.

Therefore, due to general suitability of Bootstrap CPs for negative voltage generation, this topology is selected for the required 2-stage SC-CP implementation, employed in this work. Moreover, this design choice ensures that the design principle is retained for lower supply voltages, requiring higher number of inverting stages.

Fig. 4.3: (a) Multi-phase clock-generator (b) 4-phase switching input

4.4.2 Circuit Level Implementation

4.4.2.1 Multi-Phase Clock Generator

The schematic of the multi-phase clock generator [18] used to generate the non-overlapping, 4-phase input switching signal is as shown in Fig. 4.3(a). The resulting 4-phase periodic output, as required for the Bootstrap CP operation, is as shown in Fig. 4.3(b). The clock generator comprises of one primary and two secondary cells, each of which split the input periodic signal into two out-of-phase non-overlapping outputs. Each unit cell consists of two crossed NAND latches with added delay elements. A transmission gate in ‘on’ state is added to one of the signal paths, in order to offset the inverter delay in other signal path. For the given configuration, the transmission of logic 0 requires completed transmission of logic 1 at the complementary output, thus resulting in almost twice the amount of delay for logic 0 to reach its respective output. Consequently, the in-phase output appears first for the rising edge, while the out-of phase output is obtained earlier for the falling edge, of the input signal. The given configuration therefore generates the a time-lag between the consecutive switching transitions at its output.

The secondary splitter cells, receiving the two opposite polarity of input signals, further split their respective inputs into two out-of-phase outputs, to finally derive the required 4-phase output for the CP. The primary cell implements twice the number of delay elements as that implemented within the two secondary cells. This ensures that the time lag generated between the consecutive transitions of CLK 1A and CLK 2A is comparable to delay generated between CLK 2A and CLK 1B or CLK 1A and CLK 2B, due to the operation of two secondary cells.

The 4-phase output, from this circuit implementation thus maintains a finite and almost constant delay between any two consecutive switching edges, as shown in Fig. 4.3(b). The time-lag between introduced between the consecutive switching transitions, helps to minimize the shoot-through current in the clock buffer stages, and thus contributes directly towards improving the power efficiency of the charge-pump. Moreover, such an operation enhances charge-transfer efficiency by avoiding possible loss-of-charge occurring due to the overlap between various switching events in the CP operation.

However, the given switching scheme also determines the limit for maximum operating frequency (F_{IN_MAX}) that can be utilized for the Bootstrap CP implementation. From Fig. 4.3(b), the time-period (T_{PRD}) of the input period signal can be expressed in terms of the on-time (T_{ON}) of the charge-transfer switches and the delay (T_{DLY}) between consecutive switching transitions, as mentioned in (4.10).

$$T_{PRD} = 2 \cdot T_{ON} + 8 \cdot T_{DLY} \quad (4.10)$$

Since the logic gate delay, represented by T_{DLY} , is independent of T_{PRD} , from (4.10), it can be inferred that T_{ON} reduces as CP operating frequency (F_{IN}) is increased. For the CP operation under FSC regime, a lower T_{ON} results in significantly higher output impedance, thus limiting the driving capacity and usability of the given CP implementation. This suggests that a major limitation associated with Bootstrap CP implementation, is that it cannot be utilized a high switching frequencies, and this limitation arises due to the non-overlapping switching input required for its operation.

4.4.2.2 Negative Voltage Charge-Pump

The Bootstrap CP topology was qualitatively reviewed in section 2.4.3 along with a brief analysis of the charge-transfer mechanism facilitating its operation. In addition, a quantitative review of its operation was presented in section 2.5, whereby its simulated performance was contrasted with an equivalent Latched CP implementation. This section re-visits and analyzes the CP operation with respect to 2-stage Bootstrap CP implementation utilized in this work.

The two-stage bootstrap charge-pump used in the given work, is as shown in

Fig. 4.4: (a) 2-stage Bootstrap charge-pump in inverting configuration (b) 4-Phase switching input for Bootstrap CP

Fig. 4.4a. The 4-phase switching input driving the capacitive loads within the CP is marked in the Fig. 4.4b alongside. Since the NVG system, including digital blocks, is powered from a single supply input (V_{DD} : 3.3V), the digital logic and CP driver signals transition between 0V (logic 0) and 3.3V (logic 1), as marked in Fig. 4.4b. The given inverting configuration mainly consists of a cascade of 2 inverting stages followed by one output stage, connecting the final inverting stage to the CP output node. Each inverting stage comprises of a large charge-transfer switch (SW-#A), a small bootstrap switch (SW-#B), a charge-pumping capacitor (C_P), and a gate capacitor (C_G) connected at the gate of the corresponding charge-transfer switch. The output stage is identical to inverting stage, with the exclusion pump-capacitor and is instead terminated at the CP load capacitor (C_L), placed for

Fig. 4.5: CP initial settling transient (F_{IN} : 50MHz, I_L : $0\mu A$)

collecting the unregulated CP output. In order to hold and operate with negative voltages, at various nodes of the CP circuit, the CP utilizes deep-n-well devices for both charge-transfer and bootstrap switch implementation. As mentioned earlier, the deep-n-well devices with local source-body contact, do not suffer from body-effect related threshold voltage degradation, along the CP stages. The specific magnitude of the CP design parameters (C_P , C_G , C_L , switch-size, etc.) is derived by utilizing the CP operational analysis proposed in the following section.

The CP operation can be analyzed through the steady-state node voltage transitions for the given 2-stage bootstrap CP implementation. To aid with the qualitative explanation presented here, initially no-load condition is assumed and utilized for simulations. Once the CP is enabled (by setting the EN input (Fig. 4.4a) to logic 1(3.3V)), the steady-state is typically attained within $10\mu s$ as observed from the CP's initial settling transients (derived at F_{IN} : 50MHz, I_L : $0\mu A$), presented in Fig. 4.5. The corresponding steady-state node voltage (V_1 , V_2 , V_{CP}) and gate voltage (V_{G1} , V_{G2} , V_{G3}) transitions (at no-load condition) is as shown in Fig. 4.6 and Fig. 4.7 respectively.

With reference to periodic switching signals depicted in Fig. 4.4b, in Phase-1, the rising edge of CLK 2A turns on the bootstrap switches SW-1B and SW-3B. Consequently the gate of SW-1A and SW-3A acquire the potential at their

Fig. 4.6: CP node voltage transition at no-load (F_{IN} : 50MHz, I_L : 0 μ A)

Fig. 4.7: CP gate voltage transition (F_{IN} : 50MHz, I_L : 0 μ A)

corresponding source terminal ($V_1 = V_{G1}$, $V_{CP} = V_{G3}$, as evident from Fig. 4.7), thus causing SW-1A and SW-3A to turn off. This is followed by a falling edge of CLK 1A, which pulls down node voltage V_1 and turns off switch SW-2B. Finally, negative charge is shared across nodes 1 and 2 by turning on SW-2A via CLK 1B, resulting in V_1 and V_2 arriving at the same potential, as shown in Fig. 4.6.

In the next phase of the same period, CLK 1A and CLK 2A exchange polarity, thus raising node voltage V_1 and pulling down node voltage V_2 . In a complimentary operation executed in this phase, SW-2A is turned off by turning on SW-2B, while

Fig. 4.8: CP node voltage transition at finite load-current(F_{IN} : 50MHz, I_L : 200 μ A)

SW-1A and SW-3A conduct via CLK 2B input. The cyclical operation of CP thus ensure that every charge-transfer device is turned on once every period, such that direction of negative charge transfer is maintained towards the output node. Consequently, the average node voltage magnitude is boosted proportional to input switching amplitude, as charge is pumped across each inverting stage. Therefore, for the given 2-stage implementation, the CP output magnitude in absence of a load current, is proportional to the twice the input switching amplitude.

The steady-state node voltage transition in presence of a finite load current is as shown in Fig. 4.8. In this case, the CP operation is identical, however the node voltages V_1 , V_2 and V_{CP} are adjusted such that the charge-pumped across each CP stage, within the duration of its corresponding charge-transfer switch being turned on, is equal to the total charge injected by the load current in one time period ($I_L \cdot T_{PRD}$). Quantitatively, this can be expressed as (4.11)

$$C_P \cdot \Delta V_{1L} = C_P \cdot \Delta V_{1H} = C_P \cdot \Delta V_{2L} = C_P \cdot \Delta V_{2H} = I_L \cdot T_{PRD} \quad (4.11)$$

This charge-balance across CP stages maintains constant average voltage magnitude at various CP nodes, once the steady-state is attained.

4.4.3 Derivation of Charge-Pump Linear Model

A detailed review of the limitations with existing SC-CP analytical models is presented in section 2.3.2.3. The major drawback regarding the existing analyses is that it is largely based on the CP operation under slow-switching condition (SSC), which assumes that the node voltages across any CP stage, reach equal potential within the time duration for which the corresponding charge-transfer switch is turned on in a given time-period. This implies that the given on-time of the switches (T_{ON}) is sufficiently greater than the default time constant $\tau = (R_{SW} \cdot C_P)$ (typically for SSC $T_{ON} > 5\tau$ thus implying over 99% charge-transfer efficiency) associated with charge-transfer occurring across the cascaded SC-CP stages, where R_{SW} and C_P are the effective switch resistance and pump capacitance per stages. As a result the effect of R_{SW} and T_{ON} is suppressed and the CP output characteristic is considered to be independent of these parameters. This results in a rather simplistic and inaccurate prediction of the CP output impedance ($R_{CP} \approx N/(F_{IN} \cdot C_P)$) which further leads to incorrect deductions, such as considering the parasitic component of the current (I_{PAR}) to be linearly proportional to the load current (I_L). In general, the model predication do not agree well with the circuit level response, and are therefore not suitable to be utilized for a generic SC-CP operational analysis. Moreover, it is worth noting that the CP operation under SSC regime cannot be readily assured, and for any given SC-CP implementation, it is mainly determined by the design specification and instantaneous operating conditions. In other words, this implies that for a given design specification, it may not be practical or efficient to adapt the SC-CP design for SSC operation only.

To address such existing limitations, a novel SC-CP operational analysis, that is independent of CP operation under SSC or FSC regime, is proposed and utilized in this work. The given analytical model accurately captures the effect of non-zero switch resistance (R_{SW}) and finite on-time (T_{ON}) of the switches, and is thus used to extract the frequency-dependent CP linear model for the 2-stage Bootstrap CP implementation employed for realization of NVG system. The resulting analysis is further employed to derive the magnitude the CP design parameters (C_P , C_G , C_L , switch-size, etc.) to meet the required CP related specification, as obtained in section 4.4.2 on design methodology. Finally, the CP transfer characteristic predicted by the

Fig. 4.9: 2-stage Bootstrap CP's equivalent functional model

model is shown to be in close-agreement with simulation and measurement results obtained for the actual transistor level realization of the given CP. The close correlation between the results predicted by the proposed model and that obtained for its circuit level counterpart, suggests that it can be utilized for a generic SC-CP operational analysis, independent of the CP operating regime. Moreover, the equivalent model and analytical technique utilized here can be readily extended to other linear SC-CP topologies.

In order to facilitate a quantitative analysis of the steady-state CP operation, its circuit level implementation as depicted in Fig. 4.4, is represented using a equivalent functional model, as shown in Fig. 4.9. In this analytical model, the bootstrap switch is removed and the charge-transfer switch is replaced with a series combination of an ideal switch and fixed resistance (R_{SW}), modelling the average resistance offered by the charge-transfer device. The ideal switch state is controlled using the phases CLK 1B and CLK 2B of the input signal, identical to the ones used for the corresponding charge-transfer device, in its circuit level realization. In addition, the top-plate of each pump-capacitor is connected to a lumped combination of gate capacitor (C_G), and a small parasitic capacitance (C_{PAR}), to model the loss of charge at node 1 and node 2 at the switching transitions of CLK 1A and CLK 2A inputs, respectively. The gate capacitor C_G is included at the intermediate nodes, since in any given CP stage, the bootstrap switch is turned on before any switching transition (rising or falling edge) of the clock phase driving the respective pump-capacitor (C_P) in that given stage. The same can be observed from the 4-phase

periodic input waveform shown in Fig. 4.3(b), whereby it can be verified that, by default, any bootstrap switch remains turned on via the complimentary input clock phase driving the pump-capacitor in the previous (or following) stage. The parasitic capacitance at intermediate nodes is contributed from various sources, including the (i) top-plate parasitic capacitance of the integrated pump-capacitor, (ii) input gate capacitance of the bootstrap switch in the following stage, (iii) parasitics due to silicon implementation of large charge-transfer switching devices of the current and following stage, and (iv) parasitics due to the layout and interconnects among various device and passive elements. The model henceforth assumes a combined total parasitic capacitance (C_{PAR}) and includes it together with the gate capacitor C_G .

For the proposed quantitative analysis, the following assumption are made regarding the given CP analytical model and its associated operation, as described through it. Firstly, same parasitic capacitance (C_{PAR}) is assumed to be present at both CP intermediate nodes (node 1 and node 2) and its magnitude is considered to be independent of the CP operating frequency. Secondly, the effect of switching transitions of gate voltages (V_{G1} , V_{G2} and V_{G3}) on CP node voltages (V_1 , V_2 and V_{CP}) is neglected since the gate capacitor (C_G) is typically an order of magnitude less than the pump capacitor (C_P). Lastly, the effect of lumped capacitance ($C_{PAR} + C_G$) on the top plate of CP is not considered while deriving the charge-sharing equations corresponding to a charge-transfer switch being turned on. This is because the given lumped capacitance ($C_{PAR} + C_G$) is also significantly smaller than either of the pair of two capacitance (pair of pump capacitors C_P for inverting stages or pair of pump C_P and load C_L capacitor for output stage) among which charges are shared.

With regards to the CP analytical model, and the proposed operational analysis, the CP key design parameters are identified as the charge-transfer switch resistance (R_{SW}) the pump-capacitance per stage (C_P). These two design parameter play a pivotal role in determining the CP output transfer characteristics and therefore the CP optimization effort is mainly centred around selection of R_{SW} and C_P values, to achieve an optimized CP implementation meeting the design specification, as set in section 4.3. The other design parameters include the CP load capacitor (C_L) and the gate capacitor (C_G). The load capacitor is mainly required to limit the steady-

state ripple on the CP output for a given maximum load current specification. The gate capacitor does not have any observable impact on the CP output, however it is required for the Bootstrap CP operation as it effectively couples the input switching signal with the gate of charge-transfer switching device. The derivation of specific magnitude of all the design parameters is addressed in the following section, while synthesizing the required transistor level implementation of the CP. In addition to the design parameters, the major operating parameters determining the CP output are the CP load current (I_L), the CP operating frequency ($F_{IN}=1/T_{PRD}$) and the on-time of the switches (T_{ON}), representing the duration for which each charge-transfer device is turned on within one time-period. It is to be noted that unlike other two operating parameters, T_{ON} cannot be selected independently and is in fact dependent on the F_{IN} and the logic delay (T_{DLY}) implemented within the multi-phase clock generator, as mentioned in (4.9).

For a given load current, the typical node voltage transitions, once the steady state has been attained, are as shown in Fig. 4.10. This can be co-related with the actual steady-state node voltage transitions for the non-zero load current, depicted in Fig. 4.8. The suffix ‘H’ and ‘L’ represent the node voltages being pulled high or low in response to the respective switching signal transition, and suffix ‘(i)’ and ‘(f)’ represent the initial and final value of the node voltages before and after the completion of the charge transfer phase. The given representation of steady-state node voltages in Fig. 4.10 can be directly co-related with the circuit level implementation, depicted in Fig. 4.4. The cyclical movement of each node voltage, thus aids to visualize the complete steady-state CP operation, for a finite load current, whereby it can be observed how the average node voltage magnitude is reduced in proportion to the average switching amplitude, with each CP inverting stage. Moreover, the given node voltage transition diagram is invariant of the CP operation under FSC or SSC regime, and can also be extended to other linear SC-CP topologies.

The CP output transfer characteristics are derived by basically relating the intermediate node voltages V_1 , V_2 and the CP output V_{CP} , at the switching instants of charge-pumping clock phases; CLK 1A and CLK 2A, and after each charge transfer phase is completed. In this regard, the instantaneous change in the node voltage magnitude at the rising/falling edges of CLK 1A or CLK 2A can be estimated using

Fig. 4.10: Steady-state node voltage transitions

(4.12) and (4.13).

$$\text{Rising Edge: } V_{nH(i)} = V_{nL(f)} + V_{DD} \cdot \gamma \quad (4.12)$$

$$\text{Falling Edge: } V_{nL(i)} = V_{nH(f)} - V_{DD} \cdot \gamma \quad (4.13)$$

The terms V_n represent node voltages V_1 and V_2 , and V_{DD} is the input switching amplitude and for the given implementation is same as the input supply magnitude, common for the complete NVG system implementation. The factor γ , as mentioned before in section 4.2, is a technology dependent parameter modelling the loss of charge at the switching instants. For the Bootstrap CP implementation it can be readily derived using its analytical model shown in Fig. 4.9, as mentioned in (4.14).

$$\gamma = \frac{C_P}{C_P + C_G + C_{PAR}} \quad (4.14)$$

From (4.12), it can be observed that for the Bootstrap CP implementation, factor γ is dependent on the gate capacitor magnitude (C_G), besides the actual parasitic capacitance (C_{PAR}) occurring at the CP intermediate nodes. It follows that the C_G magnitude must be reduced to minimize the resulting loss of charge.

The charge-transfer equations correspond to each time a charge-transfer switch is turned on through the input clock phases of CLK 1B or CLK 2B. The resulting pair of equations are derived for the node voltage across the enabled charge-transfer device, by solving the corresponding resistive-capacitive (RC) charge-transfer sub-circuit, with the known initial conditions. As mentioned before, the effect of C_G and C_{PAR} on the charge-sharing is not considered due to their significantly smaller magnitude relative to the pump C_P or load C_L capacitor magnitude.

For the given 2-stage Bootstrap CP, the derivation of resulting charge-transfer

equations is elaborated as follows. With reference to Fig. 4.9 and 4.10, for the first inverting stage, switch SW-1A is turned on in the positive phase of CLK 1A, following the rising edge of CLK 2B, thus causing the node voltage V_{1H} to decay towards ground potential. The corresponding initial ($V_{1H(i)}$) and final node voltage ($V_{1H(f)}$) magnitude, as obtained at the end of this charge-transfer phase can be related using the RC branch formed using pump-capacitor of the first inverting stage, switch SW-1A, CP enable switch and ground. The resulting RC discharging equation is as mentioned in (4.15).

$$V_{1H(f)} = V_{1H(i)} \cdot \exp\left(\frac{-T_{ON}}{2R_{SW}C_P}\right) \quad (4.15)$$

Similarly, the second inverting stage is activated when CLK 1A is in negative and CLK 2A is in positive phase. Thus negative charge is shared across nodes 1 and 2, while the switch SW-2A is being turned on through CLK 1B input. The corresponding RC sub-circuit is formed between the pump-capacitors in the first and second inverting stages and the switch resistance (R_{SW}) modelling the effective on-resistance of SW-2A. The resulting RC charge-transfer equations, relating the node voltages V_{1L} and V_{2H} , can be described using (4.16)-(4.18).

$$V_{1L(f)} = \frac{IC_{12} - (C_P \cdot (V_{2H(i)} - V_{1L(i)})) \cdot \exp\left(\frac{-2T_{ON}}{R_{SW}C_P}\right)}{2C_P} \quad (4.16)$$

$$V_{2H(f)} = \frac{IC_{12} + (C_P \cdot (V_{2H(i)} - V_{1L(i)})) \cdot \exp\left(\frac{-T_{ON}}{R_{SW}C_P}\right)}{2C_P} \quad (4.17)$$

$$\text{where, } IC_{12} = C_P \cdot V_{1L(i)} + C_P \cdot V_{2H(i)} \quad (4.18)$$

Following the same analogy, the RC charge-transfer equations are derived for the CP output stage, with the inclusion of current source representing, load current injected at the CP output node. As observed from Fig. 4.10, the output stage is enabled concurrently with the first inverting stage, while CLK 1A is in positive and CLK 2A is in the negative phase. The charge sharing commences when SW-3A is turned on along with SW-1A, through the input clock phase of CLK 2B. The resulting RC series branch comprises of the pump-capacitor (C_P) in the second inverting stage, switch resistance (R_{SW}) corresponding to SW-3A, load capacitor (C_L) at the

CP output node and constant current source representing load current (I_L). The corresponding RC charge transfer equation, accounting for the presence of CP load current, are derived by relating the node voltages V_{2H} and V_{CP} , before and after the completion of charge-transfer phase, as given by (4.19)-(4.24).

$$V_{2L(f)} = \frac{IC_{20} + I_L \cdot (T_{ON} - R_{SW} \cdot C_{EQ})}{C_P + C_L} + D_1 \cdot e^{(-T_{ON}/R_{SW} \cdot C_{EQ})} \quad (4.19)$$

$$V_{CP(f)} = \frac{IC_{20} + I_L \cdot R_{SW} \cdot C_P + I_L \cdot (T_{ON} - R_{SW} \cdot C_{EQ})}{C_P + C_L} + D_2 \cdot e^{(-T_{ON}/R_{SW} \cdot C_{EQ})} \quad (4.20)$$

$$\text{where, } C_{EQ} = \frac{C_P \cdot C_L}{C_P + C_L} \quad (4.21)$$

$$IC_{20} = C_P \cdot V_{2L(i)} + C_L \cdot V_{CP(i)} \quad (4.22)$$

$$D_1 = \frac{I_L \cdot R_{SW} \cdot C_{EQ} - C_L \cdot (V_{CP(f)} - V_{2L(i)})}{C_P + C_L} \quad (4.23)$$

$$D_2 = D_1 \cdot \left(\frac{-C_P}{C_L} \right) \quad (4.24)$$

The terms IC_{12} and IC_{20} , as given by (4.18), (4.22), represents the total initial charge on the two capacitors among which charges are shared, before the charge transfer phase was initiated.

In addition to the charge sharing across CP stages, the CP output increases linearly due to the injected load current, for the duration switch SW-3A remains turned of, as shown in Fig. 4.10. This linear variation relates the initial and final node voltages at the CP output node, as described using (4.25).

$$V_{CP(i)} = V_{CP(f)} + \left(\frac{I_L}{C_L} \right) \cdot (T_{PRD} - T_{ON}) \quad (4.25)$$

The system of linear equations presented henceforth is complete and consistent, and can be utilized to derive the expression of various node voltage variables ($V_{1L(i)}$, $V_{1L(f)}$, $V_{1H(i)}$, $V_{1H(f)}$, $V_{2L(i)}$, $V_{2L(f)}$, $V_{2H(i)}$, $V_{2H(f)}$, $V_{CP(i)}$, $V_{CP(f)}$) in terms of CP design (R_{SW} , C_P , C_L , C_G) and operating parameters (I_L , T_{PRD} , T_{ON}). The resulting CP output response can be defined in terms of the average CP output voltage magnitude, as given by (4.26).

$$V_{CP} = \frac{V_{CP(i)} + V_{CP(f)}}{2} \quad (4.26)$$

The given system of equations is computationally analyzed to derive an expression for average CP output (V_{CP}), as defined in (4.24), in terms of CP design and operating parameters. The resulting analysis for the 2-stage Bootstrap CP, yields the following form for V_{CP} , as mentioned in (4.27).

$$V_{CP_AVG} = -2 \cdot V_{DD} \cdot \gamma + R_{CP_FXN} \cdot I_L \quad (4.27)$$

where R_{CP_FXN} is the effective CP output impedance function for the given 2-stage Bootstrap CP, and is further evaluated in terms of CP design and operating parameters, except load current.

The resulting linear model expression in (4.27) reveals the following important characteristic regarding the SC-CP output response. Firstly, it clearly verifies the linearity of CP transfer characteristic with respect to input load current. Secondly, it can be observed that the CP output at no-load ($V_{CP_0} = -2 \cdot V_{DD} \cdot \gamma$) is only dependent on the factor γ , besides being related to number of CP stages and switching amplitude. This suggest that it is mainly limited due the effect of parasitic and gate capacitance at the CP intermediate nodes. Thirdly, The CP output impedance is independent of the load current and the factor γ . The latter is possibly true for this model, since the effect of C_{PAR} and C_G is not considered deriving the RC charge-transfer equations. The CP output impedance is thus evaluated as function of all the remaining design and operating parameters of the CP.

The charge-pump output impedance function (R_{CP_FXN}) is analyzed and simplified by breaking it down into a sum-of-product expression. The approximated output impedance is obtained in varying degree of complexity, by adjusting the number of sub-terms included in the resulting function.

For simplification purposes, if $T_{ON} > 1.5 \cdot \tau (= R_{SW} \cdot C_P)$, then a closed-form expression for R_{CP} can be estimated with reasonable accuracy, as mentioned in

(4.28).

$$R_{CP_EST1} = \frac{T_{PRD} \cdot \left[2 \cdot C_L e^{\frac{T_{ON}(5C_L+2C_P)}{2R_{SW}C_LC_P}} + 4 \cdot C_L e^{\frac{T_{ON}(3C_L+C_P)}{R_{SW}C_LC_P}} + \dots \right. \\ \left. \dots + 5 \cdot C_P e^{\frac{T_{ON}(3C_L+C_P)}{R_{SW}C_LC_P}} + 2 \cdot C_L e^{\frac{T_{ON}(2C_L+C_P)}{R_{SW}C_LC_P}} - 2 \cdot C_L e^{\frac{2T_{ON}}{R_{SW}C_P}} - 4C_L \right]}{2 \cdot C_P \cdot (C_P + C_L) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_{EQ}}} - 1 \right) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_P}} - 1 \right)} \quad (4.28)$$

The approximated CP impedance expression (R_{CP_EST1}) in (4.28) can be further simplified by incorporating lesser number of constituent terms with higher magnitude, so as to obtain a more compact equivalent expression (R_{CP_EST2}) for the same, as given by (4.29). The details of the computational analysis and the associated MATLAB code utilized in this simplification of the CP output impedance function is elaborated in Appendix I.

$$R_{CP_EST2} = \frac{T_{PRD} \cdot \left[2 \cdot C_L e^{\frac{T_{ON}(5C_L+2C_P)}{2R_{SW}C_LC_P}} + 4 \cdot C_L e^{\frac{T_{ON}(3C_L+C_P)}{R_{SW}C_LC_P}} + 5 \cdot C_P e^{\frac{T_{ON}(3C_L+C_P)}{R_{SW}C_LC_P}} \right]}{2 \cdot C_P \cdot (C_P + C_L) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_{EQ}}} - 1 \right) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_P}} - 1 \right)} \quad (4.29)$$

The actual output impedance function (R_{CP_FXN}), as mentioned in (4.27), can be visualized via a 2-D plot, versus the pump capacitance (C_P) per stage, and the switch resistance (R_{SW}), as shown in Fig. 4.11. The variation of the output impedance magnitude can also be correlated quantitatively with temperature bar presented alongside. In the derivation of this plot, the additional CP design and operating parameters, as mentioned in the Fig. 4.11 caption, are set at the same magnitude as used for the actual circuit level operation of the CP. As depicted in Fig. 4.11, the surface of the output impedance function reveals that the CP output impedance magnitude initially decreases rapidly and then eventually saturate as C_P is increased or R_{SW} is decreased.

The intersection of this plot with a constant impedance plane, as shown in Fig. 4.11, traces the locus of the pair of C_P , R_{SW} values which the resulting CP implementation delivers same output impedance magnitude. The resulting intersecting curve can be identified as an exponential function which can be used to identify the theoretical limit of the maximum switch resistance (R_{SW_MAX}) and minimum

Fig. 4.11: 2D Plot of derived R_{CP} function versus pump-capacitance (C_P), switch-resistance (R_{SW}) (T_{PRD} : 20ns, T_{ON} : 7.8ns, C_L : 260pF)

pump capacitance (C_{P_MIN}) magnitude that can be allowed to achieve a given required output impedance magnitude (R_{CP_REQ}). This implies, that if for instance, in a given CP implementation, R_{SW} is greater than R_{SW_MAX} then the resulting CP output impedance (R_{CP}) will be higher than the required CP impedance (R_{CP_REQ}), irrespective of how high a value of pump-capacitor (C_P) is employed. Similarly, if some CP, C_P is lower than C_{P_MIN} , then also R_{CP} will be greater than R_{CP_REQ} , independent of the value of R_{CP_REQ} . The value of R_{SW_MAX} and C_{P_MIN} are only for reference purposes which simply indicate the lower bounds for pump-capacitor, and upper-bound for switch-resistance magnitude, as required for a SC-CP implementation to meet a given design specification, and therefore do not correspond to a practical or efficient CP implementation.

4.4.3.1 Derivation of CP Design Parameters

As per the CP specifications derived in the section 4.2, the given CP implementation is designed and optimized to derive an output impedance (R_{CP}) of 3.5kΩ, with the R_{CP} magnitude selected to be in the middle of the specification range. In this regard, the intersection of the CP output impedance surface plot with the constant impedance plane at 3.5kΩ is as shown in the Fig. 4.11. As observed from

Fig. 4.12: Charge-Pump output impedance versus (a) Switch resistance (R_{SW}) with $C_P: 15\text{pF}$ (b) Pump capacitance (C_P) for $R_{SW}: 230\Omega$

the intersecting curvature, it can be suggested that the most area efficient approach to meet the given specification, is to select the pump-capacitance (C_P) and switch-resistance (R_{SW}) combination for which CP output impedance magnitude is not saturated with respect to either of the two design variables. It should be noted that for a first-hand approximation, the dimensions of the switching device can be considered to be inversely proportional to the required switch-resistance magnitude.

The above mentioned technique is extended to the given design with the emphasis on utilizing a minimal silicon area for the integrated pump-capacitance and implement a reasonably sized switching device, to achieve the required area optimized CP implementation. Hence to achieve an R_{CP} of $3.5\text{k}\Omega$, the C_P and R_{SW} are selected as 15pF and 230Ω , respectively. Fig. 4.12 depicts the variation of R_{CP} with respect to C_P and R_{SW} , in two separate plots, with the corresponding fixed design parameter set at the selected value, as mentioned in the figure alongside. The remaining CP parameters are same as mentioned in the Fig. 4.11 caption. As highlighted in Fig. 4.12, it can be observed that for the selected C_P , R_{SW} pair, the rate of change of R_{CP} is reasonably high with respect to both the design parameters. Thus by simultaneously maximizing the slope of R_{CP} with respect to both C_P and R_{SW} , it can be ensured that the resulting CP implementation is obtained with optimal area utilization.

The charge-transfer time constant $\tau (= R_{SW} \cdot C_P)$ for the selected C_P (15pF)

and R_{SW} (230Ω) values is 3.45ns . Moreover, for the given CP utilizing 4-phase switching input, the on-time (T_{ON}) of switches can be expressed in terms of time-period (T_{PRD}) of the switching input, as mentioned in (4.13) and repeated here in (4.30).

$$T_{ON} = 0.5 \cdot T_{PRD} - 4 \cdot T_{DLY} \quad (4.30)$$

Considering an almost fixed logic gate delay $T_{DLY} \sim 0.55\text{ns}$, at 50MHz operating frequency (T_{PRD} : 20ns), the on-time T_{ON} is $\sim 7.8\text{ns}$. This implies,

$$1.5 \cdot \tau < T_{ON} \approx 2.2 \cdot \tau < 5 \cdot \tau \quad (4.31)$$

thus suggesting that at this operating frequency (i) CP is operating sufficiently outside the SSC regime and (ii) the condition for approximation of R_{CP} expression in (4.28) and (4.29) is met. At this operating point, the computed value for the actual output impedance R_{CP_FXN} (as derived from MATLAB) is $\sim 3506.8\Omega$. In contrast, the values for the corresponding counterpart approximated closed-form expressions are: $R_{CP_EST1} \sim 3479.3\Omega$ and $R_{CP_EST2} \sim 3460.9\Omega$. This initial verification adds credibility to the analytically derived approximations and is later further validated with circuit level CP implementation.

The switching device is sized such that its linear region on-resistance (R_{ON}) is comparable to the required switch resistance (R_{SW} : 230Ω). The on-resistance magnitude is estimated from the slope of the I-V output transfer curves in the linear region, for the deep-n-well switching device. It is numerically approximated in terms of the device dimension and the effective gate-to-source potential (V_{GS}), as given by (4.32).

$$R_{ON} \approx \frac{1}{k'_n(W/L)(V_{GS} - V_T)} \quad (4.32)$$

In this case, V_{GS} can be interpreted as the effective gate-to-drain (V_{GD}) potential, since the input negative voltage appears at the drain terminal of the charge-transfer switch. Furthermore, it can be observed that the effective V_{GD} at the instant a given charge-transfer switch is turned on, is significantly lower than the input switching amplitude (V_{DD}). This is because, the input negative voltage at the drain terminal is lowered due to the parasitic capacitance at this node and the gate capacitance at

Fig. 4.13: Pass-transistor (a) I_{DS} vs. V_{DS} (b) R_{ON} vs. V_{DS} , across varying device dimensions

the preceding stage, as is captured by loss factor γ and shown in (4.12). Similarly the gate voltage magnitude is reduced due to the input gate capacitance of the large charge transfer device. As a first hand approximation, the effective V_{GD} is set at half the switching amplitude (V_{DD}) and is further verified from the circuit level operation of the CP. Using the suggested value for V_{GD} , and plugging the values of process transconductance parameter (k'_n) and threshold voltage (V_T), as obtained from dc-operating point simulation, in (4.32), the switching device dimension is estimated at $((W/L) : \frac{40\mu m}{600nm})$, to provide an R_{ON} equal to 230Ω .

Fig. 4.13 presents the simulated I_{DS} vs V_{DS} curves for varying device dimensions and with V_{GD} at $0.5 \cdot V_{DD}$. As shown in Fig. 4.13, with the charge-transfer switch sized at $(\frac{40\mu m}{600nm})$, the simulated on-resistance (R_{ON}), derived at the slope of the output curves, is also in vicinity of the required R_{SW} magnitude of 230Ω .

The load capacitor (C_L) is required to limit the CP transient steady-ripple, especially at high load currents, to magnitude that is compatible with a given regulator implementation. The CP ripple magnitude can be approximated using the difference between the initial ($V_{CP(i)}$) and final CP output ($V_{CP(f)}$) voltages, before and after

the completion of charge-transfer phase, as given by (4.33).

$$V_{CP(i)} - V_{CP(f)} = \left(\frac{I_L}{C_L} \right) \cdot (T_{PRD} - T_{ON}) \quad (4.33)$$

Using (4.29), the CP output voltage ripple magnitude to under 50mV, for a maximum load current of $800\mu A$, the load capacitor magnitude is estimated as 260pF. This relatively large load capacitor is totally integrated on chip, within the pad limited area utilized for complete NVG system implementation. Therefore, no additional silicon area was consumed to accommodate the load capacitor. Besides limiting the CP's transient ripple magnitude, C_L is critically important to ensure the stability of the feedback loop. The detailed analysis of the effect of C_L on the regulator loop stability is addressed in the following chapter and is used to find identify the theoretical limits of its magnitude that can be used for reliable regulator operation.

In the given design, area utilization is prioritized over power efficiency optimization in order to achieve a compact realization for the fully-integrated charge-pump, which is not constrained with its operation in SSC or FSC regimes. The power efficiency optimization, as covered in a number of previous works [7], [12], [9], mandates the CP operation in SSC and typically results in an area intensive CP implementation. This design aims to explore the feasibility, design and trade-off involved with the CP operation when SSC operation cannot be ascertained. The analysis presented in this work aims to provide the tools for evaluation and optimization of CP output impedance, invariant of its operating regime. In the suggested optimization scheme the CP area utilization is fixed with the selection of the fixed design parameters (mainly C_P , R_{SW}). The power efficiency optimization is not ignored, but rather addressed later in the operating phase, through the selection of appropriate CP switching frequency. It can also be verified that for the selected $C_P(=15\text{pF})$, $R_{SW}(=230\Omega)$ values and at typical operating frequencies($F_{IN} \sim 20\text{MHz}-60\text{MHz}$), the CP is operating in the transition region between SSC and FSC regimes, thus implying the CP operation in the optimum operating region where its power efficiency is maximized.

The gate capacitor (C_G), should be significantly larger than the input gate capacitance of the charge-transfer switches, such that switches are turned on completely

in response to CLK 1B/CLK 2B inputs. At the same time, it should be as small as possible, so as to maximize the charge pump magnitude at no-load $|V_{CP,0}|$, as captured by loss factor γ . As a comfortable trade-off between the two constraints, a 0.48pF sized gate capacitor is used in this work.

It is also important to consider that for the given design, CP area optimization is achieved since the proposed CP operational analysis, as presented in the preceding section, provides a framework for CP implementation, invariant of its operation under FSC or SSC regime. For instance, the resulting area optimized CP implementation obtained here operates under FSC condition, to meet the given design specification. If the given CP was adapted for operation strictly under the SSC regime only, it would have delivered higher peak power efficiency at the cost of much larger silicon footprint, in terms silicon area utilization, for both pump-capacitor and charge-transfer switch. Such a CP implementation would not be practical for integrated applications or suitable for future applications demanding higher driving capacity with fully-integrated SC-CP implementation.

4.4.3.2 Validation and Limitations of the Derived CP Model

The proposed CP operational analysis and the derived linear model is verified by contrasting the CP output response with that obtained from the simulation results of its equivalent circuit level counterpart. In this regard, the given validation is presented at two levels. Firstly, the predicted linear transfer characteristics is compared with CP output response for the required negative voltage CP, implemented with the design parameters derived in the preceding section. The second level verification is presented by comparing the variation of CP output impedance across various CP design and operating parameters, as derived from analysis and corresponding simulations. Such an extended verification, clearly establish the authenticity of the proposed analytical model and its associated analysis, allowing it to be utilized for other potential SC-CP applications.

The schematic of the transistor level implementation of 2-stage Bootstrap CP, utilizing the design parameter values derived in the previous section, is as shown in the Fig. 4.14. The dimensions of the charge-transfer and bootstrap switch, along with magnitude of other parameters is also mentioned in the Fig. 4.14 alongside,

Fig. 4.14: 2-stage Bootstrap CP with derived values of Design parameters

thus representing the complete circuit level implementation of negative voltage CP utilized for the NVG system implementation. The CP performance is firstly characterized by evaluating the CP output magnitude versus load current, for a given CP operating frequency (F_{IN} : 50MHz), as obtained for this specific CP implementation.

In Fig. 4.15, the resulting linear CP transfer characteristic, as predicted by the proposed analysis and as captured in the extracted linear model expression in (4.27), is presented alongside the results obtained from the pre-layout and post-layout simulation of its circuit level counterpart. For the actual circuit level operation, the CP output response does initially exhibit slight non-linearity at low-load currents, however, it can be observed to be strictly linear for load currents beyond $200\mu A$. The pre and post-layout simulated curves are therefore linearly extrapolated from its linear operating region, as highlighted in Fig. 4.15, so as to locate the corresponding magnitude charge-pump output at no-load ($|V_{CP,0}|$) and thus facilitate its comparison with the analytical model. It can be further noted that the CP output magnitude is always higher than the corresponding value obtained from its linear interpolation, thus ensuring that the given non-linearity does not affect the system level operation.

The corresponding linear model expression as extracted from the linear interpolation of simulated curves and as derived from the operational analysis, for the given set of design parameters, is also mentioned in the Fig. 4.15 alongside. Assuming the lumped parasitic capacitance at the intermediate nodes to be 10% of the pump capacitance magnitude (C_p : 15pF), the loss factor γ , as given by (4.14), is initially set at 0.85. Thus, for the analytical model, the CP output at no-load is predicted at -5.61V, and can be observed to lie in the middle of the values predicted

Fig. 4.15: Comparison of charge-pump output voltage (V_{CP}) vs. load current (I_L), as obtained from Analysis, Pre-layout and Post-layout simulations

by the simulations results. In fact the resulting $|V_{CP,0}|$ magnitude is about 5% below and 10% above the corresponding values predicted by pre and post-layout simulations, respectively. As analyzed in the previous section, the CP design parameters are optimized such that CP provides an output impedance (R_{CP}) of 3500Ω . The corresponding CP output impedance obtained from the circuit level simulations is 6.8% higher for the pre-layout and only 1.1% higher for the post-layout simulations, as compared to the required R_{CP} value of 3500Ω . The given comparative results for the CP output transfer characteristic thus demonstrate the close agreement between the actual circuit level operation and the results predicted from the proposed operational analysis.

It can be further emphasized that this observed close co-relation between analysis and simulations is obtained for CP operation under FSC regime. For the given CP implementation, the CP operating frequency is 50MHz, which corresponds to an on-time (T_{ON}) of 7.8ns, while the default charge-transfer time-constant ($\tau = R_{SW} \cdot C_P$) is 3.45ns. Due to the comparable magnitude of T_{ON} and τ , the CP can be regarded as to be operating under FSC condition. This further validates the fact that the proposed operational analysis is invariant of CP operating regime, and can therefore be extended to any generic linear SC-CP implementations.

The residual errors between the analysis and simulations, as seen before, arise mainly due to the inherent differences between the analytical model and the CP operation at the transistor level. This can be further elaborated as follows, specific to the Bootstrap CP implementation used in the given design. Firstly, the charge-transfer switch does not operate in the linear region throughout the duration for which it is turned on. The switch initially operates in saturation region when turned on in with the rising edge of CLK 1B or CLK 2B inputs, and then subsequently drifts into linear region, once its drain-source (V_{DS}) voltage falls below its overdrive potential ($V_{GS} - V_T$) due to on-going charge-transfer across it. Thus in principle, the switching device cannot be directly substituted with its linear region on-resistance equivalent, for the complete charge-transfer phase. Secondly, for the actual circuit level operation, the charge-transfer switch turns on partially with falling edge of CLK 1A or CLK 2A itself (respective clock phase driving the pump-capacitor in the previous stage), and is then turned on completely with rising of CLK 1B or CLK 2B driving its gate capacitor. Thus, the charge-transfer is initiated with transition of CLK 1A/CLK 2A, and is then resumed with reduced switch resistance in the positive phase of CLK 1B/CLK 2B input. This effect is not considered in the simplified analysis adopted for the analytical model. Thirdly, the value of loss factor γ is not known a priori, since it is based on estimating the parasitic capacitance magnitude (C_{PAR}) to be a certain percentage of integrated pump-capacitance (C_P) magnitude, for a given process and technology node. Moreover the frequency dependence associated with its magnitude is not captured by the given model. In practice, γ is a technology dependent parameter which is sensitive to PVT variations and typically its magnitude is reduced with increasing CP operating frequency and vice-versa.

In spite of the above limitations, the proposed CP analytical model is demonstrated to accurately predict CP output transfer characteristics. the results predicted by the analysis are verified with corresponding circuit level simulations and the derived CP output impedance function is further validated across varying CP design and operating parameters. The CP model mimics the circuit level operation while incorporating the effect of non-zero switch resistance (R_{SW}) and finite on-time (T_{ON}) of the switches. Consequently, the resulting operation analysis is invariant of CP operation FSC or SSC regime. It should be noted that although the CP op-

Fig. 4.16: Charge-flow across CP inverting stage at steady-state

erational analysis and the resulting derivation of the CP linear model is specific to the given 2-stage Bootstrap CP implementation, it can readily extended to N-stage generic linear SC-CPs as well. For the general case with N-stages, a closed-form expression for R_{CP} may not be attainable, however its magnitude can be evaluated in terms of CP parameters through iterative calculation.

4.4.4 SC-CP Efficiency Analysis and Optimization

As mentioned and analyzed earlier in section, the charge-pump power efficiency is defined as the ratio of power delivered at the output to the power consumed by the CP. Utilizing the linear model expression for CP output magnitude, for a generic N-stage linear SC-CP implementation, the CP power efficiency (η_{Eff}) can be expressed in terms of its effective output impedance (R_{CP}) and the loss factor γ , as expressed in (4.34).

$$\eta_{Eff} = \frac{V_{OUT} \cdot I_L}{V_{DD} \cdot I_{TOT}} = \frac{(N \cdot |V_{DD}| \cdot \gamma - I_L R_{CP}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{DIG})} \quad (4.34)$$

The terms $(N \cdot I_L)$ in the denominator is current drawn from the supply for the N-stage linear SC-CP, to maintain charge-balance across its inverting stages, once the steady-state has been attained. The flow of charge during steady-state can be visualized using Fig. 4.16. In any given CP inverting stage, the CP draws unit load current from the supply when the clock input driving the respective pump-capacitor is in positive phase. As highlighted, the current is drawn via the PMOS device at the output of the buffer stage and the charge flows through the switching device and two pump-capacitors, until it sinks through the NMOS device of the buffer cell

driving the pump-capacitor in the preceding stage. This component of total input current ($N \cdot I_L$) is only determined by the instantaneous load current magnitude and does not contribute towards CP efficiency degradation since it evens out with the boosting of CP output magnitude by a factor of N as well.

The term I_{DIG} represents the additional current consumed within the digital circuits employed to generate the periodic input switching signals for the CP. It mainly includes the current consumed within the digital logic gates of the multi-phase clock generator and the shoot-through current consumed within the buffer stages driving the capacitive loads within the CP. The I_{DIG} thus represents the additional input power dissipated within the CP which results in reduction of the CP efficiency. The I_{DIG} magnitude is independent of the load current while varying strictly linearly with the CP operating frequency (F_{IN}) and is directly proportional to the square of the supply magnitude (V_{DD}), as given by (4.35).

$$I_{DIG} = \kappa \cdot (V_{DD})^2 \cdot F_{IN} \quad (4.35)$$

The proportionality constant κ depends on a given technology and the specific implementation of the digital circuitry, and relates the total additional power dissipation to the operating parameters (F_{IN} , V_{DD}). It is therefore affected by factors such as number of delay cells implemented within multi-phase clock generator, sizing of devices within the buffer cells, parasitic capacitance encountered by the buffer stage driving the pump-capacitor etc.

From (4.30), the degradation of CP efficiency can be attributed to three main factors. Firstly, it is contributed by the parasitic capacitances (along with gate capacitance C_G) occurring at CP intermediate nodes, which result in reduction of the CP output magnitude at no-load ($|V_{CP,0}| = N \cdot V_{DD} \cdot \gamma$), as captured by the loss factor γ . Secondly, it occurs due to the reduction in CP output magnitude as a consequence of its finite output impedance (R_{CP}), which essentially leads to reduction in the power delivered to the output. Thirdly, the efficiency is degraded due to the additional input power dissipated within the digital logic gates, as is represented by the additional current I_{DIG} drawn from the input supply. For a given CP implementation, the effect of various design parameters on the CP efficiency is captured through the expression of CP output impedance, while the effect of CP operating

Fig. 4.17: Charge-Pump power-efficiency (η_{Eff}) vs. load-current

frequency is captured by both R_{CP} and I_{DIG} . The overall CP efficiency variation with respect to the two main operating parameters, namely load current (I_L) and operating frequency (F_{IN}) is analyzed and explained in the following sections.

4.4.4.1 SC-CP Efficiency Across Load Current

The circuit level simulations for the CP efficiency (η_{Eff}) versus load current, for the given 2-stage Bootstrap CP implementation, as derived at 30MHz and 50MHz operating frequencies, is as shown in the Fig. 4.17. As observed from Fig. 4.17, the CP efficiency magnitude is low at both low and high load currents, attaining its peak value at given load current magnitude (I_{L_MAX}), specific to a given CP operating frequency (F_{IN}). This is because, at low-load currents, the numerator of (4.30) vanishes while the denominator is non-zero due to the finite DC power dissipated in the digital circuitry. Therefore CP efficiency is minimal at low-loads, irrespective of other design and operating parameters. As load current is increased, the terms I_{DIG} remains constant, while the component of input current proportional to the load, increases rapidly by a factor of N . Consequently, at high load currents, I_{DIG}

becomes negligible in comparison to $(N \cdot I_L)$, thus allowing η_{Eff} to be approximated using (4.36).

$$\eta_{Eff} = \frac{(N \cdot |V_{DD}| \cdot \gamma - I_L \cdot R_{CP})}{V_{DD} \cdot N} \quad (4.36)$$

As inferred from (4.32), for further increase in load current, the numerator reduces due to the finite CP R_{CP} , while the denominator remains constant. Therefore the CP efficiency decreases rapidly for load current beyond which (4.32) is valid.

The expression for I_{L_MAX} can be obtained in terms of CP linear model parameters by maximizing CP efficiency expression in (4.34), as derived in (4.37).

$$I_{L_MAX} = \frac{\sqrt{I_{DIG} \cdot R_{CP} \cdot (\gamma \cdot N^2 \cdot V_{DD} + I_{DIG} \cdot R_{CP})} - I_{DIG} \cdot R_{CP}}{N \cdot R_{CP}} \quad (4.37)$$

The corresponding magnitude of maximum efficiency (η_{Eff_Max}) can be evaluated by using (4.33) in (4.30). The resulting deductions for I_{L_MAX} and η_{Eff_Max} can be simultaneously correlated with the simulated efficiency curves present in Fig. 4.17. For instance at 50MHz, derived peak η_{Eff} estimated using (4.30) is , while that obtained from post-layout simulations is . The I_{DIG} magnitude used for analysis is obtained from corresponding simulations, and is considered be constant across load current. Thus the minor difference obtained between analysis and simulation arises primarily due to difference in CP output impedance as obtained from the two techniques. The same correlation for the peak CP η_{Eff} magnitude can be shown to be valid at other CP operating frequencies. Therefore, the CP frequency dependent model, as derived from the proposed operational analysis, also facilitates a realistic prediction of CP efficiency, besides accurately predicting CP output transfer response, with respect to CP's design and operating parameters.

From Fig. 4.17, it can be further observed that the CP efficiency is higher for 30MHz till a particular cross-over load current (I_{CROSS}) magnitude, beyond which η_{Eff} at 50MHz is higher than that at 30MHz. Furthermore, as CP F_{IN} is increased, the value of I_{L_MAX} is increased while the corresponding peak CP efficiency (η_{Eff_Max}) magnitude is reduced. This given efficiency vs load current profile is obtained due to an interplay of two parameters, namely the CP output impedance (R_{CP}) and the current consumed within digital circuitry, as denoted by (I_{DIG}). The variation of R_{CP} as derived from its analytical model, and the variation

Fig. 4.18: Charge-Pump output impedance (R_{CP}) and digital current consumption (I_{DIG}) vs. CP operating frequency (F_{IN})

of I_{DIG} as obtained from circuit simulations, with respect to F_{IN} , is presented in Fig. 4.18. The CP output impedance is inversely proportional to F_{IN} as was shown in (4.26), while I_{DIG} increases linearly with input frequency, as mentioned in (4.31). Therefore, for the 30MHz operation, I_{DIG} is lower, resulting in lower input power dissipation, however R_{CP} is higher, causing lower power delivered to the load. The vice-versa hold true for 50MHz F_{IN} . Thus, with regards to CP efficiency, for $I_L < I_{CROSS}$, the effect of lower I_{DIG} at 30MHz is dominant, resulting in higher efficiency for 30MHz, while beyond I_{CROSS} , the effect of lower R_{CP} at 50MHz is stronger, thus resulting in its corresponding efficiency exceeding that obtained at 30MHz.

From the above analysis it follows that to maximize efficiency, the CP can be operated at low operating frequencies at low-load currents. However, it is to be noted that at low F_{IN} , the CP magnitude is also reduced to a higher effective R_{CP} . Hence the minimum operating F_{IN} is set by the regulator specifications such that it can be ensured pass-transistor is not driven into the linear region for a given load current specification.

4.4.4.2 SC-CP Efficiency Across Operating Frequency

The simulated CP efficiency versus operating frequency (F_{IN}) for the given 2-stage CP, as derived at $300\mu A$ and $500\mu A$ load currents, is presented in Fig. 4.19. In order to assist with the analysis, the CP output impedance function (R_{CP_FXN}) as

Fig. 4.19: Charge-pump power-efficiency (η_{Eff}) versus operating frequency (F_{IN})

obtained through the analytical model, is superimposed with the given efficiency characterization curves. The variation of R_{CP_FXN} with respect to F_{IN} is derived using computation analysis of the original R_{CP} expression, obtained without approximations, as utilized in (4.27). As observed from Fig. 4.19, the CP efficiency increases rapidly with F_{IN} till it maximizes at an optimum frequency input (F_{IN_OPT}), specific to the injected load current magnitude. Beyond F_{IN_OPT} , η_{Eff} decreases almost linearly, till it suddenly drops down at a particular frequency threshold and settles to minimal magnitude after that.

The given CP efficiency vs F_{IN} characteristic curves are obtained due to combined effect of CP output impedance (R_{CP}) and digital power consumption ($I_{DIG} \cdot V_{DD}$) with respect to the F_{IN} , as was presented in Fig. 4.18. The R_{CP} magnitude is shown to be inversely proportional to F_{IN} , as derived in (4.28). However, for the CP operation under FSC condition (such as the given CP implementation), R_{CP} is also strongly dependent on the finite on-time (T_{ON}) of charge-transfer switches, as concluded from the proposed analysis of the CP operation and evident from the approximated R_{CP} expression derived in (4.28) and (4.29). The effective T_{ON} is in turn inversely proportional to F_{IN} ($= 1/T_{PRD}$), as was estimated in (4.10) for the

4-phase input switching generator, and is re-framed here in (4.38).

$$T_{ON} = 0.5 \cdot T_{PRD} - 4 \cdot T_{DLY} \quad (4.38)$$

The relation between T_{ON} and T_{PRD} can also be verified using the circuit level simulations, which for the given multi-phase clock generator and CP implementation is as derived in (4.39).

$$T_{ON} = 0.5 \cdot T_{PRD} - 2.228 \cdot 10^{(-9)} \quad (4.39)$$

The empirical relation obtained in (4.38) complies with (4.39), and is utilized in the computation of the R_{CP} as a function of F_{IN} , as presented in Fig. 4.18. From (4.38), (4.39), it is verified that the T_{ON} decreases linearly with T_{PRD} , implying that it contributes towards increase in R_{CP} magnitude as F_{IN} is increased. Therefore, as F_{IN} is increased, R_{CP} initially decreases rapidly as a result of the faster charge-transfer occurring across the CP stages. The rate of change of R_{CP} eventually slows down as it saturates and attains its minimum value (R_{CP_MIN}) at particular frequency (F_{IN_MAX}). Beyond this frequency, R_{CP} increases marginally due the reduction in T_{ON} with the increasing F_{IN} , as observed from Fig. 4.18. Since the CP output does not yield any incremental gain beyond F_{IN_MAX} , it can be regarded as the maximum operating frequency (F_{IN_MAX}) for the CP. It can be noted that if that if the T_{ON} was assumed to be constant then the R_{CP} variation with respect to F_{IN} would have been similar to the current one, with the exception that instead of attaining a minimum value, it would have been an asymptote with respect to F_{IN} axis.

The CP efficiency variation with respect to F_{IN} can be explained using the above mentioned analysis for R_{CP} as a function of F_{IN} . At low operating frequencies, the high CP output impedance results in lowering of CP output magnitude. This translates in low output efficiency, irrespective of the load current and other CP design parameters. As F_{IN} is increased, the CP magnitude is increased due to lowering of R_{CP} , however the input power consumption also increases linearly with F_{IN} , as shown in Fig. 4.18. The net effect results in CP efficiency being maximized at an optimum frequency input (F_{IN_OPT}). As frequency is increased

further, the trend for digital power dissipation continues while the incremental gain obtained for increase in CP output magnitude is reduced due to the continuous reduction in rate of change of R_{CP} with F_{IN} . As a result, for $F_{IN} > F_{IN_OPT}$, the CP efficiency decreases linearly till F_{IN_MAX} . For frequencies higher than F_{IN_MAX} , the CP efficiency suddenly plummets down to low magnitude. This rapid reduction in efficiency magnitude occurs due to the combined effect of continued linear increase in digital power dissipation and the onset of the reduction in CP output magnitude, resulting from increase in R_{CP} for $F_{IN} > F_{IN_MAX}$.

From Fig. 4.19, it can be observed that the frequency beyond which the simulated CP efficiency suddenly drops in magnitude, coincides with the theoretical estimate of maximum CP operating frequency (F_{IN_MAX}), as obtained from the analysis of CP output impedance function (R_{CP_FXN}). This further validates the effectiveness of the proposed CP operational analysis and highlights the applicability of the derived analytical results for CP efficiency characterization.

4.4.4.3 CP Efficiency Optimization

The CP operation can be optimized to derive maximum power efficiency by way of selecting an appropriate operating frequency (F_{IN_OPT}), corresponding to the required circuit operation at a given regulated output (V_{REG}) and load current (I_L). This selection of F_{IN_OPT} is ensured that the CP is tuned for most power efficient performance while meeting the given design specifications. Based on the suitability and priorities of the end application, it can be implemented for the stand-alone CP module or at the system level, including the regulator module. The former is relative straightforward and mainly defines the selection criteria F_{IN_OPT} within the constraints of design requirements. The latter is more involved and provides additional design equations for the circuit level CP implementation such that end-to-end system level at given operation point can be maximized. The detail regarding the application of these techniques is provided as follows.

Certain applications which involve variation in the regulated output tuning range for a fixed load current specification, can target to maximize to the efficiency of the stand-alone CP module. For a given load current the CP efficiency is maximized at an optimum frequency (F_{IN_OPT}), as seen from Fig. 4.19, and analyzed in the

previous section. However since CP is operating in tandem with the linear regulator arrangement, it follows that the design constraints imposed by the given regulator implementation should also be incorporated. Firstly, the required CP output impedance (R_{CP_REQ}) can be estimated for a given combination of regulated output voltage and load current, as presented in section 4.3, and mentioned here in (4.40).

$$R_{CP_REQ} = \frac{(N \cdot V_{DD} \cdot \gamma) - |V_{REG}| - |V_{DO}|}{I_L + I_{REG}} \quad (4.40)$$

where $|V_{DO}|$ is pass-transistor dropout voltage at the given load current I_L , and I_{REG} is the current consumed within the regulator module. Following this, the CP output impedance derived at the F_{IN_OPT} can be recorded as R_{CP_OPT} . It now follows that, for the given operating point, if the $R_{CP_OPT} < R_{CP_REQ}$, then the CP can be operated at F_{IN_OPT} to derive max power efficiency from it. However, if this condition is not met, then the CP needs to operated at the next higher frequency at which CP impedance (R_{CP}) is equal or below R_{CP_OPT} . Conversely, (4.40) can also be used to estimate the minimum regulated output (V_{REG_MIN}) at a given load current for which the CP can be continued to operate at F_{IN_OPT} , as given by (4.41).

$$|V_{REG_MIN}| = (N \cdot V_{DD} \cdot \gamma) - |V_{DO}| - R_{CP_OPT} \cdot (I_L + I_{REG}) \quad (4.41)$$

This operation maintains sufficient headroom across the pass-transistor as required for it to operate in saturation region or at the dropout condition, thus ensuring that the regulator feedback loop remains active with high loop gain. It can be noted that for this case, although CP efficiency is maximized, the overall system efficiency can be quite compromised. This is because, for $R_{CP_OPT} < R_{CP_REQ}$, while the CP is operated at F_{IN_OPT} , a larger than required headroom is maintained across pass-transistor, which results in addition power dissipation across regulator and thus reduces the system level efficiency.

The end-to-end system level efficiency can also be maximized for certain applications with a set operating point at a given regulated output voltage (V_{REG}) and load current (I_L). From the on-going discussion, it follows that such an efficiency optimization can be achieved by simultaneously maximizing the efficiency of the CP module and ensuring that regulator module is operated under the dropout condi-

tion. In this regard, the first design equation is same as (4.34), whereby the required CP impedance (R_{CP_REQ}) corresponding to the given operating point is evaluated. The second design equation is obtained by maximizing the CP efficiency expression in (4.30) at an optimum operating frequency F_{IN_OPT} , as given by (4.42).

$$\frac{d\eta_{Eff}}{dF_{IN}} = \frac{d}{dF_{IN}} \left(\frac{(N \cdot |V_{DD}| \cdot \gamma - I_L R_{CP}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{DIG})} \right) = 0 \quad (4.42)$$

In (4.42), the CP output impedance (R_{CP}) is substituted with the required impedance value (R_{CP_REQ}), as evaluated in (4.40). The term I_{DIG} , denoting the current consumed within digital circuits, varies linearly with F_{IN} , as was shown in Fig. 4.18. For a given CP implementation, it can be empirically derived using representative circuit simulation, as mentioned in (4.43).

$$I_{DIG} = (49.33669 * 10^{(-12)}) * (F_{IN}) - (18.6605 * 10^{(-6)}) \quad (4.43)$$

Thus, by using (4.40) and (4.43) in (4.42), the solution of (4.42), provides an estimate of the F_{IN_OPT} . The third and final design equation is obtained by equating the CP output impedance magnitude (R_{CP}) at F_{IN_OPT} , to the required CP output impedance (R_{CP_REQ}), as mentioned in (4.44).

$$R_{CP}(F_{IN}, R_{SW}, C_P, C_L) = R_{CP_REQ} \quad (4.44)$$

The expression for R_{CP} in (4.44) can be the original expression (R_{CP_FXN}), derived through computational analysis, or its approximated equivalent, as mentioned in (4.28) or (4.29). In either case, the on-time of switches (T_{ON}) needs to be substituted in terms of F_{IN} using (4.39), in order to obtain the resulting R_{CP} expression as a function of only F_{IN} and CP design parameters.

Using the value/expression of R_{CP_REQ} from (4.40) and F_{IN_OPT} from (4.42) in (4.44), the solution of (4.44) yields a non-trivial solution relating the CP design parameters (R_{SW} , C_P , C_L) for the given regulated output and load current values. Since the load capacitor (C_L) magnitude is mainly determined by the steady-state ripple magnitude specification, the given analysis provides a useful relation between the switch-resistance (R_{SW}) and pump-capacitance (C_P) magnitude

to achieve system-efficiency optimized CP implementation, at the given operating point. However, since the optimization flow is only applicable for a pre-determined fixed operating condition, it is not utilized for the negative voltage CP employed within the NVG system implementation.

4.5 Design and Analysis of Negative Voltage Regulator

This section presents a detailed design and analysis of the linear regulator implemented as part of the proposed NVG system. In section, firstly the given regulator topology is introduced at the functional level and the practical design constrained associated with its circuit level implementation are explored. This is followed by the analysis of the transistor level implementation of the regulator sub-circuits including the supply independent bias generator and symmetrical OTA as the error amplifier. Finally, the regulator PSRR performance with respect to both of its supply rails is presented and the section is concluded with an analysis of the maximum load supported by the given topology, while the incorporating the effect of the finite CP output impedance.

4.5.1 Cascaded Linear Regulator Implementation

The negative voltage regulator module receives the unregulated CP output as input and provides low-ripple, low-noise regulated negative voltage as its output. In this design, it is configured in an inverted linear-regulator arrangement, as shown in Fig. 4.20. The main sub-circuits module include a supply-independent bias-generator, a low-power, high-bandwidth error amplifier, and a deep-n-well pass-transistor. In the given arrangement, the positive rail for the regulator (V_{POS}) can be shared with global 3.3V supply input or be provided from a second source, while the negative rail is the connected to the output of the CP. In other words, the unregulated CP output serves both as the negative power rail and noisy input to the pass-transistor, for the regulator to operate upon and provide regulated negative voltage output. Therefore, in effect, the fully-integrated CP powers the regulator active circuits, despite its limited driving capacity, due to its relatively high output impedance (R_{CP}) magnitude.

Fig. 4.20: Negative voltage regulator including frequency dependent CP model

The difference between the given and conventional linear regulator also arises due to R_{CP} magnitude and is analyzed in the following section.

Since the CP output is the most-negative potential of the circuit, the given regulator configuration allows negative voltage magnitude for the gate voltage (V_G) of the pass-transistor, derived as the output of the error-amplifier. While the regulator is in operation, the V_G magnitude is adjusted to dynamically modulate the on-resistance (R_{ON_PT}) of the pass-transistor, such that feedback voltage (V_{FB}) is driven equal to external reference input (V_{REF}). In addition to deriving the regulated output (V_{REG}) at the desired magnitude, the high loop-gain enables minute high-frequency adjustments to the R_{ON_PT} magnitude such that CP output transient ripple at its operating frequency (F_{IN}), and the CP output noise at F_{IN} harmonics, are effectively suppressed. The regulated negative voltage is thus derived as low-ripple, low-noise output with lowered output impedance.

The required tuning for the regulated output is derived by adjusting the ratio of the resistor dividers, as given by (4.45).

$$V_{REG} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) - V_{POS} \cdot \left(\frac{R_1}{R_2}\right) \quad (4.45)$$

In the given design, the positive rail (V_{POS}) magnitude can be varied from 0V to 3.3V input, while the low-noise reference input (V_{REF}) has to be maintained 1.1V below the V_{POS} magnitude, in order to maintain sufficient headroom for the input

differential pair within the error amplifier. It can be noted that for a given load current (I_L), the regulated output can be tuned from $-|V_{CP} - V_{DO}|$ to V_{REF} , where V_{CP} and V_{DO} are the CP output and the dropout voltage of the pass-device at the given I_L setting. The effect of CP noise and transfer characteristic on regulator and system level performance is captured through inclusion of its frequency dependent linear model, as derived in the previous section and as highlighted in Fig. 4.20. This enables an accurate prediction of the circuit's DC operating quiescent point and thus facilitates a realistic analysis of regulator and system level performance metrics, from both small and large signal prospective.

The high output impedance of the fully-integrated CP has major implications on the design and implementation for the regulator at the transistor level. Firstly, it results in wide variation in the available headroom for the regulator, for the supported range of load currents. For instance, at 50MHz, the CP output magnitude varies from -5.12V at no-load to -1.7V at 800 μ A load current. Secondly, the limited driving capacity for the fully-integrated CP structure dictates minimal power consumption within regulator active circuits. Moreover, this power consumption should remain relatively constant across its operating range. This is important to ensure that maximum usable margin is reserved for the supported load current for a given regulated output. Conversely, this also translates into wider output tuning range for a given load current specification.

To overcome these challenges, firstly, the regulator sub-circuits employ thick gate oxide devices, instead of using cascoding techniques. These devices with high V_{GS} and V_{DS} breakdown limits ($> 8.5V$), provide immunity against the large headroom at low load currents, while ensuring high loop gain, when the available headroom is shrunk at high loads. In terms of the device reliability, the worst-case for steady-state DC stress occurs for the pass-transistor device itself. Considering a max V_{REF} input at 2.2V (for 3.3V), the maximum V_{DS} across pass-transistor is under 8V, which is well below for the (worst-case) minimum V_{DS} breakdown limit of 8.5V for the thick gate oxide devices implemented in the given 180nm technology node. This also explains the reason behind limiting the CP to a 2-stage implementation. In addition, the error amplifier is a low-power OTA implementation and the bias current for the same is provided using a supply independent bias generator. This

ensures minimal variation in the regulator current, across the wide output range of the charge-pump. Thus allowing the regulator to effectively withstand the wide variation in its available headroom and operate reliably, while maintaining a high loop gain, across its entire envelope of operation.

The negative feedback loop is stabilized using a single off-chip capacitor (C_{EXT}) which determines the location of dominant pole along with the load resistance (R_L). A minimum value of 220nF for C_{EXT} ensures unconditional stability for the feedback loop for the supported range of load currents. The relatively small sizing of the pass-transistor ensures that the pole formed at its gate lies outside the unity-gain bandwidth, despite the high output impedance of the OTA. The low -3dB frequency set by the dominant pole ($\omega_{p1} \approx 1/(C_{EXT} \cdot R_L)$) along with high loop-gain magnitude effectively suppresses the CP noise and high R_{CP} to produce low-noise, regulated negative output with lowered output impedance.

4.5.2 Supply-Independent Bias Generator

The transistor level schematic of the supply-independent bias-generator is as shown in Fig. 4.21. The circuit utilizing known $R_B = 1/g_m$ technique provides bias current (I_B) for the error-amplifier which is independent of the voltage magnitude at both the supply rails, to a first degree of approximation. The devices MN1, MN2, MP1 and MP2 are arranged to form local positive feedback loop which force a non-zero supply-independent constant current through both its branches. The device MP2 is sized to be N times larger than MP1 to ensure a positive voltage drop across the bias-resistor (R_B). The devices MP3, MP4 and bias-capacitor (C_B) constitute the part of start-up circuitry which pushes the loop to rapidly acquire its non-zero steady state, once the regulator is powered up.

The design equation determining the bias current magnitude (I_B) can be readily derived in terms of the source-gate voltages of MP1 (V_{SG1}) and MP2 (V_{SG2}), as shown in (4.46).

$$V_{SG1} - V_{SG2} = I_B \cdot R_B \quad (4.46)$$

Assuming equal threshold voltage for both the devices, (4.46) can be extended to the overdrive potential across these devices, and thus allow it to be represented

Fig. 4.21: Supply-independent bias-generator

in terms of bias current magnitude, as shown in (4.47).

$$\sqrt{\frac{2I_B}{k'_n(W/L)_1}} - \sqrt{\frac{2I_B}{k'_n(W/L)_2}} = I_B \cdot R_B \quad (4.47)$$

In the given design the value of multiplier factor N for MP2 is kept at 4, which implies that bias current magnitude can be readily evaluated in terms of biasing resistor R_B and the dimension of MP1, as mentioned in (4.48).

$$I_B = \frac{1}{2 \cdot (R_B)^2 \cdot k'_n \cdot (W/L)_1} \quad (4.48)$$

In the given design the integrated R_B magnitude is set at approximately 100k Ω , which corresponds to an I_B magnitude of approximately 1 μ A, at normal process and temperature corner. The corresponding total regulator current variation is maintained under 15 μ A across the entire variation in CP output voltage (V_{CP}), varying from -5.1V at no-load to -1.7V at 800 μ A load current. To effectively counter the large variation in CP output magnitude, the output bias voltage V_{BN} tracks V_{CP} in order to maintain constant gate-source potential for MN1 and MN2 as required

Fig. 4.22: Small-signal gain-phase plot of (V_{BN}/V_{CP})

for the given bias current. This implies, that the biasing performance can also be assessed in frequency domain by observing the ratio of node voltages V_{BN} and V_{CP} . The corresponding AC simulation at various V_{CP} magnitude (at DC) is shown in Fig. 4.22.

From Fig. 4.22 it can be observed that V_{BN} effectively tracks V_{CP} till frequencies higher than the typical maximum operating frequency ($F_{IN_MAX} \approx 70\text{MHz}$) employed for the CP used in this design. This suggests the bias current is shielded from the transient steady-state ripple occurring at CP operating frequency, and thus the bias circuit prevents the CP noise from being injected into the error-amplifier/regulator.

The positive feedback loop has an additional stable operating point at zero bias current with all four devices within the loop turned off. Therefore the start-up circuit is indispensably required to ensure that the loop reliably acquires its second stable state with non-zero bias current. Assuming the positive and negative supply rails are initially active, at time $t=0$, MP3 is turned on, as its gate is at 0V, while MP4 is turned off since its gate shared with gates of MP2 and MP1, is tracking the positive rail potential (V_{POS}) in the initial zero I_B stable state. Consequently current is dumped at the drain of diode connected MN2, which is mirrored in MN1 and is

Fig. 4.23: Initial transient waveform for bias voltage (V_{BN}) and bias-current

thus regenerated within the positive feedback loop, thereby pushing the circuit to acquire its second stable state. As loop is activated, MP4 is tuned on which charges bias capacitor C_B , till V_{POS} and thus causes MP3 to eventually turn off.

A small magnitude of C_B , such as 300fF used in this design, is suffice to maintain reliable start-up operation while obtaining a very low start-up time. The resulting initial transient waveforms for bias voltage and bias current are as shown in Fig. 4.23. As observed, the total start-up time with given magnitude of C_B is below 100ns for various CP output magnitude. In contrast, the time required by the stand-alone CP (used in this design) to attain stead-state is in tens of microseconds. At the system level, the CP initially acquires a steady-state with low negative voltage output magnitude ($-1V < |V_{CP,0}| < -2V$) due to high in-rush current from the discharging external capacitor. The biasing circuit is verified to operate normally with such low $|V_{CP,0}|$ — magnitude while maintaining a start-up time under 100ns, across all operating conditions. The low start-up time of the bias circuit ensure that its operation does not conflicts with the system level settling transients.

Fig. 4.24: Symmetrical operational-transconductance-amplifier (OTA) as error-amplifier

4.5.3 Error-Amplifier

A low-power symmetrical operational-transconductance-amplifier (OTA), as shown in the Fig. 4.24, is utilized as the error-amplifier, in the given negative voltage regulator implementation. The OTA does not contain any internal high impedance nodes, which results in wider OTA bandwidth for a given power consumption. This also contributes towards improving the stability of the regulator feedback loop as the regulator frequency response is not affected by the OTA's internally generated poles/zeros. In addition, the structure has inherently low-offset due to symmetry of design and requires only single biasing input, resulting in a simpler implementation for the biasing circuit. The biasing current is distributed proportionally among various OTA branches by virtue of various current mirrors implemented as part of OTA topology. The gain is derived from the relative high impedance of the output stage.

To achieve a lower power design, the OTA is designed to operate with a total current of $60\mu\text{A}$, across the entire operating range. This current budget is distributed equally among the four OTA branches, via the current mirror pairs. The minimum required headroom (V_{HD_MIN}) for the OTA is defined by the overdrive voltages (V_{OV}) of current-source MN#1 (V_{OV_N1}), differential-pair MN#3A/3B (V_{OV_N3}) and

current-mirror MP#1A/1B (V_{OV_P1}), as given by (4.49).

$$V_{HD_MIN} = V_{OV_N1} + V_{OV_N3} + (V_{OV_P1} + |V_T|) \quad (4.49)$$

where $|V_T|$ representing the threshold voltage of NMOS/PMOS devices, varying from 0.72V to 0.8V, in the given technology node (GF180nm CMOS). The V_{OV_N1} is same as the overdrive potential of the corresponding mirror transistor in the biasing circuit, which is sized for a V_{OV} magnitude of approximately 100mV. The differential pair and current-mirrors devices are sized for an overdrive voltages of 150mV and 350mV respectively, at the given $15\mu\text{A}$ of bias current per branch. The larger sizing of the differential pair results in higher DC gain from the OTA and helps to reduce the input referred noise. A relatively smaller sizing of current mirrors, corresponding to a higher V_{OV_P1} , is selected, since typically a large headroom ($> 4\text{V}$) is available, even at high load currents. Considering a maximum threshold voltage magnitude of 0.8V, using (4.49), it can be inferred that the OTA can operate with input headroom voltage greater than 1.4V. This implies that if the positive supply (V_{POS}) is at 3.3V input, the OTA can operate normally even at load currents for which the negative voltage CP output is above 0V. From Fig. 4.24, the input common mode range for the reference input (V_{REF}) can also be estimated in terms of the overdrive potentials as mentioned in (4.50).

$$V_{CP} + V_{OV_N1} + V_{OV_N3} + V_T < V_{REF} < V_{POS} - V_{OV_N3} \quad (4.50)$$

The V_{REF} input magnitude is thus required to be 1.1V above the CP output magnitude ($|V_{CP,0}|$) and 150mV below the V_{POS} magnitude. The V_{REF} magnitude is desired to be as high as possible to maximize the regulated output voltage range, however in practice, it must be maintained at least 1.1V below the V_{POS} magnitude. This is essential to ensure that the differential-pair is operating in the deep saturation region, thus allowing the OTA to derive maximum gain from its single gain stage configuration.

The open-loop frequency response for OTA output at various CP output voltages, is as shown in the Fig. 4.25. The total biasing current within OTA varies from $\sim 67\mu\text{A}$ for CP output at -5.1V at no-load, to $\sim 53\mu\text{A}$ for CP output at -1.7V at

Fig. 4.25: Open-loop frequency response of the error-amplifier

800 μ A of maximum load current. As the biasing current reduces with the increasing load current, the corresponding OTA gain (at DC) increases from 48.9dB at no-load to 56.7dB at max. load (I_{L_MAX} : 800 μ A). The corresponding 3-dB cut-off frequency remains higher than 2.5MHz.

In the given OTA implementation, cascoding is intentionally avoided for two main reasons. Firstly, it results in lesser parasitic effect on the OTA frequency response and thus helps to maximize the achievable OTA bandwidth at its output. Secondly, it facilitates wide input and output voltage range, which is required to keep the regulator feedback loop active under the large variation in CP output magnitude. As mentioned previously, the OTA along with the bias-generator is implemented with thick gate oxide devices to withstand the large headroom magnitude created low-load currents. Within the OTA, the maximum steady state stress is on the output device MP#2B, at low-load currents, when the output is pulled towards the negative rail while CP output magnitude is the highest. However, since the (worst-case) V_{DS} and V_{GS} breakdown limits for employed thick gate devices is higher than the maximum available headroom, reliable operation for the regulator can be ensured across the entire operating range of the design.

4.5.4 Regulator PSRR performance

The PSRR response of the regulator can be examined with respect to either of its two supply rails: the positive rail V_{POS} and the negative supply rail V_{CP} , which is the unregulated CP output.

To start with V_{POS} , the PSRR performance would depend if the feedback (V_{FB}) and reference (V_{REF}) inputs are derived from the same supply or a separate low-noise input source(s), as shown in Fig. 4.20. In principle, the overall system can operate with single positive dc input by deriving both the V_{FB} and V_{REF} through a simple resistor divider arrangement, referenced to V_{POS} . From Fig. 4.20, it can be observed that the stand-alone PSRR performance of the regulator is over -56dB PSRR (at DC). However, if V_{POS} is shared with the feedback resistor divider, the noise on V_{POS} rail directly reaches the regulated output (V_{REG}) via the feedback node (V_{FB}), as evident from regulated output ideal response

$$V_{REG} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) - V_{POS} \cdot \left(\frac{R_1}{R_2}\right) \quad (4.51)$$

The same reasoning can be extended if V_{REF} is derived directly from V_{POS} . Consequently, in either case, or when single positive V_{POS} is utilized, the PSRR performance will be significantly compromised ($>-10\text{dB}$).

The PSRR performance with respect to negative rail or V_{CP} at different loading conditions is as shown in Fig. 4.27. This PSRR ($PSRR_{CP}$) is perhaps more important as it can be interpreted in terms of the ac rejection offered by the given regulator topology to the noise injected from the CP. It can be observed that this $PSRR_{CP}$ follows a first-order response, whereby it can be verified that the rejection magnitude at DC is proportional to the DC gain and the corresponding -3dB roll-off frequency proportional to the unity gain frequency of the regulator, at the given load current setting. As this FOM quantifies the CP noise rejection, a detailed small-signal analysis for the same, validating the above mentioned findings, is presented in the following chapter.

Fig. 4.26: Regulator PSRR with respect to positive rail (V_{POS})

Fig. 4.27: Regulator PSRR with respect to negative rail (V_{CP})

4.5.5 Maximum Load vs Regulated Output

The given regulator implementation is similar to a linear regulator arrangement, however the major difference in its operation and performance arises due to the high output impedance (R_{CP}) of the fully-integrated charge-pump. In a conventional linear regulator, the input line voltage, observed as the magnitude of drain-source

potential across the pass-transistor (V_{DS_PT}), is constant for given regulated output (V_{REG}) and independent of the instantaneous load current (I_L). Therefore, to maintain regulation, the increase in load current is compensated with a equivalent increase in gate-source potential (V_{GS_PT}) of the pass-transistor. As load current is increased the pass-transistor operation gradually transitions from saturation towards linear region. The operating point at which the pass-transistor is operating at the onset of the linear region known as the dropout condition and the corresponding I_L threshold is considered as the maximum supported load current (I_{L_MAX}) for the given regulated output, since the regulation effectiveness decreases rapidly for further increase in load current magnitude. In the given regulator topology, the same operating principle is followed, however the increase in I_L is accompanied by a decrease in V_{DS_PT} due to the high R_{CP} of the CP. This results in a much larger increase in V_{GS_PT} for the same increase in I_L magnitude. Consequently the dropout condition for the pass-transistor is reached at lower I_L magnitude as compared to a conventional regulator.

The I_{L_MAX} corresponding to a V_{REG} for the given regulator topology, can be derived by solving the CP linear model expression in conjunction with dropout condition of the pass-transistor. The corresponding design equation are as mentioned in (4.52) - (4.54).

$$V_{DS_PT} = V_{REG} - V_{CP} \quad (4.52)$$

$$V_{CP} = V_{CP_0} + (I_{L_MAX} + I_{REG}) \cdot R_{CP} \quad (4.53)$$

$$V_{DO} = V_{DS_PT} = \sqrt{\frac{2 \cdot I_{L_MAX}}{k'_n \cdot (W/L)_{PT}}} \quad (4.54)$$

where I_{REG} is the regulator current and is assumed to be constant at $50\mu A$ for the numerical evaluation of I_{L_MAX} . The quadratic equation in formed using (4.52) - (4.54), results in two solution for I_{L_MAX} , among which only one solution is valid and can be correlated with corresponding circuit simulation. The corresponding expression for I_{L_MAX} for the valid solution is as derived in (4.55).

$$I_{L_MAX} = (V_{REG} - V_{CP_0})/R_{CP} + I_{REG} + \dots + \frac{\sqrt{1 + 2 \cdot R_{CP} \cdot k'_n \cdot (W/L)_{PT}(V_{REG} - V_{CP_0} - I_{REG} \cdot R_{CP})} - 1}{(R_{CP})^2 \cdot (W/L)_{PT} \cdot k'_n} \quad (4.55)$$

Fig. 4.28: Maximum supported load current (I_{L_MAX}) vs. regulated output (V_{REG})

In addition to the above mentioned quantitative analysis for I_{L_MAX} , it can also be estimated from the feedback loop characteristics, as obtained from regulator's circuit simulations. This implies that the maximum load current can be considered as the current magnitude above which the DC gain of the feedback loop falls below a certain threshold value. The latter interpretation of I_{L_MAX} is more realistic as it also incorporates the effect of error-amplifier and is based on the actual circuit level operation of the regulator.

In Fig. 4.28, the I_{L_MAX} vs V_{REG} curve as obtained from the quantitative analysis is presented along with the equivalent curves derived from circuit simulations, for a DC gain threshold of 55dB. It can be observed that the two curves are in good agreement for regulated output below 0V. For $V_{REG} > 0V$, the difference between the two curves increases, as the quantitative analysis predicts a continued linear increase while the simulation counterpart tends towards saturation of I_{L_MAX} magnitude. The reason behind this observed divergence between the two results is revealed as the reduction in pass-transistor transconductance parameter (k'_n) with the increasing load current. The variation of k'_n magnitude and the corresponding DC-Loop gain for V_{REG} at 1.5V with respect to input load current is as shown in the Fig. 4.29.

Fig. 4.29: Pass-transistor transconductance (k'_n) vs. load current (I_L) (V_{REG} :1.5V)

4.6 System Integration

The given design is implemented on silicon using GlobalFoundries 5-metal, CMOS 180nm BCDlite process. The corresponding layout, marking the pad labels and the silicon footprint of multi-phase clock generator, the fully-integrated inverting SC-CP and negative voltage regulator, is shown in Fig. 4.30. The silicon implementation includes 290pF of total integrated MIM capacitance, with 15pF per-stage pumping capacitance, for the 2-stage CP, and the rest 260pF of CP load capacitance. The active area of the clock-gen, CP and regulator modules are, while the design occupies a total area $0.55mm^2$, including testing pads.

The integrated capacitance, utilized throughout the design, is realized using Metal-1 to Metal-3 MIM capacitor, providing a capacitance density of $1.0596fF/\mu m^2$. A variant of the same MIM capacitor, with twice the capacitance density, is offered in the same technology, however was not being made available to us, for this round of fabrication. For this design, as true for other integrated switched-capacitor based regulated voltage generators, since most of the active area is used by integrated capacitance, an increase in MIM capacitance density can result in almost proportional decrease in total (active) area utilization. The MIM capacitor is preferred over other integrated CP realizations (MOS capacitor, MOM-capacitor), due to its higher stability, higher linearity (with respect to supply voltage), lower PVT variation in

Fig. 4.30: Layout of the NVG prototype chip, fabricated in GlobalFoundries CMOS 180nm BCDlite process

absolute capacitance magnitude, and most importantly, lower top and bottom plate capacitance, which directly impact the CP output response. Due to these properties, they are ideally suited for such applications, requiring a high capacitance magnitude, despite their higher integration cost, incurring from the additional process steps involved in their fabrication. In contrast, the MOM capacitances are better suited for smaller capacitance implementation with priority on achieving better matching, while the MOS capacitances provide a high capacitance density with a fixed DC voltage input, and are therefore mainly utilized for on-chip supply decoupling applications.

The digital circuits including multi-phase clock generator along with buffer cells, are implemented using standard 3.3V devices, while the fully-integrated SC-CP and the negative voltage regulator are realized using thick gate-oxide, 6-terminal (deep-n-well) NMOS and 5-terminal (isolated n-well) PMOS devices. As compared to the standard device, the isolated-well PMOS and NMOS devices require significantly larger area, while the thick-gate oxide variant offers higher input gate capacitance, due to substantially large minimum feature size (L_{MIN} : $0.6\mu\text{m}$). However, despite these drawbacks, these devices are inevitably required for optimal system design, for two main reasons. Firstly, since each device is implemented in its own well, a local source-body connection is permitted. This prevents the threshold voltage (V_T) modulation due to body-effect, both along the CP cascaded stages, and within the regulator, thus making such devices ideally suited for operating with negative voltage. Secondly, the thick gate-oxide variant, offered in this technology, provides

Fig. 4.31: Typical and worst-case (WC) device-breakdown limits for the thick gate-oxide, deep-n-well device

high V_{GS} , V_{DS} and p-n junction breakdown limits, which helps to contain the steady-state stress on the devices within safe bounds, thus ensuring device-level reliability, and thus facilitating a robust system implementation.

The typical and worst-case breakdown limits for the given thick gate-oxide devices, for this technology, are as depicted in Fig. 4.31. As part of the device-stress analysis, it can be observed, that the maximum steady-state stress is on the pass-transistor device itself. The worst case operating point occurs at no/low-load conditions, while the regulated output is maintained at its maximum value (V_{REG_MAX} : 2.1V). At this operating point, the V_{DS} for the pass-transistor exceeds 7V, however, it is still maintained safely below the worst-case V_{DS} breakdown limit of 8.5V. Therefore, despite their larger area and higher input capacitance, the application of these devices is required to ensure device reliability, while operating under the large head-room generated across the positive and negative voltage rails. This also explains the rationale behind limiting the number of CP stages to two, for the given linearly regulated system implementation.

4.7 Chapter Summary

This chapter presented a detailed review of the circuit design and analysis of the fully-integrated SC-CP, negative voltage regulator and the overall system level implementation of the proposed NVG. In this chapter, firstly a systematic design methodology is outlined and adapted for the design and verification of the proposed NVG

system.

Following this, a novel SC-CP operational analysis, incorporating the effect of finite on-time of the switches and non-zero switch resistance, is proposed and is used to derive a closed-form expression of CP output impedance. The analytical results are utilized to obtain the required CP implementation by optimizing it for minimum area utilization. The CP transfer characteristics predicted by the analytical model is contrasted and verified with the corresponding circuit simulations. In addition, CP efficiency variation versus load current and operating frequency is analyzed.

This is followed by the design and operational analysis of the negative voltage regulator. The effect of CP output response is captured by incorporating the derived CP linear model in the regulator simulation setup. The transistor level implementation of the regulator sub-circuits is examined in detail and the maximum supported load current is quantitatively analyzed. Finally the system level implementation is presented and practical aspects related to its silicon realization are discussed.

Chapter 5

System Level Analysis and Verification

5.1 Introduction

The proposed NVG system is implemented as a combination of a fully-integrated CP and a linear regulator module, as detailed in the previous chapter. The negative voltage regulator receives both the input and power through the unregulated output of the CP, which is characterized with high output impedance and high noise-content. Consequently, the CP output response impacts the stability of the regulator's feedback loop frequency and affects the overall settling transients. Therefore, to accurately predict and evaluate system stability and performance, it is essential to capture and quantify the effect CP output, on the system level response. Moreover, due to specific transfer characteristics of the given fully-integrated CP, it follows that the overall system level functionality and performance must also be rigorously verified across its operating range, besides the block level verification of the given CP and regulator modules.

In this regard, this chapter presents a detailed analysis and verification of the proposed NVG system, while incorporating the effect of CP output on various performance parameters. The system level functionality and performance is verified from both small-signal and large-signal prospective. The small-signal analysis includes verification of the stability of the regulator's feedback loop and evaluation of the noise rejection provided by the given regulator topology to the noise injected from

the CP. The large signal verification includes a quantitative analysis of the complete settling characteristics and an estimation of total settling time as a function of CP, regulator and operating parameters. The effect of CP output response is captured by including the (CP operating frequency dependent) CP linear model, in both the analytical models and in the regulator simulation setup, as was shown in Fig. 4.20. The results and equations derived for both the small and large signal analyses is consistently verified with corresponding circuit level simulation. Finally, to validate the findings from the analyses while ensuring a robust and repeatable performance output, the system level functionality is verified through transient co-simulation of CP and regulator modules.

The chapter is organized as follows. In this following section, small-signal analysis for the verification of feedback loop stability is presented. An equivalent small-signal model is introduced and resulting loop-transfer function is analyzed to capture the effect of CP output response on the feedback loop stability characteristics. In addition, the impact of CP linear model parameters (CP output impedance (R_{CP}), CP load capacitor (C_L)) and the external capacitor's ESR resistance, on the stability performance parameters is analyzed. This is followed by an AC analysis of the CP noise rejection provided by the given regulator topology. In this section also, a representative small-signal is presented and the resulting noise-transfer function is derived to analyze the AC response of the regulator. In the next section, a first level large signal verification is presented through the derivation and analysis of the complete settling characteristics, as obtained for the given combination of fully-integrated CP and regulator modules. The presented quantitative analysis is used to derive a numerical solution for the settling transients and thus provide estimation of total settling time. Finally, system level verification through transient co-simulation of CP and regulator is presented, and a brief conclusion is drawn.

5.2 Stability of the Feedback-Loop

The circuit level schematic of the NVG system used for small-signal analysis is as depicted in the Fig. 5.1. The corresponding small-signal parameters (transconductance (g_m and output conductance ($g_{ds} = 1/r_{ds}$)) for each device/device pairs are

Fig. 5.2: Small-signal model for verification of feedback loop-stability

200 μ A), as detailed in section 3.2. As a result, the parasitic pole formed through the combination of high-output impedance of the OTA ($\approx r_{ds_OTA}/2$) and C_{GS_PT} , is pushed well beyond the unity-gain frequency (ω_u) of the feedback loop, and therefore does not have any impact of the loop-transfer characteristics. Therefore the specific sizing of pass-transistor is critical towards improving the stability criteria if the regulator feedback loop, which as analyzed below, is already compromised due to the fully-integrated CP transfer characteristics. At the circuit level, this implies that the error amplifier does not require any additional buffer stages to drive the pass-transistor and therefore translates to simpler regulator implementation with lower power consumption. It is also to be noted that the large pass-transistor dropout voltage results in tighter design constraints for the resulting CP implementation, specifically requiring a lower CP output impedance (R_{CP}) for a given number of CP stages (N), and a given regulated output and load current specification.

The open-loop transfer function obtained by breaking the loop at the feedback node is derived to be of the form as given by (5.1).

$$H(s)_{STB} \approx \frac{Av_{DC_STB}(1 + s/\omega_{z1})}{(1 + s/\omega_{p1}) \cdot (1 + s/\omega_{p2})} \quad (5.1)$$

The corresponding expressions for dc-loop gain (Av_{DC_STB}), dominant pole (ω_{p1}), and the additional pole (ω_{p2}) and zero (ω_{z1}) formed in the loop transfer function, in

terms of the small-signal model and CP parameters, is as derived in (5.3)-(5.6).

$$A_{vDC_STB} \approx \frac{[(-g_{m_diff} \cdot R_L) \cdot (g_{m_PT} - R_{CP} \cdot g_{ds_PT} \cdot g_{ds_np})\beta]}{g_{ds_np} \cdot (2R_L \cdot g_{ds_PT} + R_{CP} \cdot g_{m_PT} + R_L R_{CP} \cdot g_{ds_PT} \cdot g_{ds_np} + 2)} \quad (5.2)$$

$$\omega_{p1} \approx \frac{2R_L \cdot g_{ds_PT} + R_{CP}(2g_{ds_PT} + g_{m_PT}) + 2}{R_L C_{EXT} \cdot (2 + R_{CP} \cdot (2g_{ds_PT} + g_{m_PT})) + 2R_{CP} C_L} \quad (5.3)$$

$$\omega_{p2} \approx \frac{R_L C_{EXT} \cdot (2 + R_{CP} \cdot (2g_{ds_PT} + g_{m_PT})) + 2R_{CP} C_L}{2R_L C_{EXT} \cdot R_{CP} C_L} \quad (5.4)$$

$$\omega_{z1} \approx \frac{g_{m_PT} - R_{CP} \cdot g_{ds_PT} \cdot g_{ds_np}}{R_{CP} \cdot C_L \cdot g_{m_PT}} \quad (5.5)$$

The total dc-loop gain (A_{vDC_STB}) is a cascade of the gain derived from the OTA ($\approx g_{m_OTA} \cdot r_{ds_OTA}/2$) and the gain obtained from the pass-transistor output stage ($\approx -g_{m_PT} \cdot (R_L || r_{ds_PT})$). The feedback loop is stabilized through the low-frequency dominant pole ($\omega_{p1} \approx 1/(C_{EXT} \cdot R_{OUT})$) formed by the off-chip capacitor (C_{EXT}) and the effective output impedance ($R_{OUT} = R_L || r_{ds_PT}$) as seen by the pass-transistor. The detailed expressions for A_{vDC_STB} and ω_{p1} , capturing the effect of CP parameters (R_{CP} , C_L), is obtained through the evaluation of given small-signal model, as mentioned in (5.2) and (5.3). In addition, the fully-integrated CP transfer characteristics also results in the formation of a pole-zero pair (ω_{p2} , ω_{z1}), as given by (5.4) and (5.5). The numerical magnitude of various terms identified in the loop-transfer function mentioned in (5.1), is evaluated by utilizing the values of various small-signal parameters (g_{m_OTA} , g_{ds_OTA} ($=1/r_{ds_OTA}$), g_{m_PT} , g_{ds_PT} ($=1/r_{ds_PT}$)) as obtained from the corresponding dc-operating point simulation, along with the actual magnitude of design and operating parameters (C_L , C_{EXT} , R_L). The magnitude of ω_{p2} and ω_{z1} reveals that they are located close to each other, at frequencies slightly higher than the unity-gain frequency (ω_u).

5.3 Parametric Variation of the Feedback-Loop Stability Parameters

The circuit level simulations for the gain-phase plots at various loading conditions is as shown in Fig. 5.3. The corresponding variation of key loop-stability parameters,

Fig. 5.3: Gain-phase plot for the small-signal stability verification of the feedback loop

Fig. 5.4: DC loop-gain ($A_{v_{DC_STB}}$), phase-margin (PM) and unity-gain bandwidth (UGB) vs. load current (I_L) ($V_{REG} = -1.2V$)

namely DC loop-gain $A_{v_{DC_STB}}$, phase-margin (PM) and unity-gain frequency (ω_u , with respect to an increasing load current, is as presented in Fig. 5.4. At low-load currents ($I_L < 50\mu A$), the DC loop-gain is relatively high while low frequency dominant pole (ω_{p1}) is shifted to lower frequencies due to the high output impedance

at the pass-transistor. Consequently, the feedback loop is easily stabilized with a 90° PM and a low magnitude of unity-gain frequency (ω_u), despite the high DC loop-gain magnitude. At high load currents, the dominant pole is shifted outwards to higher frequencies while the DC loop gain is reduced. Thus, following the trends of a single-pole system, the unity-gain frequency magnitude remains relatively low and constant. As a result, at high-loads, the feedback loop is stabilized with $> 80^\circ$ PM, thus implying minimal impact from the addition poles and zeros on the overall loop transfer response. The worst-case for loop-stability occurs at mid-load conditions when the gain derived from both the OTA and the pass-transistor stage is simultaneously at its maximum magnitude. Consequently, the overall DC loop-gain is maximized and corresponding ω_u is also shifted outwards, to be located in the vicinity of the additional pole-zero pair (ω_{p2} , ω_{z1}) formed in the loop transfer function. The relative spacing of ω_{p2} and ω_{z1} and their location with respect to effective ω_u , results in the observable drop in the PM at mid-loading conditions, as shown in the Fig. 5.4. It can be further observed that, due to the combined effect of the closely located pole-zero pair in the vicinity of ω_u , the PM first drops and then stabilizes, while the slope of DC loop gain-remains almost constant at 20dB/decade.

To rigorously verify that the derived gain-phase plots and the observed drop in PM is not affected by the parasitic pole formed at the gate of pass-transistor, the loop stability is re-investigated with an ideal gate-source (C_{gs_IDL}) capacitance added across pass-transistor. The nominal value of C_{gs_PT} (as extracted from DC operating point simulation) with given sizing of pass-transistor, is below 12fF, while the added C_{gs_IDL} is varied from 10fF to 50fF in the regulator simulation setup, thus mimicking a 4x increase in pass-transistor sizing. Fig. 5.5, shows that drift in the phase plot and the observed shift in PM, corresponding to the given C_{gs_idl} variation, at the previously depicted worst-case PM operating point at mid-load conditions. The minimal variation observed in the phase plot and PM magnitude, with respect to a significantly large variation in C_{gs_IDL} , firmly establishes that C_{gs_PT} magnitude has loop- minimal impact on the open loop transfer response.

The gain-phase plots obtained from the circuit-level simulations can thus be closely co-related with the open-loop transfer function derived using its equivalent small-signal model. In addition, the phase-margin for the feedback loop is main-

Fig. 5.5: PM vs pass-transistor gate-source capacitance (C_{gs_PT})

tained over 51° , for all possible combinations of regulated output voltages and load currents, supported within its operating envelope. Thus, by utilizing exhaustive set of circuit level simulations, the proposed small-signal analysis is verified and the stability of the regulator feedback loop is ensured across the operating range.

5.3.1 Impact of Charge-Pump transfer Characteristics

The impact of fully-integrated CP transfer characteristics on the feedback loop stability can be analyzed by observing the variation in gain-phase plots and the resulting stability parameters with respect to CP parameters. The CP output response is captured primarily through its output impedance (R_{CP}) and CP load capacitor (C_L), as included in the small-signal model. The CP linear model is included in the regulator simulation setup, thus resulting in an accurate prediction of stability performance, as derived from circuit level simulations. It can be recalled that while the CP load capacitor is a design parameter fixed in the initial design phase, the CP output impedance magnitude is strongly dependent on the CP operating frequency (F_{IN}). Therefore feedback loop stability must be evaluated over a range of R_{CP} values based on the instantaneous F_{IN} selected for a set of regulated output voltages and load currents. The reference operating point utilized for this analysis

Fig. 5.6: DC loop-gain ($A_{v_{DC_STB}}$), phase-margin (PM), unity-gain frequency (ω_u) vs. CP output impedance (R_{CP})

is maintained as the worst-case for phase-margin at mid-load conditions, as shown in Fig. 5.3.

The typical variation of stability parameters (loop-gain: ($A_{v_{DC}}$), phase-margin (PM) and unity-gain frequency (ω_u) obtained with respect to R_{CP} , is as shown in Fig. 5.6. The effect of R_{CP} on loop stability characteristics is similar to that observed for the varying load current. At low R_{CP} magnitude, the gain derived from the OTA stage is reduced, since it has minimal impact on its output impedance ($R_{OTA} \approx r_{ds_OTA}/2$), mainly determined by the output impedances of the devices in its output stage. In contrast, the gain from the pass-transistor stage is high, as it operates in deep saturation region. At high R_{CP} magnitude, the situation is reversed, with the gain boosted from the OTA stage and reduced at the pass-transistor output stage. This occurs since the OTA output impedance is now increased with the addition of R_{CP} to the output impedance offered by the NMOS device in the output stage, as shown in the small-signal model depicted in Fig. 5.2. Concurrently, the gain from the pass-transistor stage is reduced as it is driven towards the linear region with increasing R_{CP} magnitude. Therefore, the overall DC loop-gain peaks at a specific CP output impedance magnitude (R_{CP_MAX}). As the loop-gain is increased, ω_u is stretched outwards to higher frequencies, resulting in stronger influence of additional pole and zero on the feedback loop frequency response. Therefore the loop PM attain

its minimum value at an R_{CP} magnitude in the vicinity of R_{CP_MAX} .

It can be noted that the gain from the OTA stage is only dependent on the R_{CP} magnitude and is not affected by any possible headroom limitation across its supply rails. This is because, both the devices in its output stage operate in the saturation region, offering an almost constant and high output impedance for the entire R_{CP} variation. This can be verified by recording the DC loop-gain with zero CP output impedance, while maintaining CP output at no-load (V_{CP_0}) at a magnitude equal to the CP output obtained (V_{CP_MAX}) with R_{CP_MAX} , as mentioned in (5.6), (5.7).

$$\text{Existing CP Model : } V_{CP_MAX} = V_{CP_0} + I_L \cdot R_{CP_MAX} \quad (5.6)$$

$$\text{Modified CP Model : } V_{CP} = V_{CP_MAX} + I_L \cdot 0 \quad (5.7)$$

Utilizing the modified CP linear model in (5.7), the obtained DC loop-gain magnitude ($\sim 55\text{dB}$) is substantially lower than the maximum gain ($\sim 64\text{dB}$) derived at R_{CP_MAX} , as observed in Fig. 5.6. This clearly validates the reasoning provided regarding the OTA gain variation with respect to the R_{CP} magnitude.

The feedback loop frequency response also exhibits high sensitivity towards the CP load capacitor magnitude. This is evident from the change in loop PM with respect C_L magnitude, as shown in Fig. 5.7. As observed, the PM variation starts with a high magnitude corresponding to a low C_L value, and decreases rapidly with the increasing C_L values, till attaining its minimum value at a specific CP load capacitor magnitude (C_{L_MAX}), beyond which it continues to increase almost linearly with respect to C_L . The given trend for the PM can be explained using the corresponding phase-plot derived for the low, mid and high C_L values representing all three regions of PM vs C_L curves. From Fig. 5.7, it can be observed that the dominant pole location remains practically unchanged, however the relative spacing between the additional pole and zero increases with the increasing C_L magnitude. At low C_L values, the effect of additional pole and zero sets in at higher frequencies and the phase plot stabilizes due to the closer spacing between ω_{p2} and ω_{z1} . Therefore the ω_u is attained with a relatively high PM magnitude. At high C_L values, the phase decrease is initiated at lower frequencies, since ω_{p2} is shifted towards the dominant pole location. However, the PM is still maintained at high value since

Fig. 5.7: Phase-margin (PM), unity-gain frequency (ω_u) vs. CP load capacitor (C_L)

the ω_u is attained while the phase is increasing due to effect of ω_{z1} . Therefore, the PM is at its minimum at the specific C_L value (C_{L_MAX}) at which ω_u is attained while phase is also at its minimum value. It should be noted that for practical CP circuit implementation, the minimum C_L magnitude is based on the tolerance limits for the CP transient ripple at maximum load current specification, as elaborated in section 4.4.3.1. The phase-plots and the PM variation with respect to C_L magnitude can be subsequently utilized to ensure that the feedback loop retains unconditional stability at the selected C_L value. Thus the optimum value can be identified as the minimum C_L magnitude at which stability of the regulator loop can be ensured across its operating range while meeting CP voltage ripple requirements. The given design utilizes 260pF of integrated CP load capacitor to limit the CP output voltage ripple below 50mV at max supported load current of 800 μ A. Moreover, the stability of the regulator feedback loop rigorously verified with the given CP implementation, whereby the PM is maintained above 51° across its operating range.

5.3.2 Effect of External Capacitor ESR

The given design relies on the dominant pole set by off-chip capacitor to meet the stability criteria of the regulator feedback loop. Such external capacitors are typically associated with a finite equivalent series resistance (ESR), typically in the

range of $1\text{m}\Omega$ to 1Ω . The ESR magnitude (R_{ESR}) modifies the location of the dominant pole and introduces an additional zero in the loop transfer function, and can have therefore have a profound impact on the stability of the feedback loop. In fact the linear regulator utilizing external capacitor(s) to achieve dominant pole compensation, are only stabilized within a bounded range of R_{ESR} , as they rely on the ESR zero to cancel any additional pole in the transfer function. The revised open-loop transfer function and the location of the dominant pole (ω_{p1_ESR}) and the ESR zero (ω_{z2_ESR}), in presence of a finite ESR resistance (R_{ESR}) can be estimated using (5.8)-(5.10).

$$H(s)_{STB} \approx \frac{Av_{DC_STB} \cdot (1 + s/\omega_{z1}) \cdot (1 + s/\omega_{z2_ESR})}{(1 + s/\omega_{p1_ESR}) \cdot (1 + s/\omega_{p2})} \quad (5.8)$$

$$\omega_{p1_ESR} \approx \frac{1}{(C_{EXT} \cdot (R_L + R_{ESR}))} \quad (5.9)$$

$$\omega_{z2_ESR} \approx \frac{1}{C_{EXT} \cdot R_{ESR}} \quad (5.10)$$

To achieve a robust implementation, the stability of the feedback loop is analyzed in presence of a finite ESR while accounting for a sufficiently large variation in its magnitude. The modified gain-phase plot for the worst-case PM, for varying R_{ESR} magnitude is reproduced in Fig. 5.8. From Fig. 5.8 and (5.9), it can be observed that the dominant pole location remains unchanged since the load-resistance (R_L) is significantly higher than R_{ESR} magnitude, for the supported range of load currents ($I_L \leq 800\mu A$). Furthermore, for $R_{ESR} < 1\Omega$, the ESR zero (ω_{z2_ESR}) is located well-beyond the unity-gain frequency (ω_u), to have any observable impact on the feedback back loop frequency response.

The variation of PM and corresponding ω_u for R_{ESR} magnitude variation from 1Ω to 100Ω , is as shown in Fig. 5.9. If R_{ESR} magnitude in the range of 1Ω to 5Ω , ω_{z2_ESR} is shifted to lower frequencies, resulting in marginal gain in phase at the ω_u . This results in small but observable improvements in PM, as shown in Fig. 5.9. Increasing R_{ESR} beyond 5Ω , shifts ω_{z2_ESR} is to even lower frequencies, to be located in the vicinity of ω_{p2} . This is observed as distinct peaking in the gain-phase plot and results in a significant increase in the ω_u and the PM magnitude, as shown in Fig. 5.9. The PM magnitude subsequently starts receding for $R_{ESR} > 10\Omega$, due

Fig. 5.8: Gain-phase plot in presence of the external capacitor ESR resistance (R_{ESR})

Fig. 5.9: Phase-margin (PM), unity-gain frequency (ω_u) vs. ESR magnitude (R_{ESR})

to increased effect of high frequency parasitic poles at the high ω_u frequency, as observed from the Fig. 5.9. The design retains stable operation with $PM > 55^\circ$ for R_{ESR} values below 60Ω .

It can thus be concluded that the regulator feedback loop does not require a minimum R_{ESR} value to deliver stable operation and is tolerant to a wide-range

of R_{ESR} magnitude (stable for $0\Omega < R_{ESR} < 60\Omega$). This R_{ESR} range which is well beyond its typical variation range ($1m\Omega < R_{ESR} < 1\Omega$) occurring in the large external capacitor components. Moreover, the given analysis suggests that, since the dominant pole location remains practically unchanged for the given design with relatively low-load currents ($I_L \leq 800\mu A$ implying $R_L \gg R_{ESR}$), an inclusion of a low-value on-chip/off-chip inclusion ESR resistance ($R_{ESR} \sim < 5\Omega$) in series with C_{EXT} , can result in a significant improvement in the PM. This can be identified as an additional design feature and can be utilized to improve the stability of the feedback loop for the limiting cases, when the PM falls below the acceptable level.

In summary, the stability of the regulator feedback loop is affected due to the specific transfer characteristics of the fully-integrated CP. The high output impedance of the CP (R_{CP}) along with CP load capacitor (C_L) determines the location of the additional pole-zero pair formed in the loop-transfer function, and results in nominal degradation of PM at mid-load conditions when DC loop gain is maximized. The feedback loop characteristics is independent of the gate-source capacitance (C_{gs_PT}) of the pass-transistor. The design remains stable in presence of the finite R_{ESR} resistance associated with external capacitor implementations, and the stability shows slight improvements for $R_{ESR} > 1\Omega$. The stability of the regulator feedback loop for the given design is rigorously verified in presence of the frequency dependent CP output impedance and large magnitude of integrated CP load capacitor. The design remains unconditionally stable, with $PM > 51^\circ$ across its entire operating envelope.

5.4 Charge-Pump Noise Rejection

As elaborated previously, the fully-integrated CP output is characterized with high output impedance, steady-state ripple and high noise-content. The output voltage ripple occurring at CP operating frequency (F_{IN}), can be observed from its transient waveform. The frequency domain analysis of the CP output suggest that, while the noise is concentrated at the harmonics of F_{IN} ($N \cdot F_{IN}$, $N \sim 1$ to 5), a significant noise component also spreads across frequency spectrum and is manifested in the form of raised potential (V_{n_rms}) of the noise-floor. The given design utilizes

a linear regulator arrangement, powered by the CP itself, to adequately suppress its non-linearities and thus derive the clean, regulated output with required specifications. The high-gain of the regulator's negative feedback loop, along with -3dB frequency set by the external capacitor (C_{EXT}), actively filters the CP noise content, to generate a low-ripple, low-noise, negative voltage output with high regulation accuracy. In order to accurately assess the regulation efficacy of this arrangement, it is essential to quantify the effective noise-rejection offered by the given regulator topology, at DC and across frequencies of interest. This frequency domain analysis also provides a theoretical estimate for the extent to which CP transient ripple and noise can be suppressed, and can thus be used for future bench-marking of the accuracy and spectral purity of regulated output, as derived from system level transient simulations and as obtained from measurement results.

The circuit level schematic for small-signal analysis of CP noise rejection is same as that utilized for loop stability analysis, as shown in Fig. 5.1. The small-signal model used for the quantitative analysis of the CP noise rejection is as presented in Fig. 5.10. The small-signal parameters can be again referred to Table 5.1. The model essentially includes the small-signal representation of the pass-transistor and all the devices used within the OTA. The CP linear model is included, with the CP output at no-load (V_{CP_0}) interpreted as the AC input noise source (V_{IN}) in series with CP output impedance (R_{CP}). The CP load capacitor (C_L) and the pass-transistor gate capacitance (C_{gs_PT}) are not included in the small-signal model and only the large external capacitor (C_{EXT}) is included as the frequency dependent component. This relaxes the complexity involved in the s-domain analysis of the noise-transfer function and aids to provide a simplified analysis, consistent with circuit level simulations.

It can be observed that, in the small-signal model, the gate voltage of current source transistor (N3 in Fig. 5.1) is maintained at the (small-signal) CP output potential at v_0 , thus resulting in effectively zero AC current ($g_{m_N3} \cdot (v_0 - v_0)$) across its drain-source terminals. This is because, at the circuit level, the biasing potential V_{BN} constantly tracks the CP output node voltage (V_{CP}), to derive supply-independent biasing current, invariant of the CP output magnitude.

To facilitate the analysis, the number of variables are reduced by assuming

Fig. 5.10: Small-signal model for CP noise rejection analysis

common representations for devices with identical aspect ratios and bias currents. In addition, common output conductance (g_{ds_np}) is assumed for devices P2A/2B, N2A/2B, and the diode connected PMOS devices are replaced with their equivalent small-signal input impedance ($1/g_{m_P1}$). The resulting output noise transfer function (V_{OUT}/V_{IN}) obtained through nodal analysis of the given model, yields a first order functional response, as denoted by (5.11).

$$H(s)_{AC} \approx \frac{Av_{AC}}{(1 + s/\omega_{-3dB})} \quad (5.11)$$

The expressions for Av_{AC} and ω_{-3dB} mentioned above are derived through computational analysis of the nodal equations obtained from the small-signal model and then simplified based on some reasonable assumptions as mentioned in (5.12), (5.13).

$$g_m \gg g_{ds} \quad (5.12)$$

$$R_{CP} \cdot g_{ds} \ll 1 \quad (5.13)$$

Using these assumptions, the approximate expressions for low frequency AC rejection (Av_{AC}) and the corresponding -3dB cut-off frequency (ω_{-3dB}), is derived in terms of CP output impedance (R_{CP}) and other design and device parameters, as mentioned

in (5.14), (5.15).

$$Av_{DC} \approx \frac{g_{ds_np} \cdot (g_{m_PT} \cdot g_{ds_N3} + 2g_{m_PT} \cdot g_{ds_np} + 2g_{m_N2} \cdot g_{ds_PT})}{(\beta \cdot g_{m_N2} \cdot g_{m_PT} \cdot g_{m_diff}) \cdot (2 \cdot R_{CP} \cdot g_{ds_N3} + 2 \cdot R_{CP} \cdot g_{ds_np} + 1)} \quad (5.14)$$

$$\omega_{-3dB} \approx \frac{(g_{m_PT} \cdot g_{m_N2} \cdot g_{m_diff} \cdot \beta) \cdot (2R_{CP}g_{ds_N3} + 2R_{CP}g_{ds_np} + 1)}{C_L \cdot g_{ds_np} \cdot [2g_{m_N2} + R_{CP}g_{m_N2} \cdot (4g_{ds_N3} + 4g_{ds_np} + 2g_{ds_PT}) + \dots \dots + R_{CP}g_{m_PT} \cdot (g_{ds_N3} + 2g_{ds_np})]} \quad (5.15)$$

It can be observed that the simplified expressions for both Av_{AC} and ω_{-3dB} mentioned in (5.14) and (5.15), are independent of the load current ($/R_L$) magnitude. The ω_{-3dB} expression can be further simplified to show its equivalence to the approximated unity-gain frequency (ω'_u) obtained for a 2-stage configuration, as shown in (5.16).

$$\omega_{-3dB} \approx \omega'_u \approx \frac{g_{m_diff} \cdot g_{m_PT} \cdot \beta}{g_{ds_np} \cdot C_L} \quad (5.16)$$

Therefore the ω_{-3dB} value can be expected to lie in the vicinity of the actual unit-gain frequency obtained (ω_u) at a given operating point. The numerical values of Av_{AC} and ω_{-3dB} are obtained by substituting the transconductance (g_m) and output impedance (g_{ds}) of various devices, as extracted from the dc-operating point simulation. For the given design, the Av_{AC} and corresponding ω_{-3dB} magnitude are evaluated at -65.7dB at 38kHz, respectively.

The simulated CP noise rejection as obtained from the AC analysis of the regulator is as shown in Fig. 5.11. In Fig. 5.11, the gain-plots of the noise-transfer function are presented at light ($50\mu A$) and maximum load conditions ($550\mu A$), at a regulated output voltage at -1.5V. The corresponding values for Av_{AC} and ω_{-3dB} are also depicted alongside in the Fig. 5.11. The circuit level simulation results thus verify the first-order frequency response (for $\omega \geq \omega_{-3dB}$) and indicate the CP noise rejection magnitude at low-frequencies ($\omega < \omega_{-3dB}$) decreases with the increasing load current magnitude. Moreover, the numerically evaluated values for both Av_{AC} and ω_{-3dB} are in the middle of the values of obtained for their simulation counterparts, across the supported load current range. The agreement between the analytical and circuit simulation results validates the representative small-signal

Fig. 5.11: AC simulation of CP noise rejection provided by the negative voltage regulator

model and the CP noise rejection function derived on its basis.

From Fig. 5.11, it can also be observed that the regulator employed in this design provides over 100dB of rejection at typical frequencies employed for fully-integrated CPs (10MHz - 100MHz), such as the one used in the given design. Moreover this rejection magnitude is 20dB-80dB higher than that obtained at low-frequencies (100kHz - 900kHz) employed by CPs employing large off-chip charge-pumping capacitors. This clearly justifies the application of fully-integrated CPs along with a linear regulator arrangements, as was proposed and explored in the design of given negative voltage generator system. At the system level, since the CP noise is mostly concentrated at the harmonics of its operating frequency, the high-rejection magnitude facilitates effective noise/ripple suppression by the linear regulator topology. The regulator is thus able to provide low transient ripple negative voltage output, with high-degree of spectral purity along-with high regulation accuracy and reduced output impedance.

5.5 Settling Time Analysis

The total settling time (t_{TOT}) can be defined as the time required for the regulated output voltage, at a given initial potential ($V_{REG}(0)$), to reach within a certain per-

centage (1%-5%) of its desired steady-state voltage magnitude. This time duration can be regarded as important performance parameter as it represents the system-level response/wake-up time to supply regulated output after the initial power-up. With regards to regulated switched-capacitor based voltage converters, the overall settling behaviour and total settling duration depends on a number of factors including the CP transfer characteristics, regulator's feedback loop frequency response and the given operating point defined in terms required regulated output voltage (V_{REG}) and load current (I_L) setting. This section provides an in-depth examination of the complete settling characteristics obtained from the given combination of the fully-integrated CP and linear-regulator, as explored in the given NVG system implementation. The detailed quantitative analysis presented alongside, accurately predicts the complete settling profile and provides as piece wise derivation of total settling time in terms of the required design (C_{EXT} , $V_{CP,0}$, R_{CP} , C_L) and operating variables ($V_{REG}(0)$, V_{REG} , I_L). The results obtained from this analysis are in close agreement with the corresponding simulation results and are further verified through measurement data.

The small-signal analysis regarding the stability of the feedback loop was presented in section 5.1. Although the regulator loop was verified to maintain unconditional stability across its operating range, for certain regulated output voltage the phase-margin was observed to drop below 55° , at mid-load conditions. Therefore, to ensure a robust implementation, the system level stability and functionality must also be verified from a large signal prospective, involving circuit level performance evaluation in the time domain. However, the combined transient simulation of CP and regulator modules is highly time and (simulation) resource intensive, and therefore cannot be utilized for broad functional verification across multiple operating conditions. A simpler yet highly effective alternative is to perform transient simulation with stand-alone regulator module while including the CP linear model, as shown in Fig. 4.20, and as utilized for loop-stability and CP noise rejection related small-signal analysis. The resulting settling profile and settling time duration can be very closely matched to its counterpart obtained from system-level transient simulations, with the accuracy mainly limited by the accuracy of CP linear model. Moreover, this first level large signal verification can also detect potential instances

Fig. 5.12: Typical settling characteristics as derived from transient simulation of regulator, including the CP linear model

of instability which may occur despite rigorous small-signal verification, and is therefore highly useful for early fault detection and performing full system verification in the initial design phase. Due to the relevance and efficacy of the given technique, the regulator schematic in Fig. 4.20 is also used as reference for the quantitative analysis of settling characteristics, by replacing the error-amplifier (OTA) with an ideal gain block. The analytical results are therefore compared against the circuit simulation results obtained for the regulator circuit incorporating the CP linear model.

The typical settling profile, as obtained from circuit-level simulation for the regulator schematic depicted in Fig. 4.20, is as shown in Fig. 5.12. The corresponding transient waveforms for the drain-source (V_{DS}) and overdrive potential (V_{OV} : $V_{GS} - V_T$) for the pass-transistor are also depicted alongside in Fig. 5.12. As indicated from the relative potential of V_{DS} and V_{OV} waveforms, the settling characteristics can be sub-divided into parts, based on the region of operation for the pass-device and can be qualitatively explained as follows. For the first t_1 seconds, while $V_{DS} > V_{OV}$, the pass-transistor operates in saturation region and therefore the external capacitor (C_{EXT}) is discharged with the (approx.) constant saturation mode current (I_{PT_SAT}). The resulting CP output (V_{CP_SAT}) acquires a constant

potential based on the I_{PT_SAT} magnitude. In the next t_2 seconds, pass-transistor operates in linear region, as V_{DS} is maintained lower than V_{OV} potential. In this region, the CP output voltage is gradually pulled down as the corresponding discharging current magnitude is reduced with time. Finally, as the feedback voltage (V_{FB}) the external reference potential (V_{REF}), the gain of the feedback loop is boosted and system rapidly acquires steady-state in the following t_3 seconds. In this fast transition region, the V_{DS} and V_{OV} potential again change sides with system reverting to $V_{DS} > V_{OV}$ configuration, thus ensuring saturation mode operation for pass-transistor at the final steady-state. In contrast to the phased transition of the CP output voltage, the regulated output follows a clean first order settling curve, as expected out of a single dominant pole system.

In the following two sub-sections, set of time-domain differential equations are formulated specific the region of operation of the pass-transistor. The solution of the given design equations are used for the evaluation of the piece wise settling time duration and thus obtain the numerical solution of the complete settling transients.

5.5.1 Pass-Transistor in Saturation Region

At time $t = 0$, when the system is powered up, the feedback voltage (V_{FB}) at the non-inverting terminal of the OTA, is typically much higher than the external reference (V_{REF}) input. Therefore the gate voltage (V_{G_PT}) of the pass-transistor at the OTA output, initially acquires a potential equal to the positive rail (V_{POS}) of the regulator. Assuming that the regulated output is also initially pulled to the V_{POS} potential, the system acquires an initial steady-state for the first t_1 seconds, based on the saturation region operation of the pass-transistor. In this initial settling phase, external capacitor (C_{EXT}) is discharged with the (approx.) constant saturation mode current (I_{PT_SAT}), while the corresponding CP output (V_{CP_SAT}) is held to a constant output potential based on the I_{PT_SAT} magnitude, as observed from Fig. 5.12. The steady-state, depicting the node voltage variables (V_{G_PT} , $V_{D_PT}(t)$, V_{S_PT}), is as shown in Fig. 5.13. It can be observed that in the given state, both the gate ($V_{G_PT} = V_{POS}$) and source potential ($V_{S_PT} = V_{CP_SAT}$) of the pass-transistor are held constant, while the regulated output ($V_{REG}(t)$) at its drain terminal is decreasing through the constant current (I_{PT_SAT}) flowing through the

Fig. 5.13: Initial settling response: Pass-transistor in saturation region

pass-transistor and eventually sinking into the CP along with the current from the regulator (I_{REG}). Using the CP linear model and the standard constant current approximation for the saturation region, the constant parameters (V_{GS_PT} , I_{PT_SAT} , V_{CP_SAT}) can be related to each other through (5.17) - (5.19).

$$V_{GS_PT} = V_{POS} - V_{CP_SAT} \quad (5.17)$$

$$V_{CP_SAT} = V_{CP_0} + (I_{PT_SAT} + I_{REG}) \cdot R_{CP} \quad (5.18)$$

$$I_{PT_SAT} = 0.5 \cdot k'_n \cdot (W/L) \cdot (V_{GS_PT} - V_T)^2 \quad (5.19)$$

The initial inrush current (I_{PT_SAT}) magnitude and the corresponding CP output voltage (V_{CP_SAT}) can thus be derived in terms of CP design ((W/L)) and process (k'_n , V_T) parameters, by simultaneously solving the equations in (5.17)-(5.19). The resulting quadratic expression for I_{PT_SAT} has two real solutions, out of which only one is consistent with circuit simulations. The I_{PT_SAT} corresponding to the valid solution, is as derived in (5.20) - (5.22).

$$I_{PT_SAT} = \frac{R_{CP} \cdot (W/L) \cdot k'_n \cdot [A] + 1 - [B]}{R_{CP}^2 \cdot (W/L) \cdot k'_n} \quad (5.20)$$

$$\text{where, } A = V_{POS} - V_T - V_{CP_0} - I_{REG} \cdot R_{CP} \quad (5.21)$$

$$\text{and } B = \sqrt{2 \cdot R_{CP} \cdot (W/L) \cdot k'_n \cdot [A] + 1} \quad (5.22)$$

In addition, the constant current discharge of the regulated output voltage ($V_{REG}(t)$), can be captured through the nodal analysis at the pass-transistor drain terminal, as described through the first-order differential equation mentioned in (5.23).

$$-I_{PT_SAT} = V_{REG}(t)(1/R_L) + (\frac{dV_{REG}(t)}{dt})C_{EXT} \quad (5.23)$$

Apart from the steady-state and differential equation, the system-state is defined the inclusion of boundary conditions on the regulated output voltage, as given by (5.24)-(5.25).

$$V_{REG}(0) = V_{POS} \quad (5.24)$$

$$V_{REG}(t_1) = V_{POS} - V_T \quad (5.25)$$

The first boundary condition in (5.24) is based on the initial regulated output potential ($V_{REG}(0)$) at the beginning of this settling phase. The second condition in (5.25) is obtained by equating the pass-transistor's drain-source voltage ($V_{DS_PT}=V_{REG}(t_1) - V_{CP_SAT}$) to its overdrive potential ($V_{OV_PT}=V_{POS} - V_{CP_SAT}$) at time t_1 , thus implying the pass-transistor transition from saturation to linear region at this instant.

The solution of differential equation in (5.23), in conjunction with the boundary conditions in (5.24)-(5.25), yields the expression for regulated output voltage as a function of time ($V_{REG}(t)$), as derived in (5.26).

$$V_{REG}(t) = \exp\left(\frac{-t}{R_L \cdot C_{EXT}}\right) \cdot (V_{POS} + I_{PT_SAT} \cdot R_L) - I_{PT_SAT} \cdot R_L \quad (5.26)$$

In addition time instant t_1 , denoting the duration of initial settling phase, can also be derived in terms of I_{PT_SAT} , as mentioned in (5.27).

$$t_1 = -C_{EXT}R_L \cdot \log\left(\frac{V_{POS} - V_T + I_{PT_SAT} \cdot R_L}{V_{POS} + I_{PT_SAT} \cdot R_L}\right) \quad (5.27)$$

The numerical value of t_1 can thus be readily evaluated by utilizing the I_{PT_SAT} magnitude derived in (5.20), and using the actual values for other design (C_{EXT} , V_{POS}), operating (R_L) and process (V_T) parameters.

5.5.2 Pass-Transistor in Post-Saturation Region

The post-saturation region operation of the pass-transistor begins at time instant t_1 , when its overdrive potential (V_{OV_PT}) crosses over the drain-source potential (V_{DS_PT}), as shown in Fig. 5.12. In this settling phase, pass-transistor operates in the linear region for the first t_3 seconds, followed by a rapid transition region for the next t_3 seconds, in which feedback loop is activated and final steady-state output voltages are attained. In the linear region, the pass-transistor is modelled as a resistor with the on-resistance ($R_{ON_PT}(t)$) magnitude dependent on the instantaneous gate-source potential ($V_{GS_PT}(t)$), as approximated in (5.28).

$$R_{ON_PT}(t) = \frac{1}{k'_n \cdot (W/L) \cdot (V_{GS_PT}(t) - V_T)} \quad (5.28)$$

The representative regulator schematic showing the transient circuit state attained in this region, is as shown in Fig. 5.14. It can be observed that, unlike the previous saturation region operation, in this settling phase the gate ($V_{G_PT}(t)$) and the CP output voltage ($V_{CP}(t)$) along with the discharging current and the regulator current ($I_{REG_Lin}(t)$) are all dynamically varying with time, along with the decreasing regulated output ($V_{REG}(t)$).

The instantaneous gate voltage derived as the output of the OTA, is obtained by modelling the OTA using the standard-logistic function, as mentioned in (5.29).

$$V_{G_PT}(t) = \frac{V_{CP}(t)}{1 + e^{k \cdot x}} + \frac{V_{POS}}{1 + e^{-k \cdot x}} \quad (5.29)$$

where the term x represents the differential input to the OTA and the factor k models the slope of the transition region. The supply potential (V_{POS}) and the instantaneous CP output voltage ($V_{CP}(t)$) represents the supply rails across the OTA. The resulting functional response can be visualized at varying OTA gain configurations, as shown in Fig. 5.15. The differential input x can be further resolved in terms of the instantaneous regulated output ($V_{REG}(t)$), reference input (V_{REF}), and the feedback factor (β), as mentioned in (5.30).

$$x = V_P - V_N = (V_{REG}(t)) \cdot \beta - V_{REF} \quad (5.30)$$

in magnitude with the increasing CP output voltage magnitude. To capture this effect in the analysis, $I_{REG_Lin}(t)$ is linearly interpolated as a function of $V_{CP}(t)$, based on the representative values extracted from the DC operating point simulation. The resulting $I_{REG_Lin}(t)$ expression is as derived in (5.32).

$$I_{REG_Lin}(t) = (-16.97\mu A/V) \cdot V_{CP}(t) - (13.34\mu A) \quad (5.32)$$

The dynamic state of the system is described through the system of equations obtained from the nodal analysis at the drain and source terminal of the pass-transistor, using the equivalent schematic shown in Fig. 5.14. The resulting equations are as derived in (5.33) and (5.34).

$$\frac{V_{REG}(t)}{R_L} + \left(\frac{dV_{REG}(t)}{dt}\right) \cdot C_{EXT} + \frac{V_{REG}(t) - V_{CP}(t)}{R_{ON_PT}(t)} = 0 \quad (5.33)$$

$$I_{REG_Lin}(t) = \frac{V_{CP}(t) - V_{REG}(t)}{R_{ON_PT}(t)} + \frac{V_{CP}(t) - V_{CP,0}}{R_{CP}} \quad (5.34)$$

Lastly, the boundary condition relating to continuity of regulated output voltage at time instant t_1 , is as mentioned in (5.35).

$$V_{REG}(t_1^+) = V_{POS} - V_T \quad (5.35)$$

The given system of differential-algebraic equations (DAE) presented in (5.28)-(5.35), although complete, does not yield a closed-form solution for solution for node voltage variables ($V_{CP}(t)$, $V_{G_PT}(t)$, $V_{REG}(t)$). This implies that even though a unique solution exists, it is not possible to derive an isolated expression for each node voltage as a function of time. Therefore, for the post-saturation region, the given set of DAE equations is computationally analyzed to obtain a numerical solution of each node-voltage variable, at different time instants. The details related to computational analysis along with associated MATLAB code is provided in Appendix II, included at the end of this thesis.

Fig. 5.16: Comparison of settling response: Simulation versus Numerical solution

5.5.3 Verification of Settling Characteristics

The numerical solution derived for the CP ($V_{CP}(t)$) and regulated output voltage ($V_{REG}(t)$), for the complete settling transients is as shown in Fig. 5.16. The corresponding transient simulation obtained from the regulator schematic in Fig. 4.20, is also presented alongside for a direct comparison. These representative results are derived for a required regulated output at $-2.8V$ at $200\mu A$ load current. As observed from Fig. 5.16, the proposed analysis results in a highly accurate prediction of the complete settling profile, including the final transition region in which the final steady-state potentials are acquired. In addition, the predicted settling transients are very closely matched to circuit level transient simulation for the regulator, incorporating the CP linear model.

The only apparent non-conformity between the analysis and simulation results occurs for the CP output at time instant t_1 , corresponding to the onset of linear region operation for the pass-transistor. This mismatch occurs because the quantitative analysis utilizes different models and design equations for the different operating regions of the pass-device. As a result, mathematically it is not possible to simultaneously enforce continuity for both the CP output and regulated output voltage at the crossover point of different operating regimes. However, in spite of this minor discontinuity, the CP output successfully retraces the waveform for its simulation counterpart after a short time lapse from t_1 .

The total settling time (t_{Tot}) obtained for simulation results is defined as sum of settling times corresponding to the pass-transistor operation in saturation region (t_1) and linear region (t_2), and final transition region (t_3), as depicted in Fig. 5.12. In contrast, the total settling time for the the analytically derived settling transients, is interpreted as the sum of settling times for the the saturation (t_{sat}) and post-saturation region (t_{psat}), as shown in Fig. 5.16, thereby implying that the transition region time t_3 is included within t_{psat} . The region-wise settling times obtained from the numerical solution is very closely matched to its simulation counterparts (t_{sat} compared to t_1 and t_{psat} compared with $(t_2 + t_3)$), which translates into close agreement in the total settling time duration, across analysis and simulation results. In-fact, the mismatch in the total settling time duration, between numerical derived and simulated values, is verified to be under 1%, across various operating conditions.

The proposed quantitative analysis is therefore shown to accurately predict the complete settling characteristics, including the initial inrush current magnitude (I_{PT_SAT}) and the final transition region (t_3). In addition, the close co-relation between analysis and simulation results, including a precise estimation settling time duration, firmly validates its findings and highlights its relevance in accurately predicting the settling behaviour across a varying set of design and operating parameters. In the following sections, the predicted settling profile is also shown to be consistent with system level transient simulations and measurement results. In such cases, the accuracy in estimation of settling time is mainly limited by the accuracy of CP linear model.

5.6 System Level Verification

The functionality and performance of the proposed negative voltage generator system is fully established through rigorous transient co-simulation of charge-pump and regulator modules. This is essentially required since the system does not implement a dedicated start-up sequence, from the instant of power-up, till the time regulated output voltage is ready. After the system is powered up, the CP output begins to ramp down in presence of the strong-inrush current from the discharging external capacitor. The details relating to the inrush current magnitude (I_{PT_SAT}) and

the corresponding CP output (V_{CP_SAT}) are elaborated and derived in the previous section. The regulator circuit, powered through the CP output, is activated when $V_{CP}(t)$ falls below a certain min. threshold, as required by the bias-gen and OTA modules to operate. Therefore, it is essential to ensure that the circuit does not enter any unstable states at any point of its initial settling transients, and can be verified to remain stable, after the steady-state has been attained.

The major challenge associate with such an extend final verification is that it encounters very long simulation times (24 to 72hrs.), despite being highly (simulation) resource intensive. This occurs in the transient simulation environment, since the time-period of the input periodic signal ($T_{PRD} \sim 10\text{ns}-100\text{ns}$) is 5 to 6 orders of magnitude lower than the typical settling time ($T_{TOT} \sim 1\text{ms}-2\text{ms}$). In order to expedite the simulation process, values for the CP output ($V_{CP}(t)$) and corresponding regulated output ($V_{REG}(t)$), at specific time-instants, can be recorded from settling characteristic obtained through the transient simulation of the regulator circuit including the CP linear model, as described in the previous section. These values for $V_{CP}(t)$ and $V_{REG}(t)$ are then used as valid initial conditions for the CP load capacitor and external capacitor respectively, in the transient co-simulation setup. This vastly reduces the effective simulation time required to achieve steady-state, and thus facilitate a full system-level performance verification across higher number of operating conditions.

The complete settling characteristic for -2.8V regulated output at 200uA load current, as obtained from system level transient co-simulation, is as shown in Fig. 5.17. The settling profile can be closely co-related with the large signal verification using regulator circuit and is therefore also consistent with results obtained from the associated analysis. The steady state ripple magnitude for the charge-pump and the regulated output voltage are 10mV and 261nV, respectively, as highlighted in Fig. 5.17. This suggests the given negative voltage regulator practically provides over 90dB rejection implementation for the CP noise and transient ripple at its operating frequency. Moreover the ultra-low steady-state ripple amplitude for the regulated output validate the superior low-noise performance of the design and indicate that for practical implementation purposes, the noise and ripple performance of the V_{REG} will only be limited by accuracy of reference input.

Fig. 5.17: System level verification through transient co-simulation of CP and regulator (V_{REG} : -3.0V, I_L : 200 μ A, C_{EXT} : 220nF)

5.7 Chapter Summary

This chapter presented a detailed review of the multi-dimensional analysis and verification of the proposed NVG system. The functionality and performance of the overall system was verified using both small and large-signal analytical techniques, including verification of loop-stability, AC analysis of regulator frequency response and large-signal, time-domain verification of initial settling transients.

In this regards, firstly, the small-signal stability of the regulator's feedback loop was verified, while capturing the effect of CP output response on the feedback loop-transfer function. The derived functional response was validated with gain-phase plots obtained from the corresponding circuit level simulations. The regulator feedback loop was verified to retain unconditional stability, with a worst-case PM of 51° and the design was also verified to remain stable for any practically occurring

magnitude of external capacitor's ESR resistance.

Secondly, frequency domain analysis of the CP noise transfer function was presented to quantify the noise-rejection provided by the given regulator topology. The predicted frequency response was co-related with corresponding AC simulation of the regulator. The AC rejection by the regulator, at typical operating frequencies employed by fully-integrated CP ($F_{IN} > 10\text{MHz}$) was observed to be $>100\text{dB}$, thus justifying their application in the given design.

Thirdly, the system was verified from a large-signal prospective through the analysis and simulation of the initial settling response, obtained for the given combination of CP and regulator modules. The proposed quantitative analysis is used to derive numerical solution of the complete settling transients and the predicted transient waveforms for CP and regulated output voltages are very closely matched to their simulation counterpart. This close agreement between the simulated and analytical results translated into a precise estimation of total settling time duration.

Lastly, the complete system functionality and performance is verified through the transient co-simulation of CP and regulator modules. The resulting settling profile is consistent with that derived from the above mentioned large-signal verification and the associated settling response analysis. In addition, the ultra low steady-state ripple magnitude for the regulated output verify the high-rejection magnitude provided by the regulator and the superior low-noise performance of the design.

Chapter 6

Experimental Verification of Proposed Negative Voltage Generator System

6.1 Introduction

This chapter presents a detailed review of the experimental verification of the proposed NVG system. The prototype chip for the given design is fabricated in GlobalFoundries CMOS 180nm BCDlite process, while the measurement is carried out on a PCB test fixture, which is instrumental in deriving the optimum low-noise performance from the design. The overall system level performance is verified using both transient and frequency domain analysis, whereby the former includes the tests for CP performance characterization, settling-time analysis and steady-state ripple measurement while the latter includes noise spectrum analysis of CP and regulated output voltages. Finally, the design is also verified with a state-of-the-art GaN-HEMT based RF power-amplifier, to further highlight its superior low-noise performance and indicate its implementation potential for precision voltage biasing and noise sensitive applications.

In this chapter, firstly the measurement test setup and the default test bench used for the performance verification, are introduced. In addition, details related to the design and relevance of a PCB testing platform, instrumental in extracting the peak performance from the design, is provided. In the following sections, the

measurement results for the stand-alone CP module is presented. The CP performance is characterized across load current and operating frequency and the resulting CP transfer response is analysed by comparing it with the corresponding simulation results and other fully-integrated CP implementations. At the system level, the measurement results for initial settling transients for the CP and regulated output waveform are presented. The resulting settling profile and the settling times are compared with the counterparts derived from simulation and quantitative analysis. Following this, the low-noise performance of the design is rigorously verified through transient steady-state ripple measurement and spectral analysis of output waveforms. Finally, the details related to the application verification with GaN-HEMT based RF PA are shared.

6.2 Measurement Setup

The proposed Negative Voltage Generator (NVG) system is implemented in Global Foundries CMOS 180nm BCDlite process. The given design utilizes thick gate-oxide, 6-terminal (deep-n-well) NMOS and 5-terminal (isolated n-well) PMOS devices, for the implementation of CP and negative voltage regulator modules. These devices allowing a locally connected source-body terminal, prevent the threshold voltage (V_T) modulation due to body-effect and are therefore ideally suited for operating with negative voltage. In addition, the thick gate-oxide variant, offered in this technology, provides high V_{DS} , V_{GS} and p-n junction breakdown limits, which helps to contain the steady-state stress on the devices within safe bounds and thus ensures a robust system level implementation, while operating under the large headroom generated across the positive and negative voltage rails. The chip micrograph of the fabricated prototype, marking the multi-phase clock generator, CP and regulator modules, is as presented in Fig. 6.1. The silicon implementation includes 290pF total integrated (MIM) capacitance and occupies a total area of $0.55mm^2$, including pads.

The design is validated using the PCB test fixture shown in Fig. 6.2. The small PCB has dimensions of 53.3mmx52.1mm, and is manufactured using the low-cost 2-layer configuration on a FR-4 substrate. The prototype chip is wire-

Fig. 6.1: Chip micrograph of the prototype fabricated in GlobalFoundries CMOS 180nm BCDlite process

Fig. 6.2: PCB test fixture with die wire-bonding

bonded to the PCB surface in a one-to-one configuration, as shown in Fig. 6.2. The simple and cost-effective PCB test setup is essential in terms of deriving the peak performance for the given design as it facilitates the placement of external capacitor (C_{EXT}), in close proximity to the regulated output pin, as shown in Fig. 6.2. This is crucial in minimizing the transient steady-state ripple and in achieving the peak noise performance, as observed from the spectral analysis of the regulated output voltage (V_{REG}). To further enhance the noise performance, critical nets, such as oscillator input and regulated output, are routed only on the top layer and surrounded by shielding vias to reduce the effect of EM coupling from nearby nets. In addition, grounding noise is reduced by placing multiple stitching vias (tied to GND) all across the PCB surface, which tightly couples the grounds on the top and

Fig. 6.3: Test-Bench used for experimental verification

bottom layer, and thus reduce the effective ground resistance.

The default test-bench used for the performance verification of the given NVG system, is shown in Fig. 6.3. The required regulated output is set by tuning the feedback resistor divider, while the corresponding load is set through one of the three load resistors included on the PCB. The supply and load current are measured simultaneously using digital multimeters, while the frequency of periodic input signal is varied externally from function generator (KeySight E33600A), based on the requirements of given testing condition. The time-domain measurements employ the KeySight 4034A digital-storage oscilloscope (DSO), while the spectral analysis of output(s) is obtained using Rhode&Schwarz FSUP Signal Analyzer.

6.3 Charge-Pump Performance Characterization

The complete system level verification is preceded with a detailed characterization of the fully-integrated, negative voltage CP used in the given design. The CP performance is evaluated in terms its output voltage (V_{CP}) and power-efficiency (η_{Eff}), as derived across the supported range of load currents (I_L) and CP operating frequencies (F_{IN}). The measured CP output voltage magnitude with respect to load current, at varying frequencies, is as presented in Fig. 6.4. The resulting CP transfer characteristics can be verified to be highly linear with respect to I_L , with only trace of non-linear response becoming apparent as load current approaches its maximum supported magnitude (I_{L_MAX} : $800\mu A$). The measured CP response thus provides the final confirmation for the derived CP linear model ($V_{CP} = V_{CP,0} + I_L \cdot R_{CP}$),

Fig. 6.4: Measured CP output vs. load current at varying operating frequencies

Fig. 6.5: CP performance characterization using linear interpolation

and its subsequent utilization throughout the course of the design and verification of the given NVG system.

The equivalent CP linear model can be extracted from the measured characterization curves, using two distinct approaches. The simplest alternative is to read the CP output at no-load ($V_{CP,0}$) directly from the measurement data and evaluate CP output impedance (R_{CP}) using any two widely-space points from the linear region of

Fig. 6.6: Comparison of CP transfer characteristics between simulation and measurement

the curve. A more involved approach is to employ linear interpolation on the measured data, as indicated in Fig. 6.4. In this technique, V_{CP_0} is obtained directly, while R_{CP} is derived as the the average slope of the resulting linearly interpolated function. It is to be noted that the extracted CP linear model can vary substantially, based on the placement of linearly interpolated response, as depicted in Fig. 6.5. For the given CP design, the equivalent linear model at varying CP F_{IN} , is as mentioned in Fig. 6.4, alongside the transfer curves. The given linear model(s) are derived using linear interpolation methodology, while ensuring maximum coverage of data-points by the approximated linear function.

The measured CP characterization data is also compared with its counterpart derived through post-layout simulations, at 50MHz F_{IN} , as shown in Fig. 6.6. In addition the comparison of the measured and simulated CP linear models ($V_{CP_0} + I_L \cdot R_{CP}$) at different F_{IN} , is compared in Table 6.1. From Table 6.1, it can be observed that while the V_{CP_0} magnitude is closely matched with the simulated value, with under 5% variation. In contrast, the measured R_{CP} is 400Ω to 1kΩ higher than its simulation counterpart, thus suggesting a 10% to 15% variation in its magnitude. To ensure an accurate comparison between the simulation and measurement data, the simulated transfer characteristics was derived using detailed top-level post-

Table 6.1: Comparison of CP linear model between Measurement and Simulation, at different operating frequencies

F_{IN}	Post-Layout	Measurement
30MHz	$-5.42 + 4.31\text{k}\Omega \cdot I_L$	$-5.12 + 5.38\text{k}\Omega \cdot I_L$
50MHz	$-5.12 + 3.54\text{k}\Omega \cdot I_L$	$-4.88 + 3.90\text{k}\Omega \cdot I_L$

layout simulations, including PADS. In addition, the measured CP characterization curves were further verified across multiple samples, which resulted in consistent CP transfer characteristics, as derived through measurement. Thus, the given nominal mismatch between simulation and measurement can be attributed to the fact that the post-layout simulations consistently under-estimate the parasitic contribution for the switched-capacitor CP operation. It can also be recalled that parasitic effect can be significantly stronger for the CP operation under fast-switching-condition (FSC) regime, as employed for the given CP implementation.

Based on the CP measurement and comparison with simulations, it can be suggested that, for switched-capacitor based regulated voltage converters, at least 10% design-margin must be reserved for PVT variation in CP linear model parameters($V_{CP,0}$, R_{CP}). To recall, the same was ensured in this design, as for the given initial specifications (V_{REG} : -3.0V, I_L : 200 μ A), and selected dropout voltage (V_{DO} : -0.6V) of pass-transistor, the required CP output voltage was set -4.0V. From Fig. 6.4, it can be observed that the measured CP magnitude at 200uA is -4.1V, and it is thus able to meet the dropout condition of pass-transistor with confidence. In general, since the regulator operation is dependent on a minimum CP output magnitude, the 10% design-margin for CP parameters is essential to ensure a robust system level implementation.

The CP power-efficiency (η_{Eff}) versus load current is recorded concurrently along with the characterization data for its output voltage. The measured peak CP η_{Eff} values are 12.13% at 350 μ A and 12.48% at 450 μ A, for 30MHz and 50MHz periodic inputs, respectively. The corresponding peak η_{Eff} number derived from the corresponding post-layout simulations are 20.21% (at 500 μ A) for 30MHz and 16.39% (at 700 μ A) for 50MHz inputs, thus indicating a 4% to 8% drop in peak efficiency for the CP measurement as compared to its simulated counterpart. To aid with the given CP η_{Eff} analysis, the η_{Eff} expression in terms of the CP output impedance

(R_{CP}) , is reproduced in (6.1).

$$\eta_{Eff} = \frac{(N \cdot |V_{DD}| \cdot \gamma - I_L R_{CP}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{PAR})} \quad (6.1)$$

From the numerator of (6.1), it can be noted that the observed reduction in the measured CP efficiency arises primarily due to the higher R_{CP} exhibited in its actual silicon implementation. However, from the analysis of both measurement and simulation data, it is revealed that η_{Eff} degradation is also contributed in part due to the higher magnitude of digital power consumption ($I_{PAR} \cdot V_{DD}$), as recorded during measurement. Since the I_{PAR} magnitude is directly proportional to the total parasitics capacitance, the given measurements also confirms the more pronounced parasitic effect for the fabricated version.

The stand-alone performance of the given negative voltage CP is contrasted with other fully-integrated SC-CP implementations with comparable power output ($\sim 0.5\text{--}5\text{mW}$) in Table 6.2. Since the CPs utilize various integrated capacitor technologies (MIM, MOM, MOS, DeepTrench etc.) with varying capacitance densities, the CP power density (at peak efficiency) is also recorded in terms of the total pump capacitance (P_{D-2} in $[mW/pF]$) in addition to its traditional interpretation in terms of the area (P_{D-1} in $[mW/mm^2]$). It can be noted that the given CP utilizes significantly lesser total pump capacitance (C_{P_TOT} : 30pF) and thus achieves one of the highest magnitude of P_{D-2} (only behind [16] with C_{P_TOT} : 15pF) and a relatively high magnitude of P_{D-1} . As compared to [16], the given CP provides a significantly more linear response (wrt. load current) with a 17% lower CP output impedance (R_{CP}) and also a lower magnitude of normalized output impedance ($R_{CP}/(C_P \cdot F_{IN})$). The R_{CP} values for other works is not mentioned since the CP output is either fixed, or it is directly regulated by operating the CP within a closed loop.

Despite the relatively high power density and linear response, the peak CP efficiency (η_{MAX}) is only limited to 12.4%. This low η_{MAX} magnitude is contributed by a number of factors including optimization preferences, CP topology and design issues. Firstly, the design opts for an area optimized approach over power efficiency maximization, as evident from the for the selection of C_P , R_{SW} pair, in the CP optimization phase. As observed from Table 6.2, the design utilizes a fraction of total

Table 6.2: Performance Comparison of stand-alone CP with other SC-CP based voltage multipliers

Param.	[2003] [JSSC] [16]	[2009] [VLSI Symp.] [49]	[2012] [BioCAS] [18]	[2016] [JSSC] [53]	[2016] [TCAS-I] [54]	[2019] [JSSC] [55]	[2019] [TCAS-I] [40] This Work
Type	Boost	Boost	Boost	Buck	Buck	Buck	Boost
Topology	Latched 1/4	Latched 1/2	Bootstrap 1/6	Div. 2/1	Div. 4/3, 3/2	Div. Contin- uous	Bootstrap 1/2
F_{IN} [MHz]	50–100	20	33.25	50	2–30	20	30–70
#Stg.	3-stg.	1-stg.	6-stg.	3-stg	1-stg.	1-stg.	1-stg.
V_{IN} [V]	1.8V	1V– 1.2V	1.8V	1.85V– 2.07V	0.6V– 1.2V	2V	3.3V
V_{OUT} [V]	6.6V– 4.9V	1.8V– 2.1V	-8.04V	0.9V	0.6V, 0.8V, 1V	0.2V– 2.22V	-4.98V – -1.73V
$I_{L,MAX}$ [mA]	0.4	1.0	0.32	4.25	0.8	2.93	0.8
Total C_P [pF]	15	400	150	10000	675	9500	30
Cap. Type	MIM	MIM		MOM	MIM+ MOS	MOM+ MOS	MIM
Active Area [mm^2]	-	2.25	1.27	2.20	0.49	1.05	0.55
R_{CP}	4.7k Ω @ 100MHz	-	-	-	-	-	3.9k Ω @ 50MHz
η_{MAX} [%]	54.0	82.0	42.3	94.6	80.0	93.0	12.4
P_{OUT} @ η_{MAX} [mW]	1.74	1.50	3.80	3.15	0.80	4.84	1.58
P_{D-1} @ η_{MAX} [mW/ mm^2]	-	0.667	2.992	1.432	1.623	4.604	2.871
P_{D-2} @ η_{MAX} [mW/pF]	0.116	0.0038	0.025	0.0003	0.0012	0.0005	0.0526
Tech.	180nm	130nm	180nm	40nm	65nm	28nm	180nm

pump capacitance ($C_{P,TOT}$), as compared to some of more recent works reporting high peak efficiency values. Since the CP conduction loss is inversely proportional to $C_{P,TOT}$, power efficiency is directly enhanced by increasing $C_{P,TOT}$ magnitude

and by ensuring that CP is operated under slow-switching limit (SSL), or within the transition region between SSL and fast-switching limit (FSL), such that the conduction loss is the major loss component.

Secondly, the η_{MAX} magnitude is reduced due to the power hungry 4-phase non-overlapping switching input required for the Bootstrap topology utilized for the given CP. In contrast, the simpler 2-phase switching input needed for Latched CPs and other CP implementations, results in significantly lower power consumption in the clock generator and drivers, thus facilitating higher η_{Eff} for the CP.

Thirdly, the low η_{MAX} magnitude is also contributed due to the sub-optimal sizing of clock drivers buffer stages driving the CP. In this regard, excessive power is dissipated in gate drivers without leading to a proportionate decrease in the CP R_{CP} . In addition, the control circuit, including multi-phase clock generator is implemented entirely using thick-oxide devices, which leads to larger device aspect ratios and thus higher parasitic power losses ($\propto C_{PAR} \cdot V_{DD}^2 \cdot F_{IN}$). Moreover, the multi-phase clock generator utilize a higher than required number of delay cells to maintain the non-overlapping switching edges. This leads to additional power losses and leading to reduction in the switch-on time (T_{ON}) while only yielding minimal advantage in terms of reducing the shoot-through currents occurring at the switching transitions.

6.4 Settling Time

The measured settling response for the CP and regulated output voltages, at different operating conditions, is as shown in Fig. 6.7. From the Fig. 6.7, the complete three phase settling transient, consistent with the corresponding simulation and analysis results, can be observed for the derived settling characteristics. As elaborated in chapter 5, the given settling response is primarily based on the operating region of the pass-transistor, implemented within the negative voltage regulator. To recap, at the instant the complete NVG system is powered up, it acquires an initial steady-state for the first t_1 seconds, with a nearly constant CP output voltage, corresponding with the saturation region operation of the pass-transistor. In the following t_2 seconds, the CP operates in the linear region and the $V_{CP}(t)$ magnitude

(a)

(b)

Fig. 6.7: Measured initial settling transients (a) V_{REG} : -2.8V, I_L : 200 μA , C_{EXT} : 220nF (b) V_{REG} : -3.0V, I_L : 250 μA , C_{EXT} : 220nF

decreases gradually along with V_{REG} . Finally, in Region III, the gain of the feedback loop is boosted as the regulated output approaches its desired magnitude, and the system acquires the final steady-state in the following t_3 seconds. The region-wise and the total settling time, for the given operating conditions, is also mentioned in

Table 6.3: Comparison of Settling time between Analysis, Simulation and Measurement (V_{REF} : -1.1V, C_{EXT} :220nF, CP Linear Model: $-4.88 + 3.9k\Omega \cdot I_L$)

Operating Condition	Analysis	Simulation	Measurement
V_{REG} :-2.8V, I_L : 200 μ A	1.162ms	1.198ms	1.2ms
V_{REG} :-3.0V, I_L : 250 μ A	1.458ms	1.508ms	1.6ms
V_{REG} :-1.5V, I_L : 400 μ A	0.625ms	0.667ms	0.8ms

Fig. 6.7.

In order to derive the given 3-phase settling characteristics, the regulator positive rail (V_{POS}) and reference input (V_{REF}) is re-adjusted to 0V and -1.1V, from its default settings. This ensures that, at time $t = 0$ seconds, the gate voltage ($V_{G_PT}(0)$) of the pass-transistor, is maintained equal to the initial regulated output ($V_{REG}(0)$) voltage at 0V. As a result, the pass-transistor operates in saturation region, at the instant the system is powered up, and hence all three regions of the settling response can be observed and measured. In the default settings, the pass-transistor is initially operating in the linear region, since the trigger is provided through the main supply, and therefore the $V_{G_PT}(0)$ is at 3.3V (default V_{POS}), while the $V_{REG}(0)$ is still pinned to 0V. To derive the complete 3-phase settling response under default settings, the system can be kept powered up while disabling the CP, such that the initial regulated output is pulled to supply potential through the feedback resistor divider. Following this, the trigger to capture the resulting settling response can be provided via enabling the CP, thus ensuring saturation region operation of the pass-transistor at time $t = 0$ seconds.

The complete measured settling profile presented in Fig. 6.7, can be verified to be consistent with the corresponding counterparts derived through transient co-simulation of CP and regulator module, large signal verification using regulator simulation setup and the numerical solution derived through the computational analysis of the settling behaviour. A comparison of the measured settling times with the corresponding simulated and analytically derived values, is presented in Table 6.3.

For the purposes of this comparison, the CP linear model used within the analytical model and the regulator simulation setup, is the one derived from the measured CP characterization curves, as presented in Fig. 6.4. As noted from the Table I, both the measured values of both the region-wise and the total settling time du-

ration can be accurately matched with the counterparts derived from large signal simulation and analysis. This further validates the proposed quantitative analysis of the settling transients and underlines its relevance in predicting the settling times as function of CP, regulator characteristics and operating parameters.

6.5 Transient Steady-State Ripple

The transient ripple amplitude is a key performance indicator which defines the performance limits of the regulated output voltage and thus provides a realistic estimate of the actual low-noise performance derived from the design. It is also an important parameter to be considered to assess the suitability of the regulated output for a given noise sensitive application. As mentioned in the section 6.2, to extract the peak performance, it is crucial to place the off-chip capacitor in close proximity of the regulated output pin. In addition, an optimized PCB implementation with effective grounding, can lead to further reduction in ripple amplitude and noise-content, and is therefore essentially required to derive the peak noise performance from the design.

In the given verification process, the required low-noise transient ripple measurement is recorded by Keysight 4034A digital-storage oscilloscope (DSO). The key advantage of this DSO is its large dynamic range, which allows direct measurement of high magnitude negative voltages. This implies that for the given system, V_{CP} and V_{REG} can be recorded directly without utilizing a pull-up resistor or using probe-scaling, thus minimizing the measurement related inaccuracies. In addition, its high BW (350MHz) and high sample rate (5Gs/sec) allows it to record both low and high frequency transient ripple, and thus facilitates an authentic low-noise measurement.

In order to capture the worst-case of the transient ripple performance, the following test conditions are enforced, while recording the steady-state waveforms presented in Figs. 6.8 and 6.9. Firstly, minimum value of external off-chip capacitor (C_{EXT} : 220nF), as required to maintain the unconditional stability of the regulator feedback loop is employed, while no decoupling capacitor is used for either supply or reference inputs. Secondly, the measurement is recorded at the maximum

(a) CP and Regulated output at a vertical resolution of 10mV/Div

(b) CP and Regulated output at a vertical resolution of 5mV/Div

(c) Reference input at a vertical resolution of 10mV/Div

Fig. 6.8: Measured steady-state ripple amplitude at (V_{REG} : -1.5V, I_L : 550 μ A, C_{EXT} : 220nF)

Fig. 6.9: Measured steady-state ripple amplitude (V_{REG} : 1.5V, I_L : 800 μ A, C_{EXT} : 220nF)

supported current magnitude corresponding to the given regulated output voltage. Thirdly long measurement time-span of 1ms is chosen in the DSO settings, to capture both low and high frequency drifts in the regulated output voltage and lastly, AC coupling is avoided to preserve the signal integrity from any possible low-pass filtering by the equipment. To further enhance the measurement accuracy, the vertical resolution of the DSO is reduced to lowest possible setting of 10mV/Div (or 5mV/Div), as feasible for the given measurement.

Referring to Fig. 6.8(a), the measured steady-state ripple amplitude for CP and regulated output is 27mV_{PP} and 2.7mV_{PP}, respectively, corresponding to regulated output at -1.5V at 550 μ A load current (I_L). As I_L is increased to 800 μ A corresponding V_{REG} at 1.5V, the CP ripple is increased to 54mV_{PP}, while the V_{REG} ripple is still maintained to 2.7mV_{PP}, as shown in Fig. 6.9. The measured reading for V_{REG} ripple amplitude further improves to 1.3mV_{PP} when the vertical resolution of the DSO is reduced from 10mV/Div to 5mV/Div, as shown in Fig. 6.8(b).

From Fig. 6.8, it can also be observed that the V_{REG} ripple is equal to ripple amplitude on the reference input (V_{REF}). Furthermore, it can be verified that V_{REG} ripple consistently tracks the V_{REF} ripple, invariant of the operating conditions and the measurement settings (horizontal/vertical resolution) of the equipment. This

observation confirms that the steady-state ripple performance is limited only by the accuracy of the reference input, and resolution of the measuring equipment, as previously predicted from the simulated steady-state ripple amplitudes of CP and regulated output, derived through the transient co-simulation of CP and regulator modules.

6.6 Noise Spectrum Analysis

The noise spectrum analysis provides an in-depth insight into the actual low-noise performance derived from the design, as it reveals the extend to which the CP noise is leaked into the regulated output. Therefore, it also provides a realistic estimate of the effective noise-suppression provided a given regulator topology, to the noise injected through the unregulated output of the CP. Since the CP noise is mainly concentrated at the harmonics of its operating frequency ($N \cdot F_{IN}$), the spectral analysis is measured in terms of the residual noise voltage level (V_{N_RMS}) at $N \cdot F_{IN}$, and capturing the resulting noise-floor level, as the remaining component of CP noise is distributed uniformly across the frequency spectrum. The regulator's noise rejection can thus be evaluated by change in the noise voltages levels as derived from the CP and regulated output voltage spectrum. The overall noise performance can be assessed by comparing the noise-floor for the regulated output with the equivalent derived for the reference input.

The given noise-spectrum analysis of the reference input and the CP and regulated output, is recorded using Rhode&Schwarz FSUP Signal Analyzer. Since the equipment is typically used for RF measurements, its high dynamic range facilitates direct rms noise-voltage measurements as low as hundreds of nV, while supporting frequency range of up to 20GHz. The input signal is AC coupled to the equipment using a SMA type DC-block component, with a frequency range from 5kHz to 23GHz. This DC-block provides minimal resistance to the input AC noise beyond kHz frequency range, thus allowing reliable noise-voltage measurements from the equipment, despite its low input impedance of 50Ω . Moreover, similar test conditions, as employed for the transient steady-state ripple measurement, are utilized to capture the worst-case performance limits of the design,. This broadly implies that

(a) CP output (V_{CP})

(b) Regulated output (V_{REG})

(c) Reference input

Fig. 6.10: Measured Noise spectrum (V_{REG} : -1.5V, I_L : 550 μ A, C_{EXT} : 220nF)

the minimum value for C_{EXT} is used for the testing, while the design is measured at the maximum load current supported for a given regulated output.

The measured noise spectrum for the CP and regulated output, corresponding to a test condition of -1.5V V_{REG} and 550uA load current, is as shown in Fig. 6.10. The resolution bandwidth is set 10kHz while the measurement span is adjusted to cover first 10 harmonics of CP operating frequency, set at 50MHz. The measurements are recorded from an averaged reading of 10 sweeps, to filter out fluctuations from thermal or ground noise. The resulting spectral analysis reveals that the maximum rms noise voltage for the CP is at $5.2mV_{RMS}$ at $2 \cdot F_{IN}$, while the corresponding number for the regulated output is below $280\mu V_{RMS}$ at $9 \cdot F_{IN}$ frequency. A comparison of the measured CP and regulated rms noise voltages at $N \cdot F_{IN}$ and the corresponding resulting regulator rejection, is as captured in Table. It can be noted that the given negative voltage regulator provides a 17-40dB of direct rejection to the harmonic noise spurs injected from the CP.

The noise spectrum of the reference input is also shown in Fig. 6.10(c). It can be observed that the rms noise-floor voltage is under $2\mu V_{RMS}$ for the reference input and under $5\mu V_{RMS}$ for the regulated output. The closely matched noise-floor voltage levels indicate minimal impact of CP noise on the of noise power spread uniformly across frequency, suggesting that the regulated output noise-floor is mainly determined by the noise-content of the reference input.

The given spectral analysis thus help to quantify the low-noise performance of the design. In addition, the low rms noise voltage levels at $N \cdot F_{IN}$ and the low rms noise-floor voltage validate the high degree of spectral purity obtained for the regulated negative output voltage.

6.7 Application Verification with GaN-HEMT PA

To examine the performance of proposed NVG system in a practical application environment, it is tested with a state-of-the-art GaN-HEMT RF power-amplifier (PA). The GAN-HEMT device having depletion mode characteristic, requires a precisely controlled negative gate voltage to bias it in the correct region of operation, as required by the end application of PA. The GaN-HEMT PA application is specifically

Fig. 6.11: Test setup for application verification with GaN-HEMT power-amplifier

demanding, since the negative gate voltage should also be low-noise input, such that noise is not up-converted to RF frequencies, resulting in potential corruption of RF output spectrum. Therefore, the GaN PA biasing is considered as the key target application for the proposed design, with the initial design specifications loosely based on the negative gate voltage tuning range and the typical maximum gate leakage current, required for such PA implementations.

In the given verification process, the PA is initially optimized to deliver maximum performance by fine tuning all the input parameters, including RF centre frequency, input power and negative voltage magnitude, supplied from an external source. As a following step, the proposed NVG is set to provide the negative gate-bias for the PA at the required magnitude. The resulting PA's linearity and efficiency performance is carefully compared to the previous case, to detect any observable impact of proposed NVG's regulated negative output on the PA performance indicators.

The complete test setup is as shown in Fig. 6.11. The standard wide-band input signal is programmed into the Arbitrary waveform generator (AWG) through a MATLAB utility running on the master PC. The corresponding baseband signal generated from the AWG is unconverted to RF frequencies using the vector signal generator (VSG) and capacitively coupled into the GaN PA after pre-amplification.

The negative gate voltage is carefully tuned to set the quiescent point of the GaN-HEMT PA to deliver maximum linearity for the given RF input power and frequency. The resulting RF output is attenuated to the required power levels and captured on a wideband signal analyzer. The digitized RF output signal is analyzed using the VSA software running on the PC, and its performance is evaluated as per the wireless standard specifications .

The proposed NVG system is tested with state-of-the-art GaN PA reported in [21]. The given PA is designed for 5GHz, 802.11ac (WLAN) application, and delivers high output power with high efficiency, while meeting the 802.11ac standard specifications. The drain voltage for the PA is at 28V, while the negative voltage is tuned from -2.8V to -3.2V, to ensure deep Class-AB operation for the GaN device, as intended for this design. In the given verification with the proposed NVG, the PA is tested with the most stringent input test waveform, in order to have a more discernible effect (if any) of NVG non-linearities on the PA performance parameters. The PA performance is thus evaluated for VHT80 MCS9 (80MHz wide bandwidth, 256 QAM constellation) and optimized using an external source to derive the correct set-point for the negative gate bias input. Following this, proposed NVG is replaced as the negative source, and is tuned to provide the gate bias at the required negative voltage magnitude.

The resulting PA performance, captured in terms of the RF output spectrum, constellation diagram and the EVM measurement, is as shown in Fig. 6.12. For the given 802.11ac input signal, the GaN delivers an output power of 24.5dBm with 31.4% drain-efficiency, while meeting the standard specification of maintaining EVM < -32dB. The given GaN PA's linearity and efficiency performance is verified to be exactly identical to that obtained using an external negative voltage source. In addition, no distortion is visible in 80MHz wide output spectrum or in 256-QAM constellation, while the EVM numbers are also same as the reference case. This application verification therefore clearly demonstrates the suitability of the proposed NVG for various precision voltage-biasing and noise-sensitive application.

(a)

(b)

(c)

Fig. 6.12: GaN-HEMT PA RF performance with proposed NVG system (a) Spectrum (802.11ac, VHT80: 80MHz BW) (b) Constellation (MCS9: 256-QAM)(c) EVM magnitude (802.11ac, VHT80, MCS9)

6.8 Performance Summary and Comparison

The complete system level performance of the proposed NVG is summarized and compared with other reported switched-capacitor based regulated negative voltage generator, as mentioned in Table 6.4. The given implementation explores and verifies the design possibility arising from the combination of fully-integrated negative voltage CP with a linear regulator arrangement, to derive regulated negative voltage output. The resulting system level implementation deliver low-noise regulated output along with wide-tuning range and moderate driving capacity. The low-noise performance of the design is rigorously verified through transient steady-state ripple measurement and spectral analysis of regulated output. The measured transient

Table 6.4: Performance Summary and Comparison with other Regulated Negative Voltage Generator

Parameters	[18]	This Work [40]
V_{DD}	1.8V	3.3V
V_{REG} Range	-8.0V	-4.4V to 2.1V
Max. Load	320 μ A	>250 μ A ($V_{OUT} > -3.0$ V) >550 μ A ($V_{OUT} > -1.5$ V)
Load Reg.	194 μ V/ μ A	102 μ V/ μ A
V_{REG} Ripple	30mV $_{PP}$	< 3mV $_{PP}$
V_{N_RMS} at $N \cdot F_{IN}$	-	< 130 μ V $_{RMS}$
Settling Time	-	< 1.2ms (C_{EXT} : 220nF)
Power	3.8mW	12.5mW
Area/ Process	1.27mm ² / 180nm CMOS	0.55mm ² 180nm CMOS

steady-state ripple for the regulated output is under $3mV_{PP}$, while the rms noise voltage level at CP operating frequency, as obtained from its spectral analysis, is below $280\mu V_{RMS}$, across its operating range. The regulated output magnitude can be further tuned over a very wide tuning range from -4.4V to 2.1V for biasing application ($I_L \sim 0\mu A$), thus verifying that both negative and positive voltage can be derived from the same regulated output node. The design also supports moderate driving capacity with a maximum supported load current of 250 μA , 550 μA and 800 μA for regulated output voltages -3.0V, -1.5V and 1.5V, respectively. Lastly, the design is application verified with GaN-HEMT PA to further validate its low-noise performance and demonstrate its implementation potential for precision voltage biasing and noise sensitive applications.

In contrast to the work reported in [18], which is designed for a fixed regulated output at -8.0V and maximum load current at 320 μA , the proposed NVG supports a much wider regulated output voltage range, including positive output voltages, while supporting a higher load current range, with the maximum load current at 800 μA (for $V_{REG} \geq 1.5$ V). In [18], the CP output is regulated by operating it within a digital feedback loop, while the given design utilizes a separate linear regulator stage. The given regulation strategy results in a significant improvement in both the regulation accuracy and the low-noise performance of the design. As compared to [18], the regulation accuracy in terms of the resulting load regulation is improved by 50%, while transient steady-state ripple is reduced by an order of magnitude. Moreover,

the measured steady-state ripple amplitude is verified to be limited only by the accuracy of external reference input. However, despite the performance advantages, the proposed NVG incurs higher power consumption as compared to [18]. This can be mainly attributed to the higher CP efficiency in [18], which utilizes a 6-stage bootstrap structure with 25pF pump-capacitance per stage (C_P), in order to derive the required high negative voltage magnitude. In contrast, in the given NVG system, the negative voltage CP is also a bootstrap topology, however implemented in a 2-stage configuration with 15pF C_P per stage, thus resulting in the significantly lesser area utilization, at the cost of lower efficiency. As compared in Table, the proposed NVG system has significantly lower silicon footprint, give that both works are implemented on the same technology node.

6.9 Chapter Summary

This chapter presents a comprehensive performance summary of the proposed NVG system, as captured through an extensive experimental verification of its fabricated prototype. The overall performance was analyzed and verified from various dimensions, including performance characterization of the CP, initial settling response and low-noise performance of the regulated output. The derived measurement results are thoroughly analyzed and contrasted with corresponding simulation and analysis results for further validation.

In terms of the experimental verification, the CP performance is characterized across load current and operating frequency, and the resulting frequency dependent CP linear model is compared with the counterpart obtained from post-layout simulations. At the system level, the measurement results for the initial settling transients are presented and the resulting 3-phase settling response is accurately matched to that corresponding values obtained from simulation and quantitative analysis.

In the following two sections, the noise performance of the design is verified using the transient steady-state ripple measurement and noise spectrum analysis for CP and regulated outputs voltages. The measured steady-state ripple amplitude is under $3mV_{PP}$ and remains equal to ripple amplitude for reference input, under all operation conditions and measurement settings, thus suggesting that the per-

formance bottleneck is set through the accuracy of reference input itself. Finally the design is application verified with a GaN-HEMT RF PA thus highlighting its usability for applications requiring well-regulated, low-noise input.

Chapter 7

Conclusion and Future Works

7.1 Conclusion

This thesis presents the design, analysis and verification of a low-noise, regulated negative voltage generator (NVG). The design primarily composed of a fully-integrated, negative voltage charge-pump (CP) and a linear regulator module, serves as a highly integrated solution for generating low-noise negative voltage output, while requiring only one off-chip capacitor, that can be shared with supply decoupling capacitor(s) of the end application. The resulting configuration, also allows the design to achieve high regulation accuracy and wide tuning range, including positive output voltages, while supporting moderate load driving capacity of loads up to $800\mu A$.

The design derives its integration advantage and low-noise performance through the adaption of fully-integrated CP, however the stability of regulator's feedback loop is impacted by the specific transfer characteristics of the given CP implementation. Thus, to ensure robust implementation, a systematic design methodology is adopted for the derivation of CP and regulator specification and the subsequent system level verification. A novel switched-capacitor (SC) CP operational analysis, invariant of the CP operating regime, is proposed and utilized to optimize the given CP implementation for minimum area utilization. The resulting CP linear model, as extracted from its transfer characteristics, is included in the regulator simulation setup and further utilized in the analytical models, to capture the effect of CP output response on the regulator and at the system level. The system level performance is evaluated using both small and large-signal techniques, including verification of

regulator’s feedback loop stability, AC analysis of the CP noise rejection and the derivation and analysis of the initial settling transients. The overall functionality and performance is additionally verified using transient co-simulation of CP and regulator modules.

The analysis and performance of the proposed NVG system is experimentally verified using a prototype chip fabricated using GlobalFoundries CMOS 180nm BCDlite process. With a 3.3V positive rail input, the design provides an output tuning range from -4.4V to +2.1V, while supporting a maximum load current of up to $250\mu A$, $550\mu A$ and $800\mu A$, for regulated output voltage at -3.0V, -1.5V and 1.5V, respectively. The measured steady-state ripple amplitude for the regulated output is under $3mV_{PP}$, while the rms noise-voltage at the CP operating frequency harmonics is below $280\mu V_{RMS}$, thus validating the low-noise performance of the design. Lastly, the design is application verified with a state-of-the-art GaN HEMT PA, whereby the PA delivers identical performance as obtained from an external negative source.

The proposed NVG is a first-of-its-kind implementation of fully-integrated CP output driving a linear regulator module. The resulting configuration deliver several key performance advantages, such as effective CP noise rejection, high-regulation accuracy and wide output tuning range, however practical design concerns arising from the high output impedance of the CP, need to be identified and addressed. A structured design flow along with a rigorous multi-dimensional analysis and verification ensures a robust implementation with reliable performance output. An in-depth analysis is presented at the both the module and system level and the analytical results are consistently validated through the corresponding simulation and measurement. Moreover the presented analysis provides scalability to the key design ideas introduced in this work, such that they can be readily utilized for the design of other switched-capacitor based regulated voltage generators. Finally, the silicon verification of the design, clearly verifies the superior low-noise performance and highlights its implementation potential for precision voltage biasing and noise sensitive applications.

Some potential directions for advancing this work are presented in the following section.

7.2 Future Works

7.2.1 Increasing Driving Capacity

The proposed NVG system is designed to support a load current range of $250\mu\text{A}$ to $800\mu\text{A}$ for regulated output voltage range from -3.0V to $+2.1\text{V}$, respectively. Although the given load driving capacity is suffice for a wide range of low-power applications, such as depletion mode biasing, static leakage reduction, biomedical tissue stimulation etc., it is not to high enough to meet the driving requirements of certain applications such as split-rail instrumentation amplifiers and LCD driver circuits. Therefore, to support multiple negative voltage applications, it is desirable to increase the load driving capacity of the current prototype by an order of magnitude ($I_L > 5\text{mA}$), while retaining the full integration of the negative voltage CP. The latter is essential since the design derives both its integration and performance advantage through the adaption of given CP implementation. It is also of immense interest to test the performance limits of a fully-integrated switched-capacitor (SC) CP in terms of its load driving capacity, while ensuring reasonable design considerations (area/power) for its practical silicon implementation.

In general, a higher load current (I_L) requirement for the CP directly translates into lower CP output impedance (R_{CP}) specification. As seen from the SC-CP analysis presented in this work, the R_{CP} magnitude can be reduced by applying one or more of the following three approaches: (i) utilize a higher pump-capacitance per stage (C_P), (ii) employ a larger switching device, implying lower switch-resistance (R_{SW}) or (iii) operate at higher switching frequency (F_{IN}). A rough estimate of the CP performance limits can be derived by varying these design and operating parameters for the 2-stage bootstrap CP used in the given design, as shown in Fig. 7.1. The modified CP implementation is characterized across C_P values while supporting a higher load current range of 1mA to 6mA . The resulting CP steady-state output voltage (V_{CP}) vs. load current (I_L) is as shown in Fig. 7.1(a) and the corresponding CP output impedance (R_{CP}) across C_P is captured in 7.1(b). It can be observed that the CP output magnitude ($|V_{CP}|$) exceeds -4.0V at $I_L < 2\text{mA}$ and $C_P > 20\text{pF}$, while $|V_{CP}|$ exceeds -3.0V for $I_L < 5\text{mA}$ and $C_P > 40\text{pF}$. This simulation result is obtained by utilizing a larger charge-transfer switch dimensioned

Fig. 7.1: 2-stage Bootstrap CP characterization at higher load currents (a) CP output vs load current across pump capacitance values (b) CP output impedance vs pump-capacitance (Switch (W/L) : (160 μ m/0.6 μ m), F_{IN} : 150MHz)

at (W/L : 160 μ m/0.6 μ m), while operating the CP at a higher frequency of 150MHz. In contrast, for the 2-stage bootstrap CP used in the given design, the charge-transfer switch was dimensioned at (W/L : 40 μ m/0.6 μ m) and the CP operating frequency was in the range of 30MHz - 70MHz. This initial feasibility study clearly highlights the potential for switched-capacitor based fully-integrated CP structures to support high load currents. It is to be noted that the actual CP performance can be significantly improved, possibly requiring lower C_P and F_{IN} values, by following a more structured optimization sequence, as presented in the given work.

To implement an overall practical and optimized CP implementation, the increase in the CP driving capacity must be carefully considered in conjunction with area, power and efficiency trade-off involved in the process. The CP area utilization increases due to both, a higher C_P and lower R_{SW} magnitude, required to achieve higher driving capacity. The higher C_P magnitude requires larger buffer stages, leading to increased power consumption in the driver circuits. Moreover, power consumed in digital circuits increases linearly with frequency, thus implying

an increase in total spurious power consumption, as CP operating frequency is increased to support higher load currents. At higher I_L magnitude, the net effect of the increased power consumption on the CP efficiency (η_{Eff}) is balanced out in part due to the higher power delivered at the output, and therefore η_{Eff} has to be carefully optimized specific to the given CP implementation and design specifications. A higher operating frequency also implies that the CP is likely operating in deep FSC condition, which results in a more pronounced effect of on-time of charge-transfer switches (T_{ON}) and switch resistance (R_{SW}), on the overall CP transfer characteristics. Therefore, the effect of T_{ON} and R_{SW} must be considered in CP optimization process, and the minimum achievable CP output impedance (R_{CP_MIN}), corresponding to the maximum CP operating frequency (F_{IN_MAX}), must be ensured to be lower than the required R_{CP} magnitude. The implication of a higher load current on the regulation design and operation is considered in one of the following sections.

7.2.2 Charge-Pump Efficiency Enhancement

The area vs power-efficiency trade-off is at the heart of switched-capacitor design and optimization effort. In the current NVG system, the negative voltage CP is optimized for minimum area utilization, however this design approach translates into low CP power-efficiency. The given CP is implemented in 2-stage bootstrap configuration and utilizes a relatively low-value of pump-capacitance (C_P : 15pF) per stage, thus resulting in smaller silicon footprint, however the peak CP efficiency is under 13%, across its operating envelope. Therefore, for future NVG implementations, firstly, it is suggested to adopt a more evenly poised design strategy, between area and power efficiency optimization, while realizing a CP implementation for a given set of design specification. Secondly, it is also essential to explore the circuit design techniques through which the ratio of peak-efficiency to CP Area ($\eta_{Eff}/Area$) can be maximized, such that a more acceptable design trade-off can be attained, while resolving the two conflicting requirements of simultaneously minimizing area utilization and power consumption.

The SC-CP efficiency versus load current and operating frequency variation was analyzed in section 4.4.4. As depicted in Fig. 4.17, for a given operating frequency

(F_{IN}), the SC-CP efficiency vanishes at low and high-loading conditions, while being maximized at a optimum load current magnitude. Therefore, in addition to maximizing the peak CP efficiency, it is also desirable to maximize the efficiency at low-load currents and preferably attain a flatter efficiency curve across the supported load current ranges. This feature can vastly improve the application potential of the improvised NVG system, allowing it to effectively support multiple applications with varying driving requirements, without incurring efficiency degradation.

The scope of CP efficiency maximization can be analyzed through its equivalent expression derived in terms of the CP output impedance (R_{CP}), as reproduced in (7.1).

$$\eta_{Eff} = \frac{(N \cdot |V_{DD}| \cdot \gamma - I_L R_{CP}) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{PAR})} \quad (7.1)$$

From (7.1), it can be observed that, the SC-CP efficiency magnitude can be increased by increasing the number of CP stages (N), reducing the CP output impedance (R_{CP}) or by minimizing the digital power consumption ($I_{PAR} \cdot V_{DD}$). In practice, increasing the number of stages is usually not feasible as N is linked to the voltage conversion ratio required by the end application. Moreover, increasing N incurs higher switching losses across the CP stages, and thus results in a higher effective R_{CP} . In contrast, R_{CP} can be reduced by increasing the pump-capacitance (C_P) or reducing the switch-resistance (R_{SW}) by utilizing a large switching device, both of which results in higher area utilization. Thus, for a practical SC-CP implementation, the R_{CP} magnitude can be minimized based on the available area, by utilizing an optimum combination of C_P and R_{SW} values, as was proposed and implemented in this work. The R_{CP} magnitude can also be reduced by increasing the CP operating frequency, however this results in a linear increase in digital power consumption ($I_{PAR} \cdot V_{DD}$), and thus cannot be applied directly for maximizing the CP η_{Eff} value.

The digital power consumption can be minimized by employing a more aggressive optimization of clock buffers, such that the inverter chain for each switching input is carefully sized as per its respective capacitive loading within the CP. In addition, I_{PAR} can be significantly reduced by utilizing a CP topology employing a simpler input switching scheme. This was verified in section 2.5.5, where the Latched CP utilizing 2-phase switching input is shown to deliver significantly higher efficiency as

compared to an equivalent bootstrap CP implementation requiring 4-phase input, while both the CPs provided a similar R_{CP} magnitude.

To maximize the CP efficiency at low-load currents, the simplest approach is to operate the CP within a digital feedback loop, as was utilized for the first regulation technique presented in section 3.3. This scheme intermittently turns off the CP and the driver circuits, based on the loading condition such that the CP output is confined within a comparator’s hysteresis range. This burst-mode operation for the CP can significantly boost the efficiency at low-loads, however, as loading is increased, the CP steadily transitions to an ‘always-on’ state and therefore the resulting efficiency from the given configuration tracks the efficiency characteristics obtained for normal CP operation at high load-currents.

In order to maximize the CP efficiency across the supported load current range, one of the directions that can be explored, is to implement a adaptive frequency selection scheme [1], which can select the optimum CP switching frequency at which the CP efficiency is maximized, at a given load current. The main design challenge would be to derive an CP efficiency dependent control voltage (or current) that can be used for the maximum power point tracking of the CP and thus be supplied to an on-chip VCO for optimal frequency selection. In addition, sufficient headroom must be maintained across the regulator’s pass-transistor as required for it operate in saturation region or under dropout condition, corresponding to the system operation at a given regulated output and load current setting. This will ensure, regulator continues to operate effectively with high loop-gain, while the CP efficiency is maximized within the adaptive frequency selection closed loop.

7.2.3 Negative Voltage Regulator Re-Design

The negative voltage linear regulator implemented in the current NVG system, provides an unconditionally stable operation across its operating range, while effectively suppressing CP noise/ripple to provide low-noise output with high regulation accuracy and reduced output impedance. However, the regulator design will need to be revisited in order to support a higher load current range and deliver a higher system efficiency. As suggested in the previous section, the next generation of NVG implementation can be targeted to achieve an order of magnitude improvement in the

driving capacity of the current system, thus supporting load currents in excess of 5mA. Moreover, to maximize the end-to-end system efficiency, the dropout voltage for the pass-transistor, under maximum loading conditions, should be maintained as low as possible. Both of these requirements will translate into a significantly larger dimension for the pass-transistor, as compared to its counterpart in the current NVG implementation. The higher load current and larger pass-transistor sizing will also have major implications on the stability of the regulator's feedback loop since the dominant load pole will shift outwards, while the parasitic pole at the gate of pass-transistor, will shift inwards to lower frequencies. Thus, to ensure stable operation, the OTA output will require to be followed by a low output impedance buffer stage for driving the large pass-transistor, such that parasitic pole at its gate is shifted beyond the unity-gain frequency of the loop. In general, the negative voltage regulator module can be expected to draw significant design effort in order to adequately adapt to the updated specifications of higher load current and lower pass-transistor dropout voltage.

In addition to upgrading the existing regulator for supporting higher load currents, novel regulation architectures, that can lead to additional design features or improvements in the regulator and system level performance, can also be explored. For instance, it can be noted that the only indispensable off-chip component required for the current design, is the external capacitor, used for stabilizing the regulator feedback loop. It thus follows that an internally compensated regulator architecture can be investigated, as this would facilitate the full integration of NVG system, and thus vastly enhance its range of potential applications.

The existing regulator topology can also be modified as shown in Fig. 7.2, in which the regulator sub-circuits are powered from standard positive and GND rails, while the pass-transistor is driven indirectly from the error-amplifier output through a resistor divider arrangement. Therefore, unlike the current NVG implementation, in which regulator utilizes the CP output as its negative supply rail, in this arrangement the regulator biasing current is not contributed towards the total current injected into the CP, and can therefore be utilized as additional driving capacity for the system. In general, for any regulator implementation, the most important consideration is to verify that stability of the feedback loop, across the operating

Fig. 7.2: Proposed modification to existing regulator topology

range, following which, the regulator performance can be evaluated in terms of the effective rejection magnitude provided at DC and at the CP operating frequency.

Author's Publications

(1) **D. Khanna**, C. C. Boon, P. Choi, L. Siek, B. Liu and C. Li, "A Low-Noise, Positive-Input, Negative-Output Voltage Generator for Low-to-Moderate Driving Capacity Applications," in *IEEE Tran. on Circuits and Sys.-I, Regular Papers*, vol. 66, no. 9, pp. 3423 - 3436, July 2019.

(2) P. Choi, S. Goswami, U. Radhakrishna, **D. Khanna**, C.-C. Boon, H.-S. Lee, D. Antoniadis and L.-S. Peh, "A 5.9-GHz Fully Integrated GaN Frontend Design With Physics-Based RF Compact Model," in *IEEE Trans. of Microw. Theory and Techniques*, vol. 63, no. 04, April 2015.

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Appendix I: Derivation of CP Output Impedance Function

This Appendix section provides the MATLAB code utilized for deducing the closed form expression of the analyzed CP output impedance function (R_{CP_FXN}). In addition, the MATLAB code is also serves the following objectives:

1. Analyze the weight of each sub-term in the derived CP output function, when expressed as SOP (sum of product) expression.
2. Derive closed-form expression of CP output impedance, with varying degree of accuracy, dependent on the number of terms incorporated in the simplified CP output impedance function.
3. Analyze the effect of CP design and operating parameters on the CP output impedance and compare the results obtained for original CP output impedance function (R_{CP_FXN}) with its simplified expression (R_{CP_EST1} , R_{CP_EST2} , R_{CP_EST3}), in order to benchmark their respective accuracy.
4. Obtain the 2-D plot for original CP output impedance function (R_{CP_FXN}) with respect to pump-capacitance (C_P) and switch-resistance (R_{SW}).

The given MATLAB code in a documented format, is presented as follow:

```
1 clear;
2 clc;
3
4 syms Voh_f Vol_f V2h_i V2h_f V2l_i V2l_f V1h_i V1h_f V1l_i V1l_f;
5 syms Rsw Cp Cs CL Tprd Ton IL Vdd;
6 syms IC12 IC20 Ceq D1 D2;
7 syms K % Ratio of (Ton/Tprd)
```

```

8 syms K2 % Ratio ( Cp/(Cp+Cs+Cpar) ):
9
10
11 % EQN-1
12 eqn1 = V2l_i == V2h_f - Vdd*K2;
13
14 % EQN-2
15 eqn2 = V2h_i == V2l_f + Vdd*K2;
16
17 % EQN-3
18 eqn3 = V1l_i == V1h_f - Vdd*K2;
19
20 % EQN-4
21 eqn4 = V1h_i == V1l_f + Vdd*K2;
22
23 % EQN-5
24 eqn5 = V1h_f == V1h_i*exp((-Ton)/(2*Rsw*Cp));
25
26 % EQN-6
27 eqn6 = V1l_f == ( IC12 - Cp*(V2h_i - ...
    V1l_i)*exp((-Ton)/(Rsw*Cp*0.5)) ) / (2*Cp);
28
29 % EQN-7
30 eqn7 = V2h_f == ( IC12 + Cp*(V2h_i - ...
    V1l_i)*exp((-Ton)/(Rsw*Cp*0.5)) ) / (2*Cp);
31
32 % EQN-8
33 eqn8 = IC12 == (Cp*V1l_i + Cp*V2h_i);
34
35 % EQN-9
36 eqn9 = V2l_f == ( IC20 + IL*(Ton - Rsw*Ceq) )/(Cp+CL) + ...
    D1*exp((-Ton)/(Rsw*Ceq));
37
38 % EQN-10
39 eqn10 = Vol_f == ( IC20 + IL*Rsw*Cp + IL*(Ton - Rsw*Ceq) ...
    )/(Cp+CL) + D2*exp((-Ton)/(Rsw*Ceq));
40
41 % EQN-11
42 eqn11 = Ceq == (Cp*CL)/(Cp + CL);

```

```

43
44 % EQN-12
45 eqn12 = IC20 == (Cp*V2l_i + CL*Voh_f);
46
47 % EQN-13
48 eqn13 = D1 == (IL*Rsw*Ceq - CL*(Voh_f - V2l_i)) / (Cp + CL);
49
50 % EQN-14
51 eqn14 = D2 == D1*(-1*Cp/CL);
52
53 % EQN-15
54 eqn15 = Voh_f == Vol_f + (IL/CL)*(Tprd - Ton);
55
56 % EQN-16
57 %eqn16 = K2 == 0.9;
58
59
60 sol = solve([eqn1 eqn2 eqn3 eqn4 eqn5 eqn6 eqn7 eqn8 eqn9 eqn10 ...
    eqn11 eqn12 eqn13 eqn14 eqn15], [Voh_f Vol_f V2h_i V2h_f ...
    V2l_i V2l_f V1h_i V1h_f V1l_i V1l_f IC12 IC20 Ceq D1 D2]);
61
62 Voh_f_expr = (sol.Voh_f);
63 Vol_f_expr = (sol.Vol_f);
64 Vout_avg_expr = 0.5*(Voh_f_expr + Vol_f_expr);
65
66 [Vout_avg_coeff , ILpowers] = coeffs(Vout_avg_expr, IL);
67
68 Vcp0_expr = Vout_avg_coeff(2);
69 Vcp0_expr = simplify (Vcp0_expr)
70 Rcp_expr = Vout_avg_coeff(1);
71
72 var_name = [Rsw Cp CL Tprd Ton Vdd];
73 var_value = [(230) (15*10^(-12)) (260*10^(-12)) (20*10^(-9)) ...
    (7.8*10^(-9)) (3.3)];
74
75 Vout_avg_val = vpa(subs(Vout_avg_expr, [var_name, IL], ...
    [var_value, (200*10^(-6))]),64 )
76 Vcp_0_val = vpa(subs(Vcp0_expr, [var_name], [var_value]),64 )
77 Rcp_val = vpa(subs(Rcp_expr, [var_name], [var_value]),64 )

```

```

78
79 Vout_avg_fxnIL = vpa(subs(Vout_avg_expr, [var_name], ...
    [var_value]),64 )
80
81 [Rcp_num, Rcp_dnm] = numden(Rcp_expr);
82
83 Rcp_num_val = vpa(subs(Rcp_num, [var_name], [var_value]),64 );
84 Rcp_dnm_val = vpa(subs(Rcp_dnm, [var_name], [var_value]),64 );
85 Rcp_val_verify = Rcp_num_val / Rcp_dnm_val
86
87 Rcp_num_terms = children(Rcp_num);
88 Rcp_dnm_terms = children (Rcp_dnm);
89
90 Rcp_num_terms_val = vpa(subs(Rcp_num_terms, [var_name], ...
    [var_value]),64 );
91
92 Rcp_terms_val = Rcp_num_terms_val / Rcp_dnm_val ;
93
94 grid on;
95 Bargraph (Rcp_terms_val)
96
97 % ----- First, Most Simplified Approximatin for ...
    Rcp-----
98 Rcp_dnm_aprx = -2*Cp*CL*(Cp+CL)*exp((Ton*(CL + ...
    Cp))/(CL*Cp*Rsw))*exp((2*Ton)/(Cp*Rsw));
99
100 Rcp_aprx1_expr = (Rcp_num_terms(26) + Rcp_num_terms(28) + ...
    Rcp_num_terms(33)) / Rcp_dnm_aprx;
101 Rcp_aprx1_val = vpa(subs(Rcp_aprx1_expr, [var_name], ...
    [var_value]),64 )
102
103 Rcp_aprx1 = (simplify (Rcp_aprx1_expr));
104 pretty (Rcp_aprx1)
105
106 % ----- Second Approximatin for ...
    Rcp-----
107
108 Rcp_aprx2_expr = (Rcp_num_terms(26) + Rcp_num_terms(28) + ...
    Rcp_num_terms(33)) / Rcp_dnm;

```



```

109 Rcp_apprx2_val = vpa(subs(Rcp_apprx2_expr, [var_name], ...
    [var_value]),64 )
110
111 Rcp_apprx2 = (simplify (Rcp_apprx2_expr));
112 pretty (Rcp_apprx2)
113
114 % ----- Third, Most Detailed Approximation for ...
    Rcp-----
115
116 Rcp_apprx3_expr = (Rcp_num_terms(1) + Rcp_num_terms(10) + ...
    Rcp_num_terms(11) + Rcp_num_terms(12)+ Rcp_num_terms(13)+ ...
    Rcp_num_terms(6)+ Rcp_num_terms(25)+ Rcp_num_terms(26)+ ...
    Rcp_num_terms(27)+ Rcp_num_terms(28)+ Rcp_num_terms(33)) / ...
    Rcp_dnm;
117 Rcp_apprx3_val = vpa(subs(Rcp_apprx3_expr, [var_name], ...
    [var_value]),64 )
118
119 Rcp_apprx3 = (simplify (Rcp_apprx3_expr))
120 pretty (Rcp_apprx3)
121
122 %-----
123 % Observing Impact of K = (Ton/TPrd) on Vavg / Rcp / Rcp_apprx1 ...
    ...etc
124
125 var_K = [Rsw Cp CL Tprd IL Vdd];
126 var_val_K = [(250) (15*10^(-12)) (260*10^(-12)) (20*10^(-9)) ...
    (500*10^(-6)) (3.3)];
127
128 Vout_K_terms = vpa(subs(Vout_avg_expr, [Ton], [K*Tprd]),64 );
129 Vout_fxn_K = vpa(subs(Vout_K_terms, [var_K, K2], [var_val_K, ...
    0.9]),64 );
130 %Vout-vs-K-Plot (Vout_fxn_K);
131
132 % Original Rcp expression in terms of K
133 Rcp_K_terms = vpa(subs(Rcp_expr, [Ton], [K*Tprd]),64 );
134 Rcp_fxn_K = vpa(subs(Rcp_K_terms, [var_K], [var_val_K]),64 ); % ...
    Green-Line 'o'
135
136 % Rcp First Approx. expression in terms of K

```

```

137 Rcp_apprx1_K_terms = vpa(subs(Rcp_apprx1_expr, [Ton], ...
    [K*Tprd]),64 );
138 Rcp_apprx1_fxn_K = vpa(subs(Rcp_apprx1_K_terms, [var_K], ...
    [var_val_K]),64 ); % Blue-Line '+'
139
140 % Rcp Second Approx. expression in terms of K
141 Rcp_apprx2_K_terms = vpa(subs(Rcp_apprx2_expr, [Ton], ...
    [K*Tprd]),64 );
142 Rcp_apprx2_fxn_K = vpa(subs(Rcp_apprx2_K_terms, [var_K], ...
    [var_val_K]),64 ); % Red-Line '*'
143
144 % Rcp Third Approx. expression in terms of K
145 Rcp_apprx3_K_terms = vpa(subs(Rcp_apprx3_expr, [Ton], ...
    [K*Tprd]),64 );
146 Rcp_apprx3_fxn_K = vpa(subs(Rcp_apprx3_K_terms, [var_K], ...
    [var_val_K]),64 ); % Cyan-Line 'x'
147
148
149 Rcp_vs_K_Plots(Rcp_fxn_K, Rcp_apprx1_fxn_K, Rcp_apprx2_fxn_K, ...
    Rcp_apprx3_fxn_K)
150
151 % Observing Impact of Cp on Rcp ...
    -----
152
153 var_Cp = [Rsw CL Ton Tprd IL Vdd];
154 var_val_Cp = [(230) (260*10^(-12)) (7.8*10^(-9)) (20*10^(-9)) ...
    (500*10^(-6)) (3.3)];
155
156 % Original Rcp expression in terms of Cp
157 Rcp_fxn_Cp = vpa(subs(Rcp_expr, [var_Cp], [var_val_Cp]),64 );
158
159 % Rcp First Approx. expression in terms of Cp
160 Rcp_apprx1_fxn_Cp = vpa(subs(Rcp_apprx1_expr, [var_Cp], ...
    [var_val_Cp]),64 ); % Blue-Line '+'
161
162 % Rcp Second Approx. expression in terms of Cp
163 Rcp_apprx2_fxn_Cp = vpa(subs(Rcp_apprx2_expr, [var_Cp], ...
    [var_val_Cp]),64 ); % Red-Line '*'
164

```

```

165 % Rcp Third Approx. expression in terms of Cp
166 Rcp_apprx3_fxn_Cp = vpa(subs(Rcp_apprx3_expr, [var_Cp], ...
    [var_val_Cp]),64 ); % Cyan-Line 'x'
167
168 Rcp_vs_Cp_Plots(Rcp_fxn_Cp, Rcp_apprx1_fxn_Cp, ...
    Rcp_apprx2_fxn_Cp, Rcp_apprx3_fxn_Cp)
169
170
171
172 %`Creating a Table for Rcp_vs_Cp
173 Cp_val = linspace((5*10−12), (60*10−12),550);
174 Cp_val = [Cp_val]';
175 Rcp_Cp_val = vpa(subs(Rcp_fxn_Cp, [Cp], [Cp_val]),64 );
176 digits(100);
177 Rcp_Cp_val = double (Rcp_Cp_val);
178
179 % Location & FileName for Tabulating Rcp_vs_Rsw
180 Rcp_vs_Cp_Tablename = '.....';
181
182 Rcp_vs_Cp_Table = table(Cp_val,Rcp_Cp_val);
183 %writetable(Rcp_vs_Cp_Table,Rcp_vs_Cp_Tablename,'Sheet',1)
184
185
186 % Observing Impact of Rsw on Rcp ...
    -----
187
188 var_Rsw = [Cp CL Ton Tprd IL Vdd];
189 var_val_Rsw = [(15*10−12) (260*10−12) (7.8*10−9) ...
    (20*10−9) (500*10−6) (3.3)];
190
191 % Original Rcp expression in terms of Rsw
192 Rcp_fxn_Rsw = vpa(subs(Rcp_expr, [var_Rsw], [var_val_Rsw]),64 );
193
194 % Rcp First Approx. expression in terms of Rsw
195 Rcp_apprx1_fxn_Rsw = vpa(subs(Rcp_apprx1_expr, [var_Rsw], ...
    [var_val_Rsw]),64 ); % Blue-Line '+'
196
197 % Rcp Second Approx. expression in terms of Rsw
198 Rcp_apprx2_fxn_Rsw = vpa(subs(Rcp_apprx2_expr, [var_Rsw], ...

```

```

    [var_val_Rsw]),64 ); % Red-Line '*'
199
200 % Rcp Third Approx. expression in terms of Rsw
201 Rcp_apprx3_fxn_Rsw = vpa(subs(Rcp_apprx3_expr, [var_Rsw], ...
    [var_val_Rsw]),64 ); % Cyan-Line 'x'
202
203 Rcp_vs_Rsw_Plots(Rcp_fxn_Rsw, Rcp_apprx1_fxn_Rsw, ...
    Rcp_apprx2_fxn_Rsw, Rcp_apprx3_fxn_Rsw)
204 %Rcp_vs_Rsw_Plots2(Rcp_fxn_Rsw, Rcp_apprx3_fxn_Rsw)
205
206 % Creating a Table for Rcp_vs_Rsw
207 Rsw_val = linspace(10,500,491);
208 Rsw_val = [Rsw_val]';
209 Rcp_Rsw_val = vpa(subs(Rcp_fxn_Rsw, [Rsw], [Rsw_val]),64 );
210 digits(100);
211 Rcp_Rsw_val = double (Rcp_Rsw_val);
212 % Location & FileName for Tabulating Rcp_vs_Rsw
213 RcpTablename = '.....';
214 Rcp_vs_Rsw_Table = table(Rsw_val,Rcp_Rsw_val);
215 %writetable(Rcp_vs_Rsw_Table,RcpTablename,'Sheet',1)
216
217 %-----
218 %-----
219 % Observing Impact of Rsw+Cp on Rcp, Using a 2-D Plot
220
221 %var_Rsw_Cp = [CL Ton Tprd IL Vdd];
222 %var_val_Rsw_Cp = [(260*10^(-12)) (7.8*10^(-9)) (20*10^(-9)) ...
    (500*10^(-6)) (3.3)];
223
224 var_Rsw_Cp = [CL Ton Tprd Vdd];
225 var_val_Rsw_Cp = [(260*10^(-12)) (7.8*10^(-9)) (20*10^(-9)) (3.3)];
226
227 % Original Rcp expression in terms of Rsw+Cp
228 Rcp_fxn_Rsw_Cp = vpa(subs(Rcp_expr, [var_Rsw_Cp], ...
    [var_val_Rsw_Cp]),64 );
229
230 Rcp_3500_plane = 3500;
231
232 % Original 2-D Plot Function

```

```

233 %Rcp-vs-Cp-Rsw-Plot(Rcp_fxn_Rsw_Cp, Rcp_3500_plane)
234
235 syms Cp_pF;
236 % Original Rcp expression in terms of Rsw+Cp with Cp in pF
237 Rcp_fxn_Rsw_Cp_pF = vpa(subs(Rcp_expr, [var_Rsw_Cp Cp], ...
    [var_val_Rsw_Cp (Cp_pF*10^(-12))]),64 );
238
239 %Defining Rcp as a 2D-Fxn of Rsw, Cp:
240 %Rsw-> 1st Variable (x) Cp-> 2nd Variable (y)
241 Rcp_2D(Rsw,Cp_pF) = Rcp_fxn_Rsw_Cp_pF;
242
243 % Updated 2-D Plot Function
244 Rcp-vs-Cp-Rsw-Plot2(Rcp_2D, Rcp_3500_plane)

```

The output of this MATLAB code depicting variation of CP output impedance function and its closed-form approximations, with respect to CP design and operating parameters, is shown in Fig. 7.3 - 7.5.

Fig. 7.3: CP output impedance function versus switch resistance (R_{SW})

Fig. 7.4: CP output impedance function versus Pump capacitance (C_P)

Fig. 7.5: CP output impedance function versus $K[T_{ON}/T_{PRD}]$

Appendix II: Derivation and Analysis of Settling Time

This Appendix section provides the MATLAB code utilized for computational analysis and derivation of the complete settling profile for the proposed NVG system.

For the initial t_1 seconds, while the pass-transistor operates in saturation region, the dynamic state of the system can be described using a first-order differential equation. For this region, a closed-form expression of time instant t_1 and constant inrush current (I_{PT_SAT}) is derived, while a numerical value for the same is readily obtained by substituting the values of design and operating parameters.

In the following settling phase, the pass-transistor operates in linear region followed by a short transition state, in which the system rapidly acquires its final steady-state. The dynamic system is defined by a set of more involved differential-algebraic equations (DAE) which do not yield a closed form solution for the transient function of node voltage variables (CP output: $V_{CP}(t)$, Regulated output: $V_{REG}(t)$, Pass-transistor gate: $V_{G_PT}(t)$). The complete settling profile, including that in transition region, is thus obtained through a numerical solution of the given DAEs at varying time instants.

The given MATLAB code in a documented format, is presented as follows:

```
1 clear;
2 clc;
3
4 syms VREG VUNREG VG_PT VREG_required Vpos;
5 syms Ipt Ireg;
6 syms Vcp0 Rcp;
```

```

7 syms Vth_PT kn_PT WbyL_PT VGS_PT VDS_PT;
8 syms RL CL CL_CP Beta; % Beta: feedback Factor
9 %syms t;
10
11 % DEFINING VALUES OF ALL CONSTANT PARAMETERS
12 %-----
13 % Operating Parameters
14 Vreg_req = -3.0;
15 IL_req = 250*10^(-6);
16 Vref_val = -1.1;
17 Vpos_val = 0.0;
18 CL_val = 220*10^(-9);
19
20 Ireg_val = 22.977*10^(-6);
21
22 % II CP Linear Model Parameters
23 Vcp0_val = -4.88;
24 Rcp_val = 3900;
25
26 % III Pass-Transistor Parameters
27 kn_PT_val = 80*10^(-6);
28 WbyL_PT_val = 16.5;
29 Vth_PT_val = 0.8;
30
31 %-----
32
33 % Deriving Load resistance and Beta (required feedback ratio)
34
35 RL_val = (Vpos_val - Vreg_req)/(IL_req)
36
37 Beta = (Vpos_val - Vref_val)/(Vpos_val - Vreg_req)
38
39 %-----
40
41
42
43 % EQN-1
44 eqn1 = VGS_PT == Vpos - VUNREG;
45

```



```

46 % EQN-2
47 eqn2 = Ipt == 0.5*kn_PT*(WbyL_PT)*((VGS_PT - Vth_PT)^2);
48
49 % EQN-3
50 eqn3 = VUNREG == Vcp0 + (Ipt + Ireg)*Rcp;
51
52 sol_sat = solve([eqn1 eqn2 eqn3], [VUNREG VGS_PT Ipt]);
53
54
55 Ipt_expr = sol_sat.Ipt;
56 pretty (Ipt_expr)
57
58 Vunreg_sat_expr = sol_sat.VUNREG;
59
60
61
62 var1 = [kn_PT WbyL_PT Vth_PT Vcp0 Rcp Ireg RL CL Vpos];
63 var1_val = [kn_PT_val WbyL_PT_val Vth_PT_val Vcp0_val Rcp_val ...
              Ireg_val RL_val CL_val Vpos_val];
64
65 Ipt_sat_val_mA = 10^(3)* (vpa(subs(Ipt_expr, [var1], ...
              [var1_val]),64))
66 Vunreg_val = (vpa(subs(Vunreg_sat_expr, [var1], [var1_val]),64))
67
68
69 syms Vreg_sat(t) Ipt_sat;
70
71 % Diff Eqn for Current Balance on Pass-T
72 eqn4 = (Vreg_sat)/RL + CL*(diff(Vreg_sat,t)) == -1*Ipt_sat;
73
74 % Initial Condition for EQN-4
75 %cond4 = Vreg_sat(0) == 0; << -- INCORRECT !!
76 cond4 = Vreg_sat(0) == Vpos; %<< -- CORRECTED !
77
78 % Solving Diff_EQN-4 with Cond-4
79 Vreg_sat_expr(t) = dsolve(eqn4,cond4)
80
81 % From t=0s to t=t1, Pass-T is in saturation region
82 syms t1;

```

```

83 eqn5 = Vreg_sat_expr(t1) == Vpos - Vth_PT;
84
85 t1_expr = solve(eqn5,t1)
86
87 %var_t1 = [CL RL Vth_PT Ipt_sat];
88 %var_t1_val = [(470*10^(-9)) (16500) (0.65) ...
    (Ipt_sat_val_mA(1)*10^(-3))];
89
90 t1_val_us = 10^(6)* (vpa(subs(t1_expr, [var1 Ipt_sat], [var1_val ...
    (Ipt_sat_val_mA(1)*10^(-3))]),64))
91
92 % Vreg at t1: VR0: intial condition for next stage, w/i Pass-T ...
    in sat.
93 Vreg_at_t1_val = (vpa(subs(Vreg_sat_expr(t1), [var1 Ipt_sat t1], ...
    [var1_val (Ipt_sat_val_mA(1)*10^(-3)) (t1_val_us*10^(-6))]),64))
94
95
96 % Pass-T operating in Lineat Region from t=t1 to t=t2,
97 % t=t2, Vreg =Vreg_req, and Steady State is reached
98 % Total Settling Time = t1+t2
99
100 % Pass-T in Linear region
101
102 syms Vreg_lin(t) Vunreg_lin(t) Ron_PT(t) VG_PT(t) Ireg_lin(t);
103 syms VR0 VUNR0 Ipt0;
104 syms Ron_Adj; % Adjustment factor for Ron_PT(linear) to ensure ...
    Vunreg_lin(0) = Vunreg_sat && Vreg_lin(0)= Vreg_at_t1_val
105
106
107 % Nodal EQN at Drain of PT
108 % Vreg_lin_expr = -CL*(diff(Vreg_lin(t),t)) + ...
    -1*(Vreg_lin(t))/RL -1*(Vreg_lin(t) - Vunreg_lin)/(Ron_PT);
109
110 eqn6 = -CL*(diff(Vreg_lin(t),t)) + -1*(Vreg_lin(t))/RL ...
    -1*(Vreg_lin(t) - Vunreg_lin(t))/(Ron_PT(t)) == 0;
111
112
113 % Putting a reasonable numerical value for Vreg, to assess if ...
    the numerical solution for Vunreg_lin/Ron_PT/VG_PT is ...

```

```

    reasonable !!
114 Vreg_val = -0.65;
115
116
117 % Nodal Equation at the Source of Pass-T
118 %eqn7_expr = (Vunreg_lin - Vcp0)/Rcp + (Vunreg_lin - ...
    Vreg)/(Ron_PT) - Ireg;
119 %eqn7_num_expr = (vpa(subs(eqn7_expr, [var1 Vreg], [var1_val ...
    (Vreg_val)]),64));
120 %eqn7_num = eqn7_num_expr == 0
121
122 eqn7 = (Vunreg_lin(t) - Vcp0)/Rcp + (Vunreg_lin(t) - ...
    Vreg_lin(t))/(Ron_PT(t)) - Ireg_lin(t) == 0;
123
124 % Deriving OTA output using 'OTA_TFxn', assuming (VREF = -1.1) & ...
    (Beta=1/3)
125 %eqn8_expr = OTA_TFxn((Vreg/3), (-1.1), 0, Vunreg_lin, 400);
126 %eqn8_num_expr = (vpa(subs(eqn8_expr, [var1 Vreg], [var1_val ...
    (Vreg_val)]),64));
127 %eqn8_num = VG_PT - eqn8_num_expr == 0
128
129
130
131 eqn8 = VG_PT(t) == ...
    OTA_TFxn((Vreg_lin(t)*Beta+Vpos_val*(1-Beta)), (Vref_val), ...
    0.0, Vunreg_lin(t), 316.2277);
132
133 % Ron_PT equation with gate voltage VG_PT derived in eqn8 and ...
    VPOS=0V
134 %eqn9_expr = 1/(kn_PT * WbyL_PT * (VG_PT - Vunreg_lin - Vth_PT));
135 %eqn9_num_expr = (vpa(subs(eqn9_expr, [var1 Vreg], [var1_val ...
    (Vreg_val)]),64));
136 %eqn9_num = Ron_PT - eqn9_num_expr == 0;
137
138 eqn9 = Ron_PT(t) == 1/(kn_PT * WbyL_PT * (VG_PT(t) - ...
    Vunreg_lin(t) - Vth_PT));
139
140 % Writing a linear approxmiation of Ireg_lin(t)
141

```

```

142 %eqn10 = Ireg_lin(t) == (-22.83626*10^(-6))*Vunreg_lin(t) - ...
      (33.87091*10^(-6));
143 eqn10 = Ireg_lin(t) == (-16.9720*10^(-6))*Vunreg_lin(t) - ...
      (13.3462*10^(-6));
144
145 % Attempting to the Numerically solve the Given ...
      Differential-Algebraic Eqn
146 % definced above, using ODE15i Solver !!
147
148 dae_eqns = [eqn6, eqn7, eqn8, eqn9, eqn10]; % Given ...
      Differential-Algrebraic (DAE) Eqns
149
150 dae_vars = [Vreg_lin(t), Vunreg_lin(t), Ron_PT(t), VG_PT(t) ...
      Ireg_lin(t)]; % Defining set of variable (unknowns) for ...
      given DAE !!
151
152 f = daeFunction(dae_eqns, dae_vars, RL, CL, Vcp0, Rcp, kn_PT, ...
      WbyL_PT, Vth_PT);
153
154 % Defining Value of Parameters
155
156
157 F = @(t, Y, YP) f(t, Y, YP, RL_val, CL_val, Vcp0_val, Rcp_val, ...
      kn_PT_val, WbyL_PT_val, Vth_PT_val);
158
159 % Determining Consistent Initial condition for the Variable set ...
      (defined as
160 % 'y0') and their derivatives (defined as 'yp0')
161
162 y0est = [(-0.8); (-1.99); (975); (0); (22.974*10^(-6))]; % ...
      Estimated Initial condition for the variables
163 yp0est = zeros(5,1); % Estimated Initial condition for the ...
      Derivative of variables
164
165 [y0, yp0] = decic(F, 0, y0est, [], yp0est, []) % Deriving Actual ...
      Initial Condition using decic function !!
166
167
168 tspan = [0, (10*10^(-3))]; % Time Span: 0 to 10ms

```

```

169
170 DAE_SOL = ode15i(F, tspan, y0, yp0); % Deploying ODE15i solver ...
    for the given DAE !!
171
172 % Plotting the Numerical Solution using DEVAL
173 tres = linspace(0, (10*10^(-3)), 10^(5)); % Setting the ...
    Time-Domain Resolution: 100,000 point => 0.1us
174 Vreg_fxn_t = deval(DAE_SOL, tres, 1); % DEVAL is used to fin ...
    solution of any DE/DAE at given time points
175 Vunreg_fxn_t = deval(DAE_SOL, tres, 2);
176 VG_PT_fxn_t = deval(DAE_SOL, tres, 4);
177
178 % Plotting Results for Vreg_lin(t), Vunreg_lin(t) and VG_PT(t) :-
179 plot_dae(tres, Vreg_fxn_t, Vunreg_fxn_t, VG_PT_fxn_t);
180
181 % Giving (ultra) small increment to each Vreg_fxn_t(k) for ...
    'interp1' fxn to
182 % work properly
183 for k = 1:length(Vreg_fxn_t)
184 Vreg_fxn_t(k) = Vreg_fxn_t(k) + k*10^(-10);
185 end
186 t2_val_us = 10^(6)*interp1(Vreg_fxn_t, tres, Vreg_req)
187
188 VG_PT_val = interp1(Vreg_fxn_t, VG_PT_fxn_t, Vreg_req)
189
190 % Compile and Display Final Results
191 disp('Output Summary:')
192 Inrush_Current_mA = Ipt_sat_val_mA(1)
193 Vreg_at_t1_val
194 t1_val_us
195 t2_val_us
196 Total_Settling_us = t1_val_us + t2_val_us
197
198 Vreg_lin_est = y0(1)
199 Vunreg_lin_est = y0(2)
200 Ron_PT_est = y0(3)
201 VG_PT_est = y0(4)
202 Ireg_lin_est = y0(5)
203

```

```

204 %-----TABULATING ...
      RESULTS-----%
205
206 %-----PASS-T in ...
      SATURATION-----%
207
208 syms Vunreg_sat(t);
209
210 var2 = [Ipt_sat RL CL Vcp0 Rcp Ireg];
211 var2_val = [(Ipt_sat_val_mA(1)*(10^-3)) RL_val CL_val Vcp0_val ...
      Rcp_val Ireg_val];
212
213 Vunreg_sat(t) = Vcp0 + (Ipt_sat + Ireg)*Rcp;
214 Vunreg_sat_fxn_t = (vpa(subs(Vunreg_sat, [var2], [var2_val]),64));
215
216 Vreg_sat_fxn_t = (vpa(subs(Vreg_sat_expr, [var2], [var2_val]),64));
217
218 tsat_val = linspace(0,t1_val_us*(10^-6),500);
219 tsat_val = [tsat_val]';
220
221 Vunreg_sat_val = Vunreg_sat_fxn_t(tsat_val);
222 Vreg_sat_val = Vreg_sat_fxn_t(tsat_val);
223
224 digits(100);
225 tsat_val = double (tsat_val);
226 Vunreg_sat_val = double (Vunreg_sat_val);
227 Vreg_sat_val = double (Vreg_sat_val);
228
229 % Location & FileName for Tabulating
230 SettlingTime_Sauration_Tablename = '.....';
231
232 SettlingTime_Sauration_Table = table(tsat_val, Vunreg_sat_val, ...
      Vreg_sat_val);
233 %writetable(SettlingTime_Sauration_Table, ...
      SettlingTime_Sauration_Tablename,'Sheet',1)
234
235 %-----Tabulating Pass-T in Saturation: ...
      COMPLETE-----%
236

```

```

237 %-----Tabulating Pass-T in Linear ...
      Region-----%
238
239 tlin_val = linspace(0,2*t2_val_us*(10^-6),1000);
240 tlin_val = [tlin_val]';
241
242 Vreg_lin_val = deval(DAE_SOL,tlin_val,1);
243 Vreg_lin_val = [Vreg_lin_val]';
244 Vunreg_lin_val = deval(DAE_SOL,tlin_val,2);
245 Vunreg_lin_val = [Vunreg_lin_val]';
246
247
248 digits(100);
249 tlin_val = double (tlin_val);
250 Vunreg_lin_val = double (Vunreg_lin_val);
251 Vreg_lin_val = double (Vreg_lin_val);
252
253 % Location & FileName for Tabulating
254 SettlingTime_Linear_Tablename = '.....';
255
256 SettlingTime_Linear_Table = table(tlin_val, Vunreg_lin_val, ...
      Vreg_lin_val);
257 %writetable(SettlingTime_Linear_Table, ...
      SettlingTime_Linear_Tablename,'Sheet',1)
258
259 %-----Tabulating Pass-T in Linear: ...
      COMPLETE-----%

```

The error-amplifier OTA is modelled using the standard-logistic function, which is defined using the following code segment.

```

1  function Vota_op = OTA_TFxn (VP, VN, Vpos, Vneg, Av)
2
3  syms k x;
4  % Approximating OTA Response using Standard Logistic Fxn: which ...
      is a smooth
5  % saturation fxn.
6  f(x) = (Vneg / (1 + exp(k*x))) + (Vpos / (1 + exp(-k*x)));

```

Fig. 7.6: Numerical solution for settling transients in post-saturation region (V_{REG} : -3.0V, I_L : 250 μ A, V_{POS} : 0.0V, V_{REF} : -1.1V)

```

7
8 fderv(x) = diff(f(x),x);
9
10 %Equation derivative (f(x) at x=0 == OTA Gain == Av == gmRL == ...
    50dB (316.22677)
11 % 60dB (10^3). Using this to calculate k: steepness of the ...
    Logistic Fxn.
12 ic1 = fderv(0) == Av;
13
14 sol = solve(ic1, k);
15 kval = sol;
16
17
18 f2(x) = vpa(subs(f(x), [k], [kval]),64);
19
20 Vota_op = f2(VP - VN);
21
22 end

```

The settling profile at a standard operating point (V_{REG} : -3.0V, I_L : 250 μ A), obtained from the given MATLAB code, for the post saturation region operation, is shown in Fig. 7.6.