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Three-Dimensional Capacitor Embedded in Fully Cu-Filled Through-Silicon Via and Its Thermo-Mechanical Reliability for Power Delivery Applications

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Abstract— This paper demonstrates the successful integration of three-dimensional (3-D) metal-insulator-metal (MIM) capacitors embedded in fully-filled Cu TSVs with diameter of 10 and 20 μm . Their thermo-mechanical reliability has been studied with both physical characterizations and electrical characterizations. The structures of D10 and D20 test vehicles remain intact after through-silicon via (TSV) Cu filling. However, it is found in TEM images that both peaks of Si scallops and the Al_2O_3 dielectric layer in MIM capacitor were impaired for D30 test vehicle. The leakage current density of MIM capacitors is 4.0×10^{-9} , 4.1×10^{-8} , 1.1×10^{-6} , and 7.4×10^{-1} A/cm^2 for D00, D10, D20, and D30 test vehicles, respectively. The results support the evidence from transmission electron microscopy (TEM), showing that the Al_2O_3 dielectric layer in the MIM capacitor is indeed impaired and loses its insulating property. Ultrahigh capacitance density is obtained as 6,547.1 nF/mm^2 and 7,091.7 nF/mm^2 for D10 and D20 test vehicles, respectively. Furthermore, some simulation work has been carried out to showcase its application as decoupling capacitor in a power delivery network (PDN). The inserted 3-D MIM capacitor helps to keep the target impedance below 2.5 Ω over a wide range of 0-5 GHz for an applied specific integrated circuit-high bandwidth memory (ASIC-HBM) system. And the voltage fluctuation is also reduced from ~ 3.0 to ~ 1.0 V by as much as $\sim 66.7\%$.

Keywords—3D IC; TSV; 3D MIM capacitor; capacitance density

I. INTRODUCTION

Scaling of passive devices, such as on-chip capacitor, is of great interest to the electronics packaging community. A novel approach to integrate on-chip capacitors has been proposed and demonstrated by the authors [1], [2]. This approach leverages on the existing through-silicon via (TSV) trenches to reduce the Si area consumption of three-dimensional metal-insulator-metal (3-D MIM) capacitors by more than 90%, compared with the area occupied by conventional trench capacitors [3]–[6]. However, those test vehicles were previously fabricated and characterized prior to the filling of the Cu core due to insufficient process equipment at that time. Therefore, the impact of thermo-mechanical stress exerted by the Cu core on those devices was not clear.

Fig. 1. The proposed 3-D MIM capacitor embedded in TSV. The top surface area is thus “freed-up” because the conventional trench capacitors are embedded in the trenches of existing TSVs.

In this work, the 3-D MIM capacitors have been successfully integrated with fully Cu-filled TSVs and the impact of thermo-mechanical stress is explored for the reliability of the devices. The test vehicles with diameter of 10 and 20 μm are intact in structural integrity after TSV Cu filling process. However, under transmission electron microscopy (TEM), it is found that the Al_2O_3 dielectric layer, in the test vehicle with 30 μm , is impaired over the peaks of Si scallops. Additionally, some peaks of Si scallops are also found damaged for the first time, different from previous findings in stress-induced defects in TSV liner alone [7]. At a bias of 1.5 V, the leakage current density is 4.1×10^{-8} , 1.1×10^{-6} , and 7.4×10^{-1} A/cm^2 for the test vehicles with trench diameters of 10, 20, and 30 μm , respectively. Among the three results, the ultrahigh leakage current of the last test vehicle suggests that the Al_2O_3 dielectric layer in 3-D MIM capacitor does not preserve the insulating property due to the high thermo-mechanical stress. A record high capacitance density of up to 7,091.7 nF/mm^2 has been achieved. Furthermore, some simulation work has been done to showcase its application as decoupling capacitor for power delivery network (PDN). The result shows the target impedance is kept below 2 Ω over a wide range of 0-5 GHz and the fluctuation of power supply voltage is reduced from ~ 3.0 to ~ 1.0 V for a target system with applied

specific integrated circuit (ASIC) and high bandwidth memory (HBM).

II. EXPERIMENTAL

Four test vehicles were designed and fabricated on the same wafer to study the integration feasibility of 3-D MIM capacitors embedded in TSVs and the impact of thermo-mechanical stress on their electrical performance. They include a planar MIM test vehicle as benchmark named as “D00” and three 3-D device test vehicles with diameters of 10, 20, and 30 μm named as “D10”, “D20”, and “D30”, respectively. A brief process flow with images taken from key steps is shown in Fig. 2.

Fig. 2. A brief process flow of 3-D MIM capacitor embedded in TSV. The images on the left are shown for key steps.

Firstly, an 8-inch *p*-type Si wafer was deposited with 200 nm SiO_2 as hard mask layer for deep trench etching. Then, it was patterned with photoresist and trenches with 10, 20, and 30 μm were formed by deep reactive ion etching (DRIE) with a target depth of 100 μm as shown in the step “trench formation”. The depth of trenches increases as the diameter increases from 10 to 30 μm due to the well-known microloading effect. Next, a 120 nm SiO_2 insulation layer was deposited by chemical vapor deposition (CVD) to keep the electrodes of capacitors electrically insulated from Si substrate. After that, MIM layers (50 nm TiN/10 nm Al_2O_3 /50 nm TiN) were deposited sequentially by atomic layer deposition to ensure their excellent step coverage as shown in the step “ALD MIM layers”. It was followed by conventional TSV fabrication steps: (a) TSV liner deposited by CVD; (b) Ti diffusion barrier layer/Cu seed layer deposited by physical vapor deposition (PVD); (c) Cu electroplating to fill up the trench; (d) annealing and chemical-mechanical polishing (CMP) to remove the Cu overburden as shown in the step “Anneal and CMP”. Finally, contact pads on top were patterned for electrical characterization. The finished wafer is shown in the last step “pad formation”. These process steps proposed and demonstrated are designed for the test vehicles in this study to be probed from the top side for both physical and electrical characterizations. The complete integration requires further process at the backside of the wafer. The depth of trenches with different diameters will all eventually be reduced to the thickness of the final Si substrate when the backside grinding step removes the excessive Si substrate and exposes all the bottom parts of the trenches. It is assumed that the backside integration process will have negligible impact on the device performance of the test vehicles.

Previously, researchers have found that the coefficient of thermal expansion (CTE) mismatch of Cu and Si could lead to built-up stress during TSV process and therefore cause cracks in SiO_2 TSV liner [7], [8]. Thus, it is important to study the impact on this device embedded in TSV with cross-sectional samples prepared by focused ion beam (FIB). After the whole process, TEM images were taken on the cross-sections near the MIM region to examine their structural integrity with TSV Cu core filling. In this case, no crack in TSV liners was seen for all three test vehicles. However, for the first time, some damaged peaks of Si scallops were observed for D30 test vehicle, which is most probably due to the process-induced thermo-mechanical stress. The comparison between the Si scallops in D10 and D30 is shown in Fig. 3. Since the D10 and D30 trenches were etched on the same wafer, the Si scallops developed during DRIE process should have similar cycles and shapes. Nevertheless, the D10 Si scallops shown in Fig. 3(a) were well preserved, whereas the D30 Si scallops shown in Fig. 3(b) were deformed at the peaks.

Fig. 3. Comparison between Si scallops in (a) D10 test vehicle and (b) D30 test vehicle.

With a closer look at the stacked MIM layers, they remain intact for those in D10 and D20 test vehicles, but not for the one in D30 test vehicle. As shown in Fig. 4, the Al_2O_3 dielectric layer becomes impaired over the peaks of Si scallop as featured with yellow-dotted boxes. It suggests that the stress level is too high for 3-D MIM layers in a TSV trenches with diameter greater than $30\ \mu\text{m}$. Therefore, its insulating property could be compromised.

Fig. 4. A TEM image on the cross-sectional MIM layers in a D30 test vehicle.

III. ELECTRICAL CHARACTERIZATION RESULTS

The electrical characterization results of Current-Voltage (I - V) and Capacitance-Voltage (C - V) imply the impact of thermo-mechanical stress on the electrical performance of test vehicles. The condition for I - V characterizations is set as DC voltage sweep from 0 V to 3.0 V, whereas the condition for C - V characterizations is set as 30 mV AC voltage sweep from -3.0 V to 3.0 V at 100 kHz.

To fairly assess the insulating properties of 3-D MIM capacitors, the I - V measurement results have been normalized to Current Density-Voltage (J - V) results with respect to their physical surface area for all four test vehicles as plotted in Fig. 5. The leakage current density at 1.5 V becomes higher as the trench diameter of the test vehicles increases from 10, 20, to $30\ \mu\text{m}$: 4.1×10^{-8} , 1.1×10^{-6} , and $7.4 \times 10^{-1}\ \text{A/cm}^2$. The results support the observation of impaired Al_2O_3 dielectric layer in D30 test vehicle, as its leakage current density of $7.4 \times 10^{-1}\ \text{A/cm}^2$ is many orders higher than that of benchmark planar D00 test vehicle $4.0 \times 10^{-9}\ \text{A/cm}^2$ at the bias of 1.5 V. The significant increases in leakage current density for all three test vehicles are in contrast to those results from early prototypes without TSV filling, where the difference in leakage current density is negligible for all test vehicles [2]. Therefore, the impact of process-induced thermo-mechanical stress on leakage current density should not be ignored and needs to be carefully managed. The integration of 3-D MIM capacitor with D30 test vehicle is proven not feasible, if the residual stress cannot be mitigated.

Fig. 5. Normalized J - V results with bias from 0 V to 3 V.

For C - V characterization results, the one from D30 should be eliminated because of its leaky dielectric layer, whereas D10 and D20 show stable response to voltage sweeping for the operation voltage ranging from -3.0 to 3.0 V. As shown in Fig. 6, at bias of 0 V, the capacitance is 592.7 pF for D00 test vehicle, 630.0 pF for D10 test vehicle, and 669.8 pF for D20 test vehicle. The capacitance contributed from 3-D MIM capacitor alone can be calculated by subtraction from that of the benchmark planar capacitor: 37.3 pF for D10 test vehicle and 77.1 pF for D20 test vehicle. Therefore, a record high

capacitance density of 6,547.1 nF/mm² is obtained for D10 test vehicle and 7,091.7 nF/mm² for D20 test vehicle. Thus, D10 and D20 test vehicles have demonstrated the integration feasibility of 3-D MIM capacitors embedded in fully-fill Cu TSVs.

Fig. 6. C - V measurement results at 100 kHz with bias from -3 V to 3 V.

IV. APPLICATION FOR POWER DELIVERY NETWORK

Rejection of noise in power supply of VLSI circuit becomes more challenging due to the shrinking chip area, increased circuit density, lower operating supply voltage, and demand for faster communication link [6], [9]–[13]. The illustration of poorly regulated power supply in PDN due to switching noise is shown in Fig. 7. To improve the power-supply noise immunity, decoupling capacitors are usually inserted between the supply rails to filter out the surging noise spikes.

Fig. 7. Illustration of poorly regulated power supply in PDN due to switching noise.

In this work, a specific high-speed digital system with ASIC-HBM is targeted as shown in Fig. 8 [8]. The top view and cross-sectional view of the PDN for an ASIC-HBM system are seen in Fig. 8(a) and (b), respectively. The network includes G-S-G lines, VSS lines, and ground shield. Due to the proximity of VSS lines to the G-S-G lines, the crosstalk between them could endanger the power integrity. 3-D MIM capacitor embedded in TSV could be considered as a good candidate for effective noise decoupling with extremely high capacitance

density. Since the capacitors are built around the existing TSVs, they can be readily integrated with 2.5-D interposer/3-D integrated circuits (ICs) with negligible footprint penalty. Thus, the proposed solution with this new technology is introduced and illustrated in Fig. 8(c).

Fig. 8. Power integrity and signal integrity cluster of ASIC-HBM with 3-D MIM capacitor as decoupling capacitor for power delivery network. (a) One-cluster of ASIC-HBM interconnects. (b) Cross-section view of the G-S-G lines, VSS, and shield-ground. (c) The proposed solution to use 3-D MIM capacitor embedded in the existing TSVs to improve the power integrity of the ASIC-HBM system.

With the contribution of 100 pF from the new capacitor, the system impedance is well kept below a specific threshold value of 2.5 Ω for this system across a wideband frequency range of 0–5 GHz as shown in Fig. 9. At the same time, Fig. 10 shows the transient response of the VSS fluctuation, due to 3dB coupling of 10 Gbps of high-speed digital signal into the VSS lines, can be largely reduced from ~3.0 to ~1.0 V by as much as ~66.7%. These results demonstrate the effectiveness of inserting 3-D MIM capacitors into PDN as decoupling capacitors for 2.5 D interposer/3-D ICs.

Fig. 9. VSS impedance of ASIC-HBM cluster interconnects before and after the implementation of 3-D MIM capacitor around the TSV. The system impedance is well kept below a specific threshold value of 2.5 Ω for this system across a wideband frequency range of 0–5 GHz

Fig. 10. VSS fluctuations at 10Gbps with high-speed digital signal coupled to VSS. The transient response of the VSS fluctuation, due to 3dB coupling of 10 Gbps of high-speed digital signal into the VSS lines, can be largely reduced from ~ 3.0 to ~ 1.0 V by as much as $\sim 66.7\%$.

V. CONCLUSION

This paper demonstrates the successful integration of 3-D MIM capacitor embedded in fully-filled Cu TSV with diameter of 10 and 20 μm . The impact of process-induced thermo-mechanical stress has been studied with both physical characterizations and electrical characterizations. The structure integrity of D10 and D20 test vehicles as well kept with full-filled Cu TSVs. However, it is found in TEM images that both peaks of Si scallops and the dielectric layer in MIM capacitor were damaged due to high stress level for D30 test vehicle. The leakage current density of MIM capacitors in D10 and D20 test vehicles gradually increases to 4.1×10^{-8} and 1.1×10^{-6} A/cm², compared with that of the benchmark 4.0×10^{-9} A/cm². On the other hand, the greatly increased leakage current density of 7.4×10^{-1} A/cm² for D30 test vehicle supports the evidence from TEM, showing that the Al₂O₃ dielectric layer in the MIM capacitor is indeed impaired and loses its insulating property. Then, ultrahigh capacitance density is obtained to be 6,547.1 and 7,091.7 nF/mm² for D10 and D20 test vehicles, respectively. Lastly, simulations were carried out to showcase its application as decoupling capacitor in a PDN. The inserted capacitor helps to keep the target impedance below 2.5 Ω over a wide range of

0–5 GHz for a specific ASIC-HBM system. And the voltage fluctuation is also reduced from ~ 3.0 to ~ 1.0 V by as much as $\sim 66.7\%$.

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REFERENCE

- [1] Y. Lin and C. S. Tan, "Physical and Electrical Characterization of 3D Embedded Capacitor: A High-Density MIM Capacitor Embedded in TSV," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, 2017, pp. 1956–1961.
- [2] Y. Lin and C. S. Tan, "Modeling, Fabrication, and Characterization of 3-D Capacitor Embedded in Through-Silicon Via," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 8, no. 9, pp. 1524–1532, Sep. 2018.
- [3] J. H. Klootwijk *et al.*, "Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 740–742, Jul. 2008.
- [4] F. Roozeboom *et al.*, "ALD Options for Si-integrated Ultrahigh-density Decoupling Capacitors in Pore and Trench Designs," in *ECS Transactions*, 2007, vol. 3, pp. 173–181.
- [5] P. Banerjee, I. Perez, L. Henn-Lecordier, S. B. Lee, and G. W. Rubloff, "Nanotubular metal–insulator–metal capacitor arrays for energy storage," *Nat. Nanotechnol.*, vol. 4, no. 5, pp. 292–296, May 2009.
- [6] O. Guiller, S. Joblot, Y. Lamy, A. Farcy, E. Defay, and K. Dieng, "Through Silicon Capacitor co-integrated with TSV as an efficient 3D decoupling capacitor solution for power management on silicon interposer," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 1296–1302.
- [7] T. Nakamura, H. Kitada, Y. Mizushima, N. Maeda, K. Fujimoto, and T. Ohba, "Comparative study of side-wall roughness effects on leakage currents in through-silicon via interconnects," in *2011 IEEE International 3D Systems Integration Conference (3DIC)*, 2011 *IEEE International*, 2012, pp. 1–4.
- [8] K. H. Lu, Xuefeng Zhang, S.-K. Ryu, J. Im, Rui Huang, and P. S. Ho, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," in *2009 59th Electronic Components and Technology Conference*, 2009, pp. 630–634.
- [9] J. Cho, Y. Kim, J. Kim, V. Sundaram, and R. Tummala, "Analysis of glass interposer PDN and proposal of PDN resonance suppression methods," in *2013 IEEE International 3D Systems Integration Conference (3DIC)*, 2013, pp. 1–5.
- [10] K. Kikuchi *et al.*, "Low-impedance evaluation of power distribution network for decoupling capacitor embedded interposers of 3-D integrated LSI system," in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, 2010, pp. 1455–1460.

- [11] C. H. Aw, L. C. Quek, and H. C. Shu, "Silicon level circuit implementation for system-on-chip power integrity improvement," in *2015 International Conference on Electronic Packaging and iMAPS All Asia Conference (ICEP-IAAC)*, 2015, pp. 748–751.
- [12] X. Meng and R. Saleh, "Active decap design considerations for optimal supply noise reduction," in *2009 10th International Symposium on Quality Electronic Design*, 2009, pp. 765–769.
- [13] S. M. Vazgen *et al.*, "Power Supply Noise Rejection Improvement Method in Modern VLSI Design," in *2019 IEEE East-West Design & Test Symposium (EWDTS)*, 2019, pp. 1–4.