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2019

Khanna, D., Boon, C. C., Choi, P., Siek, L., Liu, B., & Li, C. (2019). A low-noise, positive-input, negative-output voltage generator for low-to-moderate driving capacity applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(9), 3423-3436.
doi:10.1109/TCSI.2019.2927117

<https://hdl.handle.net/10356/144145>

<https://doi.org/10.1109/TCSI.2019.2927117>

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A Low-Noise, Positive-Input, Negative-Output Voltage Generator for Low-to-Moderate Driving Capacity Applications

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Abstract—In this paper, a generic, low-noise, negative-voltage generator with wide tuning range and moderate driving capacity is presented. The highly integrated solution, incorporating a fully-integrated charge-pump and a regulator block, requires only one off-chip capacitor that can be shared with the supply decoupling capacitors. The fully integrated charge-pump operation is analyzed quantitatively, and a closed-form expression of its output impedance is derived. Powered from a single 3.3-V dc input, the output has a tuning range from -4.4 to $+2.1$ V for biasing applications, while the design supports a maximum load current of 250, 550, and 800 μ A for the regulated output voltage at -3.0 , -1.5 , and 1.5 V, respectively. The measured steady-state ripple is under 3 mV_{pp}, while the noise voltage at the charge-pump operating frequency harmonics is below 130 μ V_{rms} and the noise floor is under 5 μ V_{rms}. The design is also the application verified with a gallium nitride power amplifier, thus further confirming its low-noise performance. Implemented in CMOS 180-nm process, the prototype chip occupies an area of 0.55 mm².

Index Terms—Fully-integrated charge-pump, regulated negative voltage generator, gallium nitride (GaN) power amplifier (PA) biasing, low-noise output, inverted low-dropout regulator.

I. INTRODUCTION

NEGATIVE voltage supply has been traditionally employed to implement low-voltage source-side erase operation in flash-EEPROM memories [1], [2], and biasing of III-V depletion mode devices for circuits such as Gallium Nitride (GaN) based RF power amplifier [3]–[5]. In recent times, the potential of negative voltage input has been

Fig. 1. Negative voltage existing and emerging application landscape.

explored for several upcoming applications, such as biphasic tissue stimulation [6], [7], static-leakage reduction [8] and high-performance oscillators [9], [10]. In Fig. 1 an overview of the existing and emerging applications of negative voltage, over multiple circuit design domains is presented. The specification and performance of the regulated negative voltage output is primarily dictated by its end application. For instance, in [7], negative voltage is employed for the constant current stimulation of high-impedance electrode-tissue junction, typically requiring high voltage magnitude and driving capacity in hundreds of micro-amperes. In contrast, application such as [5], [10] require precision negative voltage biasing and the emphasis is on wide tuning-range and low output ripple with high spectral purity. In this work, a generic negative voltage generator system, that can cater to a wide range of applications and is suitable from an integration prospective, is presented.

In a typical negative voltage generator, the charge-pump (CP) output is characterized with high output impedance, large steady-state ripple and high noise content, and therefore requires some form of post-regulation, before it can be utilized for multiple applications. In this regard, the regulation techniques that have been proposed earlier [2], [6] operate by directly conditioning the CP operation to limit its output noise and ripple. In [6], the CP is operated within a digital feedback loop, such that its output is bounded within a comparator's hysteresis range. This technique is effective

Manuscript received March 15, 2019; revised June 10, 2019; accepted June 26, 2019. This work was supported by the National Research Foundation, Prime Minister's Office, Singapore, through the Campus for Research Excellence and Technological Enterprise (CREATE) Programme. This paper was recommended by Associate Editor F. M. Neri. (Corresponding author: Devrishi Khanna.)

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Digital Object Identifier 10.1109/TCSI.2019.2927117

Fig. 2. Functional diagram of proposed negative voltage generator system.

only at low-load currents, since the system reduces to having ‘no-regulation’ as load is increased. Moreover, it is essential that the oscillator frequency remains accurately matched to the given loading condition. In [2], a high gain analog feedback loop adjusts the total current injected into the CP such that its output is maintained at two zener voltage drops below the external reference input. Since the CP noise increases proportionally with the injected current, the technique involves an inherent trade-off between the noise content and the maximum supported load current. Moreover, it relies heavily on the CP output impedance (R_{CP}) and the breakdown voltages of zener diodes, and is therefore highly sensitive to process, voltage and temperature variations. The commercially available negative voltage generator solutions [11], [12] can support high drive currents, however require multiple off-chip components, including capacitors and ferrite beads, to achieve the required driving capacity and noise performance.

This work presents a generic negative voltage generator system with regulated low-noise output, low-output impedance and wide tuning-range, while requiring only one off-chip capacitor. The design supports drive currents from $250\mu\text{A}$ to $800\mu\text{A}$ for regulated output between -3.0V to 1.5V . The organization of this paper is as follows. In section II, the design is introduced from the top level and design methodology is presented. In section III, circuit level implementation of the CP and regulator are elaborated. In the following sections, system level analysis and verification are presented, and key design aspects are highlighted. Finally, measurement results from the prototype chip are presented and a conclusion is drawn.

II. NEGATIVE VOLTAGE GENERATOR ARCHITECTURE

A. Proposed Negative Voltage Generator

The functional diagram of the proposed negative voltage generator system is as depicted in Fig. 2. In this design, a fully integrated CP with a relatively high output impedance (R_{CP} : $3\text{k}\Omega$ to $5\text{k}\Omega$), is used to power the regulator sub-circuit. The positive rail of the regulator block is shared with the nominal 3.3V supply input, while its negative supply rail is connected to the output of the CP. The unregulated output of the negative voltage CP thus serves both as power source and input to the pass-transistor, to obtain tunable, low noise output. The CP output being the most negative potential of the entire circuit, all the current from the regulator module and output load sinks into this node.

The given design derives its integration advantage and superior low noise performance through the adaption of a fully integrated CP structure. This is because, the ac rejection offered by the given regulator circuit at typically high switching frequencies (30MHz to 300MHz) employed by the fully-integrated CPs, is 50dB to 90dB higher than that obtained at low frequencies (100kHz to 900kHz) utilized by CPs employing external capacitors. Since the CP ripple is mostly centered around the switching frequency and its harmonics, the given topology results in low noise output with moderate driving capacity. Moreover, the choice of CP implies that the overall design utilizes only one off-chip capacitor, which can be shared with the supply decoupling capacitor, thus leading to a high degree of integration for the overall system.

B. Design Methodology

The systematic design procedure adapted for the negative voltage generator system design involves proceeding along the following steps, (i) sizing of pass-transistor and estimation of CP’s required output impedance (ii) design and optimization of negative voltage CP (iii) circuit level implementation of regulator sub-circuits including bias generator and error amplifier (iv) utilization of CP’s linear model to verify regulator loop stability, ac rejection and transient response, and lastly (v) system level verification through transient co-simulation of CP and regulator modules.

For an initial design specification of $200\mu\text{A}$ of minimum supported load current (I_{LOAD_MIN}) for a regulated output greater than -3.0V (V_{REG_MIN}), the pass-transistor is sized to operate in saturation region with a dropout voltage (V_{DO}) of 0.6V , as shown in (1).

$$(W/L)_{PT} = \frac{2I_{LOAD_MIN}}{k'_n(V_{DO})^2} \quad (1)$$

Assuming an additional 0.4V design-margin, the required CP output (V_{CP_REQ}) for the minimum load current is thus estimated to be 1V below the minimum regulated output. The CP output (V_{CP}) at a given load current can be extrapolated using a simplified linear model, as expressed in (2).

$$V_{CP} = V_{CP_0} + I_{TOTAL}R_{CP} \quad (2)$$

where V_{CP_0} is the CP output at no load condition, R_{CP} is the CP output impedance, assumed to be constant with the increasing load current (I_L), and I_{TOTAL} , representing the

Fig. 3. (a) Multi-phase clock generator with clock buffer and (b) 4-phase switching output.

total current injected into the CP, is the sum of load current and current consumed by the regulator module (I_{REG}). The presumed linear characteristic of the CP is well established through a quantitative analysis and further verified through simulations and measurement results.

For a switched-capacitor CP implementation, the term V_{CP_0} can be approximated in terms of number of inverting stages (N), switching amplitude (V_{DD}) and the loss factor (γ), as given by (3).

$$V_{CP_0} = -(N \cdot V_{DD} \cdot \gamma) \quad (3)$$

By equating the required CP output to its linear model expression in (2), and using (3), a first-hand approximation for the R_{CP} magnitude is derived in (4).

$$R_{CP} = \frac{(N \cdot V_{DD} \cdot \gamma) - |V_{CP_REQ}|}{I_L + I_{REG}} \quad (4)$$

The optimum N can be estimated using (5) or (6), obtained by extending the analysis for boosted charge-pumps ($V_{OUT} > V_{IN}$) in [13], [14] to the inverting charge-pump for this implementation.

$$N_{Eff_opt} = \frac{|V_{CP_REQ}|}{V_{DD}} \left(1 + \sqrt{\frac{\alpha}{1-\alpha}} \right) \quad (5)$$

$$N_{Area_opt} = \frac{2|V_{CP_REQ}|}{V_{DD}} \quad (6)$$

where N_{Eff_opt} and N_{Area_opt} are the estimated number of CP inverting stages for maximum efficiency and minimum area implementation respectively. The term α is technology dependent parameter representing the ratio of pumping capacitance (C_P) to parasitic capacitance (C_{PAR}) and varies from 0.1 to 0.5. For the given specification with required CP output (V_{CP_REQ}) at $-4V$ and input supply at $3.3V$, N_{Area_opt} is 2.4 while N_{Eff_opt} varies from 1.6 to 2.4, thus suggesting an either 2 or 3-stage CP implementation.

As inferred from (4), a 3-stage CP implementation can significantly relax the requirement for CP output impedance. However, in order to limit the stress exerted on the pass-transistor at low-load currents, in this work a 2-stage CP is adopted. Thus, with N set at 2, loss factor (γ) varying between 0.72 to 0.76 and typical regulator current (I_{REG}) assumed constant at $50\mu A$ the required R_{CP} is estimated to be in the range of $3.0k\Omega$ to $4.1k\Omega$.

This analysis is followed by the design of a fully-integrated CP, which involves derivation of a frequency dependent CP linear model. The extracted model is inserted into the regulator simulation setup for an accurate prediction of the system level functionality, including the loop stability, small signal rejection and settling characteristics.

III. CIRCUIT LEVEL IMPLEMENTATION

A. Multiphase Clock Generator

The multiphase clock generator in [6], is re-used here to derive the 4-phase switching inputs for the CP, as shown in Fig. 3(b). The clock generator, as depicted in Fig. 3(a), comprises of one primary and two secondary cells, each of which split the input signal into two out-of-phase non-overlapping outputs. The unit cell consists of a crossed nand latch with added delay elements. This configuration results in varying path delay in the transmission of logic 0 and 1 and thus generates the required time lag between the consecutive switching transitions at its output. The resulting time lapse introduced between any two switching edges help to minimize the shoot-through current in the buffer stages.

A three stage, fanout of 4 (FO4) based clock buffer sizing is adopted to drive the large capacitive loads within the CP with minimum delay. The sizing of each buffer chain is based on its respective capacitive loading and is adjusted to maintain comparable rise/fall times for all four switching inputs.

B. Negative Voltage Charge-Pump

The negative voltage CP utilizes multiphase periodic signals to generate unregulated negative voltage output. In this work, a switched-capacitor based fully-integrated CP architecture is adopted. This inductorless design choice alleviates any EMI radiation concerns and results in significantly smaller silicon footprint, thus making integration of the CP feasible.

The two well-known fully-integrated CP architectures are the cross-coupled pair [7], [15] and the bootstrap CP [1], [6]. Although the cross-coupled topology utilizes a simpler 2-phase clocking scheme and can deliver lower output impedance per unit pump capacitance; however, it cannot be readily extended to multiple stages due to an increase in threshold voltage (V_T) of the pmos devices due to the body-effect. This, results in a

Fig. 4. 2-Stage negative voltage bootstrap charge-pump.

higher output impedance and degraded efficiency as number of stages are increased. In contrast, the bootstrap CP utilizing deep-n-well devices does not suffer from ‘ V_T ’ degradation along the cascaded stages. This work therefore utilizes the latter, such that the design principle is retained for lower supply voltages, requiring higher number of inverting stages.

The 2-stage bootstrap CP used in this work, is as shown in Fig. 4. The charge-pump operates by restricting the flow of negative charge in one-direction before its deposited on the load capacitor. With reference to 4-phase switching signals depicted in Fig. 3(b), the rising edge of CLK 2A turns on the boot-strap switches SW-1B and SW-3B, and causes their corresponding charge-transfer switches SW-1A and SW-3A to turn off. This is followed by a falling edge of CLK 1A, which pulls down node voltage V_1 and turns off switch SW-2B. Finally, negative charge is shared across nodes 1 and 2 by turning on SW-2A via CLK 1B. In the next phase of the same period SW-1A and SW-3A conduct, while SW-2A remains turned off, thus maintaining the direction of negative charge-transfer towards the output node. Consequently, the average node voltage magnitude is boosted as charge is pumped across each inverting stage.

The CP output magnitude can thus be boosted further by incorporating a higher number of inverting states. Assuming same pump capacitance per stage, a higher number of inverting generally results in enhanced CP efficiency, however this comes at the cost of increased switching losses, larger area utilization and higher device stress.

C. Charge-Pump Output Impedance

In past, the switched-capacitor CP operation has been rigorously analyzed [13], [14], [16] to achieve an optimized implementation in terms of minimizing area and maximizing efficiency. However, in these analyses, the charge-transfer itself is considered ideal and the non-idealities of its operation are captured through the parasitic capacitance on the top/bottom plate of pump capacitor (C_P). This results in a rather imprecise prediction of CP impedance ($R_{CP} \approx N/(F_{IN} C_P)$) and resulting deductions such as considering CP power consumption independent of operating frequency. Furthermore, the inaccuracies become more prominent as switching frequencies are increased. In this work, a CP

Fig. 5. Charge-pump's node voltage transitions in steady-state.

analysis incorporating the effect of non-zero switch resistance and finite on-time of switches, is presented.

The CP operation is analyzed quantitatively by means of its equivalent functional model, depicted in Fig. 2. In this simplified model, the large charge-transfer devices are replaced by a combination of an ideal switch and fixed resistance (R_{SW}). A small parasitic capacitance (C_{PAR}) is added to the gate capacitor (C_G), to represent the actual loss of charge occurring at the switching instants at nodes V_1 and V_2 . The effect of CLK 1B and CLK 2B inputs on node voltages due to capacitive coupling, is neglected since the (C_G) is an order of magnitude less than the pump capacitor (C_P).

The CP's critical design parameters are identified as the switch resistance (R_{SW}), pump capacitance per stage (C_P), and the load capacitor (C_L). In addition, the operating parameters include the load current (I_L) injected into the CP, time-period (T_{PRD}) of the input periodic signal and the on-time (T_{ON}), which is the time for which each of the charge-transfer device is turned on within one period.

The CP characteristics are derived by relating the node voltages V_1 , V_2 and V_{CP} , at the switching instants of CLK 1A and CLK 2A, and after each charge transfer phase is completed. For a given load current, once the steady state has been attained, the typical node voltage transitions are as shown in Fig. 5. The suffix ‘H’ and ‘L’ represent the node voltages being pulled high or low in response to the respective switching signal transition, and suffix ‘(i)’ and ‘(f)’ represent the initial and final value of the node voltages before and after the completion of the charge transfer phase.

The instantaneous change in the node voltage magnitude at the rising/falling edges of CLK 1A or CLK 2A can be represented using (7) and (8).

$$\text{Rising Edge: } V_{nH(i)} = V_{nL(f)} + V_{DD} \cdot \gamma \quad (7)$$

$$\text{Falling Edge: } V_{nL(i)} = V_{nH(f)} - V_{DD} \cdot \gamma \quad (8)$$

$$\text{where, } \gamma = \frac{C_P}{C_P + C_G + C_{PAR}} \quad (9)$$

The terms V_n represent node voltages V_1 and V_2 , V_{DD} is the input switching amplitude and the factor γ , as given by (9), models the loss of charge due to the gate and parasitic capacitance.

The charge-transfer equations correspond to each time a charge-transfer device is turned on and are derived by solving the resulting RC capacitive charge transfer equations with the known initial conditions. The effect of C_G and C_{PAR} on the charge-sharing is not considered due to their significantly smaller magnitude relative to the C_P .

With reference to Fig. 2 and Fig. 5, switch SW-1A is turned on in the positive phase of CLK 1A, causing the node voltage V_{1H} to decay towards ground potential. The corresponding initial and final node voltage magnitude can be related as in (10).

$$V_{1H(f)} = V_{1H(i)} \cdot \exp\left(\frac{-T_{ON}}{2R_{SW}C_P}\right) \quad (10)$$

Similarly, the charges are shared across nodes 1 and 2, while the switch SW-2A is being turned on. The resulting charge-transfer equation relating the node voltages V_{1L} and V_{2H} , are described using (11) - (12).

$$V_{1L(f)} = \frac{IC_{12} - (C_P \cdot (V_{2H(i)} - V_{1L(i)})) \cdot \exp\left(\frac{-2T_{ON}}{R_{SW}C_P}\right)}{2C_P} \quad (11)$$

$$V_{2H(f)} = \frac{IC_{12} + (C_P \cdot (V_{2H(i)} - V_{1L(i)})) \cdot \exp\left(\frac{-T_{ON}}{R_{SW}C_P}\right)}{2C_P} \quad (12)$$

The term $IC_{12} (= C_P \cdot V_{1L(i)} + C_P \cdot V_{2H(i)})$ represents the total initial charge on the two capacitors among which charges are shared, before the charge transfer phase was initiated.

Along the same lines, the charge-transfer at the output stage, corresponding to the switch SW-3A being turned on, is used to derive expression for $V_{2L(f)}$ and $V_{CP(f)}$ in terms of their initial voltages $V_{2L(i)}$ and $V_{CP(i)}$. In addition, the output voltage increases linearly due to the input load current, for the duration switch SW-3A remains turned off, as given by (13).

$$V_{CP(i)} = V_{CP(f)} + \left(\frac{I_L}{C_L}\right) \cdot (T_{PRD} - T_{ON}) \quad (13)$$

The system of equation thus relates node voltage variables in terms of CP design and operating parameters. The resulting expression for average CP output voltage, ($V_{CP_AVG} = 0.5 \cdot (V_{CP(i)} + V_{CP(f)})$) yields the form mentioned in (14).

$$V_{CP_AVG} = -2 \cdot V_{DD} \cdot \gamma + R_{CP_FXN} \cdot I_L \quad (14)$$

The analysis of the functional model thus verifies the linearity of CP transfer characteristic with respect to the input load current and indicates that the magnitude of CP output at no-load ($|V_{CP_0}|$) is mainly limited due to the parasitic and gate capacitances at intermediate nodes, as captured by the

Fig. 6. 2D Plot of derived R_{CP} function versus C_P , R_{SW} (T_{PRD} : 20ns, T_{ON} : 7.8ns, C_L : 260pF).

loss-factor γ . If the on-time of switches is greater than or equal to 1.5 times the default time constant $\tau (= R_{SW} \cdot C_P)$ of the capacitive charge sharing circuit, then the CP output impedance can be estimated with reasonable accuracy (R_{CP_EST}), using the simplified expression mentioned in (15).

$$R_{CP_EST} = \frac{T_{PRD} \cdot \left[2 \cdot C_L e^{\frac{T_{ON}(5C_L + 2C_P)}{2R_{SW}C_LC_P}} + \dots \right.}{2 \cdot C_P \cdot (C_P + C_L) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_P}} - 1 \right) \cdot \left(e^{\frac{2T_{ON}}{R_{SW}C_P}} - 1 \right)} \quad (15)$$

The actual output impedance function (R_{CP_FXN}), can be visualized via a 2-D plot, versus the pump capacitance (C_P) per stage, and the switch resistance (R_{SW}), as shown in Fig. 6. It can be observed that the output impedance decreases and eventually saturates, as the C_P is increased, or the R_{SW} is decreased. The most area efficient approach to achieve the required output impedance is to select the C_P , R_{SW} combination such that the R_{CP} is not saturated with respect to either of the two design variables.

The technique is utilized in the given design with the emphasis on utilizing a minimal silicon area for the integrated pump capacitance and implement a reasonably sized switching device to achieve the required on-resistance. Fig. 7 depicts the R_{CP} variation with respect to the two design variables, with the C_P and R_{SW} value selected as 15pF and 230Ω respectively, to achieve the required R_{CP} at 3.5kΩ. As observed from Fig. 7, the rate of change of R_{CP} for the selected C_P , R_{SW} pair, is reasonably high with respect to both the parameters, thus ensuring optimal area utilization.

The switching device is sized at ($40\mu\text{m}/600\text{nm}$), such that its on-resistance ($R_{ON} \approx 1/(k'_n(W/L)(V_{GS} - V_T))$) is comparable to the required R_{SW} , with its gate-to-source (V_{GS}) voltage set at half the switching signal amplitude ($0.5 \cdot V_{DD}$). The load capacitor (C_L) is required to limit the CP ripple,

Fig. 7. Charge-pump output impedance versus (a) switch resistance (R_{SW}) with $C_P = 15$ pF and (b) pump capacitance (C_P) for $R_{SW} = 230$.

Fig. 8. Charge-pump output vs. load as obtained from analysis, pre-layout and post-layout simulations.

especially at large load currents. As inferred from (13), to contain the CP ripple under 50 mV, for a maximum load current of $800 \mu\text{A}$, the design utilizes a 260 pF load capacitor, integrated on-chip.

In Fig. 8, the linear CP characteristic obtained through this analysis is contrasted with simulation results for the derived transistor level implementation of the same. The predicted results are in close agreement with the simulation data, whereby the functional model overestimates $|V_{CP,0}|$ by 9% and underestimates R_{CP} by only 1.1%. The residual inaccuracies arise to the inherent differences between the model and the actual transistor level operation. Thus, by considering a non-ideal charge-transfer, the simplified analysis results an accurate prediction of CP transfer characteristic. Moreover, the analysis can be readily extended to N stages, whereby for the general case, a closed-form expression for R_{CP} may not be attainable, however its magnitude can be readily derived in terms of CP design parameters through iterative calculation.

D. Charge-Pump Power Efficiency

The CP efficiency (η_{CP}), defined as the ratio of power delivered at the output to the average dc power consumed by the CP, can be evaluated in terms of the derived CP impedance using (16).

$$\eta_{CP} = \frac{|V_{CP}| \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{DIG})} = \frac{(V_{DD} N \gamma - R_{CP} I_L) \cdot I_L}{V_{DD} \cdot (N \cdot I_L + I_{DIG})} \quad (16)$$

where I_{DIG} is the average dc current consumed in the multi-phase clock generator and clock buffer cells.

The simulated CP efficiency versus load current, for different operating frequencies, is as shown in Fig. 9(a). At low load currents, the efficiency is very low, since the numerator in (16) vanishes, while the denominator is non-zero due to the finite dc power consumed in digital gates and drivers. At large load currents, the term I_{DIG} becomes insignificant compared to the term $(N \cdot I_L)$, and the efficiency decreases rapidly due to the finite output impedance of the CP. Therefore, for a given frequency input, CP efficiency peaks at a particular load (I_{L_MAX}), as shown in Fig. 9(a). At higher operating frequency, (I_{L_MAX}) increases while the achievable peak efficiency is reduced.

The variation of CP output impedance (R_{CP}) and efficiency with respect to operating frequency ($F_{IN} = 1/T_{PRD}$), is as shown in Fig. 9(b). The output impedance is inversely proportional to F_{IN} , as derived in (15), however, the ratio (T_{ON}/T_{PRD}) decreases linearly with the increasing frequency, due to the finite gate delays incurred by the switching inputs. The net effect causes the CP impedance to attain its minimum value R_{CP_MIN} at a given frequency (F_{IN_MAX}) frequency, which can also be regarded as the maximum operating frequency for the CP. In contrast, the current consumption in the digital circuits (I_{DIG}) increases linearly with frequency.

At low frequency inputs, the high output impedance of the CP results in lowering of its output magnitude, thereby resulting in low output efficiency. As frequency is increased, efficiency increases rapidly till it maximizes at an optimum frequency F_{IN_OPT} , beyond which it decreases almost linearly till F_{IN_MAX} . As observed from Fig. 9(b), beyond F_{IN_MAX} efficiency drops rapidly due to combined effect of the increase in digital power and marginal increase in R_{CP} .

To ensure maximum operating efficiency for the CP, the required CP impedance (R_{CP_REQ}), for a given regulated output voltage and load current setting, as estimated using (4), is compared to the impedance obtained at optimum frequency input (R_{CP_OPT}). If R_{CP_REQ} is higher than R_{CP_OPT} , then the CP can be operated with the optimum frequency F_{IN_OPT} to achieve maximum efficiency. If this condition is not met, then the CP needs to be operated at the next higher frequency at which its R_{CP} is equal to R_{CP_REQ} thus ensuring the pass-transistor has enough headroom to operate in the saturation region.

E. Negative Voltage Regulator

The regulator block, as depicted in Fig. 10, comprises of a supply independent bias generator, a low power error-amplifier and a deep-n-well pass-transistor. The regulator is powered by the fully integrated CP and is configured in an inverted low-dropout regulator arrangement. The positive supply rail (V_{POS}) can be varied from 0V to the nominal 3.3V input while external reference (V_{REF}) input needs to be maintained at least 1.1V below the positive supply potential. The regulated output voltage (V_{REG}) can be derived as in (17).

$$V_{REG} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) - V_{POS} \cdot \left(\frac{R_1}{R_2}\right) \quad (17)$$

Fig. 9. (a) Charge-pump efficiency vs. load current. (b) Charge-pump efficiency vs. operating frequency.

Fig. 10. Negative voltage regulator including frequency dependent CP model.

Fig. 11. Schematic of (a) supply-independent bias-generator and (b) symmetrical OTA as error-amplifier.

The available regulated output voltage range varies from $-|V_{CP} - V_{DO}|$ to V_{REF} , where V_{CP} and V_{DO} are the CP output and the dropout voltage of the pass-device at the given load current setting. As observed from (17), in order to desensitize the regulated output with respect to the noise on the positive rail, the input for the feedback divider must be derived from a separate low noise source. The regulator provides over 56dB PSRR with respect to V_{POS} when it is not shared with the feedback divider.

The relatively high impedance of the fully-integrated CP results in wide variation in the available headroom for the regulator. To withstand this variation, the regulator sub-circuits employ thick gate-oxide devices with high V_{DS} and V_{GS} breakdown limits. These devices protect against the large headroom at low load currents, while retaining high loop gain, when the available headroom is shrunk at high loads.

The negative feedback loop is stabilized through an off-chip capacitor (C_{EXT} 220nF), which determines the location of the dominant pole and ensures that the loop remains unconditionally stable for the range of supported load currents. The high feedback loop-gain along with low -3dB frequency set by C_{EXT} , generates low-noise regulated output with lowered output impedance.

F. Bias Generator and Error Amplifier

The schematic for the supply independent bias generator is as shown in Fig. 11(a). The circuit utilizing the $R_B = 1/g_m$ technique, is configured to provide bias current independent of the voltage at its negative supply rail. The bias current is set by varying resistor R_B and is designed to be $1\mu A$ at normal process and temperature corner. This simple yet robust biasing technique ensures that the current variation for the

Fig. 12. Small-signal model for loop stability analysis.

regulator remains under $15\mu\text{A}$ across the entire CP output voltage range. A symmetrical operational transconductance amplifier (OTA) structure, as shown in Fig. 11(b), is utilized as an error amplifier. The given topology has inherently low offset due to symmetry of design and provides high bandwidth due to lack of any internal high impedance nodes. The latter contributes directly in maximizing the stability of the regulator feedback loop. The gain is derived through the relative high impedance of the output stage. The OTA provides a moderate gain greater than 55dB with a 3-dB cutoff frequency higher than 2.5MHz.

IV. SYSTEM LEVEL ANALYSIS

The functionality of the proposed negative voltage generator is analyzed and verified from both small and large signal prospective. The former mainly involves ascertaining of feedback loop stability and quantifying the CP noise rejection offered by the regulator. The large signal analysis includes predicting the settling characteristics and derivation of settling time as a function of the operating conditions. The results obtained from these analyses are further verified through the transient co-simulation of CP and regulator.

A. Loop Stability

The small signal model used for analyzing the stability of the regulator feedback loop, is as shown in Fig. 12. The model incorporates the CP output impedance (R_{CP}) and the CP load capacitor (C_L), while the capacitance at the gate of pass-transistor ($C_{GS_PT} < 15\text{fF}$) is neglected due to the relative small sizing of the pass-device. The OTA is represented using a transconductance element (g_{m_OTA}) and a small-signal equivalent of its output stage. The open-loop transfer function as obtained from breaking the loop at the feedback node, is as derived in (18)-(22).

$$H(s)_{STB} \approx \frac{A_{VDC_STB}(1 + s/\omega_{z1})}{(1 + s/\omega_{p1}) \cdot (1 + s/\omega_{p2})} \quad (18)$$

$$A_{VDC_STB} \approx \frac{[(-g_{m_OTA}R_L) * \dots * (g_{m_PT} - R_{CP} \cdot g_{ds_PT} \cdot g_{ds_OTA})\beta]}{g_{ds_OTA}(2R_Lg_{ds_PT} + R_{CP}g_{m_PT} + \dots + R_L R_{CP}g_{ds_PT}g_{ds_OTA} + 2)} \quad (19)$$

Fig. 13. Gain-Phase plot for the feedback loop for typical and worst-case.

$$\omega_{p1} \approx \frac{2R_L \cdot g_{ds_PT} + R_{CP}(2g_{ds_PT} + g_{m_PT}) + 2}{R_L C_{EXT}(2 + R_{CP}(2g_{ds_PT} + g_{m_PT})) + 2R_{CP}C_L} \quad (20)$$

$$\omega_{p2} \approx \frac{R_L C_{EXT}(2 + R_{CP}(2g_{ds_PT} + g_{m_PT})) + 2R_{CP}C_L}{2R_L C_{EXT} R_{CP} C_L} \quad (21)$$

$$\omega_{z1} \approx \frac{g_{m_PT} - R_{CP} \cdot g_{ds_PT} \cdot g_{ds_OTA}}{R_{CP} C_L g_{m_PT}} \quad (22)$$

The gain-phase plots for typical and worst-case phase-margin (PM) are presented in Fig. 13. The feedback loop is stabilized through the low frequency dominant pole ($\omega_{p1} \approx 1/(C_{EXT}R_L)$) formed by the external capacitor (C_{EXT}) and the output load impedance (R_L). The inclusion of R_{CP} and C_L however also results in the formation of a closely located pole-zero pair (ω_{p2} , ω_{z1}), at frequencies higher the unity-gain frequency (ω_u). The worst-case for loop-stability occurs at mid-load conditions ($300\mu\text{A}$ – $500\mu\text{A}$), when the loop gain is maximized and consequently ω_u is stretched outwards to higher frequencies. The relative location of ω_u to ω_{p2} and ω_{z1} thus results in the observable drop in PM, as shown in Fig 13.

The loop-stability is further ascertained under the presence of external capacitor's equivalent-series-resistance (R_{ESR}). Fig. 13 shows the modified gain-phase plot for the worst-case PM obtained after inclusion of 1ohm R_{ESR} in series with C_{EXT} . The dominant pole frequency ($\omega_{p1} \approx 1/(C_{EXT}(R_L + R_{ESR}))$) remains practically unchanged since the R_L is significantly higher the R_{ESR} resistance for the supported range of load currents ($I_L < 800\mu\text{A}$). In addition, an ESR zero ($\omega_{ESR} \approx 1/(C_{EXT}R_{ESR})$), typically located beyond the unity-gain frequency, is also included in the loop transfer function. If R_{ESR} magnitude in the range of 1Ω to 10Ω , the worst-case PM is slightly improved due to the presence ω_{ESR} in the vicinity of ω_u . For $R_{ESR} < 1\Omega$, the ω_{ESR} is well beyond ω_u to have any impact of stability characteristics. The design is thus tolerant to wide variation in R_{ESR} magnitude and retains unconditional stability for the entire range of its operation.

B. CP Noise Rejection

The small signal model used to evaluate the CP noise rejection offered by the proposed regulator design, is as shown in Fig. 14. The given model is formed by including the small signal representation of the pass-transistor and for each device within the OTA. With reference to OTA's transistor

Fig. 14. Small-signal model for regulator CP noise rejection analysis.

TABLE I
SMALL SIGNAL REPRESENTATION OF OTA DEVICES
AND PASS-TRANSISTOR

Device Name	Tansconductane	Output Conductance
MN#3A, MN#3B	g_{m_diff}	g_{ds_diff}
MN#1	g_{m_N1}	g_{ds_N1}
MP#1A, MP#1B	-	g_{m_P1}
MN#2A, MN#2B	g_{m_N2}	g_{ds_np}
MP#2A, MP#2B	g_{m_P2}	g_{ds_np}
Pass-Transistor	g_{m_PT}	g_{ds_PT}

level schematic in Fig. 11(b), the transconductance (g_m) and output conductance (g_{ds}) of various devices are represented as mentioned in Table I. The output noise transfer function (V_{OUT}/V_{IN}) obtained through nodal analysis of the given model, yields a first order function, as derived in (23)-(25).

$$H(s)_{AC} \approx \frac{Av_{DC}}{(1 + s/\omega_{-3dB})} \quad (23)$$

$$Av_{DC} \approx \frac{g_{ds_np} \cdot (g_{m_PT} \cdot g_{ds_N1} + \dots \cdot \dots + 2g_{m_PT} \cdot g_{ds_np} + 2g_{m_N2} \cdot g_{ds_PT})}{(\beta \cdot g_{m_N2} \cdot g_{m_PT} \cdot g_{m_diff}) * \dots \cdot \dots (2 \cdot R_{CP} \cdot g_{ds_N1} + 2 \cdot R_{CP} \cdot g_{ds_np} + 1)}$$

$$\omega_{-3dB} \approx \frac{(g_{m_PT} \cdot g_{m_N2} \cdot g_{m_diff} \cdot \beta) * \dots \cdot \dots (2R_{CP}g_{ds_N1} + 2R_{CP}g_{ds_np} + 1)}{C_L \cdot g_{ds_np} \cdot [2g_{m_N2} + \dots + R_{CP}g_{m_N2} \cdot (4g_{ds_N1} + 4g_{ds_np} + 2g_{ds_PT}) + R_{CP}g_{m_PT} \cdot (g_{ds_N1} + 2g_{ds_np})]}$$

The numerical values for Av_{DC} and ω_{-3dB} are estimated by substituting the value of g_m and g_{ds} of various devices as obtained through dc operating point simulation, and are found to agree well with the corresponding simulation results. Fig. 15 shows the simulated ac rejection at light ($50\mu A$) and maximum loading ($550\mu A$) condition, for a regulated output of $-1.5V$. It can be observed that the given regulator topology provides over 120dB of noise rejection at typical switching frequencies (10MHz-100MHz) utilized for fully-integrated charge-pumps. This allows effective suppression CP noise and ripple, thus facilitating superior low noise performance.

Fig. 15. Regulator AC Rejection at typical and max. loading conditions.

Fig. 16. Typical settling characteristic of negative voltage generator.

C. Settling Response

The settling transient characteristic of the given negative voltage generator system is analyzed quantitatively using the schematic shown in Fig. 10, with the error amplifier modelled as an ideal gain block. A typical settling profile for the CP (V_{CP}) and regulated output (V_{REG}) voltage, is as shown in Fig. 16. The corresponding drain-source potential (V_{DS}), and the overdrive voltage ($V_{OV} = V_{GS} - V_{TN}$) of the pass-transistor are also depicted alongside.

The settling behavior can be divided into three parts, based on region of operation of the pass-transistor. For the initial ' t_1 ' seconds, pass-transistor is in saturation region, while V_{DS} is greater than V_{OV} . For the next ' t_2 ' seconds, the pass-device operates in the linear region. Post this instant, gain of the error amplifier is boosted as the feedback potential approaches the reference input voltage, and the system rapidly acquires steady state within the following ' t_3 ' seconds. The regulated output voltage follows a clean first order settling, as expected out of a single pole system.

At the beginning, when the system is powered up, it acquires an initial steady state based on the saturation region operation of the pass-device. In this region, the pass-transistor current can be considered constant, and its gate voltage is set equal to positive supply rail of the OTA since the feedback potential is significantly higher than the reference input. The system state is described through (26)-(28).

$$V_{GS} = V_{POS} - C_{CP_SAT} \quad (26)$$

$$V_{CP_SAT} = V_{CP_0} + (I_{PT_SAT} + I_{REG})R_{CP} \quad (27)$$

$$-I_{PT_SAT} = V_{REG}(t)(1/R_L) + \left(\frac{dV_{REG}(t)}{dt}\right)C_{EXT} \quad (28)$$

In addition, two boundary conditions can be included based on the initial regulated output ($V_{REG}(0)$) and the regulated output at time t_1 ($V_{REG}(t_1) = V_{POS} - V_{TN}$), at

Fig. 17. Standard logistic function utilized to model error-amplifier response.

which the overdrive voltage of the pass-transistor crosses its drain-source potential.

The initial inrush current (I_{PT_SAT}) and the CP output (V_{CP_SAT}), can be derived in terms of pass-transistor design and process parameters using (25)-(27) along with the standard current approximation ($I_{DS} = 0.5 k'_n (W/L) (V_{GS} - V_{TN})^2$) used for the saturation region. The solution of differential equation (27) in conjunction with the boundary condition is used to obtain regulated output as a function of time $V_{REG}(t_1)$, and time ' t_1 ' in terms of (I_{PT_SAT}), as evaluated in (29), (30).

$$V_{REG}(t) = I_{PT_SAT} R_L \cdot \exp\left(\frac{-t}{R_L \cdot C_{EXT}}\right) - I_{PT_SAT} R_L \quad (29)$$

$$t_1 = -C_{EXT} R_L \cdot \log\left(\frac{V_{POS} + I_{PT_SAT} R_L - V_{TN}}{I_{PT_SAT} R_L}\right) \quad (30)$$

In the linear region, the pass-transistor is modelled as a resistor, with its on-resistance ($R_{ON} \approx 1/(k'_n (W/L) (V_{GS} - V_{TN}))$) dependent on its instantaneous gate to source voltage ($V_{GS}(t) = V_G(t) - V_{CP}(t)$). The gate voltage of the pass-transistor is evaluated by modelling the OTA response using the standard-logistic function, as mentioned in (31) and depicted in Fig. 17.

$$V_G(t) = \frac{V_{CP}(t)}{1 + e^{k \cdot x}} + \frac{V_{POS}}{1 + e^{-k \cdot x}} \quad (31)$$

$$x = V_P - V_N = (V_{REG}(t))\beta - V_{REF} \quad (32)$$

$$k = \frac{4A_v}{V_{POS} - V_{CP}(t)} \quad (33)$$

where β is the feedback factor and x represents the differential input to the OTA. The term k models slope of the transition region, and is derived in (33) by equating the derivative of the OTA function in (31) at 0V input, equal to the nominal gain A_v obtained from the OTA.

The dynamic system state can be described using the differential equations obtained from the nodal analysis at the drain and source terminals of the pass-transistor, as mentioned in (34) and (35).

$$\frac{V_{REG}(t)}{R_L} + \left(\frac{dV_{REG}(t)}{dt}\right) \cdot C_{EXT} + \frac{V_{REG}(t) - V_{CP}(t)}{R_{ON_PT}} = 0 \quad (34)$$

$$I_{REG} = \frac{V_{CP}(t) - V_{REG}(t)}{R_{ON_PT}} + \frac{V_{CP}(t) - V_{CP_0}}{R_{CP}} \quad (35)$$

The set differential-algebraic equations (31)-(35), although complete, do not yield a closed form solution for the node

Fig. 18. Settling characteristic: Analysis vs. simulation.

Fig. 19. System level verification through transient co-simulation of CP and regulator ($V_{REG} = -3.0V$, $I_L = 200\mu A$, $C_{EXT} = 220nF$).

voltage variables ($V_{CP}(t)$, $V_G(t)$, $V_{REG}(t)$). Therefore, for the linear region operation of pass-transistor, the given system of equations is computationally analyzed to derive numerical solutions at different time instants. The resulting settling behavior for the regulated output and charge pump output voltage, as predicted by the quantitative analysis, is compared with the simulation results in Fig. 18.

The given analysis accurately predicts the complete settling profile, including the inrush current and the transition time ' t_3 ', depicted in Fig. 16. It can be further verified, that the given analysis result in less than 1% error in estimation of total settling time, under all operating conditions.

D. System Level Verification

The stability and performance of the proposed negative voltage generator system is full established through rigorous, time-domain co-simulation of CP and regulator modules. This is also essential to ensure that the system can operate without requiring a dedicated start-up sequence. The complete settling characteristic for $-3.0V$ regulated output at $200\mu A$ load current, as obtained from system level transient co-simulation, is shown in Fig. 19. The transient behavior can be closely co-related with the large signal simulations using the CP linear model and the results obtained from the associated analysis. The simulated steady-state ripple magnitude for the CP and the regulated output are $10mV_{PP}$ and $261nV_{PP}$, thus implying over 90dB rejection at CP operating frequency.

V. MEASUREMENT RESULTS

The proposed negative voltage generator system is experimentally verified using a prototype chip fabricated in 6-metal CMOS 180nm process. The thick gate-oxide 6-terminal deep-n-well nmos, and 5-terminal pmos devices, offered in this

Fig. 20. Chip micrograph and PCB test setup.

Fig. 21. Measured CP characterization curves for different operating frequencies.

technology, have high V_{DS} , V_{DS} and p-n junction breakdown limits, which is instrumental in ensuring reliable operation for the overall design.

The design is validated using a small pcb test fixture as shown in Fig. 20. This test setup allows the external capacitor to be in close proximity of the regulated output pin, which is essential towards minimizing the steady state ripple and improving the noise performance of the design. The die photo of the prototype chip is also depicted alongside. The silicon implementation including 290pF of integrated MIM capacitance, occupies a total area of 0.55mm².

The system level verification is preceded with characterization of CP performance at different operating frequencies. The CP output vs. load current and the extrapolated linear model at 30MHz, 40MHz and 50MHz input clock, is shown in Fig. 21. The measured CP magnitude at no-load ($|V_{CP_0}|$) is 200mV to 250mV lower, while the output impedance (R_{CP}) is 350Ω to 400Ω higher, as compared to post-layout simulations. This suggests that for the system level implementation, the charge-pump output must be estimated with at least 10% design-margin reserved for the linear model parameters $|V_{CP_0}|$ and R_{CP} . The measured peak CP efficiency for 30MHz and 50MHz input is 12.13% at 350μA and 12.48% at 450μA load, which is approximately 8% and 4% below its simulation counterpart respectively. This reduction in CP efficiency arises primarily due to a higher magnitude of measured CP output but is also contributed in part by an increased digital power consumption, as recorded during measurement.

In Table II, the stand-alone performance of the CP is contrasted with other switched-capacitor based voltage multipliers. The CP supports a wide range of load current up to 800μA

Fig. 22. Measured settling characteristic ($V_{REG} = -2.8\text{V}$, $I_L = 200\mu\text{A}$, $C_{EXT} = 220\text{nF}$). Fig. 23. Measured steady-state ripple ($V_{REG} = -1.5\text{V}$, $I_L = 550\mu\text{A}$, $C_{EXT} = 220\text{nF}$). Fig. 24. Measured noise spectrum transform for regulated output ($V_{REG} = -1.5\text{V}$, $I_L = 550\mu\text{A}$, $C_{EXT} = 220\text{nF}$, $F_{IN} = 50\text{MHz}$).

while offering a relatively low and constant output impedance, for a given operating frequency. However, as compared to other works [6], [7], CP efficiency is low due to the lower pump capacitance per stage and lesser number of inverting stages, thus resulting in significantly less area utilization. In addition, it should be noted that for a given no. of stages (N), the boosting CPs ($V_{OUT} > V_{IN}$), as reported in [13], deliver higher efficiency since the CP output magnitude is increased by a factor of $N + 1$ as opposed to an increase by a factor of N for inverting CP configuration.

The measured settling characteristic for the regulated output voltage of -2.8V at $200\mu\text{A}$ load current, is as shown in Fig. 22. The complete settling profile, for both the CP and the regulated output voltage closely matches the simulation results and analysis. The measured settling time of 1.2ms, obtained under the given operating condition, also agrees very well with 1.15ms obtained using computational analysis and large signal simulations, when evaluated with the CP linear model extracted from its measured characterization curves.

TABLE II
PERFORMANCE COMPARISON OF NEGATIVE CHARGE-PUMP WITH SWITCHED-CAPACITOR BASED VOLTAGE MULTIPLIERS

Parameters	[15]	[6]	[7]	This Work
Topology	Cross-Couple	Bootstrap	Cross-Couple	Bootstrap
F_{IN} (MHz)	50-100	33.25	-	30-70
N	3-stg.	6-stg.	3-stg.	2-stg.
V_{IN} (V)	1.8	1.8	3.3	3.3
V_{OUT} (V)	6.6 ($I_L:0\mu A$) 4.9 ($I_L:350\mu A$)	-8.0 ($I_L:0 - 320\mu A$)	-8.6 ($I_L:0\mu A$) -8.3 ($I_L:200\mu A$)	-4.98 ($I_L:0\mu A$) -1.73 ($I_L:800\mu A$)
C_P /Stg.(pF)	5	25	50	15
R_{CP} (Ω)	4.7k ($F_{IN}: 100\text{MHz}$)	-	-	3.9k ($F_{IN}: 50\text{MHz}$)
Peak Eff.(%)	54 ($I_L: 350\mu A$)	42.3 ($I_L: 200\mu A$)	35.8*	12.4 ($I_L: 450\mu A$)
Technology	180nm CMOS	180nm CMOS	0.8 μm CMOS	180nm CMOS

*Simulation result

Fig. 25. Precision negative voltage biasing test with GaN-HEMT PA. (a) Test-setup. (b) Measured PA performance showing spectrum, constellation and EVM.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH REGULATED NEGATIVE VOLTAGE GENERATOR

Parameters	[6]	This Work
V_{DD}	1.8V	3.3V
V_{REG} Range	-8.0V	-4.4V to 2.1V
Max. Load	320 μA	>250 μA ($V_{OUT} > -3.0V$) >550 μA ($V_{OUT} > -1.5V$)
Load Reg.	194 $\mu V/\mu A$	102 $\mu V/\mu A$
V_{REG} Ripple	30mV _{PP}	< 3mV _{PP}
V_{N_RMS} at NF_{IN}	-	< 130 μV_{RMS}
Settling Time	-	< 1.2ms ($C_{EXT}: 220nF$)
Power	3.8mW	12.5mW
Area/ Process	1.27mm ² / 180nm CMOS	0.55mm ² / 180nm CMOS

Fig. 23 shows the measured steady state ripple for $-1.5V$ regulated output at $550\mu A$ load current, alongside the ripple on CP output and reference input. To accurately capture the transient output ripple, maximum load current for the given regulated output is utilized. In addition, long measurement time span of 1ms is chosen to capture both the high and low frequency ripple, and ac coupling is avoided to prevent any possible low pass filtering. The steady-state ripple amplitude is $2.7mV_{PP}$ and remains equal to the ripple measured for the external reference input for all vertical (voltage) and horizontal (time) division settings on the oscilloscope. This suggests that the steady-state ripple performance and the

regulation accuracy of this design is only limited by accuracy of external reference input.

The spectral purity of the regulated output is examined using a spectrum analyzer, as shown in Fig. 24. The resolution bandwidth is 10kHz and the span is set to cover the five harmonics of the CP operating at 50MHz. For a regulated output of $-1.5V$ at $550\mu A$ load current, and 220nF external capacitor, the measured noise floor is below $5\mu V_{RMS}$, while spot noise voltages at clock frequency harmonics is below $130\mu V_{RMS}$, as highlighted in Fig. 25.

To ensure that the proposed negative voltage generator is compatible with precision voltage biasing applications, it is tested with the GaN HEMT PA reported in [5], as shown in Fig. 25. The PA requires a precise negative gate bias voltage which needs to be tuned from $-2.8V$ to $-3.2V$, to extract maximum RF performance. The given GaN PA, delivers identical linearity and drain efficiency performance, as that obtained with an external negative input source, thus further verifying the low noise performance of the given design.

A comparison of the proposed design with another reported regulated negative voltage generator is drawn in Table III.

VI. CONCLUSION

This work presents the design and analysis of a highly integrated, negative voltage generator, providing tunable, low-noise, negative voltage output. The proposed solution, utilizing only one off-chip capacitor, supports wide tuning range with moderate driving capacity. The low noise performance is silicon verified with under $3mV_{PP}$ steady state ripple and high degree of spectral purity. A systematic design methodology, supplemented with an in-depth analysis of CP and regulator modules, ensures robust implementation with reliable performance output. An on-chip negative generator, can facilitate the integration of alternate technologies with mainstream CMOS, besides allowing the designer to experiment with much wider range of circuits and applications. In this regard, the proposed design and the analysis carried out in this work, can be useful towards the evolution of a negative voltage generator solution that can be included as a generic IP in future SOCs.

ACKNOWLEDGMENT

The authors would like to thank Gek Eng and David Robert Neubronner for their valuable support during testing.

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