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A 3GS/s Highly Linear Energy Efficient Constant-Slope Based Voltage-to-Time Converter

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Abstract—This paper presents a high speed highly linear energy-efficient constant-slope based voltage-to-time converter (VTC). By combining sample-and-hold with constant charging process, we achieve precise sampled step and linear charging ramp concurrently without using the extra control clock. Simple calibration has been implemented to overcome conversion gain variation due to process-voltage-temperature (PVT) variation. The post-layout simulation results show that the SFDR/THD of the proposed VTC reaches 58.7dB/56.3dB at 3GS/s near Nyquist (typical corner). The VTC achieves 144ps output range with 0.83mW power consumption at 3GHz. It occupies an active area of 41.3um x 34.4um implemented in 65nm CMOS.

Keywords—time-based, time-based ADC (TBADC), CMOS ADC, voltage-to-time converter (VTC), constant-slope, energy efficient

I. INTRODUCTION

Time-based signal processing has been a promising solution for ultra-deep submicron mixed-signal circuit design [1]. Time-based circuit benefits from the scaling of CMOS technology as it is immune to the accompanying negative effects such as the worse SNR and lower intrinsic gain of transistors. It finds wide applications in frequency generation (digital phase-locked loop), power converter (pulse width modulation DC-DC), data conversion (time-based ADC (TBADC)) and energy efficient neural network acceleration [1]. Among the various applications of time-based signal processing, TBADC has attracted a great deal of attention [2]. TBADC features friendly digital-orientation and has potential advantages over voltage-based ADC in terms of the power consumption and chip area. Several gigahertz TBADCs have been reported recently [1-3]. A 2GS/s 8-bit TBADC based on the remainder number system (RNS) has been proposed in [2]. The RNS quantization method reduces the number of comparators but the power consumption is still high. A two-step 1GS/s 8-bit TBADC with 2.3mW power dissipation has been reported in [1]. It achieves better energy efficiency compared to other gigahertz TBADCs [1]. However, the sampling rate is limited up to 1GHz due to the complicated 2-step structure. It's worth to note that the poor performance of voltage-to-time converter (VTC) is the bottleneck for these published high speed TBADCs. The existing trade-off among linearity/dynamic range, power consumption and bandwidth of VTC impedes the progress of high speed low power TBADC design.

The current starved inverter (CSI) based structure [3-5] is widely implemented in high speed VTC since no sampling circuits is needed. However, the linearity and dynamic performance are poor due to the nonlinear discharging process as shown in Fig. 1. The input transistor should be kept at saturation region before the voltage of node X crosses the threshold V_{TH} to guarantee the linearity of VTC. It results in low conversion gain and limited input range. The compensated differential CSI structure has been proposed to

improve the linearity while the conversion speed is sacrificed [1]. The constant-slope charging method has been deployed for high linear VTC and digital-to-time converter (DTC) design recently [2, 6, 7, 9]. The initial voltage step is set according to the input signal sampled by the input switch. The sensing time is linearly dependent on the input signal in consequence and will be recorded by the subsequent stage as shown in Fig. 2. Constant-slope charging improves the linearity and dynamic range compared to the CSI based structure. However, the conversion speed is reduced while power is increased [2]. To overcome this linearity and speed trade-off for low power VTC, we present a 3GS/s highly linear VTC by combining sample-and-hold with constant charging process together. The sample and hold switch setups the initial voltage through charge redistribution, and consequently, the voltage step appears at the clock signal path. The constant-slope charging is then realized by a cascaded PMOS current source. By manipulating the timing of charging/discharging and switch on/off delicately, the nonidealities can be alleviated, thus high linearity is achieved. Since the sample-and-hold is working concurrently with the charging process, the conversion speed is improved by three times compared to [4].

Fig. 1 Basic structure of CSI based VTC.

Fig. 2 Structure of the constant-slope based VTC.

The rest of this paper is organized as follows. Section II introduces the architecture of the proposed VTC and describes the circuit design in detail. It elaborates the working principle of the VTC by constructing an intuitional model. Post-layout simulation results and discussion have been presented in section III. Finally, the conclusion is drawn in Section IV.

II. ARCHITECTURE AND CIRCUIT DESIGN

A. Architecture

Since the constant-slope based VTC contains voltage stepping and linear ramp charging, control timing of the two parts should be allocated precisely to enable high linearity. It

unfortunately increases the difficulty of clock generating and power consumption, especially at several gigahertz frequency bands. Both works published in [2] and [6] need extra circuits to generate the control clock. Hence, the conversion speed needs to be reduced to guarantee the overall performance of VTC. To eliminate the extra clock generation block, we proposed a novel constant-slope based VTC combining the sample-and-hold with the constant charging process. Fig. 3 shows the architecture. The control clock for sample-and-hold switch is derived directly from the clock path. The switch S_5 is deployed to reset the node Y before the voltage step generated. When the clock rising edge reaches the input node I , switch S_1 and S_4 are on and switch S_2 and S_3 are off, the input signal is sampled by capacitor C_{IN} and node X is discharged to ground by S_4 . Meanwhile, switch S_5 resets the node Y to 0. The operation model at this sampling period is redrawn in Fig. 4 (a) for simplification. When the clock falling edge reaches I , the switch S_1 , S_4 and S_5 are closed and switch S_2 turns on. The voltage of node Y changes immediately and a voltage step V generates. The voltage of node X will follow the voltage of node Y because no charging path exists for node X instantaneously (the AC resistance of the current source is very large). The operation model at this stepping period is shown in Fig. 4 (b). Afterwards, the voltage of node X is pulled up to VDD at a constant rate charged by the current source. The time of crossing threshold V_{TH} is sensed by the next stage. The step value at node X should be lower than the threshold V_{TH} for VTC to work. Hence, capacitor C_P is added in the clock path to set a proper step value of node X . It increases the input to rail-to-rail range by shrinking the sampled voltage step.

Fig. 3 Architecture of the proposed VTC.

Fig. 4 (a) Sampling and resetting. (b) Stepping and charging.

The shrinking ratio is determined by C_T and C_P . Furthermore, the relation between V_{IN} and V_X can be calculated using charge conservation law as follow:

$$C_{IN} V_{IN} = \left(C_{IN} + \frac{C_T \times C_P}{C_T + C_P} \right) \times V_Y \quad (1)$$

$$V_X = \frac{C_T}{C_T + C_P} \times V_Y \quad (2)$$

$$V_X = \left(1 + \frac{C_T}{(C_T + C_P) C_{IN}} \right) \times \frac{C_T}{C_T + C_P} \times V_{IN} \quad (3)$$

Since the time difference is directly proportional to step value V_X as shown in Fig. 2, the conversion process is completed in linear relation with the input signal.

B. Circuit Implementation

The proposed architecture can be realized in schematic as shown in Fig. 5. To suppress the even mode harmonics and improve the SNR of VTC, pseudo differential structure is implemented. Since the input signal reaches rail-to-rail, the switch S_1 of the sample and step part is implemented using bootstrap, while switch S_2 is implemented using CMOS switch. Although the equivalent resistance of the CMOS switch varies along the full rail range, it will not influence the stepping process since charge is only redistributed between the top plate of C_{IN} and bottom plate of C_T . The reset value for S_5 is chosen properly instead of directly connecting to ground in order to increase the conversion gain. As illustrated in the lower inset of Fig. 5, negative step is achieved when V_{RESET} is larger than zero which enables larger output range. To simplify the circuit design, the current source is implemented by a voltage biased PMOS, the switch S_3 and S_4 are substituted by an inverter and the sense amplifier is implemented using an inverter. The current source transistor should be kept in saturation region before the voltage of node X crosses the V_{TH} . It guarantees constant charging. In addition, the control time for the switches and the charge transistors should be checked carefully to alleviate the nonidealities (variational equivalent resistance, charge sharing and clock feedthrough). The bias voltage of the source transistor can be used for calibration considering the gain variation across different process-voltage-temperature (PVT). The effectiveness of this simple calibration is verified in section III. Note that the varying resistance of switch S_2 will influence the charging process of node X . This effect can be reduced by choosing the proper value of C_P . C_P not only sets the conversion gain but also weakens the non-ideal effects of switch transistors and charging transistors. Moreover, unlike the conventional CSI-based VTC in which multiple inverter stages should be chained to get enough output range [4], the signal path of the proposed VTC is composed of only six stages and realizes 144ps output at 3GHz. It results in better linearity with high energy efficiency.

Fig. 5 Schematic of the proposed differential VTC.

The layout of the proposed VTC is shown in Fig. 6. It occupies an active area of 41.3um x 34.4um when implemented in 65nm CMOS technology.

Fig. 6 Layout of the proposed VTC.

III. SIMULATION RESULTS

The voltage-to-time conversion curve from post-layout simulation is presented in Fig. 7. A slow ramp input signal is utilized as the input, and the output time difference at threshold voltage is recorded and drawn. The curves swept with clock frequency show highly linear characteristic and little dependency on clock frequency. The maximum gain variation is only 1.3ps/V with 151.5ps/V average gain as shown in the inset of Fig. 7. The proposed VTC shows high stability across the whole working frequency band.

Since the CMOS inverter charge/discharge rate is influenced substantially by PVT variation, the performance of the VTC should be checked carefully under different PVT. As shown in Fig. 8 (a), the conversion process with TT/1V/27°, SS/0.96V/65° and FF/1.1V/-27° have been simulated when the working frequency sets to 3GHz. It shows the gain varies substantially across the PVT condition. The fluctuated conversion gain will increase the difficulty of the subsequent TDC design when VTC is deployed in a TBADC system. The calibration can be realized by tuning the bias voltage of current source transistor M_{cal} . In the simulation testbench, an ideal 5-bit DAC is utilized to generate 32 levels bias voltage from 0 to 0.5V. The calibrated conversion curves are shown in Fig. 8 (b) verifying the effectiveness of this simple calibration.

Fig. 7 Conversion curves with slow ramp inputs.

Fig. 8 Calibration of PVT variation for the conversion curves.

The effects of mismatch due to layout and process variation are simulated for the proposed differential VTC.

Fig. 9 (a) shows the Monte Carlo simulation results of the output time difference when input amplitude is 0 (offset). Fig. 9 (b) shows that the gain variation due to mismatch is small (321fs/V standard deviation), therefore only offset matters. The output offset can be eliminated by tuning the bias voltage of the input signal when AC coupling is used or adding tuning delay blocks before the TDC to calibrate it.

Fig. 9 Monte Carlo simulation for (a) time offset and (b) conversion gain variation.

VTC's dynamic performance is crucial since it works as the front end for the TBADC. Fig. 10 shows the SFDR, THD simulation results when clock frequency ranges from 1MHz to 3GHz and the input frequency is swept accordingly. The influence of phase mismatch of the input signal is also simulated. The SFDR and THD near Nyquist are summarized in Fig. 10 (f). The results show that the VTC achieves stable SFDR/THD performance across the whole working band even the phase mismatch of the input signal reaches 5°.

Fig. 10 (a)-(e) SFDR/THD at different clock frequency (the input frequency is normalized accordingly) and (f) SFDR/THD at Nyquist.

Fig. 11 shows the SFDR/THD with different input amplitude near Nyquist at 3GHz clock. Because of the nonidealities of the switch and the charging transistor, the performance will degrade when the input peak-to-peak amplitude reduces below 300mV. The effects of PVT variation on SFDR/THD are also simulated as shown in Fig. 12. It shows the SFDR/THD (near Nyquist at 3GHz) varies across the different PVT condition. The worst case occurs at the SS corner and the performance at this corner can be improved by increasing the power voltage. The Monte Carlo simulation for SFDR/THD is shown in Fig. 13. The standard

deviation for SFDR and THD are 1.44dB and 1.17dB respectively. The layout and process mismatch have little influence on SFDR/THD of the proposed VTC according to the simulation results.

Fig. 11 SFDR/-THD with different input amplitude.

Fig. 12 SFDR/-THD VS PVT variation.

Fig. 13 Monte Carlo simulation of SFDR/-THD.

The power consumption of the VTC core is 0.83mW at 3GHz TT corner. In conclusion, the performance of the proposed VTC is summarized and compared to the state-of-the-art high speed VTC. The Walden FOM defined for ADC can also be deployed here if we use SFDR to represent the dynamic range of VTC. Table I shows that the proposed work achieves the best energy efficiency at 65nm technology with 4.71fJ/conv. Note that the results shown in Table I are simulation results from references for fair comparison (except for the power consumption values of [4] and [6]).

It is crucial to note that the signal-to-noise ratio (SNR) for VTC is defined by output time difference over jitter. The

inverter chain has poor jitter performance at high frequency, thus the effective number of bits (ENOB) or dynamic range is limited by SNR rather than SFDR/THD (which is verified by our simulation when transient noise simulation is used counting different noise source and nonideal stimulus/bias). Therefore, the output range should be increased to improve the ENOB. Also, the output range should be large enough to guarantee the testability, since the measurement is limited by the LSB of the VTC and the accuracy of the oscilloscope. In [4], the input is quantized and the INL/DNL and THD is measured accordingly, it requires the oscilloscope to provide accuracy smaller than 1ps at 500MHz clock. However, the ENOB that can be measured is limited by this method using oscilloscope especially when sampling frequency reaches several gigahertz. Ref. [8] provides a frequency domain method by phase modulation without using high performance oscilloscope, but it is not suitable for near Nyquist testing. Although, the output range needs to be increased for both performance and testability consideration, it compromises with the working frequency. Cascading the single VTC cell may be a solution for the proposed design to get a larger output range. However, the timing control of charging/discharging and sample-and-hold switching will be more complicated.

TABLE I. PERFORMANCE COMPARISON.

	[1]	[2]	[4]	[5]	[6]	This work
Year	2019	2018	2016	2016	2019	2019
Tech. (nm)	65	65	28	65	65	65
Arch.	CSF ^a	Constant slope	2-step Transition	CSI	CSI	Constant slope
VDD (V)	1	1.2	1.2	1	1.2	1
Input Range (V)	0.8	1.2	1.2	1	1.2	1
Output Range (ps)	100	480	128	126	2340	144
Conversion Speed (GS/s)	1	2	1	4	0.5	3
SFDR (Nyquist typical) (dB)	60	48.4	57	52	68	58.7
Power (mW)	0.54	1.9	0.18 ^b	8	0.48 ^b	0.83
FOM ^c (fJ/conv.)	10	19.6	3.15	38.5	14.1	4.71

^a Compensated dynamic

^b Measurement

^c $FOM = \frac{Power}{SFDR \times F_s}$

IV. CONCLUSION

A 3GS/s highly linear energy efficient VTC has been reported in this work. The proposed VTC combines the sample-and-hold with constant charging process together, achieving the precise sampled step and linear ramp concurrently through charge redistribution and constant charging. It achieves 58.7dB/56.3dB SFDR/-THD and 144ps output range with 0.83mW power consumption at 3GHz clock. Implemented in 65nm CMOS, the VTC occupies an area of 41.3um x 34.4um.

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