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A DC-Reactor Based Solid-State Fault Current Limiter for HVDC Applications

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Abstract—Expansion of high-voltage dc (HVdc) systems to multi-terminal HVDC (MT-HVDC) systems/grids considerably increases the short circuit levels. In order to protect the emerging MT-HVDC systems/grids against fault currents, proper DC fault current limiters (FCLs) must be developed. This paper proposes an innovative high inductance solid-state DC-reactor based fault current limiter (HISS-DCRFCL) to be used in HVDC applications. In fact, during the HISS-DCRFCL normal operation, its inductance value is extremely low, and its value becomes considerably high during the fault period, which decreases the fault current amplitude. The proposed HISS-DCRFCL performance is analyzed by MATLAB/Simulink and the simulation results are verified and confirmed by laboratory experimental results using a scaled-down laboratory prototype setup.

Index Terms—HVDC, fault current limiters, DC-reactor, protection, smart grids.

I. INTRODUCTION

Voltage source converter (VSC) based multi-terminal high-voltage DC (MT-HVDC) systems, which consists of more than two stations connected to each other through HVDC links, is a technical solution for integrating harvested energy from offshore wind farms to ac grids and formation of super grids. There are several control strategies available for MT-HVDC grids [1]. In this new paradigm, protection is of utmost importance. In [2], the proposed control system is tested under various wind power generation scenarios and fault conditions. During the fault period, the stored energy in the DC side as well as a contribution of the high-voltage ac (HVAC) side, result in extremely high fault currents, which may damage the power electronic devices of the converters. Fig. 1 illustrates this issue.

Fig. 1. Fault current components in DC side of a VSC station.

As high-voltage DC circuit breakers have become commercially available, studying the nonunit protection principles of HVDC transmission lines becomes an important

issue in order to improve system security [3]. Considering the frequency response characteristics of the boundary units positioned in HVDC systems, a universal analytical method of fault characteristics for HVDC systems is developed and reported in [4]. Currently, ABB hybrid DC circuit breaker is one of the most promising devices for MT-HVDC system protection against fault currents. Fig. 2 depicts the ABB hybrid HVDC circuit breaker structure [5].

Fig. 2. Hybrid DC circuit breaker launched by ABB.

DC circuit breakers (DCCBs) are required to have rapid fault clearance and high current interruption, as well as low power loss under normal operation. In [6], a hybrid DCCB that includes a semiconductor breaker and a mechanical switch has been investigated to achieve rapid fault clearing, within 3 ms. A comprehensive review of HVDC circuit breaker technologies is presented in [7]. On the other hand, fault current limiters (FCLs) have been introduced and utilized in ac grids. The main specifications of FCLs include very low impedance during normal operation, and high impedance during fault conditions [8]–[11]. Superconductive resistive fault current limiters are recommended for HVDC applications, converters, and protection of multi-terminal HVDC systems [12]–[19]. Generally, a superconductive fault current limiter (SFCL) can be applied to mitigate the DC short circuit influence on a VSC-HVDC transmission system. This limiter uses superconducting coils and resistance to limit the rapidly growing current [20]. Verifying the impact of the SFCL integration into the current limiting inductors, current stress on the hybrid DC circuit breaker (HDCCB), surge arrester energy and the DC fault current characteristics are absolutely essential, which has been investigated in [19]–[21]. In [19], an assessment is carried out by utilizing a behavioral model of generic resistive SFCL. In [22], a flux coupling superconducting fault current limiter (SCFCL) application has been presented in decreasing HVDC commutation failure. Literature studies show that a considerable progress has been made in high temperature superconductor (HTS) materials and SCFCL development. Several solid-state devices have also been developed in recent years [23]. In addition, saturated

iron-core FCL application in an ac grid is presented [24]–[26] in order to reduce the magnitude of the fault current in HVDC systems. However, it is not an applicable method in the DC systems. DC reactor FCL is a DC-based FCL that applies to ac grids for decreasing the fault current amplitude [27]. Many investigations have been carried out and experimental tests have verified their performances [27]–[31]. DC reactor FCLs (DCRFCL) is formed by a rectifier bridge connected in series with the electrical network and a DC coil that is placed in the DC output of the rectifier bridge, as shown in Fig. 3. The inductance value of this structure plays a vital role to limit the fault current. Although, for high inductance values, the fault current can be fairly well limited, however, the DCRFCL became more sensitive to electrical load variations.

Fig. 3. Conventional dc-reactor type FCL (DCRFCL) [26].

In this paper, an innovative fault current limiter for HVDC system applications is introduced. This FCL is based on high inductance solid-state DCRFCL. During the normal operation, DCRFCL will appear as a very low inductance in the HVDC line, and its value will significantly raise by the insulated-gate bipolar transistor (IGBT) operating during the fault condition. Therefore, the proposed device can successfully protect HVDC systems/grids against fault currents.

It is worth remarking that, all the FCLs suggested for HVDC applications are based on resistive superconductor FCL [12]–[19]. Those types of FCL have no resistance in normal operation and high resistance in fault conditions. The rest of this paper is organized as follows. Section II presents the application and the fundamentals of the proposed HISS-DCRFCL. Section III reports the analytical study of the proposed FCL for the HVDC application. Simulation results are represented in Section IV. Section V reports experimental results from a scaled-down laboratory prototype. Finally, the main conclusions of this study are reported in Section VI.

II. CONFIGURATION OF THE PROPOSED HISS-DCRFCL

An HVDC line with short-circuit protection is shown in Fig. 4(b). The proposed HISS-DCRFCL comprises of two inductances that are connected in series and a bypass resistor connected in parallel with the secondary inductance via IGBT switch, as shown in Fig. 4(a). The operating principles of the proposed HISS-DCRFCL can be expressed in three states. In the first state, the FCL operates in the steady-state condition where the IGBT is in the on state.

In this operating condition, the line current does not go beyond its rated value and flows through the series inductance with a negligible voltage drop while the IGBT switch is on.

In the second operation state, power flow variations cause a line current transient, resulted in voltage induction in L_s while the IGBT switch is still on to bypass the secondary winding via the resistor (R).

Fig. 4. (a) Proposed HISS-DCRFCL structure and (b) HVDC line protected by HISS-DCRFCLs.

The secondary winding current produces a reverse flux in its magnetic core, and the voltage drop on the FCL series inductance decays to zero. In the last state, the IGBT is turned off, a considerable inductance is connected in series with the line, and its voltage drop decreases the fault current. The FCL magnetic structure and its equivalent electrical circuit are represented in Fig. 5. In addition, in order to have adequate surge protection, a ZnO surge arrester is connected in parallel with the IGBT in order to suppress transient phenomena [32]. In this structure, the core flux is generated by the windings DC current. The proposed HISS-DCRFCLs equivalent circuit consists of a high inductance series winding L_p , low resistance R_p , low series inductance winding L_s and its resistance R_s , which will be considered negligible. In addition, the IGBT in series with the bypass resistance R is connected in parallel with the low inductance winding, as shown in the equivalence circuit in Figs. 6–8.

Fig. 5. HISS-DCRFCL magnetic structure.

III. HISS-DCRFCL ANALYTICAL STUDY

In this section, the analytical study of the proposed HISS-DCRFCL is derived and reported. The study approach is based on the equivalent circuit as shown in Figs. 6–8. The HISS-DCRFCL operation modes are presented in the following sections.

A. Normal Operation Mode

In this case, the direct current has a certain value and has no transients. Therefore, there is not an inductive effect on the series inductances (L_p and L_s) and consequently, the voltage drop is negligible, there will be a small resistance in the line as shown in Fig. 6. In this state, the bypassed FCL does not influence the smoothing and the phase reactors.

Fig. 6. Equivalent circuit in normal operation mode.

The HISS-DCRFCL series voltage drop can be expressed as follows:

$$L_p \frac{di_{dc}}{dt} = L_s \frac{di_{dc}}{dt} = M \frac{di_{dc}}{dt} = 0 \quad (1)$$

$$V_{FCL} = i_{dc} (R_p + (R \parallel R_s)) \quad (2)$$

$$i_r = i_{dc} \left(\frac{R_s}{R_s + R} \right) \quad (3)$$

where V_{FCL} is the HISS-DCRFCL voltage drop, i_{dc} and i_r are DC line and IGBT current, respectively. According to (3), the IGBT current in normal operation is 0.2 times the line current.

The FCL power loss is modeled by (3), where the IGBT is not assumed to be ideal, but the FCL resistance is considered negligible.

$$P_{loss} = i_{dc}^2 (R_p + R \parallel R_s) + (i_r \cdot V_{SS}) \quad (4)$$

The IGBT switch is in the on state and ready for bypassing L_s of the FCL and consequently bypassing the coupled L_p for the dynamic operation.

B. Dynamic Operation

When the DC line current is increased or decreased by the action of the dispatching control center, a voltage induction appears on L_s . This voltage induction is bypassed by turned on IGBT. Therefore, the L_s current generates a reverse flux on the core and the core flux reaches zero. Considering the FCL equivalent circuit in Fig. 7, the series windings mutual inductance is negligible and the amount of FCL inductance in the dynamic mode declines to zero. Moreover, in this state, the FCL bypassed inductor has no effect on the smoothing reactors.

Fig. 7. Equivalent circuit in dynamic operation.

In this condition, the voltage drop on the FCL can be described as follows:

$$V_{FCL} = L_p \frac{di_{dc}}{dt} + M \frac{d(i_{dc} - i_r)}{dt} + (R_p i_{dc}) + R_s (i_{dc} - i_r) \quad (5)$$

$$i_r R = L_s \frac{d(i_{dc} - i_r)}{dt} + M \frac{d(i_{dc})}{dt} + R_s (i_{dc} - i_r) \quad (6)$$

By solving (5), the FCL voltage drop will be obtained, where i_r is the IGBT current. In this state, the FCL power loss is the same as in normal operation mode.

In the dynamic state, after fault removal and during the recovery state, the proposed FCL should impose negligible inductance to the line. The FCL limited fault current will be cleared by the HVDC breaker, and after the fault removal, the breaker will be closed again in order to reconnect the HVDC line. In the reconnection state, the current will rise from zero to its rated value. Therefore, FCL recovery time will influence the current signal profile. For this condition, the FCL topology is the same as that in Fig. 7 and, due to its very low equivalent inductance value, the FCL recovery time will be very fast, in the range of milliseconds.

B. Fault Condition Mode

In this mode, a short circuit DC fault occurs. By turning-off the IGBT switch, the current i_r reaches to zero and the high inductance L_p and low inductance L_s are connected in series with the network. The fault current cannot raise immediately. due to a high voltage drop on the series reactors. The equivalent circuit under fault mode is shown in Fig. 8.

Fig. 8. Equivalent circuit in fault condition mode.

The following equations present the voltage drop on FCL during the fault condition:

$$V_{FCL} = (L_p + L_s + 2M) \frac{di_{dc}}{dt} + i_{dc} (R_p + R_s) \quad (7)$$

$$i_{dc} = \frac{V_{FCL}}{(L_p + L_s + 2M)} e^{-(t_{fault} - t_{cle})} + \frac{V_{FCL}}{(R_p + R_s)} \quad (8)$$

Equation (7) presents the FCL voltage drop during the fault. In (8), t_{fault} refers to the time of the fault occurrence and t_{cle} is the time of the fault clearance. In this condition, FCL power loss only depends on the FCL resistance and line current.

IV. CONTROL STRATEGY

Fig. 9 illustrates the HISS-DCRFCL control strategy. In order to control the HVDC system fault current, the line current is sampled, and the two latest samples are divided by the sampling time, as shown in (9). Direct high current in the HVDC line can be sensed by fiber-optic current sensors (FOCSs) as executive measurement devices [33]. The current differential rate is defined as:

$$D_{rate} = \frac{d_{n-1} - d_n}{(1/f)} \quad (9)$$

where d_{n-1} and d_n are the two latest line current samples and f is the sampling frequency.

Fig. 9. HISS-DCRFCL control strategy.

Then, the value obtained from (9) is compared to the reference value in order to detect the fault condition. By comparing the line current amplitude with the reference value, the fault detecting accuracy can be increased. A NOR logic gate creates an output signal for the fault detector block and the pulse is generated for the driving IGBT. Moreover, after the delay of the controlling system and mechanical breaker, the fault can be cleared by an HVDC breaker (in the case the fault is not removed itself). A remote terminal unit (RTU) provides data to the dispatching center to create an auxiliary command for the transient fault in the HVDC system. On the other hand, a signal will be sent by the dispatching center to the fault removal block to reset the FCL IGBT in order to recover FCL and reclose the HVDC breaker.

V. SIMULATION RESULTS

The proposed HISS-DCRFCL is tested by simulation. For the simulations, a point-to-point HVDC line of the CIGRE B4-58 MT- HVDC test system is selected. A 50 km DC line is considered, and the simulation parameters are listed in Table (1). The HVDC line in this study is depicted in Fig. 4(b).

TABLE I
SIMULATION PARAMETERS

Parameter	Description	Value
C	Grid capacitor	80 mF
$L(\text{line})$	Line π model series inductance	50 mH
$C(\text{line})$	Line π model shunt capacitance	0.6 μ F
$L(P)$	FCL primary inductance	2 H
$L(S)$	FCL secondary inductance	10 mH
$R(P)$	FCL primary resistance	0.1 Ω
$R(S)$	FCL secondary resistance	0.01 Ω
R	Series resistance with IGBT	0.04 Ω
$P(\text{Load})$	Active power of the load	1 MW
$R(\text{fault})$	Fault resistance	0.01 Ω
$Z(\text{ac1})$	AC side 1 impedance	0.1+j0.1
$Z(\text{ac2})$	AC side 2 impedance	1+j2
$V(\text{ac1})$	AC system 1 voltage	400kV $\pm$ 5%
$V(\text{ac2})$	AC system 2 voltage	400kV $\pm$ 5%

In this section, the behavior of the proposed HISS-DCRFCL is simulated under normal, dynamic and fault conditions. The proposed HISS-DCRFCL is installed in the selected HVDC line and results are compared to the fault condition in the same point-to-point HVDC system without using the HISS-DCRFCL protection.

A. Simulation Results without Applying the Proposed HISS-DCRFCL

Fig. 10 shows the current and voltage waveform of the

simulated line. The fault is considered to occur at $t_1=52$ ms. The fault type is line-to-ground with resistance (0.1 Ω), 20 km far from the VSC-HVDC Station 2. In order to clarify the line state, at first, the ac grid provides power and the first VSC station operates as a rectifier, while the second VSC station acts as an inverter by injecting power to the second ac network. Fig. 10(a) shows the voltage sag of the AC Side 1 and its harmonic distortion because of the rectifier operation mode of the first VSC-HVDC station. Its peak value declines 55% of the normal value of the network. Fig. 10(b) shows the voltage profile of the second ac network before and after fault occurrence. In this figure, the second ac grid voltage falls to 84% of the network normal voltage. Fig. 10(c) shows the positive HVDC terminal voltage waveform during normal and fault conditions. During the fault, the voltage amplitude decays to 60 kV. Fig. 10(d) shows the phase A current in the AC Side 1 where the fault has occurred at $t_1=52$ ms. The positive part of the current reaches 7 kA and its negative part raises to 2.2 kA. In the same way, the current of the second ac network increases to 980 A, as shown in Fig. 10(e). In addition, Fig. 10(f) shows the current profile of the HVDC line after the fault occurrence. The maximum current of the HVDC line positive terminal reaches to 6.27 kA.

Fig. 10. Simulation results for a fault voltage occurring at 50 ms: (a) AC Side 1 voltage where the fault occurred, (b) AC Side 2 voltage, (c) HVDC line voltage before and after the fault, (d) AC Side 1 current, (e) AC Side 2 current and (f) HVDC line current without applying HISS-DCRFCL.

B. Simulation Results-Applying HISS-DCRFCL

In this section, the effect of applying one HISS-DCRFCL in the positive terminal of the HVDC line is studied. Fig. 11(a) shows the voltage sag of the AC Side 1 while the fault occurs at $t_1=52$ ms. In this condition, the voltage declines to 90% of the nominal voltage, but voltage sag of the second ac network increases because of a current limitation in the first AC grid by HISS-DCRFCL. The harmonic distortion is visible in normal operation and fault condition equally considering the FCL effect. The voltage of the second AC grid is represented in Fig. 11(b) where the harmonic distortion is not visible in this figure due to high power generation in the second grid. In the normal condition, the voltage drop on the FCL is very low and it just depends on the reactor resistance as shown in (1) and (2). This is shown in Fig. 11(c). Moreover, due to the limitation of current flowing to the fault, the HVDC voltage sag reaches a low value, as shown in Fig. 11(c). This is according to the FCL voltage drop (7).

The positive part of the current profile in the AC Side 1 is shown in Fig. 11(d). As shown here, the current is completely limited and its negative part approximately takes no effect. Moreover, the current of the second AC network reaches 1,150 A, as shown in Fig. 11(e). In this simulation, the main profile proves the capability of the HISS-DCRFCL in limiting the fault current in the HVDC, as shown in Fig. 11(f). The fault happens at $t_1=52$ ms, the positive terminal current is increased to 185 A, which is the maximum value of the fault current in the HVDC terminal. Because of the delay of system and IGBT switch lags at $t_2=5$ ms, the IGBT turns off and the high inductance of the DC-reactor FCL limits the fault current, which decays to a very low value with a low slope. This current transition confirms (8). By comparing Fig. 10(d) and Fig. 11(d), it can be concluded that the progress of the fault current limiting is successful. In addition, the voltage drop across the HISS-DCRFCL during normal and fault conditions proves its effectiveness, which is shown in Fig. 11(g).

Fig. 11. Simulation results for a fault voltage occurring at 50 ms: (a) AC side 1 voltage where the fault occurred, (b) AC side 2 voltage of, (c) HVDC line voltage before and after fault, (d) AC side 1 current, (e) AC side 2 current and (f) HVDC line current before and after the fault by applying HISS-DCRFCL, and (g) proposed FCL voltage drop.

C. Voltage Stress across the Switch

In this section, switch voltage stress is presented in several states according to the equivalent circuits in Figs. 6-8. In the normal operation mode, the power switch is in the on state. The FCL inductance does not have any influence on the circuit and the switch voltage is zero. In dynamic situations, the power switch is in the on state and the circuit topology is in normal operation mode. Therefore, again, in this condition, the IGBT voltage is equal to zero. The final state is changing from the steady state to the fault condition mode, where the switch should be turned off and a transient voltage appears in the power switch, as shown in Fig. 12. This voltage stress is equal to the voltage drops across L_s and R_s and because of the low inductance and resistance nature of this part of the FCL, the transient voltage will not be significant. Furthermore, ZnO surge arrester is used as an extra voltage stress protection unit. In Fig. 12, the maximum transient voltage across the switch reaches 190 kV and after the voltage spike, the switch voltage declines to a lower value than the line voltage.

Fig. 12. Voltage stress across the switch.

VI. EXPERIMENTAL RESULTS

In this section, a HISS-DCRFCL laboratory experimental prototype is tested and the results are reported. In the laboratory setup, a single-phase autotransformer is used as an ac source. The output voltage of the autotransformer is connected to a rectifier bridge and its DC output is connected to a DC-link capacitor. In addition, its π model implements the DC line. Obviously, the value of the line shunt capacitor is considerably smaller than the value of converter capacitor. Therefore, these capacitors will not significantly contribute to the faulty situations. The load-side of the DC line is connected to the IGBT-based full bridge inverter and its output feeds the ac load. In this laboratory experimental setup, the proposed HISS-DCRFCL is connected in series with the DC terminal. The suggested FCL includes high inductance coil, IGBT, and a bypass resistance. The controlling structure is built based on a

control diagram, which is shown in Fig. 4, and it is programmed by Node^{TM} and computer coding. Therefore, the fault is applied to the DC line by the solid-state relay and its command is sent by the computer-coded program. Fig. 13 shows the proposed FCL prototype.

Fig. 13. Proposed HISS-DCRFCL laboratory experimental prototype.

The values of the prototype parameters are listed in Table II. A positive terminal to ground fault is considered. The DC current and voltage measurements are carried out with and without HISS-DCRFCL connection to the line.

TABLE II
EXPERIMENTAL PROTOTYPE PARAMETERS VALUES

Param eter	Description	Value
C	Smoothing capacitor of grid	10 mF
$L_{(line)}$	Inductance of line in π modeling	50 mH
$C_{(line)}$	Parallel capacitance of line	10 μ F
$L_{(p)}$	Inductance of FCL primary	2 H
$L_{(s)}$	Inductance of FCL secondary	10 mH
$R_{(p)}$	Resistance of FCL primary	2 Ω
$R_{(s)}$	Resistance of FCL secondary	0.02 Ω
R	Series resistance with IGBT	0.06 Ω
$P(\text{Load})$	Active power of the load	100 W
$R_{(fault)}$	Resistance of terminal to earth	0.1 Ω
$Z_{(ac1)}$	Impedance of AC side 1	0.1+j0.1 Ω
$Z_{(ac2)}$	Impedance of AC side 2	0.1+j0.1 Ω
$V_{(ac1)}$	Voltage of AC system 1	100V $\pm$ 5%
$V_{(ac2)}$	Voltage of AC system 1	100V $\pm$ 5%

Table III lists further information regarding the developed experimental prototype.

TABLE III
EXPERIMENTAL PROTOTYPE TECHNICAL INFORMATION

Equipment	Specification
DC- reactor core	E-I 50 magnetic steel
DC reactor winding	3.14 mm ² wire
Rectifier	Full bridge diode 35A/ 400V

Inverter	Full bridge package IGBT with internal driver, 100V/5A
Fault switch	Mechanical electric relay
Controlling system	Node M32 hardware programed by C
Impedance of source	Toroid coil and resistance
Impedance of line	Series resistance and open-core inductance and electrolyte capacitor
Smoothing	Electrolyte capacitor
Load	100W variable resistance

A. Experimental Test of DC System without Applying HISS-DCRFCL

In the experimental test, the ac input voltage is connected to the full bridge rectifier thorough the autotransformer and its DC terminal is connected to the DC-link capacitor and line impedance. In addition, the flow of power through the DC reactor is transferred to the second AC network by a IGBT H-bridge inverter. The electrical load is connected to the second AC network. In this case, the fault is applied by a solid-state relay switch to the positive DC terminal. The first test result shows signals without using the proposed FCL. The voltage of the AC side 1 and 2 and positive DC-link are measured and reported in Figs. 14(a), (b) and (c), respectively, during normal and fault condition. In Figs. 14(d) and (e) the current of the AC side 1 and 2 before and after the fault is presented, where the AC side 1 feeds the inverter current and the AC side 2 feeds converter in the rectifier mode. The DC signal of the DC line current is shown in Fig. 14(f). The amplitude of DC line voltage is 120 V. After the fault occurrence, the voltage is reduced to a very low value where its amplitude is related to the fault resistance. Normal DC current in the DC link is 1 A. After the fault occurrence, its value is increased to 10 A, while the maximum value of the line current, the rate of current raising and its raising delay depend on the series resistance and inductance of the system and the value of the parallel smoothing capacitors. This large current will cause huge damage to the DC system on the real scale. These experimental results verify and validate the performed simulation results.

Fig. 14. Experimental results without HISS-DCRFCL (a) AC side 1 voltage during normal and fault condition, (b) AC side 1 voltage during normal and fault conditions, (c) dc line voltage before and after fault, (d) AC side 1 current during normal and fault condition, (e) AC side 2 current during normal and fault condition, and (f) dc line current before and after fault.

B. Experimental Test of DC System-Applying HISS-DCRFCL

In this case, the system is equipped with the proposed HISS-DCRFCL. During normal operation, the controlling system turns on the IGBT switch, and equivalent series inductance of the FCL becomes close to zero. During the fault inception, the fault detector circuit detects it after a short delay, consequently, the IGBT is turned-off and fault is limited by increasing the FCL inductance. The voltage and current profiles are shown in Fig. 11 where Figs. 15(a), (b) and (c) show the voltage profile during the fault in AC side 1, 2 and DC-link. In the fault condition, the voltage of the AC sides drops slightly and voltage of DC-link falls to a very low value. Figs. 15(d) and (e) illustrate the current of the first and second AC network during the fault while HISS-DCRFCL is connected to the DC line. Fig. 15(f) shows the HISS-DCRFCL behavior, which is the opposite of the fault current in the DC system, where the DC fault current is limited to less than 0.5 A. These experimental results confirm and validate the reported simulation results. Comparison of Figs. 14(f) and 15(f) proves the appropriate performance of the proposed HISS-DCRFCL. Fig. 15(g) shows the HISS-DCRFCL voltage drop during normal and fault operation modes. In normal operation, the proposed FCL voltage drop is close to zero and, by the IGBT switch operation, its voltage rises and reaches to the peak value of dc line voltage. During the fault condition, this voltage decays with a slight slope. Moreover, it can be observed in Fig. 15(h) that the stress voltage across the IGBT switch, while its first spike reaches to double of the dc line voltage. It means that during the fault period it becomes fixed and equal to the secondary winding voltage. The voltage drop measurement is in complete agreement with the simulation results in Figs. 11(g) and 12.

Fig. 15. Experimental results applying HISS-DCRFCL. (a) AC side 1 voltage during normal and fault condition, (b) AC side 1 voltage during normal and fault condition, (c) DC line voltage before and after fault, (d) AC side 1 current during normal and fault condition, (e) AC side 2 current during normal and fault condition and (f) DC line current before and after fault, (g) voltage drop with the proposed HISS-DCRFCL, and (h) voltage stress across the power electronic switch.

The superiority of the HISS-DCRFCL proposed in this paper is summarized as follow:

- The structure of the proposed FCL is simple. It includes just a DC-reactor and a single power switch.
- It is not relying on superconductive technology.
- In the normal operation mode, the power switch is on and the reactor is bypassed.
- The overall power losses are relatively low, and they depend on the reactor copper loss.
- The proposed FCL is practically applicable to low, medium, and high voltage DC lines.

VII. CONCLUSION

In this paper, a novel high inductance solid-state DC reactor based fault current limiter has been proposed and investigated, which is able to decrease the fault current and protect HVDC lines. Simulation and experimental results have been provided to validate and confirm the capability of the proposed HISS-DCRFCL. During a fault event, the HISS-DCRFCL delay is quite low and it recovers very fast after fault clearance by its solid-state switch. The main contribution of the HISS-DCRFCL is to provide enough time constant and current limiting for proper operation of the HVDC breaker. By limiting the rate of rise of current (RRC) with the proposed FCL, the overvoltage applied to power electronic switches and

line breaker is limited. In order to fully protect a dc transmission line, two HISS-DCRFCL are needed to be installed at its sending and receiving ends.

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