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Zero-Current Switching for the Alternate Arm Converter through On-Load Tap Changers

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Abstract—The combined operation of the two arms of an alternate arm converter (AAC) phase-leg is essential for SM capacitor energy balancing but is limited to a small overlap period. The director switches (DSs) operate alternatively and the overlapping operation of the DSs provides the overlap period. The alternate operation of the two arms leads to arm inductor current interruptions increasing voltage stresses across DSs during normal operation. This paper proposes a coordinated operation of the AAC operating point and transformer on-load tap changers (OLTCs) based on power reference set-points in order to achieve ZCS of the DSs regardless of the AAC operating mode. The coordinated operation utilizes the tap positions of the converter transformer effectively and extends the operating range that offers ZCS of the DSs without additional efforts of circulating current control. Results from an AAC-based HVDC converter model derived from the CIGRE benchmark MMC system demonstrate the effective use of the transformer OLTC to achieve ZCS of the DSs in AACs.

Index Terms—Alternate arm converter (AAC), zero-current switching, multilevel converter, high-voltage direct-current

I. INTRODUCTION

Voltage source converter (VSC)-based high voltage direct current (HVDC) transmission systems [1] have become a proven technology in the modern power systems [2] due to attractive features of the VSCs [3] in contrast to the conventional line-commutated current source converters. The modular multilevel converter (MMC) [4] defines the state-of-the-art amongst multiple VSC topologies and offers unique advantages [5] for HVDC applications. Owing to the large number of voltage levels, the MMC generates near sinusoidal output voltages eliminating the requirement of bulky ac-side harmonic filters. Various types of unipolar and bipolar submodules (SMs) [6] are available for the MMC but the typical MMC is based on half-bridge submodule (HB-SM). The HB-SM based MMC lacks dc-fault tolerant capabilities due to the single polarity output voltage of the unipolar HB-SM. Optionally, bipolar SMs such as full-bridge SM (FB-SM) and cross-connected SM can be used for the MMCs to provide dc-fault tolerance at the cost of increased number of semiconductor devices and losses.

The alternate arm converter (AAC) [7] is an emerging dc-fault tolerant multilevel converter topology. It combines the characteristics of MMC and the two-level converter in a modular VSC topology allowing operation with reduced stored energy in the arms compared to the MMC [8]. Despite the need for a dc-link capacitor, the total stored energy of the AAC

Fig. 1. Three-phase AAC circuit configuration.

remains lower than an equivalent MMC. The inherent energy balancing of the AAC is limited to one operating point called the “sweet-spot” that belongs to the over-modulation range [7]. Hence, fully controllable bipolar SMs, preferably FB-SMs [9], [10] are required for the AAC in order to generate ac voltages greater than the dc-link voltage. When the operating point moves away from the sweet-spot, additional effort is needed for the energy balancing. Utilization of a circulating current and internal current control is essential for energy balancing.

Energy balancing and current control methods [11]–[15] are predominantly based on an “overlap period” between the upper and lower arm director switches (DSs) that consist of series-connected switching devices. The two DSs operate alternatively, similarly to a two-level converter, and provide the overlap period around the zero crossing points of the reference voltage. During the overlap period, a circulating current flows through the phase-leg superimposed to the arm currents depending on the energy imbalance.

Alternating operation of the DSs can lead to interruption of the current through arm inductors increasing the voltage stress on the DSs. Reactive power also affects the arm current interruptions. Hence, zero-current switching (ZCS) of the DSs becomes a primary requirement for the normal operation of the AAC. The existing literature includes detailed studies of ZCS methods based on the resonance of AAC phase-leg circuit con-

figuration during the overlap period [15] and hysteresis current control within a variable overlap period [12]. ZCS operation of the DSs has also been discussed in other AAC current control methods [13], [14]. Moreover, the ZCS operation for the extended-overlap mode of the AAC and the use of snubber circuits to reduce high voltage stress on the DSs are addressed in [16], [17]. In all previous studies, only the inverter mode operation of the AAC has been considered. Therefore, further investigation is needed to provide a comprehensive approach for ZCS of the DSs independent of the operation mode also considering reactive power injection.

The objectives of this paper are: i) to analyze the ZCS conditions for the DSs at near sweet-spot operation without active circulating current control, and ii) to propose a coordinated operation of the transformer on-load tap changer (OLTC) and the AAC operating point based on power references to extend the operating region that provides ZCS of the DSs without additional efforts of circulating current control.

The paper is structured as follows. Section II describes the overview and the operating principles of the AAC. Detailed analysis of the four quadrant operation and the proposed OLTC coordination are presented in Section III. Section IV provides real-time digital simulation results and demonstrates the ZCS performance of the proposed coordinated operation. Section V summarizes the conclusions.

II. THE ALTERNATE ARM CONVERTER

A. Basic Topology and Operation

The three-phase AAC topology is shown in Fig. 1. Each phase-leg contains two arms with N series-connected FB-SMs, one inductor (L), and one DS per arm. The two DSs (DS_u and DS_l) operate during the positive and negative half-cycles of the output voltage:

$$v_a = v_{am} \frac{V_{dc}}{2} = m_a \frac{V_{dc}}{2} \cos(\omega t), \quad (1)$$

respectively, where v_{am} is the normalized reference signal and m_a is the modulation index. Hence, the total arm voltage of the AAC ($\sum_1^N V_C$) is lower than the full dc-link voltage. The two arms of a phase-leg alternatively conduct the total output current:

$$i_a = \hat{I}_a \cos(\omega t + \phi) \quad (2)$$

during the two half cycles of v_a while remaining open for the rest. Therefore, a continuous dc current that regulates the SM capacitor energy is not present throughout the fundamental voltage cycle.

Inherent energy balancing [18] is achieved when the net energy exchange of an arm over each half-cycle is zero. Considering (1) and (2), the exchanged energy in the dc-link E_{dc} and the ac-side E_{ac} are:

$$E_{dc} = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{V_{dc} \hat{I}_a}{2} \cos(\omega t + \phi) d\omega t, \quad (3)$$

and

$$E_{ac} = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{m_a V_{dc} \hat{I}_a}{2} \cos(\omega t) \cos(\omega t + \phi) d\omega t. \quad (4)$$

The net energy absorbed by the SM capacitors within an arm can be determined by (3) and (4) as:

$$\Delta E_{arm} = E_{dc} - E_{ac} = \frac{\pi V_{dc} \hat{I}_a \cos \phi}{4\omega} \left(\frac{4}{\pi} - m_a \right). \quad (5)$$

Eq. (5) shows that the modulation index for natural energy balance (sweet-spot) is $m_a = M_a = 4/\pi$, where ΔE_{arm} becomes zero at this operating point [7].

B. Circulating Current and Overlap Period

At nonsweet-spot operating points ($m_a \neq M_a$), an energy surplus or deficit occurs within the arms. Hence, an overlap period around the zero crossing points of the output voltage is introduced by allowing both DSs of the phase-leg to conduct at the same time. During the overlap period, both arms share the output current (i_a) and a circulating current (i_{circ}) flows through the phase-leg. The overlap operation of the AAC mimics the MMC operation [19] and the arm currents during the overlap period can be expressed as:

$$i_u = \frac{i_a}{2} + i_{circ}, \quad \text{and} \quad (6)$$

$$i_l = \frac{i_a}{2} - i_{circ}. \quad (7)$$

The circulating current characteristics and control dynamics depend on the arm inductance as:

$$v_{diff} = L \frac{d}{dt} i_{circ}, \quad (8)$$

v_{diff} is the differential voltage applied across the arm inductance.

During the overlap period, the two arms of a phase-leg should generate the output voltages collectively to avoid output voltage distortions [14]. Therefore, the limitation for the maximum overlap period is set by the redundant voltage of an arm [12],

$$V_r = NV_C - \frac{V_{dc}}{2} \quad (9)$$

where, V_C is the nominal SM capacitor voltage. Considering (9), the maximum overlap period ($\hat{t}_{ov}$) [20] can be expressed as:

$$\hat{t}_{ov} = \frac{2}{\omega} \sin^{-1} \left(\frac{M_a - 1}{m_a} \right). \quad (10)$$

The overlap angle ($\omega \hat{t}_{ov}$) for the normal operation of the AAC in “short-overlap” mode is typically in the range of $15^\circ \sim 18^\circ$ [21]. Operation with an overlap angle greater than 60° is also possible, in an operation mode referred as “extended-overlap” [22].

Once an overlap period is employed, the circulating current is defined based on (8) to balance the nonsweet-spot energy offset depending on the natural differential voltage generated by the difference of upper and lower arm SM capacitor voltage ripples. Moreover, active circulating current control methods [11]–[15] can be applied to achieve more accurate energy regulation. The duration of overlap period may differ depending on the requirements of circulating current control methods but, should be maintained below the maximum ($\hat{t}_{ov}$) in order to not impact the output voltage quality significantly.

C. Zero Current Switching of the DSs

Based on (6) and (7), the circulating current modifies the arm currents during the overlap period. Moreover, different active (reactive) power set-points invert (shift) the arm currents depending on the power factor. Hence, there may be non-zero arm currents at the time the DS opens. As the DSs consist of series-connected switches, the non-zero switching current (hard switching of the DSs) increases the power losses. Importantly, due to the presence of the arm inductance, hard switching produces high-voltage stress across the DSs. Therefore, ZCS of the DSs should be ensured. Alternatively, the voltage stress caused by hard switching can be maintained in a contained manner using snubber circuits [16].

III. OLTC COORDINATION FOR ZCS OF THE DSs

Current studies of ZCS focus on the inverter mode operation of the AAC at unity power factor. As the AAC energy is inherently balanced only at the sweet-spot [12], [15], the sweet-spot can be considered as the nominal operating point. Moreover, the energy deviation around the sweet-spot is small so that the effort for energy balancing (i.e. the amount of energy that exchanged by the circulating current) at near sweet-spot is lower. Depending on the power set-points, the output voltage of the AAC varies around the nominal value due to the effect of equivalent impedance of the grid-connection. Hence, the effect of four-quadrant operation on the modulation index should be further investigated in order to identify the conditions for ZCS of the DSs.

A. Conditions of Inverter and Rectifier Modes for ZCS

The fundamental requirement to achieve ZCS of the DS is to divert the current flow of the switches through the anti-parallel diodes before the DS opens. Based on this and the convention of Fig. 1, the conditions of upper and lower arm currents for ZCS are $i_u \leq 0$ and $i_l \geq 0$, respectively. Given that the output current direction is positive ($i_a > 0$) and negative ($i_a < 0$) for inverter and rectifier operation modes, respectively, the arm currents of (6) and (7) satisfy the conditions for ZCS only if at least $i_{circ} < 0$ before the DS opens.

A negative circulating current ($i_{circ} < 0$) around the zero-crossing points of v_a is always in the direction that discharges the inserted SM capacitors. Therefore, if the AAC is set to operate with an stored energy surplus ($\Delta E_{arm} > 0$) regardless of the operating mode, i_{circ} is always naturally defined to discharge the excess energy as per the explanations of Section II-B. Based on (5), the conditions of the operating point (m_a) for ZCS can be written as:

$$m_a < M_a = \frac{4}{\pi}; \quad \text{for inverter mode } (P^* < 0), \text{ and} \quad (11)$$

$$m_a > M_a = \frac{4}{\pi}; \quad \text{for rectifier mode } (P^* > 0). \quad (12)$$

B. Operating Point for Different Power Set-Points

A grid-connected circuit configuration of the AAC is shown in Fig. 2. The grid-connected operation incorporates the grid-impedance ($Z_g = R_g + jX_g$) and the transformer-impedance

Fig. 2. Grid-connected AAC.

Fig. 3. Variation of the operating point for four quadrant operation.

($Z_{tf} = R_{tf} + jX_{tf}$) between the AAC output voltage and the grid voltage. Therefore, the operating point of the AAC varies depending on different power set-points. Considering the equivalent impedance ($Z_{eq} = Z_g + Z_{tf} = R_{eq} + jX_{eq}$) at the primary side and the turns-ratio $n_{tf}\sqrt{3} = V_{pri}/V_{sec}$ of the transformer, the operating point can be calculated as:

$$m_a = \frac{2\sqrt{2}}{3V_{dc}n_{tf}} |\vec{v}_g - \vec{i}_g \cdot \vec{Z}_{eq}|. \quad (13)$$

Substituting vectors of (13) with terms from the phasor diagram of Fig. 2, (13) can be expressed as:

$$m_a = \frac{2\sqrt{2}}{3V_{dc}n_{tf}} \left[\left(V_g - \frac{R_{eq}P^*}{V_g} - \frac{X_{eq}Q^*}{V_g} \right)^2 + \left(-\frac{X_{eq}P^*}{V_g} - \frac{R_{eq}Q^*}{V_g} \right)^2 \right]^{\frac{1}{2}} \quad (14)$$

where, P^* and Q^* are the power references.

Based on (14) and fixing the apparent power at the rated value, variation of the operating point (modulation index) with the phase angle of the grid current is shown in Fig. 3 for the four-quadrant (① - ④) operation. Fig. 3 demonstrates that the operating point deviates above (below) M_a depending on the negative (positive) reactive power. The range of operating points highlighted with green (predominantly in quadrants

Fig. 4. Utilization of the transformer tap settings to extend the ZCS of DSs.

② and ④ agree with the conditions of (11) and (12) for ZCS. Operation at outside that range (highlighted with red, predominantly in ① and ③) requires additional compensation to change the operating point so that the requirements of (11) and (12) can be satisfied.

C. Proposed OLTC Coordination

HVDC transformers are typically equipped with OLTCs [23]. Therefore, the transformer tap settings can be utilized effectively to compensate for the operating point of Fig. 3 in order to meet the ZCS conditions of (11) and (12), leading to a coordinated operation of the AAC and OLTC. Considering that the transformer has an OLTC range of $\pm 10\%$ with steps of 2.5% [23], Fig. 4 shows the range of operating points that can be set by different OLTC settings (dashed blue lines).

For a particular active/reactive power set-point at rated apparent power, the uncompensated operating point can be determined by (14) and compared with M_a for the ZCS conditions of (11) and (12). If the uncompensated operating point does not meet the ZCS conditions, the required OLTC setting can be selected based on Fig. 4 and the ac-grid phase angle in order to shift the operating point satisfying (11) and (12). Otherwise, the OLTC is kept unchanged at the default setting (0%). The conditions of (11) and (12) cannot be reached for full/predominant reactive power operation of the AAC even with the extreme settings of the OLTC. As typical HVDC converters operate with a power factor close to unity, this limitation does not affect the operation within typical range of power set-points.

Extension of the ZCS operation point based on the proposed OLTC coordination is illustrated using a power set-point ($Q^* = 0.4P^*$, $S = 800\text{MVA}$) in quadrant ① (Fig. 4). The

TABLE I
AAC SIMULATION PARAMETERS

Rated Power (S)	800 MVA
DC-Voltage (V_{dc})	400 (± 200) kV
Number of SMs/arm (N)	255
SM Capacitance (C)	11.5 mF
SM Capacitor Voltage (V_C)	1 kV
Arm Inductance (L)	0.013 p.u.
Transformer ratio (n_{tf})	0.703
Transformer Leakage Inductance	0.09 p.u.
Transformer Resistance	0.003 p.u.
AC Voltage	380 kV
Short-circuit Power	30 GVA

uncompensated operating point (marked with a red dot) is below M_a and hard-switching occurs in the DSs. According to the conditions of (11) and (12), ZCS operation can be provided to DSs if the operating point can be moved above M_a . The three positive settings of the OLTC (marked with green dots) provide the option to operate the AAC slightly above the sweet-spot offering ZCS for the DSs. Hence, the proposed coordination between the transformer OLTC and the AAC operating point extends the ZCS operation of the DSs, without the support of circulating current control.

IV. SIMULATION RESULTS

In order to demonstrate the effectiveness of the proposed OLTC coordination method, a grid-connected AAC model with 255 SMs per arm is used. The AAC simulation model is derived from the benchmark model of [20] redefining the nominal operating point and developed in a real-time digital simulator. Figs. 1 and 2 show the grid-connected AAC circuit configuration and the parameters are given in Table I.

ZCS of the DSs for inverter mode operation is extensively discussed in the existing literature. Also, the analysis of Fig. 4 shows that a significant range of operating points for the typical inverter operation of the AAC (quadrant ②) falls within the proposed OLTC coordination. It is the opposite for typical rectifier operation of the AAC (quadrant ①) requiring OLTC coordination to compensate for the operating point. Therefore, the rectifier operation is the focus of all simulation results.

A. Rectifier Mode Operation without OLTC Coordination

The power references are set as $P^* = 742.8\text{ MW}$ and $Q^* = 297\text{ MVar}$ ($Q^* = 0.4P^*$). The OLTC setting is kept at 0%. The ac-grid voltages and currents are shown in Fig. 5. Fig. 6 shows the arm currents and SM capacitor voltages of phase- a . The AAC operates in quadrant ① and the operating point is below M_a . Hence, DSs are subjected to hard switching. Figs. 6(a) and (b) show interruptions of the upper and lower arm currents verifying the analysis of Section III. The generated voltage spikes of Fig. 5(a) due to hard switching affect the converter output voltage which can also slightly affect the ac-grid voltage. However, the ac-grid voltages and

Fig. 5. AC-grid-side results for the rectifier mode operation without OLTC coordination: (a) three-phase ac grid-voltages and (b) three-phase ac grid-currents.

Fig. 7. AC-grid-side results for the rectifier mode operation with OLTC coordination: (a) three-phase ac grid-voltages and (b) three-phase ac grid-currents.

Fig. 6. Results of phase *a* for the rectifier mode operation without OLTC coordination: (a) upper arm current, (b) lower arm current, and (c) upper and lower arm SM capacitor voltages.

Fig. 8. Results of phase *a* for the rectifier mode operation with OLTC coordination: (a) upper arm current, (b) lower arm current, and (c) upper and lower arm SM capacitor voltages.

currents are within the grid standards. SM capacitor voltages of Fig. 8(c) are also regulated to the reference.

B. Rectifier Mode Operation with OLTC Coordination

In order to provide the ZCS for the DSs, the proposed OLTC coordination is applied maintaining the same operating conditions of Section IV-A. The OLTC is set to +7.5% based on Fig. 4 to move the operating point above the sweet-spot. Fig. 7 shows the ac-grid voltages and currents. The ac-grid voltages and currents are within the grid standards. As the proposed OLTC coordination provides ZCS for DSs, the effect of converter output voltage distortions on the ac-grid voltages is reduced. Figs. 8(a) and (b) show the arm currents. The upper

and lower arm currents become zero when the DSs open owing to the application of the proposed OLTC coordination. The SM capacitor voltages of Fig. 8(c) are also regulated to their reference.

For a particular set of power set-points, there can be multiple OLTC settings that provides ZCS of the DSs. Fig. 9 shows a comparison of the upper arm currents without OLTC coordination and the three OLTC settings of Fig. 4. All three OLTC settings (Fig. 9(a), (b), and (c)) ensure the ZCS of DSs. As the OLTC setting increases the output voltages are also increased. Hence, the peak arm current decreases reducing the conduction losses of the arm. The results demonstrate the effectiveness of the proposed OLTC coordination to achieve

Fig. 9. Comparison of the upper arm current for different settings of OLTC at $Q^* = 0.4P^*$: (a) OLTC=0%, (b) OLTC=+5%, (c) OLTC=+7.5%, (d) OLTC=+10%.

ZCS of the DSs by effective utilization of OLTC settings, considering the rectifier mode operation of the AAC with reactive power injection.

V. CONCLUSION

The AAC is an emerging dc-fault tolerant converter topology and a potential topology for future multiterminal dc networks. The zero-current switching (ZCS) of the director switches (DSs) is one of the main concerns of the AAC and lacks the detailed analysis considering both inverter and rectifier operation with reactive power injection. This paper analyzes and derives an operating range to achieve ZCS of the DSs without applying an active circulating current control method, and proposes a coordinated operation of AAC and OLTC by effectively utilizing tap positions of the HVDC transformer. The effectiveness of the proposed OLTC coordination method is verified using real-time digital simulation results based on an RTDS.

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