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An Inverted Ring Oscillator Noise-Shaping Time-to-Digital Converter With In-Band Noise Reduction and Coherent Noise Cancellation

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Abstract—This article presents a noise-shaping time-to-digital converter (TDC) based on an inverted ring oscillator (IRO). By inverting the oscillation direction, the proposed IRO-TDC achieves quantization error and mismatch noise shaping, in-band noise reduction, coherent noise cancellation, and low disturbance to power supply at the same time. A noise model is proposed to analyze the noise performance of the proposed TDC, and to compare its noise with TDCs based on gated ring oscillator (GRO) and switched ring oscillator (SRO). An IRO-TDC prototype is fabricated in a 65 nm CMOS technology to verify the proposed IRO technique and noise model. With a sampling rate of 200 MS/s, the TDC achieves an integrated noise of 196 fs_{rms} in a 3 MHz bandwidth with a constant power dissipation of 13.2 mW. The measured coherent noise cancellation ratio is up to 36.4 dB. To the best of our knowledge, this is the first demonstration of an oscillator utilizing oscillation inversion for noise reduction and coherent cancellation to protect the TDC from power supply noise, ground noise, and substrate noise. Due to its noise cancellation and low disturbance to power supply, the proposed IRO technique also alleviates the design complexity of power supply in future TDC applications.

Index Terms—CMOS digital phase-locked loop (DPLL), controlled oscillator-based time-to-digital converter (TDC), gated ring oscillator (GRO), inverted ring oscillator (IRO), noise model, noise shaping, coherent noise cancellation, power noise rejection, switched ring oscillator (SRO).

I. INTRODUCTION

IN CIRCUIT designs with smaller feature size, time and digital information are more robust compared with voltage and current information. As the bridge from time domain

to digital domain, time-to-digital converters (TDCs) have recently gained much attention from researchers. TDCs are widely used in applications that need to measure precise time information, including time-of-flight (ToF) applications, digital phase-locked loops (DPLLs) and analog-to-digital converters (ADCs) [1]. Thanks to recent developments in low-noise TDCs, DPLLs have achieved improved noise performance [1]–[4]. TDCs for the DPLL application will be discussed in this article. In a conventional DPLL, a TDC is employed to detect the phase error between the reference clock and the feedback clock [4], and it limits the in-band phase noise performance [5]. Based on [6], the single-sided DPLL in-band phase noise can be expressed as

$$\mathcal{L}(f) = 2 \cdot |2\pi f_{PLL} G(f)|^2 S_{TDC}(f), \quad (1)$$

where f_{PLL} , $G(f)$, and $S_{TDC}(f)$ denote the DPLL output frequency, closed-loop transfer function of the DPLL, and the double-sided TDC noise spectrum, respectively. Since a wide-bandwidth PLL can provide wide data modulation bandwidth, large suppression of oscillator phase noise, and short settling time, it is preferred in modern communications or required in some scenarios [7]. Accordingly, the in-band noise $S_{TDC}(f)$ limited by the TDC becomes more important to the overall DPLL noise performance. In addition, its operation speed must be high for the high speed DPLL; while its input range must be wide for the different reference frequencies and division ratios. Therefore, the design challenges of TDC for the high performance DPLL application are low noise, high operation speed, and wide input range.

Among various TDC types, oscillator-based TDCs have been reported to achieve low in-band noise [8]–[14]. Fig. 1 shows a general structure and the development history of this TDC family. In this type of TDC, an oscillator converts the input time domain information into the oscillator's output phase, and a phase processor digitizes the output phase and calculates the final digital output to represent the input time interval. In early designs, free-running oscillators (without being controlled) were used to scramble and reduce the impact of quantization error and delay mismatch [20], [21]. Later, to further reduce the in-band noise, gated ring oscillator (GRO) was proposed to shape the quantization error and delay mismatch with a high-pass transfer function [4], [6], [8]–[11]. Since then, the concept of noise shaping using gated oscillator

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Fig. 1. (a) General structure and (b) development of oscillator-based TDCs.

has been implemented through many structures such as relaxation oscillator [12], charge-pump oscillator [13], [14], more complicated 2-dimensional GRO [15]–[17], gateable Vernier ring oscillator [18], and GRO-MASH structure [19]. In summary, during operation, these oscillators either oscillate with a fixed frequency or freeze the oscillation upon a *Stop* rising edge. In contrast, a switched ring oscillator (SRO) changes to a low oscillation frequency upon the *Stop* rising edge to achieve noise shaping [22]. Furthermore, GRO and SRO can be combined to realize more complicated processing [23]. Due to the noise shaping characteristic, quantization error and mismatch in these controlled oscillator-based TDCs have negligible contribution to the in-band noise.

However, the phase noise of the controlled oscillator, even after being noise shaped, dominates the TDC in-band noise spectrum. Moreover, other noises (e.g. power supply noise, ground noise, substrate noise, etc.) can couple into the oscillator and transform into oscillator phase noise, degrading the TDC noise performance. Besides, a GRO or SRO draws different supply current during their two operation modes. As a result, during each measurement cycle, these oscillators disturb the power supply periodically and generate interference to the power supply and other circuits.

In this article, we present a noise-shaping TDC technique based on an inverted ring oscillator (IRO) that can achieve in-band noise reduction, a unique coherent noise cancellation, and low disturbance to power supply at the same time. To explain such characteristics, a general noise model for GRO-, SRO- and IRO-TDCs is presented. This model evaluates the impact of various noise sources and predicts the total TDC output noise. Theoretical calculation for IRO coherent noise cancellation ratio is also provided. With a sampling rate of 200 MS/s, measurement result shows a low integrated noise of 196 fs_{rms} in a 3 MHz bandwidth with a constant power dissipation of 13.2 mW. Moreover, a measurement technique for coherent noise cancellation is demonstrated, through which a noise cancellation ratio up to 36.4 dB is obtained.

Fig. 2. Phase-time plot of GRO, SRO and IRO during one measurement cycle.

Fig. 3. Timing diagram of GRO, SRO, and IRO.

An overview of this article is as follows. In Section II, we briefly introduce the operation of the controlled oscillator based TDCs and describe the proposed general noise model in detail. Section III provides details of an IRO-TDC implementation. Section IV provides measurement results of the IRO-TDC prototype. Finally, a conclusion is drawn in Section V.

II. NOISE MODEL FOR XRO-TDCs

For the sake of simplicity, the GRO, SRO and IRO are uniformly named as XRO in the following discussion. Fig. 3 illustrates the operation of different XROs. Upon a *Start* rising edge, the *Control* signal sets the XRO to Mode 1, and the XRO oscillates regardless of the XRO type. When a *Stop* rising edge is received after a time interval T_{in} , the XRO is set to Mode 2. The operation of this mode depends on the oscillator types. A GRO freezes its oscillation. In contrast, an SRO switches to a lower frequency. For the proposed IRO, the oscillation direction is inverted without changing the absolute frequency. Later, the next *Start* rising edge will change the oscillator from Mode 2 to Mode 1, and the next time interval T_{in} begins.

Fig. 2 illustrates how the phase changes during an XRO-TDC measurement cycle. Upon a *Start* rising edge, the oscillation begins with a frequency ω_0 at the last phase $\phi_{XRO,n-1}$, until a *Stop* rising edge arrives and the oscillation frequency changes to $x\omega_0$, where the value of x depends on the XRO type and $x \neq 1$, as shown in the figure. For

Fig. 4. Phase skew of an XRO.

GRO-TDC, $x = 0$; for SRO-TDC, $0 < x < 1$; for IRO-TDC, $x = -1$. x can be smaller than -1, but considering the feasibility, simplicity and better coherent noise rejection performance as will be discussed later, we choose $x = -1$ for IRO-TDC.

At the next *Start* rising edge, the final phase $\phi_{XRO,n}$ is captured. At the same time the frequency changes back to ω_0 and the next measurement cycle begins. Since it is physically impossible to switch the XRO ideally from one mode to the other instantaneously, a phase skew error ϕ_{skew} is introduced to the XRO phase when the mode is changed. This effect is illustrated in Fig. 4. During this cycle, the total phase increment is

$$\begin{aligned} \Delta\phi_{XRO} &= \omega_0 T_{in} + x\omega_0(T_s - T_{in}) + \phi_{skew} \\ &= (1-x)\omega_0 T_{in} + x\omega_0 T_s + \phi_{skew}, \end{aligned} \quad (2)$$

where T_s is the sampling period and T_{in} is the input time interval to be measured. Note that although the XRO experiences two mode switches in one measurement cycle, they are combined as one ϕ_{skew} for easier analysis.

Fig. 5(a) depicts a model of XRO-TDCs. An XRO-TDC converts the time domain input T_{in} into integrated XRO phase. Added with the XRO phase noise $\phi_{n,XRO}$, the XRO phase ϕ_{XRO} is then quantized and differentiated into digital output D_{out} . Therefore, all analog noise sources can be analyzed in phase domain. The XRO phase is digitized as D_ϕ with a minimum distinguishable phase step of ϕ_{stage} and a normalized quantization error Q_E . The final TDC output D_{out} is obtained by differentiating D_ϕ . The phase step ϕ_{stage} is related to the ring oscillator stage delay T_{stage} by

$$\phi_{stage} = \omega_0 T_{stage}. \quad (5)$$

According to the model, the final TDC output can be expressed as (3), shown at the bottom of the next page. Noise shaping of oscillator phase noise and quantization error is clearly seen. Factor $(1-x)/T_{stage}$ is the gain from T_{in} to D_{out} , i.e. the TDC gain.

To evaluate the impact of the noise sources in terms of input-referred time noise $T_{n,in}$, Fig. 5(b) shows an equivalent signal flow of the XRO-TDC. Accordingly,

$$D_{out} = (T_{in} + T_{n,in}) \cdot \frac{1-x}{T_{stage}}. \quad (6)$$

By equating (3) and (6), the input-referred noise can be expressed as (4), shown at the bottom of the next page. Since T_s is fixed, the first term in (4) can be regarded as a constant offset and does not cause noise. With $S_{n,skew}$, $S_{n,XRO}$, and

$S_{n,QE}$ denoting the power spectrum density (PSD) of noise contributions from skew error, XRO phase noise, and quantization error, the PSD of $T_{n,in}$ is thus

$$S_{n,in} = S_{n,skew} + S_{n,XRO} + S_{n,QE}. \quad (7)$$

Next, we will discuss the impact of each noise source.

A. Quantization Error

According to Eq. (6) and (7), the input-referred noise caused by quantization error is

$$S_{n,QE}(f) = S_{QE} \cdot \left(\frac{T_{stage}(1-z^{-1})}{1-x} \right)^2, \quad (8)$$

where S_{QE} denotes the noise PSD of normalized quantization error Q_E . The quantization error stems from the finite delay per stage. Assuming a random input, it has a stochastic distribution and appears as a white noise with level $S_{QE} = 1/12f_s$ in the double-sided frequency spectrum. Substituting z^{-1} with $e^{-j2\pi f T_s}$ according to discrete-to-continuous time transformation, the quantization noise PSD is

$$S_{n,QE}(f) = \frac{1}{12f_s} \left(\frac{T_{stage}}{1-x} \right)^2 \left| 1 - e^{-j2\pi f T_s} \right|^2. \quad (9)$$

Total in-band noise power is therefore calculated by integrating $S_{n,QE}(f)$ within the signal bandwidth f_{BW} . Assuming $f_{BW} \ll f_s$, the in-band noise power is

$$\sigma_{QE,rms}^2 \approx \frac{2}{9} \left(\frac{\pi T_{stage}}{1-x} \right)^2 \left(\frac{f_{BW}}{f_s} \right)^3. \quad (10)$$

This reveals that an IRO (i.e. $x = -1$) reduces the in-band quantization noise by 6 dB compared with a GRO ($x = 0$) because of the factor $(1-x)^{-2}$, although their output quantization noise are the same. For example, assuming a normal T_{stage} of 30 ps in the given process and a sampling rate of 200 MS/s, the integrated noise in a 3 MHz bandwidth is 82 f_{rms} in a GRO but merely 41 f_{rms} in an IRO.

In real circuits, the stage delay mismatch can be regarded as another random quantization error. Hence, it has negligible impact to the final in-band noise due to the same noise shaping.

B. Skew Error

According to Eq. (6) and (7), the input-referred noise caused by skew error is

$$S_{n,skew}(f) = S_{\phi_{skew}} \cdot \left(\frac{1}{\omega_0(1-x)} \right)^2, \quad (11)$$

where $S_{\phi_{skew}}$ denotes the PSD of the phase skew, ϕ_{skew} . The physical reasons for skew error vary with the mechanism and implementation of the XRO. In summary, they cause a deviation from the ideal phase each time when the XRO changes its mode. The deviation depends on the XRO instantaneous phase ϕ_{XRO} . Function $\phi_{skew}(\phi_{XRO})$ can be obtained through simulation. Assuming a random input, this phase skew is also scrambled, thus $S_{\phi_{skew}}$ appears like a white noise. Calculation of $S_{\phi_{skew}}$ depends on the distribution of $\phi_{skew}(\phi_{XRO})$ and is

Fig. 5. (a) Proposed noise model for XRO-TDCs, and (b) its equivalent signal flow diagram where impact of all noises is represented by an input-referred noise, $T_{n,in}$.

beyond the scope of this article. For simplicity, an estimation of

$$S_{\phi_{skew}} = (\phi_{skew,max} - \phi_{skew,min})^2 / 12f_s \quad (12)$$

is adopted. The in-band noise power is thus calculated by integrating $S_{n,skew}(f)$ within the signal bandwidth,

$$\sigma_{skew,rms}^2 = \frac{(\phi_{skew,max} - \phi_{skew,min})^2}{12f_s} \cdot \frac{2f_{BW}}{(1-x)^2 \omega_0^2}. \quad (13)$$

For example, if $(\phi_{skew,max} - \phi_{skew,min}) = 0.015$ rad, $f_s = 200$ MHz, and XRO frequency is 600 MHz, the integrated noise within a 3 MHz bandwidth is 99 fs_{rms} in an IRO.

Besides noise, the skew error also leads to dead-zones in the DC transfer curve under some input conditions. If the input is nearly constant or sweeping very slow, the skew error may not be properly scrambled. The IRO may be locked by the injection of periodic signals, resulting in an unchanged output code. According to the appendix, the dead-zone width can be expressed as

$$T_{dz,XRO} = \frac{\phi_{skew,range}}{(1-x)\omega_0}, \quad (14)$$

where $\phi_{skew,range}$ represents the dead-zone range. Note that a constant or slowly sweeping input is an extreme case, and the dead-zones will disappear if normal input signal is applied. For example, in fractional- N digital PLLs, the input time is quickly and sufficiently dithered by DSM. Under such condition, a dead-zone should not occur.

C. Oscillator Phase Noise

According to Eq. (6) and (7), the input-referred noise caused by oscillator phase noise is

$$S_{n,XRO}(f) = S_{\phi_{n,XRO}} \cdot \left(\frac{1-z^{-1}}{\omega_0(1-x)} \right)^2, \quad (15)$$

where $S_{\phi_{n,XRO}}$ denotes the double-sided PSD of the oscillator phase noise.

Fig. 6. Phase noise contribution comparison among GRO, SRO, and IRO.

Fig. 7(a) shows a model for oscillator phase noise. Since the XRO operates in two modes, it can be modeled as two independent oscillators, i.e. OSC₁ with phase noise $S_{\phi_{n,XRO1}}(f)$ and OSC₂ with $S_{\phi_{n,XRO2}}(f)$. The XRO operates as OSC₁ and OSC₂ for durations T_{in} and $(T_s - T_{in})$ respectively, during which they contribute their own noise power to the XRO phase. Thus, assume that harmonics of the sampling frequency is not at the vicinity of IRO oscillation frequency which is true in our design, and the equivalent XRO phase noise is given by

$$S_{\phi_{n,XRO}}(f, T_{in}) = S_{\phi_{n,XRO1}}(f) \left(\frac{T_{in}}{T_s} \right) + S_{\phi_{n,XRO2}}(f) \left(\frac{T_s - T_{in}}{T_s} \right). \quad (16)$$

Discussion on $S_{\phi_{n,XRO1}}(f)$ and $S_{\phi_{n,XRO2}}(f)$ varies with XRO type. A GRO does not generate any noise after the Stop edge, yielding $S_{\phi_{n,GRO2}}(f) = 0$. This reveals a T_{in} -dependent in-band noise in a GRO-TDC. An SRO also exhibits this dependence due to its different $S_{\phi_{n,SRO1}}(f)$ and $S_{\phi_{n,SRO2}}(f)$. However, this dependence on T_{in} is inherently absent in an IRO-TDC if its OSC₁ and OSC₂ share the same structure and component size, hence the same noise profile, i.e., $S_{\phi_{n,IRO1}}(f) = S_{\phi_{n,IRO2}}(f)$.

Fig. 6 illustrates a comparison among $S_{n,XRO}(f)$ in GRO, SRO, and IRO, assuming they have the same oscillation

$$D_{out} = T_{in} \cdot \frac{1-x}{T_{stage}} + T_s \cdot \frac{x}{T_{stage}} + \frac{\phi_{skew}}{\omega_0 T_{stage}} + \frac{\phi_{n,XRO}(1-z^{-1})}{\omega_0 T_{stage}} + Q_E (1-z^{-1}) \quad (3)$$

$$T_{n,in} = T_s \cdot \frac{x}{1-x} + \frac{\phi_{skew}}{\omega_0(1-x)} + \frac{\phi_{n,XRO}(1-z^{-1})}{\omega_0(1-x)} + \frac{Q_E T_{stage}(1-z^{-1})}{1-x} \quad (4)$$

Fig. 7. XRO phase noise model, (a) shows a general model for XRO phase noise power signal flow, and (b) shows a unique model for IRO coherent noise amplitude signal flow.

frequency ω_0 , Mode 1 phase noise $S_{\phi_n,XRO1}$, and sampling rate f_s . Within the signal bandwidth f_{BW} , $S_{\phi_n,XRO1,2}$ may be dominated by the $1/f^3$ noise and $1/f^2$ noise, hence $S_{\phi_n,XRO}(f)$ contains $1/f$ and flat profiles due to the noise shaping. Both the GRO and the SRO have the maximum phase noise contribution when $T_{in} = T_s$, and the minimum contribution when $T_{in} = 0$. Note that when $T_{in} = 0$, a GRO does not oscillate and has no phase noise contribution. In contrary, the IRO phase noise contribution is constant and 6 dB lower than the maximum value of the GRO.

Total in-band noise can be calculated by integrating $S_{\phi_n,XRO}(f)$ within the signal bandwidth. Assuming $f_{BW} \ll f_s$, we have

$$\sigma_{PN,rms}^2 \approx \left(\frac{2\pi}{f_s \omega_0 (1-x)} \right)^2 \int_{-f_{BW}}^{f_{BW}} S_{\phi_n,XRO} f^2 df. \quad (17)$$

Assuming the two oscillators are with the same conditions, the ratio of TDC noise between GRO and IRO-TDCs can be derived from Eq. (16) and (17):

$$\frac{\sigma_{PN,rms,GRO}}{\sigma_{PN,rms,IRO}} = 2 \sqrt{\frac{T_{in}}{T_s}}. \quad (18)$$

As illustrated in Fig. 6, its maximum ratio is 2 (or 6 dB). For example, considering only the $1/f^2$ phase noise in a 600 MHz XRO, if the XRO has a double-sided phase noise of -93 dBc/Hz at 1 MHz offset, when sampled at 200 MS/s, the maximum integrated noise in 3 MHz bandwidth is 457 fs_{rms} for a GRO-TDC (assume $T_{in} = T_s$) and 228 fs_{rms} for an IRO-TDC. As T_{in} decreases, $\sigma_{PN,rms,GRO}$ becomes small. When $T_{in} = 0.25T_s$, GRO-TDC's noise contributed by oscillator's phase noise is equal to IRO-TDC's one. If $T_{in} = 0.1T_s$, with the same conditions mentioned above, the integrated noise of GRO-TDC is only 144 fs_{rms}. T_{in} cannot be 0 otherwise the oscillator does not work. Compared with the quantization noise and the skew noise, the contribution from the XRO phase noise is dominating the in-band noise performance.

D. IRO Coherent Noise Cancellation

A unique capability of coherent noise cancellation in IRO can be revealed by taking the model in Fig. 7 (b). Coherent noise, denoted as $\phi_{n,coh}(f)$, refers to the phase noise element caused by noise sources with unchanged transfer function to both IRO oscillation directions, such as power supply noise, ground noise, substrate noise, etc. Such noise sources affect the IRO frequency in both oscillation directions. Due to the nature of oscillation inversion, their impacts can be cancelled

TABLE I
POST-LAYOUT SIMULATION RESULTS OF THE MULTI-PATH IRO

Characteristics		Values
Frequency		665 MHz
Power		5 mW
T_{stage}		16 ps
Raw resolution		8 ps
$\phi_{skew,max} - \phi_{skew,min}$		17 mrad
Skew noise	1 MHz BW	58 fs _{rms}
	3 MHz BW	100 fs _{rms}
Phase noise	1 MHz BW	106 fs _{rms}
	3 MHz BW	116 fs _{rms}
Skew & phase noise	1 MHz BW	121 fs _{rms}
	3 MHz BW	153 fs _{rms}

out to some extent. Assuming the frequency of the coherent noise is much lower than f_s , the PSD of their contribution to XRO phase noise is

$$\begin{aligned} S_{\phi_n,coh,XRO} \left(f, \frac{T_{in}}{T_s} \right) &= \left(\phi_{n,coh}(f) \left(\frac{T_{in}}{T_s} - \frac{T_s - T_{in}}{T_s} \right) \right)^2 \\ &= S_{\phi_n,coh}(f) \left(\frac{2T_{in}}{T_s} - 1 \right)^2, \end{aligned} \quad (19)$$

where $S_{\phi_n,coh}(f)$ denotes the PSD of coherent noise. Compared with incoherent oscillator noises in (16), the noise amplitude rather than the noise power is used in the summation of the two modes. Eq. (19) reveals the fact that a slow and coherent impact on the XRO phase can be self-cancelled, depending on value of T_{in}/T_s . Specially,

$$S_{\phi_n,coh,XRO} \left(f, \frac{T_{in}}{T_s} \right) = \begin{cases} S_{\phi_n,coh}(f), & T_{in}/T_s = 0 \text{ or } 1 \\ 0, & T_{in}/T_s = 1/2 \end{cases} \quad (20)$$

refer to no cancellation and maximum cancellation, respectively. To evaluate this cancellation effect, we can define a phase noise rejection ratio (PNRR) as

$$\begin{aligned} PNRR &= 10 \log \left(\frac{\text{noise power without cancellation}}{\text{noise power with cancellation}} \right) \\ &= 20 \log \left| \frac{1}{2T_{in}/T_s - 1} \right|. \end{aligned} \quad (21)$$

This characteristic is similar to a build-in correlated double sampling (CDS) technique, but the proposed IRO-TDC does not require two samplings and the reference signal.

III. IRO-TDC PROTOTYPE IMPLEMENTATION

The IRO-TDC prototype adopts the same structure as in Fig. 1(a). For the oscillator controller, a set-reset latch takes the *Start* and *Stop* signals and generates the differential *Control* signal with sufficient driving strength to control the IRO. A phase processor captures the IRO node voltages and generates the final TDC output D_{out} . The implementation details of the IRO and the phase processor are discussed next.

Fig. 8. (a) Topology and (b) schematic of the multi-path IRO.

A. Low Skew Error Multi-Path IRO

Fig. 8 shows the schematic of the low skew error multi-path IRO. Multi-path oscillator has been reported to achieve small stage delay and low level of switching skew error because the skew errors from each stage can be “averaged” [6]. Each stage of a multi-path oscillator takes several of its preceding stages to drive its output port. The number of multi-path IRO stages should be optimized by considering the tradeoff between small stage delay and large oscillation frequency. In addition, a prime number is preferred since it inherently rejects the undesirable modes in a multi-path oscillator [6]. In this work, a 47-stage multi-path oscillator is employed. Each of the 47 delay cells consists of two opposing driver cells (driver A and B) with identical multi-input single-output structure. All IRO delay cells are controlled by $M_{1\sim4}$. When $M_{1,2}$ are turned on and $M_{3,4}$ off, all driver A are connected to supply rails and the IRO oscillates as Mode 1. Once the *Control* signals toggle, $M_{3,4}$ are turned on and $M_{1,2}$ off, thus the IRO is inverted and oscillates at the opposite direction as Mode 2. $M_{1\sim4}$ are shared by all delay cells for a simple layout and a small *Control* signal skew to each delay cell. While the layout and placement of the delay cell are customized, the routing of the whole IRO is accomplished by automatic routing tool to shorten the design period.

Fig. 10 shows a comparison of supply current between IRO and GRO. The current variation is greatly reduced in an IRO, resulting in a smaller interference to the power supply. Note that the sampling frequency is usually much higher than the Power Supply Rejection Ratio (PSRR) bandwidth of the low dropout (LDO) regulator, so the IRO has much lesser interference to other sensitive blocks. Table I summarizes the IRO post-layout simulation results and calculated noise under a 200 MS/s sampling rate.

B. Phase Processor

Fig. 9(a) depicts the structure of the adopted phase processor. Fig. 9(b) provides a timing diagram and a truth table showing the identifying of a stable ‘0’, a stable ‘1’, and

Fig. 9. (a) Phase processor implementation, and (b) illustration of stable 0, stable 1, and transition (TX) state identification.

Fig. 10. Simulated supply current comparison between IRO and GRO.

a transition state (‘TX’). The outputs of the comparators are sampled by the digital D-flip-flops (DFFs) and sent to the transition locator. The transition locator determine the location of the waveform transition and output the digitized oscillator phase code ranging from 0 to 93. There are totally $2 \times 47 = 94$ states in one IRO period. A differentiator calculates the fractional phase increment D_{frac} .

To deal with phase wrapping, a dual-edge counter as illustrated in Fig. 11 is used. Since an IRO may oscillate in two directions, two nodes (V_{L1} and V_{L24}) are used to distinguish $+1$ and -1 wrapping. To ensure correct counting, the V_{L1} edge triggers the ± 1 counting only when V_{L24} is high, as shown in

Fig. 11. Wrap counter truth table and timing diagram of positive and negative wrapping.

the truth table. At each *Start* edge, the counter is reset, and the result D_{int} is captured, multiplied by 94, and combined with D_{frac} to obtain the final TDC output.

IV. EXPERIMENTAL RESULTS

The proposed IRO-TDC is fabricated in a 65 nm CMOS technology with an active area of $280 \mu\text{m} \times 330 \mu\text{m}$. Fig. 14 depicts a microphotograph of the prototype chip and the breakdown of the total 13.2 mW core power consumption from a 1.4 V supply. A 1.8 V output level shifter is designed for robust transmission of D_{out} to the external logic analyzer. A significant portion of 6.24 mW is drawn by the conventional comparators in the phase processor. More advanced low power comparators can be used to reduce the power consumption.

Fig. 15 illustrates the test bench used to characterize the prototype TDC. Two signal generators Agilent E8267D and E8257D are used to generate *Start* and *Stop* signals. One function generator Tektronix AFG3022C is used to modulate the power supply for the noise performance test. To mimic a standard system-on-chip scenario, three independent supplies, $AVDD$, $DVDD$ and $IOVDD$, are provided by LDO regulators on PCB which are powered by Agilent E3631A. One logic analyzer Agilent 16852A is used to collect the digital output data. Measurements for this work include a linearity test, a noise performance test, and a coherent noise cancellation test.

A. Linearity Test

Fig. 12(a) shows the measured DC transfer curve of the IRO-TDC under a 200 MS/s sampling. It is obtained by offsetting the *Stop* signal 150 Hz lower than the *Start* signal to generate a ramp input and filtering the TDC output with a 3 MHz digital low-pass filter (LPF). Fig. 12(b) shows a zoom-in view of the widest dead-zone of about 20 ps at $D_{out} = 0$. In the measurement, since $T_s = 5$ ns, when $T_{in} = 2.5$ ns, output is 0 and IRO state comes back to its previous state. This means that IRO will more likely stay in a dead-zone instead of escape from the dead-zone.

The calculated least significant bit (LSB) from the DC transfer curve is 8.43 ps. As shown in Fig. 12(c), the INL across the whole range is within -0.6 and 1.8 LSB. The main source of INL is the asymmetric structure of the ring oscillator layout. Since this INL is systematic, the post-digital calibration can be applied to reduce the INL. For example, a look-up table (LUT) can be adopted to correct the output

Fig. 12. (a) DC transfer curve, (b) the widest dead-zone near TDC output code = 0, and (c) INL.

Fig. 13. The 3 MHz-filtered time domain IRO-TDC output for a 100 kHz, $\sim 2.46 \text{ ns}_{pp}$ input signal with ~ 2.67 ns offset, showing (a) the output waveform and (b) a zoom-in view near 2.5 ns output.

codes [24]. The INL due to the dead-zone is within -0.4 and 1.1 LSB. This kind of INL is difficult to be compensated due to its specific characteristic. As discussed, a dead-zone appears only with an extreme input condition, and it should disappear when a normal scrambled input is applied.

Fig. 13(a) plots the measurement result with a 100 kHz sinusoidal 2.5 ns_{pp} large signal (limited by equipment) in addition to a 2.67 ns offset. Fig. 13(b) shows a zoom-in view of the TDC output near $D_{out} = 0$ (i.e. 2.5 ns input), where a dead-zone was found in the previous DC transfer characteristic. In fact, no dead-zone was observed during this test. With an input deviation large enough, the dead-zones disappear because the IRO phase is sufficiently scrambled and

Fig. 14. (a) Microphotograph of the IRO-TDC prototype, and (b) power consumption of each part in the TDC core.

Fig. 15. Test bench for the proposed TDC.

the phase locking process does not converge. In an actual DPLL, a digital offset can also be added to the control loop so that the TDC can operate at the non-dead-zone region even if the input deviation is small.

B. Noise Performance Test

In this test, the *Start* signal is split into two, one of which is delayed through an RF cable to generate input offset. This delayed signal is further modulated by a delay buffer and used as the *Stop* signal. This removes the impact of input jitter from equipment since both clocks are generated from the same clock source. Fig. 16 shows both the measured frequency and time domain outputs with a 100 kHz sinusoidal input of 1.8 ps_{pp} in addition to an offset of 2.757 ns. In Fig. 16(a), the 65,536-point fast Fourier transform (FFT) is performed with a Hanning window on 16 sequential collects and averaged to obtain the double-sided PSD plot. The measured PSD is in good agreement with the modeled profile of IRO phase noise contribution at low frequencies. However, the actual quantization noise is higher than calculated. This may be due to the input offset voltage of comparators. A quantizer mapping logic in [6] can be adopted in future to mitigate this error. The spurs outside the signal bandwidth are normal to a first-order noise shaping converter when the sinusoidal input signal amplitude is small. When the input amplitude increases, the spurs will reduce or even disappear. The measured integrated noise is 196 fs_{rms} within 3 MHz and 145 fs_{rms} within 1 MHz bandwidth.

Fig. 16. Measured IRO-TDC output for a 100 kHz, 1.8 ps_{pp} input signal with 2.757 ns offset. (a) plots the signal and double-sided PSD in the frequency domain, and (b) shows the output after a 3 MHz digital LPF in time domain.

By comparison, the simulated total in-band noise, including the increased quantization noise, is approximately 122 fs_{rms} within 1 MHz bandwidth or 166 fs_{rms} within 3 MHz. The difference between measured and calculated noise is caused by jitters of the signal splitter, external RF cable, input buffer, and the oscillator controller. The resolution is 0.68 ps according to the 196 fs_{rms} integrated noise within 3 MHz, so the effective number of bits (ENOB) of the proposed IRO TDC is 13. When this TDC is applied in a DPLL, Eq. (1) can be used to estimate the DPLL in-band phase noise. For instance, the measured TDC noise at 200 kHz is -80 dB ps²/Hz, so a corresponding 3 GHz DPLL would achieve an in-band phase noise of -111 dBc/Hz at 200 kHz offset.

Fig. 16(b) shows the filtered time-domain waveform after a 3 MHz digital LPF. The IRO-TDC can resolve a 1.8 ps_{pp} signal clearly.

The single-shot measurement was performed, and the measured integrated noise is 213 fs_{rms} with 3 MHz bandwidth.

C. Coherent Noise Cancellation Test

To verify the unique coherent noise cancellation of the IRO-TDC, coherent noise is intentionally added to the TDC. Power supply noise is one of the coherent sources. It can be easily applied to the prototype. A sinusoidal signal is injected into AVDD to mimic power supply noise. The *Stop* signal with input peak-to-peak amplitude of 10.8 ps_{pp} is now modulated by the second RF signal generator to monitor whether the wanted signal power is affected. According to III, *T_{in}* offset can be changed for different PNRR. The IRO should exhibit

Fig. 17. (a) PNRR obtained from PSD comparison between outputs with and without noise cancellation. (b) shows PNRR vs. T_{in}/T_s with 50 kHz noise, and (c) shows PNRR vs. noise frequency with $T_{in}/T_s \approx 0.48$.

TABLE II
COMPARISON WITH STATE-OF-THE-ART OSCILLATOR-BASED NOISE-SHAPING TDCs

Design	[9]	[11]	[12]	[13]	[16]	[18]	[19]	[22]	[23]	This work
Process (nm)	130	180	130	130	65	130	65	90	65	65
Oscillator Type	M-Path GRO	M-Path GRO	Relax. Osc.	CP-OSC	2D-GRO	GVRO	GRO-MASH	SRO	GSRO	IRO
Area (mm ²)	0.04	0.0017	0.11	0.43	- ¹	0.03	0.03	0.02	0.05	0.09
Sampling (MS/s)	50	2	50	90	50	2.4	150	500	200	200
Input range (ns)	12.3 ²	297	20	5.55	3	9	5.4	12.5	4	4.6
Bandwidth (MHz)	1	3.9	0.1	2.81	1.25	1~2	15	1	4	3
$\sigma_{TDC,rms}$ (fs)	80 ³	1560	1616 ⁴	886	716 ⁴	1740	760	315	455	196
Resolution (ps)	0.28 ^{3,5}	147	5.6	3.07	2.48	7.3	2.64	1.09 ⁵	1.58	0.68
Power (mW)	≤ 31.5 ³	0.009	1.7	2.58	2	1.2	3.52	2	4.26	13.2
Supply current	Varying	Varying	- ¹	- ¹	- ¹	Varying	Varying	Const. ⁶	Varying	Const.
ENOB	15 ³	9	12	11	10	10	11	13	11	13
TDC FoM (dB) ⁷	Up to 181 ³	213	151	157	151	157	164	170	160	162
PNRR (dB)	No	No	No	No	No	No	No	No	No	Up to 36.4

¹ Not mentioned.

⁵ Estimated Resolution = $\sqrt{\sigma_{TDC,rms}^2 \times 12}$.

² with 6 ps raw resolution and 11-bit range.

⁶ Pseudo-differential structure.

³ Depends on input value, T_{in} .

⁷ TDC FoM = $20\log_{10}(\text{Input range rms}/\sigma_{TDC,rms}) + 10\log_{10}(f_{BW}/\text{Power})$.

⁴ Estimated $\sigma_{TDC,rms} = \sqrt{\text{Resolution}^2/12}$.

some PNRR when $0 < T_{in}/T_s < 1$ and nearly no cancellation when $T_{in}/T_s \rightarrow 0$ or 1.

Fig. 17(a) shows this difference between strong cancellation ($T_{in}/T_s \approx 0.48$) and very weak cancellation ($T_{in}/T_s \approx 0.96$) with a 50 kHz power noise. A 25 dB noise rejection is clearly seen and the wanted signal is not affected. Compared with 16(a), the measured noise profile increases due to the equipment jitters since the *Start* and *Stop* signals are from different generators.

Fig. 17(b) plots the PNRR with different T_{in}/T_s and a fixed 50 kHz noise. The measured PNRR agrees well with the calculated results from III. A maximum PNRR of 36.4 dB is observed at $T_{in}/T_s = 0.4918$. For DPLL applications, a digital offset can be used to bias the IRO-TDC for optimized PNRR.

Fig. 17(c) shows the PNRR performance with different noise frequencies from 3 kHz to 800 kHz. The FFT point

number is increased to measure noise at lower frequencies. Power noise injection at higher frequencies was not performed due to the strong attenuation by the capacitors and power supply. Measured PNRR ranges from 20.4 dB to 26.1 dB across the testing frequencies. At higher noise frequencies, the noise injection is affected by on-chip decoupling capacitors, resulting in a larger PNRR deviation from the calculated value. In fact, high-frequency noise can be easily attenuated and should have little impact to the TDC noise in practical applications.

Performance of this work is summarized and compared with state-of-the-art oscillator-based noise-shaping TDCs in Table II. Except for the GRO in [9] measured with a small T_{in} offset of 1.6 ns, the proposed IRO-TDC achieves the lowest integrated noise in a wide signal bandwidth of 3 MHz. The measured integrated noise performance for GRO, IRO, and

SRO-TDCs also roughly match our proposed noise model. The sampling rates of GRO-TDCs are lower compared with the IRO and SRO-TDCs. The supply currents of the typical oscillator-based TDCs are varying, only [22] employs the pseudo-differential structure to reduce the current variation. In the proposed IRO-TDC, the supply current is inherently constant. Moreover, a unique in-band coherent noise cancellation of up to 36.4 dB PNRR is achieved. Due to this PNRR, the TDC can be protected from coherent noises such as power supply noise, ground noise, substrate noise, etc. In addition, although the power consumption is not optimized in this work, the IRO-TDC draws constant supply current and generates little interference to the power supply. Accordingly, a friendly power supply interface is provided in this IRO-TDC. The phase processor can be further optimized for lower power consumption and better FoM in future designs.

V. CONCLUSIONS

In this work, we have presented an IRO technique for noise-shaping TDC. It achieves in-band noise reduction, coherent noise cancellation, as well as low disturbance to power supply. We have also proposed a general model for controller oscillator-based TDC family to predict the noise performance. Measurement results are provided to verify the noise model and the low in-band noise of the IRO-TDC. The IRO-TDC prototype achieves a unique PNRR of up to 36.4 dB to protect the TDC from coherent noise. Measured integrated noise is 196 fs_{rms} in a 3 MHz bandwidth at a 200 MS/s sampling rate with a constant power dissipation. Due to its coherent noise cancellation and low disturbance to power supply, the proposed IRO technique can greatly reduce the design complexity of power supply in future TDC applications.

Except for the customized delay cells, the oscillator controller, and the comparators, all other parts of the IRO-TDC can be implemented by digital circuits and the whole design can take advantages of the advanced automatic design flow in the future.

APPENDIX

The appendix shows the explanation of dead-zone problem. Another possible effect caused by the phase skew is that dead-zones can be found in the DC transfer characteristic of the TDC, as shown in Fig. 20 and also in the measured DC transfer characteristic in Fig. 12(b). Around certain input values, the TDC output is pushed away from the ideal curve to some values and does not change with the input. It has been briefly mentioned and measured in [6]. Here we provide a more visible and quantitative explanation.

Dead-zones can be found only when the oscillator phase is not scrambled adequately. As will be explained in detail later, the amount of phase skew ϕ_{skew} depends on the oscillator phase ϕ_{XRO} . Fig. 19 illustrates how the phase skew affects an oscillator. Each time the phase skew is generated, it is added into the oscillator and affects the future phase ϕ'_{XRO} . So $\phi'_{XRO} = \phi_{XRO} + \phi_{skew}$.

With this mechanism established, we can explain how a dead-zone is formed using Fig. 22. Let us consider a small

Fig. 18. Phase changes with $2K\pi$ phase increment near (a) a negative zero-crossing point and (b) a positive zero-crossing point.

Fig. 19. Effect of phase skew to an oscillator.

region near a zero-crossing ϕ_{skew} with a negative slope (or falling edge), as in Fig. 22(a). To find the dead-zones, firstly, assume the skew-less oscillator phase increment during each measurement cycle is exactly $2K\pi$, i.e.,

$$\Delta\phi_{XRO} = 2K\pi, \quad (22)$$

where K is an integer. That is to say, ϕ'_{XRO} becomes the next ϕ_{XRO} (after wrapped). Fig. 22(a) shows the operation

Fig. 20. Conceptual DC transfer characteristic showing a dead-zone.

Fig. 21. Relation between phase increment and dead-zone.

Fig. 22. Phase changes near ϕ_{nzc} with $2K\pi + \phi_{dev}$ phase increment.

under this scenario. If $\phi_{XRO} = \phi_{01}$ at some cycle, ϕ'_{XRO} becomes ϕ_{02} because of the phase skew. At the next cycle, $\phi_{XRO} = \phi_{02}$, and ϕ'_{XRO} becomes ϕ_{03} . In the subsequent cycles, ϕ_{XRO} is pushed towards a larger value as an effect of ϕ_{skew} . In another case, if $\phi_{XRO} = \phi_{11}$ at some cycle, ϕ'_{XRO} becomes ϕ_{12} because of the phase skew. At the next cycle, $\phi_{XRO} = \phi_{12}$, and ϕ'_{XRO} becomes ϕ_{13} . Similarly, ϕ_{XRO} is pushed towards a smaller value. As a result, if the phase increment is kept $2K\pi$, the oscillator phase will be eventually pushed to the negative zero-crossing point ϕ_{nzc} regardless of the initial ϕ_{XRO} . The reader can analyze with Fig. 22(b) using the similar flow, and will find that a positive zero-crossing point ϕ_{pzc} is not such a stable phase (but a metastable phase) because ϕ_{skew} will push ϕ_{XRO} away from ϕ_{pzc} .

From the above analysis, we can now conclude that: Firstly, a negative zero-crossing point of ϕ_{skew} results in one dead-zone. Different value of K will lead the oscillator to the same dead-zone. The negative zero-crossing point of ϕ_{skew}

is defined as the *stable point*. Secondly, if more stable points exist, there will be more dead-zones.

Next, we can add some deviation to the phase increment, and assume

$$\Delta\phi_{XRO} = (1-x)\omega_0 T_{in} + x\omega_0 T_s = 2K\pi + \phi_{dev}, \quad (23)$$

where K is an integer and ϕ_{dev} is a small deviation. The phase is shown in Fig. 22. If $\phi_{XRO} = \phi_{21}$ at some cycle, due to the phase skew, ϕ'_{XRO} becomes $\phi_{22} = \phi_{21} + \phi_{skew}(\phi_{21})$. At the next cycle, $\phi_{XRO} = \phi_{23} = \phi_{22} + \phi_{dev}$. To avoid being pushed towards the stable point, ϕ_{23} has to be further away than ϕ_{21} from the stable point, i.e.,

$$\phi_{23} = \phi_{22} + \phi_{dev} < \phi_{21}. \quad (24)$$

Accordingly,

$$\phi_{dev} < \phi_{21} - \phi_{22} = -\phi_{skew}(\phi_{21}). \quad (25)$$

Generally, to avoid being locked, the following condition should be met:

$$\phi_{dev} < -\phi_{skew}(\phi_{21}), \quad \forall \phi_{21}. \quad (26)$$

In other words, in order to escape from the dead-zone, deviation must be

$$\phi_{dev} < -\phi_{skew,max}. \quad (27)$$

Similarly, another condition that also permits the oscillator to escape from the dead-zone is

$$\phi_{dev} > -\phi_{skew,min}. \quad (28)$$

In (27) and (28), $\phi_{skew,max}$ and $\phi_{skew,min}$ refer to the positive and negative largest ϕ_{skew} from 0. Eq. (27) and (28) reveal that, a dead-zone will appear if

$$-\phi_{skew,max} < \phi_{dev} < -\phi_{skew,min}. \quad (29)$$

This conclusion is illustrated in Fig. 21. Substituting (23) into (29), the input range causing dead-zone is

$$\frac{2K\pi - \phi_{skew,max}}{(1-x)\omega_0} - \frac{xT_s}{1-x} < T_{in} < \frac{2K\pi - \phi_{skew,min}}{(1-x)\omega_0} - \frac{xT_s}{1-x}. \quad (30)$$

For simplicity, we define $\phi_{skew,range} = \phi_{skew,max} - \phi_{skew,min}$. The dead-zone width is thus

$$T_{dz,XRO} = \frac{\phi_{skew,range}}{(1-x)\omega_0}. \quad (31)$$

We can obtain the dead-zone width of a GRO ($x = 0$) as

$$T_{dz,GRO} = \frac{\phi_{skew,range}}{\omega_0}, \quad (32)$$

and that of an IRO ($x = -1$) as

$$T_{dz,IRO} = \frac{\phi_{skew,range}}{2\omega_0}. \quad (33)$$

This implies that an IRO can also reduce the dead-zone width for a same $\phi_{skew,range}$.

Certainly, the phase increment during each measurement is hardly identical. Other noises such as the thermal noise jitter of the controller and the signal input buffers can cause

some deviation, ϕ_{dev} . However, (31) does provide an important conclusion that the dead-zone width can be reduced if ϕ_{skew} can be constrained within a smaller range. If $\phi_{skew,range}$ is even less than the phase deviation caused by the thermal jitter, dead-zone is expected to disappear completely.

To conclude, a dead-zone appears if the following two conditions are fulfilled at the same time: 1) Eq. (30) is met. In other words, the input time is close enough to certain values. 2) Eq. (30) is met for long period of time. From the locking procedure shown in Fig. 22(a), the mechanism takes several consecutive cycles to lock the phase. If a large phase deviation occurs during this procedure, the phase escapes and is not likely to be locked.

For most TDC operations, a random input time is applied. For example, in fractional- N digital PLLs, the input time is quickly and sufficiently dithered by DSM. Under such condition, a dead-zone should not occur.

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