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2020

Dong, Y., Kong, L., Boon, C. C., Liu, Z., Li, C., Yang, K., & Zhou, A. (2020). A wideband variable-gain amplifier with a negative exponential generation in 40-nm CMOS technology. Proceedings of the 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 375-378. doi:10.1109/RFIC49505.2020.9218416

<https://hdl.handle.net/10356/144775>

<https://doi.org/10.1109/RFIC49505.2020.9218416>

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A Wideband Variable-Gain Amplifier with a Negative Exponential Generation in 40-nm CMOS Technology

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Abstract—A wideband variable-gain amplifier (VGA) with a negative exponential generation using 40 nm CMOS technology is reported. By compensating a single-branch negative exponential generator (NEG) which features a composite of dual Taylor series, the proposed negative exponential generation further extends the dB-linear range. The measurement results show the overall VGA achieves a dB-linear range of 51 dB (−34 ~ 17dB) with a gain error less than ± 1 dB. In addition, the bandwidth is around 7 GHz under different gain settings. The core circuit draws 24.6 mA current from a 1.1 V power supply (excluding the output buffer) and occupies an active area of 0.038 mm².

Keywords—Variable-gain amplifier, negative exponential generator, gain error compensation, Taylor series, dB-linear, wideband.

I. INTRODUCTION

With the increasing demands for high-speed wireless and wireline communication systems, wideband variable-gain amplifiers (VGA) become more and more commonly used in the analog front-end circuits and gigabit-class data communication link to improve the dynamic range of the transceiver chain or assist the automatic gain control (AGC) loop to achieve a uniform loop transient response and settling time [1]. In such applications, VGAs are always required to have dB-linear characteristics over a large signal range with an acceptable gain error. Compared to digital control approaches, the continuous analog gain control mechanism is preferred for its simplicity and immunity to glitches [2].

To achieve and extend the dB-linear gain range, various structures [1-7] are introduced to produce the exponential function. A simple way to generate the exponential relationship is to adopt the bipolar transistors and make use of its intrinsic exponential I-V relationship [3]. However, it is better if the exponential generation can be realized in a standard CMOS process due to a lower cost of integration. MOSFETs in sub-threshold region can also be used to approximate the exponential functions [4], [5], but they are not favoured for the limited input swing, matching accuracy, speed as well as noise contribution. Other methods based on pseudo-exponential and Taylor series approximations using MOSFETs in saturation region are reported, however, the circuits are usually complex due to the implementation for the numerator and denominator in the approximation function [6].

To simplify the exponential generation circuits and acquire a wide dB-linear gain range with an acceptable gain error for wideband VGAs, a negative exponential generator (NEG) composed of only three MOSFETs is designed based on the approximation of dual Taylor series [8]. The dB-linear gain range of the NEG can be further extended by employing simple

compensation circuits. In this paper, a novel implementation of negative exponential function approximation by compensating the pseudo-exponential function of the NEG is illustrated. The negative exponential approximation is accurate across a wide gain range owing to the proposed gain error compensation technique. The remainder of this paper is organized as follows. Section II describes the principle of the proposed negative exponential generation approach and the implementation of the whole wideband dB-linear VGA. Section III presents the simulation results of the proposed compensated negative exponential generation and measurement results of the whole VGA. Finally, conclusions are drawn in Section IV.

II. PRINCIPLE AND CIRCUIT IMPLEMENTATION

A. Architecture of the Proposed VGA

The block diagram of the VGA and the proposed negative exponential generation implementation are shown in Fig.1. Three cascaded variable gain stages are controlled by outputs of three NEG's respectively. By tuning the external control signal (V_{ctrl}), the gain of the variable gain stages can be varied. After that, the signal is further amplified by the post amplifier with a fixed gain to a desired level. The DC offset cancellation (DCOC) loop is implemented to reduce the DC offset of the post amplifiers by setting the high-pass corner around 200 kHz. At the last stage of the VGA, a 50- Ω output impedance f_T doubler buffer is built to drive the output signal.

B. Negative Exponential Generation Circuits

In the previous research [8], the single-branch NEG is designed based on the mathematical approximation of a composite of dual Taylor series. When x approaches “0”, according to the 2nd-order expansion of the Taylor series, the ideal e^{-x} can be approximated and expressed as

$$e^{-x} \approx A_n + B_n x + C_n \sqrt{D_n + E_n x + F_n x^2} = G_n(x) \quad (1)$$

where A_n to F_n are the normalized coefficients. By adjusting the different groups of the normalized coefficients (A_1 to F_1) and (A_2 to F_2), one concave function $G_1(x)$ and the other convex function $G_2(x)$ can be obtained to approximate the same negative exponential function around the origin. Their approximation regions may vary slightly, but both approximation errors decrease as x approaches “0”.

To realize the concave and convex function, the NEG is implemented with three MOSFETs in [8]. As shown in Fig. 2(a), by adjusting the parameters of the MOSFETs and V_{bias} , a concave function $G_1(x)$ can be realized in region I, while a

Fig. 1. (a) Block diagram of the proposed VGA; (b) NEG for the first gain stage; (c) NEG with auxiliary circuits for the second and the third gain stage

Fig. 2. (a) NEG implementation; (b) Simulation results

convex function $G_2(x)$ can be achieved in region II. The simulation results in Fig. 2(b) show the NEG can obtain a dB-linear range of 26 dB with a gain error $< \pm 1.2$ dB.

To further extend the dB-linear range of the NEG, a novel compensation method is proposed in this paper as depicted in Fig. 3(a). For the concave function $G_1(x)$ in region I, the convex function $G_2(x)$ can be shifted up along the ideal dB-linear function to make a compensation for the gain error, which can be expressed as

$$G_1(x)_{\text{compensatedI}} = G_1(x) + G_2(x + V_{h1}) + V_{v1} \quad (V_{ctrl} \leq V_m) \quad (2)$$

where $G_1(x)_{\text{compensatedI}}$ symbolizes the compensated $G_1(x)$ function in region I, V_{h1} means the absolute horizontal variation value and V_{v1} means the absolute vertical shift value. Similarly, the concave function $G_1(x)$ can be shifted down along the ideal negative dB-linear slope to compensate the gain error of the convex function $G_2(x)$ in region II, obtaining

$$G_2(x)_{\text{compensatedII}} = G_2(x) + G_1(x - V_{h2}) - V_{v2} \quad (V_{ctrl} > V_m) \quad (3)$$

Therefore, by compensating the convex function with concave function and vice versa, the resulted gain error will be reduced theoretically.

To implement this compensation mechanism, three NEGs are employed in Fig. 1. The first NEG in Fig. 1(b) is used to provide the control signals V_{x1} , V_{y1} for the first variable-gain stage. Fig. 1(c) shows the NEGs with auxiliary circuits for the second and the third variable gain stages respectively. The output control voltage $V_{yx2} (=V_{y2}-V_{x2})$ of NEG 2 is designed to

compensate the concave wave $G_1(x)$ in $V_{yx1} (=V_{y1}-V_{x1})$. The control voltage V_{ctrl} will firstly be compared with a fixed voltage V_m , which is the intersection voltage of region I and region II. If V_{ctrl} is larger, V_{g4} , the gate voltage of M_4 , will be connected to V_m . Otherwise, V_{g4} will be the same as V_{ctrl} . Then V_{g4} will be shifted up by V_{h1} and become the control voltage V_{c2} to control NEG 2. The output of NEG 3, $V_{yx3} (=V_{y3}-V_{x3})$, is generated to compensate the convex wave $G_2(x)$ in V_{yx1} . If V_{ctrl} is less than V_m , V_{g5} will be connected to V_m , or else V_{g5} will be kept the same as V_{ctrl} . Then V_{g5} will be shifted down by V_{h2} through a level shifter to V_{c3} , which controls NEG 3. Through this implementation, two new functions V_{yx2} (shows negative exponential characteristic at region I), V_{yx3} (shows negative exponential characteristic at region II) are generated and shown in Fig. 3(b).

Fig. 3. (a) Theoretical compensation scheme; (b) Simulation results of proposed compensated negative exponential generation; (c) Comparison of the proposed negative exponential generation with ideal dB-linear function

By combining V_{yx1} , V_{yx2} and V_{yx3} in dB scale, a new negative exponential approximation can be acquired. The compensated functions in region I and region II become,

$$G_1(x)_{\text{compensatedII}} = G_1(x) + G_2(x + V_{h1}) + G_1(V_m - V_{h2}) \quad (V_{ctrl} \leq V_m) \quad (4)$$

$$G_2(x)_{\text{compensatedII}} = G_2(x) + G_1(x - V_{h2}) + G_2(V_m + V_{h1}) \quad (V_{ctrl} > V_m) \quad (5)$$

Obviously, $G_1(x)_{\text{compensatedII}}$ and $G_2(x)_{\text{compensatedII}}$ give a same value at $V_{ctrl} = V_m$ and perform as two pseudo exponential functions approximating one ideal negative exponential function in both regions. Simulation results in Fig.3 (c) show that compared to the ideal dB-linear function, the compensated negative exponential approximation $[20\log(V_{yx1}V_{yx2}V_{yx3})]$ can achieve a dB-linear gain of nearly 57 dB within ± 1 dB gain error. In addition, the auxiliary circuits, i.e. the comparator and the level shifters, consume only several microwatts as the NEGs work at very low frequency.

C. Variable Gain Stages

Fig. 4 depicts a folded Gilbert structure [3] which is employed in variable gain stages. V_{cp} and V_{cn} manipulate the gain of the Gilbert cell, which can be given by,

$$A_v = \sqrt{\frac{1}{2} K_{18,19,20,21} K_{16,17} R_{1,2} V_{cpn}} \quad (6)$$

The relationship between V_{yx} and V_{cpn} ($=V_{cp}-V_{cn}$) can easily be obtained,

$$V_{cpn} = \sqrt{K_{13,15} / K_{12,14}} V_{yx} \quad (7)$$

Combining (6) and (7), the gain varies linearly with V_{yx} as the following equation,

$$A_v = \sqrt{\frac{1}{2} K_{18,19,20,21} K_{16,17} K_{13,15} / K_{12,14} R_{1,2} V_{yx}} \quad (8)$$

When three gain stages are cascaded, the total gain in dB scale can be expressed as:

$$20\log(A_{v1}A_{v2}A_{v3}) = 60\log\left(\sqrt{\frac{1}{2} K_{18,19,20,21} K_{16,17} K_{13,15} / K_{12,14} R_{1,2}}\right) + 20\log(V_{yx1}V_{yx2}V_{yx3}) \quad (9)$$

As the proposed function $[20\log(V_{yx1}V_{yx2}V_{yx3})]$ can achieve a dB-linear characteristic, the VGA's gain will vary dB linearly as well.

Fig. 4. Circuit schematics of variable gain stages

D. Post Amplifier

To further enlarge the total gain of the VGA, the post amplifier is implemented with a fixed gain and bandwidth

under various gain settings. Five common source amplifiers with RC-degeneration, as shown in Fig. 5(a), are cascaded in the post amplifier to achieve about 22.3 dB gain over a frequency range of 10 GHz. Each common source amplifier consumes roughly 3 mA current under 1.1 V supply voltage.

Fig. 5. (a) Fixed-gain amplifier; (b) f_T doubler output buffer

E. Output buffer

To measure the VGA, usually an output buffer is necessary to drive the standard input impedance of testing equipment. For high-frequency applications, the f_T doubler structure in Fig. 5(b) is widely adopted in the buffer stage as it can reduce the input impedance almost by half. In this paper, the output buffer based on the f_T doubler structure achieves only 3 dB loss over 10 GHz frequency range.

III. SIMULATION AND MEASUREMENT RESULT

In the dB-linear VGA, the exponential function generator, which makes the most contribution to the gain error, usually needs to be kept in a robust state under different process and temperature variations. Thus, to evaluate the influences of these variations on the proposed negative exponential generation, simulations ran under (SF, -40°C), (SS, -40°C), (TT, 27°C), (FF, 80°C) and (FS, 80°C) respectively. Among these corner simulation results shown in Fig. 6, the worst case (SS, -40°C) can still achieve a gain error of ± 1 dB with a roughly 50 dB gain range.

Fig. 6. Simulation results over process and temperature variations

To verify the proposed negative exponential generation, the complete VGA is fabricated in a standard 40nm CMOS process. Fig. 7 shows the die photograph, which indicates the core area of the VGA is $0.135 \times 0.28 \text{ mm}^2$. The chip consumes 24.6 mA current from 1.1 V power supply excluding the output buffer for testing. The frequency response is measured with the Keysight Network Analyzer (N5247A). As shown in Fig. 8(a), the bandwidth is almost constantly around 7 GHz while the gain varies. Fig. 8(b) depicts a dB-linear gain range of 51 dB ($-34 \sim 17\text{dB}$) with a gain error of ± 1 dB is achieved, which is almost

Table 1. Performance comparison with other state-of-the-art designs

	Springer'16 [2]	TMTT'16 [4]	JSSC'16 [6]	TCASI'19 [7]	TCASI'18 [8]	<i>This work</i>
Gain range (dB)	70 (-50 ~ 20)	22 (2 ~ 24)	40 (-15 ~ 25)	45 (-31 ~ 14)	40 (-18 ~ 22)	51 (-34 ~ 17)
Gain error (dB)	> 4	± 0.3	± 1	± 0.85	± 1	± 1
BW (GHz)	4.6	2 ~ 2.2	5	0.74	7	7
Output P_{1dB} (dBm)	-19	1.8	N/A	-14	N/A	-8**
Noise figure	8.5 dB	24 dB	N/A	30 dB	4.26 nV / $\sqrt{\text{Hz}}$	30.5 dB
Power (mW)	19.8	3.48	50*	2.49	28*	27.06
Active area (mm ²)	0.0875	0.01	0.4	0.033	0.045	0.038
Technology	180 nm BiCMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS	40 nm CMOS

* Including the peak detector and integrator for AGC, which usually consume little power.

** The actual P_{1dB} of the VGA is 3 dB higher as the loss of the output buffer is not de-embedded from the measured P_{1dB} data.

consistent with the simulated results. A performance summary of the proposed VGA is given in Table 1. The proposed wideband VGA with the compensated negative exponential generation achieves good merits like simple implementation of negative exponential generation, large dB-linear gain range, wide bandwidth and small chip area, satisfying the requirements of high-speed wireless and wireline applications.

Fig. 7. Chip photograph

Fig. 8. (a) Measured gain frequency response of the VGA; (b) Gain characteristics at 3.5 GHz

IV. CONCLUSION

A wideband dB-linear VGA with a novel compensated negative exponential approximation has been introduced. The proposed wideband VGA fabricated in 40-nm CMOS technology provides a dB-linear gain range of 51 dB with ± 1 gain error while maintaining a bandwidth of 7 GHz during gain variations. In consideration of the simple implementation, large dB-linear gain range, small chip area and wide bandwidth, the proposed VGA demonstrates its suitability for low-cost high-speed wireline and wireless applications.

ACKNOWLEDGMENT

The authors thank Dr. Li Xin for her great help. This research is supported by A*STAR under its RIE2020 Advanced Manufacturing and Engineering (AME) Industry Alignment Fund - Pre Positioning (IAF-PP) (Award A19D6a0053).

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