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Reconfigurable 2.4-/5-GHz Dual-Band Transmitter Front-End Supporting 1024-QAM for WLAN 802.11ax Application in 40-nm CMOS

Bei Liu¹, Student Member, IEEE, Xing Quan²,

Chirn Chye Boon¹, Senior Member, IEEE, Devrishi Khanna, Member, IEEE,

Pilsoon Choi³, Senior Member, IEEE, and Xiang Yi⁴, Senior Member, IEEE

Abstract—This article presents a new design methodology of a reconfigurable dual-band output matching network with high efficiency. The implemented output matching network achieves a passive efficiency of 71.6% and 75% at 2.4 and 5.5 GHz, respectively. Based on the proposed output matching network, a transmitter and a standalone power amplifier (PA) supporting 2.4-/5-GHz dual-band operation for the emerging wireless local area network (WLAN) 802.11ax application are designed and fabricated in 40-nm CMOS technology. In 2.4- and 5-GHz WLAN bands, the PA achieves a P_{sat} of 23 and 21.9–22.4 dBm with power-added efficiency (PAE) of 27% and 24.2%–28.2%, respectively. At 2.442 GHz, the transmitter delivers 8.1-dBm average output power for 40-MHz, 1024-quadrature amplitude modulation (QAM) 802.11ax signal while meeting the standard specification of error vector magnitude (EVM) below -35 dB. In 5-GHz operating mode, the transmitter achieves an average output power of 6.72–6.95 dBm with the EVM of -35 dB for 80-MHz, 1024-QAM 802.11ax signal. The PA and transmitter front end are the first published designs for dual-band WLAN 802.11ax application in the literature.

Index Terms—CMOS transmitter, dual band, error vector magnitude (EVM), power amplifier (PA), 802.11ax, wireless local area network (WLAN).

I. INTRODUCTION

RECENTLY, the accelerating growth of smartphones and mobile devices is propelling wireless communication to evolve toward a higher data rate. Currently, as the main standard for broadband wireless local area network (WLAN) in the commercial market, the IEEE 802.11ac system cannot satisfy the ever-increasing demand on a higher data rate.

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Bei Liu, Chirn Chye Boon, and Devrishi Khanna are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: liubei@ntu.edu.sg; eccboon@ntu.edu.sg).

Xing Quan is with the School of Mechano-Electronic Engineering, Xidian University, Xi'an 70001, China.

Pilsoon Choi and Xiang Yi are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

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The development of new IEEE 802.11 standards is drawing much effort in academia and industry. As the successor to current IEEE 802.11ac, the emerging IEEE 802.11ax introduces orthogonal frequency-division multiple access (OFDMA), utilizes smaller sub-carrier spacing, and employs 1024-quadrature amplitude modulation (QAM) modulation to improve overall spectrum efficiency and boost the data rate. The data rate of 802.11ax is expected to reach 10 Gb/s in order to meet the tremendous demand for high data rate applications, such as interactive and high-definition video. However, wide bandwidth and complex modulation scheme of 802.11ax result in a large peak-to-average power ratio (PAPR), requiring a large back-off for power amplifier (PA) to meet the stringent error vector magnitude (EVM) requirement, thus reducing the power efficiency. Consequently, the design of a highly linear integrated PA in a CMOS process with high efficiency remains a great challenge. Besides, the EVM requirement of 1024-QAM modulation is -35 dB, posing more stringent requirements of linearity on transmitter and phase noise on LO than the earlier 802.11 standards.

The 802.11ax's devices are designed to operate in the existing 2.4- and 5-GHz (4.9–5.9 GHz) spectrums, requiring a dual-band transmitter or a broadband transmitter covering both 2.4- and 5-GHz bands. In the literature and commercial products, two separate RF transmitting channels with different operating frequencies are integrated together to enable 2.4-/5-GHz dual-band operation [1]–[6]. Although the architecture using two RF channels can meet the requirement of dual-band operation for 802.11ax, the chip size will be large, and the cost will be high due to two RF channels used. In terms of low cost, a single transmitter supporting reconfigurable 2.4-/5-GHz operation is superior to the dual-band architecture using two transmitters. Currently, no reconfigurable dual-band transmitter using only one transmitting channel is available in academia and industry. Therefore, the effort of this article is to design such a reconfigurable 2.4-/5-GHz dual-band transmitter front end.

As a core block in a transmitter, the PA should operate in dual band or in broadband to cover both 2.4- and 5-GHz bands. There are two general approaches have been proposed to implement dual-band or multiband and broadband PAs.

The first approach is based on using reconfigurable components in the matching networks, such as switches [7]–[9], varactors [10], and p-i-n diode [11]. The other approach is based on using distributed configurations [12]–[14] and various broadband matching techniques, such as reactive filter synthesis and real frequency techniques [15]–[19]. In [7], the operating frequency of the PA can be tuned at 2.4/3.5 GHz through changing the status of the two switches in the output matching network, but the achieved maximum drain efficiency is below 16.5%. In [8] and [9], two S/X-band PAs using the same switchable transformer are presented, and the efficiency of the PAs in the X-band is only 12.5% due to the large resistance of the switch in series with the transformer. Reference [10] proposes a multiband multimode PA with an efficiency of 30%–55% using off-chip high-quality varactors. However, these high-quality varactors are realized in silicon-on-glass technology, resulting in a high cost in practical applications. If realized in CMOS technology, the quality factor of varactors will drop rapidly, leading to a significant decrease in the efficiency of PA. Besides, the ratio of $C_{\max}/C_{\min}$ of varactor limits the achievable frequency tuning range. In [11], a multiband PA is proposed using p-i-n diodes to control the inductor value, while the p-i-n diode is unavailable in CMOS technology. Compared with the PAs using reconfigurable components, the distributed PAs have a distinct advantage in the performance of return loss and wideband. However, they inherently suffer from low power efficiency and large size, making them unsuitable for low-cost application. Although the PAs using filter-based matching network have better efficiency in comparison with the distributed PAs, the power efficiency is still limited by the large loss of complex high-order output matching network, and the size of the output matching network is also quite large due to the inductors used.

In this article, switches are utilized in output matching network to realize dual-band performance, mainly based on the consideration of small chip size and low cost. A new design methodology of the reconfigurable output matching network is proposed to extract high passive efficiency, and the synthesis procedure is described in detail. Since the ON-resistance of switches significantly impacts the passive efficiency of the output matching network, how the ON-resistance affects the efficiency has been investigated theoretically, providing a foundation to pursue high efficiency in the synthesis procedure of the output matching network. Based on the proposed design methodology of high-efficiency dual-band matching, a 2.4-/5-GHz dual-band transmitter front end is designed and implemented in 40-nm CMOS technology. Besides, to further validate the methodology, a standalone PA is also designed and measured.

This article is organized as follows. Section II describes the design methodology and implementation of the reconfigurable output matching network. In Section III, the design of the transmitter is presented. Section IV presents the implementation of the reconfigurable dual-band transmitter together with a standalone PA. The stand-alone PA is tested with a continuous-wave (CW) signal to verify the design methodology of the reconfigurable output matching. Besides, the PA and transmitter are tested using practical 802.11ax signals, and the

Fig. 1. Load-pull simulation results. (a) 2.4 GHz. (b) 5.5 GHz.

measurement results are presented in Section IV. Section V gives the conclusion of this article.

II. DESIGN OF DUAL-BAND OUTPUT MATCHING NETWORK

A. Optimum Load Impedance Analysis

CMOS PAs often use a pseudodifferential pair, cascode devices to provide high output power. Thick gate-oxide devices are used in the common gate device to sustain gate–drain voltage stress in a high output power level. In this design, the PA is targeted to deliver an average output power of 10 dBm for VHT80, MCS10 802.11ax signal. To meet the requirement of the average output power of 10 dBm with at least 10-dB PAPR of the signal, the saturated output power of PA should be larger than 22 dBm. Thus, the transistor sizes of the common source and common gate devices are set to 0.896 mm/40 nm and 1.536 mm/270 nm, respectively, such that the PA can deliver a maximum output power of around 24 dBm under a supply voltage of 2.5 V. For the differential cascode devices, the optimum load impedance is given by a load resistance in parallel with an equivalent negative output capacitance [9], as

$$Z_{\text{opt}} = R_{\text{opt}} \parallel \left(\frac{-1}{j\omega C_{\text{out}}} \right). \quad (1)$$

In practice, the optimum load impedance is normally determined through load–pull simulation. The load–pull simulation is performed in the Keysight Advanced Design System (ADS) to extract the optimum load impedance at 2.4 and 5.5 GHz. The simulated power contours and power-added efficiency (PAE) contours for the fundamental at 2.4 and 5.5 GHz are demonstrated in Fig. 1. For practical PA design, PAE and output power are two critical performances that should be considered concurrently. In general, rather than to only pursue maximum PAE or maximum output power, a tradeoff between output power and PAE is normally made. In this point of view, the optimum load impedances are determined as $22.1 + j22 \, \Omega$ and $17.3 + j17.8 \, \Omega$ at 2.4 and 5.5 GHz, respectively, as marked in Fig. 1. The corresponding R_{opt} and C_{out} are 44 Ω and 1.5 pF at 2.4 GHz and are 35.6 Ω and 0.82 pF at 5.5 GHz.

B. Dual-Band Output Matching Network Design

The basic prototype of the reconfigurable dual-band output matching network using switchable capacitors is shown

Fig. 2. Prototype of the reconfigurable dual-band output matching network.

Fig. 3. Equivalent circuit of the dual-band output matching network.

in Fig. 2. In this matching network, the transformer is fixed, while the values of two capacitor C_1 and C_2 are tunable or switchable to adjust the load impedance seen into the matching network to target at the optimum impedances in the two bands of interest. In order to facilitate analysis and design, the equivalent circuit of the output matching network is utilized [20], as shown in Fig. 3. For ideal matching network, the target of matching is equivalent to achieving reflection coefficients $\Gamma_s = 0$ and $\Gamma_L = 0$ simultaneously. In practice, the ideal matching network is unachievable. Hence, we set $|\Gamma_s| \leq -20$ dB and $|\Gamma_L| \leq -15$ dB as the target for the output matching network to be designed in this work. $|\Gamma_s|$ and $|\Gamma_L|$ can be derived as

$$\Gamma_s = 20 \log \left| \frac{R_{\text{opt}} - Z_{\text{inS}}}{R_{\text{opt}} + Z_{\text{inS}}} \right| \quad (2)$$

$$\Gamma_L = 20 \log \left| \frac{50 - Z_{\text{inL}}}{50 + Z_{\text{inL}}} \right| \quad (3)$$

where

$$Z_{\text{inS}} = \frac{Z_A + R_1 + j\omega(L_1 - L_M)}{1 + j\omega(Z_A + R_1 + j\omega(L_1 - L_M)) \cdot (C_1 + C_{\text{out}})} \quad (4)$$

$$Z_{\text{inL}} = \frac{Z_B + R_2 + j\omega(L_2 - L_M)}{1 + j\omega C_2(Z_B + R_2 + j\omega(L_2 - L_M))} \quad (5)$$

and

$$Z_A = \frac{j\omega L_M(-\omega(L_2 - L_M + 50R_2C_2) + 50(1 - (L_2 - L_M)C_2))}{50(1 - (L_2 - L_M)C_2) + j\omega(L_2 + 50R_2C_2)} \quad (6)$$

$$Z_B = \frac{-\omega^2 L_M(L_1 - L_M + R_{\text{opt}}C_1' + j\omega L_M R_{\text{opt}}(1 - (L_1 - L_M)C_1'))}{R_{\text{opt}}(1 - (L_1 - L_M)C_1') + j\omega(L_1 + R_{\text{opt}}C_1')} \quad (7)$$

$$C_1' = C_1 + C_{\text{out}} \quad (8)$$

$$R_1 = \frac{\omega L_1}{Q_1}, R_2 = \frac{\omega L_2}{Q_2}. \quad (9)$$

Now, in the equivalent circuit shown in Fig. 3, there are four main parameters (L_1 , L_2 , C_1 , and C_2) to be determined. Given

Fig. 4. Range of L_1 and L_2 where optimum impedances can be achieved at 2.4 and 5.5 GHz.

the matching target at 2.4 and 5.5 GHz, first, we sweep the value of L_1 and L_2 and explore the range of L_1 and L_2 , where C_1 and C_2 have the solutions. In this procedure, the quality factor of the primary and secondary windings of the transformer are both assumed to be 15, which is a normal value for practical transformers. Besides, the solutions of C_1 and C_2 are constraint in the range of 0–6 pF, and the solutions of C_1 and C_2 above 6 pF are regarded as unreasonable and are abandoned. Here, we investigate the range of L_1 and L_2 , assuming the coupling factor of 0.67, which is a reasonable value when the primary and secondary windings are implemented in the same top metal layer.

The calculated range is plotted in the region in Fig. 4. This range of L_1 and L_2 can guarantee that C_1 and C_2 have the solutions such that the matching targeted ($|\Gamma_s| \leq -20$ dB and $|\Gamma_L| \leq -15$ dB) are achieved at the two specific frequencies. To extract the optimum value of L_1 and L_2 regarding efficiency, it is desirable to investigate the efficiency of the transformer in the achieved range of L_1 and L_2 . Assuming that the quality factors of the capacitors are high enough, the efficiency η can be expressed as [21]

$$\eta = \frac{R_L' \omega^2 L_M^2}{R_1 \left[(R_2 + R_L')^2 + \omega^2 L_2 - \frac{50^2 C_2}{1 + (50\omega C_2)^2} \right] + \omega^2 L_M^2 (R_2 + R_L')} \quad (10)$$

where

$$R_L' = \frac{50}{1 + (50\omega C_2)^2}. \quad (11)$$

The calculated efficiency η from (10) in the achieved range of L_1 and L_2 at 2.4 and 5.5 GHz is illustrated in Fig. 5. Obviously, the selection of L_1 and L_2 has a significant impact on the transformer's efficiency. Fig. 5 can provide rough guidance on the selection of L_1 and L_2 to maximize the transformer's efficiency, while, in practical circuits, the values of C_1 and C_2 are switched by turning the switches ON and OFF, as shown in Fig. 6. When the switches are turned on to increase the value of C_1 and C_2 at 2.4 GHz, the ON-resistances of the switches will decrease the quality factor of C_1 and C_2 and reduce the efficiency of the output matching network. Consequently, to determine the optimum value of L_1 and L_2 , it is indispensable to take the ON-resistance of the switches into account in estimating the efficiency of the

Fig. 5. Efficiency contours of output matching network in achieved range, and unit in contours is %.

Fig. 6. Equivalent practical circuit of the dual-band output matching network.

output matching network at 2.4 GHz. In such a case, the efficiency η' is expressed as (12), shown at the bottom of this page, and the details on the calculation of the efficiency η' is presented in the Appendix. The ON-resistance of the switches R_{SW1} and R_{SW2} depends on the transistor size of the switches, which will be discussed in Section II-C. Here, the ON-resistances R_{SW1} and R_{SW2} are both set at 1.5Ω , which is a reasonable value for a practical switch transistor. Given the value of R_{SW1} and R_{SW2} , the calculated efficiency contours at 2.4 GHz in the determined range of L_1 and L_2 are plotted in Fig. 7(a). Considering the efficiency both at 2.4 and 5.5 GHz, the optimum selection of L_1 and L_2 is marked in Fig. 7. From Fig. 7, the optimum values of L_1 and L_2 are 1 and 1.38 nH, respectively, and the calculated efficiencies are both above 76% at 2.4 and 5.5 GHz. Accordingly, the solutions of C_1 and C_2 are 1.6 and 2.08 pF at 2.4 GHz and 0 and 0.62 pF at 5.5 GHz, respectively. Then, the achieved $|\Gamma_s|$ and $|\Gamma_L|$ are both below -20 dB at 2.4 and 5.5 GHz.

C. Implementation of Output Matching Network

We have so far determined the optimum values of the components in the reconfigurable dual-band matching network; now, we step to implement the matching network with these values. The detailed schematic of the matching network is presented in Fig. 8. In practical implementation, L_1 of 1 nH and L_2 of 1.38 nH cannot be realized by a transformer with a coupling factor of around 0.67. To solve this problem, a series connection of a transformer with the winding ratio of 2:2 and

Fig. 7. Efficiency contours of output matching network with considering ON-resistance of switches, and unit in contours is %.

Fig. 8. Implemented dual-band output matching network.

an inductor with the inductance of around 0.35 nH are utilized to form a new equivalent transformer with the desired value of L_1 , L_2 , and k [22]. For the transformer in series with the inductor, the inductance L_1 and L_{2b} are both around 1 nH, the quality factors Q_1 and Q_{L2b} are 14.7–18.2 and 13–16, and the coupling factor k' between the two windings is 0.74–0.78 from 2.4 to 6 GHz, respectively. The equivalent parameters L_2 , k , and Q_2 of the new equivalent transformer are given by [22]

$$L_2 = L_{2a} + L_{2b} \quad (13)$$

$$Q_2 = \frac{\omega L_2}{\frac{\omega L_{2a}}{Q_{2a}} + \frac{\omega L_{2b}}{Q_{2b}}} \quad (14)$$

$$k = \frac{k' \sqrt{L_1 L_{2a}}}{\sqrt{L_1 + L_2}}. \quad (15)$$

Consequently, the parameters of the new transformer are $L_1 = 0.978$ nH, $L_2 = 1.375$ nH, $k = 0.656$, and $Q_1 = 14.74$, $Q_2 = 12.07$ at 2.4 GHz; $L_1 = 1.035$ nH, $L_2 = 1.42$ nH, $k = 0.69$, $Q_1 = 18.1$, and $Q_2 = 15.1$ at 5.5 GHz.

The switches SW1 and SW2 are implemented using two-stacked thick gate-oxide transistors, mainly based on the consideration of reliability in the OFF-state [23], [24]. To reduce the loss caused by the ON-resistance of the switch, the transistor's size should be as large as possible since the ON-resistance is inversely proportional to the transistor size. On the other hand, the large transistor size of the switch results in large parasitic capacitance in the OFF-state, which cannot

$$\eta' = \frac{50}{\left| 1 + \frac{jQ_{2b}L}{1+jQ_{2b}} + jQ_{2a}L \right|^2} \cdot \frac{\left| \frac{j\omega L_2 + R_2 + Z_1}{\omega^2 L_M^2} + R_2 + \left| \frac{Z_2 C_{1b}(j\omega L_2 + R_2 + Z_1)}{(1+jQ_{1b})L_M} \right|^2 R_{SW1} + \frac{Q_{2b}^2 \cdot R_{SW2}}{\left| 1 + \frac{jQ_{2b}L}{1+jQ_{2b}} + jQ_{2a}L \right|^2} + \frac{50}{\left| 1 + \frac{jQ_{2b}L}{1+jQ_{2b}} + jQ_{2a}L \right|^2} \right|} \quad (12)$$

Fig. 9. ON-resistance and C_{OFF} of switch transistor versus size.

Fig. 10. Schematic of dual-band output matching network in (a) “ON” and (b) “OFF” states.

be ignored in practical design. In the procedure of determining the optimum values of components in the matching network, the capacitance of the switch in OFF-state is not taken into account. The ON-resistance (R_{ON}) and the capacitance (C_{OFF}) in the OFF-state have been simulated for different transistor sizes, as shown in Fig. 9. In this design, the transistor sizes of SW1 and SW2 are both 1.536 mm/270 nm. Under this size, the transistor has R_{ON} of 0.75 Ω and C_{OFF} of 0.77 pF. Correspondingly, the ON-resistance R_{SW} and OFF-capacitance C_{SW-OFF} of the switches consisting of two stacked transistors are 1.5 Ω and 0.385 pF. In Section II-B, the calculated optimum values of C_2 are 2.08 and 0.62 pF when the switches are in “ON” and “OFF” states, respectively. Accounting for C_{SW-OFF} of 0.385 pF, the C_{2a} and C_{2b} are 0.235 and 1.69 pF in the implemented circuit. Since the desired C_1 is 1.6 and 0 pF at 2.4 and 5.5 GHz, respectively, C_{1a} and $2C_{1b}$ are set at 0 and 3.2 pF. The actual circuit of the output matching network when the switches are in the “ON” and “OFF” states is shown in Fig. 10, respectively. In the “OFF” state, the final C_1 is 0.31 pF rather than 0 pF at 5.5 GHz due to C_{SW-OFF} . Consequently, the resulted load impedance is $25.6 + j12.6 \Omega$

Fig. 11. Achieved load impedance of implemented output matching network in 2.4- and 5-GHz bands. (a) 2.4 GHz. (b) 5.5 GHz. (c) 4.9 GHz. (d) 5.9 GHz.

at 5.5 GHz when the switches are OFF and is $21 + j18.1 \Omega$ at 2.4 GHz with the switches turned on. As shown in Fig. 10, the deviation between the achieved load impedance and the optimum impedance results in the PAE degradation by 3% at 5.5 GHz, which is acceptable in practice. Finally, the loss of the implemented output matching network is 1.45 and 1.25 dB at 2.4 and 5.5 GHz, and the efficiency of the implemented output matching network is 71.6% and 75% at 2.4 and 5.5 GHz, respectively. In comparison, the passive efficiency of the matching network in [7] is $\sim 70\%$, and that in [9] is 64.2% and 68.5% at 3 and 9 GHz. Furthermore, to verify the matching performance in the whole 5-GHz band, the achieved load impedances at 4.9 and 5.9 GHz are also demonstrated in Fig. 11 together with the load-pull simulation results. Across the 5-GHz band, PAE will degrade by 3%, and the output power will decrease by at most 0.3 dB due to the deviation between the achieved impedance and the optimum impedances. Thus, the impedance matching network can be designed in the whole 5-GHz band with a little performance degradation.

III. TRANSMITTER FRONT-END DESIGN

The diagram of the proposed transmitter front end is shown in Fig. 12, including a local oscillator (LO) generator, a tunable low-pass filter (LPF), an active mixer, a third-order bandpass interstage matching, and the PA stage.

A. LPF and Mixer

Since 802.11ax signals have different bandwidths, the cutoff frequency of the analog baseband (BB) LPF is required to be

Fig. 12. Diagram of transmitter front end.

Fig. 13. Schematic of LPF.

Fig. 14. Schematic of the mixer.

adjustable accordingly. In the proposed transmitter front end, the Tow-Tomas biquad filter is used [25], as shown in Fig. 13. In order to tune the filter's cutoff frequency, a programmable capacitor network is used, and the cutoff frequency is given by

$$f_0 = \frac{1}{2\pi \sqrt{R_2 R_3 C_1 C_2}}. \quad (16)$$

Since the analog bandwidth of 802.11ax BB signal is half of the bandwidth of the signal, the tunable 3-dB cutoff frequencies of the filter are set to 15, 30, and 60 MHz for 802.11ax signal with 20-, 40-, and 80-MHz bandwidths, respectively.

Mixer design requires many compromises among different figures of merit, such as conversion gain, LO power, linearity, noise figure, port-to-port isolation, and total power dissipation. In this work, an active mixer is used rather the counterpart passive mixer, by the virtue of high conversion gain and large port isolation, and the proposed mixer is shown in Fig. 14 [2], [26], [27]. The mixer is driven by a quadrature 50% duty-cycle clock, which is generated from the LO generation block. A 5-bit current-steering gain control unit is stacked on the mixer, and the range of the control gain is around 24 dB.

In order to keep sufficient voltage headroom and deliver a high output power, the supply voltage for the mixer is chosen to be 2.5 V, and thick gate-oxide transistors are used in the current-steering gain control unit [2], [27].

B. Interstage Matching Between Mixer and PA Stage

The interstage matching is designed as a third-order bandpass matching [15], [16], which can cover the frequency range from 2 to 6 GHz. Since the mixer can be approximated as the current source, the bandpass matching can achieve a constant transimpedance transfer function, providing flat driving power to the following PA across a broad operating band. The interstage matching is designed based on the third-order Chebyshev low-pass prototype with a 0.5-dB ripple. In the proposed transmitter front end, the mixer drives the PA directly without any driver between the mixer and the PA. Otherwise, one more interstage matching between the driver and PA is required, which will intensify the design complexity and increase the chip size. The main advantage of the broadband interstage matching between the mixer and PA is the reduction of chip size since no driver is required and no more interstage matching is necessary between the driver and PA.

Fig. 15. Interstage matching and Norton transformation.

Therefore, the load impedance for the mixer should be large enough to ensure a sufficient transmission gain from the mixer to PA. In the PA's input side, a 50- Ω resistor is used to reduce $G_{\max}$ and ensure stability. A generic double-termination third-order bandpass network has equal impedances at two terminations; thereby, the mixer will have a low load impedance. As a result, it will cause a low transmission gain and insufficient power from the mixer to drive the PA. To address this issue, a Norton transformation is employed to boost the load impedance from 50 to 200 Ω for the mixer and increase the mixer's output power [15]. The design procedure of the interstage matching is illustrated in Fig. 15. Although four inductors are used in the interstage matching network, the total area of the matching network is only $0.33 \times 0.35 \text{ mm}^2$.

For CMOS PAs, the AM-PM distortion is a major contributor to EVM. The nonlinear variation of the gate-source capacitance of input NMOS transistors with gate-source voltage results in the AM-PM distortion. To mitigate this issue, PMOS varactors are added to compensate for the nonlinear input capacitance of input NMOS transistors [16], [28], [29]. Meanwhile, the PMOS varactors also serve as a capacitor in the interstage matching together with the input capacitance of the PA's input NMOS transistors.

C. LO Generator

Since PLL is not integrated on-chip and an external signal source will be used to provide the LO input signal, a balun is required to convert the single-ended LO input signal to a differential signal. In this work, an active balun is used due to its smaller size [30] compared with the passive balun. The simulated gain imbalance of the balun is less than 0.2 dB, and the simulated phase difference is $180 \pm 1.5^\circ$ from 0.5 to 20 GHz, showing an excellent differential performance. On the other hand, the phase noise of this active balun should be low enough, such that the balun has a negligible impact on the phase noise of the input signal. For 11-GHz input frequency, the simulated phase noise of

the balun is -134.1 and -142.4 dBc/Hz at 0.1- and 1-MHz offsets. For 4.8-GHz input frequency, the simulated phase noise is -136.7 and -145.1 dBc/Hz at 0.1- and 1-MHz offsets. The simulated phase noises indicate that the balun exhibits a quite low phase noise.

The divider to generate a 50% duty-cycle clock uses current-mode logic (CML) latch, which has the advantage of high speed.

The LO phase noise significantly impacts EVM, especially for 1024-QAM modulation. In practice, jitter is often used to quantify integrated LO phase noise in broadband communication systems. EVM can be derived as [31]

$$\text{EVM} = 100\% \cdot \sqrt{2 - 2e^{-(2\pi f_c J)^2/2}}. \quad (17)$$

To achieve lower than 0.5% (-46 dB) EVM, the jitters are required lower than 331.6 and 144.7 fs for 2.4 and 5.5 GHz, respectively. The simulated jitters of the LO generator, including the balun, divider, and buffer, are 9.96 and 7.45 fs at 2.4 and 5.5 GHz, respectively. Excluding the phase noise contribution from the LO generator, the jitters of the external signal source are required to be lower than 331.4 and 144.5 fs for 4.8- and 11-GHz input signals, respectively. In the measurement, the jitter of the external signal sources to provide LO input is lower than 40 fs below 12 GHz.

IV. MEASUREMENT RESULTS

First, to verify the proposed reconfigurable dual-band output matching design methodology, a standalone PA was designed and fabricated in the TSMC 40-nm RF CMOS process with ten metal layers. The schematic of this PA is presented in Fig. 16, and the PA has the same core transistors and output matching network proposed in Section II as the transmitter front end has. With a die area of $1.28 \times 0.56 \text{ mm}^2$, the micrograph of the fabricated PA is shown in Fig. 17(a). Second, the transmitter front end was fabricated in the same CMOS process. Fig. 17(b) depicts the micrograph of the fabricated transmitter front-end chip with a dimension of $1.94 \times 0.54 \text{ mm}^2$.

A. PA Measurement

1) *Performance With Continuous-Wave Signals:* The PA is biased in class-AB condition with a quiescent current of 41 mA under a supply voltage of 2.5 V, based on the tradeoff between linearity and efficiency. Small-signal S-parameters were measured to validate the basic amplification function. The measured S-parameters are plotted in Fig. 18 as well as the simulated results, indicating that the PA has the small-signal gain around 10 dB at 2.4 GHz and from 5 to 6 GHz.

To characterize the power gain, output power, and efficiency of the PA, CW signals were employed as the stimulus to the PA from 2.1 to 2.9 and from 4.8 to 6.2 GHz. Fig. 19 depicts the measurement results, in terms of maximum PAE, saturated output power (P_{sat}), and power gain. In the interested 2.4- and 5-GHz bands, P_{sat} 's are 23 and 21.9–22.4 dBm, and PAEs are 27% and 24.2%–28.2%, respectively. Besides, the power gain of the PA is 9.2 and 11.3–11.9 dB at 2.4 and in 5–6 GHz, respectively. Moreover, the measured power gain and PAE versus output power at 2.4 and 5.5 GHz are depicted

Fig. 16. Schematic of standalone PA.

Fig. 17. Photograph of die. (a) Standalone PA. (b) Transmitter front end.

Fig. 18. Measured S-parameters. (a) 2.4-GHz mode. (b) 5-GHz mode.

in Fig. 20. In addition, the main single-tone CW performance of the proposed PA is summarized and compared with other broadband PAs and reconfigurable dual-band PAs in Table I, illustrating that the proposed PA outperforms other broadband and dual-band PAs in PAE.

2) *Performance With Modulation Signals*: To verify the PA's practical performance for 802.11ax application, the PA was tested using a VHT20, MCS5 signal (20-MHz bandwidth, 64-QAM modulation, 3/4 code rate), a VHT40, MCS10, signal (40-MHz bandwidth, 1024-QAM, 3/4 code rate, 10.3-dB PAPR), and a VHT80, MCS10 signal (80-MHz bandwidth, 1024-QAM, 3/4 code rate, 11-dB PAPR). The measurement platform is shown in Fig. 21(a), and no predistortion (DPD) is used in EVM measurement [33].

Fig. 19. Measured P_{sat} , power gain, and PAE_{max} at different frequencies. (a) 2.4-GHz mode. (b) 5-GHz mode.

Fig. 20. Measured power gain and PAE versus output power. At (a) 2.4- and (b) 5.5-GHz modes.

EVM was first measured across the 5-GHz band, and the measured results are reported in Fig. 22. For the VHT80, MCS10 signal, when EVM is -35 dB, the PA delivers an average output power of 10.95–12.16 dBm and achieves a PAE of 7.3%–10.1% in the 5-GHz band. Although the standard EVM requirement for 1024-QAM modulation is -35 dB [34]–[36], the PA should have a more stringent EVM requirement, and at least, the 3-dB margin of EVM is necessary for the PA. At -38 -dB EVM, the PA delivers an average output power of 7–9.3 dBm with 4.1%–6.2% PAE in the 5-GHz band.

Then, EVM was measured at 2.442 GHz (Channel-7), and the measured EVM in different output power levels and the corresponding PAEs are plotted in Fig. 23(a). For the VHT40, MCS10 signal, the PA delivers 12.8-dBm average output power with 9% PAE when EVM is -35 dB. When satisfying -38 -dB EVM, the PA delivers 10.2-dBm average output power with 5.7% PAE.

Besides, EVM was measured from 2.1 to 3 GHz, and the results are reported in Fig. 23(b). Finally, a detailed

TABLE I
COMPARISON WITH OTHER BROADBAND AND DUAL-BAND PAs

Ref.	Freq (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	VDD	Chip Area (mm ²)	Technology
[7]	2.5/3/3.5	~15	22.5/21.5	16.5/15 (DE)	1.2	2.97	65nm CMOS
[8]	3.1/8	17/7.5	24.3/21.2	33.4/7.7	3.6	0.825	180nm CMOS
[16]	2-6	22.8-24.4	20.1-22.4	19-28.4	3.3	0.895	65nm CMOS
[32]	2.6/4.5	24-27	28.1/26	35.2/21.2	3	2.25	65nm CMOS
This work	2.4/ 4.9-5.9	9.2/ 11.3-11.9	23/ 21.9-22.4	27/ 24.2-28.2	2.5	0.72	40nm CMOS

TABLE II
PERFORMANCE COMPARISON OF STATE-OF-THE-ART 802.11ac PAs

Ref.	Technology	Modulation	Bandwidth (MHz)	Pout (dBm)	EVM (dB)	PAE (%)	VDD (V)	Area (mm ²)
This work	40nm CMOS	11ax 1024-QAM	80	12.1	-35	10.1	2.5	0.72
				9.3	-38	6.2		
		11ax 64-QAM	20	14	-28	14.1		
TMTT'2017 [37]	0.13μm CMOS	11ac 256-QAM	80	15.6	-35	7.5	3.6	0.62
JSSC'2015 [38]	40nm CMOS	11ac 64-QAM	40	15.3	-28	13.6	2.5	1.07
RFIC'2015 [3]	40nm CMOS	11ac 256-QAM	80	14.8	-32	9.3	2.4	N.A
RFIC'2015 [39]	SiGe BiCMOS	11ac 256-QAM	80	17	-35	7.8	3.3	1.6
RFIC'2012 [40]	SiGe BiCMOS	11ac 64-QAM	80	17.7	-34	10.1	3.3	2.4

Fig. 21. EVM measurement setup. (a) PA measurement. (b) Transmitter front-end measurement.

comparison between the performance of the proposed dual-band PA and other PAs designed for 5-GHz WLAN 802.11ac/ax is given in Table II.

B. Transmitter Measurement

The measurement setup is shown in Fig. 21(b), and the BB signal is generated from the arbitrary waveform generator (AWG: 81180A). The sampling rates of the DACs in AWG are 320, 160, and 80 Msamples/s for the 802.11ax BB signals with

Fig. 22. Measured EVM performance in a 5-GHz band. EVM and PAE in different average output power levels for (a) 20-MHz, 64-QAM signal and (b) 80-MHz, 1024-QAM signal. (c) P_{avg} and PAE versus frequencies at different EVMs.

80-, 40-, and 20-MHz bandwidths, respectively. RF output signal is sampled using the Keysight DSOZ634A oscilloscope and demodulated in Keysight 89600. EVM was first measured in the 5-GHz mode by using the VHT20, MCS5 signal at 5.18, 5.56, and 5.825 GHz, in Channels 36, 112, and 165 and then measured by using the VHT80, MCS10 signal at 5.21, 5.53, and 5.775 GHz in Channels 42, 106, and 155.

The measured EVM in different average output power levels is reported in Fig. 24. For the VHT80, MCS10 signal,

Fig. 23. Measured EVM performance in the 2.4-GHz mode. (a) EVM and PAE in different average output power levels at 2.442 GHz. (b) P_{avg} and PAE versus frequencies at different EVMs.

Fig. 24. Measured EVM versus output level for different modulation signals in the 5-GHz mode.

Fig. 25. Measured EVM in different output levels for the modulation signal at 2.442 GHz.

when satisfying the system-level standard specification of $EVM \leq -35$ dB, the transmitter delivers an average output power of 6.72, 6.91, and 6.95 dBm at 5.21, 5.53, and 5.775 GHz, respectively. Then, the transmitter was measured at 2.442 GHz, and the measured EVM versus the average output power is reported in Fig. 25. The transmitter delivers 10.8- and 8.1-dBm average output powers when $EVM \leq -28$ dB for the VHT20, MCS5 signal and $EVM \leq -35$ dB for the VHT40, MCS10 signal, respectively. Since the PAPR of the VHT80, MCS10 signal is as high as 11 dB, a large back-off is required for the transmitter to meet the stringent EVM requirement of -35 dB for 1024-QAM modulation without using DPD. If DPD is employed, the average output power will be increased by a large degree, while it is beyond the scope of this article.

In addition, the measured 1024-QAM constellation for the VHT80, MCS10 signal with -37.4 -dB EVM at 5.53 GHz is illustrated in Fig. 26. Besides, the output spectrum with -35 -dB EVM for the VHT80, MCS10 signal at 5.53 and the VHT40, MCS10 signal at 2.442 GHz is depicted in Fig. 27. Fig. 27 shows that the requirement of an emission mask is

Fig. 26. Measured 1024-QAM constellation.

Fig. 27. Output spectrum from transmitter front end. (a) VHT80, MCS10 signal at 5.53 GHz. (b) VHT40, MCS10 signal at 2.442 GHz.

satisfied both in 2.4- and 5-GHz modes. Meanwhile, the measured performance is summarized and compared with other recent 2.4-/5-GHz dual-band WLAN transceivers and 5-GHz 802.11ax transmitter in Table III. In these dual-band WLAN transceivers, two separated RF channels are employed to realize a 2.4-/5-GHz dual-band operation, while the dual-band operation can be achieved in the proposed transmitter front end using only one transmitter channel. Compared with the transmitters using two RF channels, the proposed transmitter front end may bring a reduction of chip area for RF part, while the output power of the proposed transmitter front end is smaller than some commercial works. If the proposed

TABLE III
TRANSMITTER FRONT-END PERFORMANCE SUMMARY AND COMPARISON

	This work	ISSCC2018 [6]	ISSCC2017 [4]	JSSC2017 [5]	TMTT2020 [41]
WLAN standards	11abgn/ac/ax	11abgn/ac/ax	11abgn/ac	11abgn/ac	11ax
Process (nm)	40	28	40	40	40
2.4/5G Dual-band	Yes	Yes	Yes	Yes	No
Configuration	Single Transmitter	Multiple Transmitter	Multiple Transmitter	Multiple Transmitter	Single Transmitter
Modulation signal	2.4G VHT40, MCS10,11ax	VHT40, MCS10,11ax	LG54M	LG54M	N.A.
	5G VHT80, MCS10,11ax	VHT80, MCS10,11ax	VHT80, MCS9,11ac	VHT80, MCS9,11ac	VHT80, MCS9,11ax
1024-QAM	Yes	Yes	No	No	No
TX Pout (dBm) @EVM=-35dB	2.4G 8.1	-5	21.3 (EVM=-28dB)	23.5 (EVM=-28dB)	N.A.
	5G 6.95	-5	19 (EVM=-32dB)	17 (EVM=-32dB)	8.3 (EVM=-32dB)
EVM floor	2.4G -42.5	-42.5	N.A.	-40	N.A.
	5G -40	-38.1	-36.8	-38	-38

Fig. 28. Model used to calculate the efficiency of the output matching network.

transmitter front end is used in the access point, an external PA with a 17-dB power gain is required to deliver an output power of 25 dBm.

V. CONCLUSION

In this article, a new reconfigurable dual-band output matching methodology is proposed. Based on the proposed methodology, a transmitter front end and a standalone PA supporting 2.4-/5-GHz dual-band operation are designed for the WLAN 802.11ax application. A step-by-step design procedure of the output matching network and transmitter front end is demonstrated in detail. The measurement results verify the standalone PA, and the transmitter front end can operate both in 2.4- and 5-GHz modes. The standalone PA delivers a P_{sat} of 23 and 21.9–22.4 dBm and features a PAE of 27% and 24.2%–28.2% at 2.4 GHz and in the 5-GHz band, respectively. The PA exhibits a promising performance in comparison with other broadband PAs and reconfigurable dual-band PAs in the literature. In the 5-GHz band, the transmitter achieves an average output power of 6.72–6.95 dBm with the EVM of –35 dB for 80-MHz, 1024-QAM WLAN 802.11ax signal without DPD, while, in the 2.4-GHz operating mode, the transmitter delivers 8.1-dBm average output power satisfying –35-dB EVM for the 40-MHz, 1024-QAM signal.

APPENDIX

SWITCHABLE OUTPUT MATCHING NETWORK EFFICIENCY CALCULATION

The transformer's efficiency η' is defined as the ratio of the power P_{load} dissipated in the output termination load (50 Ω)

and the total power P_{total} dissipated in all the resistors (R_1 , R_2 , R_{SW1} , and R_{SW2}) and the output termination load [21], given by

$$\eta' = \frac{P_{\text{load}}}{P_{\text{total}}} = \frac{|I_6|^2 \cdot 50}{|I_1|^2 R_1 + |I_2|^2 R_2 + |I_3|^2 R_{\text{SW1}} + |I_4|^2 R_{\text{SW2}} + |I_6|^2 \cdot 50} \quad (18)$$

To facilitate the calculation of the efficiency η' , two impedances Z_1 and Z_2 seen from different planes are employed, as shown in Fig. 28, which can be derived as follows:

$$Z_1 = \frac{1 + j\omega R_{\text{SW2}} C_{2b}}{\left(\frac{1}{50} - \omega^2 R_{\text{SW2}} C_{2a} C_{2b}\right) + j\omega(C_{2a} + C_{2b}) + \frac{R_{\text{SW2}} C_{2b}}{50}} \quad (19)$$

$$Z_2 = \frac{j\omega L_M (Z_1 + j\omega(L_2 - L_M) + R_2)}{Z_1 + j\omega(L_2 - L_M) + R_2 + j\omega L_M} + j\omega(L_1 - L_M) + R_1. \quad (20)$$

Based on Kirchhoff's equations, the relationship between the currents I_1 , I_3 , I_4 , and I_6 and the current I_2 can be written as

$$I_1 = I_2 \frac{j\omega L_2 + R_2 + Z_1}{j\omega L_M} \quad (21)$$

$$I_3 = I_2 \frac{Z_2 C_{1b} (j\omega L_2 + R_2 + Z_1)}{(1 + jQ_{1b}) L_M} \quad (22)$$

$$I_4 = I_2 \frac{jQ_{2bL}}{1 + \frac{jQ_{2bL}}{1 + jQ_{2b}} + jQ_{2aL}} (1 + jQ_{2b}) \quad (23)$$

$$I_6 = I_2 \frac{1}{1 + \frac{jQ_{2bL}}{1 + jQ_{2b}} + jQ_{2aL}} \quad (24)$$

where

$$Q_{1b} = \omega C_{1b} R_{\text{SW1}} \quad (25)$$

$$Q_{2aL} = \omega C_{2a} \cdot 50 \quad (26)$$

$$Q_{2b} = \omega C_{2b} R_{\text{SW2}} \quad (27)$$

$$Q_{2bL} = \omega C_{2b} \cdot 50. \quad (28)$$

Substituting (21)–(24) into (18), the efficiency η' can be obtained as (12).

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Bei Liu (Student Member, IEEE) received the B.E. degree in electric and information engineering from Northwestern Polytechnical University (NWPU), Xi'an, China, in 2009, and the M.S. degree from Xidian University, Xi'an, in 2012. He is currently pursuing the Ph.D. degree at Nanyang Technological University (NTU), Singapore.

From 2012 to 2014, he was with the State Radio Monitoring Center, Xi'an, where he focused on signal analysis, spectrum allocation, and radio monitoring techniques. His current research interests include CMOS power amplifier, carrier aggregation transmitters, and GaN monolithic microwave integrated circuit (MMIC) power amplifiers for wireless communication.

Xing Quan was born in Shiyan, Hubei, China, in 1989. He received the B.S. and Ph.D. degrees from Xidian University, Xi'an, China, in 2012 and 2018, respectively.

He was a Research Associate with VIRTUS, IC Design Centre of Excellence, School of Electrical and Electronics Engineering, Nanyang Technological University (NTU), Singapore, from August 2016 to September 2017. He currently holds a post-doctoral position at Xidian University. His current research interests include the MMICs, active-phase shifter, and the front-end design of transceiver.

Dr. Quan was a recipient of the Outstanding Reviewer for *Microelectronics Journal*. He also serves as a Reviewer for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, the *IET Microwaves, Antennas & Propagation*, the *Microelectronics Journal*, and the *Microwave and Optical Technology Letters*.

Chirn Chye Boon (Senior Member, IEEE) received the B.E. (Hons.) and Ph.D. degrees in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was with Advanced RFIC, Singapore, where he was a Senior Engineer. Since 2005, he has been with NTU, where he is currently an Associate Professor. He has been the Programme Director of RF and MM-wave research in the S\$50 million research center of excellence, VIRTUS, NTU, since March 2010. He specializes in the areas of radio frequency (RF) and mm-wave circuits design for communications applications.

He has conceptualized, designed, and silicon-verified many circuits/chips resulting in over 150 refereed publications and 15 patents in the fields of RF and MM-wave. He is a coauthor of the books *Design of CMOS RF Integrated Circuits and Systems* and *CMOS Millimeter-Wave Integrated Circuits for Next Generation Wireless Communication Systems* (World Scientific Publishing).

Dr. Boon also serves as a committee member for various conferences. He is one of the key NTU-team members of MIT-NTU joint collaboration project "Low Energy Electronic Systems," which has won the Singapore-MIT Alliance for Research and Technology (SMART) International Research Grant (IRG) proposal with a grant total of S\$25 million. He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is also the IEEE Electron Devices Letters Golden Reviewer. He is also the Principal Investigator for research grants of over S\$10 million.

Devrishi Khanna (Member, IEEE) received the B.Tech. degree in electronics and communication engineering from the Jaypee Institute of Information Technology University (JIITU), Noida, India, in 2009, and the M.Sc. degree in integrated circuit (IC) design through the Joint Degree Program from Nanyang Technological University and the Technical University of Munich (NTU-TUM), Singapore, in 2014.

From 2009 to 2012, he worked in industry as an RF system-design engineer, where he was directly involved in the design of LTE-WCDMA base-station transceiver boards. Since 2014, he has been a member of the Research Staff with the School of Electrical and Electronic Engineering, NTU. His research interests include switched-capacitor circuits, charge pumps, precision analog IC design, and phase-locked loops (PLLs).

Pilsoon Choi (Senior Member, IEEE) received the Ph.D. degree in electrical engineering and computer science (EECS) from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2004.

While with KAIST, he developed the first IEEE 802.15.4 CMOS radio for a low-power wireless sensor network that is now the Internet of Things (IoT). From 2004 to 2011, he was with Samsung Electronics, Seoul, South Korea, where he developed the first wireless codec SoC for real-time HD video streaming and was also involved in international standardization. Since 2012,

he has been leading a communication circuit design team of the Low Energy Electronic Systems (LEES) research program. He is currently a Research Scientist with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. His research interests include RF signal-processing and energy-processing circuits design in III-V and CMOS technologies.

Xiang Yi (Senior Member, IEEE) received the B.E. degree from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2006, the M.S. degree from the South China University of Technology (SCUT), Guangzhou, China, in 2009, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2014.

He was a Research Fellow with NTU from 2014 to 2017. He is currently a Post-Doctoral Fellow with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. His research interests include

radio frequency (RF), millimeter-wave (mm-wave), and terahertz (THz) frequency synthesizers and transceiver systems.

Dr. Yi was a recipient of the IEEE ISSCC Silkroad Award and the SSCS Travel Grant Award in 2013. He is also a technical reviewer for several IEEE journals and conferences.