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A 93.4–104.8-GHz 57-mW Fractional- N Cascaded PLL With True In-Phase Injection-Coupled QVCO in 65-nm CMOS Technology

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Abstract—A fully integrated 93.4–104.8-GHz 57-mW fractional- N cascaded phase-locked loop (PLL) with true in-phase injection-coupled quadrature voltage-controlled oscillator (QVCO) is reported. By cascading the fractional- N PLL and the subsampling PLL, good phase noise, high resolution, and wide acquisition range are achieved simultaneously. The transformer-based true in-phase injection coupled technique is adopted in the QVCO to obtain both low phase noise and low-power consumption. The proposed cascaded PLL was fabricated in a 65-nm CMOS technology with silicon size of 0.88 mm². The measured phase noise of QVCO and PLL is -113.26 and -106.63 dBc/Hz at 10-MHz offset, respectively. The FOM and FOM_T of the QVCO at 10-MHz offset are -178.4 and -180.0 dBc/Hz, respectively. The frequency resolution of the 100-GHz output is less than 3.6 kHz.

Index Terms—Cascaded phase-locked loop (PLL), CMOS voltage-controlled oscillator (VCO), frequency synthesizer, in-phase injection-coupled (IPIC), integrated circuit (IC), low phase noise, millimeter wave (mm-wave), quadrature VCO (QVCO), subsampling PLL (SSPLL), W-band.

I. INTRODUCTION

WITH the progress of CMOS technologies, design of millimeter-wave (mm-wave) integrated circuits (IC) has been developed rapidly in the past decade. f_T and $f_{\max}$ of CMOS transistors continue to rise, pushing the operation frequencies of mm-wave ICs higher and higher. CMOS compatibility with digital circuits makes the whole mm-wave system

integrated in a single chip realizable, so the total cost can be reduced. As a key block in the system, mm-wave phase-locked loop (PLL) has been employed in many applications including high-speed communication, radar, and imaging in recent years. Conventional mm-wave charge-pump PLLs (CPPLLs) suffer from poor phase noise due to the low tank quality factor and large division ratio [1]–[4]. Reported mm-wave PLLs show that the subsampling technique is capable of significantly suppressing the in-band phase noise of PLLs [5], [6]. However, the conventional mm-wave subsampling PLL (SSPLL) also suffers from the problems of low-frequency resolution and narrow acquisition range, which limits the use of PLL in some high-performance applications such as communication and radar.

On the other hand, quadrature signals are commonly used in communication and phased-array systems. However, it is very difficult to generate wideband, low phase noise, low phase error, and low power quadrature signals at mm-wave frequencies in CMOS technology. Adopting a divide-by-2 divider after a VCO is not practical at such high frequencies. The quadrature hybrid coupler method consumes huge power [7]. The use of an injection-locked multiplier suffers from the limited locking range and the intrinsic phase error due to the imbalance of the structure [7]. Therefore, a common and straightforward method is to employ a high-performance quadrature voltage-controlled oscillator (QVCO), i.e., wideband, low phase noise, low phase error, and low power. For example, the tuning range of a conventional single LC tank VCO is limited by the tunable capacitance because the inductance cannot be too small for the given oscillation frequency and power consumption. Usually, there is a tradeoff between the phase noise and the tuning range. What is more, there is other typical tradeoffs between the phase noise and the phase error, as well as the phase noise and power consumption. Therefore, the high-performance mm-wave QVCO is desired.

This paper presents a 93.4–104.8-GHz fractional- N cascaded PLL. The proposed structure utilizes the merits of fractional- N PLL and SSPLL, in order to achieve good phase noise, high-frequency resolution, and wide acquisition range simultaneously. A true in-phase injection-coupled

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Fig. 1. Proposed cascaded PLL architecture.

Fig. 2. Schematic of fractional- N $\Delta\Sigma$ M-PLL.

QVCO (TIPIC-QVCO) is proposed to solve the issues in the conventional QVCO. Thanks to the true in-phase injection coupled technique, we can achieve low phase noise with low-power consumption, and mitigate the tradeoff between the phase noise and the phase error simultaneously. The use of transformer also provides the benefit of higher operation frequency and wider tuning range. This paper is an expanded version from [8]. Detailed analysis and more measurement results are added, including the cascaded PLL architecture and the theory of the TIPIC-QVCO.

This paper is organized as follows. Section II describes the problems of conventional mm-wave CPPLL and SSPLL, then followed by the proposed cascaded PLL architecture and circuit design. Section III presents the analysis and circuit design of the proposed TIPIC-QVCO to provide designers an insight into designing a TIPIC-QVCO. In Section IV, the measurement results are demonstrated and compared to the state-of-the-art works, then the conclusion is drawn in Section V.

II. CASCADED PLL ARCHITECTURE AND CIRCUIT DESIGN

A. Problems of Conventional mm-Wave CPPLL and SSPLL

In a conventional CPPLL, the in-band phase noise $\mathcal{L}_{\text{in-band,CPPLL}}$ is mainly contributed by reference input, phase frequency detector (PFD) and charge pump (CP), and divider. $\mathcal{L}_{\text{in-band,CPPLL}}$ is amplified by the division ratio N^2 . Therefore, $\mathcal{L}_{\text{in-band,CPPLL}}$ degrades significantly when the division ratio N becomes large inevitably in a mm-wave CPPLL. For example, the in-band phase noise will rise 60 dB in a 100-GHz CPPLL with a 100-MHz reference input.

In addition, there is a tradeoff between loop bandwidth and out-of-band phase noise in the fractional- N CPPLL. When the loop bandwidth is narrow, the quantization noise from delta-sigma modulator ($\Delta\Sigma$ M) can be readily filtered out, but the phase noise from VCO cannot be suppressed outside the loop bandwidth. While the loop bandwidth is set wide enough to suppress the phase noise of the VCO, the quantization noise of the $\Delta\Sigma$ M may dominate the out-of-band phase noise of a CPPLL.

To suppress the in-band phase noise, the SSPLL architecture can be adopted. Because the divider is removed from the loop of SSPLL, noise contributed by the divider is eliminated. Due to the elimination of the division ratio N in the gain of subsampling phase detector (SSPD) and CP, the noise from SSPD and CP is not amplified by $20\log(N)$ [9]. Thus, the in-band phase noise of SSPLL, $\mathcal{L}_{\text{in-band,SSPLL}}$, is much smaller than $\mathcal{L}_{\text{in-band,CPPLL}}$. Furthermore, since the loop bandwidth of SSPLL can be much higher, the noise from VCO can be suppressed much better, which leads to a better integrated phase noise.

However, there is an inevitable tradeoff between frequency resolution and acquisition range in the conventional SSPLL. For mm-wave integer- N SSPLL, its frequency resolution is typically equal to the reference frequency or its harmonics [5]. Current fractional- N SSPLL architectures [10]–[13] are still not practical at mm-wave frequencies. For one thing, the mm-wave waveform of SSPLL cannot be modulated directly by $\Delta\Sigma$ M in current CMOS technologies. For another thing, if only the reference input is modulated, the resulting quantization noise becomes too high when the division ratio N is large in a mm-wave PLL. Moreover, due to the sinusoidal characteristic of the SSPD, the acquisition range of the SSPLL is much smaller than the reference frequency if no extra auxiliary loop is in place.

B. Proposed Cascaded PLL Architecture

To overcome the drawbacks of the conventional mm-wave CPPLL and SSPLL, we proposed a cascaded PLL architecture that combines CPPLL and SSPLL. Compared to [14] with the target application for 5G communication, this paper aims for W-band applications. In contrast to the cascaded PLL proposed in [15] which places a high-frequency fractional- N PLL after an integer- N PLL in order to reduce the quantization noise of the $\Delta\Sigma$ M, the proposed cascaded PLL puts a fractional- N PLL in front of a mm-wave integer- N SSPLL. The block diagram of the cascaded PLL is shown in Fig. 1. The first PLL (PLL1) is a fractional- N PLL with a 100-MHz reference input and a 20-bit $\Delta\Sigma$ M, and the second PLL (PLL2) is a 100-GHz integer- N SSPLL. This configuration provides several benefits as shown in the following.

- 1) The overall phase noise is reduced compared with the conventional mm-wave CPPLL [15].
- 2) The frequency resolution ($= f_{\text{ref}} \cdot N_2 / 2^{20}$) is high thanks to the $\Delta\Sigma$ M in PLL1.
- 3) The acquisition range of the SSPLL is improved, because its reference input frequency (f_{out1}) is much higher compared with a single SSPLL.

In short, compared with the conventional fractional- N CPPLL and the conventional SSPLL, the proposed PLL architecture has merits of good phase noise, fine frequency resolution, and wide acquisition range as summarized in Table I.

Generally, the in-band phase noise is dominated by the reference input, especially when the total division ratio N is large. We can choose a narrow loop bandwidth for PLL1, so the $\Delta\Sigma$ M quantization noise is suppressed. Now, the phase noise of the cascaded PLL between PLL1's bandwidth and PLL2's bandwidth is mainly determined by the multiplication

TABLE I
MM-WAVE PLL ARCHITECTURE COMPARISON

PLL Architecture	Phase Noise	Frequency Resolution	Acquisition Range
Fractional- N CPPLL	Poor	Good	Wide
SSPLL	Good	Poor	Narrow
Proposed Cascaded PLL	Good	Good	Wide

of PLL2 (N_2), and the phase noise from the first VCO in PLL1 ($\mathcal{L}_{VCO1}$) [14]: $N_2^2 \cdot \mathcal{L}_{VCO1}$. The phase noise of the cascaded PLL outside PLL2's bandwidth is mainly from the second VCO in PLL2 ($\mathcal{L}_{VCO2}$): $\mathcal{L}_{VCO2}$. We can choose a wide loop bandwidth for PLL2 and smaller N_2 , so the overall phase noise can be reduced. Smaller N_2 also means larger output frequency of PLL1 f_{out1} , which should be much higher than the frequency band spacing of VCO in SSPLL in order to avoid the SSPLL locking to the wrong frequency caused by its locking mechanism and the process, voltage, and temperature (PVT) variations. On the other hand, f_{out1} should not be too large as it is also limited by the subsequent blocks. After considering both limitations, we choose $f_{out1} = 2.7 \sim 2.8$ GHz. Therefore, the SSPLL works as a multiplier with $N_2 = 34 \sim 38$, and the frequency resolution of the cascaded PLL is $f_{ref} \cdot N_2 / 2^{20} < 3.6$ kHz (or $0.000036 f_{ref}$) when PLL1 works in the fractional- N mode. It is noted that the loop bandwidths of both PLL1 and PLL2 are limited by other system parameters such as CP current, VCO gain, and low-pass filter (LPF). Therefore, the loop bandwidths are chosen as 120 kHz and 50 MHz for PLL1 and PLL2, respectively. Since the frequencies of two VCOs in these two PLLs have the relationship of integer, the possible oscillator pulling problem, which may exist in [15], is not an issue in our proposed architecture.

C. Fractional- N $\Delta\Sigma$ M-PLL Circuit Design

Fig. 2 shows the schematic of the fractional- N $\Delta\Sigma$ M-PLL, which provides a high-resolution output f_{out1} as the reference of the following SSPLL. It consists of a PFD, a CP, a LPF, an LC VCO, a multimodulus divider (MMD), and a MASH-111 $\Delta\Sigma$ M. The LC cross-coupled VCO operates at around 2.7~2.8 GHz with four overlapping bands. The MMD is composed of four divide-by-2/3 true-single-phase-clock (TSPC) divider cells, and can generate the eight-division modulus from 24 to 31 with low-power consumption. Therefore, through the modulation of the output of MASH-111 $\Delta\Sigma$ M, it can realize a fine fractional division ratio from 27 to 28. This $\Delta\Sigma$ M-PLL is able to work in both fractional- N and integer- N modes.

The CP is modified from [16] in order to reduce the reference spurs and suppress the quantization noise of the $\Delta\Sigma$ M. The voltage-to-current (V2I) converter senses the voltage difference between V_1 and V_2 , and corrects the mismatch between charge and discharge currents. The second-order LPF (R_1 , C_1 , and C_2) is connected to V_2 to form a main pole and a zero. The spur due to the clock operation is suppressed by the big capacitor C_1 . The CP output V_1 can be regarded as

Fig. 3. Schematic of integer- N SSPLL.

Fig. 4. Schematic of 100-GHz buffers, SSPD, and TIA-CP.

V_2 after a unity-gain amplifier. Therefore, the ripple in V_2 caused by the clock operation and $\Delta\Sigma$ M can be filtered by this follower. V_1 is filtered by a first-order LPF (R_3 and C_3) and serves as the VCO control voltage V_{ctrl} to further suppress the ripple. The bandwidth of the V2I converter is set to be much larger than the PLL loop bandwidth but much smaller than the reference clock, so it can perform the filter function while does not interfere with the PLL loop locking process.

D. Integer- N Subsampling PLL Circuit Design

As shown in Fig. 3, the second PLL is a subsampling PLL that comprises a QVCO, four buffers, an SSPD, a pulse generator, a transimpedance amplifier CP (TIA-CP) [5], an automatic frequency control (AFC) circuit, and a second-order LPF. When SSPLL works at very high frequency with large frequency multiplication, some additional considerations should be taken to achieve adequate acquisition range.

Fig. 4 shows the schematic of the 100-GHz buffers, the SSPD, and the TIA-CP. The buffer is a cascode amplifier with an inductor resonating with the input capacitance of SSPD at around 100 GHz. The transmission line used between the common-source stage and the common-gate stage is to accommodate the long distance LO distribution and it also

improves the bandwidth slightly. The SSPD is a pair of nMOS sample-and-hold switch with capacitor loading. At around 100-GHz frequencies, the insertion loss and the feed-through parasitic capacitance of the switches dramatically degrade the conversion gain of SSPD. Larger switches lead to smaller insertion loss, but large parasitic capacitance and thus smaller gain. In addition, the bias voltage $V_{b,pd}$ also plays an important role in the conversion gain of SSPD since it affects the insertion loss and input capacitance of the switch, as well as the input common-mode voltage of the pMOS input pair in the TIA-CP. The optimal value of $V_{b,pd}$, as shown in Fig. 4, is set to 0.2 V according to the postlayout simulation results. The pulse generator is used to control the charge/discharge period in the TIA-CP, and its pulsewidth is tunable. The TIA-CP current is programmable in order to adjust the loop bandwidth. As mentioned previously, f_{out1} is limited by TIA-CP where the reference input is used to periodically turn on the CP in order to control its gain through tuning the pulsewidth. It is also limited by the SSPD because we need to fully turn on and off switches to improve its gain. Therefore, the size of these switches needs to be optimized carefully.

The conventional SSPLL usually needs one auxiliary frequency-locked loop to increase the acquisition range and avoid the false locking. This auxiliary loop is a conventional CPPLL that contains the power and area hungry divider chain. The tuning range of each band in QVCO should be designed as much smaller than the reference input to avoid false locking. We propose the use of capacitor banks and AFC to increase the acquisition range and avoid the SSPLL to lose its locking due to the PVT variations. One example is that the large frequency drift caused by the temperature variation may cause the SSPLL to lose its locking if the locking point is near the boundary. Since the conventional counter-based AFC is unable to work directly at mm-wave frequencies or alternatively needs a divider chain, the mixed-mode AFC is proposed. Triggered by a clock divided from f_{in2} , the AFC detects the control voltage of QVCO, V_{ctrl} , through the two analog comparators, and outputs two digital signals S_H and S_L to indicate whether V_{ctrl} is within the two reference voltages. V_{ref_H} and V_{ref_L} are chosen when tuning curves are in linear region. Once V_{ctrl} crosses the border, AFC will digitally tune the QVCO until V_{ctrl} is inside the border. At first, the frequencies tuning curves of QVCO are one-time characterized. Then the initial QVCO band is assigned near the target band. AFC automatically switches the initial QVCO band to the desired band based on the values of S_H and S_L . The operating process of the proposed AFC is shown in Fig. 5. The proposed AFC makes sure V_{ctrl} is in the linear region of the tuning curve in order to keep the loop bandwidth and phase margin.

III. PROPOSED TIPIC-QVCO

The proposed TIPIC-QVCO is improved from the in-phase injection-coupled (IPIC) QVCO in [16] and [17]. Compared with other kinds of QVCOs such as the conventional parallel-coupled QVCO (P-QVCO) [18], the IPIC-QVCO benefits from low phase noise due to its in-phase coupling. We will show here that by properly using transformer,

Fig. 5. Operating process of the proposed AFC.

Fig. 6. Schematic of the proposed TIPIC-QVCO and buffers.

the phase noise of QVCO can be reduced further. As shown in Fig. 6, the proposed TIPIC-QVCO consists of two identical VCOs and one coupling network. The coupling network is composed of four back-to-back diode-connected transistors, and the current from coupling network is injected into the primary tank through a transformer. The main difference between TIPIC-QVCO and IPIC-QVCO is the use of a pair of transformers. With the presence of transformers, the currents in the proposed TIPIC-QVCO can be guided correctly and finally the true in-phase coupling is achieved as will be analyzed in the following. The following sections will help designers to understand and design a TIPIC-QVCO.

A. Analysis of TIPIC-QVCO

1) *Operation Analysis:* To understand the basic concept of true in-phase coupling in the proposed TIPIC-QVCO, we analyze the operation of the coupling network. For simplicity, let us assume that all parasitic capacitors are ignored and only the fundamental components need to be considered due to the bandpass characteristic of the LC tank. Fig. 7 shows the simplified schematic of a part of the proposed TIPIC-QVCO, and its related phasor diagram. When the QVCO is operating, the phases of voltages V_{I+} , V_{I-} ,

Fig. 7. Operation analysis of the proposed TIPIC-QVCO.

Fig. 8. Transformer model of the proposed TIPIC-QVCO.

V_{Qt+} , and V_{Qt-} are 0° , 0° , 90° , and -90° , respectively. The drain currents of M_{C1} and M_{C2} , I_{C1} and I_{C2} have a phase of 135° and 45° , respectively. The current I_{inj} from the coupling network is equal to $I_{C2} - I_{C1}$, and its phase is 0° . As will be shown later, the induced current $I_{inj,eff}$ is in-phase with the tank current I_{tank} . Applying similar analysis to other oscillation nodes, we demonstrate that the in-phase coupling is realized in the proposed TIPIC-VCO. Because in IPIC-QVCO, the injection current is antiphase with the tank current, so the proposed TIPIC-QVCO is true in-phase.

2) *Oscillation Frequency Analysis*: Fig. 8 shows the model of the transformer. Resistors are added in series with both inductors and capacitors to account for their losses. Compared with the single inductor LC tank, we assume their inductance L and their loss R_L are the same. This assumption is reasonable, because, according to the electromagnetic (EM) simulation, the inductance and the quality factor of a single inductor are close to that of the primary or the secondary inductor of the transformer with the same dimension at around 100 GHz. To simplify the analysis, we assume the capacitance C of the single inductor LC tank is equally distributed into two windings of the transformer. Let us define $\omega_0 = 1/(LC)^{(1/2)}$, $Q_{C0} = 1/(\omega_0 R_C C)$, $Q_{L0} = \omega_0 L/R_L$, $Q_0 = Q_{C0} \parallel Q_{L0} = \omega_0 L/(R_L + R_C)$. The input impedance of this transformer is shown in (1) at the bottom of this page.

In order to estimate its resonant frequencies, we assume all LC components are lossless ($R \rightarrow 0$, $Q \rightarrow \infty$), so Z_{in} can be simplified as

$$Z_{in} = \frac{2Ls \left(\frac{(1-k^2)}{\omega_0^2} s^2 + 2 \right)}{\frac{(1-k^2)}{\omega_0^4} s^4 + \frac{4}{\omega_0^2} s^2 + 4}. \quad (2)$$

Let its denominator equals zero and we can get two resonant frequencies located at

$$\omega_{osc} = \omega_0 \sqrt{\frac{2}{1 \pm k}}. \quad (3)$$

The two solutions are corresponding to two different coupling polarities in transformer, respectively. The first and lower resonant frequencies $\omega_{osc} = \omega_0((2/(1+k))^{(1/2)})$ indicate the in-phase coupling in the transformer, and is chosen in our design due to its high-quality factor. The second resonant frequency does not exist due to its higher frequency (lower transconductance) and much lower effective inductor Q . Note that due to $0 < k < 1$, the desired oscillation frequency of the TIPIC-QVCO is higher than that of the IPIC-QVCO ($\omega_{osc} = \omega_0$) if the inductances and parasitic capacitances are the same. For $k = 0.7$, the oscillation frequency of the TIPIC-QVCO is improved 8.5%, which is also verified in the simulation. Through distributing the capacitance into two winds, the tuning range of the QVCO can be improved.

3) *Effective Quality Factor Analysis*: To calculate the quality factor at the first resonant frequency through (1), we use the definition of quality factor

$$Q_{osc} = \frac{\omega_{osc}}{2} \frac{d}{d\omega} \left(\arctan \left(\frac{\text{Im}(Z_{in})}{\text{Re}(Z_{in})} \right) \right) \Big|_{\omega=\omega_{osc}} \quad (4)$$

$$= \frac{\omega_0 L \sqrt{2(1+k)}}{2R_C + R_L} = \frac{\omega_{osc} L (1+k)}{2R_C + R_L}. \quad (5)$$

Note that here we assume $L \gg C$ and high-order terms are ignored. Q_{osc} in the proposed transformer is close to Q_0 in the single LC tank. For a typical value ($L = 25.3$ pH, $Q_{L0} = 14$, $C = 100$ fF, $Q_{C0} = 8$, $k = 0.7$) at around $\omega_{osc} = 108.5$ GHz, $Q_{osc}(= 1.12Q_0)$ is improved 12%.

Using the superposition method, we can derive the induced current $I_{inj,eff}$ due to the injection current I_{inj} as shown in Fig. 8. Note that the impedance is symmetric looking from both primary and secondary windings. For simplicity, we ignore the loss and loading in the transformer. The current I_{L1} is

$$I_{L1} = \frac{-V_{inj}}{j\omega L} = \frac{-Z_{inj} I_{inj}}{j\omega L}. \quad (6)$$

$$Z_{in} = \frac{2L \left(\frac{s}{Q_{C0}\omega_0} + 1 \right) \left(\frac{(1-k^2)}{\omega_0^2} s^3 + \frac{2}{Q_0\omega_0} s^2 + \left(A \frac{\omega_0}{Q_{L0}} + 2 \right) s + 2 \frac{\omega_0}{Q_{L0}} \right)}{\frac{(1-k^2)}{\omega_0^4} s^4 + \frac{2A}{\omega_0^2} s^3 + \left(A^2 + \frac{4}{\omega_0^2} \right) s^2 + 4As + 4} \quad A = (2R_C + R_L)C \quad (1)$$

Fig. 9. Models of diode-connected transistor, half of cross-coupled regenerative pair, and the effective LC tank.

Therefore, the sensed voltage V_{sens} caused by the induced current is

$$V_{\text{sens}} = j\omega k L \cdot I_{L1} = k Z_{\text{inj}} I_{\text{inj}}. \quad (7)$$

Therefore, the effective injection current in the primary tank is

$$I_{\text{inj,eff}} = \alpha I_{\text{osc}} \approx -k I_{\text{inj}}. \quad (8)$$

The induced current $I_{\text{inj,eff}}$ caused by the injection current I_{inj} has the same phase with I_{osc} . Therefore, the true in-phase injection coupling is realized. Note that when we consider the loss and the loading effect of transformer, $I_{\text{inj,eff}}$ will be smaller than $k I_{\text{inj}}$ which is verified through simulation. To derive the phase noise expression in the next section, we define $I_{\text{inj,eff}} = \alpha I_{\text{osc}}$, where α denotes the coupling factor of the TIPIC-QVCO.

4) *Phase Noise*: We can follow the steps in [19] and [16] to solve Alder's equation, in order to analyze the phase noise of the proposed TIPIC-QVCO. Fig. 9 shows the models of diode-connected transistors, half of cross-coupled regenerative pair, and the effective LC tank. According to Fig. 8, we can simply assume $C' = C/2$, then we have

$$L' = \frac{1}{\omega_{\text{osc}}^2 C'} = L(1+k) \quad (9)$$

$$R'_p = Q_{\text{osc}} \omega_{\text{osc}} L' = \frac{2L(1+k)}{C(2R_C + R_L)}. \quad (10)$$

Therefore, the transformer can be treated as a single LC tank. We assume the drain currents in the coupling network are $I_{C1} = i_C \cos((\theta_1 + \theta_2)/2 + (\pi/2))$ and $I_{C2} = i_C \cos((\theta_1 + \theta_2)/2)$, where $\theta_1 = \omega_{\text{osc}} t$, $\theta_2 = \omega_{\text{osc}} t + \pi/2$. Thus, the effective injection current is

$$I_{\text{inj,eff}} = -k(I_{C1} - I_{C2}) = \sqrt{2} k i_C \cos\left(\frac{\theta_1 + \theta_2}{2} - \frac{\pi}{4}\right). \quad (11)$$

Applying the generalized Alder's equation in this expression leads to the differential equation in tank θ_1 as follows

$$\frac{d\theta_1}{dt} = \omega_{\text{osc}} + \frac{\omega_{\text{osc}}}{2Q_{\text{osc}}} \frac{\sqrt{2} k i_C \sin\left(\frac{\theta_2 - \theta_1}{2} - \frac{\pi}{4}\right)}{\frac{2}{\pi} I_0 + \sqrt{2} k i_C \cos\left(\frac{\theta_2 - \theta_1}{2} - \frac{\pi}{4}\right)}. \quad (12)$$

Similarly, tank θ_2 can be also described through the differential equation as follows:

$$\frac{d\theta_2}{dt} = \omega_{\text{osc}} + \frac{\omega_{\text{osc}}}{2Q_{\text{osc}}} \frac{\sqrt{2} k i_C \sin\left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{4}\right)}{\frac{2}{\pi} I_0 + \sqrt{2} k i_C \cos\left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{4}\right)}. \quad (13)$$

The noise current can be treated as the small injection current into the tank. So that we can obtain the phase noise due to the white noise from tank, cross-couple pair, and coupling network. Phase noise can be analyzed as weak injection by using Alder's equations. We treat white noise from tanks, cross-coupled pairs, and coupling network as individual weak injection currents into these two oscillators. The injection currents directly or indirectly lead to phase noise. We analyze the phase noise of TIPIC-QVCO due to the white noise from the tank first. Suppose $i_{n,\text{tank1}} \cos((\omega_{\text{osc}} + \omega_m)t)$ is the noise current of the tank θ_1 in 1-Hz bandwidth at ω_m offset frequency. The noise current results in the output phases $\theta_i + \tilde{\theta}_i$, where $\tilde{\theta}_i$ ($i = 1, 2$) is the phase fluctuation in each tank due to noise. Thus, (12) and (13) can be rewritten as differential equations shown as follows:

$$\frac{d\tilde{\theta}_1}{dt} = \frac{\omega_{\text{osc}}}{2Q_{\text{osc}}} \frac{\sqrt{2} k i_C \sin\left(\frac{\tilde{\theta}_2 - \tilde{\theta}_1}{2}\right) + i_{n,\text{tank1}} \sin(\omega_m t)}{\frac{2}{\pi} I_0 + \sqrt{2} k i_C \cos\left(\frac{\tilde{\theta}_2 - \tilde{\theta}_1}{2}\right) + i_{n,\text{tank1}} \cos(\omega_m t)} \quad (14)$$

$$\frac{d\tilde{\theta}_2}{dt} = \frac{\omega_{\text{osc}}}{2Q_{\text{osc}}} \frac{\sqrt{2} k i_C \sin\left(\frac{\tilde{\theta}_1 - \tilde{\theta}_2}{2}\right)}{\frac{2}{\pi} I_0 + \sqrt{2} k i_C \cos\left(\frac{\tilde{\theta}_1 - \tilde{\theta}_2}{2}\right)}. \quad (15)$$

Solving these equations, we can find out that the phase fluctuation $\tilde{\theta}_i$ due to the noise current in tank θ_1 are the same

$$\tilde{\theta}_1 \approx \tilde{\theta}_2 \approx \frac{\omega_{\text{osc}}}{4Q_{\text{osc}} \omega_m} \frac{i_{n,\text{tank1}}}{I_{\text{osc}}(1+\alpha)} \cos(\omega_m t). \quad (16)$$

Therefore, the close-in phase noise spectral density defined by IEEE due to the white noise from two tanks is

$$\mathcal{L}_{\text{tank}}(\omega_m) \approx \frac{kT \omega_{\text{osc}}}{2Q_{\text{osc}} C' V_0^2 (1+\alpha)^2 \omega_m^2}. \quad (17)$$

Similarly, considering the phase noise contributed by white noise in cross-coupled pair and the coupling network, we can have the overall phase noise due to the white noise

$$\mathcal{L}(\omega_m) \approx \frac{kT \omega_{\text{osc}} (1 + \gamma(1+\alpha))}{2Q_{\text{osc}} C' V_0^2 (1+\alpha)^2 \omega_m^2} \quad (18)$$

where γ is the MOS channel noise factor. As we can see from (18), in contrast to that in IPIC-QVCO [16], there is no tradeoff between the coupling factor and phase noise in TIPIC-QVCO, and on the contrary, the larger α leads to better phase noise. Moreover, since Q and V_0 are both improved, the phase noise of TIPIC-QVCO is much better than that of IPIC-QVCO, which is also verified through simulation as shown in Fig. 10. The calculated phase noise contributed from thermal noise is close to the simulated phase noise at high offset frequencies. The flicker noise is not included in (18) because its upconversion mechanism is through nonlinear varactor and parasitic capacitance which cannot be modeled exactly in our model.

Fig. 10. Simulated phase noise of differential VCO (green). Calculated (dashed line) and simulated (solid line) phase noise of P-QVCO (black), SHC-QVCO (magenta), MC-QVCO (cyan), IPIC-QVCO (blue), and TIPIC-QVCO (red).

5) *Phase Error*: Due to the PVT variations, the mismatches will induce the phase error of quadrature outputs. Assume the mismatches exist in the LC tank resonant frequency and tail current, and all the mismatches are in the second oscillator: oscillation frequency $\omega_{osc2} = \omega_{osc} + \Delta\omega_{osc}$, and tail current $I_{02} = I_0 + \Delta I_0$, which results in the phase error represented by $\Delta\varphi$ in the second oscillator $\theta_2 = \theta_1 + \pi/2 + \Delta\varphi$. Substituting all these expressions into (12) and (13) and simplifying the results, we obtain the phase error express

$$\Delta\varphi = 2Q(1 - \alpha) \frac{\Delta\omega_{osc}}{\omega_{osc}}. \quad (19)$$

When the coupling factor α ($0 < \alpha < 1$) increases, the phase error decreases which is the same with other kinds of QVCOs. As shown in Fig. 11, the simulated results match the calculated curve based on (19) well.

Interestingly, the tail current mismatch between two oscillators does not introduce phase error theoretically. It means that the phase error is not sensitive to the tail current mismatch in the proposed TIPIC-QVCO thanks to the in-phase injection coupling. In the simulation, a 5% tail current mismatch will lead to about 1° phase error.

B. 100-GHz TIPIC-QVCO Circuit Design and Comparisons With Other VCO and QVCOs

A 100-GHz TIPIC-QVCO is employed in the SSPLL to generate 100-GHz quadrature LO signals. As shown in Fig. 6, a 6-bit binary-weighted switched-capacitor bank is used for discrete tuning in order to reduce the VCO's sensitivity and avoid false locking in the SSPLL. The switched-capacitor bank consists of six pairs of MOM capacitors placed under the inductor. The resistor-biased switches in the varactor and capacitor banks contribute less noise than other conventional switches. To avoid the flicker noise from tail current, a digitally controlled resistor R_{tail} is adopted here. Cascode amplifiers are used as the buffers for both output testing and internal feedback which is described in Section II-D.

The full EM simulation of the transformer and interconnects was performed since the parasitics affect the performance much at this frequency. Two top metals with a thickness of 3.3 and $1.325 \mu\text{m}$ are stacked for the primary and secondary windings, respectively, to obtain similar inductances, a high coupling factor, and high-quality factors. A floating isolation

Fig. 11. Simulated (symbol) and calculated (solid line) phase error of TIPIC-QVCO due to ω_{osc} mismatch.

layer formed by the high impedance N-well is inserted under the transformers to reduce the loss from substrate. According to ANSYS HFSS EM simulator, the simulated inductances and quality coefficients of the primary and the secondary inductors are about 23 and 30 pH, and 14.0 and 13.4, respectively, and the transformer coupling factor is about 0.72.

Fig. 10 shows the simulated phase noises of QVCOs and the differential VCO. All QVCOs are under the same conditions at 100 GHz: $W_1/L_1 = W_{C1}/L_{C1} = 24/0.06 \mu\text{m}$, $L = 30 \text{ pH}$, $k = 0.7$, $V_{DD} = 1.2 \text{ V}$, $I_0 = 5 \text{ mA}$, 0.1% tank mismatch. The simulation results show that the coupling network contributes negligible noise at large offset frequencies in TIPIC-QVCO because its phase noise is improved by 3 dB at 1-MHz offset frequency compared with the differential VCO. Its phase noise becomes worse at lower offset frequencies due to the flicker noise in the coupling network which can be suppressed in PLL.

The proposed TIPIC-QVCO is compared with other QVCOs such as P-QVCO [18], IPIC-QVCO, superharmonic-coupled QVCO (SHC-QVCO) [20], and magnetically coupled QVCO (MC-QVCO) [21]. Both IPIC-QVCO and TIPIC-QVCO have better phase noises compared with P-QVCO, SHC-QVCO, and MC-QVCO. For example, thanks to the in-phase coupling, the phase noise of TIPIC-QVCO at 1-MHz offset frequency is reduced by 12 dB compared with the conventional P-QVCO. What is more, SHC-QVCO suffers from large phase error due to its weak coupling strength, and the tuning range of the MC-QVCO is limited by its delicate LC shifter.

Compared with IPIC-QVCO, the proposed TIPIC-QVCO provides additional but significant benefits: First, as shown in (3), the oscillation frequency of the TIPIC-QVCO increases since the total capacitance is intentionally designed to be almost equally distributed among primary and secondary tanks. Second, by proper design, the coupling inductor currents of the transformer are in phase, thus the effective tank Q_{osc} is improved as depicted in (5). Third, compared with the IPIC-QVCO, the TIPIC-QVCO has the merits of low phase noise and low power, thanks to the larger tank current thus amplitude. In the IPIC-QVCO, there is a tradeoff between the effective tank Q_{eff} and the coupling strength of QVCO, since the tank current I_{tank} is equal to $I_{osc} - I_{inj}$, where I_{osc} and I_{inj} are the oscillating current and the injection current, respectively. Fortunately, in the TIPIC-QVCO, the coupling is truly in phase, and Q_{osc} and I_{tank} are increased, so both

Fig. 12. Die micrograph and test setup of the cascaded PLL.

Fig. 13. DC power consumption of the cascaded PLL and the $\Delta\Sigma$ M-PLL.

good phase noise and low power are achieved simultaneously. As shown in Fig. 10, the simulated phase noise of the TIPIC-QVCO is improved by at least 2 dB at both low and high offset frequencies, compared to the IPIC-QVCO. Postlayout simulation with EM models shows that the phase error of TIPIC-QVCO is within 0.8° .

IV. MEASUREMENT RESULTS

The cascaded PLL was implemented in GLOBAL-FOUNDRIES 65-nm LP CMOS technology. Fig. 12 shows the die micrograph of the PLL, which occupies $1.03 \times 0.85 \text{ mm}^2$. The cascaded PLL consumes 57 mW from a 1.5-V supply, of which, 7.5 and 49.5 mW are consumed by the $\Delta\Sigma$ M-PLL and the SSPLL, respectively. The proposed QVCO draws about 20-mA current, and can be tested individually. Fig. 13 shows the dc power consumption pie charts of the cascaded PLL and the $\Delta\Sigma$ M-PLL.

Fig. 12 also shows the test setup for the proposed TIPIC-QVCO and cascaded PLL. An R&S FSUP50 signal source analyzer with a W-band subharmonic mixer is employed to test the 100-GHz output of QVCO and PLL. As depicted in Fig. 14, the 64 bands of the QVCO cover a frequency range of 93.24–105.02 GHz, i.e., 11.9% around the center frequency. Each band can cover about 800-MHz frequency range with around 200 MHz spacing between adjacent bands. As shown in Fig. 15, the measured QVCO phase noise for the lowest band 63 (93.24 GHz), the middle band 31 (98.53 GHz), and the highest band 0 (105.02 GHz) are -94.38 , -92.82 , and -90.43 dBc/Hz at 1-MHz offset frequency, and -114.92 , -113.26 , and -111.29 dBc/Hz at 10-MHz offset frequency, respectively. The FOM of the QVCO is -178.0 and -178.4 dBc/Hz, and FOM_T -179.5 and -180.0 dBc/Hz, both at 1- and 10-MHz

Fig. 14. Measured tuning range of the TIPIC-QVCO.

Fig. 15. Measured phase noise of the TIPIC-QVCO.

Fig. 16. Measured phase noise and integrated jitter (from 10 kHz to 300 MHz) of (a) TIPIC-QVCO and (b) cascaded PLL over the operation range.

offset frequencies, respectively. Due to the lack of equipment, the measured phase error is not available. The measured phase noise of TIPIC-QVCO over the operation range is shown in Fig. 16(a).

TABLE II
MEASURED 100-GHz QVCO PERFORMANCE SUMMARIES AND COMPARISONS WITH CMOS STATE-OF-THE-ART WORKS

Ref.	Tech.	Operating Range (GHz)	P.N.@1MHz /10MHz (dBc/Hz)	FOM ^(a) @1MHz /10MHz (dBc/Hz)	FOM _T ^(b) @1MHz /10MHz (dBc/Hz)	Output Phase	Power (mW)
[22]	32 nm CMOS	100.07~104.28 (4.1%)	-75 ^(c) /-100.88	-166.55 /-172.45	-158.8 /-164.75	Differential	7.59
[23]	65 nm CMOS	100~110 (9.5%)	-92.83 /-100 ^(c)	-175.9 /-163.1	-175.5 /-162.7	Quadrature	54
[24]	65 nm CMOS	95.37~106.68 (11.2%)	-77.62 /-104.50	-168.6 /-175.5	-169.6 /-176.5	Differential	3.52~11.9
[25]	65 nm CMOS	98~103.3 (5.3%)	-75 ^(c) /-112.1	-164.49 /-181.59	-158.81 /-175.91	Differential	12~21
		91.7~95.5 (4.1%)	-80 ^(c) /-118.8	-162.79 /-181.59	-155.04 /-173.84	Eight Phases	48~85
This work	65 nm CMOS	93.24~105.02 (11.9%)	-92.82 /-113.26	-178.0 /-178.4	-179.5 /-180.0	Quadrature	30

^(a) $FOM = L\{\Delta f\} + 20 \log(\Delta f/f_0) + 10 \log(\text{Power}/1\text{mW})$.

^(b) $FOM_T = L\{\Delta f\} + 20 \log(\Delta f/f_0) (FTR/10) + 10 \log(\text{Power}/1\text{mW})$.

^(c) Estimated from figure.

TABLE III
MEASURED 100-GHz PLL PERFORMANCE SUMMARIES AND COMPARISONS WITH CMOS STATE-OF-THE-ART WORKS

Ref.	Tech.	f_{REF} (MHz)	Operating Range (GHz)	P.N. (FOM _T) @1MHz /10MHz (dBc/Hz)	Reference Spur (dBc)	Resolution (MHz)	Output Phase	Architecture	Area (mm ²)	Power (mW)
[1]	130 nm CMOS	44.8~49.3	91.8~101 (9.5%)	-66(-148.6) ^(a) /-93(-155.6)	-40~-27	f_{REF}	Single-ended	Integer- N + Push-Push	0.87	46
[2]	65 nm CMOS	371.5~377.0	95.1~96.5 (1.5%)	-76(-142.7) /-93(-139.7) ^(a)	-51.8	f_{REF}	Diff.	Integer- N	0.7	43.7
[3]	65 nm CMOS	185.7~211.9	96.8~108.5 (11.5%)	-88(-177.9) /-105(-174.9) ^(a)	-40	f_{REF}	Diff.	Integer- N + Push-Push	0.39 ^(d)	14.1
[4]	65 nm CMOS	402.6~408.5	103.058~104.58 (1.5%)	-80.41(-146.3) /-101.08(-146.9)	-63.8	f_{REF}	Diff.	Integer- N	0.84	63
[26]	65 nm CMOS	125	82.0~107.6 (27%)	-84.2~-87.1 ^(c) (-196.2~-198.1) /-106~-110 (-178~-181)	-34~-52	1.5 kHz	Single-ended	ADPLL	0.36 ^(d)	35.5
[14]	65 nm CMOS	230	26.2~32.4 (21.2%)	-116.2(-197.8) /-112.6(-194.2) ^(b)	-63.16	0.015 f_{MIXER} (ext. clock)	Quad.	Frac- N + Sub-sampling	0.28 ^(d)	26.9
This work	65 nm CMOS	100	93.4~104.8 (11.5%)	-85.75(-169.4) /-106.63(-170.3) /-85.53(-169.2) ^(b) /-105.55(-169.2)	-43.83	0.000036 f_{REF} (<3.6 kHz)	Quad.	Frac- N + Sub-sampling	0.8755	57

^(a) Estimated from figure.

^(b) PLL is in fractional- N mode.

^(c) Close-in phase noise at 0.1 MHz.

^(d) Not including pads.

A signal generator SMF100A is used as the reference input. The measured operation range of the cascaded PLL is from 93.4 to 104.8 GHz. To ensure all the frequency bands are sufficiently overlapped, a 1.5-V supply is used, and about 600-MHz operation range is achieved in every band of the SSPLL. Through using AFC, there is no acquisition limitation in the measurement. The phase noise of the cascaded PLL in integer- N mode ($N_1 = 28$, $N_2 = 36$, and reference input is about 99.206 MHz), shown in Fig. 17, is -85.75 and -106.63 dBc/Hz at 1- and 10-MHz offset frequencies, respectively, when the carrier frequency is 100 GHz. When the cascaded PLL is locked at the same frequency in fractional- N mode ($N_1 \approx 27.778$, $N_2 = 36$, and reference input is 100 MHz), the phase noise at a

1-MHz offset frequency is almost the same (-85.53 dBc/Hz), and the phase noise at 10-MHz offset frequency increases to -105.54 dBc/Hz, which should be due to the quantization noise of the $\Delta\Sigma$ M. Fig. 16(b) shows the measured phase noise of the cascaded PLL over the operation range. We also measured the phase noise of $\Delta\Sigma$ M-PLL and SSPLL individually. When the input reference is from external signal generator, the phase noise of the 100-GHz SSPLL is -99.55 and -112.22 dBc/Hz at 1- and 10-MHz offset frequencies, respectively. Its in-band phase noise is better than -95 dBc/Hz. As shown in Fig. 17, the phase noise of the proposed cascaded PLL is dominated by $\Delta\Sigma$ M-PLL due to its poor phase noise. According to the simulated phase noise contribution of blocks, the remedy is to reduce the phase

Fig. 17. Measured and simulated phase noise of the proposed PLLs.

Fig. 18. Measured output spectrum of (a) $\Delta\Sigma$ M-PLL and (b) cascaded PLL.

noise of the VCO in the $\Delta\Sigma$ M-PLL. As shown in Fig. 16(b), the measured output integrated jitters (both from 10 kHz to 300 MHz) of PLL1 over the tuning range is 208.4~235.3 and 224.1~250.8 fs in the integer- N and fractional- N modes, respectively. The measured output integrated jitters of the cascaded PLL over the tuning range are 607.3~689.5 and 612.2~697.1 fs in the integer- N and fractional- N modes, respectively. Fig. 18 shows the spectrum of the $\Delta\Sigma$ M-PLL and 100-GHz cascaded PLL output. The measured 100-MHz reference spurious level of the $\Delta\Sigma$ M-PLL is -51.54 dBc. The measured 100-MHz reference spurious level of the cascaded PLL is -43.83 dBc, the fractional spurious level is 34.23 dBc, and the 2.78-GHz spurious level is -46.25 dBc.

The measured QVCO and PLL performances are summarized and compared with the state-of-the-art works given in Tables II and III, respectively. The proposed QVCO achieves the best FOM_T value, whereas the cascaded PLL

achieves the best performance among all similar CMOS state-of-the-art works.

V. CONCLUSION

In conclusion, a 93.4–104.8-GHz fractional- N PLL is proposed. Both the high-frequency resolution and wide operation range are achieved simultaneously in the proposed cascaded PLL architecture. The proposed TIPIC-QVCO enables low phase noise and low-power consumption. Measurement results show that the proposed cascaded PLL exhibits low phase noise with high-frequency resolution less than 3.6 kHz.

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