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A 65nm CMOS Carrier-Aggregation Transceiver for IEEE 802.11 WLAN Applications

Xiang Yi¹, Kaituo Yang¹, Zhipeng Liang¹, Bei Liu¹, Khanna Devrishi¹, Chirn Chye Boon¹,
Chenyang Li¹, Guangyin Feng¹, Dror Regev², Shimi Shilo², Fanyi Meng¹, Hang Liu¹, Junyi Sun¹,
Gengen Hu³, Yannan Miao³

¹ VIRTUS, Nanyang Technological University, Singapore

² Huawei, Israel

³ Huawei, China

yixiang@ntu.edu.sg

Abstract—This work presents a parallel direct-conversion and double-conversion transceiver to solve the problems of crosstalk and LO pulling in the carrier aggregation scenario. An EVM of -34.9 dB is obtained when the output power of the PA driver is 0.4 dBm. Three aggregated carriers with 80 MHz 256-QAM modulation are demonstrated. To the authors' best knowledge, this work is the first CMOS integrated transceiver for IEEE 802.11 WLAN carrier aggregation application.

Index Terms—RF CMOS, WiFi, WLAN, transceiver, receiver (RX), transmitter (TX), carrier aggregation (CA), direct-conversion, double-conversion.

I. INTRODUCTION

Increasing demand on the broadband wireless local area network (WLAN) has been driving the development of new IEEE 802.11 standards in recent years. As the successor to IEEE 802.11ac, IEEE 802.11ax will increase the efficiency of WLAN networks, especially in high-data-rate, dense, and outdoors scenarios. Its new features, including the carrier aggregation (CA), longer FFT size, multi-user MIMO-OFDMA, and interference coordination, bring new challenges to the transceiver design. CA, which stems from LTE-Advanced standard, brings challenge for transceiver design since more carrier signals will be processed simultaneously, which causes the problems of nonlinearity, crosstalk, and local oscillator (LO) pulling.

Current receivers (RXs) [1-2] for CA are mainly for LTE-Advanced applications, and their architectures are not suitable for 802.11ax standard, whose channels are crowded and wideband. A parallel direct-conversion and low-IF architecture is adopted in [1], but the crosstalk decreases the signal-to-noise ratio (SNR) in intra-band aggregation, and the LO pulling may occur when carriers are close. A complex intermediate frequency (IF) mixer used in the double-conversion RX is proposed in [2], but it cannot be used for CA involving two or more wideband carriers with large frequency spacing.

This work presents a parallel direct-conversion and double-conversion transceiver to solve the problems of

Fig. 1. Block diagram of the proposed transceiver.

crosstalk and LO pulling for CA applications. In Section II, the transceiver architecture, including a RX, a transmitter (TX), and a LO generator, is presented. The measurement results are shown in Section III. Finally, the conclusion is drawn.

II. TRANSCEIVER ARCHITECTURE

The block diagram of the proposed transceiver is shown in Fig. 1. Both RX and TX have a similar parallel direct-conversion and double-conversion architecture, and share one LO generator. There are three paths, and up to three carriers with arbitrary aggregation method can be processed at the same time. Five LOs are employed to feed the mixers of RX and TX. As will be discussed below, our proposed architecture alleviates the crosstalk and LO pulling problems even in the scenario of crowded and wideband CA.

Conventional parallel direct-conversion RXs encounter serious crosstalk problem when the frequencies of carriers and LOs are close. In such architecture, the channel selection or filtering is not applicable, so the LO leakages from other paths down-convert the unwanted signals to direct-current (DC), which degrades the SNR of desired

Fig. 2. Analysis of parallel direct-conversion and double-conversion.

signal. In our proposed structure, the crosstalk is reduced significantly. As shown in Fig. 2, there are one direct-conversion path and one double-conversion path in parallel. Let us consider the LO leakage from Path 1 first. No matter the LO leakage appears in which mixer of Path 2, the resulting interference is far away from the DC and can be readily filtered out. Secondly, let us analyse the LO leakages from Path 2 to Path 1. When the two leakages appear at the input of mixer of Path 1, they will mix with the unwanted signal to DC only through the second nonlinearity coefficient of the mixer. Therefore, the unwanted signal at the output will be negligible since the second nonlinearity coefficient of the mixer is quite small. Similarly, when analysing Path 2 in parallel with Path 3, we can get the similar results. Moreover, the same analysis is also valid in the proposed TX. In other words, our proposed parallel direct-conversion and double-conversion is essentially immune to the crosstalk.

The schematic of the RX radio frequency (RF) front-end is shown in Fig. 3. A differential inductive source-degenerated low noise amplifier (LNA) with post-distortion linearity technique is adopted for better linearity performance [6]. The IIP3 increases dramatically after adding a diode-connected NMOS between common-source and common-gate stages in the cascode LNA. For three CAs implementation, three identical transconductance amplifiers (Gm cells) are connected to the LNA output in parallel. These amplifiers convert the same RF voltage signal to current in each path while providing substantial isolation between each other. The amplifiers are class-AB CMOS inverters, whose IIP2 and IIP3 can be improved substantially by setting the transconductance of its PMOS and NMOS devices to be equal. The transconductance amplifier in each path is followed by direct-conversion or double-conversion passive mixers. The passive mixers are driven by quadrature 25%-duty-cycle LOs. The transimpedance amplifier (TIA), which converts input current to output voltage, is in common-gate configuration with reconfigurable gain and bandwidth settings.

Fig. 3. Schematic of receiver.

Fig. 4. Schematic of transmitter.

As shown in Fig. 4, the proposed TX mixer comprises of three double-balanced active mixers sharing one common inductor load to save area. Similar to the RX, one of the three mixers is configured as direct-conversion mode while the other two are in double-conversion configuration. The double-conversion configuration is implemented by stacking two mixers together. This kind of configuration has merits of simplicity, small area and low power consumption. The mixer is followed by a two-stage power amplifier (PA) driver. The first stage with a cascode structure provides voltage gain, while the second stage is a common-source power stage to drive the external PA, to achieve good linearity performance. The transistors of the first stage are biased at class-A to guarantee the linearity and the transistors of second stage are biases at deep class-AB to optimize the efficiency and linearity. The variable gain amplifiers (VGAs) used in the front of TX mixer can compensate the gain error between each path.

In the proposed transceiver, five LOs are needed for both direct-conversion and double-conversion mixers as shown in Fig 1. Among them, LO2b and LO3b are fixed, so they can be generated from one integer- N PLL. On the other hand, LO1, LO2, and LO3 are variable, and they are generated by three fractional- N PLLs. Therefore, a cascaded PLL structure is proposed. A single integer- N PLL can be used to provide clean output for LO2b and

Fig. 5. LO frequency planning.

Fig. 6. Die micrograph of transceiver.

LO3b, as well as the following PLLs. This integer- N PLL is not implemented in this work, and an external 4 GHz signal generator is used in the measurement. The fractional- N PLL employs a high frequency reference, so the noise contribution from the quantization noise of delta-sigma modulator is small. The large loop bandwidth and small division ratio result in a small loop capacitor, fast settling time, and more suppression of phase noise from charge pump and voltage-controlled oscillator (VCO).

Frequency planning is very important in CA transceiver to avoid crosstalk and LO pulling problems. Fig. 5 illustrates the LO frequency planning. Firstly, keep all VCOs' frequencies and their harmonics outside the 5.17-to-5.835 GHz RF band, thus the crosstalk problem from VCOs is avoided. Secondly, make sure all LOs and their harmonics are not close to other VCOs' frequencies, so that LO pulling can be suppressed as much as possible. In our work, LO2b and LO3b are chosen as 1 and 2 GHz, respectively, to meet the above requirements. The duty cycle of quadrature LO signals is set to 25% in order to improve the conversion gain and reduce the noise figure, while relieving the LO crosstalk as well.

To further reduce the crosstalk and LO pulling effects, some methods are taken: (1) Eight-shape inductors are used in VCOs to avoid the coupling from each other and PA; (2) Isolation layers are placed in the empty area between each path and each LO; (3) High impedance shields are inserted under the inductors to improve their quality factors and prevent the substrate coupling; (4) Triple-well devices are employed in both aggressive and susceptible circuits; (5) Differential signal, instead of single-ended signal, is chosen for all building blocks; (6) Supplies and grounds of the RX, the TX, and three LOs are separated, respectively.

III. MEASUREMENT RESULTS

The proposed transceiver is implemented in 65 nm LP CMOS technology. Fig. 6 shows the die micrograph of the transceiver, and the circuit occupies about 3.5 mm². When

Fig. 7. Measured phase noise of LO2.

Fig. 8. Measured SSB rejection ratio.

three paths are on, the total transceiver consumes 264 mW in RX mode, and 325 mW in TX mode. The three PLLs, RX frond-end, TX mixer and PA driver consume 66.3, 52, 15 and 40 mW, respectively. Other power is dissipated by the power-hungry LO distribution for RX and TX mixers and output buffers for testing.

Fig. 7 shows the measured phase noise for a 4.25 GHz carrier. The in-band phase noises are -116.47 and -119.52 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. The out-of-band phase noise at 10 MHz offset frequency is -136.17 dBc/Hz. Since the LO is used in the wideband system, the phase noise is optimized for wide offset frequency. The integrated phase noise from 10 kHz to 100 MHz is -52.1 dBc (132.1 fs), and the PLL FOM is -244.4 dB, which is the best record among the similar works. The PLL spectrum and phase noise are totally not affected by other PLLs, which means LO pulling problem is solved.

The IQ mismatch calibration is done by fine tuning the IQ phases of the divider outputs. As shown in Fig. 8, the SSB rejection ratio of the TX output is 42.6 dB. The measured LO leakage is -56.63 dBm. An average of 0.1 degree IQ mismatch of the baseband output can be achieved in the receiver. Isolation between three TX paths are measured by injecting single tone signal in one path and testing its power in the other two paths. The isolations between each two paths are higher than 56 dB. The measured RX noise figure is 5.0 dB, and in-band IIP3 is -7.5 dBm at maximum gain of 55 dB.

Fig. 9. Measured EVM of a single carrier with 802.11ac 80 MHz 256 QAM modulation.

Fig. 10. Output spectrum of three aggregated carriers with 802.11ac 80 MHz 256-QAM modulation.

The EVM is tested based on an 802.11ac standard signal with EVM floor of -38 dB. Fig. 9 shows the constellation of a carrier with 80 MHz 256-QAM modulation. An average EVM of -34.9 dB is obtained when the output power of the PA driver is 0.4 dBm after calibration. The isolations between each path are larger than 56 dB. Three 80 MHz aggregated carriers are measured, and the output spectrum is shown in Fig. 10. The average EVMs of three aggregated-carriers are about 0.6 dB worse than that of a single carrier, as shown in Fig. 11, illustrating the crosstalk robustness of our transceiver architecture. The measured performance is summarized and compared with state-of-the-art works in Table I.

IV. CONCLUSION

A CMOS transceiver for IEEE 802.11 WLAN applications in 65 nm CMOS is presented. The parallel direct-conversion and double-conversion transceiver architecture is adopted to solve the problems of crosstalk

Fig. 11. Average EVM of three aggregated carriers with 802.11ac 80 MHz 256-QAM modulation.

and LO pulling in the scenario of crowded and wideband CA. Up to three carriers can be aggregated with total bandwidth of 3×80 MHz.

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REFERENCES

- [1] M. Mikhemar, et al., "A Rel-12 2G/3G/LTE-Advanced 3CC receiver," in *IEEE RFIC Symp.*, pp. 143–146, May 2015.
- [2] L. Sundström, et al., "A receiver for LTE Rel-11 and beyond supporting non-contiguous carrier aggregation," *ISSCC Dig. Tech. Papers*, pp. 336–337, Feb. 2013.
- [3] H. Zhang, et al., "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.
- [4] T.-M. Chen, et al., "A 2x2 MIMO 802.11 abgn/ac WLAN SoC with integrated T/R switch and on-chip PA delivering VHT80 256QAM 17.5dBm in 55nm CMOS," in *IEEE RFIC Symp.*, pp. 225–228, Jun. 2014.
- [5] M. He, et al., "A 40nm dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s over-the-air throughput," *ISSCC Dig. Tech. Papers*, pp. 350–351, Feb. 2014.
- [6] H. Zhang, et al., "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.

TABLE I

MEASURED PERFORMANCE SUMMARIES AND COMPARISONS WITH CMOS STATE-OF-THE-ART WORKS.

Ref.	Tech. (nm)	Application	PLL Ref. (MHz)	Integrated Phase Noise	PLL FOM*	RX NF (dB)	EVM (dB)	Area (mm ²)	Power (mW)
[4]	55 CMOS	2x2 11abgn/ac	40/20	-45dBc @4.9GHz (10kHz~10MHz)	N/A	4	-37.5**	7.7	RX: 317mW TX: 1722mW
[5]	40 CMOS	4x4 11ac/abgn	40	-43.8dBc @5.825GHz (10kHz~10MHz)	-244dB (10kHz~10MHz)	4.3	-37	21.5	RX: 2080mW TX: 1520mW
This work	65 CMOS	3 CAs 11ac	4000	-52.1dBc @4.25GHz (10kHz~100MHz)	-244.4dB (10kHz~100MHz)	5.0	-34.9	3.5***	RX: 264mW TX: 325mW

* FOM = $20\log(\sigma_r/1s) + 10\log(P_{dc}/1mW)$. ** Estimated from figure. *** Excluding pads.