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Small-Signal Model Considering Hot-Carrier Effect for Millimeter-Wave Frequencies

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Abstract The hot-carrier effect, which is caused by the generation of interface states, is the main degradation mechanism for MOSFETs. Predicting the degradation of circuit performance due to the hot-carrier effect is important for practical circuit design. In this paper, we propose a small-signal model considering the hot-carrier effect by establishing time-dependent model parameters, which is verified by small-signal simulation for 40-nm-process MOSFETs at millimeter-wave (mmW) frequencies. In the proposed small-signal model, the shift of relaxation time of the non-quasi-static (NQS) effect is investigated and verified for mmW frequencies for the first time. By comparing simulation and measurement results, it is shown that the shift of relaxation time of the NQS effect should be considered for the prediction of radio frequency (RF) performance degradation..

Keywords Hot-carrier degradation · millimeter wave · NMOSFETs · non-quasi-static (NQS) effect · power amplifier.

1 Introduction

With the development of CMOS technology, the power-supply voltage is reduced. However, it has not been scaled downward in proportion to the device dimensions. As a result, the electric field within a MOSFET has increased with technology scaling, increasing the significance of the hot-carrier effect. As it comes to the 65 nm node, hot-carrier effects still exist with bias voltages as

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Fig. 1 Comparison between results for model without consideration of NQS shift and measurement results.

low as 1 V, since it is demonstrated that when the energy is lowered, high-energy electrons generated by electron-electron scattering (EES) become the dominant contribution to the degradation and the electron energy distribution function is strongly "thermalized" by EES effects [1, 2].

Hot-carrier effect occurs when charge carriers are accelerated near the drain region of a MOSFET by a high lateral electric field in the channel if the device is biased in the saturation region. Owing to the vertical electric field generated by the gate voltage, the accelerated carriers are injected into the gate oxide layer and damage the oxide and the $Si-SiO_2$ interface, leading to a gradual change in important MOSFET characteristics such as the threshold voltage (V_{th}), transconductance (g_m), drain current (I_d) and so forth [3–9].

To improve the reliability of MOSFETs, their performance is usually compromised to some extent. When designing a practical circuit, it is necessary to optimize the trade-off between performance and reliability. However, with technology scaling, there are no longer large reliability margins owing to the increase in the electric field. Thus, more accurate modeling is required to ensure that the circuit achieves the required reliability under normal working conditions while maximizing the circuit performance. A small-signal model,

which consists of equivalent lumped components, is usually used to predict the small-signal performance of MOSFETs at millimeter-wave (mmW) frequencies. However, such a model does not usually consider the hot-carrier degradation effect of MOSFETs. This makes it impossible to predict the hot-carrier effect in the circuit design step, and the circuit degradation can only be measured after tape-out, which takes a long time and is inefficient. Thus, it is essential to clarify the relationship between small-signal performance degradation of circuits and the degradation of MOSFET devices.

At very high frequency, quasi-static approximation, which neglects carrier transit delay, usually shows an unreasonable current step at the input discontinuities. In comparison, the non-quasi-static (NQS) results verify that the carrier in the channel takes time to build up [6]. Thus, the NQS effect, which affects the carrier response delay, is critical for performance prediction at mmW frequencies. However, the shift of relaxation time of the NQS effect due to hot-carrier injection has not been analyzed in previously reported small signal models. In [10], small-signal equivalent-circuit degradation under hot-carrier stress was investigated. The relationship between the degradation of the RF and DC performances was addressed. The RF parameter degradation due to the RF hot-carrier stress effect was predicted by an aging model, which was implemented in the compact model in [11]. By carrying out equivalent-circuit modeling, a good description of RF performance degradations was achieved using physical parameters in [12]. However, the shift of the NQS effect was not considered in these studies, resulting in poor accuracy of RF performance degradation prediction at mmW frequencies as shown in Figure 1. The MOSFET was simulated and measured in the frequency range of 45 – 110 GHz at gate and drain voltages of 1.1 V.

In this study, the shift of the NQS effect due to hot-carrier injection is investigated for the first time. It is shown that the shift of the NQS effect should be considered to predict the RF performance degradation at mmW frequencies. A small-signal model considering NQS effect shift is proposed for the convenience of circuit performance degradation simulation. It is shown that good agreement between simulation and measurement results is achieved. The setup for the reliability measurement of NMOSFETs under DC stress is discussed in Section 2. Then in Section 3, small-signal models of NMOSFETs at different stress times are given. The stress-time-dependent model parameters are obtained and the experimental relationships between the model parameters and time are given. The physical background to NQS effect shift is also discussed briefly. Finally, a summary of the small-signal model with consideration of the hot-carrier effect is given in Section 4.

2 Experiment

The devices used for reliability measurement in this study were NMOSFETs with a 40 nm gate length and a total width of 120 μm . Each MOSFET is composed of two 60-finger structures with a finger width 1 μm . The gate oxide

Fig. 2 V_{th} degradation versus stress time.

thickness T_{ox} was 2.47 nm. The fresh threshold voltage V_{th} of the MOSFETs was about 0.62 V. The drain and gate terminals were connected to pads with ground-signal-ground (GSG) structure. The source and back gate of the MOSFETs were connected together and connected to ground.

Each device was measured using a Cascade probe station. The DC performance of each MOSFET was measured using a semiconductor parameter analyzer (Agilent 4156B). The RF performances of the devices were measured using a vector network analyzer (Anritsu 37397D). GSG probes were used to supply DC stress voltages as well as for S-parameter and DC measurements.

According to a previous study [13], when the gate and drain voltages are equal, the hot-carrier effect is largest. For the reliability measurement of a MOSFET, an acceleration test is always used. This has the benefit that the change in model parameters is mainly caused by the hot-carrier effect, reducing the influence of measurement errors. However, when we carried out an acceleration test using gate and drain voltages of 1.8 V, the drain current of the MOSFET exceeded 100 mA, which was the limit of the semiconductor parameter analyzer. Thus, to determine the significance of the hot-carrier effect, gate and drain stress voltages of 0.9 and 1.8 V were chosen, respectively. Although a drain voltage of 1.8 V is still insufficient for the average electron energy to be high enough for interface trap generation, previous research has shown that other mechanisms are dominant under low drain voltages [1, 2, 13, 14]. The stress time applied to a single MOSFET was 10000 sec, and the application of stress was stopped at various time intervals to measure the DC and RF performances. The threshold voltage was measured by sweeping the gate voltage to obtain the I_d versus V_{gs} relationship when the drain voltage was 0.1 V. In the S-parameter measurement, the gate and drain stress voltages were both chosen to be 1.1 V. The S-parameters of the pads and the connection-transmission lines were removed by multi-line TRL calibration to obtain the actual S-parameter of the MOSFETs. In Figure 2, the normalized degradation

Fig. 3 Proposed small-signal model of MOSFETs.

Table 1 Degradation of model parameters as function of stress time.

Model Parameters	Equation
$R_{in}[Ohm]$	$\log(\Delta R_{in}/R_{in}) = 0.31\log(t) - 0.64$
$C_{in}[fF]$	$\log(\Delta C_{in}/C_{in}) = 0.36\log(t) - 0.75$
$R_m[Ohm]$	$\log(\Delta R_m/R_m) = 0.22\log(t) - 0.45$
$C_m[fF]$	$\log(\Delta C_m/C_m) = 0.24\log(t) - 0.46$
$y_m[mS]$	$\log(\Delta y_m/y_m) = 0.51\log(t) - 1.44$
$R_{out1}[Ohm]$	$\log(\Delta R_{out1}/R_{out1}) = 0.44\log(t) - 0.79$
$R_{out2}[Ohm]$	$\log(\Delta R_{out2}/R_{out2}) = 0.5\log(t) - 1.49$
$C_{out}[fF]$	$\log(\Delta C_{out}/C_{out}) = 0.2\log(t) - 0.77$
$\tau[ps]$	$\log(\Delta \tau/\tau) = 0.32\log(t) - 0.16$

of V_{th} versus stress time is shown. From the measurement result, we can see that the degradation of V_{th} satisfies a power-law relationship with stress time. After 10000 sec stress, the threshold voltage had increased by about 10%.

3 Time-Dependent Small-Signal Model Considering Hot-Carrier Effects of MOSFETs

The proposed small-signal model is shown in Figure 3. Model parameters were extracted from the Y-parameter, which was converted from the de-embedded S-parameters of the MOSFETs using the method reported in [15] and [16]. C_{in} and R_{in} represent the gate-source capacitor and resistor, C_m and R_m represent the gate-drain capacitor and resistor, and C_{out} and R_{out2} represent the drain-source capacitor and resistor, respectively. R_{out1} is the channel resistor of the MOSFET and y_m is the trans-admittance of the MOSFET.

According to [8], degradations of essential parameters in the small-signal equivalent circuit can be physically explained and linked to the drift of three DC parameters (ΔV_{th} , $\Delta \mu$, ΔR_d). Owing to the generation of interface states, the amount of parameter degradation follows a power-law relationship with the stress time. Since the saturation of the degradation effect was not observed in this study, the following function can be used to express the degradation ΔX as a function of stress time [9]:

$$\Delta X = At^n. \quad (1)$$

Fig. 4 Model parameter shifts owing to hot-carrier effect.

The parameter A , which varies with the process, was obtained from curve fitting, and is strongly dependent on V_d and weakly dependent on V_g . In a log-log scale figure, the slope n , which changes with the hot-carrier injection mechanism, is strongly dependent on V_g and weakly dependent on V_d [10]. The parameters in the small-signal model were extracted using the measured S-parameter at different stress times. Thus the model parameters of NMOS-FETs were obtained at these stress times. The time dependence of model parameters is shown in Figure 4. Applying the power-law degradation function to the model parameters, the small-signal model with stress time dependence is achieved. The time dependent equations of the degradation of the model parameters are shown in Table 1. In these equations, ΔX is the absolute value of the difference between $X(t)$ and $X(0)$. We can see that since the degradation of model parameters corresponds to interface state generation, which

follows power-law time dependence, their degradation also has power-law time dependence, as shown in Table 1 [17]. All the slopes of the equations showing the time dependence of model parameter degradations lie in a small range of 0.2-0.51 (cf. Table 1).

In this small-signal model, voltage-controlled current source (*VCCS*) with y_m is defined as

$$I_m = y_m \cdot V_{Gate}, \quad (2)$$

where I_m is controlled by input signal directly, the real part of y_m is the trans-conductance and the imaginary part of y_m is used to expressing the NQS effect only, which was previously proved for an RF small-signal model in [18] (Note that in this study, the gate resistor is in parallel with y_m which is different from the gate series NQS resistor presented by some other small-signal models [19]). The NQS effect should be considered if the MOSFET operates at very high frequency, where the quasi-static assumption is no longer valid [19]. The NQS effect considers the time required for the channel charge to build up, which is ignored in the quasi-static assumption [19]. It consists of two possible delay mechanisms, represented by the delay times τ_{sup} and τ_{tran} . Using the Matthiessen rule, $1/\tau = 1/\tau_{sup} + 1/\tau_{tran}$ [20]. τ_{sup} represents the delay of the carrier supply and τ_{tran} represents the time for the carriers to move from the source to the drain. The relaxation time τ is decreased with increasing stress time in our measurement.

From the extracted results, the capacitances are decreased. Although the physical explanation for this reduction is not quite clear in our study, similar reduction of the capacitances was reported through measurement in papers [9–11]. Possible reasons for the reduction of capacitances were explained as the local flat-band voltage shift impacting the extrinsic gate to drain overlap capacitance [10].

The supply rate of carriers is increased if the gate-source and gate-drain capacitances are reduced. Thus, it can be concluded that the time for the channel charge to build up is also decreased. In this measurement, with the degradation of capacitances C_{in} and C_m , the fitting curve of normalized relaxation time $\Delta\tau$ in $\log - \log$ scale is observed to satisfy power-law degradation.

During the reliability measurement, the effective gate bias ($V_g - V_{th}$) was decreased owing to V_{th} degradation and the vertical electric field was relaxed. However, the electron mobility is reduced by hot carriers [21]. We think maybe the reason is that although the relaxed vertical electric field will decrease the Coulomb scattering and increase the electron mobility, the dominant mechanism is surface-roughness scattering under strong inversion rather than other mechanisms, as demonstrated by Cheng et al. [21, 22]. According to Y. Matsumoto [23], the effective mobility increases first with the concentration of surface carriers N_{inv} and after the peak it decreases with the increase of N_{inv} . Two mechanisms (interface roughness scattering and charged centers distributed scattering) are responsible for the shift of mobility. So the relaxed vertical electric field will slow the parameter degradation to some extent but the reduction tendency of electron mobility is not changed.

Fig. 5 Comparison between model with NQS degradation consideration and measurement results.

Figure 5 shows a comparison of results obtained using the small-signal model and de-embedded results for a $120\ \mu\text{m}$ NMOSFET with gate and drain voltages of 1.1 V. The results of the simulation using the small signal model are in good agreement with measurement results considering NQS shift. Thus, a small-signal model for the NMOSFETs considering hot-carrier effect at mmW frequencies has been developed.

4 Conclusion

In this study, the degradation of NMOSFETs due to the hot-carrier effect was investigated. A stress-time-dependent small-signal model considering hot-carrier degradation was proposed for mmW frequencies. By comparing simulation and measurement results, it was verified that the shift of the NQS effect should be considered in the simulation of RF performance. Using the proposed small-signal model, the performance degradation of MOSFETs can be predicted as a guideline for reliability and performance optimization when designing practical circuits for mmW frequencies.

References

1. C. Guerin, V. Huard, and A. Bravaix, "The energy-driven hot-carrier degradation modes of nmosfets," *IEEE Transactions on Device and Materials Reliability*, vol. 7, pp. 225–235, June 2007.
2. S. E. Rauch, F. J. Guarin, and G. LaRosa, "Impact of e-e scattering to the hot carrier degradation of deep submicron nmosfets," *IEEE Electron Device Letters*, vol. 19, pp. 463–465, Dec 1998.
3. S. Naseh, M. J. Deen, and O. Marinov, "Effects of hot-carrier stress on the rf performance of 0.18 μm technology nmosfets and circuits," in *Proc. of 40th Annual Reliability Physics Symposium Proceedings*, pp. 98–104, 2002.
4. C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced mosfet degradation - model, monitor, and improvement," *IEEE Journal of Solid-State Circuits*, vol. 20, pp. 295–305, Feb 1985.
5. I. Kurachi, N. Hwang, and L. Forbes, "Physical model of drain conductance, gd, degradation of nmosfet's due to interface state generation by hot carrier injection," *IEEE Transactions on Electron Devices*, vol. 41, pp. 964–969, Jun 1994.
6. C. Hu, W. Liu, *et al.*, "Bsim3v3. 2.2 mosfet model. users manual," *UC Berkley*, 1999.
7. J.-T. Park, B.-J. Lee, D.-W. Kim, C.-G. Yu, and H.-K. Yu, "Rf performance degradation in nmos transistors due to hot carrier effects," *IEEE Transactions on Electron Devices*, vol. 47, pp. 1068–1072, May 2000.
8. E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Letters*, vol. 4, pp. 111–113, Apr 1983.
9. B. Dubois, J. B. Kammerer, L. Hebrard, and F. Braun, "Analytical modeling of hot-carrier induced degradation of mos transistor for analog design for reliability," in *Proc. of 8th International Symposium on Quality Electronic Design (ISQED)*, pp. 53–58, March 2007.
10. L. Negre, D. Roy, S. Boret, P. Scheer, N. Kauffmann, D. Gloria, and G. Ghibaudo, "Hot carrier impact on the small signal equivalent circuit," in *IEEE International Integrated Reliability Workshop Final Report*, pp. 72–75, Oct 2010.
11. L. Negre, D. Roy, F. Cacho, P. Scheer, S. Boret, A. Zaka, D. Gloria, and G. Ghibaudo, "Aging of 40nm mosfet rf parameters under rf conditions from characterization to compact modeling for rf design," in *Proc. of IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 1–4, 2011.
12. L. Negre, D. Roy, S. Boret, P. Scheer, D. Gloria, and G. Ghibaudo, "Advanced 45nm mosfet small-signal equivalent circuit aging under dc and rf hot carrier stress," in *Proc. of IEEE International Reliability Physics Symposium (IRPS)*, pp. HV.1.1–HV.1.4, 2011.
13. A. Bravaix, V. Huard, D. Goguenheim, and E. Vincent, "Hot-carrier to cold-carrier device lifetime modeling with temperature for low power 40nm si-bulk nmos and pmos fets," in *Proc. of IEEE International Electron Devices Meeting (IEDM)*, pp. 27.5.1–27.5.4, 2011.
14. D. Ang, T. Phua, H. Liao, and C. Ling, "High-energy tail electrons as the mechanism for the worst-case hot-carrier stress degradation of the deep submicrometer n-mosfet," *IEEE Electron Device Letters*, vol. 24, no. 7, pp. 469–471, 2003.
15. K. Katayama, M. Motoyoshi, K. Takano, and M. Fujishima, "THz matrix-based layered wrapper model of common-source MOSFET," in *Extended Abstracts of the International Conference on Solid State Devices and Materials*, Japan Society of Applied Physics, sep 2012.
16. K. Katayama, M. Motoyoshi, K. Takano, R. Fujimoto, and M. Fujishima, "Bias-voltage-dependent subcircuit model for millimeter-wave cmos circuit," *IEICE transactions on electronics*, vol. 95, no. 6, pp. 1077–1085, 2012.
17. S. P. Sinha, F. L. Duan, D. E. Ioannou, W. C. Jenkins, and H. L. Hughes, "Time dependence power laws of hot carrier degradation in soi mosfets," in *Proc. of IEEE International SOI Conference*, pp. 18–19, 1996.
18. C. C. Enz and C. Yuhua, "Mos transistor modeling for rf ic design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 186–201, 2000.
19. M. Chan, K. Y. Hui, H. Chenming, and P. K. Ko, "A robust and physical bsim3 non-quasi-static transient and ac small-signal model for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 45, no. 4, pp. 834–841, 1998.

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20. D. Ferry, *Semiconductor transport*. CRC Press, 2000.
 21. T. Matsuoka, S. Taguchi, Q. D. M. Khosru, K. Taniguchi, and C. Hamaguchi, "Degradation of inversion layer electron mobility due to interface traps in metal-oxide-semiconductor transistors," *Journal of Applied Physics*, vol. 78, no. 5, pp. 3252–3257, 1995.
 22. Y. C. Cheng and E. A. Sullivan, "Effect of coulomb scattering on silicon surface mobility," *Journal of Applied Physics*, vol. 45, no. 1, pp. 187–192, 1974.
 23. Y. Matsumoto and Y. Uemura, "Scattering mechanism and low temperature mobility of mos inversion layers," *Japanese Journal of Applied Physics*, vol. 13, no. S2, p. 367, 1974.