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2018

Lim, Z., Liu, Y., Zhang, L., Pou, J., Simanjorang, R., & Gupta, A. (2018). Design of 100 kVA SiC power converter for aircraft electric starter generator. Proceedings of the 2018 IEEE 4th Southern Power Electronics Conference (SPEC). doi:10.1109/spec.2018.8635866

<https://hdl.handle.net/10356/145012>

<https://doi.org/10.1109/SPEC.2018.8635866>

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<https://doi.org/10.1109/SPEC.2018.8635866>

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Design of 100 kVA Starter Generator Facing SiC Power Converter for Aircraft Applications

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Abstract—This paper proposes two suitable converter topologies for more electric aircraft (MEA) starter generator application. The commercially available silicon (Si) and silicon carbide (SiC) semiconductor devices are also sourced to fit the given design requirements. Different possible configurations of the evaluated converter topologies are discussed. The rectifier design methodology is presented, considering device loss distribution, converter efficiency, required heatsink thermal resistance, dc-link capacitance sizing, delivered power quality and estimated gravimetric power density. The quantitative evaluations have demonstrated the beneficial needs of driving multilevel converter at higher switching frequency operation using SiC semiconductor technology.

Keywords—Rectifier design; starter generator application; gravimetric power density; multilevel topologies; SiC technologies.

I. INTRODUCTION

The ever increasing trend in moving towards more electric aircraft (MEA) is to power non-propulsive systems with electric power. By doing so, significant improvements are made in terms of achieving better reliability, lowering maintenance costs, reducing fuel consumption and improving system efficiency [1-3]. Therefore, power conversion holds an important key role in MEA by (i) delivering a stabilized electrical power network supply at all times and (ii) satisfying the growing demand of electrically driven loads.

Bearing in minds of both weight and space constraints in the aircraft, power density should be one of the top prioritized performance trade attributes when designing these power converters. Nevertheless, other trade attributes such as power quality, converter efficiency and reliability should not be comprised as well. Driving the power converter at higher switching frequency is one of the prominent solutions to achieve high power density as the passive elements sizing can be reciprocally reduced [4, 5]. The delivered power quality is also greatly improved with the reducing filter effort.

The next generation wide bandgap power semiconductor devices based on Silicon Carbide (SiC) shall be the preferable switching devices as compared to the unmaturing high power rating Gallium Nitride (GaN) based and the popularly known Silicon (Si) based devices. The essential advantages of employing the wide bandgap power devices over the common Si-based devices are already well highlighted in [6-8].

Additionally, the SiC-based power devices are reported to operate at high air ambient temperatures up to 500 °C [8, 9]. With such attractive characteristics, the SiC-based power converter can thus be operated in a harsh environment. This allowed the power converter to be placed nearer to the aircraft engine shaft-connected starter/generator (S/G) which is subjected to high ambient temperature above 200 °C.

High power density converter design as discussed in [10, 11] are all mainly for network facing inverter configuration. Hence, this paper focuses more on the three-phase converter (rectifier) design for a 100 kVA MEA S/G in Fig. 1. Important design attributes are investigated and evaluated in this paper based on different topologies, commercially available power devices selection, and dc-link capacitors sizing.

II. DESIGN REQUIREMENTS

Fig. 1. System topology diagram for MEA application.

The system topology in Fig. 1 shows that the permanent magnet synchronous starter generator (PMSG) is coupled to the shaft of the aircraft engine and is controlled by an active front-end three-phase converter. The converter must be designed to manage bidirectional power flow direction with the capability to handle a continuous power of 45 kW and 60 kW during respective motoring and generating operations.

During the generating mode, the designed converter will rectify the input generated electric power from variable frequency variable voltage to the output stable bipolar dc supply network. The dc-bus architecture is constructed with a bipolar of ± 270 V_{dc} and the neutral point must be actively controlled balance at all times.

The high-level system parameters are described in Table I. The designed converter must be able to satisfy the given input voltage and current ratings based on the PMSG parameters and also targeted to achieve with an efficiency of greater than 95%.

TABLE I
HIGH-LEVEL SYSTEM PARAMETERS

Parameters		Generating Operation	
PMSG	Rotor Speed	8000 RPM (Idle)	16000 RPM (Maximum)
	Phase Current RMS	270 A _{RMS}	130 A _{RMS}
	Back EMF Phase Voltage RMS	80 V _{RMS}	160 V _{RMS}
	Terminal Phase Voltage RMS	130 V _{RMS}	190 V _{RMS}
	Power Factor (PF)	0.6	0.85
	Electrical Frequency (f_e)	659 Hz	1350 Hz
Design Converter	Maximum Output Power	60 kW	
	Output DC Voltage	540 V _{dc} (± 270 V _{dc})	
	DC-Bus Voltage Variation	MIL-Std-704	
	Target Converter Efficiency	> 95%	

III. EVALUATED CONVERTER TOPOLOGIES

As the designed converter is required to support both motoring and generating operation modes, hence bidirectional converter architectures are being considered only. Besides that, the topologies must have the capability to control actively and maintain the bipolar dc voltages balanced. Since achieving high power density is one of the key performance attributes, two candidate topologies with lesser component counts are being selected and described in the following.

A. 2L – Voltage Source Converter with Balancer (2L-VSCB)

The three-phase two-level voltage source converter as shown in Fig. 2(a) is well-known for its simple topological structure which can be easily constructed using six switches with two switches in each phase-leg. However, the voltage source converter has zero control capability of the neutral potential in the bipolar dc-link configuration. As a result, it is necessarily to have an additional dc-dc balancer which requires extra two switches and an inductor connected between the split dc-link capacitors.

B. 3L – T-Type Clamped Converter (3L-TTCC)

The topological structure of three-phase three-level T-type clamped converter as shown in Fig. 2(b) is simple and attractive. The circuit configuration requires only twelve switches (four switches in each phase-leg) as compared to the other three-level topologies such as three-level neutral point clamped converter and three-level flying capacitor clamped converter. In addition to that, 3L-TTCC also has the control capability to balance the neutral potential with the bidirectional switches connected between the input and the mid-point of two dc-link capacitors.

IV. CONVERTER DESIGN CONSIDERATIONS

The continuous maximum power handling capability for the converter is higher during its 60 kW generating operation as compared to the 45 kW motoring mode. Thus, the converter design has to consider the maximum device ratings that support for generation conditions in Table I. Furthermore, one could observe that the current rating is higher when the PMSG rotor is rotating at lower speed. As for the device voltage rating, it greatly depends on the topology selection. In this case, only those neutral point switches of 3L-TTCC are low voltage rating devices as labelled in blue while others in red labels are high voltage rating devices.

Fig. 2. Selected bidirectional converter topologies (a) 2L-VSCB, (b) 3L-TTCC (hybrid SiC MOSFETs outer switches with Si IGBTs common-emitter configured neutral point switches), (c) common-collector configured neutral point switches and (d) alternative full SiC MOSFETs neutral-point switches for 3L-TTCC.

A. Available Commercial Power Semiconductor Devices

Sourcing for appropriate power semiconductor devices whilst satisfying the power rating requirements is essentially important in converter design as it may affect the switching frequency operation, device losses, overall efficiency, thermal management and power density. Only power module packaging based on wide bandgap SiC MOSFET and matured Si IGBT are considered in this paper.

The required blocking voltage rating of the devices must be at least 1.5 times greater than the dc-link voltage (540 V_{dc}) and the deemed current rating must be greater than 270 A_{RMS} based on the idle rotor speed. Hence, a 900 V power devices would be sufficiently good enough for the converter design. However, the lowest blocking voltage rating of the SiC MOSFET power modules found in the market that can handle the current rating of 300 A_{RMS} is only available at 1.2 kV. For fair comparison, 1.2 kV Si IGBT power modules with same 300 A_{RMS} current ratings are considered.

The candidate commercially available SiC and Si semiconductor devices are identified in Tables II and III respectively with the important device characteristics extracted from the datasheet. These required parameters for loss analysis are turn-on voltage (V_{on}), on-resistance (R_{on}), turn-on and turn-off loss (E_{on} and E_{off}), and recovery loss (E_{rec}).

According to Table II, all the SiC MOSFET devices are half-bridge configured power modules which consist solely of two switches. It can be noted that almost all the available SiC devices with same ratings in the market have different packaging except for Cree CAS300H12BM2 and Semikron SKM350MB120SCH17 which shares the similar packaging.

As for the commercial Si IGBT devices in Table III, there are different types of bidirectional configurations for the neutral point switches T3 and T4 of Fig. 2(b) which are namely

TABLE II
COMMERCIALLY AVAILABLE SILICON CARBIDE (SiC) SEMICONDUCTOR DEVICES

Parameters	1200V SiC Cree CAS300H12BM2		1200V SiC Cree CAS325M12HM2		1200V SiC Semikron SKM350MB120SCH17		1200V SiC Rohm BSM300D12P2E001		1200V SiC Fuji Electric 2CSI300CAS120A-50	
	MOSFET	Diode	MOSFET	Diode	MOSFET	Diode	MOSFET	Diode	MOSFET	Diode
V_{on} (V)	0	0.825	0	0.833	0	1.05	0	0.705	0	0.72
R_{on} (mΩ)	7.7	6.7	7.6	8	9.5	12	15	5.67	10.6	9.067
E_{on} (mJ)	5.8 (600V 300A)	-	5.6 (600V 300A)	-	8.65 (600V 300A)	-	9.5 (600V 300A)	-	4.3 (600V 300A)	-
E_{off} (mJ)	6.1 (600V 300A)	-	3.7 (600V 300A)	-	7.98 (600V 300A)	-	10.5 (600V 300A)	-	10 (600V 300A)	-
E_{rec} (mJ)	-	0.64 (600V 300A)	-	0.86 (600V 300A)	-	0.088 (800V 500A)	-	0.7 (600V 350A)	-	2.57 (600V 300A)
I_D (A)	300 / 423 ($T_j = 25^\circ\text{C}$)		325 / 444 ($T_j = 25^\circ\text{C}$)		523 ($T_j = 25^\circ\text{C}$)		600 ($T_j = 60^\circ\text{C}$)		600 ($T_j = 25^\circ\text{C}$)	
Max Junction Temperature T_j ($^\circ\text{C}$)	150		175		175		175		175	
Thermal Resistance $R_{th(j-c)}$ ($^\circ\text{C}/\text{W}$)	0.075	0.076	0.115	0.127	0.045	0.18	0.08	0.11	0.098	0.098
Packaging										
Weight (kg)	0.3		0.14		0.325		0.35		TBD	
Dimension (mm × mm × mm)	62 × 106 × 30		65 × 110 × 10		62 × 106 × 30		62 × 152 × 17		42 × 126 × 19	
Cost (USD)	558		1306		473		668		~	

(i) the antiparallel reverse blocking IGBT (RB-IGBT), (ii) common emitter anti-series IGBT (CE-IGBT) and common-collector anti-series IGBT (CC-IGBT). There are also full Si IGBT based T-type power modules with T3 and T4 configured using either RB-IGBT or CC-IGBT. Currently, there is no SiC MOSFETs based for both three-level T-type power module and the reverse-blocking switches in the market.

B. Possible Configurations of Evaluated Topologies

The 2L-VSCB in Fig. 2(a) can be constructed easily using either the wide bandgap SiC MOSFETs or the matured Si IGBTs. With reference to the previously developed high power density SiC based two-level voltage source inverter in [11], it has successfully achieved high converter efficiency with lower losses even at 100 kHz high switching frequency operation. The 50 kW prototype has clearly demonstrated the advantages of employing wide bandgap switching devices. Therefore, this paper shall focus on comparing and evaluating the performance of SiC based 2L-VSC with the 3L-TTCC.

On the contrary side, the 3L-TTCC can be constructed with (i) full SiC MOSFET, (ii) hybrid configuration of Si IGBT and SiC MOSFET (Fig. 2(b)) or (iii) full Si IGBT. Since there is no availability of SiC based power module for the neutral switches T3 and T4, the construction of full SiC configured 3L-TTCC will hence not be that straightforward. As a result, the T3 and T4 in Fig. 2(b) have to be replaced using two sets of half-bridge SiC MOSFET power modules as shown in Fig. 2(d).

The possible configurations of 2L-VSCB and 3L-TTCC will be listed in Table IV using the commercial power modules in Tables II and III. A series of performance evaluations will be carried out and investigated before recommending the potential switching devices.

V. COMPARISON METHODOLOGY AND RESULTS

For power converter design optimization, it is necessary to investigate the semiconductor device performances in terms of loss distribution, efficiency, thermal resistance, as well as the passive filter sizing. These important design considerations have great influential on the converter power density, the optimal switching frequency operation and the power quality based on the corresponding converter topologies. The evaluative analysis will be discussed in the following sections.

A. Switching and Conduction Losses

The device loss analysis is conducted assuming that (i) the converters operate under hard switching scheme, (ii) sinusoidal PWM modulation technique is employed, (iii) both voltage and current waveforms are ripple free, (iv) current sharing between MOSFET and free-wheeling diode is disregarded and (v) current is assumed to flow through the anti-parallel diode only (not considering third quadrant operation of MOSFET).

Both conduction loss and switching loss for the transistors (subscript T) and diodes (subscript D) are expressed generally in (1) and (2) respectively. V_o is initial device voltage drops, R_{on} is the turn-on resistance, V_{sw} is the actual device turn-off voltage, $\hat{I}_L$ is the peak amplitude of input current, f_s is the switching frequency operation and E_{on} , E_{off} and E_{rr} are the device turn-on, turn-off and reverse recovery energy losses under the conditions of datasheet current and voltage levels I_{ref} and V_{ref} respectively.

$$P_{conT/D} = I_{avg} V_{oT/D} + I_{rms}^2 R_{onT/D} \quad (1)$$

$$P_{swT/D} = \frac{V_{sw} \hat{I}_L}{V_{ref} I_{ref}} (E_{T/D}) f_s \quad \left| \begin{array}{l} E_T = E_{on} + E_{off} \\ E_D = E_{rec} \end{array} \right. \quad (2)$$

TABLE III
COMMERCIALLY AVAILABLE SILICON (SI) SEMICONDUCTOR DEVICES

Parameters	1200V Si Semikron SKM300GBD12T4		1200V Si Semikron SKM400GM12T4		1200V Si Infineon FF400R12KT3_E		1200V Si Fuji Electric 4MB1400VF-120R-50		1200V Si Infineon F3L400R12PT4_B26		1200V Si Semikron SEMIX405TML112E4B	
	IGBT	Diode	IGBT	Diode	IGBT	Diode	IGBT	Diode	IGBT	Diode	IGBT	Diode
V_{on} (V)	0.54	0.47	0.56	0.47	0.625	0.6	0.62 / 0.53	0.6 / 0.53	0.5 / 0.6	0.55 / 0.5	0.87 / 0.58	0.77 / 0.42
R_{on} (mΩ)	5.5	55.8	4	6.175	5.375	5.375	6.4 / 7.9	8.167 / 0	5.4 / 5.4	5.75 / 4.9	4 / 3.1	6.18 / 4.4
E_{on} (mJ)	27 (600V 300A)	-	33 (600V 400A)	-	28 (600V 400A)	-	50 / 38.3 (400V 300A)	-	13.5 / 11 (300V 400A)	-	6 / 3 (300V 400A)	-
E_{off} (mJ)	29 (600V 300A)	-	42 (600V 400A)	-	45 (600V 400A)	-	29.7 / 12.5 (400V 300A)	-	28.5 / 24.5 (300V 400A)	-	28 / 23 (300V 400A)	-
E_{rec} (mJ)	-	22.86 (600V 300A)	-	13.6 (600V 400A)	-	16 (600V 400A)	-	14.8 / 4.9 (400V 300A)	-	7.15 / 19 (300V 400A)	-	11.8 / 11 (300V 400A)
I_c (A)	324 / 422 ($T_c = 25^\circ\text{C}$)		474 / 616 ($T_c = 25^\circ\text{C}$)		400 / 580 ($T_c = 25^\circ\text{C}$)		400 / 450 ($T_c = 80^\circ\text{C}$)		600 / 360 ($T_c = 25^\circ\text{C}$)		636 / 453 ($T_c = 80^\circ\text{C}$)	
Max Junction Temperature T_j ($^\circ\text{C}$)	175		175		125		125		150		175	
Thermal Resistance $R_{th(j-c)}$ ($^\circ\text{C}/\text{W}$)	0.11	0.14	0.072	0.14	0.062	0.11	0.068 / 0.056	0.173 / 0.056	0.07 / 0.17	0.16 / 0.22	0.068 / 0.14	0.18 / 0.02
Packaging												
Switch Configuration												
Weight (kg)	0.325		0.325		0.34		0.46		0.4		0.398	
Dimension (mm × mm × mm)	62 × 106 × 30		62 × 106 × 30		62 × 106 × 30		80 × 110 × 30		70 × 130 × 20		70 × 130 × 20	
Cost (USD)	176		193		146		126		251		289	

TABLE IV
POSSIBLE CONFIGURATIONS OF 2L-VSCB AND 3L-TTCC

Topologies	T1 & T2		T3 & T4		Operating Switching Frequency
2L-VSCB (Full SiC)	SiC	CAS300H12BM2 CAS325M12HM2 SKM350MB1230SCH17 BSM300D12P2E001 2CSI300CAS120A-50	~		20 kHz / 100 kHz
3L-TTCC (Full SiC)	SiC	CAS300H12BM2 CAS325M12HM2 SKM350MB1230SCH17 BSM300D12P2E001 2CSI300CAS120A-50			20 kHz / 100 kHz
3L-TTCC (Hybrid)	SiC	CAS300H12BM2 CAS325M12HM2 SKM350MB1230SCH17 BSM300D12P2E001 2CSI300CAS120A-50	Si	SKM300GBD12T4 SKM400GM12T4 FF400R12KT3_E	20 kHz
3L-TTCC (Hybrid)	Si	4MB1400VF-120R-50 F3L400R12PT4_B26 SEMIX405TML112E4B			20 kHz

The detailed analytical loss expressions for the respective devices of the 2L-VSCB and 3L-TTCC were already developed in [12]. Due to the circuit symmetry, the device loss distribution was calculated only for T1 and D1 of 2L-VSCB (w.r.t. Fig. 2(a)) as well as T1, D1, T3 and D3 of 3L-TTCC (w.r.t. Fig. 2(b)) based on the possible configurations using different semiconductor devices as listed in Table IV.

The power semiconductor loss profiles for 2L-VSCB and 3L-TTCC in Fig. 3 are also evaluated according to different rotor speed (different power factor operation - Table I). Besides that, it is important to mention that the performance evaluated for 2L-VSCB does not include any device losses and passive inductor loss in the dc-dc balancer.

Without considering the dc-dc balancer loss, the total device losses for T1 and D1 of 2L-VSCB are already higher than the total losses of T1, D1, T3 and D3 in 3L-TTCC under

Fig. 3. Overall converter efficiency and device loss distribution based on the possible configurations of 2L-VSC and 3L-TTCC in Table IV for (a) idle speed at 8000 RPM and (b) maximum speed at 16000 RPM.

the same switching frequency operation of 100 kHz and the same full SiC MOSFETs based configuration. As for the comparison of the 3L-TTCC with different semiconductor device combinations, the full SiC MOSFET-based and the hybrid configurations (II) and (III) offer better choices compared to the hybrid (I) and the full Si IGBT-based.

The hybrid configuration (I) has poorest performance as it experienced additional conduction losses simply because of the two additional diodes (cf. Table III) in the neutral point. As for the full Si IGBT-based 3L-TTCC, high switching losses is owned to the huge amount of energies required for turning on and off the transistors. Conversely, the Si IGBT generates lower conduction losses than SiC MOSFET due to its lower on-state resistance.

As SiC MOSFET performs contrary to the Si IGBT, one can conclude that the Si IGBT is beneficial for achieving lower conduction loss. On the other hand, SiC MOSFET is attractive for generating lower switching loss. Therefore, if the 3L-TTCC is desired for operating at much higher switching frequency operation, then the full SiC MOSFET configuration would be greatly recommendable, otherwise it will be the hybrid configuration (II).

B. Converter Efficiency

It is clearly observed in Fig. 3 that higher losses are experienced when the starter generator is rotating at an idle speed of 8000 RPM (PF = 0.6) as compared to those during maximum speed of 16000 RPM (PF = 0.85). Conforming to the power balance principle theorem, the reason of experiencing high device losses is caused by the increase in the current magnitude (when power factor is low) as the voltage amplitude decreases correspondingly to the back EMF constant value (K_e = Peak EMF voltage / RPM).

Hence, it is important to design the converter efficiency to be greater than 95% based on the worst case condition when the power is generated during idle speed. Generally, all configurations have achieved efficiency of more than 95% except for 2L-VSCB using Rohm BSM300D12P2E001 and hybrid configuration (I) of 3L-TTCC as proven in Fig. 3.

For further evaluation between 2L-VSCB and 3L-TTCC, the rated converter efficiency under the condition of unity power factor was compared again in Fig. 4(a) solely based on SiC MOSFET from Cree and Semikron as they were evidently proven to produce lower device losses compared to other SiC MOSFETs in Fig. 3. It is noticeable that converters constructed using both Cree power modules CAS300M12BM2 and CAS325M12HM2 have comparable efficiency. As for the Semikron SKM350MB120SCH17, it will be beneficial in cases when 2L-VSCB operates below 32 kHz and 3L-TTCC operates at higher switching frequency range.

Therefore, Semikron SKM350MB120SCH17 is better options for analyzing the converter efficiency under different power factor operations (different rotor speed conditions) and different switching frequency operation of 20 kHz and 100 kHz as shown in Figs. 4(b) and 4(c) respectively. Again, the results have validated the discussed relationship (i) between the converter efficiency and the power factor operation based on

Fig. 4. Converter efficiency comparison for full SiC based of 2L-VSCB (excluding balancer loss) and 3L-TTCC. (a) Rated power (PF = 1), Semikron SKM350MB120SCH17 with (b) $f_s = 20$ kHz and (c) $f_s = 100$ kHz.

Fig. 5. Thermal equivalent circuit for n number of transistors (subscript T) and diodes (subscript D) used in the converter topology.

Fig. 6. Required heatsink thermal resistance for 2L-VSCB and 3L-TTCC based on full SiC and hybrid (II) configurations according to (a) idle speed 8000 RPM and (b) maximum speed 16000 RPM.

Fig. 7. Required heatsink thermal resistance for 3L-TTCC based on outer switches (T1, T2), SiC-based neutral switches (T3, T4) and Si-based for T3 and T4 according to (a) 8000 RPM and (b) 16000 RPM.

different rotor speed range (higher power factor higher efficiency) as well as (ii) between the converter efficiency and the operating switching frequency range (lower switching frequency higher efficiency). Henceforth, the converter efficiency for both 2L-VSCB and 3L-TTCC greatly depend on the desired switching frequency operation.

C. Thermal Resistance

Cooling down the power modules is essentially important when the converter is operating continuously, thus designing of heatsink is necessarily required to prevent the switching devices from thermal runaway. The main objective of designing the heatsink is to ensure that the device junction temperature ($T_{j,T/D}$) is always maintained below the maximum allowable temperature (typically between 125 °C to 175 °C depending on device datasheet).

Based on the equivalent thermal circuit as shown in Fig. 5, the required heatsink thermal resistance $R_{th,sa}$ can be determined using the derived expression (3) where T_a is the ambient or coolant temperature, $P_{loss,T/D}$ is the power loss of each respective transistors or diode, $P_{loss,mod}$ is the total power loss of transistor and diode, $R_{th,jc}$ is the junction to case thermal resistance and $R_{th,cs}$ is the case to heatsink thermal resistance.

$$R_{th,sa} = \frac{(T_{j,T/D} - T_a) - P_{loss,T/D}(R_{th,jc,T/D} + R_{th,cs})}{P_{loss,mod}} \quad (3)$$

The values of $R_{th,jc,T/D}$ for switching transistors and free-wheeling diodes can be extracted from the device datasheet, while the $R_{th,cs}$ is assumed to be 0.03 K/W and 0.12 K/W for switch and diode respectively. The conducted analysis in this study does not consider the peak junction temperature due to the transient power loss. The coolant temperature T_a is assumed to be 30 °C when used in the heatsink.

The required $R_{th,sa}$ for 2L-VSCB and 3L-TTCC are investigated based on full SiC MOSFETs and hybrid (II) configurations. SiC MOSFETs from Cree CAS300M12BM2, CAS325M12HM2 and Semikron SKM350MB120SCH17 are being chosen for thermal analysis based on the discussed performance in the device loss analysis and converter efficiency.

The minimum $R_{th,sa}$ needed to maintain the respective devices $T_{j,T}$ (as given in the Tables II and III) are shown in Figs. 6 and 7. Typically, $T_{j,T}$ requires careful attention for heatsink design as compared to $T_{j,D}$. This is mainly because the power losses for the free-wheeling diodes are generally very low. Hence, the heat sources are principally generated from the transistors.

When comparing the three selected SiC MOSFET devices based on 2L-VSCB topology in Fig. 6, CAS325M12HM2 offers lesser thermal requirement when compared to CAS300M12BM2 as it allows wider bandwidth of $R_{th,sa}$ (higher values) for designing the heatsink. This is mainly because CAS325M12HM2 has higher maximum T_j rating of 175 °C. However, the SKM350MB120SCH17 has even lesser thermal requirement when switching frequency operation is greater than 33 kHz.

For evaluating the thermal performance of 3L-TTCC, it can be clearly observed in Fig. 7 that the thermal requirement increases exponentially for the outer switches T1 and T2 while the neutral-point switches T3 and T4 remain relatively stable and constant. Thus, the thermal requirement for 3L-TTCC should be determined based on the lowest calculated $R_{th,sa}$

Fig. 8. DC current ripple factor as a function of Mx range.

values which is set as a benchmark for the heatsink design. In the event of idle speed operation, the thermal requirement for full SiC MOSFET based 3L-TTCC is highlighted in red line of Fig. 7(a). If a hybrid (II) configuration is being selected under the same conditions with outer switches T1 and T2 using SKM350MB120SCH17, the heatsink shall be designed based on the more stringent thermal requirement according to the determined $R_{th,sa}$ of the neutral switches T3 and T4 (considering the f_s operation is limited to 60 kHz for Si IGBT).

The comparison of required $R_{th,sa}$ in Fig. 6(a) shows that 3L-TTCC has lesser thermal requirement than 2L-VSCB based on the same full SiC configurations. Similarly for comparing the heatsink thermal requirement during different operating speed in Figs. 6 and 7, the heatsink $R_{th,sa}$ must be carefully designed by considering only the worst case condition which is during the idle speed operation. In general, cold plate thermal resistance can be designed with $R_{th,sa}$ lesser than 0.2 °C/W with low flow rate of about 1 litre per minute (LPM). Consequently, even the hybrid (II) configured 3L-TTCC that has highest thermal requirement can be cooled without any issues.

D. DC-Link Capacitor Sizing

Another important design factor for the AC-DC converter is the sizing and dimensioning of the dc-link capacitors, as it is required to sustain a stable bipolar ± 270 V_{dc} network. Thus, it is mandatory to comply the strict MIL-Std-704 [13] that allows only a maximum dc voltage ripple amplitude of 6V, a distortion factor of 0.015 (1.5%) and maintain the each 270 V_{dc} bus bar voltage between 250 V_{dc} to 280 V_{dc}.

For the dc-link capacitors sizing, the maximum current stress on the dc-link capacitors (C_1 and C_2) must first be determined by the geometrical subtraction of the total three-phase ac rms current and the dc average current [14, 15]. The capacitor current stress is greatly dependent on delivered power (P_o), modulation index (M_x) and the power factor angle (ϕ).

$$C_{dc(2L-VSC)} \approx \frac{\left(\frac{8 \times P_o}{3 \times M_x \times V_{dc} \times \cos \phi} \right) \sqrt{\frac{M_x \sqrt{3}}{4\pi} + \cos^2(\phi)} \left(\frac{M_x \sqrt{3}}{\pi} - \frac{9(M_x^2)}{16} \right)}{\Delta V_{dc} \times f_s} \quad (4)$$

$$C_{dc(3L-TTCC)} \approx \frac{\left(\frac{8 \times P_o}{3 \times M_x \times V_{dc} \times \cos \phi} \right) \sqrt{\frac{M_x}{2} \left(\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9 \times M_x}{8} \right) \cos^2(\phi) \right)}}{\Delta V_{dc} \times f_s} \quad (5)$$

Thereafter, the dc-link capacitance value for 2L-VSCB and 3L-TTCC can be calculated according to (4) and (5) based on the given permissible dc voltage ripple (ΔV_{dc}), the switching frequency operation (f_s) and the maximum dc capacitor current stresses that are affected by modulation index (Mx) and power factor ($\cos \phi$). The dc current ripple factor in Fig. 8 shows the dependency of the dc-link capacitor current rms value to the converter phase rms current. The capacitor rms current for 3L-TTCC (red lines) is proven to be much lower compared to 2L-VSCB (blue lines) despite of different Mx and PF operations. But one can conclude that the capacitor current ripple is experienced to be highest when the converter operates at 0.61 Mx and unity PF.

The required capacitance values ($C_1 = C_2$) for 2L-VSCB and 3L-TTCC are determined to be 433.9 μF and 306.8 μF respectively considering the worst case condition (idle speed and $f_s = 100$ kHz). According to the inversely proportional relationship between C_{dc} and f_s , it would be more desirable to operate the converter at higher switching frequency. By doing so, the capacitance values required can be significantly reduced in returns. Nevertheless, the sizing and dimensioning of the dc-link capacitors for the converter design are not that simple by just based on the calculated capacitance values. Various factors have to be taken into considerations such as (i) the total weight after series-parallel the capacitors, (ii) the equivalent series resistance (ESR) of the capacitors and (iii) also important to ensure that the maximum permissible voltage ripple and the determined capacitor current must be lesser than rated voltage and current ratings given by the manufacturer datasheet.

E. DC-Link Distortion Factor

According to MIL-STD-704-F, only the DC distortion factor of less than 0.015 (1.5%) for the 270 V_{dc} system that must be strictly complied to. The dc-link distortion factor performance presented in Table V is evaluated based on the bipolar 270 V_{dc} as well as the total dc-link 540 V_{dc} regardless of any semiconductor configurations for the evaluated topologies. The results have fully satisfied the requirements with distortion factor achieved less than 1.5 % even based on the calculated minimum dc-link capacitance values.

The dc-link distortion factor can be reduced either by (i) employing higher capacitance values or (ii) increase switching frequency operation. Besides that, multilevel topologies are alternative solution to reduce the dc-link voltage ripples. The 3L-TTCC with lower f_s operation of 20 kHz achieves comparable performance as 2L-VSCB operating at 100 kHz during the worst case condition (8000 RPM).

F. Input Power Quality Performances

The stringent requirement in MIL-STD-704-F for ac variable frequency operation only applies for the steady state rms voltage between 108 V_{rms} to 118 V_{rms} and frequency range between 360 Hz and 800 Hz. Thus, there is no official standards applicable for the given system parameters described in Table I. However, the harmonic quality of both synthesized voltage waveforms and input current shaping for the respective rectifier topologies are still evaluated in Table VI.

TABLE V
DC-LINK DISTORTION FACTOR EVALUATION

DC-Link Capacitance ($C_1 = C_2$)		800 μF		2400 μF		Calculated Capacitance	
Topology	f_s (kHz)	270 V _{dc} DF (%)	540 V _{dc} DF (%)	270 V _{dc} DF (%)	540 V _{dc} DF (%)	270 V _{dc} DF (%)	540 V _{dc} DF (%)
8000 RPM							
2L-VSCB	20	0.41	0.37	0.13	0.12	~	~
	100	0.19	0.19	0.06	0.06	0.42	0.41
3L-TTCC	20	0.73	0.20	0.62	0.06	~	~
	100	0.54	0.09	0.54	0.04	0.68	0.32
16000 RPM							
2L-VSCB	20	0.39	0.38	0.17	0.17	~	~
	100	0.10	0.10	0.04	0.04	0.19	0.18
3L-TTCC	20	0.73	0.26	0.32	0.07	~	~
	100	0.52	0.07	0.31	0.02	0.68	0.21

TABLE VI
INPUT VOLTAGE AND CURRENT DISTORTION FACTOR EVALUATION

DC-Link Capacitance ($C_1 = C_2$)		800 μF		2400 μF		Calculated Capacitance	
Topology	f_s (kHz)	V _{phase} (%)	I _{phase} (%)	V _{phase} (%)	I _{phase} (%)	V _{phase} (%)	I _{phase} (%)
8000 RPM							
2L-VSCB	20	180.98	1.64	181.22	1.62	~	~
	100	151.55	0.61	151.33	0.55	151.34	0.79
3L-TTCC	20	102.10	0.95	109.47	0.80	~	~
	100	95.59	0.31	98.44	0.42	94.55	0.51
16000 RPM							
2L-VSCB	20	95.78	8.11	96.04	8.10	~	~
	100	86.35	1.90	86.57	1.89	86.61	1.98
3L-TTCC	20	63.20	3.98	56.48	3.51	~	~
	100	56.96	1.13	51.48	0.75	58.44	1.11

At lower rotor speed, one can observe that the current (I_{phase}) THD is much lower as compared to those during higher speed condition. This is mainly due to the increasing magnitude of fundamental frequency harmonic over the other carrier and sideband harmonic components. The phase voltage (V_{phase}) THD performance is vice versa where lower THD is achieved during higher speed condition.

Generally, the input current shaping performance can be improved by (i) synthesizing higher number of stepped levels phase voltage waveforms or (ii) increasing the switching frequency operation so that the magnitudes of unwanted carrier and sideband harmonics can be reduced by shifting further away from the fundamental frequency component. Henceforth, superior power quality can be delivered by a multilevel topological converter (3L-TTCC) that operates at higher switching frequency. It is potentially beneficial for any drives.

VI. DESIGN OF 3L-TTCC PROTOTYPE

According to the analytical results discussed in Section V, the 3L-TTCC is identified to be the optimal performing topology compared to the 2L-VSCB. The estimated weight of the relevant components required for 2L-VSCB and 3L-TTCC are listed in Table VII assuming same semiconductor packaged devices, dc-link capacitors, bus bar as well as sensors and controller boards are used. The calculated power density of the 2L-VSCB does not include the weight of additional two switches and an inductor. Therefore, the power density is expected to be much lower as the balancer inductor that must be designed to handle both ac and dc current components. This resulted the 3L-TTCC to achieve superior power density. The

hybrid (II) configuration would be preferable when 3L-TTCC operates at lower f_s , otherwise constructing it with full SiC MOSFETs will be more desirable with the aim to deliver better power quality.

The 3D illustration of full SiC-based 3L-TTCC is modelled in Fig. 9 and the hardware prototype design of 3L-TTCC is currently under development. A series of experiments include double pulse tests (DPT) are performed for evaluating the switching characteristics of the selected semiconductor. It is also important to design an optimized bus bar structure with low parasitic inductance. The DPT has been conducted experimentally with the optimized dc bus bar design in [16]. The designed pin fin heatsink is developed and achieved $R_{th,sa}$ of 0.034 °C/W with the flow rate of 6 LPM. The detailed design of cold plate will be discussed again on its improved cooling capability. The completed hardware development will be comprehensively verified against the analytical work done in this study.

VII. CONCLUSION

In this paper, a quantitative evaluation is performed for identifying the most suitable rectifier topology for the 100 kVA MEA S/G facing application. The topology must be capable to support the required bipolar dc bus structure and satisfied the given requirements. Potential semiconductor technologies with appropriate ratings are sourced for all possible configurations of 2L-VSCB and 3L-TTCC. Different design elements such as device loss distribution, converter efficiency, required heatsink thermal resistance, dc-link capacitor sizing and power quality issues are evaluated and discussed. The rectifier is designed to handle the power rating based on the worst case condition which is during the idle speed operation.

According to the presented results, the 3L-TTCC achieves superior performances even when operating at lower f_s . However, driving 3L-TTCC using full SiC power modules at higher f_s is proven to be more advantageous. It allows the weight of passive dc-link capacitance to be further reduced and eliminates the need of installing additional input inductance filters. With its excellent current shaped waveforms, it is attractively beneficial for any machine drives.

ACKNOWLEDGMENT

This work was conducted within the Rolls-Royce@NTU Corporate Lab with support from the National Research Foundation (NRF) Singapore under the Corp Lab@University Scheme.

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Fig. 9. 3D CAD drawings of three-level T-type full SiC based converter.

TABLE VII
ESTIMATED GRAVIMETRIC POWER DENSITY

Components	2L-VSCB* (Full SiC)	3L-TTCC (Full SiC)	3L-TTCC (Hybrid II)
Switching Frequency	100 kHz	100 kHz	20 kHz
Power Modules*	0.975 kg	2.925 kg	1.950 kg
DC-Link Capacitors* (C1 = C2 = 800 µF)	1.84 kg	1.84 kg	1.84 kg
Bus Bar*	3.30 kg	3.30 kg	3.30 kg
Designed Pin Fin Heatsink	0.58 kg	1.74 kg	1.16 kg
DC Snubbers	0.30 kg	0.63 kg	0.39 kg
Gate Drivers	0.09 kg	0.27 kg	0.18 kg
Sensors & Controller*	1.50 kg	1.50 kg	1.50 kg
Total	8.585 kg[#]	12.205 kg	10.320 kg
Application Power Density (PF = 0.6)	6.99 kW/kg[#]	4.92 kW/kg	5.81 kW/kg
Rated Power Density (PF = 1)	11.65 kW/kg[#]	8.19 kW/kg	9.69 kW/kg

Notes:

- 1) * - Assuming same semiconductor-packaged power modules, dc-link capacitance, bus bar as well as sensor conditioning and controller boards are used.
- 2) # - The total weight of 2L-VSCB in Table VII excludes the additional weight of the active dc-dc balancer circuit (two switches and an inductor).

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