Design of RF front-end circuit blocks for low-power applications

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DESIGN OF RF FRONT-END CIRCUIT BLOCKS FOR LOW-POWER APPLICATIONS

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Master of Engineering

2008

STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Lim Kok Meng

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SUMMARY

This report aims to provide a comprehensive review as well as the design of the various high frequency circuits found in almost all the transceivers in the market today. Wireless communication has become a natural part of everyone's life, its presence can be seen all around. The high frequency circuits include low noise amplifiers (LNA), mixers and pre-amplifiers (PA).

In every receiver system, the LNA is the first block placed in the receive path, therefore its performance is critical in the exact operation of the receiver. The primary role of the LNA is to amplify the weak Radio Frequency (RF) signals, having suffered propagation loss after transmission through a medium, while minimizing its noise contribution to the overall system. Gain and noise figure are well correlated, higher gain would produce lower noise figure. Correspondingly, to achieve high gain, power consumption is increased. For mobile wireless devices, this would cause a severe drain on battery life. Therefore a novel LNA, operating in the subthreshold region is introduced to alleviate this issue.

Most modulators and demodulators are not able to achieve the high sampling rate required at RF frequencies. Thus, mixers circuits are needed to convert the modulated signals with a carrier frequency to the desired frequency. In the case of a transmitter system, the mixer is used to up convert the modulated immediate frequency (IF) into RF signal for transmission. Due to modulation scheme adopted and high bandwidth requirements of certain wireless applications, a wideband and high linearity mixer is needed to fulfill these functions.

Lastly, a transmitter would need to drive an off chip load, usually in the form of an antenna. A PA is usually employed to accomplish the task. By incorporating a power amplifier on-chip several considerations need to be addressed, a power amplifier have high gain resulting in a huge signal swings. These signals tend to find their way to other frequency sensitive circuits such as oscillators, through certain feedback paths or substrate coupling. This effect is normally known as

'injection pulling'. Proper shielding or isolation is therefore crucial for the proper operation of the entire transceiver system.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Mobile wireless communication applications are fast becoming a part of our daily lives. Their global market potential has been the continuous driving force for the improvements in the performance of these products, for example, better coverage, higher data rate, longer battery life, smaller size, and also lower cost. To meet these goals, researchers are focusing on implementing a single chip transceiver in the standard complementary metal oxide semiconductor (CMOS) or silicon germanium (SiGe) technology. The single chip solution will have both the digital signal processing circuits and the radio frequency front-end all integrated on the same chip. There is a wide range of applications specific RF chips. It is not possible to design a RF chip to cater for all the different applications. Furthermore, with the ever growing popularity of system-on-chip (SOC), radio frequency (RF) integrated circuit is facing more and more challenges to meet the demands of various wireless applications. To contain the scope of the effort, we have focus on two main challenges.

The first challenge is faced by mobile wireless communication devices. As stated, more and more companies are focusing on SOC solutions for their products. The mobile wireless communication applications based on silicon technologies can largely increase the integration density of RF module, base-band and digital signal processing (DSP) modules, etc. Therefore, with so many different power hungry modules packed into a single device, the battery life is placed under sever strain. There are many widely used frequency range of personal mobile wireless communication applications just lying in low gigahertz range, such as 900 MHz of global system for mobile communication (GSM) system, 1.8 GHz of digital communication system (DCS) system and 2.4 GHz for both Bluetooth technology

and IEEE 802.11.b/g [1] standard. As a result for such demand for mobility, to extend the battery life, low power circuits are becoming more and more popular.

To circumvent this problem, at the circuit level, the use of CMOS technology calls for a re-thinking of the traditional RF design method that relies heavily on the operation of MOS transistors in the saturation region which translates to a higher current consumption, to achieve targeted specifications. The first portion of this research focused primarily on the design of a fully-integrated weak inversion LNA using CMOS technology. In the receive path, the first block encountered is the LNA, performance of this block is therefore critical to ensure proper operation of the receiver. Its goal is to provide gain to the weak RF signals received with minimum noise contribution. Both specifications are being met with the MOS transistors biased in the saturation region. Unlike traditional LNA designs in strong inversion mode, where the design procedures are well established, the design of CMOS weak inversion LNA is still very much in its infancy stage. The design of a CMOS subthreshold LNA presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good linearity, good input and output matching and unconditional stability while reducing the power consumption through biasing conditions. The lack of high quality passive components, insufficient study or models of MOS transistors operating in the weak inversion region and the inadequate modeling of the noise sources of the transistor further complicate the design process.

The second portion of this research targets on the high bandwidth and linearity requirements of certain wireless applications. Higher bandwidth and data rate enable information intensive signals being transmitted and received, this is extremely true for wireless video streaming or high speed data transfer. To achieve the desired transmission speed is both a system as well as circuit subject. From the system point, modulation scheme adopted as well as frequency planning takes precedence. However it is vital to make use of existing available technology standards and protocols. Wide bandwidth circuits involve frequency switching capability; however, it is difficult to keep a constant power gain ratio across the frequency band. Power gain tolerance issues must be addressed. On top of the wide bandwidth requirement, RF circuit blocks are required to meet the linearity

specifications as well. Popular modulation scheme for high data throughput includes frequency division multiplexing (OFDM), quadrature amplitude modulation (QAM) and quadrature amplitude shift keying (QPSK). These schemes require highly linear circuits for operation, which would be discussed further in the later chapters. In light of the shortfalls of the CMOS process, a high performance but slightly more expensive SIGE process has to be adopted instead. A high linearity mixer, buffer and pre-amplifier were designed to meet the transmission specifications of such a wireless application.

1.2 OBJECTIVES

The objectives of this project are summarized as follows:

- (i) To study and understand the various mechanisms which degrade the performance of MOS transistor when biased in the subthreshold region;
- (ii) To study and review suitable amplifiers topologies of CMOS LNA biased in the weak inversion;
- (iii) To study and review performance specific SIGE process;
- (iv) To review suitable transmitter architectures and various topologies for high linearity bipolar junction transistors (BJT) mixers and PAs
- (v) To design, simulate, layout, fabricate and measure some RF front-end circuits such as LNAs, mixers and PAs.

1.3 MAJOR CONTRIBUTIONS OF THE THESIS

The major contributions of this thesis are broadly presented in the following sub-sections:

- (i) In this project, a simple and novel push pull amplifier design was selected for the design of the LNA. It makes use of current re-use concept to boost the gain of the LNA, as the gain of the MOS transistors biased in the subthreshold region is low.

(K.M. Lim *et al*, “A 2.4 GHz Subthreshold CMOS Low Noise Amplifier”, *Microwave and Optical Letters*, Vol. 49, Pg 743-744, Feb 2007)

- (ii) A highly linear mixer, buffer and PA were designed and integrated for a high performance wireless transmitter using SIGE process. Digital controlled varactor tank circuits were used to fulfill the bandwidth requirements.

1.4 ORGANIZATION OF THE THESIS

This thesis is organized into 6 chapters. Chapter 1 presents the motivation of this research work. It also defines the objectives of the project and highlights the major contributions of the thesis.

Chapter 2 provides a comprehensive literature review of silicon-based transistors as well as silicon passive devices. Various loss mechanisms pertaining to passive devices are discussed as well.

Chapter 3 focuses on the high frequency system parameters, the different specifications and derivations of system level performance benchmarks. A brief overall system level design is also introduced.

Chapter 4 concentrates on the design and simulation of a low power LNA, with focus on biasing the transistors in the weak inversion region to improve power consumption. Overall performance is tabulated and compared.

Chapter 5 verifies the integrated performance of a high bandwidth and highly linear transmitter using the SIGE process. The transmitter making use of non constant envelope modulation scheme is designed, fabricated and packaged, from block level. Testing is performed on a custom flame retardant 4 (FR4) board. Performance is tabulated and compared.

Finally, Chapter 6 summarizes the results of this work and recommends a few promising areas for future research.

CHAPTER 2

TECHNOLOGY REVIEW

Transistors are the basic building blocks of any RF circuit blocks. In this section, we shall focus on two main types of transistors, the bipolar junction transistor (BJT) and the metal oxide semiconductor (MOS) transistor. Both these technologies are very popular process in the industry today, with each technology having its own advantages and disadvantages. For each type of transistor, we briefly introduced their device physics, DC characteristics, high frequency response and their noise contributions. Passive inductors and capacitors, forming tuned loads for RF circuits, are essential building blocks and will be briefly reviewed.

2.1 BIPLOAR JUNCTION TRANSISTORS

BJT are composed of two PN junctions placed back to back, forming a three terminal electronic device which regulates current flow [2]. Figure 2-1 shows a cross-sectional view of a typical BJT structure used in integrated circuits. BJT can be further subdivided into NPN transistors and PNP transistors. It comprises of a heavily doped (N^+) emitter region, a lighter doped (N^-) collector region and a superseding (P) base region. Electrical contact to the base region is made through the N^+ buried layer, the N^- layer and the N^+ contact enhancement region. Isolation from other devices in the circuit is provided by the insulating silicon dioxide layer (SiO_2) layer and the p-type substrate. The corresponding symbol representation is shown in Figure 2-2.

Figure 2-1: Cross-sectional view of an NPN BJT

Under normal operating condition, the emitter-base junction is forward biased while the collector-base junction is reversed biased. In such a configuration, electron carriers for the NPN transistor are injected into the base due to the voltage drive at the emitter junction. The movement of electrons are caused by a combination of both drift and diffusion forces. These electrons move through the base, due to the reverse bias at this junction, the electrons are swept into the collector junction, giving rise to current flow. The current, originating in the emitter is predominately controlled by the voltage across the emitter-base junction and accounts for this structure being an active device.

Figure 2-2 : Symbol and sign conventions for (a) NPN transistor; (b) PNP transistor

2.1.1 LARGE SIGNAL MODEL

A relatively simple, but yet adequate large signal model for the BJT is the Ebers-Moll model [3]. It describes the transistor current in terms of the two PN junctions with their respective voltage across the junctions. In the forward active region, where the base emitter junction is forward biased and the base-collector junction is reversed biased, the relationship can be expressed by equations (2.1), (2.2) and (2.3).

$$I_c = \frac{qAD_n n_{po}}{W_B} \exp \frac{V_{BE}}{V_T} \quad (2.1)$$

$$= I_s \exp \frac{V_{BE}}{V_T} \quad (2.2)$$

Where

$$I_s = \frac{qAD_n n_{po}}{W_B} \quad (2.3)$$

Saturation current (I_s), a constant, is used to describe the transfer characteristic. From analysis, the collector current (I_c) and the base current (I_B) are both proportional to the forward current gain (β_F), shown in equation (2.4).

$$I_B = \frac{I_c}{\beta_F} \quad (2.4)$$

Other operating regions include the saturation and reverse active region, however such regions are usually avoided in analog and RF circuits due to low gain. A graphically representation for equation (2.2) is depicted by Figure 2-3. From the figure, one can deduce by operating in the active region, the output resistance is infinite.

Figure 2-3 : I_C versus V_{CE}

Practically the output resistance is not infinite, actual performance shows that I_c does change with respect to V_{BE} . This phenomenon is called the ‘Early effect’. Therefore a more accurate large signal equation is shown by equation (2.5).

$$I_C = I_S \left(1 + \frac{V_{CE}}{V_A} \right) \exp \frac{V_{BE}}{V_T} \quad (2.5)$$

2.1.2 SMALL SIGNAL MODEL

In most applications, the magnitudes of the input signals in a circuit are small compare to the bias voltages and currents. Therefore linear circuit models can be used to determine the circuit response to the small signals. The advantage of doing so is that now a linear circuit is analyzed instead of a nonlinear circuit.

Figure 2-4 : BJT Small Signal Model

Figure 2-4 shows the common small signal model of the BJT operating in the forward active region. It consists of both DC and RF frequency components. Transconductance (g_m) is defined as the ratio of the change in collector current to the change in base voltage, governed by the equations (2.6) and (2.7). It is used to express the performance of transistors. In general, the larger the g_m for a device, the greater the gain it is capable of delivering, when all other factors are held constant.

$$g_m = \frac{\partial I_C}{\partial V_{BE}} \quad (2.6)$$

Rewriting

$$\Delta I_C = g_m \Delta V_{BE} \quad (2.7)$$

Substituting equation (2.5) into (2.7) to get (2.8).

$$\begin{aligned} g_m &= \frac{\partial}{\partial V_{BE}} I_s \exp \frac{V_{BE}}{V_T} \\ &= \frac{I_s}{V_T} \exp \frac{V_{BE}}{V_T} \\ &= \frac{I_C}{V_T} \\ &= \frac{qI_C}{kT} \end{aligned} \quad (2.8)$$

Other critical components depicted in the small signal model include the small signal base resistance (r_{Π}). Resistor (r_o) is used to characterize ‘Early effect’ which results in the BJT having a finite resistance at the output. Due to operation and inherent material physics, would form capacitance across terminals. These capacitances limit the high frequency performance of the BJT. Base emitter capacitance is represented by c_{Π} and base collector capacitance is shown by c_u .

2.1.3 FREQUENCY RESPONSE

As mentioned in the previous section, the capacitances limit the frequency response of the transistor. This is critical when we are attempting to use the transistors in high frequency circuits. The frequency capability, transition frequency (f_T), is often specified in practice by determining the frequency where the magnitude of the short circuit common emitter current gain falls to unity. Figure 2-5 shows the small signal equivalent circuit for the calculation of f_T .

Figure 2-5 : Small Signal Model for Calculation of f_T

Applying Kirchoff's current law (KCL) and Kirchoff's voltage (KVL), we can express f_T by equation (2.9).

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{\pi} + C_u} \quad (2.9)$$

2.1.4 NOISE SOURCES

When the BJT is operating in the active region, the movement of minority carriers generates noise sources. i_c would give rise to shot noise and can be represented by a shot noise generator represented by $\overline{i_c^2}$ from collector to emitter in the small signal equivalent circuit of Figure 2-6 [4].

Figure 2-6 : Noise Sources of BJT

Since recombination process occurs in base, it gives rise to shot noise generators. On top of it another source of noise source known as flicker noise, which is generated due to process defects and crystal traps, is lumped together. The base resistor (r_b) is a physical resistor and thus have thermal noise. The collector resistor (r_c) does exhibits thermal noise; however, since it is connected to a high impedance noise, this noise source is generally swamped and can be neglected. The resistors r_{π} and r_o are fictitious resistors that are used for modeling. They do not generate thermal noise. The full small signal equivalent circuit including all the noises for the BJT is shown in Figure 2-6. Since they arise from separate, individual physical mechanisms, all the noise sources are independent of each other and have mean square values. The noise sources describe above can be presented by the following equations (2.10), (2.11) and (2.12), where Δf refers to the frequency of interest.

$$\overline{v_b^2} = 4kTr_b\Delta f \quad (2.10)$$

$$\overline{i_c^2} = 2qI_c\Delta f \quad (2.11)$$

$$i_b^2 = \underbrace{2qI_B\Delta f}_{\text{Shot noise}} + \underbrace{K \frac{I_B^n}{f}\Delta f}_{\text{Flicker noise}} ; \text{where } n \text{ is a constant, } 1 < n < 2 \quad (2.12)$$

2.2 METAL OXIDE SEMICONDUCTOR TRANSISTOR

Figure 2-7 : Cross Sectional View of Typical NMOS Transistor

Figure 2-7 depicts the cross-sectional view of a NMOS transistor [5]. The transistor is fabricated on a p-type substrate. Two heavily doped n-type regions, labeled n^+ source and n^+ drain, are created into the substrate to serve as source and drain terminals of the transistor. An extremely good electrical insulator, SiO_2 is grown as a thin layer on the surface of the substrate, covering the area between the drain and source regions. A strip of poly-silicon is deposited on top of the oxide layer to form the gate electrode terminal of the transistor. Metal contacts are dropped into source, drain and substrate, otherwise known as the body. This would therefore form the four terminals of a transistor: the gate terminal (G), the source terminal (S), the drain terminal (D), and the body terminal (B).

With the source terminal grounded, a positive voltage is applied to the gate terminal. This positive gate voltage would cause holes in the positively charged substrate to be repelled from the region of the substrate under the gate, forming a

depletion region. On the other hand, as the positive charges are repelled from the depletion region, electrons are attracted to the positive gate voltage. The value of gate-to-source voltage (v_{GS}) at which sufficient number of electrons is attracted to the gate to form a conducting channel is called the threshold voltage (v_{TH}). Lastly by applying a positive potential between the drain and the source, current flows through an induced channel commonly known as drain current (i_D). This induced channel is commonly known as the inversion layer.

2.2.1 LARGE SIGNAL MODEL

MOS equations can be derived by calculating the amount of charge in the channel at each point, and integrating such as expression from the drain-to-source, commonly called the charge sheet model [5]. Equations (2.13), (2.14) and (2.15) are the equations for the NMOS transistor in the saturation, linear and weak inversion states, respectively. Note the equations used are simplified, ignoring secondary MOS transistor's effects. However, these equations are enough to provide good insight and rough hand calculations. Note MOS transistors suffer from 'Early effect' as well, and would be taken into consideration by more detailed equations.

$$i_D = \frac{\mu_n C_{ox}}{2} \frac{w}{l} (v_{GS} - v_{TH})^2; v_{GS} > v_{TH} \text{ \& } v_{DS} > v_{GS} - v_{TH}; \text{Saturation} \quad (2.13)$$

$$i_D = \mu_n C_{ox} \frac{w}{l} [(v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2}]; v_{GS} > v_{TH}, v_{DS} < v_{GS} - v_{TH}; \text{Linear} \quad (2.14)$$

$$i_D \approx i_0 \frac{w}{l} e^{\left(\frac{v_{GS} - v_{TH}}{nV_T}\right)}; v_{GS} < v_{TH}, v_{DS} > v_{GS} - v_{TH}; \text{WeakInversion} \quad (2.15)$$

2.2.2 SMALL SIGNAL MODEL

When the magnitude of the input signal is small as compared to the bias conditions, we can generally view the transistor linearly. Figure 2-8 shows the small signal representation of the MOS transistor.

Figure 2-8 : Small Signal Model of MOS Transistors

Notice that subtle differences between the small signal model of the BJT as that of the small signal model of the MOS transistor. The gain of the MOS transistor is expressed similarly to that of the BJT through its g_m representation. However, for the MOS transistor is using the i_D over v_{GS} . Since we are only interested in the saturation and weak inversion region, the gain of the MOS transistor in the two regions can be expressed simply by the following equations.

$$g_m = \frac{i_D}{v_{GS}} = \mu_n C_{ox} \frac{w}{l} (v_{GS} - v_{TH}) \quad (2.16)$$

$$g_m = \frac{1}{n V_T} i_o \frac{w}{l} e^{\left(\frac{v_{GS} - v_{TH}}{n V_T} \right)} \approx \frac{i_D}{n V_T} \quad (2.17)$$

2.2.3 FREQUENCY RESPONSE

As with the BJT transistors, the frequency response of the MOS transistors is hampered by the inherent parasitic capacitance. The small signal model of the

MOS transistors with parasitic capacitance components are shown in Figure 2-9. Again f_T is used to characteristic the high frequency performance of the transistor, is shown to be governed by equation (2.18).

$$f_T = \frac{g_m}{(c_{GS} + c_{GD})} \quad (2.18)$$

Figure 2-9 : Small Signal Model with Parasitic Capacitance

2.2.4 NOISE SOURCES

The inversion channel under the gate is modulated by v_{GS} , allows i_D to flow, acts as a resistive channel [6]. This resistive channel exhibits thermal noise. As current flows beneath the gate oxide, any defects in the gate oxide would lead to trapping and releasing of electrons, giving rise to flicker noise. The thermal and flicker noise components are lumped together and can be represented by the noise current generator $\overline{i_d^2}$. Another source of noise in the MOS transistor is caused by the gate current and can be represented by shot noise denoted by $\overline{i_g^2}$. Shot noise can be computed using equation (2.19). Since that are two components in the drain current generator, equation (2.20) is made up of the two independent noise sources. Figure 2-10 shows the small signal model of MOS transistor with noise sources, [7].

$$\overline{i_g^2} = 2qI_G \Delta f \quad (2.19)$$

$$\overline{i_d^2} = \underbrace{4kT\left(\frac{2}{3}g_m\right)\Delta f}_{\text{Thermal noise}} + \underbrace{K\frac{I_D^n}{f}\Delta f}_{\text{Flicker noise}}; \text{where } n \text{ is a constant, } 1 < n < 2 \quad (2.20)$$

Figure 2-10 : Small Signal Model of MOS Transistor with Noise Sources

2.3 PASSIVE COMPONENTS

RFIC designs are characterized by the use of many passive components. Their advantages include low power consumption and good linearity. Integrated inductors and capacitors are fundamental components in RF applications. In-depth understanding of the characteristics of integrated passive components is essential to use them effectively. In this chapter, the design and characteristics of inductors and capacitors will be presented.

2.3.1 INDUCTORS

The inductor is a key element in determining the performance of an LC tank. The on-chip spiral inductor is constructed based on the lithography, where the geometry of coils is well-controlled. There are several topologies of the spiral inductor available, for example, square, hexagonal and circular. The square spiral inductor has been widely used for its easy layout. However, it suffers from higher

insertion loss compared with the circular spiral inductor as well as current crowding effect. Figure 2-11 shows the various geometrical layout of a spiral inductor. The inductor is usually routed using the top metal layer and connected to the other terminal using the underpass metal layer, usually one metal layer lower. The design parameters of an inductor are given by the number of turns (n), the metal width (w), the metal to metal spacing (s), the inner diameter (ID) and the outer diameter (OD). The latter parameters are shown.

Figure 2-11 : a)Square b)Octagonal c)Hexagonal d)Circular layout pattern

The lumped element model is widely used to simulate the performance of an inductor. A typical π -equivalent model [8], [9] is shown in Figure 2-12.

Figure 2-12 : The lump element model of an on-chip inductor

It consists of nine components, where L is the total inductance produced by the metal winding and mutual coupling, R_L is the total loss of the inductor, C_{OX} is the capacitance between inductor and substrate, R_{si} and C_{si} are the parasitic resistance and capacitance of the substrate. The efficiency of an inductor is defined by the quality factor (Q), from [10] is represented by equation (2.21).

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy lost per cycle}} \quad (2.21)$$

Equation (2.22) defines the energy stored in the inductor and provides an indication of how much energy is lost as it is being transferred. The energy stored is actually the sum of the average magnetic and electric energies. However, for a silicon spiral inductor, only the energy stored in the magnetic field is of interest. Any energy stored in the form of electric field by the parasitic capacitance is counterproductive. Hence, Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies:

$$Q = 2\pi \frac{\text{Peak Magnetic Energy} - \text{Peak Electric Energy}}{\text{Energy Loss Per Cycle}} \quad (2.22)$$

In most standard processing technology, the quality factor of the on-chip inductor is generally lower than that of the capacitor. Therefore it is critical to know some of the inductor operating parenthesis for some quick hand calculation. There are two ways of obtaining the parameters stipulated, one of them is to refer to the modeling data provided by the foundry. The other is to run a simulation, and infer from the high frequency results. With the help of simple computer aided design (CAD) tools, perform the simple setup as shown in Figure 2-13 and run an S-parameter simulation.

Figure 2-13 : Simulation Setup

Converting the S-parameter to y-parameters data, the important inductor's parameters can be calculated using Table 2-1. The data can be tabulated graphically as shown by Figure 2-14.

Table 2-1 : Calculation using Y-parameters

$L = \frac{\text{imag}\left(\frac{1}{Y_{11}}\right)}{2\pi f}$	$Y_{11} = \frac{((1 - S_{11}) * (1 + S_{22}) + (S_{12} * S_{21}))}{((1 + S_{11}) * (1 + S_{22}) - (S_{12} * S_{21}))}$
$Q = \frac{\text{imag}(Y_{11})}{\text{real}(Y_{11})}$	$Y_{11} = \frac{((1 - S_{11}) * (1 + S_{22}) + (S_{12} * S_{21}))}{((1 + S_{11}) * (1 + S_{22}) - (S_{12} * S_{21}))}$
$r = \text{real}\left(-\frac{1}{Y_{12}}\right)$	$Y_{12} = \frac{-2 * S_{12}}{((1 + S_{11}) * (1 + S_{22}) - (S_{12} * S_{21}))}$

a) Inductance versus Frequency

b) Q versus Frequency

c) Resistance versus Frequency

Figure 2-14 : Graphical Representation of Inductor's Parameters

2.3.2 CAPACITORS

Metal-insulator-metal (MIM) capacitor, have good linearity, high-quality factor, coupled with small temperature variations, plays an important role in RF circuits. The design of a MIM capacitor will be described in this section.

Figure 2-15 : a)MIM Capacitor b)Equivalent Model

Figure 2-15(a) shows a MIM capacitor, and Figure 2-15(b) shows its corresponding model. The model is similar to that of [11], with some slight variation for substrate parasitic. In the model, C_P is the device capacitance and is given by equation (2.23).

$$C_P = \epsilon_{ox} \frac{WL}{H} \quad (2.23)$$

ϵ_{ox} is the permittivity of silicon oxide. W and L are the width and length of the capacitor's plate respectively while H is the separation between the plates. Parasitic capacitance between the bottom plate and the substrate is denoted by C_{ox} . Substrate parasitic capacitance and resistance are represented by C_{si} and R_{si} . They are usually quite significant and account for almost 20% of the total capacitance. R_S is the series resistance, and L_S is the lead inductance. Dielectric losses are represented by R_P . The parasitic resistance if left unchecked could become a significant source of thermal noise [12]. One disadvantage of MIM capacitor is the smaller unit capacitance as compared to a MOS capacitor or poly insulator poly capacitor. Figure 2-16 show the characteristics of the MIM capacitor over frequency.

a) Capacitance versus Frequency

Figure 2-16 : Simulation Results of MIM Capacitors

2.4 CONCLUSION

In this chapter, the basic active and passive components are reviewed. The characteristics of transistors are presented while their high frequency behaviors are analyzed. Finally, passive components are presented and briefly explained.

CHAPTER 3

RF CIRCUIT PERFORMANCE PARAMETERS

An RF transceiver typically consists of three main sections, receive, transmit and frequency synthesizer or phase lock loop (PLL) system. For the receiver as the name implies is to receive desired signals from a potentially dense spectral environment, provide an amplification of the signal to a level suitable for the demodulator to recover the transmitted information. In this section, the various performance measures will be defined, and their effects on the requirements of the LNA will also be discussed subsequently. The transmitter is used to amplify the modulated signal from the base-band to a higher power level so as to counter the various loss mechanisms associated during free space transmission. An important consideration which the transmitter must fulfill is the transmitted output spectrum mask. Due to limited available frequencies in the industrial scientific medical (ISM) band, the transmitted spectrum has certain criteria to meet the specifications from the Federal Communications Commission (FCC).

3.1 SYSTEM ANALYSIS

The ability of the transceiver to carry out these tasks is typically quantified by performance measures such as sensitivity, noise figure (NF), linearity, and dynamic range [13], [14].

3.1.1 SENSITIVITY

RF signals tend to be attenuated through the transmission medium resulting in weaker signals at the input of the receiver. The capability of detecting and amplify

these weak signals by the receiver is known as the sensitivity of the receiver. Sensitivity can be expressed in terms of the minimum detectable signal (MDS) level. The MDS and noise at the antenna is amplified by the receiver chain, receiver internal noise is coupled onto the signal, to produces some acceptable level of signal to noise ratio (SNR) at the demodulator output. MDS is given by equations (3.1) and (3.2). Where $P_{n,\min}$ represents MDS, P_{RS} is the thermal noise and B refers to the bandwidth of interest.

$$P_{n,\min} \text{ dBm} = P_{RS} \text{ dBm/Hz} + NF \text{ dB} + SNR_{\min} \text{ dB} + 10 \log B \quad (3.1)$$

$$P_{n,\min} = -174 \text{ dBm/Hz} + NF + SNR_{\min} + 10 \log B \quad (3.2)$$

Assuming conjugate matching at the input and at room temperature of 290K, thermal noise can be approximated to be -174 dBm/Hz , by taking log after the multiplication of Boltzman's constant (k) by temperature (T) in Kelvin. NF is the cascaded noise figure of the entire system in decibels (dB) before the demodulator. Bandwidth (B), the effective noise bandwidth, is used in SNR calculation of the demodulator. This is usually set to the application's channel bandwidth. $SNR_{\min}$ is the minimum SNR ratio required by the demodulator to maintain a certain level of fidelity. This value is typically related to the bit error rate (BER) and selected modulation scheme [15]. Taking the summation of the first three terms is the total integrated noise of the system and is sometimes referred to the '*Noise floor*'.

3.1.2 NOISE FIGURE

From the equations from the previous section, the noise performance of the system defines the sensitivity of the receiver by limiting the lowest RF power that can be detected. There are many sources of noise that can affect to the quality of the signal. The noise factor (F) is a figure of merit defining the amount of noise added by a system. The *IEEE* definition of noise factor is the ratio of output noise to

available input noise power due to the source [16]. The noise factor expressed in dB is usually referred to as NF governed by (3.3).

$$F = \frac{SNR_{in}}{SNR_{out}} NF; NF = 10\log(F) \quad (3.3)$$

For simplicity, we shall only consider thermal noise and use the receiver for illustration. Thermal noise is a function of random movement of particles in the medium. As shown in equation (3.4), thermal noise power is dependent on the signal bandwidth and temperature of the medium. Naturally, the noise power increase with temperature and bandwidth. Therefore for a cascading receiver network, the noise figure can be expressed by equation (3.5). Equation (3.5) is called the '*Friis equation*'. It indicates the amount of noise contribution from each stage when individual blocks are hooked up to form the system.

$$P = k_B T \Delta f \quad (3.4)$$

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (3.5)$$

It is very critical to note that the formula is only valid and useful when the input signal is at the threshold of sensitivity. When the input signal is large, the inherent noise power of the input signal dominates the thermal noise of the receiver, and eliminates the effect of thermal noise from the receiver. Therefore the quality of the received signal is no longer limited by the receiver noise but by the quality of the transmitter it originated. Vice versa, when the input signal is weak and its noise level is below the thermal floor, the receiver thermal noise would severely corrupt the SNR ratio as the signal propagates through the system. It correlates well with the equations presented. Figure 3-1 shows the effect of thermal noise as the signal propagates through the receiver.

Figure 3-1 : Impact of the noise figure as it moves down the chain a) High Power Incoming Signal b) Low Power Incoming Signal

3.1.3 GAIN COMPRESSION

An ideal amplifier is able to continuously amplify the input signal regardless of its signal strength. However, RF systems are non-linear in nature, the output is unable to track the input after a certain operating range due to nonlinearities. This phenomenon is known as harmonic distortion. This operating range defines the saturation point of the RF system. At the point where the input signal is amplified by an amount 1 dB less than the small signal gain, the 1 dB compression point (P_{1dB}) has been reached. A rapid decrease in gain will be experienced after the 1 dB compression point is reached.

Figure 3-2 : P_{1dB} Compression Point

Figure 3-2 shows the gain compression due to the nonlinearities in the system causing the power gain to deviate from its idealized curve. Therefore, for linear operation, systems have to be biased a couple of dB below its compression point.

3.1.4 THIRD ORDER INTERCEPT

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are harmonics of the input frequencies. This mixing of two signals is known as inter-modulation, specifically the third order inter-modulation product (IM3) is commonly used to characterize the linearity of the system. The intersection of the IM3 line and linearly amplified signal gives rise to the third order intercept point (IP_3). Equation (3.6) describes the generation of the IM3 for the nonlinear behavior. Another way of looking at the advantage of IP_3 , whereas the IM3 products are dependent on the signal power and cannot be used independently to describe performance, the intercept points are indeed independent parameters that can be used to compare linearity of different circuits. From the IM3 the input IP_3 can be derived to reach equation (3.7) [13].

$$y(t) = \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \quad (3.6)$$

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} \quad (3.7)$$

This relationship dictates a '3:1' slope for the input IP_3 point. Output IP_3 point can be easily calculated by multiplying the gain of the block to the appropriate input IP_3 , shown in (3.8).

$$A_{IP3,out} = \alpha_1 A_{IP3} \quad (3.8)$$

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \dots + \frac{G_1 G_2 \dots G_n}{IIP3_n} \quad (3.9)$$

Figure 3-3 shows the result of a two tone power sweep with the fundamental signal and its inter-modulation products plotted as a function of input RF power. The intercept points are extrapolated using the plotted data. For a link budget analysis, these numbers can be lineup, equation (3.9), to determine the impact of the individual blocks on the overall linearity of the overall system. One easier approach to understand the formula is to realize that the overall linearity is dependent on the linearity of the limiting block.

Figure 3-3 : Graphical Representation of IP3 Concept

3.1.5 DYNAMIC RANGE

Another system parameter used to characteristic the performance of RF systems is known as the dynamic range. Dynamic range is defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the system is able to produce reasonable signal quality. It is most similar to the rail to rail specifications used to describe analog circuits. The upper end of the dynamic range is limited by the nonlinear behavior of the system, which causes inter-modulation products. The lower end of the dynamic range is defined by the sensitivity of the system. The difference between these two values would give the spurious free dynamic range (*SFDR*) of the system. The *SFDR* can be easily calculated using (3.10). On a separate note, the *SFDR* represents the maximum relative level of interferers that a system can tolerate while producing an acceptable signal quality from a smallest input level the system is able to detect.

$$SFDR = IP_3 - MDS \quad (3.10)$$

3.2 SYSTEM ARCHITECTURE

A thorough system analysis is essential in designing any RF system. The system design helps to define specifications and scope of the RF system as well as each individual cascaded building block. Frequency planning, design partitioning and interfacing between blocks are determined. The resulting specifications for the functional RF blocks then form the basis for the RF circuit designer to develop the transistor level implementation. Although the specifications of cascading RF blocks could have infinite combinations, system architectures are still broadly classified into three major architectures, superheterodyne [17], [18], direct conversion or homodyne [19] and lastly the low immediate frequency (IF) structure. A short description for each of them will be given.

3.2.1 SUPERHETERODYNE

The superheterodyne architecture is probably the oldest and most widely used architecture until recent times. Figure 3-4 shows the superheterodyne architecture, the entire input RF spectrum is down converted to a fixed IF using a tunable oscillator. The image is further attenuated to an acceptable level by using external image reject filter before the down conversion block. The channel selection is normally done using an IF filters following the down conversion. The choice of IF is critical in determining the selectivity and sensitivity of the front-end system

Figure 3-4 : Superheterodyne Architecture

Superheterodyne are viewed as the most reliable receiver topology with excellent selectivity and sensitivity, attained by proper selection of IF and filters. However, the cost penalty in order to attain adequate performance is through the use of external high Q band pass filters for image rejection and channel selection. All these tradeoffs make it difficult to achieve integration of a transceiver on a single chip.

3.2.2 DIRECT CONVERSION

The motivation for higher level integration and eliminating off chip components has led to zero IF receiver architecture. Figure 3-5 shows the block diagram for such a system.

Figure 3-5 : Direct Conversion System

For this topology, the RF spectrum is directly down converted to DC and channel selection is performed by the high roll off low pass filter. Since the incoming RF frequency is the same as that of the local oscillator (LO) frequency, image problem is eliminated thus avoiding the use of external high Q image rejection filters. Eliminating off chip components makes this architecture attractive for integration. Moreover single stage mixing helps to reduce reciprocal mixing. Overall, this architecture is excellent at saving current consumption, cost and silicon area. However, it has problems caused by time varying DC offset, LO leakage and flicker noise can hamper the proper detection of information. This architecture is also more prone to second order inter-modulation products (IM2).

3.2.3 LOW IF

The concept of on-chip band pass filtering has led to the generation of another architecture which avoids some the pitfalls of the zero IF system. Instead of direct mixing down to DC level, the IF is at a low frequency typically ranging from a few hundred kHz to a few MHz [20], [21]. As usual the RF spectrum is first amplified by the LNA and filter by a complex filter to produce quadrature signals. The quadrature down conversion is performed using a complex mixer. The complex mixer only mixes the positive RF frequencies with the negative LO frequency and vice versa achieving active image rejection. Advantages include high level of on-chip integration yet avoiding the pitfalls of the direct conversion architecture. It also provides a high degree of flexibility in the processing of signals. However due

to of inherent device mismatches and processing defects, it is unable to generate symmetrical I and Q signals. Therefore image rejection of the low IF system is limited to about 40 dB. Figure 3-6 illustrates the low IF architecture. Power consumption is also higher from using the complex mixer.

Figure 3-6 : Low IF Architecture

3.3 CONCLUSION

In this chapter, a brief overview of concepts and performance attributes of RF circuits are presented. The major RF receiver system architectures are discussed briefly. Irregardless of the architecture employed, there still exists numerous variations to construct the entire system, and not limited to the block diagrams presented. Lastly, although receiver systems were emphasis, the same concepts could be generically applied to transmitter systems with certain changes in concepts.

CHAPTER 4

DESIGN OF WEAK INVERSION LNA

LNA have been the basic building blocks in modern communication receiver systems. The operating frequency of the LNA is dependent on the desired application operation frequency. The function of the LNA is to receiver weak RF signals, having suffered high attenuation, after propagation of the transmission medium air. The SNR ratio at the receiver is already low; therefore it is important that the LNA does not degrade the SNR any further. It basically states that the LNA should have very low or no inherent noise. On top of the low noise criteria, the LNA should also achieve high gain, this helps to lower the noise contribution from subsequent cascaded blocks along the receive chain. Both low noise and high gain conditions fulfills the '*Friis equation*' stated in the previous chapter. Other significant considerations would be power consumption and linearity of the LNA. In today's consumers markets, more and more mobile wireless applications are introduced, with every new application packing more functions and features. This has shown to be a strain on the mobile battery pack. The linearity of the LNA determines the highest power RF input signal it could receive before saturation. It helps to define the dynamic range of the receive RF signal but is still subjected to system considerations and performance of subsequent blocks.

4.1 DESIGN CONSIDERATIONS

In this section we shall present our proposed LNA and the concepts behind the design. From our literature review, we know that we must be able to increase the gain of the amplifier without any increase in i_D . One popular technique for low voltage low power design is the current reuse technique. It is based on a simple ideology which uses the same DC current as bias for another device. An excellent

example of a circuit that uses the current reuse technique is the simple push-pull amplifier. For a push-pull amplifier, it consists of two transistors working in tandem with one another, a PMOS transistor on the top and a NMOS transistor in the bottom. Figure 4-1 shows a simple push-pull amplifier.

Figure 4-1 : A Simple Push-Pull Amplifier

The operation of the push-pull amplifier is as follows. When the RF signal cycle is positive, transistor NMOS M_1 is 'ON', therefore the output would track the positive cycle of the input signal as shown. When the RF signal cycle is negative, PMOS M_2 is 'ON', and the output starts tracking the negative cycle of the input instead. Note that both transistors are operating with one common bias current i_D . However, the above structure would suffer from cross over distortion. This occurs during switching or when both transistors are 'ON' simultaneously. For this period of time there would be no signal at the output. A more realistic example depicting the operation of the push-pull is shown in Figure 4-2.

Figure 4-2 : Push-Pull Amplifier showing Cross-over Distortion

A common solution to the cross-over problem can be resolved by leaving transistors M_1 and M_2 'ON'. This would get rid of the switching cycle causing the problem. As always this is done at the expense of current. On the other hand, as we are attempting to operate the transistors in subthreshold region, current consumption which is already low, would not pose a problem.

The proposed amplifier is shown in Figure 4-3 with main core of the LNA make up of a push-pull amplifier. The usage of a push-pull amplifier as a LNA is not new [22], [23], but has yet been demonstrated in subthreshold operation.

Figure 4-3 : Schematic of Proposed LNA

Performing the small signal analysis in the push pull core, the gain for this structure is higher than that of a single CS LNA. The small signal model of the push pull amplifier with the output load is shown in Figure 4-4. Equation (4.1) can be derived by taking KCL at node V_{IN} . Subsequent current equations (4.2) and (4.3) can be derived by KCL at their respective nodes, V_1 and V_2 . Assuming infinite output resistance, certain terms can be ignored. The output node, KCL at node V_{OUT} , is described by equation (4.4). Substituting equations (4.2) into (4.3) can arrive at equation (4.5). Further simplifying can be performed by combining equation (4.1) and (4.5) to get (4.6). Through substituting equations (4.4) into (4.6) arrive at (4.7). Lastly allowing $I_o = \frac{V_{OUT}}{Z_L}$ and $V_{gs(p)} = V_{gs(n)} = V_{IN}$, we can reach (4.8).

$$I_{in} = \{[V_{in} - V_2] * j\omega C_{gd(N)}\} + \{V_{in} * j\omega C_{gs(N)}\} + \{[V_{in} - V_1] * j\omega C_{gd(P)}\} + \{V_{in} * j\omega C_{gs(P)}\} \quad (4.1)$$

$$[V_{IN} - V_1] * j\omega C_{gd(P)} = g_{m(N)} * V_{gs(P)} + \frac{V_1}{R_{o(p)}} + [V_1 - V_2] * j\omega C_L + \frac{V_1 - V_{OUT}}{j\omega L_1} \quad (4.2)$$

$$[V_{IN} - V_2] * j\omega C_{gd(N)} + [V_1 - V_2] * j\omega C_L + \frac{V_{OUT} - V_2}{j\omega L_2} = g_{m(n)} * V_{gs(n)} + \frac{V_2}{R_{o(n)}} \quad (4.3)$$

$$\frac{[V_1 - V_{OUT}]}{j\omega L_1} + I_o = \frac{[V_{OUT} - V_2]}{j\omega L_2} \quad (4.4)$$

$$[V_1 - V_2] * j\omega C_{gd(N)} + [V_{IN} - V_1] * j\omega C_{gd(P)} - g_{m(P)} * V_{gs(P)} - \frac{V_1 - V_{OUT}}{j\omega L_1} + \frac{V_{OUT} - V_2}{j\omega L_2} = g_{m(N)} * V_{gs(N)} \quad (4.5)$$

$$V_{IN} * j\omega C_{gs(P)} + V_{IN} * j\omega C_{gs(N)} + g_{m(P)} * V_{gs(P)} + g_{m(N)} * V_{gs(N)} = \frac{V_{OUT} - V_2}{j\omega L_2} - \frac{V_1 - V_{OUT}}{j\omega L_1} \quad (4.6)$$

$$V_{IN} * j\omega C_{gs(P)} + V_{IN} * j\omega C_{gs(N)} + g_{m(P)} * V_{gs(P)} + g_{m(N)} * V_{gs(N)} = I_o \quad (4.7)$$

$$Gain = \frac{V_{OUT}}{V_{IN}} = \underbrace{[g_{m(P)} + g_{m(N)}]}_{\text{Current Reuse}} + j\omega [C_{gs(N)} + C_{gs(P)}] * Z_L \quad (4.8)$$

Figure 4-4 : Small Signal Analysis of the Push Pull Amplifier with Load

The current reuse scheme can be clearly seen, with the PMOS and NMOS transistor are both feeding from the same bias current. With higher g_m and employing current reuse technique, the gain of the push-pull amplifier is therefore higher as compared with a single CS transistor operating in the weak inversion

region, while drawing smaller current. Advantages of the push-pull amplifier include better linearity and reverse isolation as reported in literature [24].

4.2 TRANSISTOR SELECTION

Transistor selection is the first and most important step in LNA design. The transistor should be selected with the most important LNA design trade-off in mind. Ideally, the transistor should exhibit a high gain, have a low noise figure, and offer a high IP_3 performance at the lowest possible current consumption, while preserving relatively easy matching at the frequency of operation [25]. For simple hand calculations, transistor sizes can be selected as follows. Reproducing the current and gain equations of MOSFETs operating in the weak inversion region.

$$i_D \approx i_O \frac{w}{l} e^{\left(\frac{V_{GS} - V_{TH}}{nV_T} \right)} \quad (4.9)$$

$$g_m = \frac{\delta i_D}{\delta V_{GS}} \approx \frac{i_D}{nV_T} \quad (4.10)$$

Therefore the aspect ratio must be determined from these equations. Rearranging (4.9), we are able to get (4.11) or (4.12).

$$V_{GS} = V_{TH} - n \cdot V_T \cdot \ln \left(\frac{i_O}{i_D} \right) \quad (4.11)$$

or

$$V_{GS} = V_{TH} - n \cdot V_T \cdot \ln \left[\frac{\mu_n C_{ox} \cdot n V_T^2}{\frac{i_D}{(W/L)}} \right] \quad (4.12)$$

Therefore we can determine the sizes of the transistor from (4.12). With i_D and V_{GS} as constraints, we are able to work out the sizing of transistors. With an

operating voltage of 1.0 V, we can first arbitrarily determine the operating v_{GS} , by setting v_{GS} (NMOS) to 0.5 V and v_{GS} (PMOS) to 0.5 V. Next we can easily find out the transistor's size ratio W/L from the targeted power consumption. Due to the difference in carrier velocity, between electrons and holes, the size of the PMOS transistor was selected to be three times bigger and fined tuned through simulation.

A 0.18 μm CMOS process is selected for the implementation of the LNA. Before the transistor to be used in the LNA can be selected, transistors of various aspect-ratios and biases need to be characterized to understand how the performance of the MOSFET varies with its aspect ratio and bias in the weak inversion region. Devices with aspect-ratios of 100 $\mu\text{m}/0.18 \mu\text{m}$, 150 $\mu\text{m}/0.18 \mu\text{m}$, 200 $\mu\text{m}/0.18 \mu\text{m}$, 250 $\mu\text{m}/0.18 \mu\text{m}$, and 300 $\mu\text{m}/0.18 \mu\text{m}$ are simulated for their gain, linearity and noise performance for a bias current of 0.3 mA to 1.0 mA. The characterization is performed using Cadence SpectreS with the BSIM3V3 model. DC analysis has been performed to obtain v_{th} for the various sizes, as shown in Appendix A. The S-parameter simulation is performed to obtain the forward gain (S_{21}) and noise parameters of the MOSFET, and the swept periodic steady-state (SPSS) simulation is performed to obtain the IIP_3 of the MOSFET. Another figure of merit introduced is g_m/i_D , gain normalized to current. This figure shows the gain versus current, or DC power consumption. From simulation results, by sweeping g_m/i_D against v_{GS} , we obtained the following curve displayed. From this, we can easily conclude to get the most gain for the least current consumed, we should bias the transistors in the weak inversion region. Figure 4-5 shows the characteristics of the 200 $\mu\text{m}/0.18 \mu\text{m}$ MOSFETs as it is swept from weak inversion to moderate inversion. Characteristics of the other transistors sizes can be found in Appendix A.

Figure 4-5 : Length 0.18um Width 200um a) Small Signal Gain b) Noise Figure c) Linearity d) g_m/I_D

From Figure 4-5 and Appendix A, it is seen that the minimum noise figure ($NF_{\min}$) of the MOSFET improves as V_{GS} increases. However, the noise figure curves shows that by avoiding basing the MOSFET in deep subthreshold region, reasonable NF could still be obtained. Another important consideration to take into account is the S_{21} , the feed-forward gain follows the trend set by the NF, with higher gain obtain through higher current consumption. An important observation shows that the IIP_3 of the MOSFET shows u-shaped curve. The linearity tends to be very good at extremely low bias conditions. It gets poorer as V_{GS} increases, and at moderate weak inversion, the linearity improves again. Linearity and gain have an inverse relationship. Therefore smaller transistor sizes tend to have better linearity and g_m/i_D , but the gain and NF is poorer and may be unsuitable for some operation. Therefore, the design approach is to select the transistor with reasonable g_m/i_D to ensure sufficient gain with respect to current consumption. At the same time, the MOSFET is able to exhibit good linearity and noise figure. For this reason a transistor size of 200 μm seems a suitable candidate for initial design phase.

4.3 DESIGN FOR TESTING

For RF measurements vector network analyzer (VNA) are 50 ohms (Ω) based equipments, therefore designs must take this consideration when design for testing. Figure 4-6 shows the actual on-wafer testing conditions with measurement equipment.

Figure 4-6 : Equipment Testbench

Once the core transistors are chosen, the rest is just a matter of designing the input and output matching networks. For a low noise and high gain amplifier, the design of the input matching network plays a critical role in determining the noise and the input return loss performance of the LNA [26], [27].

Input matching can follow that of inductive source degeneration. Taking the main core of the LNA as a black box, we can determine the input impedance of the push-pull LNA shown in Figure 4-7. Ignoring the parasitic resistance R_g and parasitic capacitance C_{DG} , the input impedance looking in is purely capacitive. We can see that ignoring R_g is a valid assumption, as R_g is already small and could be further reduced through good layout practices. The total capacitance look in can be derived to (4.13). Effectively, capacitors C_2 and C_3 , serves as DC chokes therefore their flexible in values can help to reduce the size of inductor L_s .

$$C_{total} = (C_3 // C_{gs1}) + (C_2 // C_{gs2}) \quad (4.13)$$

Figure 4-7 : Input Impedance of Core LNA

Traditional LNA designs make use of inductive source degeneration. As we will see, the proliferation of this architecture is no accident; it offers the possibility of achieving the best noise performance of any architecture. It was first proposed in [28], [29]. Figure 4-8 shows a typical common cascoded LNA with inductive source degeneration.

Figure 4-8 : Cascoded Inductor Source Degeneration LNA

In the figure, biasing circuitries are omitted for clarity. It consists of two transistors connected in differential configurations, transistor M_1 is connected CS while transistor M_2 is CG. M_1 is the first high gain stage. M_2 plays an important role in reducing miller effect. Miller effect has a highly undesirable effect on RF performance, due to the high capacitive load it presents to the input.

Figure 4-9 shows the small signal analysis of for the initial stage of the LNA. To derive the formulae shown by (4.16), we have to compute the Z_{in} of the LNA. Working out KCL at node 1 to get equation (4.14), and KVL around loop 1, equation (4.15). Through substitution, the two equations can be derived to (4.16). Intuitively, there is a real part and imaginary part to (4.16). The imaginary part can be tuned out while making the real part to 50Ω for matching purpose.

Figure 4-9 : Small Signal Analysis

Inductors L_s , L_g serve as impedance matching network, the effect of these inductors can be shown to be (4.16).

$$i_s = v_{GS} j\omega C_{GS} + g_m v_{GS} \quad (4.14)$$

$$v_{IN} = v_{GS} j\omega C_{GS} j\omega L_g + v_{GS} + i_s j\omega L_s \quad (4.15)$$

Where $i_{IN} = v_{GS} j\omega C_{GS}$

$$\begin{aligned} Z_{in} &= s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}} \right) L_s \\ &\approx \omega_T L_s \end{aligned} \quad (4.16)$$

The C_{total} from (4.13) can be substituted into C_{gs} of (4.16) to determine the value of L_s and L_g . Therefore with the variation, the final equation can be worked out to be (4.17). Another distinct advantage is that the inductor sizes can be reduced significantly with the increase of the input impedance looking into the amplifier.

$$\begin{aligned} Z_{in} &= s(L_s + L_g) + \frac{1}{sC_{total}} + \left(\frac{g_{m(n)} + g_{m(p)}}{C_{total}} \right) L_s \\ &\approx \omega_T L_s \end{aligned} \quad (4.17)$$

Output matching is completed by using a t-coil inductor load, it provides high gain as well as impedance matching to 50 Ω load of the bias tee. The principle of the t-coil load can be better explained through the illustration in Figure 4-10, taking the NMOS transistor as the conducting transistor, while the t-coil inductors and PMOS as the load. The load can be shown to act as a high impedance load as well as forming an impedance matching L-type network.

Figure 4-10 : T-Coil Load Output Matching

4.4 RESULTS

The push-pull LNA was designed using Chartered's 0.18 μm CMOS process. It is a six metal process. Inductors are fashioned using thick top metal for better performance. While MIM capacitors are fabricated using the two top most metals. Designed environment used is Cadence Virtuoso schematic capture with Spectre RF simulator. The layout was drawn in Cadence layout editor. The LNA occupies a die area measuring 1050 μm x 723 μm , the layout is shown in Figure 4-11.

Figure 4-11 : Layout of Proposed LNA

The following figures show the simulated results. Figure 4-12 shows the input return loss of the push-pull amplifier. As stated the matching can be first calculated and fine tuned through simulation.

Figure 4-12 : S11 Input Matching

Figure 4-13 shows the output return loss.

Figure 4-13 : S22 Output Matching

Figure 4-14 shows the power gain of the amplifier. The push pull amplifier achieves a gain of 9.8 dB at 2.4 GHz.

Figure 4-14 : S21 Power Gain

Noise figure is 3.6 dB at frequency of interest as shown in Figure 4-15, which is comparable to those that have been reported for subthreshold LNA circuits. As described earlier in Chapter 2, this is mainly caused by the transistors being noisier

in the weak inversion region and the inherent more noise contribution by two transistors in the first stage.

Figure 4-15 : Noise Figure

Another specification we look at is the linearity of the amplifier. Linearity can be measured by two means. The first is the 1 dB compression point and the other is the 3rd inter-modulation intercept. The 1 dB compression curve is shown in Figure 4-17 and IP_3 curve in Figure 4-17 respectively.

Due to the smaller power gain, the linearity of the amplifier is therefore improved showing better inter-modulation as well. A brief performance comparison between subthreshold LNAs was also performed and the results tabulated in Table 4-1. A new figure of merit, normalized IIP_3 to power consumption is used to characterize

the LNAs performance. Due to the fact that IP_3 ranges from negative to positive values, a normalization factor is applied. It is then divided by the power consumption to obtain the ratio. A high ratio would only imply that the LNA has achieved good blocking while drawing low power, two very important merits of an LNA.

Table 4-1 : Performance comparisons of this work and recently reported 2.4 GHz 0.18 μ m CMOS LNAs

	Supply (V)	Current (mA)	Gain (dB)	NF (dB)	IP3 (dBm)	(Nom. IP3)/Power (dBm/W)
Vidojkovic V [30]	3.6	4.0	17.0	2.25	0.5	0.73
L.H Lu [31]	1.8	6.5	10.1	2.9	-5.0	0.43
J. Long [32]	1.2	2.3	12.9	0.75	14.4	8.84
W Hu [34]	1.2	6.5	15.6	2.78	1.19	1.43
Z.Y Luo [35]	1.0	13.0	23.0	3.8	-9.1	0.07
*Perumana [35]	1.0	0.26	13.6	4.6	7.2	66.15
This work	1.0	0.65	9.8	3.6	-2.7	11.23

* 1GHz operating frequency

4.5 CONCLUSION

The design difficulties of weak inversion LNA are investigated. A subthreshold LNA has been successfully implemented for 2.4 GHz operation. The proposed LNA achieves reasonable gain and noise figure with very high linearity, while consuming low power, in comparison to the performance of the existing designs.

CHAPTER 5

DESIGN OF 802.11 OVER COAX

TRANSMITTER

In recent years, the growth of home and office has been phenomenal. Wireless applications targeted at the mass consumers market are taking place at a frantic pace. A new exciting application, riding on the popular IEEE 802.11 standard, also known as WIFI wireless standard is currently actively researched. The WIFI standard has emerged very popular and is now the de-facto standard of every home and office networking. The standard has shown significant improvement in bandwidth from the IEEE 802.11b to IEEE 802.11g from 11 Mbps to 54 Mbps. With 54 Mbps, it is possible to transmit video signal. Therefore a hybrid 802.11 over coax [36] is proposed. Since the coax cables are already in place, it would make sense to make use of existing technology to allow service providers to provide high bandwidth media contents to the user's domain. Upon reaching the user's domain, the data rich information can be converted for wireless transmission.

Figure 5-1 shows a brief overview of the IEEE 802.11 over coax system. The hybrid system would allow high bandwidth applications to be transmitted wirelessly throughout the existing home, making use of the existing coax system and reducing the usage of any new protocol and standards, riding on the widely accepted WIFI standard.

Figure 5-1 : Hybrid IEEE 802.11 over Coax System

To handle the high throughput, high bandwidth modulation schemes must be employed. Due to the modulation scheme, a high linearity high bandwidth transmitter is required to satisfy the specifications. In the traditional sense the transmitter usually up converts before the signal is transmitted through the medium, however in this application, the transmitter functions slightly differently, it would down convert the 2.4 GHz WIFI signal to a 1.0 GHz signal for transmission to the service providers.

5.1 DESIGN SPECIFICATIONS

The goal was to design an RF transmitter for bridging between two standards, the IEEE 802.11 and the existing coax medium. A WIFI front-end is used to detect 2.4 GHz signal, the modulated signal is then down converted to 1.0 GHz and amplified for coax transmission. Input frequency has an operating range from 2412 MHz to 2485 MHz. Individual channel has a bandwidth of 20.0 MHz. Upper side band injection was preferred, this results in a LO frequency of 3400 MHz to 3560 MHz. Output frequency occupies a range from 915 MHz to 1148 MHz, bandwidth is considerably large compared to center frequency. Wideband matching circuit

techniques are required to fulfilled output matching specifications. As mentioned earlier, due to nature of data and modulation scheme, required linearity for overall system is higher. Correspondingly to achieve the high linearity specifications, current consumption has to be higher.

To cover the required bandwidth, it is difficult to maintain the gain level throughout. Some form of frequency band switching technique must be employed. Furthermore when switching across the different frequency bands, gain variation must also be controlled. Output noise floor is set at -141 dBm, with respect to theoretical noise floor of -174 dBm, it leaves an achievable noise figure of 33 dB across the frequency. Having a mixer in the RF path, give rises to RF mixing. RF mixing creates spurs at other frequencies, sufficient attenuation of these spurs is therefore crucial for proper operation. The amount of attenuation is taken with respect to the reference output signal therefore the units for spurs rejection are in dBc. Table 5-1 tabulates the entire transmitter RF specifications in detail.

Table 5-1 : Transmitter Design Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
FRF	RF Frequency Range	Center of 20 MHz Channel	2412		2485	MHz
FIF	IF Frequency Range	Center of 20 MHz Channel	915		1148	MHz
FLO	LO Tuning Range		3400		3560	MHz
CIMP	Output/Input Characteristic Impedance			100		Ω
POUT_MAX	Maximum RF output power for full performance	Balun Load 100 Ω :50 Ω ; Balun Termination :50 Ω		1		dBm
POUT_MIN	Minimum RF output power for full performance	Balun Load 100 Ω :50 Ω ; Balun Termination :50 Ω		-15		dBm
TX_GAIN	TX Path Gain	Variation across Process, V_{DD} & Temperature Conditions		12.0		dB
P1dB	TX Path 1 dB compression point			9.0		dBm
OIP3	Tx Path Output 3rd Order Intercept Point	2 tones @ -6dBm		19.0		dBm
S11	Input Return Loss	Includes external Balun		12.0		dB
BGAINV	Gain Variation over RF Band			± 1.0		dB
CGAINV	Gain Variation over channel	BW= ± 20 MHz		± 0.5		dB
LOFT	LO Feed Through			-42.0		dBc
UPFT	Upper Side Band Rejection @ 5.8 GHz			-40		dBc
SPOUT	Level of Spurs at Output	Frequency Band @50~850 MHz		-40.0		dBc
OSP	Other Spurs at Output	Other Frequencies		-40.0		dBc
S22	Output return Loss	Includes external Balun		12.0		dB
CCONS	Current Consumption			50.0		mA

5.2 TRANSMITTER ARCHITECTURE

The superheterodyne architecture was selected for its robustness and practicability. LO signal is selected for high side injection so that the image frequency is far away and could easily be filtered out by the resonant tank circuits doing away with expensive off-chip surface acoustic wave (SAW) filters. Due to the high linearity requirements, careful system planning is required. The mixer is designed to contribute minimum gain, instead gain is mostly contributed by the pre-amplifier (PA), this helps tremendously in reducing the linearity specifications of the PA during integration of the entire system. Figure 5-2 shows the block diagram of the required transmitter.

The transmitter for this project included the down-converting mixer and driver amplifier. To alleviate the problem of ‘*injection pulling*’ output power is set at 1dBm. Better noise rejection can be achieved from the use of differential signals. However the drawback would be need for single to differential converters, baluns are usually used for this purpose. However on-chip baluns have inferior RF performance and are silicon area intensive. Therefore off-chip baluns are used instead. The insertion loss from the input and output baluns cannot be ignored and can be as high as 2.0 dB [37], [38]. Bandwidth requirement presents a big strain at the output of the transmitter, and requires external off chip matching network to meet the required specifications.

Figure 5-2 : Block Diagram for the Transmitter

Between the mixer and PA, a buffer is inserted to provide better isolation between the LO signal and high powered RF signal.

5.3 BIASING CIRCUIT

As the test chip would be packaged, biasing circuits are required to reduce package pin count. Our aim is provide a compensated biasing circuit for consistent circuit

performance across process, voltage and temperature variation. Control bits are worked into the biasing circuits for additional freedom in tweaking of performance after fabrication. Control bits are supply though 8 bit registers and can be controlled externally through serial parallel interface (SPI) port.

Figure 5-3 : NTAT Current

The biasing circuit is shown in Figure 5-3. It shows only the main core with start up circuit. The start up circuit core would ensure that the node n in the biasing circuit does not remain at 0.0 V, instead it is pulled up to V_{DD} before settling at the stable operating voltage. Formation of the temperature sensitive current occurs in the closed loop formed between Q_1 and Q_2 and the R_1 [3], [39]. Bootstrapping the biasing circuit has advantage of the current source being highly supply independent.

5.4 MIXERS

Down conversion is carried by the mixer, making use of the double balanced gilbert cell structure [40], [41]. The gilbert cell structure consists of two main blocks, the g_m stage and the switch quad stage. The g_m stage as its name implies is where the active mixer amplifies the input high frequency signal, it is also the most important stage to design to in order to obtain good overall linearity for the mixer. The switch quad stage is where mixing of the RF and LO signals takes place to generate the IF signals. Traditionally gilbert mixer structure, the g_m stage is constructed using a differential pair in a common emitter configuration, with a tail current source for high gain mixers. However the tail current tends to limit the linearity of the mixer, therefore a pseudo-differential g_m is preferred [42], [43]. Another variation is to bias the transistors in a common base configuration to improve the linearity of the mixer. In the common base configuration, with proper biasing and transistor and resistor size selection, it is possible to obtain good input matching with respect to the source impedance, doing away with one stage of matching network.

Figure 5-4 : Pseudo-Differential Mixer

Figure 5-4 shows the schematic of the pseudo differential pair. Biasing circuitries are omitted for clarity. DC decoupling capacitors C_3 and C_4 are used to block DC and low frequency components, allowing desired frequency band to pass through. The first stage, the differential g_m cell consists of Q_1 , Q_2 , R_1 and R_2 . Switching function is performed Q_3 , Q_4 , Q_5 and Q_6 . LC loads are used for high gain and band-pass function. Inductor L_1 and capacitors C_1 are tuned center frequency of 1.0 GHz.

Frequency band selection is performed using the varactor banks working in tandem with the LC tank circuit. To tune to the frequencies at the lower end of the working spectrum, additional capacitance are switched on and vice versa for the frequency on the other end. However the additional capacitors add additional parasitic resistance causing the gain for the lower frequencies to be lower. Since gain variation across different frequency bands must be properly controlled. Intended gain attenuation at higher frequency bands are performed by drawing slightly longer interconnects. The longer interconnect add additional parasitic resistance

which help to attenuate the signals for higher frequencies. This helps to even the gain across the different bands.

5.5 BUFFERS

A differential buffer has been designed to provide better isolation. Besides improving leakage, it helps to prevent the strong RF signals from affecting the mixer. The most traditional common collector configuration is used. It has good buffering capabilities with slight signal attenuation yet drawing reasonable power.

Figure 5-5 : Differential Common Collector Buffer

Q_1 and Q_2 acts as the common collector transistors providing high input impedance to the preceding block while subsequent stage sees a low impedance load. Active loads are used through Q_3 and Q_4 .

5.6 PRE-AMPLIFIERS

The design considerations are numerous and varied, however one significant consideration is still the modulation scheme adopted. There are numerous modulation schemes to choose from, each with individual pros and cons. Associated with the modulation schemes are its envelope modulation. Envelope modulation are divided into constant envelope modulation and non-constant envelope modulation. General rule of thumb, is non-constant envelope modulation requires a highly linear PA for operation [44]. The effect of using a non-linear on a non-constant envelope modulation would cause spectral re-growth [45]. Figure 5-6 a) illustrates effect of constant envelope and non-constant envelope modulation with some of the associated modulation schemes. Figure 5-6 b) illustrates the concept of spectral re-growth, when a non-linear PA is used on a modulation scheme with non-constant envelope modulation.

Figure 5-6 : a) Envelop Modulation b) Non-constant Envelop Modulation c) Spectral Regrowth

Therefore a class A PA is selected for the transmitter [46], [47]. However tradeoff for a highly linear class A PA is that the PA is less efficient and therefore consumes higher current. A cascode class A PA was design for the intended application as

shown in Figure 5-7. The main gain transistors consist of Q_1 and Q_2 . Cascode transistors Q_3 and Q_4 were used not so much in gain improvement but to provide better isolation and reduce *miller* effect. Degen resistors R_1 and R_2 were used to improve the linearity. The use of output LC tanks, L_1 , L_2 , C_1 , and C_2 help to achieve high gain and provide band-pass filtering capability.

Figure 5-7 : Differential Class A PA

5.7 FABRICATION & RESULTS

5.7.1 LAYOUT & PACKAGING

The transmitter was fabricated using IBM's RF 0.35 μm SIGE process. Layout was drawn using Cadence Virtuoso Layout Editor. Isolation is crucial to the successful operation of the chip. Separate power and ground were used for different blocks. The biasing circuit, mixer and buffer share a common V_{DD} because they do not

generated high amplitude signals, while the PA has its own V_{DD} supply pin because it generates high amplitude signals. The ground pins were separated for every individual blocks to have better isolation and minimize coupling between blocks. Ground pins of RF blocks were also double-down bonded to reduce package lead parasitic as illustrate in Figure 5-8.

Figure 5-8 : Double Down Bond

On-chip decoupling capacitors were used for each V_{DD} . In addition, individual block was surrounded by a ring of substrate contacts. Key RF transistors were also surrounded by a ring substrate contacts. The layout of individual RF block has to be laid out in perfect symmetry to take advantage of the differential architecture. Key RF traces such as pad connections and inter-block connections were routed using thick top metal and kept as short as possible. The whole process calls for careful floor planning and layout. IC pads were all protected using double diode for electronic static discharge (ESD) protection. ESD protection circuits were designed to withstand a zap test of 1.5 kV human body model (HBM) and 0.5 kV charge device model (CDM).

The fabricated chip was packaged using a 32-pin quad flat no-lead (QFN) IC package. Figure 5-9 shows the lead frame of such a package. High frequency electrical models of the package lead must be included in top level simulation to consider packaging effects.

Figure 5-9 : QFN Lead Frame

Table 5-2 shows the material parameters and properties. Using a three dimensional modeling simulator, the package model could be modeled for any of the pins. The packaged model used in the top level simulation is shown in Figure 5-10. Testing and measurement were carried out on a custom built FR4 board.

Table 5-2 : Packaging Materials Parameters and Properties

Item	Dimension	Material	Material Property
Package Size	5.0 <i>mm</i> * 5.0 <i>mm</i>	X	X
Die Size	3.6 <i>mm</i> * 3.6 <i>mm</i>	X	X
Lead Thickness	0.20 <i>mm</i>	C7025	2.9E7 S/M
Lead Width	0.25 <i>mm</i>	X	X
Lead Pitch	0.50 <i>mm</i>	X	X
PCB Thickness	0.50 <i>mm</i>	FR4	4.4 (Dielectric const.)
Body Thickness	0.50 <i>mm</i>	Compound	4.1 (Dielectric const.)
Wire Diameter	0.020 <i>mm</i> (0.8 <i>mil</i>)	Gold	4.35E7 S/M

Figure 5-10 : Package Model

Figure 5-11: Microphotograph of the Transmitter

Figure 5-12 : Custom Built Evaluation Board

Figure 5-11 shows the microphotograph of the de-capsulated die. Figure 5-12 shows the custom built PCB for testing, measurement and evaluation of the designed transmitter. A more detailed representation can be found in Appendix B.

5.7.2 LOSS MECHANISM

The various loss associated with the measurement setup have to be calibrated. Losses can occur from the connecting cables, PCB trace loss, balun loss and SMA connectors. The following figures illustrate the measured loss associated with each component.

Figure 5-13 : Cable Loss Calibrated at 1.0 GHz

Figure 5-14 : Cable Loss Calibrated at 2.4 GHz

Figure 5-15 : Loss Measured from SMA Connector, 15 cm PCB 50 Ω Transmission Trace & Balun 1.0 GHz

Figure 5-16 : Loss Measured from SMA Connector, 15 cm PCB 50 Ω Transmission Trace & Balun 2.4 GHz

From Figure 5-13 and Figure 5-14, cable loss at 1.0 GHz is measured to be 0.5 dB while cable loss at 2.4 GHz is measured to be 1.15 dB. From Figure 5-15, loss of SMA connectors, PCB trace and balun at 1.0 GHz is measured to be 3.93 dBm, subtracting the input and output cable loss, actual loss at the output of the transmitter is calculated to be 2.93 dB. Figure 5-16 shows the measured loss at the input of the transmitter 7.19 dBm, subtraction of cable loss would put the loss at 4.89 dB. The PCB trace is fabricated on the same FR4 board, with its own set of SMA connectors. The PCB trace length used in measurement is 15.0 cm long actual trace width is almost half the length, therefore the actual board loss can be divided by two for accurate results. With the losses calibrated, any gain measurement can be compensated by input cable at 2.4 GHz 1.15 dB, input SMA connector, PCB trace and 2.4 GHz balun 2.45 dB, output cable at 1.0 GHz 0.5 dB, input SMA connector, PCB trace and 1.0 GHz balun 1.47 dB. Adding the total loss, a gain of 6.0 dB is compensated to actual measured results.

5.7.3 RESULTS

Figures 5-17 and 5-18 show the measured reflection S-parameters at the input and output of the packaged transmitter. The input reflection S-parameter is labeled as S_{11} and the output s-parameter is labeled as S_{22} . The results indicate a S_{11} better than -15.0 dB and a worst case of S_{22} better than -11.7 dB across the required bandwidth. Due to the larger bandwidth strain at the output S_{22} is unable to achieve as unable to achieve excellent matching as S_{11} , however it is still good enough for proper functioning and operation of the transmitter.

Figure 5-17 : S-parameter S_{11}

Figure 5-18 : S-parameter S_{22}

Next, we take a look at the measured gain of the transmitter. Figure 5-19 a) shows the input signal, power level set at -10.0 dBm at a frequency of 2.45 GHz. Figure 5-19 b) shows the output signal, power level set at -5.4 dBm at a frequency of 1.0 GHz. With losses compensated the transmitter achieved a gain of 10.6 dB. The transmitter has achieved excellent spur rejection at the lower frequency range -56.0

dBc shown in Figure 5-20. LO leakage at 3.4 GHz and spurs at the higher end of the frequency spectrum is also well attenuated -43.0 dBc illustrated in Figure 5-21.

Figure 5-19 : a) Input Signal Power set at -10.0 dBm b) Measured Output Signal Power -5.4 dBm

Figure 5-20 : Spurs Rejection between 50.0MHz to 1.5GHz

Figure 5-21 : LO Leakage and High Frequency Spurs

Figure 5-22 a) shows the two tone input signal while b) measures the inter-modulation products at the output of the transmitter. The resulting OIP₃ can be calculated using in-house software.

Figure 5-22 : OIP₃ Measurement Result a) Two Tone Input Signal Injected b) Two Tone Output Signal Measured c) Calculation of IP₃

The transmitter inter-modulation measurement with dual tone 2.44 GHz and 2.46 GHz at -10 dBm, gain of 10.6 dB with an inter-modulation product of -58.0 dBc, resulting OIP₃ of 18.56 dBm. Lastly, Figure 5-23 shows the gain response as the varactor bank in the mixer switches. The varactor bank is controlled by three SPI bits giving nine different control modes. During measurement, it was shown that out of the nine different control settings, three of the control settings are sufficient to cover the desired bandwidth. Therefore, only the three controls setting are shown in Figure 5-23. From Figure 5-23, the gain response of the transmitter has a gain variation of 2.1 dB from 900 MHz to 1100 MHz.

Figure 5-23 : Gain Variation of Varactor Bank Switching

Table 5-3 tabulates the desired specifications against measurement results. Post simulation results were already over designed. Therefore, the measurement results track the desired specifications very closely. Table 5-5 compares the performance of similar transmitters found in the literature. As transmitter designs have varied specifications and different architectures, focus is targeted at SIGE process transmitters operating at the 2.4 GHz frequency band with high data rate modulation schemes.

Table 5-3 : Specification versus Measured Results

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Measured	Unit
FRF	RF Frequency Range	Center of 20 MHz Channel	2412		2485	NA	MHz
FIF	IF Frequency Range	Center of 20 MHz Channel	915		1148	NA	MHz
FLO	LO Tuning Range		3400		3560	NA	MHz
CIMP	Output/Input Characteristic Impedance			100		NA	Ω
POUT_MAX	Maximum RF output power for full performance	Balun Load 100 Ω :50 Ω ; Balun Termination :50 Ω		1		0.6	dBm
POUT_MIN	Minimum RF output power for full performance	Balun Load 100 Ω :50 Ω ; Balun Termination :50 Ω		-15		0.6	dBm
TX_GAIN	TX Path Gain	Variation across Process, V_{DD} & Temperature Conditions		12.0		10.6	dB
PI1dB	TX Path 1 dB compression point			9.0		8.5	dBm
OIP3	Tx Path Output 3rd Order Intercept Point	2 tones @ -6dBm		19.0		18.5	dBm
S11	Input Return Loss	Includes external Balun		12.0		15	dB
BGAINV	Gain Variation over RF Band			± 1.0		± 1.05 dB	dB
CGAINV	Gain Variation over channel	BW= ± 20 MHz		± 0.5		± 0.5 dB	dB
LOFT	LO Feed Through			-42.0		-43	dBc
UPFT	Upper Side Band Rejection @ 5.8 GHz			-40		< -43.0	dBc
SPOUT	Level of Spurs at Output	Frequency Band @50~850 MHz		-40.0		< -56.0	dBc
OSP	Other Spurs at Output	Other Frequencies		-40.0		< -43.0	dBc
S22	Output return Loss	Includes external Balun		12.0		11.7	dB
CCONS	Current Consumption			50.0		54	mA

Table 5-4 : Performance Comparisons

	Supply (V)	Current (mA)	Gain (dB)	IP3 (dBm)	LO Rejection (dBc)	Output Power (dBm)
Charlon O. [48]	2.8	66.0	30.0 (<i>baseband+RF</i>)	15.0	35.0	-10.0
Locher M. [49]	2.8	135.0	75.0 (<i>baseband+RF</i>)	-9.0	30.0	1.0
Klepser B.U. [50]	3.0	155.0	23.0	NA	26.0	-9.0
*Jirou He [51]	1.8	40.0	12.0	17.7	50.0	0.0
This work	3.3	54.0	10.6	18.5	43.0	0.6

* CMOS process

5.8 CONCLUSION

In this chapter, a transmitter for a new exciting application is proposed. This transmitter was designed in IBM's 0.35 μm SIGE process. Testing is performed on packaged die with custom built PCB evaluation board. With performance mainly focus on current and linearity tradeoff, high linearity circuit techniques were employed in the design of the transmitter blocks. Measured results are able to tack required specifications closely.

CHAPTER 6

CONCLUSION & FUTURE WORK

6.1 CONCLUSION

This thesis describes a wide range of circuit blocks found in RF front-end circuits such as LNAs, mixers, PAs and isolation buffers. The ever growing field of wireless applications has a profound impact on our everyday life. Wireless networks allow us to sense, manage and communicate and are already embedded in the fabrics of our daily living environment. Such technology provides endless possibilities in a huge variety of application scenarios. RF engineers are required to understand a wide range of skill set, from analog design to data communications to microwave techniques to device physics. The fundamentals of the CMOS and BJTs transistors have been reviewed. The physical conditions and working principles of the different transistors were discussed. Large signal equations were introduced with emphasis on the different operating regions followed by the small signal equations and models. Other RF devices, particularly the inductors and capacitors were discussed. These passive devices characteristics have a huge frequency correlation. Therefore it is critical to have some knowledge and understanding. Various RF system specifications were analyzed in detail. To have a good grasp of overall system performance and how the specifications can be translated into individual circuit block designs. From the overall system specifications, it is then important to select the system architecture. Different system architectures have their own pros and cons, it is important to realize the advantages and disadvantages of the different architectures and select the one that is best suited for the required application.

Widespread development of mobile wireless networks requires each node to consume less power for a long usage lifetime and low operational cost, for seamless integration into our physical environment. Power constraint is the most

challenging hurdle to overcome. This thesis has investigated the viability to operate the LNA in the weak inversion region, advantage being low power consumption. However, the other specifications of the LNA must still be reasonable to fulfill its role from the overall system point of view. A novel push-pull structure operating with the concept of current reuse is proposed. Emphasis was placed on testing with proper matching designed to interface with test equipment. The proposed LNA has shown to achieve an acceptable gain of 9.8 dB, and a good noise figure of 3.6 dB. With proper implementation of matching networks, S_{11} and S_{22} were able to achieve more than -11.0 dB and -21.0 dB respectively. Linearity was able to reach -11.6 dBm for P_{1dB} and IIP_3 of -2.7 dBm. The current consumption was limited to 650 μ A.

Lastly, a transmitter system was designed for an application 802.11 over coax. Due to system requirement and modulation scheme, certain specifications are more essential for proper operation. Inter blocks interfacing to packaging effects to ESD protection must be considered. Off-chip components such as baluns must also be considered during simulation. Finally, proper test setup and de-embedding must be done to get accurate test results. The proposed TX has achieved an output power of 0.6 dBm, and a gain of 10.6 dB. S_{11} and S_{22} were able to achieve more than -15.0 dB and -11.7 dB respectively, P_{1dB} of 8.5 dBm and IIP_3 of 18.5 dBm while consuming 54 mA of current. Spurs and LO rejection were well controlled and shows good rejection of spurious signals.

6.2 FUTURE WORK

It is shown that high frequency operation is possible in the weak inversion region. However, very accurate subthreshold RF models are still found lacking. In-depth study and modeling of transistors device in the weak inversion region is essential. This technique could be extended to other RF circuit blocks such as mixers and voltage-control oscillators (VCO). With the entire RF front-end operating in the

micro-amperes (μA), it would be truly possible to achieve a micro-power transceiver operating at several giga-hertz.

For high throughput applications, more efficient PAs could be investigated. Currently, class A PA is used because it is highly linear. However, its drawback is poor efficiency, therefore more current is consumed. Several other liberalizing techniques for other classes of PAs could be studied and integrated effectively.

A phase lock loop (PLL) operating at a center LO frequency of 3.45 GHz could be designed and integrated with the transmitter system. With the integration, more system level measurement data such error vector magnitude (EVM), startup timing and turn around timing can be measured.

REFERENCES

- [1] ANSI/IEEE Std. 802.11
- [2] R.F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996
- [3] R. Paul Gray *et al*, *Analysis and Design of Analog Integrated Circuits*, 4th ed., John Wiley, 2001
- [4] A. van der Ziel, *Noise in Solid State Devices and Circuits*, New York: Wiley, 1986
- [5] Y. Tsividis, *Operation and Modeling of MOS Transistor*, 2nd ed., McGraw-Hill, 1999
- [6] A. Abidi, "High-frequency noise measurements on FET's with small dimensions," IEEE Transactions Electron Devices, Volume ED-33, November 1986, Pages(s):1801 - 1805.
- [7] G. Knoblinger, P. Klein, and M. Tiebout, "A new model for thermal channel noise of deep-submicron MOSFET's and its application in RF-CMOS design," IEEE Journal Solid-State Circuits, May 2001, Pages(s):831 - 837.
- [8] K.T. Christensen and A. Jorgensen, "Easy simulation and design of on-chip inductors in standard CMOS processes," IEEE Int. Symposium Circuits and Systems, Volume 4, 31 May-3 June 1998 Page(s):360 – 364.
- [9] A. Scuderi, T. Biondi, E. Ragonese and G. Palmisano, "A lumped scalable model for silicon integrated spiral inductors," IEEE Transactions Circuits and Systems, Volume 51, June 2004, Page(s):1203 - 1209
- [10] C. Patrick Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," IEEE Journal Solid State Circuits, Volume 33, May 1998, Page(s): 743-752.
- [11] J. N. Burghartz, M. Soyuer, and K. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," IEEE Transactions Microwave Theory Technology, Volume 44, Jan. 1996, Pages(s): 100-103.
- [12] J. Chang, "An Integrated 900 MHz Spread-Spectrum Wireless Receiver in 1- μ m CMOS and a Suspended Inductor Technique," Ph.D dissertation in Electrical Engineering. Los Angeles: University of California, 1998
- [13] B. Razavi, *RF Microelectronic*, Prentice-Hall, 1998
- [14] J.G. Proakis and M. Salehi, *Communications System Engineering*, Prentice-Hall, 1994
- [15] Hyun Seob Shin, Jai Hyung Park, Ji Hoon Kim and Hyung Joun Yoo, "System-level performance analysis and design of RF receiver for W-CDMA user equipment," Int. Conference Microwave and Millimeter Wave Technology, Sept. 2000, Page(s):319 – 322.
- [16] IRE Standards on Methods of Measuring noise in Linear Twoports, Proc. IRE, 1960, Pages(s) : 60-68.
- [17] S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," IEEE Communication Magazine, Volume 38, Nov. 2000, Page(s): 132-139.

- [18] M. Valkama and M. Renfors, "Advanced receiver architectures and I/Q signal processing," Int. Symposium Control, Communication and Signal Processing, 2004, Page(s): 71-74.
- [19] H. Tsurumi and T. Maeda, "Design study on a direct conversion receiver front-end for 280 MHz, 900 MHz, and 2.6 GHz band radio communication systems," IEEE Conference Vehicular Technology, May 1991, Page(s): 457 – 462.
- [20] B.J. Minnis and P.A. Moore, "A highly digitized multimode receiver architecture for 3G mobiles," IEEE Transactions Vehicular Technology, Volume 52, May 2003, Page(s):637 – 653.
- [21] Ho-Kwon Yoon and M. Ismail, "A fully-integrated CMOS RF front-end for Wi-Fi and Bluetooth," IEEE Northeast Workshop Circuit and Systems, June 2004, Page(s):357 – 360.
- [22] A. Karanicolas, "A 2.7V 900MHz CMOS LNA and Mixer," IEEE Journal Solid State Circuits, Volume 21, Dec. 1996 Page(s):1939 – 1944.
- [23] Chang Soek Lee, Min Gun Kim, Joe Jin Lee, Kwang Eui Pyun and Hyung Moo Park, "A low noise amplifier for a multi-band and multi-mode handset," IEEE Symposium Radio Frequency Integrated Circuits, June 1998, Page(s):47 – 50.
- [24] Kwyro Lee, I. Nam, Ickjin Kwon, J. Gil, Kwangseok Han, S. Park and Bo Ik Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," IEEE Transactions Electron Devices, Volume 52, July 2005 Page(s):1415 – 142.
- [25] J. Lucek, and R. Damen, "Designing an LNA for a CDMA Front-end," RF Design, Feb. 1999, Page(s): 20-30.
- [26] R. Soares, J. Graffeuil, and J. Obregon, Applications of GaAs MESFETs, Artech House, 1983.
- [27] Guillermo Gonzalez, Microwave Transister Amplifiers: Analysis and Design, 2nd ed., Prentice Hall, 1996.
- [28] K. R. Cioffi, "Monolithic L-band amplifiers operating at milliwatt and sub milliwatt DC power consumptions," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp., 1992, pp. 9-12.
- [29] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF front-end IC," IEEE Journal of Solid State Circuits, Volume 29, Mar. 1994 Page(s):350 – 355.
- [30] V. Vidojkovic, J. van der Tang, E. Hanssen, A. Leeuwenburgh and A. van Roermund, "Fully-integrated DECT/Bluetooth multi-band LNA in 0.18 μ m CMOS," Proceedings Int. Conference Circuits and Systems, Volume 1, May 2004, Pages(s):565 – 568.
- [31] L.H. Lu, H.H. Hsieh and Y.S. Wang, "A compact 2.4/5.2GHz CMOS dual-band low-noise amplifier," IEEE Microwave and Wireless Components Letters, Volume 15, October 2005, Pages(s):685 – 687.
- [32] J. Long and R.J. Weber, "A low voltage, low noise CMOS RF receiver front-end," Proceedings 17th Int. Conference on VLSI Design, 2004, Pages(s):393 – 397.
- [33] W. Hu, Y.W. Guo, Z.J. Qiu and L.X. Yang, "A 1.2V 2.4GHz 0.18 μ m CMOS low noise amplifier," IEEE Int. Conference Communications, Circuits and Systems, Volume 1, July 2002, Pages(s):470 - 473.

- [34] Z.Y. Luo, S.C Rustagi, M.F Li and L. Yong, "A IV, 2.4GHz fully integrated LNA using 0.18 μ m CMOS technology," Proceedings 5th Int. Conference ASIC, Volume 2, October 2003, Pages(s):1062 – 1065.
- [35] Perumana, B.G. Chakraborty, S. Chang-Ho Lee and J. Laskar, "A fully monolithic 260-/spl mu/W, 1-GHz subthreshold low noise amplifier," IEEE Microwave and Wireless Components Letters, Volume 15, June 2005 Page(s):428 – 430.
- [36] L. Ophir and Y. Bitran, "802.11 over coax - a hybrid coax-wireless home network using 802.11 technology," IEEE Conference Consumer Communications and Networking, Jan 2004, Page(s): 13-18.
- [37] HHM1520A2, Multilayer Balun Specifications, TDK Corp., Jun. 2007, Version. 4.0
- [38] HHM1523C1, Multilayer Balun Specifications, TDK Corp., Oct. 2003, Version. 1.0
- [39] M. Gunawan, G.C.M. Meijer, J. Fonderie and J.H. Huijsing, "A curvature-corrected low voltage bandgap," IEEE Journal Solid State Circuits, Volume 28, June 1993, Page(s): 667-670.
- [40] S. Chakraborty, S.K. Reynolds, T. Beukema, H. Ainspan and J. Laskar, "Architectural trade-offs for SiGe BiCMOS direct conversion receiver front-ends for IEEE802.11a," Symposium Gallium Arsenide Integrated Circuits 24th Annual Technical Digest, Oct. 2002, Page(s): 120-123.
- [41] C. Carta, R. Vogt and W. Bachtold, "A low-power SiGe-HBT active double-balanced mixer for compact integrated C-band wireless-LAN receivers," IEEE MTT-S Conference Microwave and Optoelectronics, Volume 3, Sept. 2003, Page(s): 20-23.
- [42] Domine Leenaerts *et al*, Circuit Design For RF Transceivers, Springer US, 2003.
- [43] F. Bahmani and E. Sánchez-Sinencio, "A highly linear pseudo-differential transconductance," European Solid-State Circuits Conference, Sep. 2004.
- [44] I. Hibon, C. Berland, D. Pache, M. Villegas, D. Belot and V. Le Goasoz, "Linear transmitter architecture using a 1-bit spl Sigma spl Delta," The European Conference Wireless Technology, Oct. 2005, Page(s): 321.
- [45] G.T. Zhou, "Analysis of spectral regrowth of weakly nonlinear power amplifiers," IEEE Communications Letters, Volume 4, Nov. 2000, Page(s): 357-359.
- [46] H. Thomas Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge University Press, 2004.
- [47] J.P. Comeau, J.M. Andrews and J.D. Cressler, "A Monolithic 24 GHz, 20 dBm, 14% PAE SiGe HBT Power Amplifier," 36th European Microwave Conference, Sept. 2006, Page(s): 419-422.
- [48] O. Charlon, M. Locher, H.A. Visser, D. Duperray, J. Chen, M. Judson, A.L. Landesman, C. Hritz, U. Kohlschuetter, Yifeng Zhang, C. Ramesh, A. Daanen, Minzhan Gao, S. Haas, V. Maheshwari, A. Bury, G. Nitsche, A. Wrzyszc, W. Redman-White, H. Bonakdar, Rachid El Waffaoui and M. Bracey, "A low-power high-performance SiGe BiCMOS 802.11a/b/g transceiver IC for cellular and bluetooth Co-existence applications," IEEE Journal Solid State Circuits, Volume 41, July 2006, Page(s):1503 -1512.

- [49] M. Locher, J. Kuenen, A. Daanen, H. Visser, B. Essink, P.P. Vervoort, O. Charlon, A. Landesman and U. Kohlschutter, "A low power, high performance SiGe BiCMOS 802.11e dual conversion transceiver IC," IEEE Symposium Mobile WiMAX, March 2007, Page(s):66–69.
- [50] B.U. Klepser, M. Punzenberger, T. Ruhlicke and M. Zannoth, "5-GHz and 2.4-GHz dual-band RF-transceiver for WLAN 802.11a/b/g applications," IEEE Symposium Radio Frequency Integrated Circuits, June 2003, Page(s): 37-40.
- [51] Jirou He, Xiaoping Gao, Weilun Shen, Xiaofeng Yi, Yumei Huang, and Zhiliang Hong, "A 2.4-GHz Fully CMOS Integrated Transmitter for 802.11b Wireless LAN," Int. Conference ASIC, Volume 1, Oct. 2005, Page(s): 381 – 384.

APPENDIX A

TRANSISTORS CHARACTERISTICS

V_{th} for Transistors Length 0.18 μm , Width 100 μm , 150 μm , 200 μm , 250 μm and 300 μm

Length 0.18um Width 100um a) Small Signal Gain b) Noise Figure c) Linearity d) g_m/I_D

Length 0.18 μ m Width 150 μ m a) Small Signal Gain b) Noise Figure c) Linearity d) g_m/I_D

Length 0.18um Width 250um a) Small Signal Gain b) Noise Figure c) Linearity d) g_m/I_D

Length 0.18um Width 300um a) Small Signal Gain b) Noise Figure c) Linearity d) g_m/I_D

APPENDIX B

EVALUATION BOARD