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**A DESIGN METHODOLOGY OF
TRANSFORMER-BASED CLASS-E POWER
AMPLIFIER**

ALFRED LIM WEE CHUNG

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

**A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy**

2019

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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21/09/2020

Date

Goh Wang Ling

AUTHORSHIP ATTRIBUTION

STATEMENT

This thesis contains material from 4 paper published or pending publication in the following peer-reviewed journal(s) and conferences where I was the first and/or corresponding author.

Chapter 3 is published as:

1. Alfred Lim, Aaron Tan, Zhi Hui Kong and Kaixue Ma, "A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier," in Electronics 2019, 8, 494

The contributions of the co-authors are as follows:

- I designed, ran the experiments and did the floor-planning of the circuits
- I prepared the manuscripts and they were proof-read by both Asst/Prof Zhi Hui Kong and Prof Kaixue Ma
- Aaron Tan provided his EDA tools expertise in designing the circuits
- Asst/Prof Zhi Hui Kong provided valuable feedbacks on the drafts and helped to proof-read the manuscripts. She also fine-tuned the selling points of this work
- Prof Kaixue Ma provided the direction of the trends of PA in this research and gave his technical insights in PA design

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- Prof Kaixue Ma provided the direction of the trends of PA in this research and gave his technical insights in PA design
- Prof Keat Seng Yeo gave his insights and fine-tuned the DPA designs based on his experience with general RF circuits

3. Alfred Lim, Kaixue Ma, and Yeo Kiat Seng, “Transformer-Based Class-E CMOS Power Amplifiers”, 4th IEEE International Symposium on Next-Generation Electronics (IEEE ISNE 2015), May, 2015.

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- Prof Kaixue Ma provided the direction of the trends of PA in this research and gave his technical insights in PA design
- Prof Keat Seng Yeo gave his insights and fine-tuned the DPA designs based on his experience with general RF circuits

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- Aaron Tan provided his EDA tools expertise in designing the circuits

- Assoc/Prof Wang Ling Goh provided valuable feedbacks on the drafts and helped to proof-read the manuscripts. She also fine-tuned the selling points of this work
- Prof Kaixue Ma provided the direction of the trends of PA in this research and gave his technical insights in PA design

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Alfred Lim Wee Chung

ABSTRACT

Wireless system has increasingly developing and growing since the first mobile phone systems was first introduced. Due to the technology advancement in CMOS process, it can provide a high level of integration, low-cost and the feasibility to operate at radio frequencies (RF) due to the significant scaling of the transistors, CMOS technology thus becomes the best solution in RF applications. However, this has also become a challenge in order to meet the requirements on efficiency, output power, linearity and bandwidth from a low voltage supply (V_{DD}) arise from the scaling of transistors, especially the power amplifier (PA) one of the most important RF building blocks.

For the PA, the efficiency is a big challenge for the overall performance of most wireless system. Therefore, the design of a high-efficiency PA is the . A power amplifier's classes (A, AB, B, C, D, E, F, etc), and design fundamentals are presented. The class-E PA has a maximum theoretical efficiency of 100%. It consists of a single transistor that is driven as a switch and a passive load network. The passive load network is designed to minimize drain voltage and overlapping of current waveforms, which reduces the output power dissipation to the minimum. Of all the passive structures used in the class-E PA, high-quality inductors and transformers or baluns are the most difficult to realize monolithically due to their bigger size and loss as compared with other passive structures. In CMOS process they suffer from the presence of lossy substrates and high- resistivity metal, typically limiting the Q to about $7 \sim 10$ at around 2 GHz. This causes many high-speed RF power PAs using on-chips inductors, to have limited performance compared to designs using off-chip components. However, the use of off-chip components adds complexity and cost to design of these circuits.

In spite of its limitation, sub-micron CMOS prove to be the best process to implement the PA operating at frequency up to few GHz range. Therefore, the focus of this project is to propose a

design methodology to improve the efficiency and output power of a class-E PA with on-chip transformer integrated in CMOS technology.

Since the operation of the PA exerts a lot of stress on the switching transistor, a finite DC-feed inductance in the class-E load network is applied in order to reduce the drain-source voltage stress from 3.57 times to 2.5 times the supply voltage. Such an amplifier is designed and optimized by using an on-chip transformer such that the magnetic fluxes are constructive instead of destructive. Thus, the inductance reinforces itself and this reduces the sizes of both inductors significantly. Consequently, the quality factor of the on-chip inductors is enhanced and improve the efficiency due to lower inductor losses. The completed designs of the transformer-based class-E PA was submitted for fabrication using the GLOBALFOUNDRIES 65-nm RFCMOS technology is presented in chapter3, 4 and 5 with different design techniques.

The supply voltage of CMOS decreases with each new technology generation. To achieve sufficient output power at a low supply voltage, several design techniques have been proposed upon the use of on-chip transformer. The first approach is to use a transformation which makes the series resistance of the inductors smaller while still maintaining the inductance value. The second approach to use cascade or stacked transistor structure, which in combination with common-gate transistor allows operation at higher supply voltage while keeping reliability at a higher level. This result is higher output power, higher load and lower current, which potentially leads to lower losses and higher efficiency. The third approach to increase the output power for a given load is to use a differential structure. The signal is split into two antiphase paths using a balun or transformer, two similar PA blocks are used, and the signal is merged at the PA output using the same technique. Simulated results were compared for the different approaches and contrasted against theoretical understanding using derived equations.

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Contents

Statement of Originality	1
Supervisor Declaration Statement	2
Authorship Attribution Statement	3
Abstract	6
Acknowledgement	8
List of Figures	vi
Lists of Tables	vii
1 Introduction	1
1.1 Background	1
1.2 Motivation	3
1.3 Objectives and Specifications	3
1.4 Major contribution of the Dissertation	4
1.5 Organization of the Dissertation	5
2 Literature Review	6
2.1 General Considerations	6
2.1.1 Power Capability	7
2.1.2 Efficiency Calculations	7
2.1.3 Matching Considerations	8
2.2 Classification of Power PAs	11

2.2.1	Class-A	13
2.2.2	Class-AB, B and C	14
2.2.3	Class-F	15
2.2.4	Class-D	16
2.2.5	Class-E	17
2.3	Topologies of Class-E PA	19
2.3.1	Injection Locking Class-E PA	20
2.3.2	Wideband Load Transformation Networks Class-E PA	21
2.3.3	Efficient Class-E PA For Short-Distance Communications	22
2.3.4	Power-Combining Class-E PA with Finite Choke	23
2.3.5	High Power Wideband Class-E PA	24
2.4	Conclusions	25
3	A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier	26
3.1	Background	27
3.2	Methodology and Implementation on Transformer-Based Class-E PA	38
3.2.1	Design of the Inductors with Magnetic Coupling	38
3.2.2	Design of the DC-feed Inductance	41
3.2.3	Design of Inductors and Transformers	43
3.2.4	Transformer Layouts in Class-E PA	45
3.3	Measurement Results	47
3.4	Conclusions	52
4	A Design Methodology and Analysis for Cascode Transformer-Based Class-E Power Amplifier	53
4.1	Background	53
4.2	Methodology and Implementation on Transformer-Based Cascode Class-E PA	55
4.3	Measurement Results	61
4.4	Conclusions	63

5	A Design Methodology and Analysis for Transformer-Based Differential Class-E Power Amplifier	64
5.1	Background	64
5.2	Methodology and Implementation on Transformer-Based Differential Class-E PA	65
5.3	Measurement Results	72
5.4	Conclusions	75
6	Conclusion	76
6.1	Recommendations for Future Work	77
	AUTHOR'S PUBLICATIONS	87

List of Figures

1.1	Class-E power PA and soft-switching behaviour.	2
2.1	Normalized power-added efficiency versus gain. [1]	8
2.2	Block diagram of PA and matching circuits. [1]	9
2.3	Large-signal versus small-signal matching. [1]	10
2.4	Power PA family tree. [2]	11
2.5	A simplified PA, namely linear PA or current PA. [3]	12
2.6	class-A power amplifier.	13
2.7	class-AB, B and C power amplifiers.	14
2.8	class-F power amplifiers.	15
2.9	Class-D power PA schematic.	16
2.10	Class-E power PA schematic.	17
2.11	Equivalent circuit of the class-E PA.	20
2.12	Schematic of wideband class-E PA.	21
2.13	Circuit model of the class-E PA. (a) Conventional class-E PA. (b) Efficient class-E PA.	22
2.14	Power-combining class-E PA with finite choke and transmission-line harmonic trap.	23
2.15	High power wideband class-E PA.	24
3.1	Conventional Class-E power amplifier (PA) using NMOS transistor with radio frequency RF-choke and series LC network.	28
3.2	Ideal Class-E power amplifier.	29

3.3	Transformer-Based Class-E PA: magnetic coupling and determining correct dot placement.	39
3.4	Basic model of transformer.	40
3.5	Maximum voltage stresses on transistor M1 in both on and off states.	42
3.6	Schematic of on-chip transformer 3-D view	44
3.7	The quality factor plotted versus frequency for the inductors: (a) Coupling-inductors; (b) DC-feed inductor; (c) Output series inductor.	46
3.8	Microphotograph of the implemented power amplifier.	47
3.9	Transformer-based class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey).	48
3.10	Uncoupled class-E PA: Output power, drain efficiency and power-added efficiency versus the dc supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey). Drain efficiency (DE) and power-added efficiency (PAE)	49
3.11	Transformer-based class-E PA: Measured output power, drain efficiency and power-added efficiency versus operating frequency.	51
4.1	Schematic of the proposed transformer-based cascode class-E PA.	56
4.2	Drain voltage waveforms of common-gate (M_2) and common-source (M_1) transistors of class-E PA based on a cascode topology	56
4.3	Shunt capacitance against the load resistance	58
4.4	Output power against the load resistance	58
4.5	DC-feed current against the power loss	59
4.6	Class-E PA with two stacked transistors	60
4.7	Microphotograph of the implemented power amplifier.	61
4.8	Transformer-based cascode class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage	62
5.1	Current flowing in the DC-feed inductance.	65
5.2	A differential technique to limit current swing.	66

5.3	Schematic of the proposed transformer-based Differential class-E PA.	67
5.4	Symmetric inductor in a differential topology.	68
5.5	Current distribution in a conductor at (a) low and (b) high frequencies.	69
5.6	Current distribution in adjacent turns.	70
5.7	Two adjacent metal placed in series.	71
5.8	Two adjacent metal, placed in parallel.	72
5.9	Microphotograph of the implemented power amplifier.	73
5.10	Transformer-based differential class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage	73

List of Tables

2.1	Comparison of the of properties of different PA classes.	12
3.1	Advantages and drawbacks of interleaved and stacked configurations.	45
3.2	Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM). . .	51
4.1	Maximum V_{GS} and V_{DS} stresses on M_1 and M_2 in both on and off states.	57
4.2	Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM). . .	63
5.1	Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM). . .	74

Chapter 1

Introduction

1.1 Background

Wireless system has increasingly growing to become due to the advancements in wireless and mobile phone systems, and the applications span across a wide range of areas [4], among which wireless networks for general packet radio service (GPRS), worldwide interoperability for microwave access (WiMAX), wideband code division multiple access (WCDMA), wireless local area network (WLAN), radar, enhanced data rates for GSM evolution (EDGE), mobile communications (GSM) [5–7], heating, electronic warfare [8, 9], and medical microwave imaging [10–15].

Optimizing electrical performances (linearity, power gain, efficiency, and output power) of power amplifier (PA) is very challenging for any wireless communication system. This challenge will become more challenging to overcome when it comes to the full design integration of on-chip inductors. Hence, it is crucial to come up with a methodology to overcome the PAs design issues in the CMOS process.

PA is one of the most critical and power-consuming components in the transmitter architecture. The PA as a component has different topologies such as differential PA [16, 17], cascade PA, [18, 19] and cascode PA [20, 21], to name a few. The PA does come with design trade-offs between different electrical parameters such as efficiency, power, gain, and linearity. Another aspect of RF circuits is the reliability issues such as hot carrier stress, gate oxide breakdown [22], and junction breakdown [23] are some examples. For PA, in general, the output power

is required to be high as the conventional component before the antenna in a transmitter. One topology would be more preferred than the others for PA applications due to its high output power requirements. Furthermore, to design a PA with full integration in CMOS process still, a challenging problem needs to be overcome, and some PA designs have obtained a full integration. However, the output power remains low [24–27].

Using class-E PA [28] as an example as shown in Figure 1.1, there are some of the emerging class-E PA architecture introduced in the recent years, such as injection locking [29], harmonic matching [30], and power combining [31], which are implemented to overcome the disadvantages of silicon processes such as inherent low supply voltage (V_{DD}), silicon substrate losses and low drain-source breakdown voltages of transistors.

Figure 1.1: Class-E power PA and soft-switching behaviour.

The objective of the dissertation is to focus on the class-E PA, including the essential operation (soft-switching), theoretical analysis, and circuit design with a fully integrated on-chip transformer. For a PA, there are four critical electrical parameters, namely the efficiency, power, linearity, and gain that need to be met the requirements of the wireless communication system. In

this dissertation, the proposed design methodology implemented on class-E PA is to enhance the efficiency and output power in CMOS process and will be discussed in chapter 3. The proposed methodology is also expanded on transformer-based class-E PA in cascode and differential topologies in chapter 4 and chapter 5, respectively.

1.2 Motivation

Performance is only an aspect of concern for consumers as the lifetime of the battery is also essential. In other words: low-cost CMOS technology and a high-efficiency PA. Initially, CMOS was for digital technology as it was not developed for RF designs. However, the real advantage of CMOS is the low cost of production when scaling and potentially provide a PA design with full integration.

The existing designs of the class-E PA in CMOS encounter the challenges of design trade-offs between low V_{DD} , lossy power loss in the inductors, high transistors turn-on resistance (r_{on}) and parasitic capacitances of transistors. Due to the above challenges, most PAs are designed in gallium arsenide (GaAs) or silicon-germanium (SiGe) process to try to overcome them. It is also the reason why most of the PAs still employ high-quality factor (Q) microstrip lines or off-chip inductors. This serves as the primary motivation to propose a design methodology to implemented on transformer-based class-E PA topology in a highly integrated solution in CMOS process.

1.3 Objectives and Specifications

The CMOS technology provides the possibility of low power, low cost, and high integration. However, the performance of the RF circuit implemented using CMOS technology is limited. This dissertation focuses on the design methodology of high-efficiency class-E PA using CMOS technology, including the basic operation, theoretical analysis, and circuit design. Then, a transformer-based class-E PA is proposed and implemented. Subsequently, the proposed class-E PA is evaluated to explore the possibilities to improve the output power and efficiency in CMOS RF class-E PA.

1.4 Major contribution of the Dissertation

This dissertation focuses on the design methodology of a circuit using a transformer-based class-PA as an example. The methodology concentrates first on the transformer-based class-PA single-ended architecture. The analysis uses the design of inductors and transformers to quantify a metric for bench-marking of class-E PA, where efficiency and output power is a primary concern. After which, a topology cascode consideration is given to the transformer-based class-E PA to enhance the efficiency and output power, demonstrating the potential that a lower supply voltage (V_{DD}) process can show comparable performance to a higher supply voltage (V_{DD}) process due to higher breakdown voltage of the transistor. Moreover, the differential topology implemented on the transformer-based class-E PA allows us to improve further the output power and cancellation of the frequency of the even harmonics at the output with no added complexity to the circuitry. The following detailed contributions have been achieved:

1. An analysis of the conventional class-E PA was discussed
2. A methodology and flow are proposed for circuit design using transformer-based class-E PA and demonstrated the design in CMOS 65 um process.
3. The advantages of DC-feed over RF-choke inductance was discussed
4. The design and layout consideration of inductors and transformers were proposed
5. The issues due to hot carrier effect and oxide breakdown was addressed in class-PA. We proposed a cascode topology implemented on the transformer-based class-E PA using the CMOS 65 um process to enhance the output power and efficiency of the class-E PA design, demonstrating the lower supply voltage process can yield comparable performance with the high supply voltage process.
6. A differential topology implemented on transformer-based class-E PA was proposed and results in an excellent second harmonics cancellation and output power enhancement to class-E PA without adding additional circuitry to increase its complexity.

1.5 Organization of the Dissertation

This dissertation is organized into five chapters. Chapter 1 introduces the background knowledge of the class-E PA limitations and challenges. It also includes the background and motivation for research of this area and lists the significant contributions of this dissertation.

Chapter 2 first introduces the important electrical parameters to quantify a metric to evaluate the PA. This is then followed by a classification of PAs based on their conduction angle and their drain voltage and current waveforms at the out network.

Chapter 3 proposes a design methodology implemented on the transformer-based class-E power PA by using the mutual magnetic coupling effect. The effect of magnetic coupling was first discussed and followed by a comparison between DC-feed and RF-choke inductance, layout consideration, and the limitation due to hot carrier effect and oxide breakdown in the design.

Chapter 4 presents the investigation of the possibilities to combine high power and efficiency in one single PA by using a cascode topology implemented on the transformer-based class-E PA. The experiment results for the cascode topology is discussed in this chapter as well.

Chapter 5 proposes a differential topology implemented on the transformer-based class-E PA to obtain a good second harmonics cancellation without adding additional circuitry to increase its complexity. The experiment results for the differential topology is discussed in this chapter as well.

Chapter 6 concludes this research and gives the area that merits future investigations.

Chapter 2

Literature Review

Power Amplifiers (PA) are used mainly in the RF transmitter. The perennial trade-off between efficiency and linearity is of utmost importance in a monolithic circuit design implementation. High efficiency implies a longer lifetime of a battery, and it is needed to realize small and mobile devices. Integrated circuits usually have a maximum of V_{DD} to avoid device breakdown and electron-migration due to large current. Several research works [32–34] have highlighted potential problems and solutions to achieve high efficiency and linearity in a fully integrated PAs.

2.1 General Considerations

It has been shown that the issue in PA design [35, 36], namely, the trade-off between the output power and the voltage swing experienced by the output transistor. It can be proven that the product of the breakdown voltage and f_T of silicon devices is around 200 GHz·V [36]. Thus, transistors with a f_T of 200 GHz dictate a voltage swing of less than 1 V. To reduce the V_{peak} of the output transistor, a matching network designed to match the PA output and the load reduces the load resistance seen by the PA such that smaller voltage swings can still deliver the required output power. The need for transforming the voltage swings means that the current generated by the output transistor must be proportionally higher.

2.1.1 Power Capability

One of the design objectives of PAs is to transfer a required power to a load from the supply voltage. This is contributed by the load resistor and the V_{DD} . An example would be 3V of V_{DD} , and a R_L of 50 Ω , the maximum power is thus given to be

$$P = \frac{V_{DD}^2}{2R} = \frac{3^2}{2 \cdot 50} = 90mW = 19.5dBm \quad (2.1)$$

This will result in a tuned PA with a V_{p-p} of 6V with V_{min} at 0V.

2.1.2 Efficiency Calculations

The efficiency η , is also called DC-to-RF efficiency, is given by

$$\eta = \frac{P_{out}}{P_{dc}} \quad (2.2)$$

Where P_{out} is the ac output power and, with the assumption of current and voltage are zero degrees out of phase, and is shown as:

$$P_{out} = \frac{i_1 v_1}{2} = \frac{i_1^2 R_L}{2} \quad (2.3)$$

Where i_1 and v_1 are the fundamental peak values of the current and voltage, respectively, which are also determined by Fourier analysis. P_{dc} is the power from the supply voltage and is shown as:

$$P_{dc} = \frac{1}{T} \int_0^T V_{DD} i_{DS} dt = V_{DS} I_{dc} \quad (2.4)$$

Power-added efficiency (PAE) is a design metric to indicate how power efficiency a PA is; however, it takes into consideration the gain of PA and is given by:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} - P_{out}/G}{P_{dc}} = \eta \left(1 - \frac{1}{G}\right) \quad (2.5)$$

Thus, it can be seen that the PAE is the same as DC-to-RF efficiency for high gain.

Figure 2.1 shows the plot of efficiency and PAE for a range of output power gains. From the

figure, gain above 10dB has PAE within a delta of 10% from efficiency η . As the gain starts to compress, the PAE is showing a downward trend. As an example, when the gain is 3 dB, the PAE is only half of the dc-to-RF efficiency.

Typically, as the input power of the PA increases, the PA goes into compression with the gain and PAE decreasing. This demonstrates that there is an optimal value of PAE, and it usually is at a few dB beyond the PA 1dB-compression point.

Figure 2.1: Normalized power-added efficiency versus gain. [1]

2.1.3 Matching Considerations

To obtain maximum P_{out} of the PA, the output should not have a conjugate matching. Instead, the load is designed in such a way that the voltage and current should play the part to deliver the required power. The diagram of conjugate matching can be seen from Figure 2.2. In the figure, Γ_S is the source reflection coefficient, and Γ_L is the load reflection coefficient.

Figure 2.2: Block diagram of PA and matching circuits. [1]

In the PA linear regime where the input power is low, the maximum output power can be obtained with $\Gamma_L = S_{22}^*$. The non-linearities would result in gain compression, the onset of harmonics, and signals' phase shifts. This can result in a deviation of operating point and output load impedance. The large-signal operation, typically for PAs, employs load-pull to determine the optimal load of R_L . The result between small signal and large signal tuning can be seen in Figure 2.3.

Figure 2.3: Large-signal versus small-signal matching. [1]

As shown in Figure 2.3, the graph of the small-signal curve will end up with a higher output power for a small-signal while the large-signal curve shows that that would be higher output power for large signals. If the operation is to be set at the optimal PAE, the optimal power tuning will result in about 1 to 3 dB of a higher power.

One can estimate the optimum impedance (Z_{opt}) by adjusting the load so that the current and voltage are 180 degrees out of phase as shown in Figure 2.2 such that the complex load is reactively matched.

2.2 Classification of Power PAs

PAs generally have two modes of operations as shown in Figure 2.4. If the main PA transistor is functioning as a trans-conductance element, which means it converts the RF input signal from the gate of the transistor into a current flowing through the drain-source terminal, the PA is therefore classified as a linear or current PA. If the transistor of PA just operates as a switch, the PA is then classified as a switching PA.

Figure 2.4: Power PA family tree. [2]

Current PAs, as shown In Figure 2.5, can be further classified into different classes of operation based on their conduction angle [35]. For PAs, it can be further classified into linear and nonlinear PAs. The nonlinear PAs refers to a PA that only has phase linearity but no amplitude linearity. The advantage of using a nonlinear PAs is the high efficiency that can be obtained. The poor linearity of a PA is not always a disadvantage when efficiency has a more top priority.

Figure 2.5: A simplified PA, namely linear PA or current PA. [3]

Table 2.1 shows the comparison of the properties of different classes of PA. There exist different variants of fundamental classes such as inverted Class F and Class E et. cetera [37]. There are also classes of PA past class-F, but they are still not clearly defined for use at RF and will not be included in this discussion.

Table 2.1: Comparison of the of properties of different PA classes.

Class	Maximum drain efficiency [%]	Peak drain voltage	Peak drain current	Maximum output
A	50	$2 * V_{DD}$	$2 * V_{DD}/R$	$V_{DD}^2/2R$
B	78.5	$2 * V_{DD}$	$2 * V_{DD}/R$	$V_{DD}^2/2R$
C	100	$2 * V_{DD}$	$2 * V_{DD}/R$	$V_{DD}^2/2R$
D	100	$1 * V_{DD}$	V_{DD}/R	$\frac{(\frac{2}{\pi} * V_{DD})^2}{2R}$
E	100	$3.6 * V_{DD}$	$1.7 * V_{DD}/R$	$\frac{0.577^2 V_{DD}^2}{R}$
F	100	$2.5 * V_{DD}$	V_{DD}/R	$\frac{(\frac{4}{\pi} * V_{DD})^2}{2R}$

The most popular class of PA in RF design is class-AB, which is not listed in Table 2.1. It is

in between class-A and class-B and inherits properties of both of these two classes. It has been mostly tapped on as it offers a good trade-off between efficiency, linearity, and stand-by current.

2.2.1 Class-A

For class-A PA, the conduction angle of the current is 360 degrees, which results in low efficiency but high linearity due to low harmonics distortion.

Figure 2.6: class-A power amplifier.

The shapes of the current and voltage wave-forms cannot be determined by the transistor if it is turned off. It is, however, determined by the external passive circuits that will have a significant impact on efficiency. The shaping of the current and voltage wave-forms also shape the current and voltage overlaps, which will change the efficiency of the PA.

Higher harmonics will be generated when the transistors are turned off. The termination of the harmonics will be necessary for the shaping of the current and voltage wave-forms.

2.2.2 Class-AB, B and C

The class-B PA seems to be preferable due to its comparable output power to a class-A PA, and its efficiency is increased to 78.5%. To achieve the same output power as class-A PA, the drain-source voltage swing at the gate of the transistor need to be doubled. This implies that the gain of class-A PA is double that of class-B PA., as indicated in Figure 2.7.

For small conduction angles such as for a class-C PA, the output power approximates to zero when it is not conducting, The explanation for this is that the voltage amplitude at the output is lesser than or equal to V_{DD} . Still, the value of the load resistance approximates to a very high value. For both P_{out} and P_{DC} to be reduced at the same time explains the contradicting ideal 100% efficiency even though no P_{out} is delivered, and because of the low P_{out} of class-C, therefore, it a less than ideal option for low voltage applications in RF circuit design.

Figure 2.7: class-AB, B and C power amplifiers.

2.2.3 Class-F

The efficiency can be increased by reducing the transistor turn-on time, as a result of minimizing the drain voltage-current overlap. However, if the transistor conduction time is over, reducing the output power of the PA will be reduced drastically. The shaping of the drain voltage-current overlap while still maintaining a 50% conduction angle can be accomplished by the harmonic trap across the load resistor R_L . This PA design is called as class-F and is depicted in Figure 2.8 [38]. The drain-source voltage V_{DS} is equal to the output voltage, plus the voltage across each of the harmonic resonators, that are resonated with all the odd harmonics frequency. The superimpose of the frequency of the odd harmonics across the transistor drain-to-source terminal will make the drain-to-source voltage resemble a square wave, and the overlapping of the current and voltage is therefore reduced and resulting in a 100% efficiency [39,40].

Figure 2.8: class-F power amplifiers.

A critical difference between a switching PA and the non-linear PAs is the hard non-linearity of the PA. PA with hard non-linearity (i.e., class-A and AB, B, C, and F) still have some correlation between the input and output amplitude. Whereas for switching PA (i.e., class-D

and E), the output only has a consistent amplitude, which will solely be relying on the supply voltage.

2.2.4 Class-D

The input signal V_{IN} and the output signal V_{DS} for class-D PA shown in Figure 2.9 are both square waves, if square waves are applied to R_L , harmonic power would be dissipated. Therefore the series tank consisting of L_O and C_O , only allows sinusoidal current through R_L , which would result in a drain efficiency of 100% in the ideal case. However, it poses a significant challenge to integrate a class-D PA in CMOS process.

Figure 2.9: Class-D power PA schematic.

One of the drawbacks is the fast switching property of PA as the switch would turn off once the voltage across it falls below a certain value. In CMOS design, the large parasitic capacitance from the transistors is inevitable. When the transistor is turned on, the energy of $E_C = \frac{1}{2}CV^2$ will be dissipated in the switch. Therefore, $P_{diss} = \frac{1}{2}fCV^2$. The finite switching times between on and off states of the transistor is another loss to degrade the performance [41].

Another disadvantage is the required of high driving power. In practice, the size of the pMOST over the size of the nMOST is typically a factor of three. The high parasitic input capacitance, consequently makes the class-D PA unfavorable for RF applications.

2.2.5 Class-E

Similar to class-D, class-E PA has the potential to achieve 100% efficiency. The fundamental class-E PA design is shown in Figure 2.10 [28]. The tuned series tank (L_0 and C_0) would result in the output voltage is sinusoidal, and thus, no harmonic power will be dissipated in the ideal case. The NMOS acts as the switch in Figure 2.10. If the transistor is turned on, the DC current will flow through the large RF-choke (L_{RFC}) and NMOS. If the switch is turned off, the DC current less the output will be dumped into capacitor C_1 .

Figure 2.10: Class-E power PA schematic.

The most interesting property of class-E PA occurs at the transistor is being turned on again, at this instant of time when the first derivative and its drain-to-source voltage both return to zero again. Hence, the switching losses reduce to zero.

The theory of Class E PA [28] requires both the first derivative and the switch voltage to be zero when the switch is turned off as shown in equations 2.6 and 2.7

$$V_{DS}(t = t_1) = 0 \quad (2.6)$$

$$\left. \frac{dV_{DS}}{dt} \right|_{t=t_1} = 0 \quad (2.7)$$

t_1 indicates the time at which the transistor is turned off, and $V_{DS}(t)$ represents the drain-to-source voltage. The first derivative is not essential to achieve a 100% efficiency in the PA. However, if it equals or close to zero, the PA would be less sensitive to variations of components in the design, and the output power will be maximized for a given drain voltage peak.

For the conventional class-E PA, inductor L_{RFC} is assumed to be very large, and the current through the R_L is considered to be purely sinusoidal. Hence no losses are taken into consideration. Under these conditions, the design equations can be derived and are shown to be [42]

$$C_1 = \frac{8}{\pi(\pi^2 + 4)} \frac{1}{\omega R_L} \approx 0.1836 \frac{1}{\omega R_L} \quad (2.8)$$

$$L_x = \frac{\pi(\pi^2 - 4)}{16} \frac{R_L}{\omega} \approx 1.1525 \frac{R_L}{\omega} \quad (2.9)$$

$$P_O = \frac{8}{\pi(\pi^2 + 4)} \frac{V_{DD}^2}{R_L} \approx 0.5786 \frac{V_{DD}^2}{R_L} \quad (2.10)$$

The conventional class-E circuit is simple, but the shunt capacitor C_1 makes the PA attractive for CMOS integration, owing to the large drain-to-source parasitic capacitance from the CMOS transistor which can be integrated into a class-E PA design. Therefore, the parasitic capacitance is not a weakness anymore when it comes to designing in class-E PA.

2.3 Topologies of Class-E PA

Taking into account the circuit simplicity, the beneficial use of the parasitic drain-source capacitance, and the superior performance regarding hot carriers, CMOS seems to be the natural habitat of the class-E PA. However, the maximum theoretical peak drain-source voltage is about three and a half times the supply, which is a significant drawback using a finite inductance instead of an RF-choke [L_{RFC} in Fig. 2.9], the peak voltage can be reduced to two and a half times the supply [43, 44]. Higher output power, higher load resistance, or higher efficiency can also be achieved using a finite inductance [44]. However, the peak voltage across the switch still consider quite high to make sufficient output power and safe operation at a low-voltage CMOS technology. The most common way to extend the tolerable supply voltage is to use the cascade or stacked transistor structure [45], which in combination with thick-oxide transistors allows operation at higher supply voltage while keeping reliability at a high level. The result is higher output power, higher load, and lower current, which potentially leads to lower losses and higher efficiency. Operating points have to be carefully selected so that the devices work optimally with good headroom; otherwise, there is no performance gain. Another way to operate at high supply voltages is to use high-breakdown CMOS-compatible RF devices. Lateral double-diffused MOS (LDMOS) transistors have proven to be successful in base-station applications [37, 46]. The advantages of LDMOS for RF PA applications are its thermal stability, high ruggedness, and excellent linearity characteristics.

Another necessary consequence of a reduced DC-feed inductance is the increased current swing in the DC-feed, and thus an increased AC-current that has to be delivered by the power supply. The solutions to solve the problem of the AC power supply currents are the use of differential topologies or decoupling capacitors. In the following, this report reviews a compilation of state-of-the-art published results for class-E PA with the focus on high efficiency while keeping gain, output power, and linearity at a reasonable level.

2.3.1 Injection Locking Class-E PA

The concept of the injection-locking technique was adopted in a PA by Oh [47], and the injection-locking class-E PA achieves high PAE with low driving power. The approach is to use the small-signal equivalent circuit to predict the boundary condition of the oscillation, and the derivation of the oscillation condition can be obtained. The equivalent circuit of the class-E PA is shown in Figure 2.11 [29]. To satisfy the startup oscillation condition at the gate terminal, the real part of Z_{in} must be negative. The negative resistance is used to compensate for the losses in the circuit.

Figure 2.11: Equivalent circuit of the class-E PA.

2.3.2 Wideband Load Transformation Networks Class-E PA

The wideband load transformation networks class-E PA with finite DC-feed inductance, L_X , instead of an ideal RFC is illustrated in Figure 2.12 [48]. In the parallel circuit load network, the class-E conditions (i.e., ZVS and ZDS) can be fulfilled by using only the $L_X - C_X$ resonator. For a given output power, the resulting R_E (2.42 times) is significantly larger than in the conventional load transformation networks, which allows attaining wide bandwidths.

Figure 2.12: Schematic of wideband class-E PA.

2.3.3 Efficient Class-E PA For Short-Distance Communications

The inductance constraint imposed by L_0 can be relaxed if it functions as DC-feed instead of RF-choke. Conventionally, only series resonant network is used to improve the harmonic rejection. For Figure 2.13(a) [30] with large R_{eq} (required for low output power), the rejection ratio is directly related to $R_{eq}/[R_{eq} + X_S(n\omega_O)]$, where ω_O is the desired output frequency, and n is the n^{th} harmonic generated by class-E PA ($n \geq 2$). To improve the rejection, the conventional design have no choice but to increase X_S and thus L_{S0} . For Figure 2.13(b) [30] a parallel network is added. Now the rejection ratio would depend on the ratio of $X_P(n\omega_O)/[X_P(n\omega_O) + X_S(n\omega_O) + R_{eq}]$ for $n \geq 2$. Due to presence of X_P , it relaxes the requirement on X_S to achieve same harmonic rejection. This will reduce the L_{S0} and allow better on-chip integration.

Figure 2.13: Circuit model of the class-E PA. (a) Conventional class-E PA. (b) Efficient class-E PA.

2.3.4 Power-Combining Class-E PA with Finite Choke

A small value choke of 2.2nH was used to substitute for the massive RF-choke inductance required in the conventional class-E design. Besides, by adopting the three-harmonic suppression levels of 50 and 46 dBc, respectively, were obtained. The resulting architecture is shown in Figure 2.14 [31].

Figure 2.14: Power-combining class-E PA with finite choke and transmission-line harmonic trap.

The two open circuit stubs TL2A (Z_{02A} and $\theta_{2A} = 45^\circ$) and TL2B (Z_{02B} and $\theta_{2B} = 30^\circ$) in order to suppress the undesired second and third harmonic components, respectively.

2.3.5 High Power Wideband Class-E PA

The high-power, high-efficiency, wideband class-E PA designed upon the load admittance synthesis concept and built using an uncomplicated low-loss load network with a low loss wideband admittance transformer as the main component. The admittance transformation provided by the transformer ($1:n^2$) allows using higher reactance components for the load plane “LP3”. Having higher reactance, these components exhibit higher quality factors (Q) and self-resonance frequencies. The resulting architecture is shown in Figure 2.15 [49]

Figure 2.15: High power wideband class-E PA.

2.4 Conclusions

In this chapter, some important topics related to the amplification of RF signals have been reviewed and defined. First, the generation of a modulated RF signal, and some signal properties that are relevant for or have a significant impact on the design of a power amplifier, have been discussed.

Next, the classification of power amplifiers was discussed as well. Taking into account the circuit simplicity, the beneficial use of the parasitic drain-source capacitance, and the superior performance regarding hot carriers, CMOS seems to be the natural habitat of the class-E amplifier. Class-E indeed does achieve a high efficiency, but the amplitude linearity is completely lost in this amplifier. The design of a class-E amplifier in CMOS and the different trade-offs that exist will be the topic of the next chapter.

Chapter 3

A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier

The major drawback of the class-D PA is that the frequency of operation is limited by the rise and fall times of the transistor output pulse. The non-zero switching time is a result of parasitic capacitances in the circuit and transistor.

The class-E PA concept was first introduced by Ewing in 1964 and later independently rediscovered by N. O. Sokal and A. D. Sokal [28] in 1975. In 1977 and 1978, Raab derived design equations for the class-E PA [42, 50]. This work was later expanded to include a relationship between maximum efficiency and output maximum power. The derivation was done for an arbitrary duty cycle of 50 % similar to [51] and [10] simply because of high-frequency switching is difficult and counterproductive at a duty cycle other than 50 %.

The essential feature of the class-E PA is to produce a voltage wave across the capacitance shunting the transistor that has zero amplitude and zero slope when the transistor is turned on. This relieves the switching speed requirement of the class-D PA and yet maintains the possibility of 100 % efficiency.

This chapter proposes a new technique and design methodology on a transformer-based Class-E complementary metal-oxide-semiconductor (CMOS) power amplifier (PA) with only one transformer and two capacitors in the load network. An analysis of this amplifier is presented

together with a uncomplicated and straightforward design procedure. The experimental results are in good agreement with the theoretical analysis. The following performance parameters are determined for optimum operation: The current and voltage waveform, the peak value of drain current and drain-to-source voltage, the output power, the efficiency, and the component values of the load network are determined to be essential for optimum operation. The measured drain efficiency (DE) and power-added efficiency (PAE) is over 70 % with 10-dBm output power at 2.4 GHz, using a 65 nm CMOS process technology.

3.1 Background

With the explosive growth of wireless and mobile communication systems adoption, the demand for compact, low-cost, and low power portable transceiver has increased dramatically. One of the technical issues that are generally encountered for the portable transceivers is the limited lifetime of the battery. The power amplifier (PA) is typically the most power-hungry building block in the transceiver. Therefore, the design of a high-efficiency radio frequency (RF) PA is the most critical solution to overcoming the battery lifetime limitation in portable communication systems. The class-E PA, as depicted in Figure 3.1 has a maximum theoretical efficiency of 100%. It consists of a single output transistor that is driven as a switch and a passive load network. The passive load network is designed to minimize the drain voltage and current waveforms from overlapping [28], which causes output power loss. The significant difference between class-E PA and others (e.g., Classes A, B, AB, C, D, and F) is that it incorporates the parasitic drain-source capacitance [42] as part of the passive load network design, which is an advantage, especially in CMOS design. In class-E PA, the circuit operation is determined by the transistor when it is on, and by the transient response of the load network when the transistor is off [42]. It dramatically reduces the transistor power losses during the off-to-on transition of the device, resulting in high efficiency. To minimize these power losses, the following two conditions need to be met [28, 42, 52]:

$$V_{DS}(t = t_1) = 0 \quad (3.1)$$

$$\frac{dV_{DS}}{dt}\bigg|_{t=t_1} = 0 \quad (3.2)$$

Figure 3.1: Conventional Class-E power amplifier (PA) using NMOS transistor with radio frequency RF-choke and series LC network.

In the conventional class-E PA, the RF-choke (RFC) is assumed to have a sufficiently high reactance, and the output current through the load resistor R_L is essentially a sinusoidal at the fundamental frequency. A simple equivalent circuit of this PA is based on the following assumptions [42]:

- The RF-choke allows only a constant (dc) input current and has no series resistance
- The Q of the series-tuned output circuit is high enough that the output current is mainly a sinusoidal at the carrier frequency
- The total shunt capacitance is independent of the drain voltage

Analysis of a conventional class-E PA begins by determining the drain voltage waveform as a function of the dc input current and the sinusoidal output current [28]. An idealized equivalent circuit is shown in Figure 3.2.

Figure 3.2: Ideal Class-E power amplifier.

The output voltage with amplitude a and unspecified phase ϕ is

$$v_o(\theta) = a \cdot \sin(\omega t + \phi) = a \sin(\theta + \phi) \quad (3.3)$$

and the output current is

$$i_o(\theta) = \frac{a}{R} \sin(\theta + \phi) \quad (3.4)$$

The voltage, $v_\gamma(\theta)$, is also sinusoidal but with a phase offset γ :

$$\begin{aligned} v_\gamma(\theta) &= v_o(\theta) + v_\psi(\theta) \\ &= a \sin(\theta) + X \frac{a}{R} \cos(\theta + \phi) \end{aligned} \quad (3.5)$$

These two terms may be added together by defining b and ψ as

$$\frac{xa}{R} = b\sin(\psi) \quad (3.6)$$

$$a = b\cos(\psi) \quad (3.7)$$

then

$$\begin{aligned} v_\gamma(\theta) &= b\cos(\psi)\sin(\theta + \phi) + b\sin(\psi)\cos(\theta + \phi) \\ &= b\sin(\theta + \gamma) \\ &= b\sin(\xi) \end{aligned} \quad (3.8)$$

where

$$\gamma(\theta) = \phi + \psi = \phi + \arctan(X/R) \quad ; \quad \xi = \theta + \gamma \quad (3.9)$$

and

$$b = a\sqrt{1 + (X/R)^2} = a\rho \quad (3.10)$$

When the switch is turned off, the voltage across the switch results from charging the shunt capacitance C_1 with $i_c(\theta)$. This voltage is not sinusoidal:

$$\begin{aligned} v_1(\theta) &= \frac{1}{\omega C} \int_0^\theta i_c(\xi) d\xi \\ &= \frac{1}{B} \int_0^\theta [I_{dc} - \frac{a}{R} \sin(\xi + \phi)] d\xi \\ &= \frac{I_{dc}}{B}(\theta) + \frac{a}{BR} \cos(\theta + \phi) - \frac{a}{BR} \cos(\phi) \end{aligned} \quad (3.11)$$

At the fundamental frequency, the tuned circuit is resonant, so at this frequency $v_1(\theta) = v_\gamma(\theta)$, and the fundamental amplitude of the switch voltage is

$$b = \frac{1}{\pi} \int_0^\pi v_1(\theta) \sin(\theta + \gamma) d\theta \quad (3.12)$$

$$b = b_1 + b_2 + b_3 + b_4 \quad (3.13)$$

Fourier Analysis:

$$\begin{aligned} b_1 &= \frac{I_{dc}}{\pi B} \int_\gamma^{\gamma+\pi} \xi \sin(\xi) d\xi \\ &= \frac{I_{dc}}{\pi B} (-\xi \cos(\xi)) \Big|_\gamma^{\gamma+\pi} + \int_\gamma^{\gamma+\pi} \cos(\xi) d\xi \\ &= \frac{I_{dc}}{\pi B} (\pi \cos(\gamma) + 2\gamma \cos(\gamma) - 2\sin(\gamma)) \end{aligned} \quad (3.14)$$

$$\begin{aligned} b_2 &= -\frac{I_{dc}}{\pi B} \gamma [-\cos(\theta + \gamma)] \Big|_0^\pi \\ &= -\frac{I_{dc}}{\pi B} 2\gamma \cos(\gamma) \end{aligned} \quad (3.15)$$

$$\begin{aligned} b_3 &= \frac{a}{2\pi BR} \int_0^\pi [\sin(2\theta + \gamma + \phi) + \sin(\gamma - \phi)] d\theta \\ &= \frac{a}{2\pi BR} \sin(\psi) \end{aligned} \quad (3.16)$$

$$\begin{aligned} b_4 &= \frac{a}{\pi BR} \cos(\phi) \cos(\theta + \gamma) \Big|_0^\pi \\ &= -\frac{a}{\pi BR} 2\cos(\gamma) \cos(\phi) \end{aligned} \quad (3.17)$$

The sum of these four terms gives

$$b = a\rho = \frac{I_{dc}}{B} \cos(\gamma) - \frac{I_{dc}}{\pi B} \sin(\gamma) + \frac{a}{2\pi BR} \sin(\psi) - \frac{2a}{\pi BR} \cos(\gamma) \cos(\phi) \quad (3.18)$$

This can be solved for the value of a , which will provide a relationship between the dc power supply current and the amplitude of the output signal:

$$a = I_{dc}R \frac{\pi \cos(\gamma) - 2 \sin(\gamma)}{\pi BR \rho + 2 \cos(\phi) \cos(\phi + \psi) - (\pi/2) \sin(\psi)} \quad (3.19)$$

At the fundamental frequency, the quadrature component of $v_1(\theta)$ must be zero. This gives a second relationship for a . Again for the half period when $v_1(\theta) \neq 0$,

$$\begin{aligned} 0 &= \frac{1}{\pi} \int_0^\pi v_1(\theta) \cos(\theta + \gamma) d\theta \\ &= \int_0^\pi \left[\frac{I_{dc}}{B}(\theta + \gamma) - \frac{I_{dc}}{B}\gamma + \frac{a}{BR} \cos(\theta + \phi) - \frac{a}{BR} \cos(\phi) \right] \cos(\theta + \gamma) d\theta \\ &= c_1 + c_2 + c_3 + c_4 \end{aligned} \quad (3.20)$$

Fourier Analysis:

$$c_1 = \frac{I_{dc}}{B} [-\pi \sin(\gamma) - 2\gamma \sin(\gamma) - 2 \cos(\gamma)] \quad (3.21)$$

$$c_2 = \frac{2I_{dc}}{B} [\sin(\gamma)] \quad (3.22)$$

$$c_3 = \frac{a\pi}{2BR} [\cos(\psi)] \quad (3.23)$$

$$c_4 = \frac{2a}{BR} [\cos(\theta) \sin(\gamma)] \quad (3.24)$$

which when summed together gives

$$0 = \frac{I_{dc}}{B} [-\pi \sin(\gamma) - 2 \cos(\gamma)] + \frac{a}{BR} \left[\left(\frac{\pi}{2} \right) \cos(\psi) + 2 \sin(\gamma) \cos(\theta) \right] \quad (3.25)$$

$$\begin{aligned} a &= I_{dc}R \frac{2 \cos(\gamma) + \pi \sin(\gamma)}{(\pi/2) \cos(\psi) + 2 \cos(\phi) \sin(\gamma)} \\ &= (I_{dc}R) g(\theta, \psi, \gamma) \end{aligned} \quad (3.26)$$

Power and Efficiency:

$$\begin{aligned}
a &= I_{dc}R_{dc} = \frac{1}{2\pi} \int_0^\pi v_1(\theta) d\theta \\
&= \frac{1}{2\pi} \int_0^\pi \left[\frac{I_{dc}}{B} \theta + \frac{a}{BR} \cos(\theta + \phi) - \frac{a}{BR} \cos(\phi) \right] d\theta \\
&= \frac{I_{dc}}{2\pi B} \left(\frac{\pi^2}{2} \right) + \frac{a}{2\pi BR} [\sin(\pi + \phi) - \sin(\phi)] - \frac{a\pi}{2\pi BR} \cos(\phi)
\end{aligned} \tag{3.27}$$

And

$$R_{dc} = \frac{1}{2\pi B} \left(\frac{\pi^2}{2} - 2g \sin(\phi) - \pi g \cos(\pi) \right) \tag{3.28}$$

R_{dc} is the resistance that the PA shows to the power supply.

$$P_{dc} = V_{DD} I_{dc} \tag{3.29}$$

And using $a = I_{dc} Rg$

$$P_o = \frac{v_o^2}{2R} = \frac{a^2}{2R} = \frac{I_{dc}^2 Rg^2}{2} \tag{3.30}$$

So the efficiency is

$$\eta = \frac{P_o}{P_{dc}} = \frac{I_{dc} Rg^2}{2V_{DD}} = \frac{Rg^2}{2R_{dc}} \tag{3.31}$$

To achieve 100% efficiency, the drain-to-source voltage, $v_1(0)$ and $v_1(\pi)$, must be zero. Because of the transient response of the capacitance, the slope of this voltage must be zero, that is, $dv(\theta)/d\theta = 0$ at $\theta = \pi$. The class-E PA does not depend on having a zero rise and fall time for a pulse.

$$\begin{aligned}
0 &= v_1(\pi) = \frac{I_{dc}}{B} \pi + \frac{a}{BR} \cos(\pi + \phi) - \frac{a}{BR} \cos(\phi) \\
&= \frac{I_{dc}}{B} \pi - \frac{2a}{BR} \cos \phi
\end{aligned} \tag{3.32}$$

$$\cos(\phi) = \frac{\pi}{2g} \quad (3.33)$$

To this is now added the constraint that the voltage slope is zero at $\theta = \pi$:

$$0 = \left. \frac{dv_1(\theta)}{d\theta} \right|_{\theta=\pi} = \frac{I_{dc}}{B} - \frac{a}{BR} \sin(\pi + \phi) \quad (3.34)$$

$$\sin(\phi) = \frac{1}{g} \quad (3.35)$$

So,

$$\tan(\phi) = \frac{\sin(\phi)}{\cos(\phi)} = -\frac{2}{\pi} \quad (3.36)$$

Therefore,

$$g = \frac{1}{2} \sqrt{4 + \pi^2} \quad (3.37)$$

For 100% efficiency

$$1 = \eta = \frac{Rg^2}{2R_{dc}} = \frac{1}{g}(4 + \pi^2) = 1.734R \quad (3.38)$$

This gives a relationship between the PA load resistance, R , and the dc power source voltage-to-current ratio.

$$R_{dc} = \frac{1}{\pi B} = R \frac{1}{8}(4 + \pi^2) \quad (3.39)$$

So,

$$B = \frac{8}{\pi R(4 + \pi^2)} \quad (3.40)$$

This represents the optimum total shunt susceptance that incorporates C_{DS} , the parasitic capacitance, and the additional circuit capacitance needed to provide 100% efficiency.

$$g(\phi, \psi) = \frac{2\cos(\phi + \psi) + \pi\sin(\theta + \psi)}{(\pi/2)\cos(\psi + 2\cos(\phi)\sin(\phi + \psi))} \quad (3.41)$$

$$\begin{aligned} & 2(\cos(\phi)\cos(\psi) - \sin(\phi)\sin(\psi)) + \pi(\sin(\phi)\cos(\psi) + \sin(\psi)\cos(\phi)) \\ &= g\left[\frac{\pi}{2}\cos(\psi) + 2\cos(\phi)(\sin(\phi)\cos(\psi) + \sin(\psi)\cos(\phi))\right] \end{aligned} \quad (3.42)$$

$$\tan(\psi) = \frac{2\cos(\phi) + \pi\sin(\phi) - \frac{g\pi}{2} - 2g\sin(\phi)\cos(\phi)}{2\sin(\phi) - \pi\cos(\phi) + 2g\cos^2(\phi)} \quad (3.43)$$

Substituting for $\cos(\phi)$, $\sin(\phi)$ and g gives

$$\tan(\psi) = \frac{\pi}{4}\left(\frac{\pi^2}{4} - 1\right) \quad (3.44)$$

so that

$$\psi = 49.052^\circ \quad (3.45)$$

since $\tan(\psi) = X/R$,

$$X = \frac{\pi}{4}\left(\frac{\pi^2}{4} - 1\right)R = 1.153R \quad (3.46)$$

This optimum series reactance must be inductive. It should be noted that in practice, the series resonant circuit absorbs this additional reactance, X , so the total output network does not operate at resonance when operating at maximum efficiency.

$$P_{dc} = I_{dc}V_{DD} = P_o = \frac{a^2}{2R} \quad (3.47)$$

$$V_{DD} = \frac{a}{4}\sqrt{4 + \pi^2} = 0.931a \quad (3.48)$$

In summary, the conventional design process for the maximum efficiency class-E PA begins with knowing the desired output voltage amplitude, a , and the load resistance R . The shunt susceptance, B the series reactance, X and the power supply voltage, V_{DD} , are found by using the respective equation derived above. The resonant tank circuit, L_o , and C_o must be of sufficiently high Q to block harmonic frequencies. The series Q is proportional to L_o , and the resonant frequency determines the capacitance. The value for L_1 is chosen to be high enough to provide a dc current with negligible ac content.

Under these conditions, the analytical design equations can also be derived and are given by [53]:

$$R_L = 0.5768 \cdot \frac{V_{DD}^2}{R_L} \quad (3.49)$$

$$C_1 = 0.1836 \cdot \frac{1}{\omega R_L} \quad (3.50)$$

$$L_x = 1.1525 \cdot \frac{R_L}{\omega} \quad (3.51)$$

where $\omega = 2\pi f$, and $f = 2.4$ GHz, V_{DD} and P_{out} are the operating frequency, supply voltage, and the desired output power, respectively. The combination of $L_2 = 0.34$ nH and $C_2 = 12.88$ pF forms a harmonic filter that is tuned to the operating frequency of the class-E PA. The major drawback of the class-E PA is the presence of high drain voltage when the switch is opened. This value is, in the ideal case, given by [54]

$$V_{DS,max} = 2\pi \left[\frac{\pi}{2} - \arctan\left(\frac{\pi}{2}\right) \right] \cdot V_{DD} \approx 3.562 \cdot V_{DD} \quad (3.52)$$

and the value of $V_{DS,max}$ threatens the transistor's reliability, especially in CMOS technology, due to its low breakdown voltage. The maximum drain voltage can be alleviated by using a finite inductance instead of RF-choke, whereby the peak voltage can be reduced to $2.5 \cdot V_{DD}$ [55]. This paper presents an analysis and design methodology on transformer-based class-E PA involving the circuit equations, the relationships among the transistors switching "on-off" and the load quality factor (Q) at the resonant frequency (f_o) of the load network, the essential performance, and design parameters are discussed in this paper as well. Experimental results are demonstrated, and they are in good agreement with the theories.

3.2 Methodology and Implementation on Transformer-Based Class-E PA

3.2.1 Design of the Inductors with Magnetic Coupling

The proposed transformer-based class-E PA with a finite DC-feed inductor is shown in Figure 3.3. The two coupled inductors (DC-feed and output series inductors) are inter-wound to form a transformer. The amount of coupling between the two inductors is quantified by defining a mutual magnetic coupling denoted as k , which can take on any value between one and zero. For the two coupled inductors (L_{DC} and $L_2 + L_X$), k and mutual inductance (M) are related by:

$$k = \frac{M}{\sqrt{L_{DC}(L_2 + L_X)}} \quad (3.53)$$

A simplified transformer model is shown in Figure 3.4. This is modeled as two inductors, but with the addition of k between them and inter-winding capacitance C_{IW} from input to output [56]. Note that the open-circle dots on inductors in Figure 3.3 are placed such that if current flows in the indicated direction, then there is a summation of magnetic fluxes [57]. Thus, the inductance reinforces itself, and for a given inductance, the designs of both the L_{DC} and $L_2 + L_X$ have shorter lengths (shortened approximately by 437 μm) which implies lesser series resistance R_S . This would allow a higher quality factor Q to manifest in the on-chip inductors, which translates to higher efficiency. In basic physics, the Q is defined as (3.54), where Z_{ind} is the impedance of the inductor.

$$\begin{aligned} Q &= 2\pi \frac{\text{Energy Stored}}{\text{Energy Dissipated per Cycle}} \\ &= \frac{|Im(Z_{ind})|}{|Re(Z_{ind})|} \\ &= \frac{\omega L}{R_S} \end{aligned} \quad (3.54)$$

Figure 3.3: Transformer-Based Class-E PA: magnetic coupling and determining correct dot placement.

Figure 3.4: Basic model of transformer.

According to Faraday's law of electromagnetic induction [58] states that the induced electromotive-force (ε) through a coil is equal to the negative of the time rate of change of the magnetic flux (ϕ_B):

$$\varepsilon = -\frac{d\phi_B}{dt} \quad (3.55)$$

The ϕ_B through the coil is proportional to the magnetic field (B), which in turn is proportional to the current I in the coil.

$$\phi_B \propto B \quad ; \quad B \propto I \quad \Rightarrow \quad \phi_B \propto I \quad (3.56)$$

From Equations (3.55) and (3.56), we conclude that the induced ε is proportional to the negative of the time rate of change of the current.

$$\varepsilon \propto -\frac{dI}{dt} \quad \Rightarrow \quad \varepsilon = -L\frac{dI}{dt} \quad (3.57)$$

where L is the inductance of the coil, for a given rate of change of the current, the induced back-emf increases with the inductance. Therefore, the inductance of a coil is a measure of its opposition to a change in current. Using Equation (3.57), we can express the inductance as:

$$L = -\frac{\varepsilon}{dI/dt} \quad (3.58)$$

Equating Equations (3.55) and (3.57)

$$\varepsilon = -\frac{d\phi_B}{dt} = -L\frac{dI}{dt} \Rightarrow \frac{d\phi_B}{dt} = \frac{dLI}{dt} \Rightarrow \phi_B = LI \quad (3.59)$$

Therefore, the inductance of a coil is also given by

$$L = \frac{\phi_B}{I} \quad (3.60)$$

3.2.2 Design of the DC-feed Inductance

There are two main reliability issues in the design of power amplifiers in submicron CMOS, namely oxide breakdown and the hot carrier effect. They increase the threshold voltage and consequently degrades the devices' performance. The critical property of class-E PA is the separation of drain voltage and drain current in the time domain. In this regard, high voltage and high current never coincide, and when the transistor starts to conduct current, the drain voltage is close to zero due to the load network. As such, the class-E PA is limited by the oxide breakdown but not the hot carrier effect. This will set limits for the maximum drain voltage equal to the oxide breakdown voltage of the NMOS transistor. A significant drawback is the maximum voltage stress on the transistor, $V_{DS,max}$, which can be as high as $3.57 \cdot V_{DD}$. Using a finite inductance instead of an RF-choke, the peak voltage can be reduced to $2.5 \cdot V_{DD}$, as shown in Figure 3.5 [55]. A common practice [59] is to keep the maximum voltage drop across the transistor below two times the nominal supply voltage ($V_{DDnom} = 1.2$ V) to ensure a reasonable device and circuit lifetime.

Figure 3.5: Maximum voltage stresses on transistor M1 in both on and off states.

The class-E PAs can be categorized into two types according to the inductor's function: Class-E PA with RF-choke inductor or with DC-feed inductor. The proposed PA with a finite DC-feed inductor is shown in Figure 3.3. Using a finite DC-feed inductor instead of a large RF-choke in the class-E PA has several advantages [60] including:

- Significantly reduce the loss due to a smaller electrical series resistance
- A reduction in overall size and cost
- Simplifying the design of the matching network

3.2.3 Design of Inductors and Transformers

Among all the passive structures used in RF circuits, high-quality inductors and transformers are the most difficult to realize monolithically. In silicon, they suffer from the presence of lossy substrate and high-resistivity metal. Therefore, well-designed inductors and transformers are very crucial, and they must exhibit the following properties [61]:

- Low series resistance in the primary and secondary windings
- High magnetic coupling between the primary and the secondary coils
- Low capacitive coupling between primary and the secondary coils
- Low parasitic capacitances to the substrate

To obtain an optimum design of monolithic transformer on silicon, we must follow carefully the suggestions and guidelines provided as follows:

1. To minimize the series resistance and the parasitic capacitance, the spiral is implemented in the top metal layer (which is the thickest) [62]
2. It is desirable to minimize the outer dimensions of inductors, and this can be accomplished by decreasing W (line width) or increasing N (numbers of turns) [63]
3. A diameter of 5 to 6 times W should be chosen for the inner opening to ensure negligible coupling [64]
4. Differential geometry (driven by differential signals) also exhibits a higher Q [65], because each half experiences its substrate loss and it will be reduced by a factor of two
5. Choose a line spacing S of approximately three times the minimum allowable value for the particular technology being used to fabricate the design
6. As a general rule of thumb, D_{in} (inner dimension) lower than $50\text{ }\mu\text{m}$ should be avoided unless it is mandatory to obtain very low inductance values ($L \leq 0.5\text{ nH}$) [66]
7. For multi-turn inductors, do not use very tight metal spacing (i.e., coil thickness/line spacing ≤ 3) to limit the performance degradation as this will cause the proximity effects to become worse [67]

ANSYS High-Frequency Structure Simulator (HFSS) was used to design and simulate the transformer structure and is shown in Figure 3.6. The primary inductor has an outer dimension of $187\text{ }\mu\text{m}$ and a thickness of $3.3\text{ }\mu\text{m}$ while the secondary inductor has an outer dimension of $122\text{ }\mu\text{m}$ and a thickness of $0.9\text{ }\mu\text{m}$. Both of them have a line width of $12\text{ }\mu\text{m}$. This geometry has better symmetry compared with traditional inductors (its S parameters look the same from either side).

Figure 3.6: Schematic of on-chip transformer 3-D view

3.2.4 Transformer Layouts in Class-E PA

Another important aspect is to choose an appropriate transformer configuration to maximize the coupling between coils. Only two types provide acceptable performance; stacked [68] and interleaved [68, 69] transformers. An interleaved transformer is built by two inductors fabricated using the same metal layer whose coils (i.e., metal layers) are laterally interleaved. The interleaved topology provides full symmetry but has a poor magnetic coupling. A stacked transformer is made up of two identical inductors fabricated using different metal layers placed on top of each other. Stacked topology gives higher coupling factors, but the two inductors have different electrical parameters due to different metal layers.

The main advantages and drawbacks of these two configurations are presented in Table 3.1. The magnetic coupling between winding is measured by the magnetic coupling factor (k), which is typically around 0.7–0.9 for a monolithic transformer due to poor confinement of the magnetic flux.

Table 3.1: Advantages and drawbacks of interleaved and stacked configurations.

Configurations	Area	k	f_{SR}	Capacitance	Electrical Symmetry
Interleaved	Medium	Medium	Excellent	Excellent	Excellent
Stacked	Excellent	Excellent	Medium	Poor	Medium

The stacked transformer is adopted in this design to increase the quality factor Q , but at the expense of increased capacitance to the substrate and a resultant decrease in self-resonant frequency. This technique is of benefit for small inductors for which the substrate loss is not dominant and the design is at low enough frequency, safely away from the self-resonant frequency. Note that the magnetic fluxes through the two windings will reinforce one another and the total inductance of the structure will be larger. As a result, the inductors will have a higher quality factor of Q . The quality factor Q of the coupled inductors (Q of $L_{DC} = 11.4$; Q of $L_2 + L_X = 16.1$) uncoupled Q of L_{DC} and $L_2 + L_X$ are about 10 as shown in Figure 3.7.

Figure 3.7: The quality factor plotted versus frequency for the inductors: (a) Coupling-inductors; (b) DC-feed inductor; (c) Output series inductor.

3.3 Measurement Results

The proposed methodology was implemented with a 2.4 GHz transformer-based class-E cascode PA fabricated in GLOBALFOUNDRIES' 65 nm CMOS process, and it occupies an area of $0.49 \times 0.43 \text{ mm}^2$ including the I/O pads. The microphotograph of the fabricated PA is shown in Figure 3.8 and the measurement results of the design, i.e., transformer-based class-E PA based on differential inductors topology, and conventional uncoupled class-E PA are illustrated in Figures 3.9 and 3.10, respectively. The simulation results are appended in the same figures as well.

Figure 3.8: Microphotograph of the implemented power amplifier.

Figure 3.9: Transformer-based class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey).

Figure 3.10: Uncoupled class-E PA: Output power, drain efficiency and power-added efficiency versus the dc supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey). Drain efficiency (DE) and power-added efficiency (PAE)

The measurements are performed for the PA using on-wafer probing with Agilent E4407B ESA-E spectrum analyzer and Cascade Elite 300 after cable loss calibration until the RF probe tips. The large-signal behavior of the PA is characterized by 1.2 to 3.4 GHz in steps of 0.1 GHz. All large-signal measurements are presented as the mean from 4 die samples with the inclusion of cable and probe loss of 1 dB.

In Figure 3.9 when $V_{DD} = 1.4$ V, the PA delivers an output power of 10-dBm, and maximum DE, and PAE were measured as 74% and 70% at a frequency of 2.4 GHz. Figure 3.11 shows the output power, DE and PAE over the range from 2.3 to 3.4 GHz. As can be seen in Figure 3.11, the output power is reduced by 4.8 dBm over the frequency range. This decrease hypothesizes that it could be due to the skin effect, which results in a higher series resistance at higher frequencies as well as the parasitic drain capacitance.

In the proposed design, the primary inductor has a rectangular copper line with a width of $12\ \mu m$, a thickness of $3.3\ \mu m$, and a total length of $2818\ \mu m$. To obtain the parasitic resistance of the line at dc at 2.4 GHz, it had been assumed that all current flows in regions that are of one skin depth from the surface. By assuming that copper has a resistivity of $1.72\ \mu\Omega \cdot cm$, a simple estimate used in this work to describe the resistance due to the skin effects is given by:

The skin depth at 2.4 GHz is :

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_o}} = \sqrt{\frac{1.72\ \mu\Omega \cdot cm}{\pi * 2.4\ GHz * 4\pi * 10^{-7}}} = 1.35\ \mu m \quad (3.61)$$

The resistance of copper at 2.4 GHz is hence:

$$R = \frac{\rho L}{Wt - (W - 2\delta)(t - 2\delta)} = \frac{1.72\ \mu\Omega \cdot cm * 2818m}{12\ \mu m * 3.3\ \mu m - 9.3\ \mu m * 0.6\ \mu m} = 1.42\ \Omega \quad (3.62)$$

Despite is just $1.42\ \Omega$, however, it could cause a power loss of about 2.5 dB. This is just one of the hypotheses to explain the discrepancies. Other factors that may be presence are the nearby currents that changes the magnetic flux in and around the copper line, hence causing mutual coupling between nearby copper lines. Also, the large signal model was not accounted for in the simulation and will contribute to the disparity.

The following Figure-of-Merit (FoM) [48] is used to compare the performance of the designed chip with state-of-the-art CMOS switch-mode PAs (SMPAs) [30, 48, 70–75]:

$$FoM = \frac{PAE \cdot freq\ [Hz]^{0.25}}{chip\ size\ [mm^2]} \quad (3.63)$$

Figure 3.11: Transformer-based class-E PA: Measured output power, drain efficiency and power-added efficiency versus operating frequency.

Due to its high efficiency (PAE = 70%) as shown in Figure 3.9 and compact size (die area = 0.21 mm²) including the I/O pads, the proposed design methodology implemented on this work, has an FoM of 735, which is the highest among all designs in comparison as shown in Table 3.2.

Table 3.2: Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM).

Reference	P_{out} [dBm]	PAE [%]	f [GHz]	Die Area [mm ²]	Process [nm]	FoM
[48]	28.7	48	2.3	1.2	90	121.74
[30]	5.7	55	2.4	1	130	100.37
[70]	30	60	2	0.3	65	423
[71]	31.5	51	1.8	1	130	111.23
[72]	29.6	51	1.8	1.5	180	70
[73]	21.7	37.9	2.6	1.21	250	70.7
[74]	22.3	49.5	5	0.235	250	560
[75]	29	38.7	1.8	1.53	350	52
[76]	21.5	41.1	1	0.318	180	229.8
[77]	1.4	51	2.45	0.17	130	667.4
This Work	10.7	70	2.4	0.21	65	735

3.4 Conclusions

In this chapter, we presented a proposed methodology on the design of the transformer-based class-E PA implemented in 65 nm CMOS technology. The class-E operating principles were reviewed, and the design is based on the transformer coupling effect to simultaneously reduce the chip area and improve the quality factor Q of the inductors. The methodology implemented allows the PA to deliver 10-dBm output power with 74% DE and 70% PAE at 2.4 GHz using the 65 nm CMOS process.

For a given combination of the supply voltage and the load resistance, the proposed design methodology delivers less power. Therefore, the proposed design methodology is not suitable for high power applications. The main advantages of the proposed methodology on the design of the transformer-based class-E PA are summarized below:

- The proposed design methodology does not require an RF-choke in the supply path, and hence the loss due to parasitic resistance is greatly reduced as well as less prone to supply parasitics. Moreover, the peak voltage across the transistor can be reduced to two and a half times the supply. .
- The proposed PA with magnetic coupling between the primary and the secondary coils of the transformer allows the same inductance to be realized in a smaller area, resulting in decreased impedance to dc while increased finite ac impedance.

Chapter 4

A Design Methodology and Analysis for Cascode Transformer-Based Class-E Power Amplifier

4.1 Background

Due to technology scaling, CMOS has become capable of operating at GHz frequencies. However, the dimension of the CMOS transistor gate will be scaled down proportionally. This will lead to a smaller transistor's on-resistance (r_{on}), which can reduce power loss and improve efficiency. In CMOS process, the r_{on} of an CMOS transistor in the triode region is given by [3]

$$r_{on} = \frac{1}{\mu_n C_{ox} W_g / L_g (V_{GS} - V_{th,n} - V_{DS}/2)} \approx \frac{1}{W_g} \quad (4.1)$$

The advancement of the CMOS technology, implying that the dimension of the transistor gate will be decreased by $1/\sqrt{2}$. Therefore, the r_{on} is also decreased by $\sqrt{2}$, and the supply voltage is reduced by the same factor of $\sqrt{2}$ as well. The reduction in the supply voltage will need the output resistance to be scaled down by a factor of two to obtain the same output power. Therefore, an impedance transformation technique is used to obtain sufficient output power at a low supply voltage, which will transform the impedance of the amplifier to a smaller value. However, losses will arise in the transformation network, and they are proportional to the impedance transformation ratio, resulting in a more significant impedance transformation with

lower efficiency. Some first-order calculations [50, 78] showed that the drain efficiency is

$$\eta = \frac{1}{1 + 1.4 \cdot \frac{r_{on}}{R_L}} \quad (4.2)$$

The advancement to a smaller tech-node will decrease the transistor r_{on} by $\sqrt{2}$. However, the output resistance needs to be reduced by two as well to achieve the same output power. Thus, the ratio r_{on}/R_L increase by $\sqrt{2}$. The ratio r_{on}/R_L it can also be expressed as r_{on}/V_{DD}^2 if similar output power to be obtained. Therefore transistor needs to be enlarged to keep the ratio r_{on}/R_L constant. However, the decrease in the optimum output load resistance R_L will strongly reduce the efficiency of the PA to achieve sufficient output power. There are two important issues in the design of power amplifiers in sub-micron CMOS processes, which are the oxide breakdown and hot carrier effect. The oxide breakdown will limit the maximum swing at the drain. At the same time, the hot carrier effect will increase the threshold voltage and degrade the performance of the device, causing reliability issues. To prevent the degradation due to hot carrier effect, the recommended drain-gate voltage must be lower than $2 * V_{DD_{nominal}}$ ($V_{DD_{nominal}} = 1.2V$). For a 65nm CMOS process, this leads to a reduced supply voltage. To maintain the same output power, one has to reduce the output impedance. However, this will increase the loss in the parasitic resistors in the matching network and the transistor.

Another technique to increase the output power is to do design a cascode PA [45] as shown in Figure 4.1. The V_{DD} is set to be twice the V_{nom} . Figure 4.2 shows the simulated V_{DS} versus time for both transistors M_1 and M_2 .

This approach is beneficial for transistors can only sustain a low voltage across it as a PA can be designed using a low supply voltage and still able to deliver an impressive output power. Also, the cascode transistors can obtain a high output power without the need for an impedance transformation circuit. If the V_{DD} is made to be twice the V_{nom} , the current will be reduced by a factor of 2. Hence, the power dissipation will be reduced by a factor of 4 and result in higher efficiency.

4.2 Methodology and Implementation on Transformer-Based Cascode Class-E PA

The proposed methodology implemented with a transformer-based cascode class-E PA is shown in Figure 4.1. Transistor M_1 and M_2 are the common source and common gate devices, respectively. In this way, the peak V_{DS} voltage is divided between the two transistors. The RF signal V_{IN} is applied to the gate terminal (V_{G1}) of M_1 . Gate terminal (V_{G2}) of M_2 is RF grounded with a dc value of V_{G2} . The dc voltage at the drain terminal (V_{D2}) of M_2 is equal to the power supply (V_{DD2}). At maximum output power, the voltage at node X swings down close to zero and up to 2.5 times V_{DD2} . In the cascode configuration, this enables the proposed cascode class-E PA to have the same maximum V_{DG} , which will enable a larger signal swing at X before entering the hot carrier degradation regime. This will enable us to apply a larger V_{DD} , which can boost the output power.

From the reliability perspective of a cascode topology, the biasing voltage of V_{DS2} is to minimize the voltage drops across the oxide of M_1 and M_2 , V_{DG1} and V_{DG2} , respectively. And the value of V_{G2} and V_X must be designed carefully to guarantee V_{DS2} and V_{DG2} remain below $1.25*V_{DD2}$ at all times as demonstrated in Figure 4.2.

$$V_{DS2} = 2.5 * V_{DD2} - (V_{G2} - V_{th2}) \quad (4.3)$$

$$V_{DG2} = 2.5 * V_{DD2} - V_{G2} \quad (4.4)$$

Figure 4.1: Schematic of the proposed transformer-based cascode class-E PA.

Figure 4.2: Drain voltage waveforms of common-gate (M_2) and common-source (M_1) transistors of class-E PA based on a cascode topology

From equations (4.2) and (4.3), we can write respectively,

$$2.5 * V_{DD2} - (V_{G2} - V_{th2}) \leq 1.25 * V_{DD2} \quad (4.5)$$

$$2.5 * V_{DD2} - V_{G2} \leq 1.25 * V_{DD2} \quad (4.6)$$

The former (i.e., equation (4.4)) is a stronger condition and can be reduced to

$$1.25 * V_{DD2} \leq (V_{G2} - V_{th2}) \quad (4.7)$$

For the proposed cascode topology, the $V_{G2} = 2.4V$, leading to a maximum device stress of V_{DG1} and $V_{DG2} = 1.9V$. With the body effect, V_{th2} may reach 0.5V in 65-nm technology, therefore the $V_{DD2} = 1.7V$. Table 4.1 shows maximum V_{GS} , V_{DS} and V_{GD} when the M_1 and M_2 is on and off respectively.

Table 4.1: Maximum V_{GS} and V_{DS} stresses on M_1 and M_2 in both on and off states.

		$V_{GS_{max}}$	$V_{DS_{max}}$	$V_{GD_{max}}$
M_1	ON	V_{IN}	0	V_{IN}
	OFF	0	$V_{G2} - V_{th2}$	$V_{G2} - V_{th2}$
M_2	ON	V_{G2}	0	V_{G2}
	OFF	V_{th2}	$2.5 * V_{DD2} - V_{G2} + V_{th2}$	$2.5 * V_{DD2} - V_{G2}$

The design parameters of the class-E PA ($L_{DC}, L_2, L_X, C_1, \text{and } C_2$) are unaffected by the supply voltage. Therefore there is no change if an increase in the supply voltage of the class-E PA. Although the increase in V_{DD} increases the output power, the efficiency of the PA is unaffected by the supply voltage. The only drawback is the output resistance of the class-E PA, which will affect the design of the capacitors and inductors adversely. If the V_{DD} is followed as:

$$V_{DD}^{new} = \sqrt{\frac{R_L^{new}}{R_L}} \cdot V_{DD} \quad (4.8)$$

Figure 4.3 shows the shunt capacitance against load resistance. The P_{out} is depicted by the solid line in Figure 4.4 can be seen to decrease while the efficiency increases as the current flowing through the transistor is reduced. The dc current against the power loss is given in Figure 4.5, and the output power stays constant as depicted by the dotted line in Figure 4.4.

Figure 4.3: Shunt capacitance against the load resistance

Figure 4.4: Output power against the load resistance

Figure 4.5: DC-feed current against the power loss

The selection of the on-resistance (when the CMOS transistor is in the turn-on state) will be significantly affected by the reduction of the required shunt capacitance, as it reduces the maximum width of the transistor. However, it will also reduce the current, which will result in a similar efficiency.

The parasitic drain capacitance for cascode devices are not well studied. The work by T. Sowlati and D. Leenaerts et. Al [79], as shown in Figure 4.6, demonstrated that the lower transistor acts as the switch while the transistor at the top divides the voltage swing across the cascode devices in order to maintain the performance of the PA. And the total parasitic drain capacitance can be shown as:

$$C_d = \frac{1.9pF}{1000um} \cdot W_g \quad (4.9)$$

including the parasitic interconnect parasitic capacitance from the two transistors, the total resistance of the transistors will also be doubled, since two transistors are connected in series and thus

$$r_{on} = 2 \cdot 1000\mu m \cdot 0.550\Omega \cdot \frac{1}{W_g} \quad (4.10)$$

Figure 4.6: Class-E PA with two stacked transistors

The performance of the power amplifier against the total r_{on} of the cascode transistors will limit the applications of the cascode configuration for class-E PA. Also, it will put less stress on the impedance transformation network as the resistance of the load is four times as large when compared to a single transistor.

Therefore, using a cascode topology to achieve higher P_{out} will double the supply voltage while the value of the shunt capacitance and the load resistance remains unchanged. Due to the lower parasitic drain capacitance of the cascode topology, the transistor width would be higher than the one shown in Figure 3.1 it can be shown that the cascading of FETs helps to increase the efficiency of the impedance transformation network and the efficiency of the PA. However, a higher V_{DD} will result in a more significant value in the load resistance and a smaller value in the shunt capacitance with a similar P_{out} . Hence, cascode topology with a large number of transistors will increase the design footprint and degrade the performance.

4.3 Measurement Results

The proposed methodology was implemented with a 2.4 GHz transformer-based cascode class-E PA fabricated in GLOBALFOUNDRIES' 65 nm CMOS process, and it occupies an area of $0.49 \times 0.43 \text{ mm}^2$ including the I/O pads. The microphotograph of the fabricated PA is shown in Figure 4.7 and the measurement results of the design, i.e., transformer-based class-E PA based on cascode topology is illustrated in Figures 4.8

Figure 4.7: Microphotograph of the implemented power amplifier.

Figure 4.8: Transformer-based cascode class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage

The measurements are performed for the PA using on-wafer probing with Agilent E4407B network analyzer and Cascade Elite 300. The large-signal behavior of the PA is characterized from 1.2 to 3.4 GHz in steps of 0.1 GHz. All large-signal measurements are presented as the mean from 4 die samples with the inclusion of cable and probe loss of 1 dB.

In Figure 4.8 when $V_{DD} = 2.2$ V, the PA delivers an output power of 15-dBm, and maximum DE and PAE were measured as 77% and 80% at a frequency of 2.4 GHz.

Due to its high efficiency (PAE = 77%) as shown in Figure 4.8 and compact size (die area = 0.21 mm^2) including the I/O pads, the proposed design methodology implemented on this work, has an FoM of 735, which is the highest among all designs in comparison as shown in Table 4.2.

Table 4.2: Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM).

Reference	P_{out} [dBm]	PAE [%]	f [GHz]	Die Area [mm ²]	Process [nm]	FoM
[48]	28.7	48	2.3	1.2	90	121.74
[30]	5.7	55	2.4	1	130	100.37
[70]	30	60	2	0.3	65	423
[71]	31.5	51	1.8	1	130	111.23
[72]	29.6	51	1.8	1.5	180	70
[73]	21.7	37.9	2.6	1.21	250	70.7
[74]	22.3	49.5	5	0.235	250	560
[75]	29	38.7	1.8	1.53	350	52
This Work	15	77	2.4	0.21	65	753

4.4 Conclusions

In this paper, we presented a proposed methodology on the design of a transformer-based cascode class-E PA implemented in 65 nm CMOS technology. The class-E operating principles were reviewed, and the design is based on the transformer coupling effect to simultaneously reduce the chip area and improve the quality factor Q of the inductors. The methodology implemented allows the PA to deliver 15-dBm output power with 80% DE and 77% PAE at 2.4 GHz using the 65 nm CMOS process.

Chapter 5

A Design Methodology and Analysis for Transformer-Based Differential Class-E Power Amplifier

5.1 Background

The class-E PA has up to 100% RF efficiency as the current and voltage are shaped in such a way that they do not superimpose, and harmonic frequencies generate a negligible amount of energy due to the series-tuned resonant circuit ($C_2 - L_2$). To obtain a larger P_{out} , the larger transistors with an inherent capability to handle higher power are discussed. However, the relatively large parasitic capacitance of CMOS will ultimately increase the design footprint. The parasitic capacitance at the gate needs to be charged and discharged periodically; therefore, increasing in the transistor width will increase the power dissipation of the driver stages. Consequently, it will correspond to an optimal transistor width to achieve maximum overall efficiency. Therefore, the maximum transistor width will be limited by the parasitic drain capacitance. For designing a class-E PA, the parasitic capacitance of the drain can be integrated by the shunt capacitance (C_1) of the class-E output network, which poses as an advantage compared to other classes of PAs design. The width of the NMOS is constrained by the required shunt capacitance, where at high frequencies is typically smaller than the actual output capacitance of a large device. Apart from the cascode techniques. Alternatively, differential techniques can also be applied.

5.2 Methodology and Implementation on Transformer-Based Differential Class-E PA

In section 3.3.2, it has been shown that the DC-feed inductance can improve the efficiency and performance of the class-E PA but causing a downside of a sizeable current swing across the DC-feed inductance as shown in Figure 5.1, which is incurred by the voltage supply. The V_{DD} unable to provide such a high frequency alternating current. This can be resolved by having some large decoupling capacitors deployed close to the chip packaging. However, this demand for a very high Q capacitor which will resonate at a higher frequency compared to the operating frequency. The issue with such off-chip capacitors is that they will form a series path with the parasitic inductors of the bond wires.

Figure 5.1: Current flowing in the DC-feed inductance.

The issue of the alternating currents can be solved by using a differential structure. For the operation, two PAs are placed adjacent to one another in a parallel configuration and are regulated by an input voltage that is entirely out of phase in the time domain. If the supply currents are mirrored, the current flowing through the voltage supply will be approximated to

DC, as shown in Figure 5.2.

Figure 5.2: A differential technique to limit current swing.

Increase the size of the output PA transistor will enhance the output power; however, the impedance will be lowered to reach a point whereby it will require complex and large impedance transformer to transform to $50\ \Omega$. Another way is to employ a differential structure to increase the output power [2]. The signal is split into two anti-phase voltages using a passive network such as a balun or transformer and then merged again at the PA output.

With this structure, we can gain an output power of almost four times for a given load. However, there are losses in the splitting and merging of passive components, but this way is still easily achievable.

The differential structure has a virtual ground, which reduces the number of bond wires needed, and it can lead to a good cancellation of even harmonics. The differential PA can be obtained using an LC balun [80], and the concept illustrated in Figure 5.3 can be extended to a multitude of 1-to-1 transformers to obtain a greater R_L/R_{in} ratio. Figure 5.3 shows a 2.4 GHz

differential transformer-based class-E PA. Each transformer is realized as an on-chip coupled inductors (DC-feed and output series inductors) are inter-wound to form a transformer. The DC-feed inductor has an outer dimension of $207\ \mu\text{m}$ and a thickness of $3.3\ \mu\text{m}$ while the output series inductor has an outer dimension of $142\ \mu\text{m}$ and a thickness of $0.9\ \mu\text{m}$. Both of them have a line width of $12\ \mu\text{m}$ to handle large currents with small resistance. This geometry has better symmetry compared with traditional inductors (its S parameters look the same from either side).

Figure 5.3: Schematic of the proposed transformer-based Differential class-E PA.

Differential circuits can be used as a single symmetric inductor rather than two asymmetric inductors, as shown in Figure 5.4. The symmetric inductor also has an advantage in terms of area reduction. Note that a pair of differential signals drive the class-E PA. Thus, the inductance reinforces itself, and for a given inductance, the shape of the symmetric inductor has a shorter length, which offers a smaller series resistance. This results in a higher Q factor and also enhance the output power and efficiency.

Figure 5.4: Symmetric inductor in a differential topology.

The presence of currents around a region will induce a magnetic flux in and around the conductors. This will result in a mutual coupling effect between them, which is also termed as proximity effect [81, 82]; at high frequency, the current through a conductor prefers to flow at the surface. If the overall current is viewed as many parallel current components, these components tend to repel each other, migrating away to create maximum distance between them. This trend is illustrated in Figure 5.5. Flowing through a smaller cross-section area, the high-frequency current thus faces a higher resistance. The actual distribution of the current follows an exponential decay from the surface of the conductor inwards, $J(s) = J_0 \exp(-s/\delta)$, where J_0 denotes the current density (in A/m^2) at the surface, and δ is the "skin depth." The value of δ is given by

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad (5.1)$$

where f denotes the frequency, μ the permeability, and σ the conductivity, for example, $\delta \approx 1.4 \text{ um}$ at 10 GHz for aluminium. The extra resistance of a conductor due to the skin effect is equal to

$$R_{skin} = \frac{1}{\sigma \delta} \quad (5.2)$$

Parallel spirals can reduce this resistance if the skin depth exceeds the sum of the metal thicknesses.

Figure 5.5: Current distribution in a conductor at (a) low and (b) high frequencies.

In a spiral inductor, the proximity of adjacent turns results in a complex current distribution. As illustrated in Figure 5.5, the current may concentrate near the edge of the wire. To understand this "current crowding" effect, consider the more detailed diagram shown in Figure 5.6, where each turn carries a current of $I(t)$ [81, 82]. The current in one turn creates a time-varying magnetic field, B , that penetrates the other turns, generating loops of current (i.e. eddy currents) according to Faraday's law states that the voltage induced in a conducting circuit is proportional to the time derivative of the magnetic field, these components add to $I(t)$ at one edge of the wire and subtract from $I(t)$ at the other edge. Since the induced voltage increase with frequency,

the eddy currents, and hence the nonuniform distribution, become more prominent at higher frequencies.

Figure 5.6: Current distribution in adjacent turns.

Two cases will be discussed and compared here, as shown in Figure 5.7 and Figure 5.8. One with the current through parallel conductors to flow in the opposite direction while the other case is current through a series of conductors to flow in the same direction

For the first example, the interaction and resultant of the magnetic fields due to the two currents will be partially canceled and hence, reduced the inductance of each of the wires. The structure is shown in Figure 5.7.

Figure 5.7: Two adjacent metal placed in series.

The other example shows that when two metal traces in a parallel configuration, is depicted in Figure 5.8. Because of the parallel nature, the magnetic flux density of the two conductors will be reinforced if they are proximity to each other.

Figure 5.8: Two adjacent metal, placed in parallel.

5.3 Measurement Results

The proposed methodology was implemented with a 2.4 GHz transformer-based differential class-E PA fabricated in GLOBALFOUNDRIES' 65 nm CMOS process, and it occupies an area of $0.89 \times 0.43 \text{ mm}^2$ including the I/O pads. The microphotograph of the fabricated PA is shown in Figure 5.9 and the measurement results of the design, i.e., transformer-based class-E PA based on cascode topology is illustrated in Figures 5.10

Figure 5.9: Microphotograph of the implemented power amplifier.

Figure 5.10: Transformer-based differential class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage

The measurements are performed for the PA using on-wafer probing with Agilent E4407B network analyzer and Cascade Elite 300. The large-signal behavior of the PA is characterized by 1.2 to 3.4 GHz in steps of 0.1 GHz. All large-signal measurements are presented as the mean from 4 die samples with the inclusion of cable and probe loss of 1 dB.

In Figure 5.9 when $V_{DD} = 1.4$ V, the PA delivers an output power of 17-dBm, and maximum DE and PAE were measured as 54% and 57% at a frequency of 2.4 GHz, and in Figure 5.10 the constant drain efficiency (DE) and PAE obtained within a wide range of supply voltage give an indication of increase or decrease the supply voltage will not change the value of the passive components of the proposed Class-E PA. The efficiency of the PA will be independent of the supply voltage, although the output power increases or decreases with the power supply.

Table 5.1: Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM).

Reference	P_{out} [dBm]	PAE [%]	f [GHz]	Die Area [mm ²]	Process [nm]	FoM
[48]	28.7	48	2.3	1.2	90	121.74
[30]	5.7	55	2.4	1	130	100.37
[70]	30	60	2	0.3	65	423
[71]	31.5	51	1.8	1	130	111.23
[72]	29.6	51	1.8	1.5	180	70
[73]	21.7	37.9	2.6	1.21	250	70.7
[74]	22.3	49.5	5	0.235	250	560
[75]	29	38.7	1.8	1.53	350	52
This Work	17	54	2.4	0.21	65	753

5.4 Conclusions

In this paper, we presented a proposed methodology on the design of a transformer-based differential class-E PA implemented in 65 nm CMOS technology. The class-E operating principles were reviewed, and the design is based on the transformer coupling effect to simultaneously reduce the chip area and improve the quality factor Q of the inductors. The methodology implemented allows the PA to deliver 17-dBm output power with 57% DE and 54% PAE at 2.4 GHz using the 65 nm CMOS process.

Chapter 6

Conclusion

The class-E PA functionality and challenges in the CMOS process were studied and were found that it can be well integrated with the parasitic drain capacitance from the CMOS transistor as compared to other classes of PAs. A design methodology implemented on a transformer-based class-E PA in different topologies (single-ended, cascode, and differential) were proposed in chapter 3, 4, and 5, respectively.

In chapter 3, the effect of electromagnetic effect was studied and implemented into the transformer design. And a comparison between DC-feed and RF-choke inductor were discussed to enhance the efficiency and output power of the class-E PA. Subsequently, the alternative transformer geometries (stacked and interleaved) were compared and found that the stacked geometry is preferable for the transformer-based class-E PA design due to the high magnetic coupling effect. And the reliability issues of the class-E PA are mainly due to the

- junction breakdown in the transistor due to high electric-field across the gate terminal
- hot-carrier effect arising from the ionization of the electrons penetrated through the gate oxide
- gate oxide breakdown

In this regard, the voltage across the gate-to-drain, gate-to-source, and drain-to-source need to be kept within a safe range, and a transformer-based class-E PA design was realized in CMOS 65 μm process.

In chapter 4, the cascode topology was proposed and implemented on the transformer-based class-E PA to improve the output power and efficiency further. Whereas, in chapter 5, a differential topology was introduced to enhance the performance of the class-E PA due to its good second harmonics frequencies cancellation.

6.1 Recommendations for Future Work

Class-E PA indeed does achieve a high efficiency, but the amplitude linearity is completely lost in this amplifier. Polar modulation is suggested to combine both efficiency and linearity in a fully integrated CMOS class-E PA. This technique offers two key advantages that allow a high efficiency: (1) it can operate with an arbitrarily nonlinear output stage, and (2) it does not require an output combiner (e.g., the subtractor in the feedforward topology).

Polar modulation uses a nonlinear RF amplifier and a linear low-frequency amplifier that delivers the supply voltage of the nonlinear RF amplifier. This technique results in an efficient RF amplifier since the efficiency of the class-E amplifier is independent of the supply voltage, even if the losses of the inductors and the loss of the switch are included. Changing or modulating the supply voltage of a nonlinear amplifier is denoted as polar modulation and will be studied in the future.

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1. Lim, A.; Tan, A.; Kong, Z.-H.; Ma, K. A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier. *Electronics* 2019, 8, 494.
2. Tan, A.; Toh, R.T.; Lim, A.; Li, Y.; Kong, Z.H. A Simplified Methodology to Evaluate Circuit Complexity: Doherty Power Amplifier as a Case Study. *Electronics* 2019, 8, 313.

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1. A. Lim, K. Ma, Z. H. Kong and K. S. Yeo, "Transformer-based class-E CMOS PA with shunt LC network," 2015 International SoC Design Conference (ISOCC), Gyungju, 2015, pp. 205-206.
2. Alfred Lim, Kaixue Ma, and Yeo Kiat Seng, "Transformer-Based Class-E CMOS Power Amplifiers", 4th IEEE International Symposium on Next-Generation Electronics (IEEE ISNE 2015), May, 2015.