A study of wireless inter-chip interconnect

Chen, Zhiming

2008

Chen, Z. (2008). A study of wireless inter-chip interconnect. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/14559>

<https://doi.org/10.32657/10356/14559>

A Study of Wireless Inter-Chip Interconnect

Chen Zhiming

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2008

Acknowledgements

I would like to acknowledge many people for their assistance and support during my doctoral programme, both technical and moral.

First of all, I would like to express the deepest gratitude to my advisor, Dr. Zhang Yueping, for years of patient guidance, inspiring suggestions, and persistent support. Without his assistance and encouragement, this thesis could not have been completed. I also would like to thank Dr. Hu Aiqun, from Southeast University, China, for having inspiring discussions.

I would like to acknowledge technical staff: Sia Liang Poo, Jimmy, and William of Centre for Integrated Circuits and Systems, Kang Meng Fai, Lim-Tan Gek Eng, and David of Integrated System Research Lab, Leong-Tan Min Lin and Seow-Guee Geok Lian of IC Design II, and Toh Kai What and Lim Cheng Chye of Communication Research I, for providing support and convenience during my research programme.

Also I would like to thank friends of my team: Dr. Wang Jun Jun, Dr. Sun Mei, Dr. Li Qiang and Mr He Jin, for their invaluable advice and technical discussions.

Last, I would like to thank my family for their endless love, patience, understanding and encouragement over all the years. Without their support, this thesis is not possible.

Table of Contents

Acknowledgements	i
Table of Contents	iii
Summary	vii
List of Figures	xi
List of Tables	xvii
List of Abbreviations	xix
1 Introduction	1
1.1 Background and Motivations	1
1.1.1 Traditional Wire Interconnect	1
1.1.2 Wireless Interconnect	5

1.2	Objectives	12
1.3	Major Contributions of the Thesis	12
1.4	Organization of the Thesis	13
2	Literature Review	16
2.1	RF Interconnect	16
2.2	Characteristics of Integrated Antennas	18
2.3	Intra- and Inter-Chip Clock Distribution	28
2.4	Intra- and Inter-Chip Data Communication	32
3	Measurement, Characterization and Modeling of Wireless Inter-chip Channel	33
3.1	Introduction	33
3.2	UWB Inter-Chip Channel Measurement	36
3.2.1	Channel Measurement Techniques	36
3.2.2	Equipment	38
3.2.3	Procedures	42
3.3	Data Processing and Result Analysis	44
3.3.1	Large-Scale Analysis	46

3.3.2	Small-Scale Analysis	50
3.4	Model Implementation, Simulation and Verification	56
4	Propagation Mechanism of Radio Waves over Intra-chip Channels	60
4.1	Introduction	60
4.2	Frequency-Domain Measurement	63
4.2.1	Integrated Monopoles and Testing Vehicles	63
4.2.2	Measurement Setup and Frequency-Domain Results	66
4.3	Time-Domain Analysis	71
4.3.1	Path Loss	73
4.3.2	Delay Spread	76
4.3.3	Propagation Mechanisms	77
5	BER Analysis of UWB Radio Using BPSK Modulation over Inter-chip Radio Channels	80
5.1	Introduction	80
5.2	System Description	83
5.3	ISI Reduction	86
5.4	BER Analysis Over Inter-Chip Channels	94

6	Synchronization Scheme for Impulse-Based UWB	103
6.1	Introduction	103
6.2	Analysis of the Synchronization Scheme	107
6.2.1	Basic Properties of Gaussian Pulse	107
6.2.2	Synchronization Scheme	111
6.2.3	Tradeoffs of Gaussian Pulse Order	120
6.3	Effects of Antennas and Channels	122
6.3.1	Calculation of the Received Pulse with Antennas and Freespace Channel	122
6.3.2	Impairments of Antennas and the Freespace Channel on a Re- ceived Pulse	124
6.3.3	Effects of UWB Multipath Channels	125
7	Conclusions and Recommendations	130
7.1	Conclusions	130
7.2	Recommendations	134
	Author's Publications	137
	Bibliography	139

Summary

In semiconductor industry, device feature dimension has been continuously scaled down to reduce device size and to improve circuit performance. In parallel with the device feature dimension down scaling, the width and thickness of wire interconnect have been reduced. On the other hand, to integrate more functions together, chip size continues growing. Therefore, the down-scaled wire interconnect has to route over an ever increasing chip area, implying degraded interconnect performance. As a matter of fact, performance of interconnects rather than device has become a bottleneck of ICs system performance. With improved radio frequency silicon technologies and higher-degree integration, wireless interconnect, which realizes wireless communications among cores within a chip or different chips within a module, is a viable candidate for solving problems in future generations of interconnects.

As a critical part of wireless inter-chip communications, inter-chip wireless channel has been measured, analyzed, and modeled. The wireless inter-chip channel is sampled in frequency domain inside a computer casing on a laboratory workbench. To convert data from frequency domain to time domain, a novel technique for doubling the time-

domain resolution has been proposed using the inverse discrete Fourier transform. In large-scale analysis, it is found that the path loss factor is less than two for a closed computer casing and greater than two when the casing is open. In small-scale analysis, energy in local-area movement is observed with Lognormal distribution as the best-fitted one. With the obtained model parameters in both large- and small- scale analyses, the wireless inter-chip channel is implemented.

Propagation mechanism of radio waves over intra-chip channels has been studied. The intra-chip channel is sampled in frequency domain from 10 to 110 GHz with a network analyzer and analyzed in time domain. It is found that the path loss factor is constantly less than two and the propagation delay of the first-arrival wave is significantly longer than that by free-space transmission. It is concluded that the propagation of radio wave over an intra-chip channel is mainly carried out with the surface wave on the air-wafer interface instead of the space wave.

Bit-error rate (BER) performance of the inter-chip wireless channel has been studied with the binary phase-shift keying (BPSK) modulation scheme. A technique to reduce the inter-symbol interference (ISI) is proposed by dynamically shifting the integral window position at a receiver. Analytical BER expressions are derived and verified with Monte Carlo simulations. It is found that data communication over inter-chip channels with a BER less than 10^{-6} is feasible for a distance up to 252 mm with a data rate 650 Mbps. Besides, link margin analysis shows that a link margin of 28.22 dB can be obtained.

A synchronization scheme has been designed for the ultrawide band (UWB) radio over wireless inter-chip channels. The synchronization scheme consists of two feedback loops: a sliding correlator and a phase-locked loop (PLL). Properties of Gaussian group pulses are explored as rationales of the synchronization scheme. Tradeoffs on selecting Gaussian pulse orders are discussed according to difficulty in circuit implementation and superiority in system performance.

List of Figures

1.1	Block diagram for intra-chip wireless interconnect.	9
1.2	Block diagrams of wireless inter-chip interconnect: (a) wireless inter-chip interconnect inside a MCM package and (b) wireless inter-chip interconnect for chips in different packages.	10
2.1	Inter-chip RF interconnect system inside the MCM package.	17
2.2	Wave components for on-chip antennas (layers not drawn to ratio). . .	21
3.1	Measured S_{11} of UWB antenna over frequency.	38
3.2	UWB antenna radiation patterns: (a) and (b) E plane co- and cross- polarization respectively; (c) and (d) H plane co- and cross- polarization respectively. Thick, normal and thin lines are for frequencies 3.5, 6.85 and 10.0 GHz respectively in each plot.	39

3.3	UWB antenna normalized transfer function and group delay: Top, normalized transfer function; bottom, group delay.	40
3.4	Measurement setup for channel in a computer casing.	41
3.5	Measurement snapshot.	43
3.6	Measurement points on motherboard.	43
3.7	NLOS received power for computer casing closed.	45
3.8	Path loss fitting of inter-chip channel.	48
3.9	Decay rates over distance.	49
3.10	Small scale distribution of inter-chip channel, casing closed.	51
3.11	Fitting of first bin into Lognormal distribution, casing closed.	52
3.12	Small scale distributions, casing open.	53
3.13	Fitting of first bin into Lognormal distribution, casing open.	53
3.14	Fitting of μ into Normal distribution, casing closed.	54
3.15	Fitting of σ into Normal distribution, casing closed.	55
3.16	Fitting of μ into Normal distribution, casing open.	56
3.17	Fitting of σ into Normal distribution, casing open.	57
3.18	(a):Generated small scale PDPs for casing closed. (b):Experimental small scale PDPs for casing closed.	58

3.19	Comparison between experimental and generated CDF of received power.	59
4.1	Cross-sectional and top views (not to scale) for integrated zigzag, linear and meander antennas on silicon wafer.	64
4.2	Die photo of a test vehicle using 0.18 μm process.	65
4.3	Setup for frequency domain measurement of on-chip monopoles. . . .	66
4.4	Measured S_{11} versus frequency for meander antennas.	68
4.5	Magnitude and phase responses of S_{21} for the zigzag antenna pairs at $d = 5\text{mm}$	69
	(a) High resistivity substrate	69
	(b) Low resistivity substrate	69
4.6	Effect of metal interference structures on the magnitude of S_{21} of linear antenna pairs at $d = 5\text{ mm}$	70
4.7	Magnitude responses of S_{21} for zigzag antennas at $d = 10\text{ mm}$	70
4.8	Received power delay profile of the zigzag antenna pairs at $d = 5\text{ mm}$: (a) High resistivity substrate (b) Low resistivity substrate.	73
4.9	PL versus log distance for zigzag, meander and linear monopole antennas.	74

4.10	Delay spread versus the separation distance between the transmitting and receiving antennas.	77
4.11	Scatter and fitted lines for first arrival locations over distance.	78
5.1	The block diagram for an inter-chip wireless communications system.	83
5.2	An example for effects of ISI.	89
5.3	$Z_{j,r}(\tau_{sh})$ over time shift τ_{sh} for the j th pulse as ‘0’ and ‘1’. τ_{sh} is in the unit of T_f	90
5.4	$Z_{j,r}(\tau_{sh})$ over time shift τ_{sh} for the j th pulse as ‘1’. τ_{sh} is in the unit of T_f . The vertical dashed line represents $\tau_{sh,opt}$	92
5.5	Flow chart for $\tau_{sh,opt}$ searching.	93
5.6	Theoretical BER plot (solid line) and Monte Carlo verification (solid dot) at T-R separation 228 mm.	98
5.7	Switching noise measurement setup.	98
5.8	BER over E_{TX}/N_0 over different distances with a data rate at 650 Mbps. The T-R distances are: 62, 84, 133, 156, 162, 208, and 252 mm.	100
5.9	BER over E_{TX}/N_0 over different data rates with T-R separation as 235 mm. Data rates: 450, 500, 550, 600, 650, and 700 Mbps.	101
6.1	The normalized temporal waveform of a G5 pulse.	108

6.2	$R_{55}(\tau)$: normalized auto-correlation of G5; solid horizontal line: $R_{55,th}$.	109
6.3	$R_{56}(\tau)$: the normalized cross-correlation of G5 and G6. Vertical lines: τ_e region of interest from -100 ps to $+100$ ps.	110
6.4	The values of τ_e and τ_m of Gaussian pulses from order 1 to 14.	112
6.5	Block diagram for the synchronization scheme in an IR-UWB system.	113
6.6	Sampling time for the S/H block in frequency synchronization (not drawn to ratio).	118
6.7	Effect of sampling time on synchronization performance during lock- ing. Thick line: sampling at t_2 ; thin line: sampling at $t_2 + 2T_c$	119
6.8	The transmitted and received temporal G5 pulse with effects of an- tennas and the freespace channel. Solid curve: the transmitted pulse; dashed curve: the received pulse.	124
6.9	Transmitted and received G5 pulse with effects of antennas and IEEE UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 40 ns.	126
6.10	Transmitted and received G5 pulse with effects of antennas and BAN UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 20 ns.	128

- 6.11 Transmitted and received G5 pulse with effects of antennas and inter-chip UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 40 ns. 129

List of Tables

- 1.1 Interconnect Latency ($d = 1$ mm) at Different Technology Generations . 4

- 3.1 Path Loss Parameters. 47
- 3.2 Parameters for Decay Rates over Distance. 49

- 4.1 PL Parameters for Antennas. 74
- 4.2 Effects of Interference Structures on PL for Antennas. 75
- 4.3 Effect of Rotation on PL in dB θ (degrees). 76

List of Abbreviations

3D	Three dimensional
AWGN	Additive white Gaussian noise
BAN	Body area network
BER	Bit-error rate
BPSK	Binary phase-shift keying
CCI	Capacitive-coupled interconnect
CDMA	Code-division multiple access
CIR	Channel impulse response
CMOS	Complementary metal oxide semiconductor
CPW	Coplanar waveguide
DCI	Direct-coupled interconnect
DFT	Discrete Fourier transform
DLL	Delay-locked loop
DS	Direct sequence
EIRP	Effective isotropic radiated power
FCC	Federal Communications Commission
FDMA	Frequency-division multiple access
FT	Fourier transform

G2	Gaussian second derivative
G5	Gaussian fifth derivative
ICs	Integrated Circuits
IDFT	Inverse discrete Fourier transform
IFT	Inverse Fourier transform
iid	Independent and identically-distributed
IIS	Inductive inter-chip signalling
IR	Impulse radio
ISI	Inter-symbol interference
LAN	Local area network
LNA	Low-noise amplifier
LOS	Line-of-sight
LPF	Low-pass filter
MB	Multi-band
MCM	Multi-chip module
MF	Matched filter
ML	Maximum likelihood
MLE	Maximum likelihood estimator
MTL	Microstrip transmission line
MUX	Multiplexer
NF	Noise figure
NLOS	Non-LOS
OFDM	Orthogonal frequency-division multiplexing
PD	Phase-detector
PDP	Power delay profile
PG	Pulse generator

PLL	Phase-locked loop
PN	Pseudo noise
PPM	Pulse-position modulation
PSD	Power spectral density
RF	Radio frequency
RFI	RF interconnect
S/H	Sample-and-hold
SNR	Signal-to-noise ratio
SoC	System-on-chip
SOI	Silicon on insulator
SOS	Silicon on sapphire
SSA-PDP	Small-scale average PDP
SSE	Sum of squares due to errors
TDMA	Time-division multiple access
TH	Time-hopping
T-R	Transmitter-receiver
ULSI	Ultra large scale integration
UWB	Ultra-wideband
VCO	Voltage-controlled oscillator
VNA	Vector network analyzer
VSWR	Voltage standing wave ratio
WCAN	Wireless chip area network
WLAN	Wireless LAN
XOR	exclusive OR

Chapter 1

Introduction

1.1 Background and Motivations

1.1.1 Traditional Wire Interconnect

Over the past decades, performance of integrated circuits (ICs) has mainly depended on device properties. In order to improve circuit and system performance, the major effort has been focused on improving the device speed through scaling of device feature dimension. On the other hand, the chip size continues increasing to integrate more functions together towards the direction of system-on-a-chip. For the complementary metal oxide semiconductor (CMOS), the feature size has been rapidly down scaled to 45 nm and the maximum operation frequency has well exceeded 100 GHz [1]. A high level of integration with improved performance can be achieved through down scaling

in the device feature dimension and growth in the chip size. In proportion to down scaling in transistor feature dimension, interconnects are scaled down to achieve a better routing density. However, miniaturization of interconnects cannot improve their performance even when issues such as resistivity degradation, new material integration and reliability problems due to electrical, thermal and mechanical stresses can be solved [2].

Interconnect consists of three parts: wire, contact and via. Together with down-scaling in transistor feature dimension, interconnect wire pitch, namely wire width and spacing, are scaled down. As the length of local interconnect wire is scaled down as well, the wire resistance is maintained constant [3]. Worse aspect ratios in contact and via stem from down scaling: smaller diameter and fixed height. Therefore, resistances of contact and via are scaled up. On the other hand, the number of contacts remains as constant and the number of vias increases with more metal layers and more complex circuits. Hence, interconnect resistance increases with down scaling.

For a piece of interconnect wire, the parasitic wire capacitance is composed of a plate component and a sidewall component. The plate capacitance is also referred as inter-metal capacitance as it results from the structure of two metal layers and the in-between dielectric. The sidewall component is related to the intra-metal capacitance since it is due to two wires running in parallel on the same metal layer. The wire capacitance per unit length increases and the total capacitance over local interconnects remains approximately constant. Nevertheless, the ratio of contributors to the total

capacitance has changed: the intra-metal contribution becomes larger than the inter-metal one.

To avoid signal loss over a long wire interconnect, repeaters are inserted. For an interconnect with a given repeater and a capacitance C at the repeater output, there is a resistance R which makes the interconnect a transmission line. With the increased unit-length resistance r_{int} and capacitance c_{int} of traditional wire interconnect due to rapid scaling, interconnect lines behave like transmission lines. Interconnect delay is defined as the delay from the input of a line driver to the output of a line receiver, with a transmission line in the middle. The transmission line can be viewed as a simple or complex network of r_{int} and c_{int} . For a single isolated interconnect which is RC -limited with an ideal return path, the interconnect delay or latency τ can be expressed as [4]

$$\tau = r_{int}c_{int}d^2 \quad (1.1)$$

where d is the interconnect line length. As the distributed resistance-capacitance product $r_{int}c_{int}$ increases with interconnect scaling, interconnect latency becomes larger, as shown in Table 1.1. As local and intermediate interconnects tend to scale in length, latency is dominated by global interconnects routing large functional blocks [5].

As transistor operating voltage continues scaling downwards, interconnect crosstalk becomes increasingly an important issue and noise must be suppressed within certain

Table 1.1: Interconnect Latency ($d = 1$ mm) at Different Technology Generations .

Technology Generations (nm)	1000 [†]	100 [‡]	68 [§]	59 [§]	52 [§]	45 [§]
RC Latency (ps)	1	30	890	1183	1465	2100

[†]Al conductor [6].

[‡]Cu conductor [6].

[§]Cu conductor, assume width-dependent scattering and with a conformal barrier of thickness [1].

level to avoid spurious transistor turn-on. The signal integrity depends on the ratio between intra- and inter-metal capacitances [3, 5]. As long as the ratio is maintained lower than unity, signals on interconnect have a good stability and perturbations introduced by adjacent lines hardly change the state.

Operating frequency of IC continues to spiral upward and effects of parasitic inductance of interconnects must be taken into consideration [5, 7, 8]. When the circuit frequency increases beyond 500 MHz, especially for the top global routing metal which is thick and wide, the parasitic inductance of wire interconnects has negative effects on both the interconnect latency and crosstalk. Besides, the interconnect inductance could give rise to signal ringing and reflection under a fast input slew rate condition.

The bit rate capacity of wire interconnect is set by the aspect ratio of the interconnection - the ratio of the length d to the total cross-section dimension $\sqrt{A}$ of the wire interconnection. On-chip wire interconnect has a capacity in bits per second around 10^{16} and 10^{17} - 10^{18} for equalized lines [9]. Other issues such as dynamic power dissipation CV^2f and voltage drop IR limit system performance with a high level of integration as well [7].

As listed above, the interconnect system performance has been degraded with scaling while fast scaling in semiconductor industry enhances intrinsic gate delay. Therefore, performance of IC is dominantly limited by traditional hard-wired interconnect, instead of device properties.

1.1.2 Wireless Interconnect

In order to circumvent problems in traditional wire interconnect due to scaling in feature size, a great amount of work has been focused on improving the interconnect performance with different approaches. Attempts include using a low-resistivity interconnection material (copper) or reducing the dielectric constant of the interlayer material (low- κ polymer). However, these approaches will encounter the fundamental material limit sooner or later, to which no known solution exists yet [10].

One possible solution to the problems in wire interconnect of microprocessors is to implement the architecture with multi cores instead of a single high-performance core [1]. Parallel data processing in the multi-core architecture could achieve comparable or even higher processor performance at lower core frequencies at reduced power consumption, where compared to a single-core high performance processor. However, significant modifications introduced to the circuit architecture result in disadvantages that new design tools are required. Moreover, the performance is very dependent on software architectures. For some software, lower processor performance is obtained with multi-core processors, when compared with a single-core high performance pro-

cessor.

Without changing the microprocessor architecture or in a more general way, revolutionary approaches have also been proposed to keep pace with the progress of future nano-regime ultra large scale integration (ULSI) technology: three-dimensional (3D) IC, optical interconnects and radio frequency (RF)/wireless interconnect systems. 3D interconnect makes use of two or more active Si strata that are integrated together by an approach such as bonding. By taking advantage of the vertical dimension, the die size can be reduced and hence global interconnect wire length can be reduced dramatically. Besides, near field inductive and/or capacitive coupling (superconnect and proximity communications) techniques can be implemented in 3D IC for a better channeling among chips [11, 12]. However, 3D requires a new technology of integrating those layers. More importantly, as more functions are integrated onto the same chip, much more power is consumed. Therefore, heat removal is a great challenge for 3D interconnects [13, 14].

On the other hand, optoelectronic techniques have been applied in optical interconnect due to the incentive of huge bandwidth for signalling. As silicon is not an efficient photon absorber, germanium or gallium arsenide is used, which is 50 times more efficient than silicon [15]. Even more recently when Intel successfully combined the light-emitting capabilities of Indium Phosphide based materials and the lighting-routing capabilities of silicon, integrating the compound materials into silicon still requires more efforts for large-volume and low-cost productions.

Finally, RF/wireless interconnect makes use of signal propagation either through freespace or guided mediums [7, 16, 17, 18, 19, 20, 21]. Capacitive coupler and off-chip but in-package microstrip transmission line (MTL) are used in [7]. RF signals are up-linked to the shared propagation medium from a transmitting chip and down-linked to a receiving chip from the MTL both through capacitive couplers. Frequency-division multiple access (FDMA)/code-division multiple access (CDMA) combined modulation scheme was adopted to achieve system advantages such as effective bandwidth, multi-I/O service, re-configurability, online computing etc. With orthogonal-coded and/or frequency-filtered RF transceivers, a MTL can be very suitable to relay ultrabroad-band signals up to 150 GHz. One great advantage of the MTL-based wireless interconnect is the compatibility with the main stream silicon CMOS process and multi-chip module (MCM) technology.

As the MTL-based interconnect achieves improvement in speed, signal integrity and channel reconfiguration over traditional hard-wired interconnect, it is still not truly a wireless interconnect. Essentially, the MTL-based interconnect is still a wired interconnect: an “active” RF interconnection rather than the traditional “passive” metal interconnect. The use of capacitive coupler and the “active” RF interconnect gives rise to some problems: the coupling capacitor is as large as $600 \mu\text{m}^2$ and the “active” RF interconnect brings system latency as well, especially for a large chip size. Since chip sizes and operating frequency of ICs increase due to scaling, integration of on-chip antenna becomes feasible [10, 22, 23, 24]. Moreover, the break through in antenna technology has realized integration of antennas onto packages [25]. With the

benefits of growing chip sizes and ever-increasing operation frequency and feasibility of on-chip/on-package antennas, wireless interconnect realizes communication among different cores within a chip (intra-chip) or among different chips within a MCM (inter-chip) [26]. The wireless interconnect is realized in the form of electromagnetic wave propagating at the speed of light. As a result, the propagation delay is expected to be smaller than those of “active” or “passive” wireless interconnects. Another reason why wireless interconnect becomes superior to wire interconnect is the emergence of the ultrawide band (UWB) technology. In terms of architecture, UWB radios are much simpler than conventional ones [20]. In the circuit implementation of UWB radios, no reference oscillator, frequency synthesizer, mixer or power amplifier is required; therefore, the required circuitry overhead will be smaller and power consumption will be lower. Due to the huge bandwidth of UWB technology, a high data rate can be supported according to Shannon’s channel capacity [2]. Therefore, wireless interconnect with UWB as its physical layer has been proposed for wireless chip area network (WCAN), including intra- and inter- chip wireless interconnects [18, 20, 26, 27, 28].

Although modulation schemes and system architectures for wireless communications have been well developed over the past century, it is a novel approach to realize intra- and inter- chip interconnects using wireless radios as shown in Figure 1.1 and 1.2, respectively. Floyd *et al.* have developed on-chip antennas, integrated transmitters and receivers for clock distribution using intra-chip wireless interconnect [17]. Zhang has proposed the WCAN concept using UWB radio as its physical layer to save circuitry overhead and power consumption [16, 20, 26]. More

Figure 1.1: Block diagram for intra-chip wireless interconnect.

specifically, some work has been done for the idea of wireless interconnect to come true. As antennas is one of the most important components in wireless communication, an extensive amount of work has been performed on characterization of on-chip antennas [10, 21, 22, 23, 24, 29, 30, 31, 32, 33]. Radiation pattern, transmission gain, metal line interference and substrate resistivity effect have been studied. On the system level, bit-error rate (BER) of an intra-chip wireless interconnect has been analyzed based on binary phase-shift keying (BPSK) modulation scheme [16]. Performance of inter-chip RF-interconnect based on coplanar waveguide (CPW), capacitive coupler and UWB transceiver has been analyzed and compared [20]. A wireless inter-chip radio has been realized with BPSK modulation scheme based on UWB technology [18]. Global clock distribution using wireless interconnect has been realized with integrated antennas [17].

However, some crucial issues have to be solved before global wire interconnect or package interconnect can be replaced by wireless interconnect. As for wireless in-

Figure 1.2: Block diagrams of wireless inter-chip interconnect: (a) wireless inter-chip interconnect inside a MCM package and (b) wireless inter-chip interconnect for chips in different packages.

terconnect with integrated antennas, another key factor is the communication channel. For wireless interconnect to communicate, especially for wireless data communication with a modulation scheme, knowledge of the channel is particularly important. When propagating through a channel, the signal gets attenuated, distorted and faded. Therefore, performance of a wireless link is directly related to characteristics of the channel. With characteristics of the channel, the capacity of wireless channel needs to be explored to find the maximum supported data rate. As wireless interconnects offer the capability of high data rate, low system latency, multi-I/O, reconfiguration etc., it would be more meaningful to apply wireless interconnect for inter-chip link: including interconnection among different chips within a MCM package and among chips in different modules. Therefore, wireless inter-chip interconnect will be studied in this thesis. There are two scenarios for wireless inter-chip interconnect: communications among chips within a multi-chip module in Figure 1.2(a), where integrated antennas are used, and among different chips inside different packages in Figure 1.2(b), where discrete antennas could be used. In most existing work, integrated antennas are used. However, the propagation mechanism of integrated antennas is still unknown even for the intra-chip communication. Therefore, the wave propagation mechanism of integrated antennas in the scenario of intra-chip communications needs to be studied as well.

1.2 Objectives

There are two objectives for this thesis. One is to perform channel characterization for wireless inter/intra-chip interconnects. Another is to analyze the system capacity of wireless inter-chip interconnects.

1.3 Major Contributions of the Thesis

This thesis studies wireless inter-chip interconnects. The major contributions of this thesis are listed as follows. The first contribution is that we carried out the characterization of inter-chip wireless channel. More specifically, we measured inter-chip wireless channel in frequency domain, proposed a technique to convert data from frequency domain to time domain with an improved time-domain resolution, analyzed the large- and small-scale distributions and performed simulation of the modeled channel; the second contribution is that we analyzed propagation mechanisms for radio waves over intra-chip channels with integrated antennas: including path loss analysis, delay spread characterization and radio wave propagation mechanism investigation; the third contribution is that we evaluated BER performance of inter-chip wireless channel of a UWB radio with BPSK modulation scheme. In order to reduce the inter-symbol interference (ISI), we proposed a technique of dynamically shifting integral window position. Analytically derived BER expressions have been verified by Monte Carlo simulations; the fourth contribution is that we designed a synchronization scheme for UWB wireless

inter-chip interconnects based on a sliding correlator and a phase-locked loop (PLL): we discussed about properties of Gaussian group pulses, analyzed the synchronization scheme and investigated effects of antennas and communication channels on synchronization performance.

1.4 Organization of the Thesis

Inter-chip wireless interconnect system is studied in this thesis, which is organized into six chapters. Chapter 2 presents a literature survey on the current status of research in wireless interconnect, including both intra- and inter-chip applications. Basically there are four different topics on the research of wireless interconnect. One part studies the RF interconnect, which is based transmission line but still a wired interconnect. The second part studies characteristics of integrated antennas, which are the key element for wireless interconnects. The third one investigates the feasibility of using wireless interconnect for intra- and inter-chip clock distribution. The fourth topic works on the realization of wireless interconnect for high data-rate and short-distance communication. Review on existing work for wireless interconnects could reveal the directions which need more efforts of research in order to realize wireless interconnect.

Chapter 3 gives the measurement, characterization and modeling of a typical wireless inter-chip channel. First, we give a brief introduction on background and necessity of the channel modeling for inter-chip wireless interconnects. Second, we describe the

measurement for wireless inter-chip channel including the background of frequency-domain measurement, equipment and procedures. Particularly, we will propose a technique on how to double the time domain-data resolution when converting data from frequency domain into time domain using the inverse discrete Fourier transform (IDFT). Third, after acquiring measurement data, we analyze the channel in both large and small scales to produce model of the channel. Finally, we implement, simulate and verify the fitted channel model.

Chapter 4 studies the propagation mechanism of radio wave over wireless intra-chip channels. First, we review the existing research work on wireless intra-chip interconnect. Then, we proceed to describe the frequency domain measurement, including the monopoles for testing, measurement setup and the frequency-domain results. Thirdly, similar to the study for wireless inter-chip channel, we convert the data from frequency domain into time domain to study the characteristics including path loss and delay spread. Particularly, we reveal the radio wave propagation mechanism for wireless intra-chip interconnects.

Chapter 5 analyzes the BER performance of a BPSK UWB radio over the inter-chip channels presented in Chapter 3. First, the status of wireless interconnects and ISI reduction techniques are reviewed. Second, we present the system description for wireless inter-chip interconnects communication. Third, we propose an ISI reduction technique particularly for the wireless inter-chip interconnect system. Finally we analyze the BER performance of the UWB wireless inter-chip interconnect system, includ-

ing analytical BER expression derivation, Monte Carlo verification, wireless inter-chip interconnect BER performance over distance and data rates, and link budget analysis.

Chapter 6 describes a synchronization scheme for the UWB radio used in wireless inter-chip interconnects. First we present the status of UWB synchronization. Second, the synchronization scheme is analyzed based on properties of Gaussian pulses, including tradeoffs of choosing Gaussian pulse orders. Third, we investigate the effects of antennas and channels on the proposed synchronization scheme.

In Chapter 7, we present the conclusions and recommendations for future work.

Chapter 2

Literature Review

Wireless inter-chip interconnect is studied in this thesis. A large amount of work has been done on the topic of radio frequency (RF) and wireless interconnects, including inductive/capacitive coupling and wireless intra- and inter-chip interconnect. The existing research work can be categorized into four topics: RF interconnect, characterization of integrated on-chip antennas, intra- and inter-chip clock distribution, and intra- and inter- chip data communication.

2.1 RF Interconnect

An RF interconnect (RFI) technology is presented by Chang *et al.* in [7] as shown in Figure 2.1. The signal from a chip (ultra large scale integration (ULSI) A) is up-linked to a common shared medium (coplanar waveguide (CPW) or microstrip transmission

Figure 2.1: Inter-chip RF interconnect system inside the MCM package.

line (MTL)) by a coupling capacitor, transmitted through the guided medium and down-linked to another chip (ULSI B) by another coupling capacitor. Modern modulation schemes frequency-division multiple access (FDMA)/code-division multiple access (CDMA) are combined to realize multiple accesses to the shared CPW/MTL. With orthogonal-coded and/or frequency-filtered RF transceiver, a passive CPW or MTL can be feasible to relay ultrabroad-band signals up to 150 GHz. Limitations of direct-coupled interconnect (DCI) and capacitive-coupled interconnect (CCI) can be overcome by employing RFI. The RFI improves signal-to-noise ratio (SNR), reduces voltage swing and improves data speed [34, 35, 36]. An RFI has achieved a maximum data rate of 2.2 Gb/s with 10.5 GHz RF-carrier in 0.18 μm a complementary metal oxide semiconductor (CMOS) process [35].

Capacitive/inductive coupling techniques have been used for short-range interconnection as well [11, 12, 37, 38, 39, 40, 41]. A self-synchronized RFI is presented in [38] based on capacitive coupling and peak signal detection, where a bit-error rate (BER) of 1.2×10^{-10} and an RMS jitter of 1.28 ps have been achieved. Capacitive cou-

pling is also used in a high-density AC coupled interconnection [40]. High-bandwidth and low-power digital chip-to-package connections have been developed with the contactless series capacitance structure. By making use of capacitive coupling, chips are placed in a face-to-face manner [12]. Sixteen-bit words pass from one chip to another in parallel without detectable error at 1.35 billion data items per second with a total data rate of 21.6 Gigabits per second. Inductive coupling is another approach for short-distance communications. Wireless interconnect using inductive coupling, also named as inductive inter-chip signaling (IIS), solves the issue of yield degradation in three-dimensional (3D) IC. Besides, delay, power and area consumption can be reduced as the non-contact interface removes a highly capacitive ESD protection structure [11]. Local connections utilizing resonant coupling between spiral inductors are studied in [37], where a transmission rate of 800 Mbps/channel was realized. It was found that crosstalk in inductive inter-chip wireless superconnect can be reduced to a negligible level when the separation between interconnections is set to certain value to minimize the interference-to-signal ratio. A technique based on time-division multiple access (TDMA) can reduce crosstalk further [41].

2.2 Characteristics of Integrated Antennas

On-chip integrated antennas have been characterized on the transmission gain about effects of substrate, metal interference structure, antenna size and orientation, crosstalk, wave propagation layers etc [10, 22, 30, 32, 42, 43, 44]. The transmission gain G_a is

defined as [29]

$$G_a = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} = G_t G_r \left(\frac{\lambda}{4\pi d} \right)^2 e^{-2\alpha d} \quad (2.1)$$

where G_t and G_r are the transmitting and receiving antenna gains, λ is the wavelength assuming a uniform medium, d is propagation distance, and α is to account for the substrate conduction loss. It should be noted that both the antennas gains G_t and G_r and the substrate loss parameter α are frequency dependent.

The transmission gain gives the power transmission relationship between a transmitting and a receiving antennas when both antennas are perfectly matched. It is found that G_a increases monotonically with frequency irrespective to the fact that there is a resonance in the reflection coefficient (S_{11}). The reason is that S_{11} and S_{22} are much less than unity and therefore the denominator of (2.1) becomes almost unity [10]. On the other hand, S_{21} increases with frequency as the wavelength of electromagnetic wave emitted from an antenna becomes shorter at a higher frequency in comparison with the physical length of the antenna. From (2.1), it can be deduced that the effects of G_t , G_r , and the substrate loss dominate over that of the factor $\lambda/4\pi d$.

One important factor that affects G_a of integrated antennas is the substrate resistivity. As silicon substrate has conductive loss, which leads to a reduction in G_a , G_a can be improved by using a Si substrate with high resistivity [22, 32, 42, 44]. With an antenna length of 2 mm and a transmitter-receiver (T-R) separation of 3 mm at

the frequency of 20 GHz, the increase in G_a with Si substrate resistivity can be more than 10 dB. However, when the Si substrate resistivity exceeds 1 k Ω ·cm, G_a becomes saturated [32].

Another similar experiment to explore the effects of substrate resistivity on G_a has been performed by fabricating on-chip antennas on 5 Ω ·cm bulk, silicon-on-insulator (SOI) with a 10 Ω ·cm substrate and silicon-on-sapphire (SOS) substrate [22]. Similar observations have been recorded that G_a of an antenna pair on an SOS substrate are higher than those on bulk and SOI substrates by more than 10 dB, since the bulk and SOI substrates have higher conduction loss.

During measurement of G_a , metal chuck under the sample plays an important role as well. If a thick low- κ dielectric layer is inserted between the sample and the metal chuck, the measured G_a can be improved by more than 10 dB as compared to the case when a sample is placed directly on the metal chuck [44]. Interestingly, when a high- κ material is inserted between the metal chuck and measurement sample, G_a can be increased as well [45]. When a measurement sample is placed directly on the metal chuck, a ground plane is present and therefore the dominant path is along the surface. However, when a low- κ material is inserted between the sample and metal chuck, two other paths through and below the substrate become possible as depicted in Figure 2.2; therefore, more energy is collected due to the two extra available paths and G_a increases. In the case when a high- κ layer is placed between the measurement sample and metal chuck, the critical angle for total internal reflection of the high-

Figure 2.2: Wave components for on-chip antennas (layers not drawn to ratio).

κ /oxide stack-layer is around 16° . Hence a large portion of the electromagnetic wave gets reflected at the interface due to total internal reflection. Therefore, G_a increases. Moreover, the radiation efficiency is increased as the high permittivity reduces the effective wavelength.

When metal interference structures are placed between transmitting and receiving antennas in normal and parallel directions, which refer to the metal line placement with respect to wave propagation direction, the transmission gain G_a are investigated [10, 45, 46]. When metal lines are placed parallel to the wave propagation direction, the transmission gain G_a increases as compared to the case without metal lines. Besides, for a dipole antenna with a length of 2 mm, G_a increases slightly when the number of parallel metal lines increases from 10 to 50. In contrast, G_a reduces with metal lines placed normal to the wave propagation direction as compared to the situation without metal lines in between an antenna pair.

This phenomenon can be explained by propagation waves of on-chip antennas as shown in Figure 2.2, which presents the cross-sectional view of a chip. The integrated

antennas radiate plane waves and launch surface waves along the dielectric surface guide. A portion of the plane wave will be reflected from dielectric-dielectric and dielectric-metal interfaces and intercepted by the receiving antenna. For parallel metal line placement, the plane wave propagates through the metal line spacing. Furthermore, a part of the outgoing electromagnetic wave directed away from the receiving antenna will be redirected to the receiving antenna. Hence there is an increase in G_a . However, when metal lines are placed normal to the wave propagation direction, the plane wave component propagating in the plane of transmitting and receiving antennas gets reflected and therefore cannot be picked up by the receiving antenna. However, the surface wave and plane wave components reflected at the dielectric-dielectric and dielectric-metal interfaces are not affected. Therefore the transmission gain G_a decreases rather than vanishes.

The effects of metal lines on G_a become more pronounced for the normal and parallel placement when the metal line density increases. For metal lines placed normal to the wave propagation direction, G_a increases when metal line length is reduced. No significant reduction in G_a is found if metal lines are shorter than one quarter of the antenna length.

In practical cases, metal lines are routed in both parallel and normal directions with respect to the wave propagation direction. Due to the competing effects of parallel and normal metal lines, reduction in G_a can be minimized [10]. However, if there exists a floating metal plate between an antenna pair, the decrease in G_a can be up to 10 dB.

Apart from metal lines, size, orientation and type of transmitting and receiving antennas affect the transmission gain, too [10, 29, 43]. A longer antenna pair has a higher G_a than a shorter one. When impedance of an integrated antennas is calculated from measured S -parameters, the impedance consists of the radiation impedance and the impedance associated with metal structure and substrate. For antennas fabricated on $20\ \Omega\cdot\text{cm}$ substrate at 15 GHz, the 1-mm antenna has the highest resistance mostly due to the high substrate resistance component [29]. For an antenna with a length of 2 mm or more, the resistance increases with antenna length, which is caused by a decrease of the substrate resistance component and an increase of the radiation and loss resistance. Besides, antenna width could change the transmission gain as well. Widening antennas from $2.5\ \mu\text{m}$ to $30\ \mu\text{m}$ results in approximately 10 dB increase in G_a . The increase in gain is attributed to the lower loss resistance of antenna arms, leading to higher power efficiency. Measurement also shows that the gain increase becomes small for an antenna width greater than $10\ \mu\text{m}$.

Typically, transmitting and receiving antennas are placed in a face-to-face manner, i.e., the relative angle θ between the antennas pair is zero. However, the relative angle θ affects the transmission gain [10]. As the angle θ increases, the effective antenna length $L \cos \theta$ becomes shorter, where L is the antenna arm length. Therefore, the transmission gain G_a decreases with θ . In practice, according to measurement results, no significant reduction G_a is observed when θ increases up to 30° .

Different types of antennas have been fabricated for characterizing G_a [29, 43].

A wide range of linear, meander, and zigzag dipoles and loop antennas have been characterized. It is found that zigzag antenna pairs have higher G_a than linear dipole pairs. For zigzag dipoles, G_a varies with the bend angle. An antenna with a bend angle of 30° has a gain roughly 6 dB higher than that with a bend angle of 120° . A loop antenna with a single loop of $200\ \mu\text{m}$ and metal width of $30\ \mu\text{m}$ has a similar gain as a zigzag antenna with a length of 2 mm near 18 GHz. More importantly, loop antennas have an isotropic radiation pattern on the wafer plane. As a loop antenna has an isotropic radiation pattern and compact size, it can be used as a transmitting antenna.

Sierpinski carpet (fractal) dipole antennas have been fabricated on chip and characterized [43]. It has been found that the fractal dipole antennas have reflection coefficient less than -10 dB in the frequency range of 6-26.5 GHz, showing an ultrawide-band response. Besides, the input impedance of the fractal antennas is within the voltage standing wave ratio (VSWR) < 2 circle throughout the bandwidth of 6 to 26.5 GHz.

When antennas are integrated on chip, crosstalk and interference to signal-carrying metal lines are inevitable [45, 47]. For on-chip antennas of 3 mm, the reflection coefficient S_{11} for metal lines of the same length has a peak around 7-9 GHz. However, the maximum power transmission from integrated monopoles occurs at the same frequency. Around the resonant frequency for maximum power transmission, the corresponding crosstalk signal about 12% of the antenna excitation signal. On the other

hand, when the same antenna is used off the resonant frequency (at 20 GHz), the crosstalk is approximately 6% of the excitation signal. Moreover, at a far field distance (> 1 mm), the crosstalk is negligible at all frequency. Therefore, it is found that a large reduction in crosstalk can be achieved by operating the antenna slightly off the resonance point [47]. Simulation of interference effect shows that G_a decreases when the number of signal carrying metal lines between the transmitter and receiver increases or the distance between metal lines and the transmitter/receiver decreases [45]. More specifically, G_a decreases exponentially with the increase in the number of interference structures placed between the antenna pair. It is also found G_a decreases exponentially with a decrease of separation distance of the interference structures from the transmitter/receiver in the near field region where capacitive coupling becomes prominent.

A metal cover for an IC package has an effect on G_a as well [48]. With a typical spacing between the metal cover and IC as 1 to 2 mm, the effect on antenna input impedance is negligible. However, when a metal plate is placed 1 mm above antennas on 20 $\Omega\cdot\text{cm}$ substrate separated by 1 cm, the phase of G_a is changed by around 100 degrees. Besides, a metal plate in this placement degrades the magnitude of G_a by roughly 10 dB. If the plate is separated 4 mm or even further from the IC, the impact of the plate becomes negligible.

Wave propagation layers for integrated antennas have also been studied [10, 45, 49, 50]. Some signals are neglected since they are highly attenuated during propagation. For example, rays traveling through the top oxide layer are neglected as the oxide

thickness is negligibly small compared to a wavelength. Multiple reflected rays are ignored as well since the reflection coefficient at the silicon/bottom layer interface is significantly less than unity and the path length is increased. Contribution from the ray propagating through the silicon layer is neglected as well due to conductive loss of the low-resistivity substrate. Therefore, main contributions for G_a are identified as: surface wave along the air/oxide interface, the lateral wave propagating on the bottom layer side of the silicon/bottom layer boundary, and the ray reflected by the metal chuck.

Apart from the application for communications among on-chip antennas, integrated antennas can be used as a link between separate chips [30, 51, 52]. G_a has been measured for integrated antennas on different substrates (inter-chip) and compared with the gain for antennas on the same substrate (intra-chip) [30]. There is a 3 dB reduction in G_a for inter-chip antennas with separation 3.5 mm including a gap of 0.5 mm between two substrates, as compared with intra-chip antennas on one substrate with a separation as 3 mm. The reduction in G_a is partially due to the 0.5 mm air gap between two substrates as signal transmission efficiency is lower in air than that through Si substrate. Another reason for the reduction is that the propagation distance for inter-chip is 0.5 mm longer than that for intra-chip. For the same inter-chip case, when one substrate is raised 2.6 mm higher than the other one without overlapping, G_a is reduced by 5.6 dB as compared to the intra-chip case. The reduction is due to the fact that the effective distance of the receiving antenna from the transmitting antenna increases and also the major path of electromagnetic wave through Si and low- κ substrates is interrupted by the air gap before arriving at the receiver. However, when the two substrates are com-

pletely overlapping with each other with a T-R separation as 3.5 mm, G_a increases by approximately 5 dB as compared with the case when one substrate is raised 2.6 mm above the other one without overlapping. This is due to the fact that the total path travelled by electromagnetic wave through Si layer is longer when the chips completely overlap each other and antenna efficiency of transmission through air is less than that through Si substrate.

G_a has been characterized between an integrated antenna and an off-chip antenna [51]. Transmission gain between an integrated 2 mm zigzag dipole antenna and an off-chip antenna increases by 5 dB and 10 dB when the substrate is changed from 5 $\Omega\cdot\text{cm}$ to 20 $\Omega\cdot\text{cm}$ silicon wafer and from 20 $\Omega\cdot\text{cm}$ silicon substrate to a sapphire substrate, respectively. Moreover, there is an increase in G_a around 20-30 dB for off-chip communication, as compared with a pair of on-chip antennas, resulting in roughly 25 dB better sensitivity for an off-chip wireless receiver. When a heatsink above a receiving antenna is present, G_a does not decrease. Instead, by making use of fins and apertures opened in the based plate of the heatsink as wave guides, G_a can be improved by 1-5 dB [53].

Transmission over freespace with integrated antennas has also been investigated [52, 54]. G_a can be improved by reducing silicon substrate thickness, increasing substrate resistivity, and decreasing the spacing between an antenna and chip edge. G_a for a 2 mm long integrated zigzag dipole antennas fabricated on 20 $\Omega\cdot\text{cm}$ substrates have been studied near 24 GHz for T-R separation up to 15 m [52]. It is found that dependency

of G_a on inverse square of T-R separation has been validated up to 4-5 m. Beyond this range, deviations from ideal behavior are observed due to the presence of multipaths.

Transient characteristics of integrated dipole antennas on silicon has been characterized for ultrawide band communications [55]. A group of aluminium dipole antennas with $10\ \mu\text{m}$ width and $1\ \mu\text{m}$ thickness were fabricated for characterization. The antenna length varies from 1 to 6 mm. By observing the reflection coefficient S_{11} , 6 mm long antennas are chosen for measurement of transient response at frequency less than 10 GHz in frequency domain. Baluns were used in the setup and the received waveforms are time derivatives of the input Gaussian monocycles. The number of time derivations is found as equal to the number baluns present in the circuit. Therefore, it was concluded that baluns in the measurement circuit plays the role of time derivative devices and the Si integrated antennas could be used for ultrawide band (UWB) communication in an integrated circuit chip with Gaussian pulses.

2.3 Intra- and Inter-Chip Clock Distribution

As shown in Figure 1.1, with antennas integrated on chip, it is inevitable that noise from digital circuit on the same substrate will be coupled to integrated antennas and therefore degrades the received SNR [56, 57]. Testing structures were fabricated in $0.25\ \mu\text{m}$ and $0.1\ \mu\text{m}$ CMOS processes. Two main types of noise coupling were considered: noise generated by transistors in digital circuits injecting currents into the

common substrate and noise capacitively coupled to antenna arms from long metal bus lines located near the antennas arms. It has been observed that noise coupling from voltage-controlled oscillator (VCO) to the antennas was seen only at harmonics of the VCO operating frequency. A significant reduction (around 12 dB) of noise energy was found in differential measurement as compared with a single-ended one. The reduction in noise shows that noise coupling from VCO to antenna is largely common-mode in nature. This noise is attributed to the substrate current injected during switching transients, which is common mode in nature. However, noise coupling from the long interconnects test structure to antenna is not common mode in nature, since results of differential measurements do not show the reduction of the received noise energy as compared to those of single-ended measurements. The reason is that interconnect lines and antenna arms can be modeled as capacitively-coupled distributed RC networks. Propagation delay and loss in interconnects will cause the signal on interconnect to couple to the antenna arms with different magnitudes and phases at different points along the line. Thus, the noise coupling is no longer common mode in nature. Furthermore, it has been found that circuits such as buffers are relatively noisier and generate more noise at higher operating frequencies [57]. As a result, in order to reduce interference coupling from digital circuits on the same substrate to on-chip antennas, signal frequency on antenna can be chosen much greater than the circuit frequency. Another possible solution is to use antennas with a differential or balanced feed structure to greatly reject switching noise coupling, which is mostly common mode in nature.

Jitter of transmitted wireless clock has been found much like jitter of convention-

ally distributed clock signals [58]. Jitter in received clock increases as large inverter chains are enabled. Noise from nearby digital circuits reduces the low-noise amplifier (LNA) gain and shifts the divider self-oscillator frequency, leading to degraded receiver sensitivity. Therefore, the receiver clock jitter increases and eventually the receiver clock circuit may fail to lock onto the transmitted clock signal. Moreover, peak-to-peak jitter almost falls linearly with an increase of clock power supplied to transmitting antenna in dBm.

An intra-chip wireless interconnect using integrated antenna for clock distribution has been demonstrated in a flip-chip ball grid array package [59]. The transmitter-receiver pair of the wireless interconnect is fabricated in a $0.18\ \mu\text{m}$ CMOS process. A 14.768-GHz signal is generated and broadcast over the IC. The transmitter is separated around 4 mm from the receiver and there are approximately 70 solder balls between the transmitter and receiver. Output of the VCO is divided by eight to produce 1.846 GHz clock. It has been found that the receiver is able to lock onto the received clock signal at 1.846 GHz. Moreover, the packaged IC is used to receive a sine wave transmitted from a 2-mm zigzag dipole antenna on a $20\ \Omega\cdot\text{cm}$ silicon wafer. The receiving packaged IC is placed 40 cm from the transmitting antenna with an incident power to antenna as 21 dBm at frequency 14.3 GHz. The package IC has sensitivity as -35 dBm and can be improved by 50 dB or more by employing conventional radio architecture.

Intra- and inter-chip wireless interconnect for clock distribution have been discussed in [17, 19, 54, 60, 61]. Using a $0.18\ \mu\text{m}$ CMOS technology, the transmitter

consists of a VCO, an output amplifier and an antenna, while the receiver consists of an antenna, an LNA, a frequency divider and buffers. The wireless clock transmitter with integrated antennas generates and broadcasts a 15-GHz global clock signal across a test chip of $7 \times 6 \text{ mm}^2$, and the wireless clock signal is picked up by a receiving antenna. The receiving antenna is located 5.6 mm away from the transmitting antenna and the received wireless clock signal is divided by eight to produce a local clock signal at 1.875 GHz [17, 60]. Another demonstration of wireless clock distribution using a receiver located 2.2 cm away from a wireless clock transmitter generating a 15-GHz clock signal [19, 61]. Utilizing an external horn antenna for an inter-chip wireless clock distribution system, a clock signal with a total skew less than 14 ps can be provided over an area of $3.8 \text{ cm} \times 3.1 \text{ cm}$. This is sufficient for a system operating around 3 GHz and the chip area is four times larger than an area which is typically thought possible for synchronization of such frequencies.

The projected power consumption of a wireless clock distribution system has been estimated and compared with conventional systems [62]. For a wireless interconnect system for global clock signal distribution with antenna frequency as 20 GHz or higher and system frequency as 4 GHz or lower, the analysis compares the projected power dissipation of the wireless clock distribution system to conventional grid-based and H-tree based distribution systems for $0.1 \text{ }\mu\text{m}$ generation processors, based on the total capacitive loading of the global distribution system. It has been found that in terms of power dissipation, the wireless clock distribution system is comparable to conventional ones.

2.4 Intra- and Inter-Chip Data Communication

For data communications, one or some modulation schemes are employed to improve the efficiency of transmission and spectrum usage. Moreover, synchronization is needed for high data rate communication where coherent detection is usually used. Besides, more complicated circuitries, especially at the receiver side, are required for data communication. Therefore, the data communication is quite different from the clock distribution. BER analysis has been performed for a wireless intra-chip interconnect system using binary phase-shift keying (BPSK) modulation as shown in Figure 1.1 [16]. The intra-chip interconnect system operates on a wireless channel at 15 GHz. With increases in T-R separation distance and data rate, the system BER performance gets degraded. When the transmitted power is 10 dBm, a high data rate at 2 Gbps with a low BER $< 10^{-5}$ over the whole chip $20 \text{ mm} \times 20 \text{ mm}$ can be achieved.

A wireless inter-chip interconnect with UWB has been demonstrated as shown in Figure 1.2(b) [18]. The wireless interconnect consists of a transmitter with a pulse generator and a driver amplifier and a receiver with LNA and multiplier. The pulse generator produces second-order Gaussian pulses and a pair of monopole UWB antennas is utilized to generate and receive signal. The prototype impulse radio is implemented in a $0.18 \mu\text{m}$ CMOS process with BPSK modulation. A data rate of 165 Mbps over the inter-chip wireless channel of length 20 cm has been achieved with a power consumption of 120-mW. Other modulation schemes such as pulse position modulation (PPM) are also proposed for inter/intra-chip wireless interconnects [27].

Chapter 3

Measurement, Characterization and Modeling of Wireless Inter-chip Channel

3.1 Introduction

For the past few decades, performance of IC has mainly depended on device properties. In order to enhance the circuit and system performance, the major effort has been focused on improving the device speed through scaling of device feature dimension. The down-scaling of device dimension has led to operating speed and cut-off frequency (f_t and f_{max}) exceeding 100 GHz and at the same time the proportional reduction in interconnect cross-sectional area and pitch together with via size [1].

Metal wiring method has been adopted for traditional interconnect technology. The decrease in physical dimension of hard-wired metal interconnects degrades the circuit and system performance seriously, especially at high operating frequencies, e.g., interconnect resistance, capacitance, inductance and bit-rate capacity. The associated parasitic capacitance and inductance increase the time delay (RC or LC). Signal attenuation and dispersion in wire resulted from scaling give rise to degraded bit-rate capacity whose upper bound is $10^{16}A/l^2$ (or $10^{17}A/l^2$ by equalizing channels) [7], where A and l are the cross-sectional area and the length of the interconnect wire respectively. Other issues such as IR voltage drop, CV^2f power loss and crosstalk between wires become significant as well.

To circumvent the problems in interconnect caused by down-scaling of device feature dimension, a great amount of work has been focused on improving the interconnect performance by reducing the interconnect resistivity (using copper) or reducing the dielectric constant of the interlayer material (using low- κ polymer). However, these approaches will encounter the fundamental material limit sooner or later, to which no known solution exists currently. Therefore, to conquer the obstacle in the evolution of deep submicron ultra large scale integration (ULSI) technology, revolutionary approaches must be pursued. One possible solution is to use the multi-core architecture instead of a single-core high performance processor. Parallel data processing would achieve comparable or higher processor performance when compared with the single core high performance processor. However, this technology also brings the disadvantages of needing new design tools and software, as described in Subsection 1.1.2. In a

general approach, three different approaches have been attempted: three-dimensional integration, optical links, and wireless interconnect [5, 63, 64]. As only wireless interconnects are compatible with the mainstream system-on-chip and system-in-package technologies for low-cost system production, they have drawn considerable attention recently. For example, Floyd *et al.* have developed on-chip antennas, integrated transmitters and receivers for wireless interconnects [17]. Zhang has proposed the wireless chip area network (WCAN) concept using impulse or ultrawide band (UWB) radio as its physical layer to save circuitry overhead and power consumption [16, 20, 26]. It is seen that some work has been done in the design of on-chip antennas and circuits for wireless interconnects or WCAN applications [20, 26, 44]. However, little work has been done to understand the wireless communication channel within a chip or among chips. To realize WCAN over intra- or inter- chip channels, it is essential to have knowledge of the channel. Therefore, we focus on understanding of inter-chip wireless communication channels in this chapter. Radio propagation channel within a computer metal casing as a practical situation is characterized for both casing closed and open conditions. Models are extracted and simulated for the inter-chip wireless communication channel. Simulated responses are compared with empirical data, showing that generated channel responses closely match experimental data in the practical situation. Measurements in different computer casings give consistent channel parameters. Therefore, the channel presented is for typical wireless inter-chip communication.

The chapter is organized as follows. In Section 3.2, experiment background, equipment and procedures are described. Data processing and parameter extraction using

best fit procedures are presented in Section 3.3. In Section 3.4, channel models have been implemented based on the parameters derived, and simulation results of the implemented model are compared with experimental data.

3.2 UWB Inter-Chip Channel Measurement

3.2.1 Channel Measurement Techniques

Channel measurement can be performed in either frequency domain [65, 66] or time domain [67]. A comparison for characterizing UWB channel using the two techniques has been given in [68]. Because of the Fourier transform relationship between channel impulse response and channel transfer function in frequency domain, data measured using a vector network analyzer (VNA) can be converted to time domain using the inverse discrete Fourier transform (IDFT). Being a swept frequency technique, high measurement dynamic range is readily obtainable. The generic system is relatively flexible since the frequency of operation, multipath resolution and maximum measurable delay can be reconfigured by adjusting the operation parameters of the VNA. Furthermore, since the VNA system operates with a transmitted reference, it provides a power delay profile (PDP) with an absolute delay. This frequency-domain channel measurement technique has been proven as accurate as many time domain techniques when long distance measurement is not required [65]. For interested readers, a detailed description of utilizing VNA for wideband channel measurement has been provided

in [69].

The time domain resolution is $1/B$ in complex baseband approach [66], where B is the measured frequency range. However, by making use of properties of discrete Fourier transform (DFT) and IDFT, the time domain resolution can be increased up to $1/2B$. For a $2N + 1$ -point finite length discrete-time signal $x[n]$, $n = 0, 1, 2, \dots, 2N$, DFT is given by $X[k] = \sum_{n=0}^{2N} x[n] \exp(-j2\pi \frac{k}{2N+1} n)$, where $k = 0, 1, 2, \dots, 2N$. DFT of $x[n]$ is $2N+1$ -point periodic. The frequency domain signal has the magnitude response as an even function and the phase response as an odd function. If a VNA is used to record the frequency response of the $2N+1$ discrete time signal $x[n]$, only $N+1$ frequency points can be observed, which corresponds to $k = 0$ to Nyquist component ($k = N$) of the sequence $X[k]$. If the discrete-time domain signal is reconstructed based on the $N+1$ points frequency response, the time domain data becomes $N+1$ points, yet still covers the same time span as the original discrete time signal $x[n]$, which has $2N+1$ points. Therefore, the time-domain resolution becomes half of the original discrete time signal. To prevent this loss of the time domain resolution, the obtained $N+1$ -point frequency response is extended into $2N+1$ -point by reconstructing components above $k = N$.

IDFT can be applied together with various windows. A rectangle window gives time domain resolution as $1/2B$ while hamming window leads to a worse resolution $1.37/2B$. On the other hand, rectangle and hamming windows result in 13.3 dB and 42.5 dB sidelobe attenuations respectively. To get the best time domain resolution,

Figure 3.1: Measured S_{11} of UWB antenna over frequency.

rectangle window is applied during IDFT to sampled frequency domain data, while attenuation of 13.3 dB is sufficient for suppression of sidelobes.

3.2.2 Equipment

Antenna is a critical component for characterizing the inter-chip wireless channel. To sample inter-chip channel, a pair of UWB antennas [18] is used, whose measured impedance bandwidth is shown in Figure 3.1. The adopted UWB antenna has S_{11} lower than -10 dB over 6.7 GHz from 3.75 to 10.45 GHz.

Measured radiation patterns of UWB antenna in both E and H planes are depicted in Figure 3.2 for frequencies 3.5, 6.85 and 10 GHz. It can be observed that the UWB antennas display quasi omni-directional patterns.

Figure 3.2: UWB antenna radiation patterns: (a) and (b) E plane co- and cross- polarization respectively; (c) and (d) H plane co- and cross- polarization respectively. Thick, normal and thin lines are for frequencies 3.5, 6.85 and 10.0 GHz respectively in each plot.

Figure 3.3: UWB antenna normalized transfer function and group delay: Top, normalized transfer function; bottom, group delay.

In addition to impedance bandwidth and radiation patterns, normalized transfer function and group delay are given in Figure 3.3, where the measured S_{21} is normalized to the standard antenna to calibrate the range related effect [70]. The transmitting and receiving antennas are placed in a face-to-face co-planar orientation with a separation distance of 1.6 meters. A dual-polarized quad-ridged horn antenna WJ-48430 is chosen as a standard antenna, which has been proved well matched to the measurement system from 3 to 18 GHz. A relatively flat gain and nearly constant group delays can be observed over the band of interest.

Time domain performance of the UWB antenna has been checked against distortion with the fourth derivative of a Gaussian pulse with $T = 175$ ps

Figure 3.4: Measurement setup for channel in a computer casing.

$$p(t) = \left[3 - 6 \left(\frac{4\pi}{T^2} \right) t^2 + \left(\frac{4\pi}{T^2} \right)^2 t^4 \right] \exp \left(-2\pi \left(\frac{t}{T} \right)^2 \right) \quad (3.1)$$

and a modulated pulse with $f_c = 5$ GHz and $\alpha = 300$ ps

$$p(t) = \sin(2\pi f_c t) \exp \left(- \left(\frac{t}{\alpha} \right)^2 \right) \quad (3.2)$$

Both pulses comply with the Federal Communications Commission (FCC) indoor emission mask for UWB. Fidelity factor [71], expressed in (3.3), is used to evaluate pulse distortions introduced by antennas and a unity fidelity factor indicates no distortion. The UWB antenna has high fidelity factors of 0.98 and 0.9958 for Gaussian fourth derivative and the modulated pulses respectively. In (3.3), $\omega_{tr}(t)$ and $\omega_{rec}(t)$ are the transmitted and received pulses, respectively. More details regarding the UWB antenna can be found in [72]

$$\text{Fidelity} = \arg \max_{\tau} \left[\frac{\int_{-\infty}^{\infty} \omega_{tr}(t) \omega_{rec}(t - \tau) dt}{\sqrt{\int_{-\infty}^{\infty} \omega_{tr}^2(t) dt \int_{-\infty}^{\infty} \omega_{rec}^2(t) dt}} \right] \quad (3.3)$$

In the measurement of inter-chip channel within a computer casing, it is found difficult to place antenna close to chip surface as large-area chips are not readily available and there are many surrounding discrete components. Therefore, a pair of UWB antennas described above is placed vertically using a right angle connector. The network analyzer built-in cables are too thick and too short for direct channel measurement. In order to sound the channel in the computer casing, two 20 cm semi-flexible cables are inserted between antennas and network analyzer cables.

The network analyzer used for recording is an Agilent PNA-L network analyzer of model N5230A up to 20 GHz. Data collection is performed in a typical commercial COMPAQ personal computer, where components such as independent graphic card, memory, hard drive, floppy drive and zip drive are installed. Measurement setup is shown in Figure 3.4 and a photograph is given in Figure 3.5.

3.2.3 Procedures

To measure WCAN channel in a computer casing, the sampling points on the motherboard are shown in Figure 3.6, where labeled points correspond to the snapshot in Figure 3.5. During measurement, no object is moving around. Further more, for closed computer casing, the enclosure are well shielded against external interferences. There-

Figure 3.5: Measurement snapshot.

Figure 3.6: Measurement points on motherboard.

fore, the multipath channel can be considered frozen or quasi-static [73]. Heatsink and CPU fan are removed for the convenience of measurement. There are four series of measurement. Series B places transmitting and receiving antennae on Chip X

and grids of CPU respectively. In Series C, the receiving antenna is placed on grids of Chip Y while transmitting antenna remains on Chip X. For both series B and C, the line-of-sight (LOS) path is blocked by the graphic card inside of the casing. In series D, the transmitting antenna is placed on the top right grid of Chip Y and receiving antenna moves on the grids of CPU. Series E has 6 measurement configurations: Chip X-A, B, memory, C, D and E. Chip C is on the standing graphic card and is not shown in Figure 3.6. Sampling frequency range is chosen as 3.1-10.6 GHz to obtain the highest allowable emitting power under FCC regulations. For all recorded data in channel measurement, the computer casing is placed on work bench in a typical laboratory and recording is performed for both computer casing closed and open. Full 2-port calibration has been performed up to right-angle connector tips.

3.3 Data Processing and Result Analysis

Surrounding environment, such as PCI card, chips, discrete components, wires, metal casing etc., results in multipath effect. Hence signals arriving at the receiver get attenuated, delayed and phase-shifted differently. Impulse response can be presented mathematically by

$$r(t, \tau; d) = \sum_{k=1}^{N_{bins}} a_k(t; d) \exp(j\theta_k(t; d)) \delta(t - \tau_k) \quad (3.4)$$

where d is the transmitter-receiver (T-R) separation distance, N_{bins} is the number of

Figure 3.7: NLOS received power for computer casing closed.

multipath components, a_k is the amplitude, θ_k is the associated phase and τ_k is the excess delay of k th path relative to the first arrival. δ is the Dirac delta function. The multipath PDP in time domain of (3.4) is converted from recorded frequency response using IDFT. Delay axis is quantized into bins [74]. Since two multipath components arriving within a bin cannot be resolved, the bin size $\Delta\tau$ is generally chosen to be the resolution of the specific measurement. For measurement in a computer casing, the bin size is 66.6667 ps. To reduce observation noise, the energy in each bin below a certain threshold is set to zero. The threshold is set to 10 dB above noise floor, which is determined by average received noise. The noise floor is determined from the segment of 15 to 20 ns as the energy decays almost completely around 10 ns. Figure 3.7 gives a typical non-LOS (NLOS) received power when computer casing is closed.

For inter-chip channel characterization, statistic parameters for large scale and

small scale are analyzed separately. The large scale fading characterizes the changes in the received signal when the transmitter-receiver distance changes significantly or the position and/or environment of the transmitter changes [74]. For WCAN measurement, large scale is defined as when transmitter is fixed on one chip, and receiver moves on another chip. The PDP averaged over a local area is denoted as small-scale average PDP (SSA-PDP) to determine global parameters. On the other hand, small-scale fading characterizes the changes in the received signal when the changes of positions of transmitter or receiver are not significant. Hence, moving the receiving antenna on grids of the same chip gives small scale data, which are used to extract local parameters. Inter-chip wireless communication within a computer casing is close to practical situations. Details of channel modeling and analysis are given in the subsections below.

3.3.1 Large-Scale Analysis

Path loss factor is an important parameter for large scale modeling and can be extracted from SSA-PDPs. The path loss factor determines the average received power over distance. Path loss model [74] can be described by

$$PL = \gamma 10 \log_{10}(d/d_0) + PL_0 + X_\sigma \quad (3.5)$$

PL is the path loss, which gives power attenuation in dB at distance d . d_0 is the reference distance. PL_0 is the interception of model fitted line with vertical power

Table 3.1: Path Loss Parameters.

	Casing closed	Casing open
γ	1.607	2.692
$d_0(mm)$	62	62
$PL_0(dB)$	23.78	25.27
$\sigma(dB)$	0.5482	1.9088

loss axis. γ is the power loss factor. The factor X_σ is a zero mean Gaussian distributed random variable (in dB) with standard deviation σ [72]. By fitting the data to the above models with confidence level 95%, parameters for path loss model can be extracted as given in Table 3.1.

Fittings of path loss scatter plot are depicted in Figure 3.8. During WCAN sampling, there are discrete components in close proximity of antennas such that antenna characteristics are altered more or less [75]. As a result, antenna effect cannot be calibrated out from sampled inter-chip channel response. Rich multipath in the computer casing does change the path loss factor. When the computer casing is closed, most energy bounces inside of the casing, leading to a small path loss factor and low power attenuation. However, when the casing is open, a significant portion of energy escapes out of the casing and the remaining portion still gets reflected and attenuated, giving a higher power loss and path loss factor. The difference in path loss between casing closed and casing open increases when T-R distance increases. Another important factor is the distance between the antenna and the metal cover. When antenna is too close (7 mm) to the metal casing, either surrounding or ceiling metal cover, much lower power attenuation than that for other situation is observed. This is clearly shown in

Figure 3.8: Path loss fitting of inter-chip channel.

Figure 3.8 by the data points in an ellipse. These points are excluded during fitting since antenna is supposed to keep certain distance from metal casing to avoid reactive coupling and short circuit. It could be due to the fact that energy reflected from metal cover is collected before it scatters out, like the reflective antennas [75]. From the standard deviation σ in (3.5), it can be seen that the closed computer casing gives a more uniform environment, leading to a smaller shadowing effect.

In the derivation of path loss parameters, the average PDPs have been derived for series B, C, and D. For series E, individual profile is taken to model the decay rate ε . The averaged PDPs of series B, C, and D are fitted into exponential law to obtain the power decay rate. It is found that for series B, C and D, the decay rate of the averaged PDP is very close to the average decay rate for individual PDPs and the decay rates have around 10% deviation from the respective mean values. Therefore an amount of

Figure 3.9: Decay rates over distance.

Table 3.2: Parameters for Decay Rates over Distance.

	m (dB/ns/mm)	ε_0 (dB/ns)
Casing closed	-0.0044721	2.576
Casing open	-0.008199	4.528

10% deviation should be included for simulation since the decay rates for series E are obtained from their individual PDPs. The change of power decay rate over distance, as shown in Figure 3.9, is described by (3.6)

$$\varepsilon = m \times d + \varepsilon_0 \quad (3.6)$$

where m , d , and ε_0 are the slope, T-R distance in mm and decay rate at zero interception distance respectively. Parameters for decay rates over distance are summarized in Table 3.2.

From Figure 3.9, it can be seen that decay rate is higher when the casing is open than that for the closed casing, i.e., energy decays faster when the casing is open. It is due to the fact that the closed casing allows signal to bounce more times before it decays completely. It implied that more received signal energy could be collected and therefore a lower level of transmitted signal power could achieve the link budge requirement. On the other hand, the long decaying time implies a high level of inter-symbol interference, and therefore limits the data rate. Negative values of m indicate that when T-R distance increases, signal has more paths to arrive at the receiving antenna, resulting in a lower time decay rate. A steeper slope for the open casing shows that the increase in the number of paths in proportion to T-R distance is more important for the open casing. For the closed casing, there are a lot of paths even for short distance due to the closed environment; therefore, the increase in number of paths due to increase in T-R distance is not as critical as that when casing is open.

3.3.2 Small-Scale Analysis

Variations of energy amongst grids of chips are investigated in small scale analysis. Energy of each bin in small scale is fitted into distributions using best fit procedures. Seven distributions are used to fit measurement data, including Gamma, Lognormal, Nakagami- m , Normal, Rayleigh, Rician and Weibull distributions. For Lognormal distribution, the power in each bin has been converted into log scale, i.e., $P_{dB} = 10 \log_{10}(P)$ and fitted to a Normal distribution later on. For Nakagami- m distri-

Figure 3.10: Small scale distribution of inter-chip channel, casing closed.

bution, the maximum likelihood estimator (MLE) is from [76], where the psi function $\psi(m)$ is taken as the second order approximation of its asymptotic expansion. For the K -parameter of the Rician distribution, the moment-based estimator from [77] is used. All other parameter estimations are based on the methods provided in MATLAB 6.5 documentation [78].

Fitted distributions of each bin are shown in the Figure 3.10 for inter-chip wireless channel when the computer casing is closed. The horizontal axis is the number of bins and the vertical axis indicates the distribution for the corresponding bins. From 1 to 7, distributions are Gamma, Lognormal, Nakagami- m , Normal, Rayleigh, Rician and Weibull distributions respectively. The position zero indicates that energy in that particular bin is lower than the threshold value, which is 10 dB above the noise floor.

It can be observed that from bin 1 to bin 90, the Lognormal distribution gives the

Figure 3.11: Fitting of first bin into Lognormal distribution, casing closed.

best fitting results. From bin 90 onwards, the energy is negligible. Therefore, small scale modeling for casing closed is Lognormal distribution up to bin 90. Fitting into the Lognormal distribution of the first bin is shown in Figure 3.11 as an illustration.

Best fitting results for the open casing is given in Figure 3.12. It can be seen that first few bins follow Weibull and Normal distributions and afterwards, Lognormal distribution is the best fitting. However, by observing the sum of squares due to errors (SSE), it is found that for the first few bins, Lognormal still gives a good fitting quality even though it is not the optimum fitting. Small scale distribution for bin 1 is given in Figure 3.13 for the open casing as an example.

As a result, for both the casing closed and open, Lognormal is taken as the small scale distribution up to bin 90. Beyond bin 90, it is considered negligible energy exists.

For the casing closed, fitting of normalized energy into Lognormal distribution

Figure 3.12: Small scale distributions, casing open.

Figure 3.13: Fitting of first bin into Lognormal distribution, casing open.

Figure 3.14: Fitting of μ into Normal distribution, casing closed.

from bin 1 to bin 90 gives 90 sets of parameters for the Lognormal distributions $L_N(\mu, \sigma)$. It is found that μ and σ follow Normal distribution as given by Figure 3.14 and Figure 3.15.

Fitting μ into Normal distributions gives two parameters $\mu_{-\mu}$ and $\sigma_{-\mu}$. The dependency of the two parameters on distance is given by (3.7)

$$\mu_{-\mu} = 0.009741 \times d - 2.313 \quad (3.7a)$$

$$\sigma_{-\mu} = -0.004473 \times d + 1.909 \quad (3.7b)$$

Similarly, fitting σ into Normal distribution gives another two parameters $\mu_{-\sigma}$ and $\sigma_{-\sigma}$, which are distance-dependent as described by (3.8)

Figure 3.15: Fitting of σ into Normal distribution, casing closed.

$$\mu_{\sigma} = -0.006687 \times d + 5.239 \quad (3.8a)$$

$$\sigma_{\sigma} = -0.003702 \times d + 1.631 \quad (3.8b)$$

Similarly when the computer casing is open, the small scale distribution of energy in each bin follows the Lognormal distribution: $L_N(\mu, \sigma)$. Parameter μ for different bins gives the Normal distribution with parameters μ_{μ} and σ_{μ} as shown in Figure 3.16. Variation of the two parameters over distance is described (3.9a) and (3.9b). The standard deviation of the Lognormal distribution gives another Normal distribution as given in Figure 3.17. The Normal distribution parameters μ_{σ} and σ_{σ} change over distance as described by (3.9c) and (3.9d).

Figure 3.16: Fitting of μ into Normal distribution, casing open.

$$\mu_{-}\mu = -0.00219 \times d - 1.405 \quad (3.9a)$$

$$\sigma_{-}\mu = -0.003338 \times d + 2.12 \quad (3.9b)$$

$$\mu_{-}\sigma = 0.002901 \times d + 4.244 \quad (3.9c)$$

$$\sigma_{-}\sigma = -0.005302 \times d + 2.872 \quad (3.9d)$$

3.4 Model Implementation, Simulation and Verification

The inter-chip wireless channel is generated according to parameters extracted in the last section. Given a certain distance, the total power attenuation PL can be generated according to (3.5) and parameters of γ , d_0 , PL_0 , σ given in Table 3.1. PL is converted

Figure 3.17: Fitting of σ into Normal distribution, casing open.

into linear scale to obtain the power ratio r . The decay rate ε is generated from (3.6) and parameters in Table 3.2. SSA-PDPs can be generated with the power ratio r and decay constant ε . The observation window length is set to 90 bins with bin width the same as the measurement resolution. For the inter-chip channel, Equations (3.7)-(3.9) give Lognormal distribution parameters, which can be used to generate individual PDPs for both casing closed and open. Figure 3.18 gives the comparison of small-scale PDPs for computer casing closed.

From the comparison, it can be seen intuitively that the model-generated results closely match the experimental data. A quantitative comparison between measured and simulated CDF (fitted using Normal distribution) of received power is shown in Figure 3.19 for a distance of 84 mm and available LOS signal. The received power is obtained by lumping energy over all bins for each local PDP [67].

(a)

(b)

Figure 3.18: (a):Generated small scale PDPs for casing closed. (b):Experimental small scale PDPs for casing closed.

Figure 3.19: Comparison between experimental and generated CDF of received power.

The modeling makes sense if the experimental data are sampled in a typical environment for wireless inter-chip channel. Sampled data from a Ranger WorkHorse commercial computer denoted as series K are used for comparison. The Ranger WorkHorse personal computer have independent graphic card, memory, hard drive, floppy drive and zip drive installed. During measurement series K, the CPU heatsink and fan were not removed to make it a practical scenario. The measurement distance covers the range from 43 to 218 mm. Analysis shows that series K has path loss close to value predicted by (3.5) within 2 dB and 5 dB for the casing closed and open respectively. Besides, series K indicates that low path loss is obtained when receiving antenna is close to the metal casing, as mentioned above. Further more, when the T-R distance is too short (43 mm), the path loss model cannot predict received power since the antennas are not in each other's far field. It is found that delay spread in series K is within the range of measurement series B to E, too.

Chapter 4

Propagation Mechanism of Radio

Waves over Intra-chip Channels

4.1 Introduction

The complementary metal oxide semiconductor (CMOS) technology has been continuously scaling down in order to increase the degree of integration and to improve device performance. Recently, the MOS transistor feature dimension has been scaled below 100 nm and the speed of operation has exceeded over 100 GHz. CMOS technology scaling causes great interconnect challenges. On one hand, the width and thickness of metal interconnect lines are scaled down in proportion with device feature dimension. On the other hand, metal wires have to be routed over a bigger chip area for ultra large scale integration (ULSI) or system-on-chip (SoC) solutions. As a result,

the fundamental material limit of wire interconnect will be approached sooner or later. In other words, traditional wire-interconnect has become a bottleneck in further development of ULSI or SoC. To carry on the progress of current and future ULSI or SoC, wireless interconnect has been proposed. Floyd *et al.* have developed on-chip antennas, which were integrated with transmitter and receiver, for wireless clock distribution [17]. Zhang has evaluated the intra-chip data communication system using wireless interconnect [16]. More recently, the idea of wireless interconnect has been extended to the concept of wireless chip area networks. A wireless chip area network uses radio waves rather than metal wires to communicate among cores within a chip (intra-chip) or among chips within a module (inter-chip) [18, 20, 26, 79].

The wireless chip area network features a unique intra/inter chip-scale radio propagation channel. It is known that understanding of chip-scale radio propagation channels is essential for the analysis and design of a wireless chip area network. Chen and Zhang have studied an inter-chip radio propagation channel with on-package monopoles over the ultra wideband frequency range from 3.1 to 10.6 GHz [80]. As expected, the inter-chip radio propagation channel is a multi-path radio propagation channel and the received radio signal suffers from frequency-selective fading and time-domain dispersion. The propagation loss depends on whether the inter-chip radio propagation channel is located in an open or enclosed casing. The path loss factor is less than 2 in the enclosed casing and larger than 2 in the open casing. Kim *et al.* have studied an intra-chip propagation channel in the frequency domain from 6 to 18 GHz with integrated dipoles on a silicon wafer [50]. They proposed a plane-wave model to explain

the propagation mechanisms and found transmission gain can be improved by inserting a low-loss dielectric layer between the silicon wafer and the probe-station chuck, which functions as a ground plane.

Integrated or on-chip antennas excite and receive radio signal in an intra-chip propagation channel. Being inseparable from the intra-chip propagation channel, an on-chip transmitting antenna, an intra-chip propagation channel, and an on-chip receiving antenna are considered in this chapter as an intra-chip radio propagation channel. The intra-chip radio propagation channel has been characterized on the transmission gain [10, 22, 24, 32]. Kim and O measured the transmission gain in the frequency domain from 10 to 18 GHz for axially 2-mm long straight dipoles fabricated on bulk, silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) substrates [22]. They found that the transmission gain of dipoles increases with frequency and has higher value on the SOS substrate than those on the bulk and SOI substrates. The lower transmission gain for dipoles on the bulk and SOI substrates is due to the low resistivity of the substrates, which has a higher loss as compared to the SOS substrate. Resistivity of silicon substrate can be greatly increased by proton implantation, leading to a lower substrate loss and therefore a higher transmission gain [32]. A high transmission gain window in frequency domain was observed from measurements of on-chip monopoles up to 110 GHz [24]. The wireless chip area network is recommended to operate within the high-gain window for optimized performance. In addition, there are many metal structures such as bus lines, power lines, and solder joints, which inevitably occur between transmitting and receiving antennas and affect the characteristics of the intra-chip ra-

dio propagation channel. It was found that the parallel and normal metal lines between antenna pair increase and decrease the transmission gain, respectively [10].

Literature survey shows that the intra-chip radio propagation channel has been measured and analyzed in frequency domain. Yet, no time-domain analysis of intra-chip radio propagation channel has been made. As a result, available received power and delay-spread characteristics of the intra-chip radio propagation channel are still not clear. The intra-chip radio propagation channel has not been fully characterized, which necessitates the work performed in this chapter. We describe the test vehicles, integrated antennas, and frequency-domain measurements in Section 4.2. We analyze characteristics of intra-chip radio propagation channel in time-domain and offer a physical insight into propagation mechanism in Section 4.3.

4.2 Frequency-Domain Measurement

Integrated monopoles, test vehicles, measurement setup, and frequency-domain results are described in this section. The test vehicles refer to chips where the testing antennas and structures are built [24].

4.2.1 Integrated Monopoles and Testing Vehicles

Dipole antennas are preferred for wireless chip area networks because they can adequately reject noise and interfering signals generated by other circuits on the same

Figure 4.1: Cross-sectional and top views (not to scale) for integrated zigzag, linear and meander antennas on silicon wafer.

substrate. However, dipole antennas are not compatible with most currently existing test facilities. Baluns are required to perform measurements for dipoles. It is known that baluns are narrow-band devices, which partially explains why most reported frequency-domain measurements are below 26.5 GHz [24]. To experimentally characterize intra-chip radio propagation channels over a much broader bandwidth, integrated monopole antennas, including zigzag, linear, and meander antennas, were laid out on standard 6-in p-type silicon wafer, whose cross-sectional view is depicted in Figure 4.1. An oxide layer of $2\text{ }\mu\text{m}$ thickness is grown on silicon substrate of $633\text{ }\mu\text{m}$ thickness for isolation. Monopole antennas with axial length 1 mm are drawn using aluminum layer of $2\text{ }\mu\text{m}$ thickness and $10\text{ }\mu\text{m}$ width. Monopoles were then fabricated into test vehicles using NTU 1.2- μm CMOS process, where resistivity of silicon wafers are $10\text{ }\Omega\cdot\text{cm}$ and $5\text{ k}\Omega\cdot\text{cm}$, respectively. The maximum size of a test vehicle is $10.8\times 10.8\text{ cm}^2$ [24].

Antennas, once integrated on a substrate, are impossible to move or rotate with respect to each other. Therefore, in order to cover various scenarios for the character-

Figure 4.2: Die photo of a test vehicle using 0.18 μm process.

ization of intra-chip radio propagation channels, monopole antenna pairs separated at a specific distance d between the T-R antennas and oriented with a specific angle were designed as shown in Figure 4.1. Sixteen pairs of monopole antennas with a 2.5-mm increment in T-R distance and 10 pairs of monopole antennas with a 10° increment in relative angle were implemented in test vehicles, which cover separation from 2.5 to 40 mm and relative angle from 0° to 90° . As shown in Figure 4.1, metal lines, which can be densely or loosely spaced, were placed between monopole antenna pairs in both parallel and normal directions. By parallel and normal directions, we mean metal lines are placed parallel and normal to the wave propagation direction, respectively.

In addition, another test vehicle was designed and fabricated together with other circuits on a standard 8-in p-type silicon wafer of low resistivity $10\ \Omega\cdot\text{cm}$ using the state of the art 0.18- μm CMOS technology. An oxide layer of thickness 26 μm was

Figure 4.3: Setup for frequency domain measurement of on-chip monopoles.

grown on silicon substrate of thickness $750\ \mu\text{m}$ for isolation [23]. Monopole antennas with axial lengths of 1 and 2 mm were implemented using copper layer of $4\ \mu\text{m}$ thickness and $30\ \mu\text{m}$ width. A die photo for the test vehicle using $0.18\ \mu\text{m}$ process is shown in Figure 4.2, where there are dipoles, inverted-F, and loop antennas with complex circuits placed in between.

4.2.2 Measurement Setup and Frequency-Domain Results

The measurement setup consists of a MicroTech probe station and an HP8510XF network analyzer to get the S -parameters in the frequency range of 10-110GHz, as depicted in Figure 4.3. It is seen that the test vehicle wafer is mounted on the metal chuck of the probe station. Having calibrated the network analyzer with the standard calibration kit and procedures, we conducted the reflection measurements to obtain S_{11} and S_{22} and the transmission measurements to obtain S_{12} and S_{21} . The results of reflection measurements at various distances d are displayed in Figure 4.4 for meander monopoles on both high- and low-resistivity silicon wafers of $5\ \text{k}\Omega\cdot\text{cm}$ and $10\ \Omega\cdot\text{cm}$,

respectively. It is evident that S_{11} is insensitive to the T-R separation distance. Over the whole frequency range, there is no sharp resonance dip observed for antennas on the 10 $\Omega\cdot\text{cm}$ silicon wafer. In contrast, sharp resonance dips can be seen at 25 and 75 GHz for meander monopoles on the 5 $\text{k}\Omega\cdot\text{cm}$ silicon wafer. The wideband response of the antennas on the low-resistivity substrates are attributed to the substrate loss and therefore a low- Q resonance network. The matching of monopole antennas on the 5 $\text{k}\Omega\cdot\text{cm}$ silicon wafer over the whole frequency range from 10 to 110 GHz is not good for applications in a real system but is acceptable for the application in the channel characterization. This is because the matching affects the transmitted and received power, so does the performance of the real system; however, the matching will not affect the path loss factor, delay spread and the propagation mechanisms. Moreover, one can locate the S_{11} -matched frequency range into the high gain window to maximize the power transmission [24].

Figure 4.5 shows the transmission coefficient S_{21} for the zigzag monopole antenna pairs on both high- and low-resistivity silicon wafers at the T-R separation of $d = 5$ mm. The high S_{21} windows can be seen in the frequency range from 15 to 30 GHz and 25 to 60 GHz for the low and high-resistivity silicon wafers, respectively. Within the high S_{21} windows, phase responses are linear or nearly linear indicating clearly that the radio signal transmission between the monopole antennas occurs through the propagation of a dominant mode or path [24]. The performance of the antennas are poor in the high frequency range. It is due to the facts that both the antennas and the propagation channel are frequency selective, and the antennas are not designed to

Figure 4.4: Measured S_{11} versus frequency for meander antennas.

operate at frequencies above 60 GHz.

Figure 4.6 shows the effects of metal interference structures on the transmission coefficient between a pair of linear monopole antennas on high-resistivity substrate. It is observed that the existence of metal lines improves gain within the S_{21} window. This is because the periodic layout of the metal lines enhances the band pass characteristic of the intra-chip radio propagation channel [24]. This characteristic can be used wisely to improve antenna transmission gain performance.

Figure 4.7 compares the magnitudes of the transmission coefficient S_{21} measured for zigzag antennas at the T-R separation of $d = 10$ mm on the $10 \Omega\cdot\text{cm}$ silicon wafers fabricated using both $1.2\text{-}\mu\text{m}$ and $0.18\text{-}\mu\text{m}$ CMOS processes. It is seen that the transmission is significantly improved over the frequency range from 20 to 40 GHz, by the $26 \mu\text{m}$ thick oxide layer and better conducting material, which is copper.

(a) High resistivity substrate

(b) Low resistivity substrate

Figure 4.5: Magnitude and phase responses of S_{21} for the zigzag antenna pairs at $d = 5\text{mm}$.

Figure 4.6: Effect of metal interference structures on the magnitude of S_{21} of linear antenna pairs at $d = 5$ mm.

Figure 4.7: Magnitude responses of S_{21} for zigzag antennas at $d = 10$ mm.

4.3 Time-Domain Analysis

Based on observation of reflection and transmission coefficients, the frequency range, which favors signal transmission, can be determined. However, information provided by analysis in frequency domain only is not sufficient for the design of wireless chip area networks. The total power attenuation and the delay spread of channel impulse response (CIR) determine transmitter/receiver gain and number of taps to capture enough energy for the demodulation. Furthermore, the upper limit of data rate is set by the channel time-domain characteristics as well.

The characterization of intra-chip channel in time domain requires a fine resolution to differentiate rays from different paths. Direct measurements could be difficult in designing the extremely narrow transmitted pulse and obtaining high time domain resolution. Due to the Fourier transform relationship between time domain and frequency domain signals, measurement in frequency domain is a good alternative for short-range time domain channel characterization, which requires fine resolution. CIR can be converted from transmission coefficient S_{21} using the inverse discrete Fourier transform (IDFT). The obtained CIR has a corresponding time domain resolution $1/2B$, where B is the measurement frequency span [80]. A high value of B is necessary for a fine time domain resolution, making rays from different paths differentiable. Furthermore, measurement range has to cover the high-gain window, which spreads from 13 to 65 GHz for antennas on high-resistivity substrate [24].

Through observation over the received power delay profile, resistivity of silicon

wafer significantly affects the received signal power. As a comparison, received power delay profiles of zigzag antennas at the T-R separation of $d = 5$ mm are shown in Figure 4.8 for both low and high resistivity silicon wafers. It can be seen that the received power delay profile peak for the antenna pair on the low-resistivity silicon wafer has been heavily attenuated by more than two orders of magnitude, as compared to that for antennas on high-resistivity silicon wafer. Besides, the received power delay profile peak for the low-resistivity case is only a few times above the noise floor at 5 mm. The noise floor is set to 10 dB above average noise. Noise floor for the low-resistivity substrate is 6.4×10^{-7} V², as plotted in Figure 4.8. However, for the high resistivity substrate, noise floor of 8.6×10^{-7} V² cannot be observed as it is around 3 orders of magnitude lower than the signal peak. Further increasing the T-R separation to $d = 10$ mm gives a received power delay profile, which is entirely buried in noise. Generally, there is more than 10 dB extra power loss for monopoles integrated on the low-resistivity silicon wafer than those on the high-resistivity silicon wafer, and this difference can be up to 17 dB in extreme cases, making low-resistivity substrate an inferior candidate in on-chip antenna applications. Therefore, it is highly recommended that the proton implantation technique be used to increase the resistivity of silicon wafer [32, 81] for wireless intra-chip radio communications. The proton implantation technique has negligible degradation on gate oxide integrity [81]. The following analysis will focus on the intra-chip radio propagation channel on the high-resistivity silicon wafer since the low-resistivity silicon wafer leads to a much higher loss, the transmitting power and receiving sensitivity of our measurement setup is limited, and

Figure 4.8: Received power delay profile of the zigzag antenna pairs at $d = 5$ mm: (a) High resistivity substrate (b) Low resistivity substrate.

the propagation mechanisms cannot be well revealed.

By inspection over all the power delay profiles obtained, energy decays completely within 1 ns. To reduce the effect of noise on analysis results, noise component needs to be removed. Therefore, the time segment from 1 to 2 ns is selected to determine the average noise floor. Bins in a power delay profile below certain threshold are considered as no energy, where the threshold is set to be 10 dB above the average noise floor.

4.3.1 Path Loss

To understand the relationship between power attenuation and T-R separation, power loss in dB is plotted over log distance and fitted using (3.5) [74]. The scatter plot and fitted lines for zigzag, meander and linear antennas are shown in Figure 4.9. The

Table 4.1: PL Parameters for Antennas.

	γ	PL_0 (dB)	σ (dB)
Zigzag	1.454	23.7	0.5587
Meander	1.342	26.93	0.8736
Linear	1.411	24.41	0.8276

Figure 4.9: PL versus log distance for zigzag, meander and linear monopole antennas.

respective parameters of (3.5) are summarized in Table 4.1 for the three antennas.

Good fitting qualities of PL can be observed as the standard deviations of the random variable X_σ are quite small. Another interesting observation is that the PL factor γ is significantly lower than the free-space PL factor, which is equal to 2. It implies that signal is not carried through space wave. Instead, the wave propagation is through some manner of guided wave.

Metal interference structures, either in parallel or normal placement, improve transmission as compared to the T-R pairs without metal structures in between. This is because the periodic layout of metal lines enhances the bandpass characteristics of the

Table 4.2: Effects of Interference Structures on PL for Antennas.

	Zigzag	Meander	Linear
No interference	27.322	31.245	26.97
Loose parallel	26.809	28.071	25.501
Dense parallel	25.099	25.872	24.3
Loose normal	22.367	24.6	21.769
Dense normal	24.985	24.453	21.92

intra-chip radio propagation channel. However, other interference structures, such as floating metal lines in both normal and parallel directions, reduces the transmission gain slightly. A metal plate placed between the antenna pair degrades the received signal further [10, 46]. On the other hand, discontinuous metal blocks of $10\ \mu\text{m} \times 10\ \mu\text{m}$ do not reduce transmission gain seriously [46]. PL for antennas with different interference metal lines is compared with no interference situations in Table 4.2. An important observation is that a normal interference structure gives an even lower PL than that by the parallel metal lines, which is opposite to observation made in [10]. However, there is no conflict between the two observations. In [10], the sampled frequency range is below 26.5 GHz. They could not find the high-gain window located roughly from 25 to 60 GHz, which is the dominant range that contributes to the received signal in our study, as shown in Figure 4.6.

Relative angle between transmitting and receiving antennas changes the received signal strength as well. With respect to the relative rotation angle θ , variations of PL are summarized in Table 4.3. As θ increases, due to polarization mismatch, PL gradually increases. The loss by antenna rotation can be up to 4 dB when linear antennas are placed normal to each other.

Table 4.3: Effect of Rotation on PL in dB θ (degrees).

	Zigzag	Meander	Linear
0	28.032	31.142	27.517
30	28.423	31.238	27.226
45	28.784	32.538	28.164
60	30.137	33.391	29.687
90	30.974	33.994	31.624

4.3.2 Delay Spread

Apart from total power attenuation, the delay spread is another important factor for a radio propagation channel. As a measure of effective length of a CIR, the delay spread covers major portion of the received signal energy. For different antennas, the delay spread is plotted over the T-R separation distance in Figure 4.10. It can be observed that delay spread generally increases with the T-R separation, although the delay spread for a specific CIR depends on the surrounding of the T-R pair. In other words, receiver signal energy spreads over a longer time span with increased T-R separation distance.

When interference structures are placed between antenna pairs, it is found that metal lines, either in parallel or normal placement, help reduce delay spread for both zigzag and linear antennas. Another interesting observation is that for all antennas, with parallel interference structures, densely placed metal lines give a lower delay spread than that for loosely placed metal lines. However, for normal interference structures, dense metal lines lead to a higher delay spread than loose metal lines. It is due to the fact that parallel interference structures help guide the wave propagation, while normal metal lines tend to scatter the energy away [10].

Figure 4.10: Delay spread versus the separation distance between the transmitting and receiving antennas.

4.3.3 Propagation Mechanisms

In addition to the characterization of intra-chip radio propagation channels, the understanding of the propagation mechanisms is very important for intra-chip radio communications. With the knowledge of the propagation mechanisms over the intra-chip radio channels, we can design more efficient integrated antennas, minimize electromagnetic interference, etc.

To understand the propagation mechanisms, the first arrival for each CIR is located. It is found that the first peak arrives significantly later than the propagation delay calculated from the space wave, implying again that propagation is through some manner of guided waves. Antennas pairs with parallel interference structure give shorter delay than antennas without interference. In contrast, normal metal lines result in longer

Figure 4.11: Scatter and fitted lines for first arrival locations over distance.

delay than the no-interference situation. For antenna pairs without interference metal lines, the relationship between the first peak location and distance is plotted over linear distance in Figure 4.11. The scatter plot of the first peak location has been fitted into a linear equation and a good fitting quality can be observed, especially for linear and zigzag antennas. The good fitting indicates that the propagation mechanisms are the same for antennas placed at various separation distances.

Generally, there are three types of waves based on which signal can propagate: space wave through air, surface wave by the air-wafer interface, and guided wave within the wafer. Leaky wave is not considered here, because it leaks energy continually into the direction perpendicular to the wafer surface, decreases exponentially over the intra-chip radio channel, and thus contributes to the received signal negligibly in the far-field region. Space wave is supported as if there were no wafer but an infinite

air space. Surface wave occurs near the interface between the air and wafer as if air and wafer extended infinitely into their respective sides. Guided wave is realized by the reflection within the wafer. As the T-R separation increases, surface wave constitutes the dominant contribution because of its cylindrical characteristics as opposed to the spherical behavior of space wave [82] and also the large attenuation of guided wave due to lossy wafer. It is known from [83] that for an integrated antenna on a dielectric substrate of high permittivity there is more energy carried by surface wave than by space wave when the ratio d/λ_0 is greater than 0.045, where d and λ_0 are the substrate thickness and free-space wavelength respectively. With d/λ_0 increasing up to 0.15, surface wave becomes more dominant over space wave. As the high window is in the range of 25 to 60 GHz here, the corresponding d/λ_0 is between 0.053 and 0.127; surface wave dominates in the propagation over the intra-chip channel.

As mentioned above, the PL factor is significantly less than 2; therefore, space wave is impossible to be the dominant contribution to the received signal. The first arrival is not transmitted by space wave, since it arrives much later than free space transmission. Furthermore, the linear relationship between first arrival location and T-R distance excludes the possibility that first arrival is received through a reflected wave. As a result, it can be summarized that space wave contributes negligibly to the received signal and surface wave is the dominant path of received signal. Integrated antennas for intra-chip radio communications should be designed to launch effectively the surface wave rather than space wave.

Chapter 5

BER Analysis of UWB Radio Using BPSK Modulation over Inter-chip Radio Channels

5.1 Introduction

In long-range systems, a wireless network covers a distance on the order of kilometers with a data rate of hundreds of kbps. With a shrinkage in the coverage range, the data rate increases. In the local area network (LAN), a wireless network is able to support a high rate on the order of tens of Mbps. For example, wireless LAN (WLAN) standard 802.11g can cover an indoor distance around 30 meters up to 54 Mbps as released in June 2003 [84]. As the communications distance further reduces, the data rate rockets

up to 600 Mbps over a distance of a few meters [85]. From the range-speed relationship in the evolution of wireless communications, it can be interpreted that with a sub-meter coverage, the communication speed can be improved further, i.e., to Gbps.

Ultrawide band (UWB) technology emerges as a promising candidate for low-cost, high-performance and short-range applications. With a minimum fractional bandwidth of 20% or absolute bandwidth of 500 MHz, the maximum allowed effective isotropic radiated power (EIRP) is -41.3 dBm/MHz within the typical frequency range of interest from 3.1 to 10.6 GHz [86]. For impulse radios, such wide bandwidths can be realized by transmitting extremely narrow pulses at a very low power spectral density (PSD). With a wide bandwidth and a narrow pulse width, the UWB technology offers a variety of competitive advantages: low probability of detection and interception, high resolution capability, through-obstacle penetrating capability and robustness over multipath channel [87, 88]. Therefore, UWB is suitable for indoor high-rate data communications, low-rate data communications and accurate ranging.

On the other hand, in the semiconductor industry, the device feature dimension has been continuously scaled down to allow more components to be integrated into the same chip and to improve device performance. Furthermore, the chip size continues increasing at the same time such that more functions can be integrated into the same chip. However, as the width and thickness of wire interconnects scale down in proportion to the device feature dimension, down scaling also results in problems of wire interconnects, especially at high frequencies, e.g., increased time delay, signal

attenuation and dispersion, degraded bit-capacity, crosstalk, etc [7, 12]. To tackle the problems of wire interconnects in the age of high-speed semiconductor technology, wireless chip area network (WCAN) proposed by Zhang is an innovative application which provides high data rates in close proximity [16, 20]. Apart from the application as an alternative for wire interconnects, a short-range high data rate wireless communication system can be used to monitor and to diagnose computer system as well [89]. Wireless interconnects can exist in concurrency with wire interconnects as a backup communication channel when mission-critical applications are running. An intra-chip bit-error rate (BER) evaluation and an inter-chip demonstration have been performed [16, 18]. In order to fully explore the capacity of wireless inter-chip channels, frequency domain data have been sampled inside computer enclosures over 3.1 to 10.6 GHz for inter-chip channels and converted into time domain using the inverse discrete Fourier transform (IDFT). Channel characteristics were obtained based on statistical modeling and the inter-chip channel has been simulated for a typical inter-chip radio channel [80], as described in Chapter 3.

As the inter-chip channel contains dense multipaths, inter-symbol interference (ISI) becomes a significant performance limitation. Conventionally, ISI can be reduced by using orthogonal frequency-division multiplexing (OFDM) in a multi-carrier communication system [90, 91], or using various equalizers in pulse-based systems [92, 93, 94, 95]. In this chapter, a relatively simple algorithm is proposed to alleviate ISI in an impulse-based UWB radio. More importantly, for a transceiver to be designed to fully explore the communications radio channel capacity, it is necessary to perform

Figure 5.1: The block diagram for an inter-chip wireless communications system.

a BER analysis to find out the supported data rates. Therefore, based on the inter-chip wireless channel modeled in [80], BER analysis will be performed for practical communications scenarios taking various noise sources into consideration.

This chapter is organized as follows. In Section 5.2, the communications system model is described. The proposed ISI reduction technique is presented in Section 5.3. Based on the proposed ISI-reducing technique, analytical BER expressions and numerical results of BER analysis for inter-chip channels are derived in Section 5.4.

5.2 System Description

With the binary phase-shift keying (BPSK) modulation adopted in the evaluation of BER performance for intra-chip interconnect systems and the design for wireless inter-chip interconnects [16, 18], we consider the same modulation scheme in this chapter. Figure 5.1 shows the block diagram of the inter-chip wireless communications system under consideration. The modulating signal $\{d_j\}_{j=-\infty}^{\infty}$ is an independent and identically-distributed (iid) random variable and can be ‘0’ or ‘1’ for binary signalling.

Through the modulator of BPSK, the transmitted signal $s_{tr}(t)$ can be expressed as

$$s_{tr}(t) = \sum_{j=-\infty}^{\infty} \sqrt{A} \beta_j \omega_{tr}(t - jT_f) \quad (5.1)$$

where T_f is the pulse repetition frame time and $\omega_{tr}(t)$ is the energy normalized transmitted pulse with a duration T_m . A is to adjust the transmitted power. The modulation signal β_j for the j th pulse has a mapping with the source signal d_j as

$$\beta_j = 2 \times d_j - 1 = \begin{cases} -1, & d_j = 0 \\ +1, & d_j = 1 \end{cases} \quad (5.2)$$

The channel impulse response $h(t)$, including the effects of both transmitting and receiving antennas, can be expressed as

$$h(t) = \sum_{l=0}^{L-1} \alpha_l \delta(t - \tau_l) \quad (5.3)$$

where α_l and τ_l are the signal attenuation and delay for the l th path. $\delta(t)$ is the Dirac delta function and L is the total number of multipaths present. The channel impulse response can be obtained based on the work presented in Chapter 3 [80].

The received signal at the input of the receiver correlator can be obtained as

$$\begin{aligned}
r(t) &= s_{tr}(t) \otimes h(t) + n(t) \\
&= \sum_{j=-\infty}^{\infty} \sqrt{A} \beta_j \omega_{rec}(t - jT_f - \tau_d) + n(t)
\end{aligned} \tag{5.4}$$

where τ_d the propagation delay between the transmitter and receiver involved and $n(t)$ is the additive white Gaussian noise (AWGN) characterized by a mean zero and a two-sided PSD $N_0/2$. The notation $\otimes$ denotes the convolution operation. $\omega_{rec}(t)$ is the received pulse waveform including effects of the communications channel and both antennas

$$\begin{aligned}
\omega_{rec}(t - jT_f - \tau_d) &= \omega_{tr}(t - jT_f) \otimes h(t) \\
&= \sum_{l=0}^{L-1} \alpha_l \omega_{tr}(t - jT_f - \tau_l)
\end{aligned} \tag{5.5}$$

By assuming perfect knowledge of the communications channel has been obtained, the decision variable Z_j at the synchronized receiver can be obtained as

$$Z_j = \int_{\tau_r + (j-1)T_f}^{\tau_r + jT_f} r(t)v(t) dt \tag{5.6}$$

where τ_r is the receiver time reference and $v(t)$ is the locally generated mask signal to be correlated with the received signal. The decision variable Z_j is then fed into a

comparator to perform estimations of the transmitted bits $\{\hat{d}_j\}_{j=-\infty}^{\infty}$ according to

$$\hat{d}_j = \begin{cases} 0, & Z_j < 0 \\ 1, & Z_j > 0 \end{cases} \quad (5.7)$$

5.3 ISI Reduction

The transmitted basic pulse is chosen as a polypulse described by

$$\omega_{tr}(t) = \frac{1}{\sqrt{E_p}} \sin(2\pi f_e t) \sin(2\pi f_c t) \quad (5.8)$$

where $f_e = 1/T_e$ and $f_c = 1/T_c$ are the envelope and carrier frequencies, respectively. E_p is to normalize the energy of the pulse to unity. The duration of the pulse is limited by $t \in [0, T_e/2]$. In order to meet requirements of the Federal Communications Commission (FCC) UWB emission mask and a high data rate, we set $T_e = 0.75$ ns and $T_c = 0.15$ ns. With this polypulse, the -10 dB cut-off frequencies are at 3.9793 and 9.6166 GHz respectively, leading to a -10 dB bandwidth as 5.6373 GHz.

The correlator mask signal at the receiver can be written as

$$v(t) = \sum_{j=-\infty}^{\infty} \omega_{cor}(t - jT_f - \tau_r) \quad (5.9)$$

where $\omega_{cor}(t)$ is a energy-normalized pulse waveform used for correlation and τ_r is

the receiver time reference. With an All-RAKE receiver implementation, $\omega_{cor}(t)$ is the same as $\omega_{rec}(t)$. Therefore, from (5.6), the decision variable Z_j for the j th pulse can be expanded as

$$\begin{aligned}
 Z_j &= \int_{\tau_r+(j-1)T_f}^{\tau_r+jT_f} \left[\sum_{m=-\infty}^{\infty} \sqrt{A}\beta_j \omega_{rec}(t - jT_f - \tau_d) + n(t) \right] \times v(t) dt \\
 &= \sum_{m=-\infty}^{j-1} \sqrt{A}\beta_m \int_{\tau_r+(j-1)T_f}^{\tau_r+jT_f} \omega_{rec}(t - mT_f - \tau_d) \times v(t) dt \\
 &\quad + \sqrt{A}\beta_j \int_{\tau_r+(j-1)T_f}^{\tau_r+jT_f} \omega_{rec}(t - jT_f - \tau_d) \times v(t) dt \\
 &\quad + \int_{\tau_r+(j-1)T_f}^{\tau_r+jT_f} n(t) \times v(t) dt \\
 &= Z_{j,ISI} + Z_{j,D} + Z_{j,n}
 \end{aligned} \tag{5.10}$$

where $Z_{j,ISI}$, $Z_{j,D}$ and $Z_{j,n}$ are the contributions in Z_j from ISI, the desired signal and Gaussian noise. With the channel impulse response length T_{ch} defined by the first and the last arrivals of the channel impulse response above noise floor, a metric k can be defined to quantify the severity of ISI

$$k = \lceil (T_m + T_{ch})/T_f \rceil \tag{5.11}$$

where $\lceil x \rceil$ rounds x up to the nearest integer. $k - 1$ gives the number of preceding pulses, whose residuals affect the decision of the j th pulse, when j is not less than k .

Therefore the ISI-contributed term in Z_j can be rewritten as

$$Z_{j,ISI} = \sum_{m=j-k+1}^{j-1} \sqrt{A}\beta_m \int_{\tau_r+(j-1)T_f}^{\tau_r+jT_f} \omega_{rec}(t - mT_f - \tau_d) \times v(t) dt \quad (5.12)$$

The ISI term $Z_{j,ISI}$ will be non-zero with the value of k greater than unity. If the residuals of the preceding $k - 1$ bits are strong enough, a wrong estimation of the j th transmitted pulse may be resulted. For different values of j , the number of preceding pulses, which affect the j th pulse, can be expressed as

$$\begin{cases} k - 1, & j \geq k \\ j - 1, & j \leq k - 1 \end{cases} \quad (5.13)$$

To illustrate the effects of residuals from the preceding pulses on the pulse under consideration, Figure 5.2 depicts the mixer output where k has a value of 5. The transmitted bits are 101010. Therefore, the correlator output should be $+ - + - + -$ for a correct decision making. However, the obtained results are $+ + - + - +$, i.e., all the received bits are incorrectly estimated except for the first bit where there is no ISI.

Conventionally, ISI problems can be alleviated using approaches of OFDM techniques in a multi-carrier system [90, 91] or various equalizers in pulse-based systems [92, 93, 94, 95]. For the adopted polypulse, the received signal preserves the same zero-crossing rate as the mask signal except at transitions in the successively transmitted bits. As the transmitted signal passes through a multipath radio channel, the

Figure 5.2: An example for effects of ISI.

received signal is actually a sum of replicas of the transmitted signals with different delays and gains. The transmitted signal is a sinusoidal signal with an envelope as half a period of another sinusoidal signal. Therefore, the added replicas still possess the same zero-crossing rate but with a different phase and gain, as compared to the transmitted signal. A transition in the consecutively transmitted bits will result in a distorted zero-crossing rate in $r(t)$ with respect to the mask signal $v(t)$ due to the residuals of the preceding bit with a different sign, and therefore affect the decision making. In other words, if the consecutively transmitted bits are the same, the decision making will be correct even when there exists ISI.

On the other hand, it is known that the received energy generally decays exponentially over time. Most of the received energy is actually confined in the beginning portion. Therefore, by finding an “optimal” position for the integral window, i.e., by

Figure 5.3: $Z_{j,r}(\tau_{sh})$ over time shift τ_{sh} for the j th pulse as ‘0’ and ‘1’. τ_{sh} is in the unit of T_f .

adjusting τ_r in (5.6), the integral can be performed with a focus in the desired pulse whereas effects of the preceding and succeeding pulses can be limited to a very low level. More specifically, the receiver time reference τ_r can be re-written as

$$\tau_r = \tau_d + \tau_{sh} \quad (5.14)$$

where τ_d is to synchronize the receiver with $r(t)$ and τ_{sh} is to further dynamically search for the “optimal” integral window position. To avoid distortions of many succeeding pulses, we limit the range of τ_{sh} as $\tau_{sh} \in [0, T_f)$. By denoting the decisional variable due to the received signal as $Z_{j,r} = Z_{j,ISI} + Z_{j,D}$, $Z_{j,r}$ is a function of $k + 1$ pulses for $j \geq k$: the preceding $k - 1$ pulses, the j th pulse under investigation and the $(j + 1)$ th pulse due to shifting of the integral window position. The maximum number

of possible $Z_{j,r}$ can be derived as

$$P = \begin{cases} 2^{k+1}, & j \geq k \\ 2^{j+1}, & j \leq k-1 \end{cases} \quad (5.15)$$

Figure 5.3 depicts the function $Z_{j,r}(\tau_{sh})$ over the shifted time τ_{sh} with k equal to 5. It can be observed that $Z_{j,r}(\tau_{sh})$ is symmetrical about the horizontal axis. The symmetry corresponds to the balanced source signal $\{d_j\}_{j=-\infty}^{\infty}$. For instance, the modulating source sequences 101101 and 010010 are mirrors of each other and their $Z_{j,r}(\tau_{sh})$ will be symmetrical about the horizontal zero axis. As a result, from (5.15), the maximum number of possible $Z_{j,r}$ can be reduced to

$$P = \begin{cases} 2^k, & j \geq k \\ 2^j, & j \leq k-1 \end{cases} \quad (5.16)$$

To obtain the optimal value of τ_{sh} , Figure 5.4 gives the plot of $Z_{j,r}(\tau_{sh})$ when the j th pulse is for '1' and the vertical dashed line indicates the optimal time shift $\tau_{sh,opt}$. The desired correlator output is positive for a correct decision making. A more positive $Z_{j,r}(\tau_{sh})$ is preferred against noise during the decision making. Therefore, for the p th possible combination of the modulating source bits, where $p \in P$ as shown in (5.16), an algorithm for obtaining the optimal time shift $\tau_{sh,opt}$ can be described as

Figure 5.4: $Z_{j,r}(\tau_{sh})$ over time shift τ_{sh} for the j th pulse as ‘1’. τ_{sh} is in the unit of T_f . The vertical dashed line represents $\tau_{sh,opt}$.

$$\tau_{sh,opt} = \arg \max_{\tau_{sh}} \left\{ \arg \min_p \{Z_{p,r}(\tau_{sh})\} \right\} \quad (5.17)$$

More specifically, Figure 5.5 gives a flow chart on how to find the $\tau_{sh,opt}$. For different values of p , the minimum values of $Z_{p,r}(\tau_{sh})$ at each τ_{sh} are stored in buffer 2. The maximum value in buffer 2 corresponds to the position of $\tau_{sh,opt}$. How close to theoretical maximum for the actually obtained $\tau_{sh,opt}$ depends on the shifting resolution during the searching process for the optimum integral window position. Besides, if there exists a relatively flat region near the $\tau_{sh,opt}$ point as the segment of $0.65T_f$ to $0.8T_f$ in Figure 5.4, the requirement on shifting resolution could be relaxed. Furthermore, it should be noted that scaling the mask signal $v(t)$ with a constant does not change the sign of $Z_{j,r}$. Therefore, for a transmitted bit as ‘1’, any constant neg-

Figure 5.5: Flow chart for $\tau_{sh,opt}$ searching.

ative $Z_{j,r}(\tau_{sh})$ over the entire range of τ_{sh} indicates an error decision, which cannot be solved by the proposed technique of shifting integral window position. The error decision is caused by the overlapping of successively transmitted pulses, leading to an uncontrollable ISI. In this case, the solution is to lower the transmission bit rate or use other means to reduce the ISI. It is worthwhile to mention that apart from the BPSK modulation scheme, the technique of dynamically shifting integral window position has been verified in binary pulse position modulation (PPM) scheme as well.

5.4 BER Analysis Over Inter-Chip Channels

For certain combination of the transmitted modulating source bits, the probability of bit error $P_{e,j}$ can be expressed as a function of Z_j

$$P_{e,j} = Q\left(\frac{E(Z_j)}{\text{std}(Z_j)}\right) \quad (5.18)$$

where $E(x)$ gives the expected value of x and std the standard deviation. The Q function is defined as

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-t^2/2} dt \quad (5.19)$$

From (5.10) and (5.12), $E(Z_j)$ can be obtained as

$$\begin{aligned} E(Z_j) &= E\left(\sum_{m=j-k+1}^{j+1} \sqrt{A}\beta_m \int_{\tau_d+\tau_{sh,opt}+(j-1)T_f}^{\tau_d+\tau_{sh,opt}+jT_f} \omega_{rec}(t - mT_f - \tau_d) \times v(t) dt\right) \\ &\quad + E\left(\int_{\tau_d+\tau_{sh,opt}+(j-1)T_f}^{\tau_d+\tau_{sh,opt}+jT_f} n(t) \times v(t) dt\right) \\ &= \sum_{m=j-k+1}^{j+1} \sqrt{A}\beta_m \int_{\tau_d+\tau_{sh,opt}+(j-1)T_f}^{\tau_d+\tau_{sh,opt}+jT_f} \omega_{rec}(t - mT_f - \tau_d) \times v(t) dt \end{aligned} \quad (5.20)$$

And the variance of Z_j can be derived as

$$\begin{aligned}
Var(Z_j) &= Var \left(\sum_{m=j-k+1}^{j+1} \sqrt{A} \beta_m \int_{\tau_d + \tau_{sh,opt} + (j-1)T_f}^{\tau_d + \tau_{sh,opt} + jT_f} \omega_{rec}(t - mT_f - \tau_d) \times v(t) dt \right) \\
&\quad + Var \left(\int_{\tau_d + \tau_{sh,opt} + (j-1)T_f}^{\tau_d + \tau_{sh,opt} + jT_f} n(t) \times v(t) dt \right) \\
&= \frac{N_0}{2} R_{vv}(0)
\end{aligned} \tag{5.21}$$

where $R_{vv}(\tau)$ is the auto-correlation function of the reference mask signal $v(t)$. Therefore, the general probability of error bits for the j th received pulse can be written as

$$P_{e,j} = \frac{1}{P} \sum_{i=1}^P Q \left(\frac{E(Z_{j,i})}{std(Z_{j,i})} \right) \tag{5.22}$$

where P is defined in (5.16). In the case when the total number of bits transmitted is N , the probability of error bits can be obtained as

$$P_e = \frac{1}{N} \sum_{i=1}^N P_{e,i} \tag{5.23}$$

The Q function in (5.22) can be re-written in the form of transmitted bit energy and the noise PSD $N_0/2$. The received pulse amplitude $\omega_{rec}(t)$ is proportional to the square root of the transmitted bit energy E_{TX}

$$\omega_{rec}(t) = B\sqrt{E_{TX}} \quad (5.24)$$

where B is an unknown constant. Meanwhile, $E(Z_j)$ is in proportion to the received pulse amplitude as in (5.20)

$$E(Z_j) = C \times \omega_{rec}(t) \quad (5.25)$$

where C is another constant. Combining (5.24) and (5.25)

$$\begin{aligned} E(Z_j) &= C \times B \times \omega_{rec}(t) \\ &= D\sqrt{E_{TX}} \end{aligned} \quad (5.26)$$

D is the product of B and C . Therefore the Q function in (5.22) can be modified as

$$\begin{aligned} Q\left(\frac{E(Z_j)}{std(Z_j)}\right) &= Q\left(\frac{D_j\sqrt{E_{TX}}}{\sqrt{(N_0/2)R_{vv}(0)}}\right) \\ &= Q\left(\sqrt{\frac{E_{TX}}{N_0}} \frac{D_j}{\sqrt{0.5R_{vv}(0)}}\right) \end{aligned} \quad (5.27)$$

D_j , the constant D for the j th pulse, can be obtained for each combination of

the modulation source bits. The total number of D can be obtained from (5.16) as $\sum_{i=1}^k 2^i = 2(2^k - 1)$. For the inter-chip channel with the value of k as 5, only 372 bits are required to determine the optimal shift time $\tau_{sh,opt}$.

By observing (5.23), the BER performance is a function of the transmitted bits number. However, through calculation, it is found that the probability of error bits for the k th bit dominates for a large number of bits transmitted. A negligible effect of N in BER performance is found for $N > 10$. In practical communications, the inequality can always be satisfied. In order to verify the BER analysis derived above, Monte Carlo simulations have been performed. Figure 5.6 compares the theoretical BER curve in a solid line with the Monte Carlo results in solid dots for a wireless inter-chip channel at 228 mm with a data rate at 650 Mbps. To ensure the accuracy, the Monte Carlo simulations run up to 1.1×10^6 bits. An excellent matching between the solid-line curve and the solid dots validates the analytical BER expression.

For the application of wireless interconnects inside computer casings, the wireless propagation channel is shielded almost completely by the metal enclosure. The communications channel can be considered as quasi-static. Hence, the rate of channel estimation can be at a low level. Furthermore, co-channel interfering sources from outside is negligible. In this case, we consider two major noise sources: thermal and switching noise. The thermal noise PSD can be calculated using

$$N_{0,Th} = k_B(T_{Ant} + T_0(F - 1)) \quad (5.28)$$

Figure 5.6: Theoretical BER plot (solid line) and Monte Carlo verification (solid dot) at T-R separation 228 mm.

where k_B , T_{Ant} , T_0 and F are the Boltzmann constant, antenna temperature (taken as 320 K due to the hot environment), standard temperature (290 K), and noise factor. Noise figure (NF), noise factor in dB, is around 5–8 dB for a UWB receiver [96]. Therefore, the thermal noise PSD can be obtained as -165.91 dBm/Hz with an assumption that NF is 8 dB over the 3.1–10.6 GHz band.

Figure 5.7: Switching noise measurement setup.

In order to obtain an estimation of the switching noise PSD, we use a monopole

planar UWB antenna [72] to sample the noise spectrum while a computer is running at full capacity. A leading-edge NEC dual-core commercial computer, with a CPU frequency 3.0 GHz, is used for measurement as shown in Figure 5.7. The switching noise occurs at harmonics of the fundamental frequency 1.5 GHz. The 3rd to 7th harmonics fall into the range of 3.1 to 10.6 GHz. The 3rd harmonic at 4.5 GHz is recorded as -89.93 dBm whereas all other harmonics beyond the 3rd one fall below the noise floor and therefore cannot be detected. With the measured harmonics, the switching noise PSD S can be obtained as

$$S = \sum_i \sum_j \frac{\chi_{ij} A_{ij}^2}{2} / B_W \quad (5.29)$$

where χ_{ij} is the i th coupling factor from the j th switching noise sources and A_{ij} is the amplitude of the i th harmonic from the j th switching noise source within the system bandwidth B_W [18]. Therefore, by spreading the switching noise over the frequency span of 3.1 to 10.6 GHz, the switching noise PSD S can be obtained as -188.58 dBm/Hz. In multi-chip modules, typically there is more one switching noise source. However, generally the switching noise is 10 dB lower than thermal noise even for integrated antennas, as the switching noise is common-mode in nature and it can be effectively suppressed by balanced antenna structures and differential circuit architectures [17]. When the antenna used for sampling is not integrated into chips, the measured switching noise is even lower. Combining both noise sources, the total noise PSD is obtained as $N_{0,n} = N_{0,Th} + S = -165.88$ dBm/Hz.

Figure 5.8: BER over E_{TX}/N_0 over different distances with a data rate at 650 Mbps. The T-R distances are: 62, 84, 133, 156, 162, 208, and 252 mm.

When the transmitter-receiver (T-R) propagation distance increases, path loss increases logarithmically, leading to lower received bit energy. For a data rate of 650 Mbps, Figure 5.8 shows BER curves for the T-R distances at 62, 84, 133, 156, 162, 208, and 252 mm along the BER deteriorating direction. It can be observed that around 21 dB more energy is required to achieve the same BER performance (10^{-6}) for the largest T-R separation, as compared to the shortest one. For the bit rate of 650 Mbps, the transmitting power Pow in dBm is related to the transmitted bit energy E_{TX} of mJ in log scale by

$$\begin{aligned} Pow &= E_{TX} - 10 \log_{10}(T_f) \\ &= E_{TX} + 88.13 \end{aligned} \tag{5.30}$$

Figure 5.9: BER over E_{TX}/N_0 over different data rates with T-R separation as 235 mm. Data rates: 450, 500, 550, 600, 650, and 700 Mbps.

As a result, the power-to-noise ratio Pow/N_0 varies from 129.03 to 150.11 dB over the variations of the T-R separation distances. With the noise PSD including both thermal and switching noise as described above, the corresponding transmitting power required varies from -36.85 to -15.77 dBm if the desired BER performance is better than 10^{-6} .

Apart from the bit energy and T-R separation distance, BER performance is a function of the data rate as well. Lowering the data rate is to increase the frame time T_f . Correspondingly, k , the channel length in terms of number of pulses, becomes small, which implies that less preceding bits have effects on the pulse under investigation. Generally, this leads to a reduced ISI effect. At a propagation distance of 235 mm, Figure 5.9 shows the BER plot over data rate at 450, 500, 550, 600, 650, and 700 Mbps along the BER worsening direction. It can be observed that for the same channel

impulse response (CIR), a variation around 15 dB in E_{TX}/N_0 is resulted when the bit rate is changed from 450 to 700 Mbps.

To obtain the insight of the power-performance relationship, it is necessary to perform a link budge analysis. Taking the longest distance 252 mm as an example, the required transmitting power Pow' is -15.77 dBm to achieve a BER lower than 10^{-6} for a data rate at 650 Mbps. The required transmitting power covers the path loss and gains of the transmitting and receiving antennas. Under the FCC regulations, the PSD of a transmitted UWB signal over 3.1 to 10.6 GHz can be up to -41.3 dBm/MHz, i.e., $P_{max} = -2.55$ dBm in total. The link margin G_m can be expressed as

$$G_m = P_{max} - Pow' + G_r \quad (5.31)$$

where G_r is the receiver gain, which is taken as 15 dB [18]. Therefore, the link margin is calculated as 28.22 dB. The implementation margin in [18] is assumed as 15 dB to cover the loss due to inevitable metal lines between the transmitter and receiver antennas and other marginal losses. The obtained high link margin G_m suggests that the transmitted power can be much lower than the maximum possible transmitted power, though, in practice, the maximum transmitted power can never be -2.55 dBm as derived.

Chapter 6

Synchronization Scheme for Impulse-Based UWB

6.1 Introduction

Ultrawide band (UWB) technology is a promising candidate for low cost, high performance, and short range applications [97]. In any application, the operation with UWB has to occupy a fractional bandwidth not less than 20% or an absolute bandwidth at least 500 MHz. The typical frequency range of interest is from 3.1 to 10.6 GHz, within which the maximum allowed effective isotropic radiated power (EIRP) is -41.3 dBm/MHz, according to the emission mask set by the Federal Communications Commission (FCC) in April 2002 [86]. In traditional UWB systems, i.e., impulse radios, such huge bandwidths are realized by transmitting trains of extremely narrow

pulses at very low power spectral density (PSD) [88, 98]. Due to the large bandwidth and narrow pulse width, UWB technology offers various competitive features: low probability of interception, high resolution capability, through-obstacle penetrating property, and robustness over multipath channel. With these characteristics, UWB can be used for high-rate indoor data communication, low-rate data communication, and accurate ranging [18, 20, 87, 97, 99, 100]. There are two competing schemes for UWB, namely direct sequence (DS) UWB and multi-band (MB) UWB. DS-UWB, also referred as impulse radio (IR) UWB, transmits single-band impulses occupying the whole UWB bandwidth, whereas MB-UWB partitions the UWB bandwidth into sub-bands, each of which at least 500 MHz. With the IR-UWB implementation, relatively simple transceiver architectures can be used, and therefore the resulted hardware cost will be lower. On the other hand, the adopted extremely narrow pulse poses great challenges on synchronization in IR-UWB.

A brief overview of synchronization algorithms for DS-UWB is provided in [101]. The matched filter (MF) synchronization based on maximum-likelihood (ML) estimation requires that the input serial signal be correlated with all possible pulse positions of locally generated template replicas. All correlators operate simultaneously and a large data observation pool can be obtained, making MF synchronization scheme the fastest in acquisition speed and the simplest method in theory. However, the complexity and cost in hardware implementation is prohibitive in many practical systems. In practical communication systems, sliding correlator is often used to serially search for the position of received pulse [100]. More closely on the circuit-level implementation

of synchronization with a received impulse, a two-step synchronization method based on a sliding correlator was proposed [102]. Coarse and fine step sizes are used in signal acquisition and tracking stages, respectively. Another synchronization technique based on a sliding correlator used two sample-and-hold (S/H) circuits to lock to the zero-crossing point of the received pulse [103, 104]. Synchronization is performed in two steps: search mode detects the crossover point and track mode maintains synchronization using a feedback control loop. Furthermore, a synchronization scheme based on delay-locked loop (DLL) has been developed as well [105, 106]. With the product of a Gaussian second-order monocycle and its replica delayed by the mainlobe width as a template at receiver, a positive slope was obtained in the correlation of received pulse and the local template. A negative feedback loop can be formed based on the correlation property and realized in a DLL. Finally a synchronization scheme based on phase and frequency synchronizations was briefly explained for synchronization in a wireless intra/inter-chip system [107]. The pulse used for analysis was the Gaussian second order pulse and the synchronization step size was limited by the pulse width in phase synchronization.

Due to the finite step size of a sliding correlator, synchronization for UWB cannot always be obtained perfectly, leading to a performance loss in demodulation. In the DLL-based synchronization scheme, the maximum step size required is half mainlobe width of the pulse adopted [105]. To achieve a better performance, an even smaller step size is needed and more branches of correlators are desired, therefore resulting in tough issues in hardware design and a high cost with sub-nanosecond pulses [106].

Another concern is the frequency offset between transmitter and receiver oscillators. As a result, a synchronization scheme with frequency tuning capability could be a better choice.

In conventional wireless and communication systems, a phase-locked loop (PLL) is widely used to synchronize the local oscillator at receiver to a received signal. Techniques of phase locking have been well developed from control-centric theory to monolithic IC implementations [108, 109, 110]. Therefore, it is unsurprising to bring in the concept of PLL to UWB system synchronization, if possible.

An improved synchronization scheme based on a sliding correlator and a PLL will be presented and analyzed. As rationales of the synchronization scheme, properties of Gaussian group pulses will be investigated. Concepts of a PLL will be applied to the analysis of the synchronization technique. The modified synchronization scheme can be proved as superior to the DLL-based method and a different conclusion on synchronization step size will be drawn as compared to the existing work performed in [107]. As antennas and communication channels introduce distortion to received pulses, it is necessary to investigate impairments of the two factors on the presented synchronization scheme as well.

The chapter is organized as follows. Section 6.2 presents the analysis of the synchronization scheme, where the basic properties of Gaussian group pulses, working principles of the synchronization scheme, and tradeoffs in selecting the order of Gaussian pulses are discussed. Effects of antennas and communication channels are exam-

ined in Section 6.3, including an approach for evaluating the effects of UWB antennas and freespace channel on the received pulse, impairments of distortions on received pulses and therefore the synchronization scheme, and simulations of practical communications over different UWB multipath channels.

6.2 Analysis of the Synchronization Scheme

Different orders of Gaussian pulse have been used in UWB communication systems. Gaussian second (G2) and fifth (G5) derivatives are popular choices [18, 111]. We first analyze Gaussian pulse properties based on G5 pulse, and extend the analysis to other orders of Gaussian monocycles in the subsequent parts.

6.2.1 Basic Properties of Gaussian Pulse

The G5 pulse, as expressed in (6.1), has the parameters A_{mp} for signal power adjustment and σ^2 as the variance of a Gaussian distribution. By defining the shaping factor as $\alpha = 2\sigma\sqrt{\pi}$ and setting $\alpha = 0.714$ ns, the temporal waveform with a unity absolute peak for G5 is given in Figure 6.1.

$$G5(t) = A_{mp} \left(-\frac{t^5}{\sqrt{2\pi}\sigma^{11}} + \frac{10t^3}{\sqrt{2\pi}\sigma^9} - \frac{15t}{\sqrt{2\pi}\sigma^7} \right) \times \exp\left(-\frac{t^2}{2\sigma^2}\right) \quad (6.1)$$

Figure 6.1: The normalized temporal waveform of a G5 pulse.

The -10 dB bandwidth of the pulse is over 998.8 MHz to 2.673 GHz. It is possible to adjust the shaping factor such that no filtering is required to meet the FCC indoor emission mask [111]. However, for the application of wireless inter-chip interconnects [80], transmitters are expected to radiate within the closed metal boundary. Therefore, interferences to external devices can be neglected. Moreover, as we will prove, by setting the shaping factor to satisfy the FCC indoor mask, the generated pulse will be much narrower and synchronization for such a system will be more difficult.

To receive information from a transmitter using a sliding correlator, correlation properties between the received pulse and the local template play a significant role. For both the local template and the received pulse as G5 pulses, Figure 6.2 gives the auto-correlation $R_{55}(\tau)$ of the G5 pulse, where the horizontal solid line at 0.4068 indicates

Figure 6.2: $R_{55}(\tau)$: normalized auto-correlation of G5; solid horizontal line: $R_{55,th}$.

the highest sidelobe level $R_{55,th}$. During synchronization, the sidelobe level sets a discriminating threshold V_{th} for finding the relative position between the local template and the received pulse. The difference between mainlobe and the highest sidelobe amplitudes should be as large as possible such that the mainlobe can be easily located against noise and sidelobes for synchronization and demodulation purposes. Due to the symmetry of G5 pulse, $R_{55}(\tau)$ has an even symmetry with respect to the relative delay τ , i.e., when the local template leads or lags the received pulse by the same amount of time, the value of $R_{55}(\tau)$ remains unchanged. To achieve synchronization, the sliding correlator step size $\Delta\tau$ has to be smaller than the effective mainlobe width τ_e , which is defined by mainlobe width intercepted by $R_{55,th}$. More specifically, τ_e can be described as

$$R_{55}(\tau) > R_{55,th}, \forall \tau \in \tau_e \quad (6.2)$$

Figure 6.3: $R_{56}(\tau)$: the normalized cross-correlation of G5 and G6. Vertical lines: τ_e region of interest from -100 ps to $+100$ ps.

In this particular case, the intercepting points are located ± 100 ps, leading to a maximum $\Delta\tau$ as 200 ps for the sliding correlator.

With $\Delta\tau$ and V_{th} set by $R_{55,th}$, another interesting property between Gaussian fifth and sixth (G6) derivatives can be explored. Unlike the G5 pulse with an odd symmetry, a G6 pulse has an even symmetry. Figure 6.3 depicts the normalized cross-correlation $R_{56}(\tau)$ between G5 and G6 pulses with respect to the relative delay τ , where R_{xy} is the correlation between signal x and y . Instead of the even symmetry for $R_{55}(\tau)$, $R_{56}(\tau)$ has an odd symmetry with respect to τ . More importantly, within the region of τ_e of $R_{55}(\tau)$, i.e., ± 100 ps, $R_{56}(\tau)$ monotonically increases, resulting in a positive slope. $R_{56}(\tau)$ has a value of zero when G5 and G6 pulses are aligned perfectly, as G5 and G6 pulses are of odd and even symmetries, respectively. A similar monotonic region has been obtained for a Gaussian second derivative in the analysis for an analog

impulse radio multiple-access receiver in [88].

In the above analysis, it is assumed particularly that the transmitted signal is a G5 pulse. However, it has been examined that the aforementioned discussions of auto- and cross- correlations are valid for all the orders of Gaussian group pulses. Yet, there are some differences over the change of Gaussian pulse order n . With an increase in n , Gaussian pulses have more and higher sidelobes, but narrower mainlobes, resulting in higher sidelobes, narrower mainlobes and therefore lower values of τ_e in the auto correlations $R_{nn}(\tau)$ and narrower regions of τ_m in the cross correlations $R_{n,n+1}(\tau)$. It therefore implies that for a given shaping factor α , a higher order of Gaussian pulse needs a sliding correlator with a smaller step size, imposing more stringent requirements in hardware implementation. For α as 0.714 ns, values of τ_e in $R_{nn}(\tau)$ and τ_m in $R_{n,n+1}(\tau)$ are depicted in Figure 6.4 for Gaussian pulses from the first to the fourteenth derivatives. Unlike for Gaussian pulses with order n greater than 2, for the first and second Gaussian derivatives, τ_m is lower than τ_e . As we will see in next subsection, the maximum value of $\Delta\tau$ is set by the lower of τ_e and τ_m .

6.2.2 Synchronization Scheme

A synchronization scheme based on phase and frequency synchronizations has been proposed in [107]. But neither analysis on Gaussian pulse properties nor descriptions of the circuit working principle are provided. Moreover, as we will present in this section, the sliding correlator step size should be limited by the smaller of τ_e and τ_m ,

Figure 6.4: The values of τ_e and τ_m of Gaussian pulses from order 1 to 14.

instead of the pulse width. We will analyze the frequency synchronization in analogy to a PLL as well.

The block diagram for the synchronization scheme is shown in Figure 6.5. For an IR-UWB communication system based on time-hopping (TH), the transmitted signal $s^{(k)}(t)$ for user k can be expressed as [112]

$$s^{(k)}(t) = \sum_{j=-\infty}^{\infty} A \omega_{tr}(t - jT_f - c_j^{(k)}T_h - \delta \alpha_{\lfloor j/N_s \rfloor}^{(k)}) \quad (6.3)$$

where $\omega_{tr}(t)$ is the transmitted waveform, T_f is the nominal pulse repetition period, and T_h is the chip duration, which is greater than pulse width T_c for a pulse position modulation (PPM). Each symbol has N_s pulses. δ is the modulation index for PPM. The decimal codes $\{c_j^{(k)}\}$ are pseudo-random codes unique for user k in TH-

Figure 6.5: Block diagram for the synchronization scheme in an IR-UWB system.

UWB multiple-access scheme. The pulse amplitude is represented by A . In TH-PPM, $\delta\alpha_{\lfloor j/N_s \rfloor}^{(k)}$ modifies the pulse timing position, where $\lfloor x \rfloor$ gives the integer part of x .

For the ease of analysis in synchronization mechanism, it is assumed that communication is performed in a single-user and single-path environment and no data is transmitted during synchronization, the received pulse $r(t)$ can be simply expressed as

$$r(t) = \sum_{j=-\infty}^{\infty} A\omega_{rec}(t - jT_f - \tau_d) \quad (6.4)$$

where $\omega_{rec}(t)$ is the received pulse waveform and τ_d accounts for the delay between the transmitter and receiver involved. If effects of the low-noise amplifier (LNA) on the received pulse are neglected, the signals appearing at the inputs of mixers 1 and 2 are the same as $r(t)$.

The synchronization can be achieved in two steps, namely phase and frequency synchronizations. The phase synchronization is a pulse-searching process, as shown

by the dashed-line box in Figure 6.5. In order to detect the approximate location of the received pulse $\omega_{rec}(t)$ in the receiver signal $r(t)$ amplified by LNA, the local template signal $v(t)$, from the pulse generator (PG), is correlated with received signal $r(t)$ first. The template signal $v(t)$ can be expressed as

$$v(t) = \sum_{j=-\infty}^{\infty} \omega_{cor}(t - jT_f - \tau_r) \quad (6.5)$$

where $\omega_{cor}(t)$ is the energy-normalized template pulse waveform and τ_r the receiver time reference. τ_r is contributed by τ_0 , the time reference of the receiver voltage-controlled oscillator (VCO), and τ_j , the delay selected by the multiplexer (MUX) for the j th pulse. The difference $\Delta\tau_{async}$ between τ_d and τ_r is to account for the asynchronism between the transmitter and receiver under investigation. By neglecting effects of antennas and the communication channel in the first-round analysis, the received pulse waveform $\omega_{rec}(t)$ is the same as the template pulse $\omega_{cor}(t)$, Gaussian n th derivative Gn in the presented synchronization scheme. The output of the correlator 1 for the phase synchronization is then sampled as $x_1(t)$ at a proper time t_1 and compared with the threshold V_{th} which is determined by $R_{nn,th}$ of the Gn pulse adopted. Finally the decision $y_1(t)$ of the comparator is fed into a multiplexer, which outputs a delayed version of the pulse if no pulse has been detected in the received j th pulse yet. The process keeps going on until V_{th} has been exceeded, i.e., the phase synchronization has been achieved. More specifically, the process can be described by

$$\tau_{j+1} = \begin{cases} \tau_j + \Delta\tau, & \text{if } x_1(t) < V_{th} \\ \tau_j, & \text{if } x_1(t) \geq V_{th} \end{cases} \quad (6.6)$$

where $\Delta\tau$ is the unity delay of the delay system, i.e., step size of the sliding correlator aforementioned. With N_d defined as the ratio of T_f and $\Delta\tau$, the MUX increases τ_j from zero to $(N_d - 1)\Delta\tau$, and restarts the process if no pulse has not been detected after one-round search. As described in [107], the step size in the delay system of the sliding correlator is limited by the pulse width, 2 ns particularly for the G5 pulse presented. However, with the discussion aforementioned, we find out that the maximum value of $\Delta\tau$ should be constrained by τ_e of $R_{55}(\tau)$ for the adopted G5 pulse, i.e., 200 ps.

It can be observed that the phase synchronization by means of the sliding correlator merely finds the approximate location of the received pulse. Taking G5 pulse as an example, phase synchronization may fail to achieve the highest auto-correlation value, given that $\Delta\tau_{sync}$ is a random value. More specifically, with the maximum possible output of correlator 1 normalized to unity, phase synchronization is achieved as long as $x_1(t)$ is greater than $R_{55,th}$, 0.4068. On the other hand, decision making for the received signal prefers a higher signal-to-noise ratio (SNR), i.e., at a higher correlation value. Therefore, by only phase synchronization, the phase alignment between the transmitter and the receiver involved cannot be achieved completely, which necessitates a fine synchronization.

Block diagram for the fine synchronization tuning is shown in the dotted box at the

bottom of Figure 6.5. The fine synchronization, namely the frequency synchronization process, only starts to function after phase synchronization has been achieved. $v'(t)$ is obtained by taking derivative on the output of PG once, resulting in a $G(n+1)$ pulse when a G_n pulse is used for the phase synchronization. An S/H block is added as compared with the work in [107]. An intermediate result of the integrator may be misleading and feeds back wrong information to input of the VCO. As a result, output of correlator 2 is only valid at the end of the locally generated pulse, leading to the S/H circuit. The sampled output of correlator 2, $x_2(t)$, is fed into a low-pass filter (LPF) to remove high frequency components, and eventually $y_2(t)$ is passed to the input of VCO. Essentially the fine pulse-position adjustment is performed by varying VCO output frequency. This is equivalent to a PLL. Generally, the transient response of a PLL cannot be analyzed linearly whereas the whole system is typically investigated in the frequency domain [108, 109, 110]. Conceptually, correlator 2 compares ϕ_r and $\phi_{v'}$, the phases of $r(t)$ and $v'(t)$, and gives an output proportional to the phase difference, performing the function of a phase detector (PD). If $v'(t)$ leads $r(t)$ by certain amount of time after phase synchronization has been achieved, $x_2(t)$ of the PD, namely correlator 2, is negative, according to $R_{56}(\tau)$ shown in Figure 6.3. The negative value changes the output of VCO to a lower frequency, i.e., a longer period, making the local template less leading and eventually aligned with the received pulse. A similar analysis can be performed if $v'(t)$ is lagging relative to $r(t)$. The VCO output frequency keeps unchanged only when perfect synchronization is achieved.

From the block analysis, it can be concluded that there are two feedback loops, i.e.,

phase and frequency synchronizations for the approximate pulse-position searching and the fine pulse position adjustment, respectively. When the frequency synchronization feedback loop is compared with the DLL-based synchronization scheme [105, 106], $R_{n,n+1}(\tau)$ is equivalent to the non-flat discriminator characteristics. However, the presented synchronization scheme allows a larger delay step size $\Delta\tau$ 200 ps while the step size is half of the mainlobe width [105] as 137 ps or 30% of the mainlobe width [106] as 82 ps for the DLL-based synchronization method. On the other hand, four branches of correlators are required in [106], which incurs a higher cost in hardware implementation. Further more, the method based on DLL is only valid for pulses with even symmetry, more specifically, even orders of Gaussian pulses, whereas the discussed synchronization scheme applies to all orders of Gaussian pulses. Finally, due to the use of VCO, a frequency offset between the involved transmitter and receiver can be eliminated in a locked condition [108, 109, 110].

One important point for the presented synchronization scheme is that within the range of $\Delta\tau$, $R_{n,n+1}(\tau)$ must be monotonic; otherwise the VCO frequency may change oppositely to the undesired direction [110]. For the Gaussian pulse order n as 1 or 2, τ_m in $R_{n,n+1}(\tau)$ is smaller than τ_e of $R_{nn}(\tau)$. Therefore, for the two pulses, the step size $\Delta\tau$ should be constrained by τ_m rather than τ_e .

As mentioned above, the fine synchronization has an analogy with a PLL. Nevertheless, there are some aspects different from a conventional PLL. Taking G5 as an example, first, the slope S of $R_{56}(\tau)$ in the monotonic region is not a constant. In-

Figure 6.6: Sampling time for the S/H block in frequency synchronization (not drawn to ratio).

stead, it varies from 4.1146×10^9 to 1.2525×10^{10} V/s for the normalized $R_{56}(\tau)$ within the range of τ_e . Moreover, K_{PD} , the gain of the PD in rad/V for the presented PLL, is related to S by $K_{PD} = ST_f/2\pi$. Third, conventional PD has a much wider monotonic range, e.g., 0 to π for exclusive OR (XOR) PD and 0 to 2π for PD based on S-R latch [110]. In IR-UWB applications, a very low duty cycle is typically used. The monotonic region τ_m in radians for the correlator-based PD is $-\tau_m\pi/T_f$ to $\tau_m\pi/T_f$, namely $-0.0255 \times 10^{-3}\pi$ to $0.0255 \times 10^{-3}\pi$ rad for a nominal period T_f as 10 ns. Therefore the phase synchronization has to be re-activated once the threshold V_{th} is not satisfied in fine synchronization due to system jitters or improper parameter settings. Fourth, sampling instance is important since an S/H block is used in the synchronization loop for frequency synchronization. Due to the low duty cycle of IR-UWB characteristics, the pulse width is a small portion of one clock frame. As shown in Figure 6.6, the output of mixer 2 is zeros after t_2 , the end of the locally generated pulse, when the template $v'(t)$ leads, aligns with and lags the received pulse $r(t)$ for pulses $j-1$, j , and $j+1$ respectively. Therefore the integrator output needs to be sampled at t_2 within the clock frame under consideration to reduce effects of noise

Figure 6.7: Effect of sampling time on synchronization performance during locking. Thick line: sampling at t_2 ; thin line: sampling at $t_2 + 2T_c$.

on sampled value. Meanwhile, sampling at t_2 gives the locking loop a longer time to response, therefore leading to a better synchronization performance.

Figure 6.7 depicts the simulation of sampling time effects on synchronization performance. In the simulation, the normalized value of $x_1(t)$ at unity indicates perfect synchronization and the clock frame time is 10 ns. When correlator 2 output is sampled t_2 , ripples in the normalized correlation is less pronounced than that with correlator 2 output sampled at $t_2 + 2T_c$. With 88% of maximum normalized $x_1(t)$ as a criterion, sampling of integrator output at t_2 achieves synchronization within 15 clock cycles whereas sampling at $t_2 + 2T_c$ needs 17 clock cycles more to complete synchronization using the same criterion.

In the simulation, a first-order simple RC LPF is used for simulation. To achieve a better performance, an LPF with a feed-forward zero or at a higher order can be

used to improve performance at the cost of more sophisticated system parameter tuning [110]. One can design the system carefully with well-documented techniques and guidelines [108, 109, 110].

6.2.3 Tradeoffs of Gaussian Pulse Order

There are some factors to be taken into account when one is selecting the order of Gaussian pulses. As mentioned above, for the n th Gaussian pulse, sidelobes in $R_{nn}(\tau)$ get more and higher and therefore a higher discriminating threshold V_{th} set by $R_{nn,th}$ when n increases. On the other hand, the mainlobe of $R_{nn}(\tau)$ becomes narrower over the increase of n . As a result, the step size $\Delta\tau$ for the phase synchronization becomes smaller for higher order of Gaussian pulses. A smaller step size $\Delta\tau$ for the sliding correlator implies that hardware realization gets more difficult, especially in designing accurate delay lines.

In contrast, synchronization using a low order of Gaussian pulse suffers less from the problems as synchronization with a high-order pulse does. Furthermore, low orders of Gaussian pulses benefit from the ease of realization of the pulse in IC implementation due to fewer times of derivative operations required. A second order of Gaussian pulse has been used for UWB communication in [18], where the circuit implementation is relatively simple. However, for a high order of Gaussian pulse, it requires more times of derivatives, leading to more complicated IC implementation. A simulation of G5 pulse is provided in [111] and circuit implementation is performed in [113], where

the generated pulse consists of single shapes at difference phases. An underlying problem for the implementation in [111, 113] is that when the pulse width shrinks to sub-nanosecond range, slight process or temperature variations could alter the generated pulse significantly, leading to failures in the pulse generation. Therefore, robustness is an important issue for a high-order Gaussian pulse implemented using the digital approach as in [111, 113].

However, when the FCC regulations are taken into account, a high-order pulse is superior to its low-order counterpart. With an increase in n or shrinkage in T_c , the center frequency of the Gaussian pulse PSD shifts to a higher frequency [114]. The G5 pulse is a single pulse complying with the FCC regulation mask without filtering [111]. In contrast, popular choices of Gaussian first and second derivatives in impulse radio must be filtered out to comply with the FCC regulations. Apart from effects of antennas and communication channels, the required filter introduces an additional distortion to received pulse at the receiver. Subsequently, the distortion on the received pulse gives rise to non-idealities in the auto- and cross- correlations, and therefore has impairments on the synchronization performance and decision-making for the received signal. As a result, when selecting the Gaussian pulse order n for a UWB communication system, one has to take into account both ease of implementation and superiority in performance.

It is worthwhile mentioning that the proposed synchronization is suitable for BPSK modulation scheme as well. In the synchronization, the coarse and fine pulse adjust-

ments are involved, so it is more like a PPM scheme. In a BPSK modulation system, one can set all the transmitted bits to ‘1’s during the synchronization.

6.3 Effects of Antennas and Channels

Communication channels and antennas of a UWB link behave as filters on the propagation of UWB signals. A method to calculate effects of antennas and freespace channel on a received pulse will be introduced first. However, as the antenna response used for calculation has an impedance bandwidth spreading from 3.1 to 10.6 GHz [18] and UWB radio channels are typically modeled for the 3.1 to 10.6 GHz band [80, 115, 116], the shaping factor is chosen with $\sigma = 51\text{ps}$ such that the -10 dB bandwidth of the pulse is within 3.1 to 10.6 GHz. Distortions on the received pulse will be evaluated for the synchronization scheme presented. Finally, simulations are performed to check the effects of different practical UWB multipath channels on the presented synchronization method.

6.3.1 Calculation of the Received Pulse with Antennas and Freespace Channel

As the generated pulse is transmitted through a transmitting antenna, a specific communication channel, and a receiving antenna, distortions are introduced to the received pulse. Therefore, it is important to evaluate the distortion and its effects on the pre-

sented synchronization technique.

Planar monopole UWB antennas are popular choices for UWB communications due to their attractive electrical, mechanical and economical merits [117, 118]. Normalized transfer functions, $H_{N,Tx}(f)$ and $H_{N,Rx}(f)$, of planar monopole UWB transmitting and receiving antennas [18] can be obtained, respectively [70]. The frequency domain expression, $\omega_{tr}(f)$, of a generated single temporal Gaussian pulse $\omega_{tr}(t)$ is obtained using Fourier transform (FT) and the corresponding received signal frequency-domain expression $\omega_{rec}(f)$ is related to $\omega_{tr}(f)$ by $\omega_{rec}(f) = \omega_{tr}(f)S_{21}(f)$. From [70], $S_{21}(f)$ can be expressed as

$$S_{21}(f) = \frac{j\lambda}{4\pi d} H_{N,Tx}(f) H_{N,Rx}(f) \exp(-j2\pi f \frac{d}{c}) \quad (6.7)$$

where λ , d , and c are the wavelength, transmitter-receiver distance and light speed in freespace, respectively.

The temporal waveform $\omega_{rec}(t)$ at receiver can be obtained using the inverse Fourier transform (IFT). Freespace transmission is considered in (6.7). Taking G5 pulse as the transmitted signal, the transmitted and received temporal pulses with unity peaks are shown in Figure 6.8. The transmitter-receiver separation is assumed as 20 cm for the ease of observation. Attenuation effects have been removed by normalizing the absolute peak to unity. It can be observed that the distortion, introduced by antennas and the freespace channel, creates stronger sidelobes and alters the temporal waveform

Figure 6.8: The transmitted and received temporal G5 pulse with effects of antennas and the freespace channel. Solid curve: the transmitted pulse; dashed curve: the received pulse.

somehow between G5 and G6 pulses. To check the distortion on received pulse, the fidelity factor [70] between the transmitted and received pulses, $\omega_{tr}(t)$ and $\omega_{rec}(t)$, is calculated using (3.3) and obtained as 84.64%.

6.3.2 Impairments of Antennas and the Freespace Channel on a Received Pulse

Correlation $R'_{55}(\tau)$ between $\omega_{tr}(t)$ and $\omega_{rec}(t)$ has been calculated. Due to distortions in the mainlobe and stronger sidelobes of $\omega_{rec}(t)$, $R'_{55}(\tau)$ has been distorted as well. The highest sidelobe $R'_{55,th}$ increases from 0.4068 in ideal case to 0.6309 due to distortions in $\omega_{rec}(t)$, leading to a smaller effective mainlobe width τ'_e from -22.55 ps to $+21.115$ ps rather than ± 25.33 ps in ideal case. Therefore, the maximum sliding

correlator step size $\Delta\tau$ for phase synchronization becomes 43.665 ps, which is smaller as compared with 50.66 ps for an ideal G5 pulse.

Besides $R'_{55}(\tau)$ for the phase synchronization, during frequency synchronization, correlation $R'_{56}(\tau)$ between the local template G6 pulse and $\omega_{rec}(t)$ is important for the fine pulse-position tuning. It has been found that the slope S of $R'_{56}(\tau)$, proportional to the gain of the PD, is slightly less than that of $R_{56}(\tau)$ for the ideal case. Therefore one has to take the change of S into account when setting parameters in circuit design. More importantly, $R'_{56}(\tau)$ is located at a positive value, i.e., non-zero, when the involved transmitter and receiver are synchronized. A zero correlation is obtained when the local G6 pulse leads $\omega_{rec}(t)$ by certain amount of time. In other words, when the output of the correlator 2 is zero, the actual relative position is that the local G6 pulse leads $\omega_{rec}(t)$ by certain amount of time. Therefore, some sort of level shifting in circuit implementation is necessary to restore the correlation to zero at perfect synchronization.

6.3.3 Effects of UWB Multipath Channels

Freespace transmission is assumed in the above-mentioned discussion for effects on received pulse. Multipath is not present due to the ideality of freespace channel. In reality, multipath will affect the received signal. Practical multipath UWB channel can be simulated based on IEEE 802.15.SG3a channel model [115]. By selecting proper values for the arrival rates, decay rates, and standard deviations for different scenarios,

Figure 6.9: Transmitted and received G5 pulse with effects of antennas and IEEE UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 40 ns.

a multipath UWB channel can be obtained.

By replacing the term $\exp(-j2\pi fd/c)/d$ in (6.7) with the channel frequency domain transfer function, the received signal with effects of antennas and the UWB multipath channel can be obtained [119]. For the scenario with the line of sight (LOS) and range 0 to 4 meters (case A), Figure 6.9 depicts the transmitted and received G5 pulses. Both the transmitted and received pulses are normalized with unity absolute peaks and aligned in timing by removing the relative delay. It can be observed that for a single ray, the local template, namely the ideal G5 pulse, matches the received pulse with distortion reasonably well. Taking the received pulse due to the first ray as an example, the correlation between the received pulse and ideal G5 has the highest normalized sidelobe level $R_{55,th}$ at 0.6135, and a phase synchronization step size $\Delta\tau$

as 39.553 ps. The slight deviation of correlation properties is due to the partial overlapping of adjacent received pulses. Due to the presence of multipath, energy combining can be performed.

Another application for UWB as lifestyle and medical applications is the wireless connectivity in a body-area network (BAN), which has a shorter coverage than the IEEE 802.15.SG3a channel [116]. Radiographs of path loss and delay spread are provided in [116]. During measurements, the transmitting antenna was placed on the right upper arm and the receiving antenna on testing points of a cylindrical distribution. For a LOS channel measured in a staff lounge, the transmitted and received G5 pulses are depicted in Figure 6.10, including the effects of UWB antennas. The obtained highest sidelobe level $R_{55,th}$ is 0.708 and maximum sliding correlator step size $\Delta\tau$ as 38.33 ps, raising difficulties in design for accurate delay elements.

As a viable candidate for short-range high-rate communications, UWB has been applied for intra/inter-chip communications, where the transmitter-receiver separation is only up to a few tens of centimeters [18, 20]. Radio propagation channel for inter-chip wireless communications has been modeled based on measurements performed in computer enclosures [80], as presented in Chapter 3. To check the performance of the presented synchronization scheme for inter-chip wireless communications, a simulation for non-LOS (NLOS) scenario has been performed as depicted in Figure 6.11. Compared to the IEEE 802.15.SG3a UWB channel, denser multipaths but a shorter delay spread has been observed due to the contained environment for inter-chip ap-

Figure 6.10: Transmitted and received G5 pulse with effects of antennas and BAN UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 20 ns.

plications. When the G5 pulse is used for the presented synchronization scheme, the discrimination threshold $R_{55,th}$ obtained as 0.5518, and a sliding correlator step size $\Delta\tau$ as 46.838 ps, resulting in a less stringent requirement in hardware implementation than those for the IEEE 802.15.SG3a or the aforementioned BAN channels.

From simulations over different multipath channels, it can be observed that different effects have been introduced on the presented synchronization scheme. Therefore, for an optimized synchronization performance, one has to taken into account the effects of antennas and the specific communication channel.

Figure 6.11: Transmitted and received G5 pulse with effects of antennas and inter-chip UWB channel. Black thick curve: transmitted signal; Gray thin curve, received signal. Insert: time span 0 to 40 ns.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

Wireless inter-chip interconnect has been studied in this thesis, including channel characterization for wireless inter-chip channel, wave propagation mechanism for intra-chip channel, bit-error rate (BER) analysis for inter-chip channel, and synchronization scheme design for impulse-based ultrawide band (UWB) communications.

Chapter 2 presented a literature survey on the current research status of wireless interconnect for both intra- and inter- chip applications. Microstrip transmission line (MTL)-based radio frequency (RF) interconnect is discussed first, which is an “active” wire interconnect. Capacitive coupling and modern modulation schemes are adopted to achieve a high data rate. Second, characteristics of integrated on-chip antennas are described mainly based on the transmission gain. Effects of substrate, metal in-

interference structures, antenna size and orientation, crosstalk, wave propagation layer, and transient characteristics have been investigated. Third, discussions about intra- and inter-chip clock distribution are offered, including the feasibility study, noise coupling, system jitter etc. Fourth, data communications for intra- and inter-chip applications are presented, including a BER analysis for wireless intra-chip interconnect with binary phase-shift keying (BPSK) modulation scheme and a wireless inter-chip interconnect demonstration with UWB as its physical layer.

Chapter 3 characterized wireless inter-chip channel. Data were sampled in a computer casing on a laboratory workbench. The data sampling is performed in frequency domain over 3.1 to 10.6 GHz. Measurements cover the transmitter-receiver (T-R) separations from 62 mm to 252 mm including both line-of-sight (LOS) and non-LOS (NLOS) scenarios. Time-domain data are obtained using the inverse discrete Fourier transform (IDFT). A novel technique to double time-domain resolution is proposed when converting data from frequency domain to time domain. Data analysis shows that, in large-scale analysis, the path loss factor is less than two when the computer casing is closed and greater than two with the casing open. In small-scale analysis, Lognormal distribution is found as the best-fitted one. With both large- and small-scale data, channel model is implemented and simulated. Comparison between the simulated and measured data shows that the implemented model is very close to the measured one. In order to ensure the data sampling is performed in a typical environment for wireless inter-chip interconnect, measurements are selectively carried out in another computer casing with a similar but different internal configuration. Measured

data show that sampled channel parameters are consistent in different environment, making the modeling work a typical one for wireless inter-chip communications.

In Chapter 4, propagation mechanism of radio wave over intra-chip channel has been studied. Intra-chip channel is sampled in frequency domain over 10-110 GHz for integrated antennas on both high- and low-resistivity substrates. Time-domain data are obtained using IDFT with an improved time-domain resolution, similar as the work for inter-chip channel. It is found that for low-resistivity substrates, the received channel impulse response (CIR) is not strong as compared with the average noise floor. Therefore, intra-chip channel study is performed for high-resistivity substrates. In path loss analysis, it is found that path loss factor is constantly less than two for zigzag, meander and linear antennas. Furthermore, the first arrival in CIR is significantly later than that by free-space propagation. The linear relationship between the first arrival and T-R distance excludes the possibility that the first arrival is received through a reflected wave. As a result, it is concluded that surface wave is the dominant path of the received signal in intra-chip communications. It is also found that metal interference structures, either placed parallel or normal to the wave propagation direction, improve the transmission gain. For metal lines in parallel placement, path loss decreases with metal line density while it is the opposite case for normally placed metal lines. Delay spread increases with the T-R distance. Furthermore, metal interference structures, either in parallel or normal placement, help reduce delay spread for both zigzag and linear antennas.

BER analysis of UWB radio using BPSK modulation scheme over wireless inter-

chip channels were provided in Chapter 5 for inter-chip radio channels. A novel technique to reduce the inter-symbol interference (ISI) effect is proposed by dynamically shifting the integral window position at a receiver. Analytical BER expressions are derived and verified using Monte Carlo simulations. It is found that data communication with $\text{BER} < 10^{-6}$ is feasible for a data rate up to 650 Mbps with a T-R separation up to 252 mm. By considering thermal and switching noise as the dominant noise sources, a link margin of 28.22 dB can be obtained with a data rate as 650 Mbps at the largest T-R distance as 252 mm.

Chapter 6 presented a synchronization scheme for impulse-based UWB. Correlation properties of Gaussian pulses are explored as rationales of the synchronization scheme. Increasing Gaussian pulse order or reducing the pulse width shifts the spectrum center to a higher frequency and therefore fits the Federal Communications Commission (FCC) regulations better. On the hand, the synchronization scheme with a higher order of Gaussian pulse or narrower pulse width requires a smaller step size in the sliding correlator and gives a narrower monotonic region in the cross-correlation, resulting in tougher issues in hardware implementation. Synchronization can be achieved by using two feedback loops: a sliding correlator and a phase-locked loop (PLL)-like frequency synchronization loop. Analogy of the frequency synchronization loop to a PLL is discussed. It is found that within 15 clock cycles, synchronization can be achieved with 88% of the sliding correlator ideal output as a criterion. Effects of antennas and channels on the synchronization are discussed. It is observed that distortions introduced by antennas and channels place more stringent requirements on the

hardware implementation of the synchronization scheme.

7.2 Recommendations

In this thesis, a study of wireless inter-chip interconnect has been presented, including wireless inter-chip channel characterization, intra-chip wave propagation mechanism investigation, BER analysis of wireless inter-chip channel, and synchronization scheme design for impulse-based UWB. However, some important issues still have to be solved before wireless inter-chip interconnect comes to reality.

The wave propagation mechanism for integrated antennas in the intra-chip wireless interconnect has been studied in Chapter 4. Simulation could be performed to verify the propagation mechanism of integrated antennas. This work can be extended into the scenario for inter-chip communications among different chips within a multi-chip module (MCM), as shown in Figure 1.2(b). Based on this, the system study for communications within a MCM can be performed as well.

In the BER analysis for wireless inter-chip channel, an assumption of single user is made. However, in the real situation, multiple access is inevitably necessary. The multi-user interference introduces a new source of noise at the receiver. Therefore, communications with multiple access need to be considered. Another point is package-error rate would be more reasonable than bit-error rate in practical communications. The BER performance could be verified with respect to the simulation results, by using

a specially designed transceiver which incorporates the ISI-reduction technique.

In the synchronization scheme design, we assumed a relatively ideal scenario, i.e., no multipath present, no time hopping (TH), direct sequence (DS), or data transmission during synchronization. Even so, the synchronization scheme is based on pulse synchronization, rather than symbol synchronization. In practical communications, either in the IEEE UWB channel or the wireless inter-chip UWB channel, multipaths are always present. As a result, at the receiver certain RAKE power combining scheme has to be used to capture more energy of the received signal. A more complicated system architecture may be required in order to realize synchronization of wireless inter-chip interconnect in a practical scenario.

Author's Publications

International Journal Papers

- [1] **Z. M. Chen**, and Y. P. Zhang, “Inter-chip wireless communication channel: measurement, characterization, and modeling,” *IEEE Transactions on Antennas and Propagation*, vol. 55, no. 3, pp. 978–986, Mar. 2007.
- [2] Y. P. Zhang, **Z. M. Chen**, and M. Sun “Propagation mechanisms of radio waves over intra-chip channels with integrated antennas: frequency-domain measurement and time-domain analysis,” *IEEE Transactions on Antennas and Propagation*, vol. 55, no. 10, pp. 2900–2906, Oct. 2007.
- [3] **Z. M. Chen**, Y. P. Zhang, A. Q. Hu, and T. S. Ng, “Bit-error-rate analysis of UWB radio using BPSK modulation over inter-chip radio channels for wireless chip area networks,” Accepted with minor revision and revised for *IEEE Transactions on Wireless Communications*.
- [4] **Z. M. Chen**, and Y. P. Zhang, “Effects of antennas and channels on the perfor-

mance of synchronization in pulse-based UWB radios,” to be submitted to *IEEE Transactions on Antennas and Propagations*.

Conference papers

- [1] Y. P. Zhang, **Z. M. Chen**, M. Sun, and J. He, “Wireless chip area network (WCAN): A new paradigm for RF microelectronics and radio communications,” *Invited Address at IEEE Workshop on Electrical Design of Advanced Packaging and Systems*, 16–18 Dec 2006, Shanghai, China.

- [2] **Z. M. Chen**, and Y. P. Zhang, “A modified synchronization scheme for impulse-based UWB,” presented at *International Conference on Information Communications and Signal Processing*, 10–13 Dec. 2007, Singapore.

Bibliography

- [1] “International technology roadmap for semiconductors,” 2007 update.
- [2] J. A. Davis *et al.*, “Interconnect limits on gigascale integration(GSI) in the 21st century,” *Proc. IEEE*, vol. 89, no. 3, pp. 305–324, 2001.
- [3] J.-P. Schoellkopf, “Impact of interconnect performances on circuit design,” in *Proc. Int. Interconnect Technol. Conf.*, 1998, pp. 53–55.
- [4] J. D. Meindl *et al.*, “Interconnect opportunities for gigascale integration,” *IBM J. Res. & Dev.*, vol. 46, no. 2/3, pp. 245–263, 2002.
- [5] R. H. Havemann and J. A. Hutchby, “High-performance interconnects: an integration overview,” *Proc. IEEE*, vol. 89, no. 5, pp. 586–601, 2001.
- [6] “International technology roadmap for semiconductors,” 1999.
- [7] M. C. F. Chang, V. P. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, “RF/Wireless interconnect for inter-and intra-chip communications,” *Proc. IEEE*, vol. 89, no. 4, pp. 456–466, 2001.

- [8] M. Lee, A. Hill, and M. H. Darley, "Interconnect inductance effects on delay and crosstalk for longon-chip nets with fast input slew rates," in *ISCAS'98 Proc. 1998 IEEE Int. Symp. Circuits Syst.*, vol. 2, 1998.
- [9] D. A. B. Miller and H. M. Ozaktas, "Limit to the bit-rate capacity of electrical interconnects from the aspect ratio of the system architecture," *J. Parallel Distrib. Comput.*, vol. 41, pp. 42–52, 1997.
- [10] A. Rashid, S. Watanabe, and T. Kikkawa, "Characteristics of integrated antenna on Si for on-chip wireless interconnect," *Jap. J. Appl. Phys.*, vol. 42, pp. 2204–2209, 2003.
- [11] D. Mizoguchi, Y. B. Yusof, N. Miura, T. Sakura, and T. Kuroda, "A 1.2 Gb/s/pin wireless superconnect based on inductive inter-chip signaling (IIS)," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, pp. 142–143.
- [12] R. J. Drost, R. D. Hopkins, R. Ho, and I. E. Sutherland, "Proximity communication," *IEEE J. Solid State Circuits*, vol. 39, no. 9, pp. 1529–1535, 2004.
- [13] R. Reif, A. Fan, K. N. Chen, and S. Das, "Fabrication technologies for three-dimensional integrated circuits," in *Proc. Int. Symp. Quality Electronic Design (ISQD)*, San Jose, CA, 2002, pp. 33–37.
- [14] R. Zhang, K. Roy, C. K. Koh, and D. B. Janes, "Power trends and performance characterization of 3-dimensional integration," in *IEEE Int. Symp. Circuits Syst.*, vol. 4, 2001, pp. 6–9.

- [15] “Germanium-on-insulator detectors could crack interconnect bottleneck,” *optics.org*, 2004.
- [16] Y. P. Zhang, “Bit-error-rate performance of intra-chip wireless interconnect systems,” *IEEE Commun. Lett.*, vol. 8, no. 1, pp. 39–41, 2004.
- [17] B. A. Floyd, C. M. Hung, and K. K. O, “Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers, and transmitters,” *IEEE J. Solid State Circuits*, vol. 37, no. 5, pp. 543–552, 2002.
- [18] Y. J. Zheng, Y. P. Zhang, and Y. Tong, “A novel wireless interconnect technology using impulse radio for interchip communications,” *IEEE Trans. Microw. Theory Techniques*, vol. 54, no. 4 Part 2, pp. 1912–1920, 2006.
- [19] K. K. O *et al.*, “On-chip antennas in silicon integrated circuits and their applications,” *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1312–1323, 2005.
- [20] M. Sun and Y. P. Zhang, “Performance of inter-chip RF-interconnect using CPW, capacitive coupler, and UWB transceiver,” *IEEE Trans. Microw. Theory Techniques*, vol. 53, no. 9, pp. 2650–2655, 2005.
- [21] K. Kimoto and T. Kikkawa, “Transmission characteristics of Gaussian monocycle pulses for inter-chip wireless interconnections using integrated antennas,” *Jap. J. Appl. Phys.*, vol. 44, no. 4B, pp. 2761–2765, 2005.

- [22] K. Kim and K. Kenneth, "Characteristics of integrated dipole antennas on bulk, SOI, and SOS substrates for wireless communication," in *IITC*. IEEE, 1998, pp. 21–23.
- [23] Y. P. Zhang, L. H. Guo, and M. Sun, "High transmission gain inverted-F antenna on low-resistivity Si for wireless interconnect," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 374–376, 2006.
- [24] Y. P. Zhang, M. Sun, and W. Fan, "Performance of integrated antennas on silicon substrates of high and low resistivities up to 110 GHz for wireless interconnects," *Wiley Inter-Science Microw. Opt. Technol. Lett.*, vol. 48, no. 2, p. 302, 2006.
- [25] Y. P. Zhang, "Antenna-in-package technology for modern radio systems," *IEEE Int. Workshop Antenna Technol. Small Antennas Novel Metamaterials*, pp. 37–40, 2006.
- [26] —, "Wireless chip area network: A new paradigm for antennas, RF (MM) ICs, and communications," in *Asia-pacific Microw. Conf.*, India, 2004.
- [27] P. K. Saha, N. Sasaki, and T. Kikkawa, "A CMOS UWB transmitter for intra/inter-chip wireless communication," *2004 IEEE Eighth Int. Symp. Spread Spectrum Techn. Applicat.*, pp. 962–966, 2004.

- [28] N. Sasaki, P. K. Saha, and T. Kikkawa, "A single chip UWB receiver based on 0.18- μm CMOS technology for wireless interconnection," in *Second Hiroshima Int. Workshop Nanoelectron. Tera-Bit Informat. Process.*, 2004, pp. 28–29.
- [29] K. Kim, "On-chip wireless interconnection with integrated antennas," in *IEDM Tech. Dig.*, 2000, pp. 485–488.
- [30] A. Rashid, S. Watanabe, and T. Kikkawa, "Characteristics of Si integrated antenna for inter-chip wireless interconnection," *Jap. J. Appl. Phys.*, vol. 43, no. 4b, pp. 2283–2287, 2004.
- [31] M. Sun and Y. P. Zhang, "100-GHz quasi-Yagi antenna in silicon technology," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 455–457, 2007.
- [32] S. Watanabe, A. Rashid, and T. Kikkawa, "Effect of high-resistivity Si substrate on antenna transmission gain for on-chip wireless interconnects," *Jap. J. Appl. Phys.*, vol. 43, no. 4b, pp. 2297–2301, 2004.
- [33] Y. P. Zhang, M. Sun, and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1664–1668, 2005.
- [34] H. Shin and M. F. Chang, "1.1 Gbit/s RF-interconnect based on 10 GHz RF-modulation in 0.18 μm CMOS," *Electronics Lett.*, vol. 38, no. 2, pp. 71–72, 2002.

- [35] H. Shin, Z. Xu, and M. F. Chang, "RF-interconnect for multi-Gb/s digital interface based on 10 GHz RF-modulation in 0.18 μm CMOS," in *IEEE MTT-S Int. Microwav. Symp. Digest*, vol. 1, 2002, pp. 477–480.
- [36] H. Shin, Z. Xu, K. Miyashiro, and M. F. Chang, "Estimation of signal-to-noise ratio improvement in RF-interconnect," *Electronics Lett.*, vol. 38, no. 25, pp. 1666–1667, 2002.
- [37] D. Arizono, A. Iwata, and M. Sasaki, "A wireless chip interconnect using resonant coupling between spiral inductors," *Technical report of IEICE. ICD*, vol. 105, no. 184, pp. 13–18, 2005.
- [38] Q. U. N. Gu, Z. Xu, J. Kim, J. Ko, and M. F. Chang, "Three-dimensional circuit integration based on self-synchronized RF-interconnect using capacitive coupling," in *2004 Symp. VLSI Technology and Circuits (VLSI)*, HI, 2004, pp. 96–97.
- [39] K. Kanda *et al.*, "1.27 Gb/s/pin 3mW/pin wireless superconnect (WSC) interface scheme," in *IEEE ISSCC Dig. Tech. Papers*, 2003, pp. 186–187.
- [40] S. Mick, J. Wilson, and P. Franzon, "4 Gbps high-density AC coupled interconnection," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 133–140.
- [41] N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Cross talk countermeasures in inductive inter-chip wireless superconnect," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2004, pp. 99–102.

- [42] T. Kikkawa, A. Rashid, and S. Watanabe, "Effect of silicon substrate on the transmission characteristics of integrated antenna," in *IEEE Topical Conf. Wireless Commun. Technol.* IEEE, 2003, pp. 144–145.
- [43] K. Kimoto, S. Watanabe, T. Kikkawa, P. S. Hall, and V. Yuan, "Characteristics of fractal dipole antennas integrated on Si for ULSI wireless interconnects," in *2004 IEEE AP-S Int. Symp. and USNC/URSI National Radio Science Meeting*, Monterey, CA, 2004, pp. 3437–3440.
- [44] A. Rashid, S. Watanabe, and T. Kikkawa, "High transmission gain integrated antenna on extremely high resistivity Si for ULSI wireless interconnect," *IEEE Electron Devices Lett.*, vol. 23, no. 12, pp. 731–733, 2002.
- [45] A. Rashid, S. Watanabe, T. Kikkawa, X. Guo, and K. K. O, "Interference suppression of wireless interconnection in Si integrated antenna," in *Int. Interconnect Conf.* IEEE, 2002, pp. 173–175.
- [46] X. Guo, R. Li, and K. K. O, "Design guidelines for reducing the impact of metal interference structures on the performance on-chip antennas," in *Proc. IEEE AP-S Int. Symp. USNC/URSI National Radio Science Meeting*, vol. 1, Columbus, OH, 2003, pp. 606–609.
- [47] A. Rashid, S. Watanabe, and T. Kikkawa, "Crosstalk isolation of monopole integrated antenna on Si for ULSI wireless interconnect," in *Proc. IEEE Interconnect Technol. Conf.*, 2003, pp. 156–158.

- [48] H. Yoon, K. Kim, and K. K. O, "Interference effects on integrated dipole antennas by a metal cover for an integrated circuit package," in *Proc. IEEE AP-S Int. Symp. USNC/URSI National Radio Science Meeting*, 2000, pp. 782–785.
- [49] X. Guo, J. Caserta, R. Li, B. Floyd, and K. K. O, "Propagation layers for intra-chip wireless interconnection compatible with packaging and heat removal," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, 2002, pp. 36–37.
- [50] K. Kim, W. Bomstad, and K. K. O, "A plane wave model approach to understanding propagation in an intrachip communication system," in *Proc. IEEE AP-S Int. Symp. USNC/URSI National Radio Science Meeting*, vol. 2. Boston, MA: IEEE, 2001, pp. 166–169.
- [51] R. Li, W. Bomstad, J. Caserta, X. Guo, and K. K. O, "Evaluation of integrated antennas for wireless connection between an integrated circuit and an off-chip antenna," in *Proc. 2003 Int. Interconnect Conf.*, San Francisco, CA, 2003, pp. 120–122.
- [52] J. J. Lin *et al.*, "Integrated antennas on silicon substrates for communication over free space," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 196–198, 2004.
- [53] R. Li and X. Guo, "A technique for incorporation of a heatsink for a system utilizing integrated circuits with wireless connections to an off-chip antenna," in *Proc. Int. Interconnect Technology Conf.* San Francisco, CA: IEEE, 2004, pp. 160–162.

- [54] J. J. Lin *et al.*, “ $10\times$ improvement of power transmission over free space using integrated antennas on silicon substrates,” in *2004 Custom Integrated Circuits Conf.*, Orlando, FL, 2004, pp. 697–700.
- [55] S. Watanabe, K. Kimoto, and T. Kikkawa, “Transient characteristics of integrated dipole antennas on silicon for ultra wideband wireless interconnects,” in *2004 IEEE AP-S Intl. Symp. and USNC/URSI National Radio Science Meeting*, vol. 3, Monterey, CA, 2004, pp. 2277 – 2280.
- [56] T. O. Dickson, D. Bravo, and K. K. O, “Noise coupling to on-chip integrated antennas,” in *2002 IEEE Int. Symp. EMC*, vol. 1, Minneapolis, MN, 2002, pp. 340–344.
- [57] J. Mehta, D. Bravo, and K. K. O, “Switching noise picked up by a planar dipole antenna mounted near integrated circuits,” *IEEE Trans. Electro-Magnetic Compatibility*, vol. 44, no. 2, pp. 282–290, 2002.
- [58] T. O. Dickson, B. Floyd, and K. K. O, “Jitter in a wireless clock distribution system,” in *Int. Interconnect Technology Conf.* IEEE, 2002, pp. 154–156.
- [59] J. Branch, X. Guo, L. Gao, A. Sugavanam, and J. J. Lin, “Wireless communication in a flip-chip package using integrated antennas on silicon substrates,” *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 115–117, 2005.
- [60] B. A. Floyd *et al.*, “Wireless interconnects for clock distribution,” in *TAU '02: Proceedings of the 8th ACM/IEEE international workshop on Timing issues in*

the specification and synthesis of digital systems. Monterey, California, USA: ACM, 2002, pp. 105–108.

[61] K. O *et al.*, “Wireless communication using integrated antennas,” in *Proc. Int. Interconnect Technol. Conf.*, San Francisco, CA, 2003, pp. 111–113.

[62] B. A. Floyd and K. K. O, “The projected power consumption of a wireless clock distribution system and comparison to conventional distribution systems,” in *IEEE Int. Interconnect Technology Conf.*, San Francisco, CA, 1999, pp. 248–251.

[63] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, “3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration,” *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, 2001.

[64] D. A. B. Miller, “Rationale and challenges for optical interconnects to electronic chips,” *Proc. IEEE*, vol. 88, no. 6, pp. 728–749, 2000.

[65] S. S. Ghassemzadeh, R. Jana, C. W. Rice, W. Turin, and V. Tarokh, “Measurement and modeling of an ultra-wide bandwidth indoor channel,” *IEEE Trans. Commun.*, vol. 52, no. 10, pp. 1786–1796, 2004.

[66] L. Rusch, C. Prettie, D. Cheung, Q. Li, and M. Ho, “Characterization of UWB propagation from 2 to 8 GHz in a residential environment,” 2003. [Online]. Available: www.intel.com

- [67] D. Cassioli, M. Z. Win, and A. F. Molisch, "The ultra-wide bandwidth indoor channel: From statistical model to simulations," *IEEE J. Select. Areas Commun.*, vol. 20, no. 6, pp. 1247–1257, 2002.
- [68] Z. Irahhaute, H. Nikookar, and G. J. M. Janssen, "An overview of ultra wide band indoor channel measurements and modeling," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 8, pp. 386–388, 2004.
- [69] A. M. Street, L. Lukama, and D. J. Edwards, "Use of VNA's for wideband propagation measurements," *Proc. Inst. Elect. Eng. Commun.*, vol. 148, no. 6, pp. 411–415, 2001.
- [70] T. G. Ma and S. K. Jeng, "Planar miniature tapered-slot-feed annular slot antennas for ultrawide-band radios," *IEEE Trans. Antennas Propagat.*, vol. 53, no. 3, pp. 1194–1202, 2005.
- [71] Y. P. Zhang and M. Sun, "Chip antennas for ultrawideband radios," *IEEE Trans. Antennas Propagat.*
- [72] M. Sun and Y. P. Zhang, "A chip antenna in LTCC for UWB radios," *IEEE Trans. Antennas Propagat.*, vol. 56, no. 4, pp. 1177–1180, 2008.
- [73] M. Z. Win, F. Ramirez-Mireles, R. A. Scholtz, and M. A. Barnes, "Ultra-wide bandwidth (UWB) signal propagation for outdoor wirelesscommunications," in *Proc. IEEE 47th Vehicular Technology Conf.*, vol. 1, 1997, pp. 251–255.

- [74] T. S. Rappaport, *Wireless communications: Principles and Practice*. Upper Saddle River, NJ: Prentice Hall PTR, 2002.
- [75] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. Hoboken, NJ: Wiley-Interscience, 2005.
- [76] J. Cheng and N. C. Beaulieu, "Maximum-likelihood based estimation of the Nakagami m parameter," *IEEE Commun. Lett.*, vol. 5, no. 3, pp. 101–103, 2001.
- [77] A. Abdi, C. Tepedelenlioglu, M. Kaveh, and G. Giannakis, "On the estimation of the K parameter for the Rice fading distribution," *IEEE Commun. Lett.*, vol. 5, no. 3, pp. 92–94, 2001.
- [78] "MATLAB 6.5 documentation."
- [79] Y. P. Zhang, Z. M. Chen, M. Sun, and J. He, "Wireless chip area networks: A new paradigm for RF microelectronics and radio communications," in *Workshop on Electrical Design of Advanced Packaging and Systems*. Shanghai: IEEE, 2006.
- [80] Z. M. Chen and Y. P. Zhang, "Inter-chip wireless communication channel: Measurement, characterization, and modeling," *IEEE Trans. Antennas Propagat.*, vol. 55, no. 3, Part 2, pp. 978–986, 2007.
- [81] K. T. Chan *et al.*, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 11, pp. 487–489, 2003.

- [82] N. Alexopoulos and I. Rana, "Mutual impedance computation between printed dipoles," *IEEE Trans. Antennas Propagat.*, vol. AP-29, pp. 106–111, 1981.
- [83] D. Pozar, "Considerations for millimeter wave printed antennas," *IEEE Trans. Antennas Propagat.*, vol. AP-33, no. 5, pp. 740–747, 1983.
- [84] "IEEE Standard 802.11g," Jun. 2003.
- [85] J. P. Van't Hof and D. D. Stancil, "Ultra-wideband high data rate short range wireless links," *IEEE Vehicul. Technol. Conf.*, vol. 1, pp. 85–89, 2002.
- [86] "In the matter of revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," pp. 02–48, Apr. 2002.
- [87] J. Y. Lee and R. A. Scholtz, "Ranging in a dense multipath environment using an UWB radio link," *IEEE J. Select. Areas Commun.*, vol. 20, no. 9, pp. 1677–1683, 2002.
- [88] M. Z. Win and R. A. Scholtz, "Ultra-wide bandwidth time-hopping spread-spectrum impulse radio for wireless multiple-access communications," *IEEE Trans. Commun.*, vol. 48, no. 4, pp. 679–691, 2000.
- [89] H. Eberle, "A radio network for monitoring and diagnosing computer systems," *IEEE Micro*, vol. 23, no. 1, pp. 60–65, 2003.
- [90] D. Gerakoulis and P. Salmi, "An interference suppressing OFDM system for ultra wide bandwidth radio channels," in *Proc. IEEE Ultra-Wideband Syst. Technol.*, Baltimore, MD, 2002, pp. 259–264.

- [91] R. van Nee and R. Prasad, *OFDM for Wireless Multimedia Communications*. Norwood, MA, USA: Artech House, Inc., 2000.
- [92] R. Chen Jr, P. L. Chiu, and H. L. Yang, "Design and performance analysis of DS-UWB rake receiver," in *IEEE Int. Symp. Circuits Sys.*, 2006, p. 4.
- [93] R. J. Chen and C. L. Tsai, "Design and performance analysis of the receivers for DS-UWB communication systems," in *IEEE Int. Conf. UWB*, Waltham, MA, 2006, pp. 651–656.
- [94] J. G. Proakis, *Digital communications*, 4th ed. New York: McGraw-Hill, 2000.
- [95] M. E. Sahin and H. Arslan, "Inter-symbol interference in high data rate UWB communications using energy detector receivers," in *IEEE Int. Conf. UWB*, 2005, pp. 176–179.
- [96] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18- μm CMOS selective receiver front-end for UWB applications," *IEEE J. Solid State Circuits*, vol. 41, no. 8, pp. 1764–1771, 2006.
- [97] M. Z. Win and R. A. Scholtz, "Impulse radio: how it works," *IEEE Commun. Lett.*, vol. 2, no. 2, pp. 36–38, 1998.
- [98] M. Z. Win, "Spectral density of random UWB signals," *IEEE Commun. Lett.*, vol. 6, no. 12, pp. 526–528, 2002.

- [99] R. J. M. Cramer, R. A. Scholtz, and M. Z. Win, "Evaluation of an ultra-wide-band propagation channel," *IEEE Trans. Antennas Propagat.*, vol. 50, no. 5, pp. 561–570, 2002.
- [100] T. Terada, S. Yoshizumi, M. Muqsith, Y. Sanada, and T. Kuroda, "A CMOS ultra-wideband impulse radio transceiver for 1-Mb/s data communications and ± 2.5 -cm range finding," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 891–898, 2006.
- [101] J. Chen and Z. Zhou, "The overview of synchronization in DS-UWB," in *IEEE Int. Symp. Commun. Informat. Tech.*, vol. 2, 2005, pp. 983–986.
- [102] H. Bing, X. Hou, X. Yang, T. Yang, and C. Li, "A "two-step" synchronous sliding method of sub-nanosecond pulses for ultra-wideband (UWB) radio," in *Proc. IEEE Int. Conf. Communications, Circuits and Systems and West Sino Expositions*, vol. 1, Chengdu, China, 2002, pp. 142–145.
- [103] N. Deparis *et al.*, "Transposition of a base band ultra wide band width impulse radio signal at 60 GHz for high data rates multiple access indoor communication systems," *Europ. Conf. Wireless Technol.*, pp. 253–256, 2004.
- [104] N. Deparis, A. Boe, C. Loyez, N. Rolland, and P. A. Rolland, "Receiver and synchronization for UWB impulse radio signals," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, 2006, p. 14141417.

- [105] S. Tachikawa and S. Sumi, "A novel delay locked loop for UWB-IR," in *Int. Workshop Joint UWBST & IWUWBS*, 2004, pp. 273–277.
- [106] W. Zhang, H. Shen, Z. Bai, and K. S. Kwak, "Design of delay-locked loop (DLL) with low jitter and high lose lock time in UWB-IR system," *APCC'06. Asia-Pacific Conf. Commun.*, pp. 1–5, 2006.
- [107] N. Sasaki, P. K. Saha, and T. Kikkawa, "The development of UWB Gaussian monocycle pulse synchronization circuit based on 0.18- μm CMOS technology," in *2005 Hiroshima Univ. COE Workshop*, 2005.
- [108] D. Abramovitch, "Phase-locked loops: a control centric tutorial," *Proc. American Control Conf.*, vol. 1, pp. 1–15, 2002.
- [109] F. M. Gardner, *Phaselock Techniques*, 3rd ed. New York: John Wiley & Sons, 2005.
- [110] B. Razavi, "Design of monolithic phase-locked loops and clock recovery circuit-sla tutorial," in *Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design*. Piscataway, NJ: IEEE Press, 1996.
- [111] H. Kim, D. Park, and Y. Joo, "All-digital low-power CMOS pulse generator for UWB system," *Electronics Lett.*, vol. 40, no. 24, pp. 1534–1535, 2004.
- [112] I. Guvenc and H. Arslan, "On the modulation options for UWB systems," in *Proc. IEEE MILCOM '03*, vol. 2, 2003, pp. 892–897.

- [113] H. Kim and Y. Joo, "Fifth-derivative Gaussian pulse generator for UWB system," in *IEEE RFIC Symp.*, 2005, pp. 671–674.
- [114] M. G. Di Benedetto and G. Giancola, *Understanding Ultra Wide Band Radio Fundamentals*. Upper Saddle River, NJ: Prentice Hall PTR, 2004.
- [115] J. Foerster, "Channel modeling sub-committee report (Final)[EB/OL]. Study Group IEEE 802.15. SG3a," 2002.
- [116] Y. P. Zhang and Q. Li, "Performance of UWB impulse radio with planar monopoles over on-human-body propagation channel for wireless body area networks," *IEEE Trans. Antennas Propagat.*, vol. 55, no. 10, pp. 2907–2914, 2007.
- [117] Y. Chen, G. Y. Li, and Y. P. Zhang, "An LTCC planar ultra-wideband antenna," *Microw. Opt. Technol. Lett.*, vol. 42, no. 3, pp. 220–222, 2004.
- [118] Y. Chen and Y. P. Zhang, "Integration of ultra-wideband slot antenna on LTCC substrate," *Electronics Lett.*, vol. 40, no. 11, pp. 645–646, 2004.
- [119] A. Sibille, "About the role of antennas in UWB impulse radio," in *9th Management Committee Meeting of COST Action 273*, vol. 273, Athens, OH, Greece, 2004, pp. 26–28.