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A Parallel Sliding-IF Receiver Front-End With Sub-2-dB Noise Figure for 5–6-GHz WLAN Carrier Aggregation

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Abstract—This article presents a parallel sliding-IF 5–6-GHz wireless local area network (WLAN) receiver front-end supporting two-band carrier aggregation (CA), which alleviates potential local oscillator (LO) pulling and crosstalk problems. The supported frequency spacing between any two different carriers ranges from tens to hundreds of MHz. First, a complementary current-reused single-ended LNA with very low noise figure (NF) is developed to guarantee a low noise performance. Second, an active balun-splitter establishes a bridge between the LNA and the following parallel fully differential down-conversion paths. Next, to optimize the performance of the passive double-conversion mixer, a detailed analysis has been conducted and shown that the time offset with specific values between the two LOs maximizes conversion gain and minimizes noise contribution, which enhances harmonic rejection simultaneously. Fabricated in 65-nm CMOS technology, this receiver front-end achieves an average 1.9-dB NF with a 39-dB gain at 5–6 GHz for single-carrier scenario, degraded by 0.4 dB with 35-dB gain for two-band CA scenario. It consumes 35 and 60 mA with 1.2-V supply for single carrier and two-band CA scenario, respectively. The total area is 0.56 mm².

Index Terms—802.11ac, 802.11ax, active balun, carrier aggregation (CA), CMOS LNA, image rejection, passive mixer, radio frequency, receiver, sliding-IF.

I. INTRODUCTION

SINCE its first release, Wi-Fi has become ubiquitous all around the world. Targeting faster speed, wider and denser coverage, Wi-Fi standards have never stopped evolving. The first 802.11 protocol is released in 1997, followed by 11b, 11a, 11g, 11n, and 11ac. As depicted in Fig. 1(a), it has two main frequency bands for all these Wi-Fi protocols: 2.4 and 5 GHz. Each new generation protocol delivers significantly higher

Fig. 1. (a) Evolution of IEEE 802.11 protocols. (b) 5-GHz 802.11ac channel allocation in North America.

peak data rate than its predecessor, which is accomplished with larger available channel bandwidth (BW) and more complicated modulation scheme. To fulfill the requirement of large-scale and high-density Wi-Fi deployment scenarios, 802.11ax, the successor to 802.11ac, is designed as the current Wi-Fi generation. Fig. 1(b) introduces the 802.11ac/ax channelization in North America from 5.17 to 5.835 GHz. It consists of three discontinuous frequency bands with a total available BW of 500 MHz. It is compulsory to support 20-/40-/80-MHz channel BW which is recommended for high-density deployment, while it is optional to support 80 + 80-MHz contiguous or noncontiguous BW [1] which is suitable for low channel utilization. As depicted in Fig. 1(b), it introduces six 80-MHz channels, resulting in a total of 12 different combinations of 80 + 80-MHz noncontiguous

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carrier aggregation (CA). The frequency spacing between any two noncontiguous carriers ranges from 160 to 565 MHz.

Significant work has been done to support up to 80-MHz 802.11ac/ax [2]–[6]. In recent years, several architectures supporting contiguous or noncontiguous 80 + 80-MHz 802.11ac/ax are also reported [7]–[10]. In other words, this frequency combination is a new kind of CA employed by 802.11ac/ax [11]–[13]. In contrast to LTE-A, the 5-GHz-frequency bands are more concentrated and the available BW is larger. One straightforward approach to realize CA receiver is to employ several parallel direct-conversion paths [7]–[9], [14]–[17]. While it achieves a good tradeoff among power, noise, and linearity, this architecture is prone to local oscillator (LO) pulling, especially when working at intra-band mode. Increasing the frequency interval of two carriers or physical layout distance will mitigate the pulling effect, but will be subjected to the penalty of large area and limited frequency combinations. Meanwhile, various approaches have been proposed to deal with intra-band CA [18]–[21]. One attractive approach is to utilize the Weaver architecture [18], [19]. The complex down-conversion of them is implemented in analog and digital domain, respectively. Another complex signal processing approach is realized in [20] and [21]. While these two low-IF receivers support more than two carriers, both of them require further down-conversion before final signal demodulation. In summary, the complex signal processing, including the Weaver architecture, is prone to process, voltage, and temperature (PVT) variation thus requiring complicated and well-matched interaction between I - and Q -paths, resulting in limited BW. If the Wi-Fi receiver supporting 80 + 80-MHz noncontiguous CA employs parallel ZERO-IF architecture, it will be vulnerable to voltage-controlled oscillator (VCO) pulling and LO coupling, especially when dealing with small frequency spacing like 160 MHz [14]–[17]. If it employs complex signal processing which only supports less than 100-MHz-frequency spacing [18]–[21], even the minimum frequency spacing of 160 MHz will be difficult to deal with. To alleviate these problems, a hybrid direct-/double-conversion architecture is proposed [12]. However, it requires at least three LOs for the aggregation of any two carriers and a careful frequency planning to avoid VCO pulling. Another direct re-centered offset receiver uses a “re-centering” mixer to generate two copies of the original signal, one of which down-converted, while the other up-converted [13]. In addition to the problems same with that in [12], the up-converted path does need an LO with higher frequency than the original carrier frequency, thus consuming more power.

Within this context, we propose a new receiver architecture exploiting parallel sliding-IF to support 5–6-GHz wireless local area network (WLAN) CA. Section II presents the overall architecture. Section III details the analysis and design of key building blocks. The measurement results are provided in Section IV, and conclusions are drawn in Section V.

II. PROPOSED PARALLEL SLIDING-IF RECEIVER

The block diagram of proposed sliding-IF receiver targeting 5–6-GHz WLAN application is shown in Fig. 2(a).

Fig. 2. (a) Proposed receiver front-end utilizing parallel sliding-IF. (b) Comparison with prior arts when employed for 5–6-GHz WLAN.

First, the receiver begins with a single-ended LNA. It is shared by both the carriers and the input matching condition keeps constant. Next, a gm-cell with negligible gain succeeds the LNA to provide current-mode signal to the following stages. The LNA and gm-cell can be bypassed when working at low gain mode. The gm-cell is followed by a splitter to divide the signal equally between the two parallel down-conversion paths for CA working mode, whereas connecting to only one path for single-carrier working mode. Meanwhile, the splitter also works as an active balun to provide differential output. Then, a transimpedance amplifier (TIA) amplifies the down-converted current-mode signal to voltage-mode. Finally, a testing buffer is added before the output port, which brings neglectable gain and noise degradation.

The configuration of the LO generator is also shown in Fig. 2(a). For Path-1, a single-ended LO is provided externally, then converted to differential with 50%-duty-cycle before driving the first-stage passive mixer. The differential LO will be further divided by a divide-by-2 quadrature frequency divider to attain 25%-duty-cycle before driving the second-stage passive mixer. For Path-2, the architecture is similar except that it uses a divide-by-4 quadrature frequency divider. In fact, all buffers and dividers are controlled through serial-parallel interface (SPI) to tune the delay and phase imbalance. Based on the frequency allocation, Path-1 and Path-2 will also be referred to as “ $2x + 1x$ ” and “ $4x + 1x$ ”

thereinafter, respectively. The relationship between carrier frequency and LO frequency is given by

$$\begin{cases} f_{RF1} = \underbrace{f_{LO1,a}}_{f_{LO,1}=2*f_{LO1,b}} + f_{LO1,b} = \frac{3}{2} * f_{LO,1} \\ f_{RF2} = \underbrace{f_{LO1,a}}_{f_{LO,2}=4*f_{LO2,b}} + f_{LO2,b} = \frac{5}{4} * f_{LO,2}. \end{cases} \quad (1)$$

From (1), it can be seen that the required LO frequency for Path-1 is two-third of the carrier frequency and four-fifth of the carrier frequency for Path-2. As to conventional parallel direct-conversion, the required f_{LO} is twice the carrier frequency. When working at CA mode, it is better to leave the carrier with lower frequency to Path-1 and the carrier with higher frequency to Path-2, through which the frequency spacing will be larger than the other way round. For example, an f_{RF} and $f_{RF} + 160$ -MHz carrier combination results in a $2/15 * f_{RF} + 128$ -MHz LO frequency spacing when allocating f_{RF} to Path-1, while the spacing will be $2/15 * f_{RF} - 320/3$ MHz when allocating Path-1 with $f_{RF} + 160$ MHz. For parallel direct-conversion architecture, the LO frequency spacing will always be 320 MHz. Based on this allocation principle, an f_{RF} of 5.1 GHz brings a frequency spacing of 808 MHz which significantly helps to avoid LO pulling [22]. Meanwhile, the double-conversion implementation greatly lowers the effect of signal crosstalk [11], [12]. Performance comparison with prior arts is shown in Fig. 2(b).

III. CIRCUIT IMPLEMENTATION

A. Complementary LNA

The complementary architecture has been chosen which reuses dc current and provides double transconductance, aiming at a low noise figure (NF). Self-biased with a feedback resistor R_f , it requires no extra biasing circuit. By setting R_f with an appropriate value, it can achieve input matching without extra matching network. Under this condition, however, the noise performance will be bad, especially for working frequency as high as 5–6 GHz. In fact, R_f is designed with a rather large value to minimize its noise contribution. The matching network consists of a series capacitor C and a parallel inductor L . The parallel parasitic resistance of L is denoted by R_p . Fig. 3(a) depicts its schematic and equivalent noise model, which includes the channel thermal noise of the MOSFETs and the thermal noise of R_p . At the resonating frequency and under perfect matching condition, the noise factor is obtained

$$\begin{aligned} F &= 1 + \frac{\frac{4kT}{R_p} \cdot (r_s \parallel R_p \parallel r_{in})^2}{\underbrace{4kT R_s \cdot |A_{v,1}|^2}_{\text{from } R_p}} + \frac{4kT \gamma g_m \cdot \left| \frac{Z_{out} \parallel Z_F}{1 + \theta} \right|}{\underbrace{4kT R_s \cdot A_{v,1}^2 \cdot A_{v,2}^2}_{\text{from MOSFET}}} \\ &= 1 + \frac{r_s}{R_p} + \frac{4\gamma}{g_m r_s \cdot |1 + \theta|^2} \end{aligned} \quad (2)$$

where $A_{v,1} = V_{gs}/V_s$, $A_{v,2} = V_{ds}/V_{gs}$, and θ is defined as

$$\theta = g_m Y_F \cdot \frac{Z_{out} \parallel Z_F}{Y_{IN}^* + Y_F + G_P} \quad (3)$$

where $Z_{out} = r_{out} \parallel (1/SC_{out})$, $Y_F = 1/Z_F = SC_{gd}$, $G_P = 1/R_p$, and $Y_{IN} = 1/r_{in} + SC_{in}$. Once the biasing current and the dimension of the complementary cell are decided, θ will be fixed accordingly. Based on (2), F is inversely proportional to R_p and g_m , thus a higher Q_L and I_{ds} will lead to a better NF.

Simulated NF versus Q_L and I_{ds} curves at 5.5 GHz are depicted in Fig. 3(b). It is clearly seen that the simulation results agree well with (2). Due to the limitation of on-chip implementation, Q_L will generally be less than 20. To achieve an NF around 1.5 dB, a Q_L around 15- and 6-mA current will meet the requirement. The simulated gain is around 18 dB with a 1.5-dB NF when S11 stays all below -10 dB across 5–6 GHz, as shown in Fig. 3(c). Simulated input third-order intercept point (IIP3) is -2 dBm, limited by the fixed biasing condition and the high gain.

B. Active Balun-Splitter

Fig. 4(a) shows the schematic of the active balun-splitter. It consists of one gm-cell and one active balun-splitter. Gm-cell directly scales down from and well layout-matches with the preceding LNA thus requiring no extra biasing circuit. For the balun-splitter, as shown in Fig. 4(b), it contains three stages to achieve the balun function: the inductive-coupling stage achieved by L/C, the capacitor-cross-coupling (CCC) common gate (CG) pair M_1/M_2 , and the inductive-cross-coupling load L_1/C_1 .

- 1) For the inductive-coupling stage, the differential inductor can be considered as a transformer with a coupling factor of k . Based on the schematic shown in Fig. 4(b), it has

$$\begin{cases} V_N = L_p S * I_N + k L_p S * I_P \\ V_P = -(L_p S * I_P + k L_p S * I_N) \\ V_P = R_L * (I_P + SC * (V_N - V_P)). \end{cases} \quad (4)$$

At the resonating frequency when $2(k+1) * L_p C \omega^2 = 1$, it has

$$\frac{V_P}{V_N} = -\frac{1}{1 + j * \frac{2(1-k)}{Q}} \quad (5)$$

where $Q = R_L/L_p \omega$. However, Q is limited by CG-loading which is rather small, providing only primitive differencing.

- 2) For the CCC stage, define

$$\begin{cases} V_N = +(1 + \alpha) * \cos(\omega t + \theta) \\ V_P = -(1 - \alpha) * \cos(\omega t - \theta). \end{cases} \quad (6)$$

Due to the cross-coupling effect, the equivalent voltage driving M_1 and M_2 will be $V_1 = V_N - (1 - \beta) * V_P$ and $V_2 = V_P - (1 - \beta) * V_N$, where $1 - \beta$ is the coupling factor and slightly smaller than 1. Thus, V_1 and V_2 can be calculated as

$$\begin{aligned} V_1, V_2 &= \pm [(2 - \beta) \sqrt{\cos^2 \theta + \alpha^2 \sin^2 \theta} \cos(\omega t + \gamma) \\ &\quad \pm \beta \sqrt{\alpha^2 \cos^2 \theta + \sin^2 \theta} \cos(\omega t + \tau)] \end{aligned} \quad (7)$$

where $\sin \gamma = \alpha * \sin \theta / (\cos^2 \theta + \alpha^2 \sin^2 \theta)^{1/2}$ and $\sin \tau = \sin \theta / (\alpha^2 \cos^2 \theta + \sin^2 \theta)^{1/2}$. Apparently, the differential part is largely reduced when factor β is involved.

Fig. 3. (a) LNA schematic and its equivalent noise model. (b) Simulated NF swept with Q_L and I_{ds} at 5.5 GHz. (c) Simulated S11, gain, and NF.

Fig. 4. (a) Schematic of the active balun-splitter. (b) Schematic of all three coupling stages functioning as an active balun. (c) Performance comparison between double- and single-CG-stage. (d) Monte-Carlo simulation of gain and phase imbalance at different differential-nodes.

3) For the inductive-cross-coupling stage, we can get

$$\begin{cases} \frac{V_{1+}}{R_{L1}} = (1 - \frac{\mu}{2}) * I_{ds+} + \frac{\mu}{2} * I_{ds-} \\ \frac{V_{1-}}{R_{L1}} = (\frac{\mu}{2} - 1) * I_{ds-} - \frac{\mu}{2} * I_{ds+} \end{cases} \quad (8)$$

where

$$\mu = \frac{1}{1 + \frac{j(1-k_1)}{Q_1}} \quad \text{and} \quad Q_1 = \frac{R_{L1}}{\omega L_{p1}} \quad (9)$$

and Q_1 is much larger than Q making μ nearly equal to 1.

Similarly, the two cross-coupling stages induce cross-coupling between differential pairs at different nodes and greatly eliminate gain and phase imbalance. To increase the reverse isolation, a double CCC-stage rather than single-stage is employed. A comparison table between single- and double-CCC-CG stage is provided in Fig. 4(c). The Monte Carlo simulation of gain and phase imbalance at different differential nodes is shown in Fig. 4(d). The gain imbalance reduces from 2.8 dB down to less than 0.2 dB while the phase imbalance from 18° down to 0.4° across 5–6 GHz. The biasing current is 4 mA for the gm-cell and

Fig. 5. (a) Schematic of adopted passive double-conversion mixer and its driving LO. (b) Equivalent model of single-ended cascaded switch.

2 mA for each balun. This proposed balun-splitter brings several advantages. First, it acts as an active balun providing more gain and better imbalance compared to passive balun generally achieved by a transformer. Second, the enhanced reverse isolation helps lower the crosstalk between the two parallel paths. Third, the input impedance is low due to employing CCC-CG input, therefore avoiding large voltage amplification. Lastly, each balun can be turned on and off separately while the resonating frequency can be tuned to maximize its performance.

C. Sliding-IF Passive Mixer

The circuit of adopted passive double-conversion mixer is depicted in Fig. 5(a). As mentioned above, the first-stage mixer is differential driven by LO₁ with 50%-duty-cycle, while the second-stage mixer is quadrature driven by LO₂ with 25%-duty-cycle. The desired working frequency is the sum of LO₁ and LO₂ and the mixer is configured to be fully differential to reduce LO leakage and crosstalk from the other path. This double-conversion mixer can also be named as sliding-IF mixer due to the fact that the LO₁ frequency is integer times of that of LO₂ [23]–[25]. To simplify the analysis, Fig. 5(b) shows the equivalent model of single-ended passive cascaded switches. The switch can be modeled as a series of an ideal switch and a resistor in parallel with a capacitor. Accordingly, there exists some parasitic capacitance at the interconnection node of the cascaded mixer. Based on simulation, it shows a capacitance at the level of tens of fF. The ON-resistance of the switch is at the level of tens of ohm, resulting in a time constant at the level of ps, which is 1000 times lower than the period of the desired signal. Consequently, the memory effect of the parasitic capacitance can be neglected. This helps to simplify the cascaded switches to one single switch driven by an equivalent LO that is the multiplication of the two separate LOs. The equivalent resistance of this single switch is the sum of resistances of the two cascaded switches. Therefore, the equivalent LO for *IQ* paths of Fig. 5(a) can be written as

$$\begin{cases} LO_I = (LO_{1+} - LO_{1-}) * (LO_{2I+} - LO_{2I-}) \\ LO_Q = (LO_{1+} - LO_{1-}) * (LO_{2Q+} - LO_{2Q-}). \end{cases} \quad (10)$$

According to (10), Fig. 6 depicts the waveforms of LO₁, LO₂, and the equivalent LO_I and LO_Q for three different frequency combinations, denoted by “1x + 1x,” “2x + 1x,”

and “4x + 1x,” respectively. One intuitive combination is to use LO₁ and LO₂ with the same frequency, i.e., “1x + 1x.” To obtain 25%-duty-cycle, the LO frequency needs to be twice the frequency of LO₂. The advantage is the fundamental frequency of LO_I and LO_Q is the sum of LO₁ and LO₂ and equal to the desired carrier frequency thus none image induced. However, the problem is that its *IQ* phase difference is not always 90° but depends on Δ*t*, which is the time offset between LO₁ and LO₂. Based on (10) and the waveforms of LO₁ and LO₂ shown in Fig. 6(a), the relationship between *IQ* phase difference and Δ*t* can be calculated and is also shown in Fig. 6(a). As we know, an accurate 90° phase difference is a must for quadrature demodulation. Therefore, it requires a high precision time offset between LO₁ and LO₂ which is given by

$$\begin{aligned} T_{\text{shift}} &= \frac{n}{4} * T_{2x}, \quad \text{where } n = 1, 3, 5, \dots \\ &\equiv \pm \frac{1}{4} * T_{2x} \equiv \frac{1}{2} * T_{4x} \\ &\cong f_{4x} \text{ in differential mode.} \end{aligned} \quad (11)$$

As can be seen, the time offset needs to be precisely odd times of one-fourth of *T*_{2*x*} as indicated by the red dots in Fig. 6(a). To provide such precise time offset, it requires an LO with minimum frequency that is twice of *f*_{2*x*}, thus making it no better than the single-stage direct-conversion architecture, which is driven by LO with the same frequency but brings less insertion loss. Luckily, for active mixer, the “1x + 1x” architecture is still applicable and requires no specific time offset between LO₁ and LO₂ [26].

Frequency combinations of “2x + 1x” and “4x + 1x” are shown in Fig. 6(b) and (c), respectively. Based on (10) and the waveforms, the equivalent LO_I and LO_Q of “2x + 1x” and “4x + 1x” have the relationship

$$\begin{cases} LO_{Q, "2x+1x"}(t) = LO_{I, "2x+1x"}\left(t - \frac{3}{4}T_{1x}\right) \\ LO_{Q, "4x+1x"}(t) = LO_{I, "4x+1x"}\left(t - \frac{1}{4}T_{1x}\right) \end{cases} \quad (12)$$

where 3/4 * *T*_{1*x*} is equal to 9/4 * *T*_{3*x*} for “2x + 1x” and 1/4 * *T*_{1*x*} equals to 5/4 * *T*_{5*x*} for “4x + 1x.” They both correspond to a 90° phase difference at the desired working frequency, whatever Δ*t* is. Although Δ*t* has no impact on the orthogonality between LO_I and LO_Q, by applying the Fourier transformation to LO_I and LO_Q, it is found that the

Fig. 6. (a) LO waveform of "1x + 1x" and the IQ-phase difference of its equivalent LO versus Δt . (b) LO waveform of "2x + 1x" and the magnitudes of the harmonics of its equivalent LO versus Δt . (c) LO waveform of "4x + 1x" and the magnitudes of the harmonics of its equivalent LO versus Δt .

magnitudes of its 1st-, 3rd-, and 5th-harmonics of "2x + 1x" are directly decided by Δt as given by

$$\begin{cases} |\mathcal{F}_{1x}| = \frac{2}{\pi} \sqrt{6 - 4\sqrt{2} * \sin\left(\frac{1}{3} \frac{\Delta t}{T_{3x}} 2\pi + \frac{\pi}{4}\right)} \\ |\mathcal{F}_{3x}| = \frac{2}{3\pi} \sqrt{6 + 4\sqrt{2} * \sin\left(\frac{\Delta t}{T_{3x}} 2\pi - \frac{\pi}{4}\right)} \\ |\mathcal{F}_{5x}| = \frac{2}{\pi} \sqrt{6 - 4\sqrt{2} * \sin\left(\frac{5}{3} \frac{\Delta t}{T_{3x}} 2\pi + \frac{\pi}{4}\right)}. \end{cases} \quad (13)$$

As can be seen, the fundamental frequency is f_{1x} rather than f_{3x} which is the desired frequency and it has no even harmonics. $|\mathcal{F}_{3x}|$ reaches minimum and maximum at some specific values of Δt . The difference between the minimum and the maximum is 7.66 dB, which agrees well with that in [27]. When $|\mathcal{F}_{3x}|$ reaches maximum, which is the ideal case to attain maximum gain and minimum noise contribution, $|\mathcal{F}_{1x}|$ reaches minimum, while $|\mathcal{F}_{5x}|$ reaches maximum resulting in 5.77-dB rejection to f_{1x} and 4.44-dB rejection to f_{5x} . Similarly, for "4x + 1x" it has

$$\begin{cases} |\mathcal{F}_{1x}| = \frac{2}{\pi} \sqrt{10 - 4\sqrt{2} - 4\sqrt{4 - 2\sqrt{2}} * \sin\left(\frac{1}{5} \frac{\Delta t}{T_{5x}} 2\pi + \frac{3}{8}\pi\right)} \\ |\mathcal{F}_{3x}| = \frac{2}{3\pi} \sqrt{10 + 4\sqrt{2} - 4\sqrt{4 + 2\sqrt{2}} * \sin\left(\frac{3}{5} \frac{\Delta t}{T_{5x}} 2\pi + \frac{1}{8}\pi\right)} \\ |\mathcal{F}_{5x}| = \frac{2}{5\pi} \sqrt{10 + 4\sqrt{2} + 4\sqrt{4 + 2\sqrt{2}} * \sin\left(\frac{\Delta t}{T_{5x}} 2\pi - \frac{1}{8}\pi\right)}. \end{cases} \quad (14)$$

TABLE I
COMPARISON OF THREE EQUIVALENT LOS

Features	3 Frequency Combinations		
	"1x + 1x"	"2x + 1x"	"4x + 1x"
$\frac{f_{fund.}}{f_{desire}}$	$\frac{2x}{2x}$	$\frac{1x}{2x}$	$\frac{1x}{5x}$
I/Q Phase Difference	Uncertain	90°	90°
Image	No	Out-of-band	Out-of-band
$\frac{f_{vco}}{f_{carrier}}$	1	$\frac{2}{3}$	$\frac{4}{5}$
LO gain	-3.9 dB	-2.8 dB	-3.7 dB

As shown by (14), the fundamental frequency is still f_{1x} . Unlike "2x + 1x," f_{5x} is the desired frequency. $|\mathcal{F}_{5x}|$ also reaches minimum and maximum at some specific values of Δt . The difference between the minimum and the maximum is 3.5 dB. When $|\mathcal{F}_{5x}|$ reaches maximum, both $|\mathcal{F}_{1x}|$ and $|\mathcal{F}_{3x}|$ reach minimum resulting in 18.86-dB rejection to f_{1x} and 2.57-dB rejection to f_{3x} . Note that the rejection calculated here is only related to the equivalent LO, not same with the conversion gain which is also related to the loading and other blocks. Note that the simulation results are indistinguishable from the equation.

The advantages and disadvantages of all three frequency combinations are summarized in Table I. Due to the uncertainty of IQ phase difference for "1x + 1x," combination of "2x + 1x" and "4x + 1x" is chosen for this work

Fig. 7. Schematic of the TIA with gain tuning function.

to implement a parallel sliding-IF receiver which supports two-band CA.

D. TIA

As shown in Fig. 7, the TIA is also based on a complementary cell to enhance its noise performance. Meanwhile, this architecture can easily achieve a wideband signal BW which supports 802.11ac and 802.11ax. To lower the flicker noise, both PMOS and NMOS transistors are sized large enough. The feedback resistor R_f acts as the transimpedance to amplify the down-converted current-mode signal. There always exists some gain imbalance between I - and Q -paths due to layout and process mismatch, which degrades SNR and increases the difficulty for demodulation. For modulation schemes like 256-quadratic-amplitude modulation (QAM) and 1024-QAM that support high data rate, the requirement about IQ gain imbalance is more stringent. To reduce the gain imbalance, gain tuning function is integrated into the TIA as shown in Fig. 7. Three tunable resistor networks are employed to realize three different gain tuning levels, which are 0.5-dB coarse tuning, 0.05-dB moderate tuning, and 0.01-dB fine tuning realized by R_1 , R_2 , and R_3 , respectively. To realize the 0.01-dB tuning step, unlike R_1 and R_2 which are made up of a resistor network, it utilizes a transistor-based resistor whose V_{gs} is biased through another resistor network. All three gain tuning cells help to minimize the gain imbalance between I - and Q - paths. The total gain tuning range is 3 dB. Each TIA consumes 0.8 mA and it requires four identical TIAs for each path.

As analyzed before, the desired LO frequency is in fact a harmonic of the fundamental tone for each path. All RF input signals located at different harmonic frequencies will be down-converted to the same baseband simultaneously, thus making them become co-channel interferers which degrade the SNR. Although the optimized time offset helps to reject most of other harmonics, this rejection alone is not enough. Luckily, the desired frequency band of 5–6 GHz is not too wide and all these unwanted harmonics are out-of-band, which can be greatly rejected by employing an external passive bandpass filter (BPF). In addition, the LNA and balun can provide further rejection. The simulation results of the overall conversion gain are provided in Fig. 8. RF input frequencies include all the 1st-, 3rd-, and 5th-harmonics, which will all be down-converted to the same IF-baseband. Fig. 8(a) shows

the simulation results of Path-1 whose desired LO is the 3rd-harmonic of the fundamental tone, where the solid lines are obtained with ZERO time offset while the dash lines are obtained with $3/8 * T_{3x}$ time offset between $f_{LO1,a}$ and $f_{LO1,b}$. With ZERO time offset, gain rejections to the 1st- and the 5th-harmonics are 61 and 39 dB, respectively. With $3/8 * T_{3x}$ time offset, for the desired frequency, i.e., the 3rd-harmonic, gain increases by 3.2 dB while the 5th-harmonic gain increases by 7.5 dB but the 1st-harmonic gain degrades by 11 dB, thus making gain rejections to the 1st- and the 5th-harmonics change to 76 and 35 dB, respectively. Fig. 8(b) shows the simulation results of Path-2, where the solid lines are obtained with ZERO time offset while the dash lines with $5/16 * T_{5x}$ time offset between $f_{LO2,a}$ and $f_{LO2,b}$. The simulation results agree well with the trends shown in Fig. 6(b) and (c). However, there is still slight gain variation between simulation and analysis, which is because the conversion gain is decided not only by the driving LO but also the loading which has not been analyzed. The additional rejection is contributed by the LNA and balun. With a high-pass input matching network, the LNA helps to reject the low-frequency harmonics. Moreover, the balun acts as a BPF which helps to reject all other undesired tones. Through simulation it is observed that the PVT variation will change the harmonic rejection at the level of several dB, because the harmonic rejection contributed by the LNA and balun will be easily affected. However, with optimized time offset it always helps to reject the 1st-harmonic based on (13) and (14).

Meanwhile, accompanied with a blocker located at unwanted harmonics that will become co-channel interferers, Fig. 8(c) provides the corresponding conversion gain and double-sideband (DSB) NF of both paths. For Path-1, the co-channel blocker is located at the 1st- and 5th-harmonics. For Path-2, it is located at the 1st- and 3rd-harmonics. As the blocker strength increases, the gain and NF are worsened clearly because LNA saturates with blocker present. As discussed previously, all the co-channel blockers are located out-of-band and can be rejected with an external BPF. Based on the simulation, a rejection of more than 30 dB will be enough to keep both paths work properly, which can be easily achieved.

E. LO Generation

Fig. 9(a) shows the architecture of LO generation circuit. For each path it employs one active balun in the front to convert the single-ended external LO to differential. $f_{LO1,a}$ and $f_{LO2,a}$ are generated directly from the active balun with 50%-duty-cycle. For $f_{LO1,b}$, it is generated from a divide-by-2 divider with 25%-duty-cycle output. For $f_{LO2,b}$, it also needs a divide-by-2 divider with 50%-duty-cycle output before the 25%-duty-cycle divider. The 50%-duty-cycle divider is implemented with two D flip-flops which generate better differential signals than one single D flip-flop. For all four LO paths, each has a delay-tunable buffer before driving the passive mixer, which helps to realize expected time offset as analyzed in Section III-C. The schematic of proposed wideband active balun is shown in Fig. 9(b). The input signal is applied on the gate of an NMOS transistor, and

Fig. 8. (a) Simulated conversion gain for RF located at different LO harmonics of Path-1. (b) Simulated conversion gain for RF located at different LO harmonics of Path-2. (c) Simulated desired conversion gain and DSB-NF accompanied with input blocker located at unwanted LO harmonics.

Fig. 9. (a) Architecture of the internal LO generator. (b) Schematic of the proposed wideband active balun. (c) Frequency planning for the proposed receiver. (d) Schematic of divide-by-2 divider with 25%-duty-cycle output. (e) Schematic of delay-tunable buffer.

the differential outputs are taken from its source and drain stages. R_b is used to self-bias the transistor with a large value, and both R_N and R_P are tunable which tunes the phase difference between the differential outputs. The differential outputs are connected to two parallel differential amplifiers. One of them adopts a capacitor C_s to introduce a pole in order to extend the BW. Therefore, the proposed active balun can work from 1 to 15 GHz with a maximum phase error of 6°. The frequency planning is provided in Fig. 9(c), which ensures all four LOs are non-overlapping. As is shown, the frequency ranges are 1.036–1.165, 1.727–1.942, 3.453–3.883, and 4.144–4.660 GHz for $f_{LO2,b}$, $f_{LO1,b}$, $f_{LO1,a}$, and $f_{LO2,a}$, respectively. This frequency planning is very

important to avoid crosstalk and pulling from LOs and their harmonics

The schematic of employed divide-by-2 divider is shown in Fig. 9(d). This frequency divider employs two identical D-latches in a master-slave configuration with negative feedback driven by complementary clocks CLK_N and CLK_P, same as that in [28]. Based on this architecture, this divider has made two improvements. First, it utilizes a complementary cell to do the cross-coupling between the two D-latches. Through this configuration, the output phase noise can be improved and the output driving capability also increases. Another improvement is that two tunable current sources are added for each D-latch. By tuning the variance of the biasing current,

Fig. 10. (a) Die photograph. (b) Testing board. (c) Measurement setup with three different configuration modes.

Fig. 11. Measured (a) S11, (b) conversion gain, (c) DSB-NF, (d) gain and NF versus RF, and (e) and (f) gain for RF located at different harmonics for two paths.

additional phase imbalance between the IQ output signals is achieved. The minimum tuning step of phase imbalance is 0.25° and 0.12° for Path-1 and Path-2, respectively, with a total of 32 steps. The schematic of proposed delay-tunable buffer is shown in Fig. 9(e), which consists of a series of buffer cells. Configured with different dimensions for the tail MOSFETs in different cells, coarse tuning and fine tuning are realized. As analyzed previously, the optimized time offset is $3/8 * T_{3x}$ for Path-1 and $5/16 * T_{5x}$ for Path-2, where T_{3x} and T_{5x} mean a signal period whose frequency spans from 5.17 to 5.835 GHz. To cover the whole frequency band, a maximum delay of 100 ps is implemented with some margin to counter PVT variation. The delay-tuning function can be turned on and off. When the coarse tuning is turned off, the time offset between two LOs approaches ZERO with the help of fine tuning. When the coarse tuning is turned on, with some

fine tuning the optimized time offset can also be achieved. Simulated phase noise of the delay-tunable buffer cascaded with the preceding divider is below -145 dBc/Hz at 1-MHz offset for both paths.

IV. MEASUREMENT RESULTS AND COMPARISON

The proposed parallel sliding-IF receiver is fabricated in 65-nm CMOS technology. The die photograph is shown in Fig. 10(a), where “V-I” module refers to the gm-cell following the LNA and Path-1 and Path-2 refer to the active balun-splitter including the following down-conversion part. The core circuit including LO generation module occupies a total area of 0.56 mm^2 . The testing board and measurement setup are shown in Fig. 10(b) and (c), respectively.

Under 1.2 V, it consumes 35 mA for single-carrier working mode, where 20 mA is contributed by LO and 60 mA for

Fig. 12. (a) Measured IIP3 with max. gain of Path-1. (b) Illustration of “conversion gain rejection.” (c) Measured “conversion gain rejection” between two paths.

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART RECEIVERS

Ref.	Tech. (CMOS)	Topology	Freq. (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	BW (MHz)	CA	Harm. Rej.(dB)	Area (mm ²)	IIP2 (dBm)	P1dB (dBm)	Power (mW)
[2]	55nm	4x4 Dual-Band	2.4 / 5	4.2/4.8	-	-	<=160 (1024-QAM)	-	-	-	-	-	322/420
[7]	28nm	4x4 Dual-Band	2.4 / 5	2.9/3.2	-	-	<=160 (1024-QAM)	<=2	>53 IRR**	-	-	-	354/447
[8]	28nm	2x2 Dual-Band	2.4 / 5	3.6/3.8	-	-	<=160 (256-QAM)	<=2	-	-	-	-	-
[14]	40nm	Parallel Zero-IF	0.572-2.7	2.1/2.5	-	+1 OIP3*	<= 60	<= 3	-	11.3	+55 OOB***	-	13.7/17.6 mA
[17]	65nm	Parallel Zero-IF	0.69-2.1	1.3-3.2	42	+8 OIP3	12-70	2/4	46/46	1.1	-	-	96/192
[18]	65nm	Analog Complex-IF	1.96	4.5	45	2.4 OIP3	-	<= 3	> 80	0.74	>27 In-band	-15.5	155/435
[19]	45nm	Digital Complex-IF	< 3	3.8	37	-13.7	< 20	> 2	>70 IRR**	0.158	>31 In-band	-	15
[29]	65nm	Without LNA#	5.1-5.9	5.3	48/5	+2.6	20	No	-	0.183	-	-	11.6
This Work##	65nm	Parallel Sliding-IF	5.1-5.9	1.9/2.4	39/18	-14/-3	80/160	<=2	1- 70/35 2-100/35	0.56	>30 In-band	-28.5/-10	42/72

* OIP3 means out-of-band IP3. ** IRR refers to image-rejection ratio. *** OOB means out-of-band.

It uses a passive transformer to replace LNA. ## This work doesn't include baseband VGA/Filter.

two-band CA working mode where LO contributes 40 mA. Measured S11 is plotted in Fig. 11(a), which stays below -10 dB across the whole 5.17–5.835-GHz targeted frequency band. The input RF bonding wire is designed to be as short as possible and its parasitic inductance is absorbed by the input series capacitor, thus minimizing its impact on input matching.

The measured conversion gain of two paths versus IF is shown in Fig. 11(b). The working frequency is set to be 5.4 GHz for Path-1 and 5.5 GHz for Path-2. With the help of fine tuning, nearly ZERO and optimized time offset can be achieved when the coarse tuning is turned on and off. Accordingly, two types of conversion gain with ZERO and optimized time offset are attained. With ZERO time offset and only one path ON, the gain of Path-1 is 36.2 and 37.4 dB for Path-2. Both gain degrades by around 4 dB when both paths ON. With optimized time offset, the gain of Path-1 increases by 3.2 dB and by 1.6 dB for Path-2. The measured gain improvement is lower than previous simulated value due to limited tuning step and range. The measured minimum

conversion gain is 18 dB when the LNA and gm-cell are bypassed.

Measured DSB-NF versus IF is plotted in Fig. 11(c). With ZERO time offset and when only one path ON, the NF of Path-1 is 2.06 dB and 1.97 dB for Path-2 at 10 MHz. When both paths ON, both DSB-NF of two paths increases by around 0.4 dB. With optimized time offset, the NF of Path-1 reduces to 2.0 dB and Path-2 reduces to 1.87 dB. The conversion gain and DSB-NF measured at 10-MHz IF versus RF are summarized in Fig. 11(d). At different RF frequencies, the center frequency of the active balun and the time offset are tuned through SPI to attain the best performance. Across 5–6 GHz when only one path ON, the conversion gain of Path-1 ranges from 40 to 38.2 dB and from 39.4 to 37.4 dB for Path-2. Both gain degrade by around 3–4 dB when both paths ON. Meanwhile, when only one path ON, the NF of Path-1 changes from 2.16 to 1.74 dB and from 2.17 to 1.78 for Path-2. Both NF increase by around 0.4 dB when two paths ON. As the frequency increases, both conversion gain and NF

decrease, which agrees well with the previous analysis about the LNA. Fig. 11(e) and (f) shows measured conversion gain of the two paths versus RF located at different harmonics. All measurement results match well with that in Fig. 8.

A combined two-tone signal is applied at the input for IIP3 and input second-order intercept point (IIP2) measurement. As shown in Fig. 12(a), the measured IIP3 of two paths are -14 and -3 dBm with -28.5 and -10 dBm 1-dB compression point for maximum and minimum conversion gain, respectively. The measured in-band IIP2 is above 30 dBm. With the help of gain tuning from the TIA and IQ phase tuning from the divide-by-2 divider, measured gain and phase imbalance are below 1.2 dB and 1.9° , respectively.

The “conversion gain rejection” between two paths is defined and measured in Fig. 12(b) and (c), respectively. The unexpected conversion gain of the other path, whose LO frequency is different from the frequency of the input signal, is due to the parasitic coupling and limited isolation. The measured larger than 73-dB rejection across the whole band shows that the parallel sliding-IF architecture provides a good isolation between each other.

Table II summarizes the performance of the proposed receiver and other state-of-the-art literatures. Utilizing parallel sliding-IF architecture, this receiver achieves the lowest NF at the highest frequency with the largest supported BW.

V. CONCLUSION

A parallel sliding-IF-based receiver supporting two-band CA applicable for 802.11ac and next generation Wi-Fi standard has been introduced. With only two LOs required, the LO pulling and crosstalk problem can be alleviated. The time offset between the two sliding-IF LOs is found important for the conversion gain of the passive double-conversion mixer. By optimizing the time offset, larger conversion gain and lower NF can be achieved at the desired frequency for both “ $2x + 1x$ ” and “ $4x + 1x$ ” sliding-IF paths. Together with an optimized complementary LNA, a 5–6-GHz receiver is achieved with sub-2-dB NF and 39-dB conversion gain.

In fact, all RF input signals located at different harmonic frequencies will be down-converted to the same baseband simultaneously, making them become co-channel interferers which degrade the SNR. Luckily, all unwanted harmonic frequencies are located out-of-band and can be greatly attenuated by virtue of an external BPF.

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