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A Dual-Mode Modulation Technique for Controlling the Average Neutral Point Current in Neutral-Point-Clamped Converters

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Abstract—This paper presents a dual-mode modulation technique which aims to control the average current flow into the neutral point (NP) of the neutral-point-clamped (NPC) converter without the need for any additional hardware. The two modes of operation are normal mode and compensating mode. In the normal operation mode, all the three phases switch between two consecutive voltage levels (between the positive or negative dc-rail and the neutral point) in a switching period. In the compensating operation mode, at least one of the phases switches between the positive and negative dc-rails in a switching period. An analytical solution is developed to determine the duration of these two operation modes within each fundamental cycle based on the converter's operating condition. An advantage of this solution is that it can be generalized for balancing the capacitor voltages in all applications employing NPC converters. The proposed solution also determines the maximum average NP current injection capacity of the NPC converter under dual-mode modulation technique, which indicates the stable operating range of the converter. The performance of the proposed modulation technique is validated experimentally for various loading conditions.

Index Terms—Carrier-based pulsewidth modulation, neutral-point-clamped (NPC) converter, neutral-point current.

NOMENCLATURE

v_{ga}, v_{gb}, v_{gc}	Grid phase voltages
θ_g	Grid voltage angle
f	Grid frequency
f_s	Carrier frequency
i_a, i_b, i_c	AC-side currents in abc frame
i_d, i_q	AC-side currents in dq frame
I_m	Maximum value of phase current
i_d^*, i_q^*	AC-side current references in dq frame
ϕ	Phase angle difference between the ac-side current and the grid voltage
v_a, v_b, v_c	AC-side phase voltages of the NPC converter
v_{ab}, v_{bc}, v_{ca}	AC-side line-to-line voltages of the NPC converter
v_a^*, v_b^*, v_c^*	Normalized ac-side phase voltage references of the NPC converter in abc frame
v_d^*, v_q^*	AC-side voltage references of the NPC converter in dq frame
m	Modulation index

δ	Phase angle difference between the converter's ac-side voltage and the grid voltage
L	Grid connection filter inductor
v_{dc}	DC-link voltage
V_{dc}^*	DC-link voltage reference
C_1, C_2	DC-link capacitors
v_{C1}, v_{C2}	DC-link capacitor voltages
R_{d1}, R_{d2}	Bipolar dc-bus resistive loads
I_{d1}, I_{d2}	Bipolar dc-bus average currents
i_{NP}	Neutral-point current
$\bar{i}_{NP}$	Neutral-point current averaged over a fundamental period of the grid voltage
i_{NPref}	Neutral-point current reference
$\bar{i}_{NPref}$	Neutral-point current reference averaged over a fundamental period of the grid voltage
i_{NPmax}	Maximum instantaneous neutral-point current
i_{NPmaxa}	Minimum value of i_{NPmax} in a fundamental period of grid voltage
i_{NPmaxb}	Maximum value of i_{NPmax} in a fundamental period of grid voltage
α	Duration of the compensating operation mode
$d_{NP_a}, d_{NP_b}, d_{NP_c}$	Duty cycles for connecting the three phases to the neutral-point
$d_{l_a}, d_{l_b}, d_{l_c}$	Duty cycles for connecting the three phases to the negative dc-rail
$d_{h_a}, d_{h_b}, d_{h_c}$	Duty cycles for connecting the three phases to the positive dc-rail

I. INTRODUCTION

In the past half-century, the neutral-point-clamped (NPC) converter has gained wide popularity due to its advantages like improved output voltage waveform quality, reduced dv/dt and lower semiconductor voltage ratings as compared to conventional two-level voltage source converters. The NPC converter can operate with a single dc source and has a simple structure leading to a small footprint [1]. Moreover, the neutral point (NP) accessibility allows independent control of the split dc-link capacitors. As a result, the NPC converter has been extensively utilized in various applications including medium

voltage drives [2]–[5], grid integration of renewable energy sources like solar [6]–[10] and wind [11]–[15], static reactive power compensators [16]–[19], etc.

One of the major challenges associated while employing the NPC converter for the aforementioned applications is balancing the dc-link capacitor voltages. Many attempts have been made in the literature to address this issue. One of the solutions for controlling back-to-back NPC converter-based wind energy systems is to apply the finite control set model predictive control (FCS-MPC) due to its inherent capability of handling multiple objectives and constraints for such nonlinear systems [11], [12], [14]. Although the dc-link capacitor voltages can be balanced with FCS-MPC, it has a large computational complexity especially when the prediction horizon is greater than one. A capacitor voltage balancing strategy using optimum-predictive control is also presented in the literature for bipolar back-to-back NPC converters employed in high-voltage dc transmission systems [20].

In [13], the authors added an active current compensation device (constituted by a dc-dc boost converter) to the back-to-back NPC converter configuration to balance the dc-link capacitor voltages and to supply the additional average NP current required under unbalanced load conditions. The compensation device helps in balancing the capacitor voltages. In [21], the authors presented a new architecture to charge the electric vehicles using the bipolar dc-bus of the grid-integrated NPC converter. An additional voltage balancing circuit (constituted by an extra phase leg) was also employed to facilitate the capacitor voltage balancing under all operating conditions. Similarly, an auxiliary converter was added to ensure maximum power production from solar photovoltaic arrays integrated to the grid using a central NPC converter in [8]. The addition of extra circuits and converters in all the previous approaches increases the switching losses and system cost, size and complexity.

In [10], the authors proposed a pulsewidth modulation (PWM) method to control two solar PV arrays asymmetrically by modifying the three-phase turn-on times. The effect of asymmetric capacitor voltages on the ac-side output voltages is eliminated by modifying the reference voltages. Another technique based on virtual space-vector pulsewidth modulation (SVPWM) is presented in [6] to independently control the PV array voltages in a multilevel diode-clamped converter. With

these techniques, the solar PV arrays can track the maximum power point independently. However, the maximum average NP current injection capability of the NPC converter with these techniques is not presented in the literature.

The capacitor voltage balancing issue becomes more challenging to deal with when unbalanced dc loads are connected to the bipolar dc-bus causing a nonzero average current flow in the NP which, if not compensated, causes the capacitor voltages to diverge, and hence destabilizing the converter [13]. The capacitor voltage balancing solutions presented in the literature [8], [11]–[15], [21] are generally designed to target a particular application of the NPC converter, consequently, such solutions are not extendable to other systems employing NPC converters. Moreover, previous attempts to control the NP current were focused on controlling the instantaneous NP current [6], [22]–[24]. Fig. 1(a) shows the variation of maximum instantaneous NP current ($i_{NP_{max}}$) that can be generated over a fundamental time period with the assumption of a sinusoidal ac-side voltage and current. Due to the time-varying nature of $i_{NP_{max}}$, the required average NP current ($i_{NP_{ref}}$) can be linearly controlled only when its value is less than $i_{NP_{maxa}}$. When the required $i_{NP_{ref}}$ lies between $i_{NP_{maxa}}$ and $i_{NP_{maxb}}$, the controller is partially saturated as shown in Fig. 1(b). Consequently, the generated average NP current is lower than the required $i_{NP_{ref}}$. The controller output becomes completely saturated when the required $i_{NP_{ref}}$ exceeds $i_{NP_{maxb}}$ and utilizes the maximum capacity of the NPC converter in order to generate the maximum possible average NP current. In order to avoid partial saturation of the generated average NP current, this paper proposes a simple dual-mode modulation technique based on an average NP current approach. The main advantage of the proposed solution is its generality for balancing the capacitor voltages in all bipolar dc-bus applications employing NPC converters such as wind energy systems, grid-integrated solar photovoltaic systems, static reactive power compensators, electric vehicle charging systems, etc.

The proposed dual-mode modulation technique, as the name suggests, has two operating modes: normal operation mode (NOM) and compensating operation mode (COM). In NOM, all the phases switch in two consecutive voltage levels in each switching period, i.e., either between the positive dc-rail and the NP or between the negative dc-rail and the NP. In COM,

Fig. 1. (a) Variation of maximum NP current over a fundamental time period, and (b) partial saturation under instantaneous NP current approach.

at least one of the phases switches between the positive and negative dc-rail in a switching period to inject the required average NP current. An analytical solution is developed to determine the duration of these two operation modes within each fundamental cycle based on the converter's operating condition. The main contributions of the proposed dual-mode modulation technique are:

- The proposed modulation strategy is based on average NP current.
- In the proposed technique, average NP current is correlated to a new control variable (α), which allows for having a linear control system design unlike the modulation strategies controlling the instantaneous NP current.
- This correlation is developed analytically by using the ac-side voltages and currents, and the required average NP current over the fundamental period.
- The maximum average NP current injection capability of the NPC converter under dual-mode modulation technique is analytically calculated, which indicates the stable operating range of the converter unlike the proportional-integral controller-based conventional voltage balancing techniques.
- The proposed generalized solution is applicable to all bipolar dc-bus applications employing the NPC converter.
- A dq -based control scheme is presented using the proposed dual-mode modulation technique for a three-phase grid-connected NPC converter feeding bipolar dc-loads with the aim of balancing the dc-link capacitor voltages.

The organization of the paper is as follows. Section II introduces the proposed analytical solution for injecting the required average NP current and explains the two operation modes. Section III presents the proposed control scheme of the NPC converter. Section IV provides experimental results to validate the performance of the proposed modulation technique, while Section V concludes the outcomes of this work.

II. PROPOSED AVERAGE NP CURRENT INJECTION STRATEGY

Fig. 2 shows the circuit diagram of a three-phase three-level NPC converter. In order to generalize bipolar dc-bus applications of the NPC converter [11]–[15], [21], the dc-side is represented using two current sources (I_{d1} and I_{d2}). The back-to-back converter can be regarded as a special case of this generalized circuit in which the current sources are replaced by another NPC converter. Similarly, these current sources can be a representation of multiterminal dc-loads. Considering the two dc-link capacitor voltages to be equal, for a balanced bipolar dc-bus ($I_{d1} = I_{d2}$), i.e., no average current flows through the NP. However, if $I_{d1} \neq I_{d2}$, a nonzero average current flows to the NP. Each of the three phases of the NPC converter behave as a single-pole triple-throw switch and can be connected to either positive dc-rail (+1), negative dc-rail (-1) or NP (0) [1]. As a result, the NP current is contributed by all the phases and is dependent on the duty cycles connecting the phases to the NP and the phase currents as follows:

$$i_{NP} = \sum d_{NPj} i_j \quad \text{with} \quad j = \{a, b, c\}. \quad (1)$$

Fig. 2. Schematic of a three-phase NPC converter.

The obtained i_{NP} is averaged over the fundamental grid voltage period in order to obtain the average NP current ($\bar{i}_{NP}$). It is clear that the duty cycle connecting the respective phase to the NP plays a major role in determining $\bar{i}_{NP}$. Different modulation strategies have been implemented in the literature to calculate the duty cycle. One of the most commonly employed modulation techniques is the two-level modulation [25], in which each phase switches only in two consecutive voltage levels over a switching period, i.e., either between the positive dc-rail and the NP or the negative dc-rail and the NP. Using two-level modulation, the NP duty cycle for phase j is given by [25], as:

$$d_{NPj} = 1 - |v_j^*| \quad (2)$$

where, v_j^* represents the normalized ac-side voltage reference of phase ' j ' in the abc frame. The waveforms of normalized voltage and current of phase ' a ', i_{NP} and $\bar{i}_{NP}$ are shown in Fig. 3(a). The results in this figure are obtained from (1) with the assumption of a sinusoidal ac-side voltage and current, i.e., $v_a^* = m \cos(\theta_g + \delta)$ and $i_a = I_m \cos(\theta_g - \phi)$. As can be seen, in the two-level modulation strategy, the contribution of phase ' a ' to $\bar{i}_{NP}$ is zero. The effect of the remaining phases can also be analyzed in a similar manner. As a result, the average NP current adds to zero over a fundamental period when all the phases switch in two consecutive voltage levels (shown in Fig. 3(a)). Therefore, in applications requiring an average NP current, this modulation technique is not effective.

Lopez *et al.* [22] presented the 'three-level modulation' technique in which one of the phases is chosen to switch in three voltage levels in one switching period, i.e., positive dc-rail, negative dc-rail and NP, while the other two phases switch only in two consecutive voltage levels (like the two-level modulation). In [22], the authors only analyzed the three-level modulation technique for a single dc voltage source without utilizing the NP ($\bar{i}_{NP} = 0$) and the main objective of the paper was to completely eliminate the NP voltage ripples.

Fig. 3. Waveforms of normalized phase voltage and current of phase ‘a’ with producing: (a) Zero $\bar{i}_{NP}$, (b) positive $\bar{i}_{NP}$ and (c) negative $\bar{i}_{NP}$.

Nevertheless, the study showed that switching one or more phases in three voltage levels is an effective way of controlling the NP current.

In a simpler way, if phase ‘j’ switches only between the positive dc-rail and the negative dc-rail in a switching period, then $d_{NPj} = 0$. This feature provides a freedom to inject or withdraw current in/from the NP in order to generate the required average NP current $\bar{i}_{NP}$, as shown in Figs. 3(b) and (c). These figures demonstrate how the $\bar{i}_{NP}$ changes by modifying d_{NPj} . By switching a phase between the positive and negative dc-rails during the compensating operation mode for an α interval within a fundamental period, the symmetry of i_{NP} is disturbed resulting in a net nonzero $\bar{i}_{NP}$. The d_{NPj} is zero for the α interval while it is calculated using the two-level modulation for the rest of the interval and is equal to $1 - |v_j^*|$. The α span for each phase is placed symmetrically on the positive or negative peak of the phase current, which determines the direction of $\bar{i}_{NP}$. Fig. 3(b) shows that the NP current contribution of phase a is zero for the α span. As the α span coincides with negative values of i_a , the resultant average NP current is positive. In Fig. 3(c), a negative average NP current is obtained by making $d_{NPj} = 0$ when i_j is

positive. Therefore, an average NP current over a fundamental cycle can be easily generated by switching the phases between the positive and negative dc-rails for an interval α . When $\alpha \leq 2\pi/3$, only one phase switches between the positive and negative dc-rail (Fig. 4(a)). However, when $2\pi/3 < \alpha \leq \pi$, two phases switch between the positive and negative dc-rail simultaneously (Fig. 4(b)). The maximum $|\bar{i}_{NP}|$ is obtained when $\alpha = \pi$.

In this paper, an analytical solution is developed for calculating α in order to inject/withdraw the required amount of NP current to maintain the dc-link capacitor voltages balanced. The magnitude of $\bar{i}_{NPref}$ is equal to the total average current generated under COM. The main advantage of the proposed analytical solution is its capability to linearly control the NP current reference by just employing the ac-side voltages and currents. Considering all the phases contribute equally to the average NP current, the per-phase contribution of one phase is equal to one-third of the required average NP current ($\bar{i}_{NPref}$). Therefore, the average NP current contribution of phase a can

Fig. 4. Compensating operation mode when: (a) $\alpha \leq 2\pi/3$ and (b) $2\pi/3 < \alpha \leq \pi$.

Fig. 5. Calculation of α for different power factor angles.

be equated to one-third of $\bar{i}_{NPre f}$ as follows,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - |v_a^*|) i_a d\theta_g. \quad (3)$$

with the assumption of sinusoidal voltage and current,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - |m \cos(\theta_g + \delta)|) I_m \cos(\theta_g - \phi) d\theta_g. \quad (4)$$

If ϕ lies in the first quadrant, such that $0 \leq \phi \leq \pi/2$, then from Fig. 4:

$$\phi + \frac{\alpha}{2} \leq \frac{\pi}{2} - \delta \implies \alpha \leq \pi - 2\delta - 2\phi \quad (5)$$

Equation (4) can be written as,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - m \cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g \quad (6)$$

Integrating (6) with respect to θ_g yields,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{I_m}{4\pi} \left[-m \cos(\phi + \delta) \sin \alpha - \alpha m \cos(\phi + \delta) + 4 \sin\left(\frac{\alpha}{2}\right) \right] \quad (7)$$

The MATLAB curve-fit tool is utilized to approximate the sine

functions as quadratic functions for obtaining a direct solution. These approximations have less pronounced effects on the solution as their R^2 (measure of goodness-of-fit) value is very close to 1. Therefore, $\sin\alpha$ and $\sin(\alpha/2)$ are approximated as,

$$\begin{aligned} \sin\alpha &= -0.4162\alpha^2 + 1.308\alpha - 0.0475 \text{ and} \\ \sin\left(\frac{\alpha}{2}\right) &= -0.08449\alpha^2 + 0.5972\alpha - 0.02353. \end{aligned} \quad (8)$$

Substituting (8) in (7) and rearranging, a quadratic equation as a function of α is obtained as,

$$\begin{aligned} &(0.4162m\cos(\phi + \delta) - 0.33796)\alpha^2 \\ &+ (-2.308m\cos(\phi + \delta) + 2.3888)\alpha \\ &+ \left(0.0475m\cos(\phi + \delta) - 0.09412 - \frac{4\pi\bar{i}_{NPref}}{3I_m}\right) = 0. \end{aligned} \quad (9)$$

Solving (9) for α :

$$\begin{aligned} \alpha &= \frac{28850m\cos(\phi + \delta) - 29860 \pm 12500\sqrt{k}}{10405m\cos(\phi + \delta) - 8449} \text{ where} \\ k &= 5.2477m^2\cos^2(\phi + \delta) - 10.805m\cos(\phi + \delta) \\ &+ 6.9699m\frac{\bar{i}_{NPref}}{I_m}\cos(\phi + \delta) - 5.6597\frac{\bar{i}_{NPref}}{I_m} \\ &+ 5.5791 \end{aligned} \quad (10)$$

If the condition in (5) is not met, then (4) can be written as:

$$\begin{aligned} \frac{\bar{i}_{NPref}}{3} &= \frac{1}{2\pi} \left[\int_{\phi-\alpha/2}^{\pi/2-\delta} (1 - m\cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g \right. \\ &\quad \left. + \int_{\pi/2-\delta}^{\phi+\alpha/2} (1 + m\cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g \right] \end{aligned} \quad (11)$$

Integrating (11) with respect to θ_g yields,

$$\begin{aligned} \frac{\bar{i}_{NPref}}{3} &= \frac{I_m}{4\pi} \left[-2m\sin(\phi + \delta)\sin^2\left(\frac{\alpha}{2}\right) \right. \\ &\quad \left. + (2\delta + 2\phi - \pi)m\cos(\phi + \delta) + 4\sin\left(\frac{\alpha}{2}\right) \right] \end{aligned} \quad (12)$$

Rearranging (12),

$$\begin{aligned} &2m\sin(\phi + \delta)\sin^2\left(\frac{\alpha}{2}\right) - 4\sin\left(\frac{\alpha}{2}\right) \\ &- (2\delta + 2\phi - \pi)m\cos(\phi + \delta) + \frac{4\pi\bar{i}_{NPref}}{3I_m} = 0 \end{aligned} \quad (13)$$

Equation (13) is a quadratic equation of $\sin(\alpha/2)$, which can be solved to obtain α as,

$$\begin{aligned} \alpha &= 2\sin^{-1}\left(\frac{2 \pm \sqrt{p}}{2m\sin(\phi + \delta)}\right), \text{ where} \\ p &= 4 + m^2(2\delta + 2\phi - \pi)\sin(2\phi + 2\delta) \\ &\quad - \frac{8m\pi}{3} \frac{\bar{i}_{NPref}}{I_m} \sin(\phi + \delta) \end{aligned} \quad (14)$$

Similar steps have been taken to calculate α under different power factor angles and are summarised in Fig. 5. The calculated α determines the duration of COM.

Fig. 6. Variation of the maximum NP average current with respect to I_m under different modulation indices and load phase angles with $\delta = 0^\circ$.

Moreover, the maximum magnitude of NP average current injection is obtained when $\alpha = \pi$ radians. Setting $\alpha = \pi$ radians in (3) and integrating, the following relations are obtained:

$$\begin{aligned} |\bar{i}_{NPref_{max}}| &= |\bar{i}_{NPref_{min}}| = \frac{3I_m}{2\pi} \left[2 - m\sin(\phi + \delta) \right. \\ &\quad \left. + \left(\phi + \delta - \frac{\pi}{2}\right)m\cos(\phi + \delta) \right] \\ &\text{for } 0 \leq \phi \leq \pi \end{aligned} \quad (15)$$

and

$$\begin{aligned} |\bar{i}_{NPref_{max}}| &= |\bar{i}_{NPref_{min}}| = \frac{3I_m}{2\pi} \left[2 + m\sin(\phi + \delta) \right. \\ &\quad \left. - \left(\phi + \delta + \frac{\pi}{2}\right)m\cos(\phi + \delta) \right] \\ &\text{for } -\pi \leq \phi \leq 0 \end{aligned} \quad (16)$$

where $\bar{i}_{NPref_{max}}$ and $\bar{i}_{NPref_{min}}$ are the maximum and minimum NP average currents that can be injected under the proposed dual-mode modulation technique, respectively. Fig. 6 shows the variation of maximum average NP current with respect to I_m under different modulation indices and load phase angles with $\delta = 0^\circ$. Therefore, the average NP current injection capability increases when the modulation index decreases. Moreover, the effect of phase angle (ϕ) on the maximum NP average current capability is more prominent at higher modulation indices.

III. PROPOSED CONTROL SCHEME

The proposed dual-mode modulation technique is applicable to all bipolar dc-bus applications employing NPC converters as it only requires the converter's ac-side voltages and currents and the average NP current reference for its implementation. For validating the analytical solution obtained using the dual-mode modulation technique, a three-phase grid-connected NPC converter feeding bipolar dc-loads, as shown in Fig. 7, is considered. The overview of the proposed control strategy is shown in Fig. 8 and the functionality of different components is explained below.

1) DC-link voltage control

The sum of dc-link capacitor voltages is compared to

(a)

(b)

Fig. 7. (a) Circuit diagram of a three-phase grid-connected NPC converter, and (b) picture of the hardware prototype.

the dc-link voltage reference and is fed to a proportional integral (PI) controller in order to generate i_d^* .

2) Current controller

A dq -based current controller is employed to generate the ac-side voltage references of the NPC converter in the dq frame.

3) Generation of converter voltage references

The ac-side voltage references in dq frame are transformed into abc form and are then normalized to obtain v_a^* , v_b^* and v_c^* .

4) Calculation of average NP current reference

In order to keep the dc-link capacitor voltages balanced, the capacitor voltage v_{C1} is compared to half of the dc-link voltage reference (V_{dc}^*) and the difference is fed to a PI controller to obtain i_{NPref} .

5) Calculation of the duration of the compensating mode

The obtained i_{NPref} , m , δ , I_m and ϕ values are utilized

TABLE I
EXPERIMENTAL PARAMETERS

Parameter	Value
DC-link voltage reference, V_{dc}^*	350 V (2 pu)
DC-link capacitors (each), $C1, C2$	2.2 mF (0.041 pu)
Carrier frequency, f_s	2 kHz
Nominal voltage	175 V (1 pu)
Nominal power	1.3 kW (1 pu)
Nominal current (rms)	3.5 A (1 pu)
Power factor	1
Grid frequency, f	50 Hz
Grid connection filter inductor, L	5 mH (0.045 pu)

to calculate α using the equations shown in Fig. 5. If the average NP current reference is outside the range of maximum and minimum average NP current, α is taken as π radians.

6) Computation of duty cycles

Depending on the operation mode, the duty cycle connecting the phases to the NP is computed. When applying COM, the phase switching between the positive and negative dc-rail has its NP connecting duty cycle zero, while the rest of the phases switch in two consecutive voltage levels and their NP duty cycles are calculated using (2). When applying NOM, all the phases switch in two consecutive voltage levels.

The duty cycles for connecting phase 'j' to the negative and positive dc-rails are calculated as [22]:

$$d_{lj} = \frac{1 - d_{NPj} - v_j}{2}, \quad \text{with } j = \{a, b, c\}. \quad (17)$$

$$d_{hj} = 1 - d_{NPj} - d_{lj}. \quad (18)$$

The calculated duty cycles are fed to a state machine, which is explained in the Appendix. The state machine model has been implemented in practice to avoid any forbidden commutation state of the converter. It plays an important role in case the semiconductors of the converter are not able to deal with the total dc-link voltage. The state-machine model also helps in reducing the dv/dt while operating in three voltage levels. The duty cycles generated from the state machine are then compared with the carrier signal to generate the switching pulses of the NPC converter [26].

IV. EXPERIMENTAL RESULTS

For validating the performance of the proposed dual-mode modulation technique, different tests have been performed on a laboratory prototype using dSPACE controller with the circuit diagram shown in Fig. 7. The parameters of the experimental setup are provided in Table I.

A. Dynamic Performance of the Proposed Dual-Mode Modulation Technique

Fig. 9 shows the dynamic performance of the proposed dual-mode modulation technique when the bipolar dc-bus load is varied. When $R_{d1} = R_{d2} = 50\Omega$, the average NP current reference (i_{NPref}) is zero. From the results, it is clear that the

Fig. 8. Control scheme: (a) Generation of normalized reference ac-side voltages and (b) computation of duty cycles.

Fig. 9. Dynamic performance of the proposed dual-mode modulation technique under different dc-load conditions: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c and (b) waveforms of α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$.

generated average NP current ($\bar{i}_{NP}$) tracks the $\bar{i}_{NPref}$ and the capacitor voltages are balanced under balanced bipolar dc-bus load.

Under unbalanced bipolar dc-bus loads, in which $R_{d1} \neq R_{d2}$, a nonzero average NP current is required in order to balance the capacitor voltages. From Fig. 9(b), it can be seen that with the proposed dual-mode modulation technique, the generated average NP current follows the nonzero $\bar{i}_{NPref}$. The angle α increases (implying that the duration of COM increases) with the increase in load imbalance as expected. As a result, the steady state capacitor voltages are balanced even in the presence of dc-load imbalance, as shown in Fig. 9(a). It is clear that the proposed dual-mode modulation technique has the capability to generate negative average NP current and maintain balanced capacitor voltages.

B. Steady State Performance of the Proposed Dual-Mode Modulation Technique

For analyzing the performance of the proposed dual-mode modulation technique comprehensively, Figs. 10 and 11 show the steady-state performance under balanced load ($R_{d1} = R_{d2}$) and unbalanced load ($R_{d1} \neq R_{d2}$), respectively. The capacitor voltages are balanced under both the cases. However, the THD of v_{ab} observed is higher under unbalanced dc-load as compared to balanced dc-load. This is due to the fact that with unbalanced dc-loads, the proposed modulation technique operates for more duration in the COM, resulting in more harmonic components at high frequencies. This is also observed in Fig. 12 that as the duration of COM, i.e., α increases, the THD of v_{ab} increases. Consequently, the ac-side currents show more distortion under unbalanced load, as observed from the THD of i_a . Figs. 10 and 11 also show the common-mode voltage (v_{CM}) obtained at steady-state which is given by:

$$v_{CM} = \frac{v_{a0} + v_{b0} + v_{c0}}{3}. \quad (19)$$

From Figs. 10(d) and 11(d), it is observed that as α increases, the high frequency components of v_{CM} also increase. Therefore, one of the drawbacks of the proposed modulation technique is that higher common-mode voltages are observed at higher values of α . As a result, for applications susceptible to electromagnetic interference arising from common-mode voltages, a filter needs to be designed and incorporated along with the proposed dual-mode modulation technique.

C. Performance of the Proposed Dual-Mode Modulation Technique under Excess Average NP Current Injection

As mentioned before, the maximum average NP current that the NPC converter can inject is when $\alpha = \pi$ radians. Fig. 13 shows the performance of the proposed dual-mode modulation technique when R_{d1} is varied resulting in an increase in $|\bar{i}_{NPref}|$. From the figure, it is clear that α increases with an increase in $|\bar{i}_{NPref}|$ and reaches a maximum value of π radians when the required $|\bar{i}_{NPref}|$ is greater than the maximum average NP current injection limit. Under this condition, the capacitor voltages obtained are unbalanced. If the NPC converter with dual-mode modulation technique is

Fig. 10. Steady-state performance with balanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM} .

Fig. 11. Steady-state performance with unbalanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, and (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM} .

Fig. 12. Total harmonic distortion of the line-to-line voltage (v_{ab}) at different values of α .

Fig. 13. Validation of maximum average NP current injection limits: waveforms of v_{C1} , v_{C2} , α (in rad), $\bar{i}_{NPref}$ and $\bar{i}_{NP}$.

employed for an application, which requires the capacitor voltages to be balanced in addition to an average NP current reference greater than $\bar{i}_{NPref_{max}}$, an external circuit can be considered.

V. LOSS COMPARISON AMONG DIFFERENT MODULATION TECHNIQUES

A switching and conduction loss comparison is carried out by following the power loss procedure laid out in [23], [24] using the simulation parameters shown in Table II. Fig. 14 shows the switching and conduction loss comparison among

TABLE II
SIMULATION PARAMETERS FOR LOSS CALCULATION

Parameter	Value
DC-link voltage reference, V_{dc}^*	1500 V (2 pu)
DC-link capacitors (each), $C1, C2$	5.8 mF (0.048 pu)
Carrier frequency, f_s	2.5 kHz
Nominal voltage	750 V (1 pu)
Nominal power	75 kW (1 pu)
Nominal current (rms)	47.13 A (1 pu)
Power factor	1
Grid frequency, f	50 Hz
Grid connection filter inductor, L	8 mH (0.22 pu)

Fig. 14. Loss comparison among different modulation techniques.

two-level modulation, three-level modulation and the proposed dual-mode modulation technique under different loading conditions. From this figure, it is clear that the conduction loss is almost the same for all the three modulation techniques as the only difference lies in the conducting device (IGBT/diode) at various instants. As $R_{d1} = R_{d2}$, $\alpha = 0 \text{ rad}$ implying no phase is switching in three voltage levels, the difference between the switching losses of two-level modulation and the proposed dual-mode modulation technique is very small, while the highest switching losses are obtained with three-level modulation. When $\alpha = \pi/2 \text{ rad}$, the switching losses obtained under three-level modulation and the proposed dual-mode modulation is almost the same. However, for $\alpha = \pi \text{ rad}$, the switching losses are higher for proposed modulation technique as two phases are switching in three voltage levels, unlike three-level modulation wherein only one phase switches in three voltage levels. Thus, as the duration of COM increases, i.e., when α increases, the switching losses obtained with the proposed dual-mode modulation technique also increase.

VI. CONCLUSION

In this paper, a dual-mode modulation technique has been presented to balance the dc-link capacitor voltages under all bipolar dc-bus applications employing NPC converters. Using a combination of two modes, the modulation technique provides the average current required at the NP keeping the capacitor voltages balanced. An advantage of the proposed modulation technique is that an analytical solution has been developed using the NPC converter's ac-side voltages and currents in order to determine the durations of the two modes. Experimental results confirm the effectiveness of the proposed dual-mode modulation technique under the steady-state and dynamic operations. Moreover, the analytical solution provides the maximum average NP current injection capability of the NPC converter with the proposed dual-mode modulation technique, which determines the stable operating region of the converter. The proposed approach presents a benchmark for further extending the operating limits of this converter. In this regard, controlling the duty cycle by common mode voltage and flexibility with changing the reactive power magnitude seem to be viable options to explore as future directions of this study.

APPENDIX STATE MACHINE MODEL

A state-machine model, as shown in Fig. 15, has been implemented to avoid any forbidden commutation state of the converter. This model also helps in reducing the dv/dt jumps when a phase operates in COM, i.e., when it is switching in three voltage levels.

Fig. 15. State-machine model.

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