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CMOS POWER DETECTOR AND POWER AMPLIFIER DESIGN FOR WLAN 802.11ax

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School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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李晨阳

.....

Li Chenyang

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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.....

Boon Chirn Chye

Authorship Attribution Statement

This thesis contains material from 2 paper(s) published in the following peer-reviewed journals where I was the first and/or corresponding author.

Chapter 3 is published as Chenyang Li, Chirn Chye Boon, Xiang Yi, Zhipeng Liang, Kaituo Yang. "Compact Switched-Capacitor Power Detector with Frequency Compensation in 65-nm CMOS." IEEE Access (accepted) and Chenyang Li, Xiang Yi, Chirn Chye Boon, Kaituo Yang. "A 34-dB Dynamic Range 0.7-mW Compact Switched-Capacitor Power Detector in 65-nm CMOS." IEEE Transactions on Power Electronics 34(10): 9365-9368.

The contributions of the co-authors are as follows:

- Prof. Boon provided the initial project direction and edited the manuscript drafts.
- The schematic and layout design of the circuit was accomplished by me.
- Dr. Yi assisted on analyzing the data and organized the flow of the manuscript.

- Dr. Liang helped on the digital circuit design.
- I conducted the measurement of the fabricated circuit with the help of Kaituo Yang.

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Summary

With the trend of increasing data throughput, modern wireless communication standards prefer to utilize high spectral-efficiency modulations, such as 256-Quadrature amplitude modulation (QAM) and 1024-QAM modulations, which leads to large peak-to-average power ratio (PAPR). This requires radio frequency (RF) power amplifiers (PAs) with high linearity and high efficiency performances even when operating in the power back-off (PBO) region. Besides, power control is essential for power amplifier to maintain reliable communications and extend battery life in mobile devices. Power detector (PD) is usually utilized for this purpose in the transmitter systems. With large PAPR, wide dynamic range (DR) is required for PD to work in modern systems. Therefore, the focus of this thesis is to design high linear PAs with reasonable efficiency integrated with wide DR PDs working in multi-band supported modern communication systems.

Firstly, a novel PD with wide DR and area efficiency is proposed for wireless local area network (WLAN). The proposed diode PD solves low dynamic range problem by using both the positive and negative cycle of the

input signals. Then, a variation of the proposed diode PD is introduced by replacing the diode by self-biased metal–oxide–semiconductor field-effect transistors (MOSFETs). The difference between the diode and MOSFET PD is also analyzed. Finally, a PD with frequency detection circuits to compensate the effect of input frequency variations by changing the load resistances is presented to support multi-band in modern communication systems. The PD employs self-biased P-type and N-type MOSFETs as switches and utilizes a balanced structure to increase the DR of the PD.

Secondly, a linear PA with compensated non-linear trans-conductance integrated the proposed PD is introduced. The adaptive body biasing technique is achieved through envelop detectors to obtain the envelope information of the input signal. Based on this information, the body bias is changed accordingly to extend the duty cycle of MOSFET working in saturation region. This way the MOSFET works less in non-linear regions such as cut-off region or triode region in one duty cycle. Therefore, the power amplifier improves the linearity without degrading other performances of PA. The output power of the PA can be monitored by the proposed PD.

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List of Abbreviations

ABB	Adaptive Body Bias
ACI	Adjacent Channel Interference
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
A-MPDU	Aggregate MAC Protocol Data Unit
A-MSDU	Aggregate MAC Service Data Unit
APC	AM/PM Conversion
CA	Collision Avoidance
CD	Common-Drain
CG	Common-Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common-Source
CSMA	Carrier Sense Multiple Access
CW	Continuous-Wave
C/I	Carrier-to-Intermodulation
DCF	Distributed Coordination Function
DE	Drain Efficiency
DL	Downlink

DNW	Deep N-Well
DR	Dynamic Range
DSP	Digital Signal Processing
ED	Envelope Detector
EDCA	Enhanced Distributed Channel Access
EVM	Error Vector Magnitude
FOM	Figure Of Merits
FVC	Frequency-to-Voltage Converter
HBT	Heterojunction Bipolar Transistor
HCCA	HCF Controlled Channel Access
HCF	Hybrid Coordination Function
IC	Integrated Circuit
IMD	Intermodulation-Distortion
LPF	Low Pass Filter
MAC	Media Access Control
MGTR	Multi-Gate Transistors
MIMO	Multiple Input Multiple Output
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MU-MIMO	Multi-User MIMO
NAND	NOT-AND
NAV	Network Allocation Vector
NMOS	N-type Metal-Oxide-Semiconductor
NPR	Noise-Power Ratio
OBSS	Overlap Basic Service Set
OFDM	Orthogonal Frequency-Division Multiplexing

OFDMA	Orthogonal Frequency-Division Multiple Access
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PAR	Peak-to-Average Ratio
PBO	Power Back-Off
PCF	Point Coordination Function
PD	Power Detector
PDA	Personal Digital Assistant
PEP	Peak Envelope Power
PHY	Physical Layer
PM	Phase Modulation
PMOS	P-type Metal-Oxide-Semiconductor
PVT	Process, Voltage, and Temperature
QAM	Quadrature Amplitude Modulation
RAW	Restricted Access Window
RF	Radio Frequency
RTS/CTS	Request To Send / Clear To Send
SiGe	Silicon-Germanium
TSPC	True Single-Phase Clock
TWT	Target Wakeup Time
TXOP	Transmission Opportunity
UL	Uplink
WLAN	Wireless Local Area Network

Chapter 1

Introduction

1.1 Motivation

With the development of semiconductor technology, and essentially complementary metal oxide semiconductor (CMOS) technology, wireless communication systems advanced tremendously in the past two decades. Today, the ubiquitous wireless transceivers appear not only in long range communication systems such as mobile phones, base stations, and satellite networks, but in tablets, laptops, and personal digital assistants (PDAs) which equipped with short range communication systems. One of the wireless communication technology exists virtually on any user's devices is Wi-Fi, based on the IEEE 802.11 family of standards, which are commonly used for wireless local area networking (WLAN) of devices and Internet access.

The success of 802.11 standard lies on many-fold: the use of unlicensed spectrum, the reduction of cost due to economies of scale, their ease of management, and so on [8]. In the past 28 years, there is a significant in-

crease of the nominal data rates: from 2 Mbit/s IEEE 802.11-1997, to the 11 Mbit/s of 802.11b, the 54 Mbit/s of 802.11a/g, the 600 Mbit/s of 802.11n, and the above Gbit/s rates of the latest 802.11ac [7]. The increase of Wi-Fi data rates was achieved by means of more complicated modulation and coding schemes, wider channels, and the utilization of Multiple Input Multiple Output (MIMO) technologies [9]. Nevertheless, the users are becoming more demanding as the density of networks and users are increasing. Realizing the shortage of current Wi-Fi standard in high dense environment, IEEE 802.11ax was launched to solve this problem, aiming to increase the throughput-per-area.

Similar to previous improvement of the nominal data rates, 802.11ax utilize higher modulation and coding schemes, while the number of the MIMO spatial streams and the width of the channel remain the same. The key feature of 802.11ax is the adoption of orthogonal frequency-division multiple access (OFDMA), a multi-user version of the popular orthogonal frequency-division multiplexing (OFDM) digital modulation scheme. The main features of 802.11ax were summarized in Table 1.1. We can see that the new features raise more challenges on the wireless transceiver design.

A typical WLAN transceiver system diagram is shown in Fig. 1.1. Most of the radio frequency (RF) building blocks in this figure can be designed successfully in advanced complementary metal–oxide–semiconductor (CMOS)

Table 1.1: Main Features of 802.11ax [7].

	Legacy feature	New 802.11ax features
PHY		
Spectrum	up to 40 MHz at 2.4 (11n), up to 160 MHz at 5 GHz (11ac), or up to 16 MHz at 0.9 GHz (11ah)	up to 40 MHz at 2.4, up to 160 MHz at 5 GHz
OFDM Constellation Order	256-QAM (11ac)	1024-QAM
OFDM Symbol duration	3.2 us	12.8 us
OFDM Guard Interval	0.4 or 0.8 us (10 or 20% overhead)	0.8, 1.6 or 3.2 us (5, 10 or 20% overhead)
MIMO Order	4 (11n), 8(11ac)	8
Maximal Data Rate	7 Gbps	9.6 Gbps
Channel Access		
Basic channel access	CSMA/CA	OFDMA on top of CSMA/CA
Random Channel Access	DCF, EDCA	UL OFDMA Random Access on top of CSMA/CA
Contention-free Access	PCF, HCCA (not implemented in real devices), RAW (11ah)	Trigger-based UL OFDMA
MU Technology	MU-MIMO (11ac)	MU-MIMO OFDMA
MU transmission direction	DL (11ac)	DL and UL
Fragmentation	Static	Flexible
Aggregation	A-MSDU, A-MPDU (11n) without fragmentation	A-MPDU, A-MSDU with fragmentation
HE/Legacy Fairness		2 EDCA Parameter Sets
OBSS Management		
Interference Mitigation	NAV, RTC/CTS, HCCA TXOP Negotiation	Two NAVs, Quiet Period
Spatial Reuse	Sectorization (11ah)	Adaptive Power and Sensitivity Threshold, Color
Power Management		
Power Management	Many	Enhanced TWT, Enhanced Microsleep

Figure 1.1: A typical wireless transceiver system diagram.

technology. However, with the scaling of supply voltage, designing power amplifier (PA) with high output power in advanced CMOS technology became even more challenging. Techniques such as transformer stacking and power combining were proposed to solve this problem [10], [11], [12]. Besides output power, linearity of PA is a major concern in the new 802.11ax standard as it employs more spectrally efficient modulation up to 1024 quadrature amplitude modulation (QAM). Furthermore, the use of multiple sub-carriers increases the peak-to-average power ratio (PAPR) of the signal, deteriorating the signal constellation accuracy and generating spectral regrowth, which will cause the adjacent channel interference (ACI).

Traditionally, two common approaches to improve the linearity are operating in the back-off region or adding a linearization scheme. In the first approach, the amplifier output power is backed-off until the distortion level is acceptable, which results in lower efficiency. In the second approach, a

linearization scheme should be added whose design can be challenging, especially for wideband applications.

Different techniques have been proposed to overcome this challenge, which can be classified into these major categories: dynamic control of the power amplifier quiescent current, dynamic control of the load impedance, output harmonic control and dynamic supply voltage control (envelope tracking). However, each of the above techniques has its own challenges, which will be explained later in this chapter.

Radio frequency power detectors (PDs) are usually used for monitoring the transmitted power in communication systems. One way of detecting the power of the signal is using a Schottky diode as a PD, exploiting its exponential V-I relationship. However, the dynamic range and detectable power is limited to be used in more advanced system.

1.2 Objectives of the Thesis

It is well known that linearity and efficiency of the PA do not go hand-in-hand. Nonlinear or switching PAs such as Classes D and E are very efficient but cannot transmit amplitude modulation. Hence, most linear PAs use Class-A/AB amplifiers as a compromise between efficiency and linearity. Due to the inherent difficulty in the realization of a linear and efficient PA, much

work has gone into transmitter architectures that can incorporate nonlinear PAs yet transmit amplitude information.

The focus of this thesis is to design high linearity PAs with reasonable efficiency integrated wide dynamic range (DR) power detector (PD) for wireless local area network (WLAN) systems in CMOS technology. There are three contributions in my research. The first is wide DR PDs using diodes and MOSFETs as switches, the MOSFET-switch PD is going to be integrated with the proposed PA. The second is a PD with frequency compensation technique, this PD is supposed to be integrated with a wide-band PA. The third design is a linear PA design utilizing adaptive body bias technique. The first PD can also be used as an envelop detector, which is of great usage in the last PA design of this thesis.

1.3 Major Contributions of the Thesis

Firstly, a PD using diodes to overcome the limited DR and limited maximum input power problem with the aids of switched-capacitor structure and optimum biasing condition is proposed. With this structure, the diodes are working not only at the positive half-cycle as traditional diode PDs, but also at the negative half-cycle which will increase the linearity hence the dynamic range of the PD. According to the measurement results, the power detector operates from 4 GHz to 6 GHz with a dynamic range of 34 dB and ± 1 dB

error at 5 GHz. To the authors' knowledge, it is the first power detector that has achieved such wide dynamic range with input power of 35 dBm, making this work able support large input power in CMOS technology. The core of the power detector occupies an area of 0.0036 mm^2 and consumes 0.7 mW static power.

Secondly, to minimize the effect of input frequency variations on the output voltage of PD, a PD with frequency compensation technique is proposed. By adding a feed-forward frequency detection circuit, the load resistors of the power detector are changed according to the input frequencies. Thus, the effect of input frequency variation is minimized. The PD employs self-biased P-type and N-type MOSFETs as switches and utilized a balanced structure to increase the DR. Measured operation frequency of the power detector is from 3 GHz to 5 GHz with a dynamic range of 20 dB. The variations of output voltage is reduced from more than 4 dB to $\pm 0.5 \text{ dB}$, achieving a variation less than $\pm 0.25 \text{ dB/GHz}$. To the authors' knowledge, it is the first power detector with input frequency compensation which make it more suitable for wide-band applications. The core of the power detector occupies an area of 0.014 mm^2 and consumes 2.04 mW static power. This PD is supposed to be integrated with a wide-band PA.

Thirdly, an adaptive body biased linear power amplifier for IEEE 802.11ax WiFi is presented. This method is to adjust the body bias voltage of MOS-

FETs according to the input power level. To obtain the envelope of input signal, the MOSFET PD is used in the PA design. When input power is high, the body bias voltage is increased, so is the threshold voltage and vice versa. Thus, the MOSFETs will mainly work under saturation region instead of cut-off region in one period. Since signals are less distorted in saturation region than cut-off region, the linearity of MOSFET is better in one period. Thus the linearity of PA is improved without degradation of other performances of the PA. From measurement, this PA is with a saturated power of 22 dBm while the P1dB is 21 dBm with maximum efficiency of 26%.

1.4 Organization of the Thesis

The organization of this thesis is as follows.

Chapter 2 provides the background of this research. Firstly, the basic concept of RF PA circuits design in CMOS technology is introduced. Then the fundamentals of Linearity of PA are described. Finally, the methods to design linear of PAs are discussed.

In Chapter 3, the design of several PDs for modern communication systems are introduced. After reviewing literature of previous published PDs, a novel switched-capacitor structure based PD is proposed. The working principle and designing methodology are discussed with measurement re-

sults. Then, a PD with input frequency compensation circuit is proposed for the wide-band or multi-band communication applications.

In Chapter 4, the main focus is the design of adaptive body bias PA. Firstly, literature review of adaptive bias method is provided and the advantage and disadvantage of former works are discussed. Secondly, the analysis of the proposed method is discussed. Thirdly, the implementation of the proposed PA is presented. Finally, the measurement results are provided.

Chapter 5 draws the conclusion of this research and provides suggestions for future work.

Chapter 2

Background on CMOS Power Amplifiers

2.1 Fundamentals of PA

A power amplifier [10–25] is an essential element for a wireless communication system. It is used to increase the power level of a signal by using energy taken from a power supply. Linearity of transmitters is important as it suppress the interference and spectral regrowth. A typical block diagram of an RF power amplifier is shown in Fig. 2.1. It consists of input network, transistor, output network, and RF choke.

In RF power amplifiers, a transistor can be operated [13]

- as a dependent current source,
- as a switch, and
- in overdrive mode (a dependent source with partially switch mode)

Figure 2.1: A typical block diagram of an RF power amplifier.

In Fig. 2.2, a model of an RF power amplifier is shown. The transistor is operated as a dependent current source. In this case, the drain current of the MOSFET is determined by the gate-source voltage as well as the quiescent operation point of the transistor. The drain voltage of the transistor is determined by the dependent drain current together with the impedance of the loading network. The transistor in an RF power amplifier can also operate as a switch. The voltage drop on the transistor is almost zero when the switch is ON. The drain current of the transistor is mainly determined by the external circuit. When the switch is OFF, the drain current of the transistor is zero. The drain voltage of the transistor is determined by the external circuit.

If the transistor enters the triode region, it will operate as a switch and cannot operate as a dependent current source. To operate as a depen-

Figure 2.2: Model of transistor work as a dependent current source in RF power amplifiers.

dent current source, the transistor must be biased in the saturation region. For the transistor to remain in saturation region, the real time drain-source voltage v_{DS} must be higher than $V_{D,sat}$, which is the minimum allowable v_{DS} . $V_{D,sat}$ is defined by $V_{GS} - V_{TH}$, where V_{TH} is the threshold voltage of transistor. In this saturation region, the drain current i_D are almost determined by the gate-source voltage v_{GS} . Therefore, to design a linear power amplifier, it is preferable for the transistor to operate in saturation region.

The model of an RF power amplifier, in which the transistor operates as a switch, is shown in Fig. 2.3. The transistor must be in the triode region when the switch is ON and cut-off region when the switch is OFF in order for

Figure 2.3: Model of transistor work as a switch in RF power amplifiers.

the MOSFET to operate as a switch. For the transistor to remain in triode region, the real time drain-source voltage v_{DS} must be lower than $V_{D,sat}$. Operated as a switch, the drain current i_D and the drain-source voltage v_{DS} are mainly determined by external circuit. The benefits to operate transistor as switches is that the efficiency of the power amplifier will be increased, since when the switch is on, the transistor conducts current but the voltage drop on the transistor is almost zero, resulting in low power loss.

The main function of the output network are as follows[13]:

- Impedance transformation.
- Harmonic suppression.

- Filtering the spectrum.

2.1.1 Classes of Operation of RF Power Amplifier

Power amplifiers are divided into different classes (A, B, C, D, E, F, etc.) considering the conduction angles, operating mode, input and output voltage waveforms. A comparison table of different classes is shown in Table 2.1 considering power efficiency and linearity. The waveforms of output drain current i_D of a transistor versus sinusoidal gate-source voltage v_{GS} for class A, B, AB and C are shown in Fig. 2.4. Fig. 2.5 shows the quiescent operation points for various power amplifier classes.

Table 2.1: Comparison of different power amplifier classes

Class	A	AB	B	C	D	E	F
Conduction angel (%)	100	50-100	50	<50	50	50	50
Max. efficiency (%)	50	50-78.5	78.5	100	100	100	100
Linearity	Excellent	Good	Good	Poor	Poor	Poor	Poor

The conduction angel 2θ of the transistor in Class A is 360° . The real time gate-source voltage v_{GS} should be larger than the threshold voltage V_{TH} of the transistor during the entire cycle. It means the quiescent operation point of the gate-source voltage of the transistor V_{GS} must be larger than $V_{TH} + V_{gsm}$, where V_{gsm} is the amplitude of the ac component of input RF voltage signal. The quiescent operation point of the drain current I_D should

Figure 2.4: Waveforms of the drain current i_D in various classes of operation: (a) Class A, (b) Class B, (c) Class AB, and (d) Class C.

be larger than the amplitude of the ac component of the drain current I_m . In this case, the conduction angle of the transistor is 360° . The input signal of Class A amplifiers is amplified during entire cycle with almost same gain. Although the efficiency is low (lower than 50%), Class A amplifiers are linear.

The conduction angle 2θ of the transistor in Class B is 180° . The quiescent operation point of the gate-source voltage V_{GS} is equal to V_{TH} . Thus, the quiescent operation point of drain current I_D is zero. In this case, the

Figure 2.5: Operating points for Classes A, B, AB, and C.

conduction angle of the transistor is 180° . The conduction angle 2θ of the transistor in Class AB is between 180° and 360° . The quiescent operation

point of the gate-source voltage V_{GS} is a little above V_{TH} . Thus, the quiescent operation point of drain current I_D is small. Although the efficiency is low (lower than 78.5%), Class AB amplifiers are linear.

The conduction angle 2θ of the transistor in Class C is less than 180° . The quiescent operation point of the gate-source voltage V_{GS} is lower than V_{TH} , the transistor is biased in the cutoff region. Thus, the quiescent operation point of drain current I_D is zero. In this case, the conduction angle of the transistor is less than 180° . Class C amplifiers are distorted since it works at cutoff region in part of entire cycle. They are nonlinear amplifiers but have a higher efficiency.

In Class D, E, and DE power amplifiers, the transistor functions as a switch. In Class F, the transistor functions as either a switch or a dependent current source.

2.1.2 Efficiency of RF Power Amplifiers

When the resonant frequency of the output network f_o is equal to the operating frequency f , the drain power (the power delivered by the drain to the output network) is given by

$$P_{DS} = \frac{1}{2}I_m V_m = \frac{1}{2}I_m^2 R = \frac{V_m^2}{2R} \quad \text{for } f = f_o \quad (2.1)$$

where I_m is the magnitude of the first order RF component of the drain current, V_m is the magnitude of the first order RF component of the drain-

source voltage, and R is the resistance seen from the drain output of the transistor looking into the output matching network at the first order RF frequency. If the resonant frequency f_o is not equal to the operating frequency f , the drain power of the fundamental component is given by

$$P_{DS} = \frac{1}{2} I_m V_m \cos \phi = \frac{1}{2} I_m^2 R \cos \phi = \frac{V_m^2 \cos \phi}{2R} \quad (2.2)$$

where ϕ is the phase shift between the fundamental components of the drain current and the drain-source voltage reduced by π .

The instantaneous drain power dissipation is

$$p_D(\omega t) = i_D v_{DS} \quad (2.3)$$

The time-average drain power dissipation for periodic waveforms is

$$P_D = \frac{1}{2\pi} \int_0^{2\pi} p_D d(\omega t) = \frac{1}{2\pi} \int_0^{2\pi} i_D v_{DS} d(\omega t) = P_I - P_{DS} \quad (2.4)$$

The dc supply current is

$$I_I = \frac{1}{2\pi} \int_0^{2\pi} i_D d(\omega t) \quad (2.5)$$

The dc supply power is

$$P_I = V_I I_I = \frac{V_I}{2\pi} \int_0^{2\pi} i_D d(\omega t) \quad (2.6)$$

The drain efficiency at a given drain power P_{DS} is

$$\begin{aligned}\eta_D &= \frac{P_{DS}}{P_I} = \frac{P_I - P_D}{P_I} = 1 - \frac{P_D}{P_I} = 1 - \frac{\int_0^{2\pi} i_D v_{DS} d(\omega t)}{V_I \int_0^{2\pi} i_D d(\omega t)} \\ &= \frac{1}{2} \left(\frac{I_m}{I_I} \right) \left(\frac{V_m}{V_I} \right) \cos \phi\end{aligned}\quad (2.7)$$

where ϕ is the phase difference between the fundamental current and voltage. When the operating frequency is equal to the resonant frequency $f = f_0$, the drain efficiency is

$$\eta_D = \frac{P_{DS}}{P_I} = \frac{1}{2} \left(\frac{I_m}{I_I} \right) \left(\frac{V_m}{V_I} \right) \quad \text{for } f = f_0 \quad (2.8)$$

Efficiency of power amplifiers is maximized by minimizing power dissipation at a desired output power.

For amplifiers in which the transistor is operated as a dependent current source, the highest drain efficiency usually occurs at the peak envelope power (PEP). Power amplifiers with time-varying amplitude have a time-varying drain efficiency $\eta_D(t)$. These amplifiers are usually operated below the maximum output power. This situation is called power backoff. The peak-to-average power ratio (PAPR) is the ratio of the PEP of the AM waveform PEP to the average envelope power for a long time interval $P_{O(AV)}$

$$PAPR = \frac{\text{Peak Power}}{\text{Average Power}} = \frac{PEP}{P_{O(AV)}} = 10 \log \left(\frac{PEP}{P_{O(AV)}} \right) \text{ (dB)} \quad (2.9)$$

The output power delivered to a resistive load is

$$P_O = \frac{1}{2} I_{om} V_{om} = \frac{1}{2} I_{om}^2 R_L = \frac{V_{om}^2}{2R_L} \quad (2.10)$$

where I_{om} is the amplitude of the output current and V_{om} is the amplitude of the output voltage. The power loss in the resonant output network is

$$P_r = P_{DS} - P_O \quad (2.11)$$

The efficiency of the resonant output network is

$$\eta_r = \frac{P_O}{P_{DS}} \quad (2.12)$$

The overall power loss on the output side of the amplifier (in the transistor(s) and the output network) is

$$P_{Loss} = P_I - P_O = P_D + P_r \quad (2.13)$$

The efficiency of the amplifier at a specific output power is

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_{DS}} \frac{P_{DS}}{P_I} = \eta_D \eta_r \quad (2.14)$$

The gate-drive power is

$$P_G = \frac{1}{2\pi} \int_0^{2\pi} i_G v_{GS} d(\omega t) \quad (2.15)$$

For sinusoidal gate current and voltage waveforms, the gate-drive power is

$$P_G = \frac{1}{2} I_{gm} V_{gsm} \cos \phi_G = \frac{r_G I_{gm}^2}{2} \quad (2.16)$$

where I_{gm} is the amplitude of the gate current, V_{gsm} is the amplitude of the gate-source voltage, r_G is the gate resistance, and ϕ_G is the phase shift between the fundamental components of the gate current and the gate-source voltage.

The power gain of a power amplifier is given by

$$k_p = \frac{P_O}{P_G} = 10 \log \left(\frac{P_O}{P_G} \right) \text{ (dB)} \quad (2.17)$$

The power-added efficiency (PAE) is the ratio of the difference between the output power and the gate-drive power to the dc supply power

$$\begin{aligned} \eta_{PAE} &= \frac{\text{Output Power} - \text{Drive Power}}{\text{DC Supply Power}} = \frac{P_O - P_G}{P_I} = \frac{P_O}{P_I} \left(1 - \frac{P_G}{P_O} \right) \\ &= \frac{P_O}{P_I} \left(1 - \frac{1}{P_O/P_G} \right) = \frac{P_O}{P_I} \left(1 - \frac{1}{k_p} \right) = \eta \left(1 - \frac{1}{k_p} \right) \end{aligned} \quad (2.18)$$

2.1.3 Non-linear Effects in PA

The nonlinearities are often not predicted by small-signal models. These phenomena for memory less systems whose input/output characteristic can be approximated by

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad (2.19)$$

We may consider α_1 as the small signal gain of the system, and the other two terms are negligible for small input swings. The nonlinearity effects primarily arise from the third-order term in equation (2.19).

2.1.3.1 Harmonic Distortion

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. In equation (2.19), if $x(t) = A \cos \omega t$, then

$$y(t) = \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \quad (2.20)$$

$$= \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2} (1 + \cos 2\omega t) + \frac{\alpha_3 A^3}{4} (3 \cos \omega t + \cos 3\omega t) \quad (2.21)$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\omega t \quad (2.22)$$

In equation (2.22), the first term on the right-hand side is a DC quantity arising from second-order nonlinearity, the second is called the “fundamental,” the third is the second harmonic, and the fourth is the third harmonic. In many RF circuits, harmonic distortion is unimportant or an irrelevant indicator of the effect of nonlinearity. Nonetheless, harmonics must always be considered carefully before they are dismissed.

2.1.3.2 Gain Compression

The small-signal gain of circuits is usually obtained with the assumption that harmonics are negligible. However, as shown in equation (2.22), our formula of harmonics indicates that the gain of $A \cos \omega t$ at fundamental frequency is $\alpha_1 + 3\alpha_3 A^2/4$ and hence varies appreciably as A becomes larger. From

Figure 2.6: Definition of 1-dB compression point.

equation (2.19), we note that if $\alpha_1 \alpha_3 > 0$, then $\alpha_1 x + \alpha_3 x^3$ overwhelms $\alpha_2 x^2$ for large x regardless of the sign of α_2 , yielding an "expansive" characteristic. On the other hand, if $\alpha_1 \alpha_3 < 0$, the term $\alpha_3 x^3$ "bends" the characteristic for sufficiently large x , leading to "compressive" behavior, a decreasing gain as the input amplitude increases. Most RF circuits of interest are compressive.

With $\alpha_1 \alpha_3 < 0$, the gain experienced by $A \cos \omega t$ in equation (2.22) falls as A rises. This effect is quantified by the "1-dB compression point," defined as the input signal level that causes the gain to drop by 1 dB. Fig. 2.6 shows as a function of input power, the output power P_{out} , falls below its ideal value by 1 dB at the 1-dB compression point, $P_{\text{in},1\text{dB}}$. 1-dB compression point may also be specified in terms of the output power level at which it occurs, $P_{\text{out},1\text{dB}}$.

Figure 2.7: Cross modulation.

2.1.3.3 Cross Modulation

If a weak signal and a strong interferer signal pass through a nonlinear system, the interferer will be modulated over the signal. This phenomenon is called "cross modulation" and is explained by the equation (2.23):

$$y(t) = \left[\alpha_1 + \frac{3}{2} \alpha_3 A_2^2 \left(1 + \frac{m^2}{2} + \frac{m^2}{2} \cos 2\omega_m t + 2m \cos \omega_m t \right) \right] A_1 \cos \omega_1 t + \dots (2.23)$$

This effect is illustrated by Fig. 2.7.

2.1.3.4 Intermodulation

If two signals at ω_1 and ω_2 are applied to a nonlinear system, the output signals are from the mixing of the two components. Assume $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, applied to equation (2.19), we could obtain the following intermodulation(IM) products:

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos \omega_2 (2\omega_1 - \omega_2)t (2.24)$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos \omega_2 (2\omega_2 - \omega_1)t (2.25)$$

The IM characterization is indicated by a "two tone" test, two equal amplitude pure sinusoidal signals are applied to the input. Then the ratio of the

Figure 2.8: Definition of IP_3 .

output IM products to the fundamentals and the input power level is tuned. The results is called the third intercept point (IP_3).

$$\text{RelativeIM} = 20\log\left(\frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2\right) \text{ dBc} \quad (2.26)$$

As the amplitude of input signal rises, the output IM products increase more sharply. The amplitude of the IM products eventually becomes equal to the input signals. This is illustrated in Fig. 2.8. The input level at which this occurs is called the input third intercept point (IIP_3). The one corresponding output is called OIP_3 .

2.1.3.5 AM/PM Conversion

AM/PM conversion (APC) is the phenomenon that the phase shift is depended on the signal amplitude. For an input $V_{in}(t) = V_1 \cos \omega_1 t$, the fundamental output component is shown by

$$V_{out}(t) = V_2 \cos[\omega_1 t + \phi(V_1)] \quad (2.27)$$

where $\phi(V_1)$ denotes the amplitude-dependent phase shift. This phenomenon is mainly caused by the non-linearity of capacitors in the circuit.

2.1.3.6 Memory Effect

Electrical systems can be classified into four main categories as listed in Table 2.2: linear and nonlinear system with or without memory. An energy storage element such as a linear capacitance causes memory. Nonlinear effects in electrical systems are caused by one or more nonlinear elements. Memory effects introduce a phase shift between the input and the output.

Table 2.2: Classification of electrical systems

	Memoryless	With Memory
Linear	Linear resistance	Linear capacitance
Nonlinear	Nonlinear resistance	Nonlinear capacitance or nonlinear resistance and linear capacitance

2.2 State-of-the-Art PA Linearization Technique

Linear amplification is required when the signal contains both amplitude and phase modulation. Linearity is characterized, measured, and specified by various techniques, depending upon the specific signal and application.

The carrier-to-intermodulation (C/I) ratio, compares the amplitude of the desired output carriers to the intermodulation-distortion (IMD) products. Noise-power ratio (NPR) is the ratio of the notch power to the total signal power when a PA is driven by noise with a spectral notch. Adjacent channel power ratio (ACPR) compares the power in an adjacent channel to that of the signal. It is currently the most widely used parameter to measure the linearity of a system, but defined differently for each application. Error vector magnitude (EVM) is the distance between the desired and actual signal vectors.

Nowadays, tight EVM specification and over 10dB peak to average ratio (PAR) of OFDM signal require extremely high linearity over a broad power range. The former mentioned linearization techniques at system level always come with complex circuits and are doubted whether they work with signals with larger band width. For this reason, a classical PA biased at Class AB mode is usually utilized and there are some simple linearization techniques that work well for Class AB PA.

2.2.1 Harmonic Circuitry to Enhance Linearity

In this work[1], to improve the linearity, several harmonic traps are introduced to minimize the second- and third-order harmonics, and hence, the third-order intermodulation distortion. A highly linear fully integrated RF power amplifier for advanced long-term evolution is fabricated in a 180-nm

standard silicon-on-insulator process. The impact on the linearity of the RF PA of each of the harmonic controls is studied. The schematic of the RF PA with harmonic traps is shown in Fig. 2.9.

Figure 2.9: Simplified schematic of the RF PA with harmonic traps[1].

The gate of this amplifier is biased a little more than the threshold voltage, so the PA works in deep Class AB mode. Working in this mode has several benefits: it will have a maximally flat gain and will extend the P_{1dB} almost until the saturated output power [26].

The Adjacent channel leakage ration (ACLR) linearity performance of the RF PA is certainly affected by the third- and fifth-order intermodulation components[27]. In [28], it was shown that ACLR relates to third-order intermodulation distortion(IMD3) calculating an ACLR for n subcarriers using a two-tone signal as

$$ACLR_n = IMD3 + c_n \quad (2.28)$$

where c_n is a correction factor depending on the amount of subcarriers n in the applied signal [29].

The IMD3 components are created due to the nonlinear gate-source capacitance, an outphased second harmonic component is superposed on the in-phase gate voltage[30]. And the effect of this nonlinear gate-source capacitance can be minimized by introducing a second-order harmonic short[31], [32], [3], [33]. The second-order harmonic short is formed by a series L-C[34]. The Values for both L and C are chosen as such that simultaneously a high impedance for the third harmonic component is realized [34]. Several second harmonic traps are introduced at the center tap of the input matching transformer and the gates of the common source and common gate transistors. Thus, the even harmonics trapped at the common nodes in a differential PA are significantly reduced. The reduced distortion at the gate directly improve the voltage waveform at the drain of PA, showing much less second-order harmonics at the drain. From measurement results, it shows that introducing the traps at the bias lines and center tap also reduces the difference between upper and lower intermodulation distortion.

2.2.2 Adaptive gate bias control technique

Adjusting the gate bias is one of the efficient methods because the performances of the PAs are strongly depend on the gate bias [1, 2, 35–40].

The PAs biased at a deep Class-AB operation are the most optimized condition for linearity and efficiency [41]. However, biased near the threshold voltage region, the PA tend to generate large inter-modulation distortion (IMD) when the input power is in low and mid range. In this bias condition, the gain of the amplifier expanded as the increase of the input power, which degrades the AM-AM [30, 42] performance. The gate adaptive bias circuit of the common-gate (CG) amplifier is proposed to improve linearity and to suppress AM-AM distortion in [2]. Besides, it is proved that in a common-source (CS) amplifier, injecting the envelope signal through a bias circuit to the gate reduces the IMD components at a high power region by canceling the distortions [43–47].

It is reported that the linearity of the PAs is improved by combining both adaptive bias circuits at the gates of the CS and the CG stages in [2]. The memory effects that are generated by the bias circuits are reduced using second harmonic control circuits at the source of the CS and the gate of the CG stages. The block diagram of the adaptive gate biasing PA is shown in Fig. 2.10.

This linearization technique uses the adaptive gate bias circuits along with the second harmonic short circuits together in a PA. The envelope signal is injected into the gate of the CS stage of PA through bias circuit. It is properly designed that the injected signal will cancel the distortions in the

Figure 2.10: Block diagram of the adaptive gate biasing PA[2].

PA when the input power is high. Thus, the IMD3 performance is improved. The CS stage is biased in a deep Class-AB condition. It is also said that the optimized gate bias of the CG stage will suppress the sideband asymmetry.

Another benefit is combining a gain-expansion stage (deep Class-AB) and a gain compression stage (Class A) compensate the AM-AM distortion through reduction of the gain deviation. Multi-gate transistors (MGTRs) method utilize this characteristic of Class B (or deep Class-AB) and Class A to compensate each other's gain nonlinearity [48–50].

These previous works demonstrated that highly efficient and linear PAs using adaptive bias control method. The main idea is that when a high voltage envelope signal is input to the PA, the gate bias is increased from low to high to improve the linearity at the expense of more current consumption. However, adaptive gate biasing also change the trans-conductance of the MOSFET, introducing other non-linear factors.

2.2.3 Nonlinear input capacitance compensation technique

The non-linear input capacitance is one of the main source of non-linear effect in PAs. Several methods are reported to compensate the non-linear input capacitance.

In [3], a PMOS device is placed alongside the NMOS device that works as the amplifying unit, such that the overall capacitance seen at the amplifier input is a constant, thus improving linearity. The simplified schematics of Class-AB amplifiers used to illustrate the impact of the gate-source capacitance on linearity is shown in Fig. 2.11.

Figure 2.11: Linearized Class-AB amplifiers using capacitance-compensation technique[3].

However, this method increase the input capacitance of the PA. Besides, the PMOS is not used as a gain stage.

stage compensate each other, reducing the distortion caused by input capacitance variations.

In this method, the gain of common-drain stage is quite low. Besides, using the PMOS instead of NMOS as the gain stage also reduces the gain of PA, degrading the efficiency.

2.3 Summary

In this chapter, we review the PA and non-linearity fundamentals and showed three basic and three state-of-the-art linearization techniques. Harmonic circuitry, adaptive gate bias, and nonlinear input capacitance compensation techniques are discussed and reviewed. The advantages and disadvantages of these three methods are analyzed.

Chapter 3

Design of Switched Capacitor Power Detector

3.1 Introduction

In a radio frequency (RF) integrated circuit (IC) system, power control is essential for power amplifier to maintain reliable communications and extend battery life in mobile devices. In transmitter systems, power detector is usually used to adjust transmission power, increasing the capacity and quality of the network. Since modern systems have a large peak to average power ratio, the output power of PA varies dramatically which demand the investigation of power detector with wide dynamic range.

Several techniques are introduced to increase the dynamic range (DR) and bandwidth of the power detector (PD) [51–53]. A PD consists of heterojunction bipolar transistors (HBTs) in cascode configuration with diode connected P-type metal-oxide-semiconductor (PMOS) load in a SiGe BiCMOS technology is reported in [51]. The cascode configuration is used to

provide wide-band input matching independent of input power level. The DR of the PD is improved by implementing diode connected PMOS load to reduce the load impedance for high DC currents. However, the linearity of this PD is not good enough, so the high dynamic range is realized by increasing the error of the detected power. Cascading gain amplifiers and squaring circuits are utilized to achieve wide DR using the power level segmented detection method in [52]. The frequency response is enhanced by gain amplifiers with a cross-coupled NMOS structure. The power level is divided into several segments and each segment is detected separately. In [53], a capacitor attenuation array and seven-stage CMOS rectifiers are utilized. The attenuation capacitors reduce the input signal into segments, each signal from these segments is rectified so the PD can detect input power precisely. Auxiliary capacitors are introduced to improve the DR by making the rectifier maintain the transfer characteristic at saturation region. However, these circuits are complicated and difficult to realize. Although the DR is increased but the minimum detectable power is too large to be used in wireless communication applications. Besides, the use of PD in wideband frequency system is troublesome because of the output voltage is affected by the input frequencies. So an input frequency compensated PD is need for multi-band applications.

3.2 Design of Diode Switched-Capacitor Power Detector

In this thesis we propose a PD using diodes and overcome the limited DR problem with the aids of switched-capacitor structure. The proposed power detector realizes logarithmic transfer function utilizing the exponential relationship between the applied voltage and current of diodes. The proposed power detector is designed using junction diodes in 65-nm CMOS process. It shows more than 30dB dynamic range and consumes very small area and 0.7mW static power which make it suitable to be integrated on chip in mobile devices.

3.2.1 Analysis of the Proposed Design

The proposed switched-capacitor PD is shown in Fig. 3.1. It consists of four diodes working as switches, two input capacitors to block DC signals, one load resistor, and one output filter network to filter out high frequency components. In the proposed power detector, although the diodes work as switches and the structure is similar to a switched-capacitor circuit, its operation is different from the traditional switched-capacitor circuit because the capacitors in our circuit are more like DC-blockers.

The supply of the power detector is at a voltage such that it provides the PN junctions of the four diodes are biased just below the threshold volt-

Figure 3.1: Block diagram of the proposed power detector.

age. There are two benefits in this biasing condition. Firstly, since the bias voltage is below the threshold voltage, the electrons cannot flow through the depletion region so that the static current and the power consumption is low. Secondly, with a small increase of input voltage, the currents of the diodes are changed dramatically, which will improve the sensitivity of the power detector.

The working principle of the proposed power detector is shown in Fig. 3.2 and Fig. 3.3. When biased properly, if the differential RF input signals are positive at $Port_1$ and negative at $Port_2$, as shown in Fig. 3.2, the switch SW_2 and SW_3 are closed, while the switch SW_1 and SW_4 are open. Thus, the capacitor C_1 is discharged through the load resistance and C_2 is charged

by the supply voltage. If the differential input RF signals are negative at $Port_1$ and positive at $Port_2$, as shown in Fig. 3.3, the switch SW_1 and SW_4 are closed, while the switch SW_2 and SW_3 are open. Thus, the capacitor C_1 is charged by the supply voltage and C_2 is discharged through the load resistance. The charging and discharging currents depend on the average voltage drop across the diode in one cycle. In the positive cycle, suppose the voltage swing of the input signal is Δv , then the current of the diode SW_3 is:

$$i_{diode} = I_S \left(e^{\frac{V+\Delta v}{nV_T}} - 1 \right) \quad (3.1)$$

where I is the diode current, I_S is the reverse bias saturation current, V is the bias voltage of the diode, V_T is the thermal voltage and n is the ideality factor of the diode.

When the input power is increased, the average voltage swing across the diode in one cycle is increased and the average current is also increased. Then the voltage drop on the load resistor becomes higher in one cycle. With the low pass filter to filter out the high frequency components, when the input power is fixed, a steady output voltage can be obtained. Then the relationship between the output DC voltages and the input powers is established. The proposed power detector differs from traditional PD with a single Schottky diode or a half bridge. For conventional PD [54], the swing

Figure 3.2: Positive cycle of the proposed diode power detector.

of RF signal should be larger than the threshold voltage of the diode for the PD to work, which will decrease the sensitivity of the PD. In contrast, in the proposed balanced switched-capacitor structure, since the diode is biased just below the threshold voltage, a small swing of signal will turn on or off the switches, improving the sensitivity of the PD. So the balanced switched-capacitor structure and the optimum biasing condition together realize the wide dynamic range of the PD.

In practice, the diode used in this design is the PN junction diode instead of diode-connected MOSFET because the current and applied voltage relationship of MOSFET diode is not linear when the voltage goes as high as

Figure 3.3: Negative cycle of the proposed diode power detector.

Figure 3.4: PD performance with different diode areas.

Figure 3.5: PD performance with different load resistance.

Figure 3.6: PD performance with different supply voltages.

6 V. Thus, the output of MOSFET PD is not linear when the applied power is too high. To enhance the ability of the power detector working at high input power, the area of diode should be increased, which allows higher current to flow through the diode. However, the diode resistance is different in small and large signals. When the signal is small, the voltage divider on each branch is sub-threshold resistance and switch-on resistance; when the signal is large, the voltage divider on each branch is switch-off resistance and switch-on resistance. Since the diode with larger area has lower sub-threshold resistance, in this case, the voltage divider in small and large signals are different, which will decrease the linearity of the PD. Simulated output voltages of PDs using different diode areas are shown in Fig. 3.4. It is shown that the diode with smaller area tends to have better linearity. However, diode with smaller area is easily damaged when the input power is high. Considering the current density of the diode, the area of the diode is designed to be $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$ for optimum working performance in this design. With appropriate load resistance and supply voltage, the diodes in this circuit are biased just below the threshold voltage, so that a small input signal will switch the nearly conducted diodes on or off, increasing the sensitivity of the circuit. The load resistance affects the performance of the PD by changing the bias condition of the switches. Simulation results of the PD performance with different load resistances are shown in Fig. 3.5. Changing

the load resistance will shift the output voltage higher or lower as shown in the figure. In this design, the load resistance is chosen to be $100\ \Omega$, which is the load with the most linear performance. Simulation results of the PD performance with different supply voltages are shown in Fig. 3.6. Detection of power above 10 dBm is not much affected with different supply voltages, but the detection of power below 10 dBm varies much with supply voltages. The supply voltage is 1.8V in this design to obtain the highest dynamic range. It can be supplied from DC-DC, LDO or bandgap circuits in real applications. The minimum available size of capacitor in the 65-nm CMOS process is used as the DC-blocking capacitor. This will enhance the sensitivity and provide high input impedance of the power detector to minimize the loading effect when it is connected to other circuits.

3.2.2 Measurement Results

The proposed power detector was implemented in GlobalFoundries 65-nm CMOS process. The die micrograph of the fabricated power detector is shown in Fig. 3.7. The chip area is $540\ \mu\text{m} \times 410\ \mu\text{m}$, which is mainly consumed by the pads for measurement. The area of the power detector is only $60\ \mu\text{m} \times 60\ \mu\text{m}$, including the input DC blocking capacitors and the low pass filter. The switched-capacitor power detector consumes 0.39 mA from a 1.8 V supply voltage. The power detector is measured on-wafer using

Figure 3.7: Micrograph of the proposed power detector.

Figure 3.8: Measurement setup of the proposed power detector.

Figure 3.9: Simulated and Measured output voltage of the proposed power detector.

Figure 3.10: Measured error of the proposed power detector.

Cascade Elite 300 probe station at room temperature. The measurement setup is shown in Fig. 3.8. The continuous-wave (CW) signal is provided by an R&S SMF 100A signal generator. The CW signal is amplified by two cascaded amplifiers, then converted to differential signals using a 180-degree hybrid coupler. In order to obtain accurate measurement results, the effects of test setup should be removed from measurement data. Before the measurement of the PD, the output of the hybrid coupler is connected to an attenuator and then to a Keysight power meter to de-embed the non-linearity of the two amplifiers and the loss of the hybrid coupler and coaxial cables at different input powers. The losses of the RF probes are also de-embedded using the S-parameters provided by CASCADE. Thus, when measuring the PD, the accurate input power can be calculated. The output voltage of the PD is measured by a Keysight 34401A multimeter.

Fig. 3.9 and 3.10 show the output voltages and errors versus input power at different frequencies. The proposed power detector has an operation frequency range from 4 GHz to 6 GHz. The measurement results indicate that the power detector has more than 30 dB, 34 dB and 31.5 dB dynamic range with ± 1 dB error at 4 GHz, 5 GHz and 6 GHz, respectively. The maximum input power is 35 dBm. Compared with other PDs (Table 3.1), our design advances with large input power, high dynamic range, and a compact area.

Table 3.1: Comparisons with Other Wide DR Power Detectors

Reference	Dynamic Range (dB)	Error (dB)	Operating Frequency (GHz)	Power Consumption (mW)	Measured Max Input Power (dBm)	Active Area ($\mu\text{m} \times \mu\text{m}$)	Process
[52]	>40	± 0.8	0.7-4	5.8	<10	150000	28-nm CMOS
[55]	43	± 1	2-14	35.2	<20	1750000	130-nm CMOS
[56]	40	± 1	0-20	-	10	385000	180-nm BiCMOS
[51]	52	-	7-20	7.2	<10	420000	250-nm BiCMOS
[57]	29	± 1	1.8	16	0	479400	180-nm CMOS
[58]	40	± 1	0.9-8	70	<5	980000	180-nm CMOS
[59]	21	± 1	0.5-20	0.12	<10	85000	130-nm CMOS
[60]	20	± 0.5	0.125-8.5	0.18	-5	12600	130-nm CMOS
[61]	20	± 2.4	3.1-10.6	3.8	-5	360000	180-nm CMOS
[62]	25	-	60	0.06	<5	6400	65-nm CMOS
Diode PD	30(@4GHz) 34(@5GHz) 31.5(@6GHz)	± 1	4-6	0.7	35	3600	65-nm CMOS

3.2.3 Variation of the Proposed Design

Although the dynamic range is large for the diode based power detector, the minimum detectable power is not small enough for its implementation on CMOS PAs. So the MOSFET based switched-capacitor power detector is proposed for lower power applications.

Figure 3.11: Block diagram of the proposed MOSFET power detector.

The working principle of the MOSFET power detector is the same as the diode counterpart, as shown in Fig. 3.2 and Fig. 3.3. The schematic of the proposed power detector is shown in Fig. 3.11. The difference between the diode version and MOSFET version is that two resistors are added for self-bias of the PMOS and NMOS. When the input power level is high, as the swing of the input power is large, the PMOS is opened and NMOS is closed. When the input power is low, as the swing of the input power is small, The NMOS is opened and PMOS is closed. Thus the PMOS and NMOS act as switches as the input is sinusoidal signal.

There are two major benefits of the MOSFET version. Firstly, the power supply could be much lower than the diode version. This will reduce the

Figure 3.12: Simulated and Measured output voltage of the proposed MOSFET power detector.

power consumption. Secondly, it is more sensitive to small signal compared to the diode PD. In the diode, if the swing is low, it will change the current of the diode, but the change is not as significant as the MOSFET since the MOSFET will work in two different regions, the saturation region and the cut-off region. That means the MOSFET PD is more sensitive to the amplitude of the input signal.

The proposed MOSFET power detector is implemented in GlobalFoundries 65-nm CMOS process. The chip area is $540\mu\text{m} \times 410\mu\text{m}$ including pads. The area is mainly consumed to place the pads for measurement. The switched-capacitor power detector consumes 0.12 mA from a 1.2 V supply

Figure 3.13: Measured error of the proposed MOSFET power detector.

voltage. The power detector is measured on-wafer using Cascade Elite 300 probe station at room temperature. The measurement setup is the same as the diode PD, shown in Fig. 3.8.

Fig. 3.12 and 3.13 show the output voltages and errors versus input power at different frequency. The difference between simulation and measurement results are mainly because of the parasitic capacitance in the circuit. The proposed power detector has wide dynamic range from 4-6 GHz. The measurement results indicate that the power detector has more than 35.8 dB, 34.8 dB and 32.7 dB dynamic range with ± 1 dB error at 4 GHz, 5 GHz and 6 GHz, respectively. Comparison with other PD is shown in Table 3.2.

Table 3.2: Comparisons with Other Wide DR Power Detectors

Reference	Dynamic Range (dB)	Error (dB)	Operating Frequency (GHz)	Power Consumption (mW)	Measured Max Input Power (dBm)	Active Area ($\mu\text{m} \times \mu\text{m}$)	Process
[52]	>40	± 0.8	0.7-4	5.8	<10	150000	28-nm CMOS
[55]	43	± 1	2-14	35.2	<20	1750000	130-nm CMOS
[56]	40	± 1	0-20	-	10	385000	180-nm BiCMOS
[51]	52	-	7-20	7.2	<10	420000	250-nm BiCMOS
[57]	29	± 1	1.8	16	0	479400	180-nm CMOS
[58]	40	± 1	0.9-8	70	<5	980000	180-nm CMOS
[59]	21	± 1	0.5-20	0.12	<10	85000	130-nm CMOS
[60]	20	± 0.5	0.125-8.5	0.18	-5	12600	130-nm CMOS
[61]	20	± 2.4	3.1-10.6	3.8	-5	360000	180-nm CMOS
[62]	25	-	60	0.06	<5	6400	65-nm CMOS
Diode PD	30(@4GHz) 34(@5GHz) 31.5(@6GHz)	± 1	4-6	0.7	35	3600	65-nm CMOS
MOSFET PD	35.8(@4GHz) 34.8(@5GHz) 32.7(@6GHz)	± 1	4-6	0.144	21.5	720	65-nm CMOS

3.3 Design of Power Detector with Frequency Compensation

3.3.1 Design of Power Detector

Supporting multi-band is a trend in modern communication systems. However, for different frequency bands, the outputs of PD varies with input fre-

quencies. This variation can be up to several dB, which requires calibration on these frequencies, making the measurement of input powers difficult. To solve this problem, the frequency compensation technique is required. Besides, since modern systems have a large peak-to-average power ratio, this demand the investigation of power detector with wide dynamic range. Also, the power detector should have a compact size and low power consumption to be integrated in the whole system.

Figure 3.14: Block diagram of the proposed frequency compensated power detector.

The proposed power detecting circuit is shown in Fig. 3.14. It consists of two N-type and two P-type MOSFETs, two input capacitors as DC blockers, two feedback resistors for self-biasing of the MOSFETs, a variant load

resistor controlled by digital signals, and a second order RC low-pass filter network to obtain the output DC voltage.

The structure of the proposed power detector is similar to the one published in [63], replacing the diodes used in [63] with self-biased MOSFETs. There are two reasons that the self-biased MOSFET is preferred to diode switch in this design. Firstly, since the PN-junction diode has a higher threshold voltage, the power supply could be much lower using MOSFET switches. This will reduce the power consumption. Secondly, the self-biased MOSFET is more sensitive to small signals compared to the diode. This may be due to the I_{ds} - V_{gs} curve of the MOSFET has a sudden change of slope from the cut-off region to the saturation region when the V_{gs} increases gradually. However, for diode device, the slope of I-V curve changes gradually. Therefore, for the same voltage increase, the MOSFET will conduct more current than the diode.

In this structure, the four MOSFETs work as four switches. With proper supply voltage, the N-type and P-type MOSFETs are just biased below the saturation region. When a positive cycle RF input signal is applied to the $Port_1$, the N-type MOSFET M_{n1} is closed, while the P-type MOSFET M_{p1} is open. At the same time, a negative cycle input signal is applied to the $Port_2$, the P-type MOSFET M_{p2} is closed, while the N-type MOSFET M_{n2} is open. The capacitor C_1 is discharged through the load resistance and

C_2 is charged by the supply voltage. When a negative cycle input signal is applied to the $Port_1$ and a positive cycle signal is applied to the $Port_2$, switch M_{p1} and M_{n2} are closed, while the switch M_{p2} and M_{n1} are open. Then the capacitor C_1 is charged by the supply voltage and C_2 is discharged through the load resistance. The charging and discharging currents depend on the average voltages applied on terminals of the MOSFETs in one cycle.

Figure 3.15: Schematic of the clock generator of the proposed power detector.

3.3.2 Design of Frequency Detection Circuit

As shown in Fig. 3.14, the frequency detection circuit is composed of an inverter chain, two true single-phase clock (TSPC) dividers, a clock generator, a frequency-to-voltage converter (FVC) and a 2-bit analog-to-digital converter (ADC). The inverter chain is used to amplify the input signal and to convert the input sinusoidal signal to a square wave signal. If the input

Figure 3.16: Schematic of the FVC of the proposed power detector.

Figure 3.17: Control signals of the clock generator.

Figure 3.18: Output voltage versus input frequency of FVC.

signal is large, the inverter chain works as a limiter to protect the following stage. Two series TSPC dividers are utilized to divide the input frequency by 4 to generate the clock for the next stage. Dividing the frequency of the input signal by 4 allows the FVC works at higher frequency.

The schematic of the clock generator and FVC are shown in Fig. 3.15 and Fig. 3.16. The working principles of these two circuits are similar to the work published in [64]. The clock generator provides three control signals S_1 , S_2 , and S_3 , controlling transistors of M_1 , M_2 , and M_3 as shown in Fig. 3.16. The input and output signals of the clock generator are presented in Fig. 3.17. It is composed of a D flip-flop, a non-overlapping circuit, two NANDs, and eleven inverters. The input frequency is divided by two to

generate the signal S_1 . With the non-overlapping circuit and NANDs, we can obtain two non-overlapping signals S_2 and S_3 whose frequency is half of the input signal.

These three control signals are with the same frequency. The general operation of the FVC is to charge capacitors C_3 and C_4 by the current mirror when signal S_3 is high. The capacitor C_3 is discharged when signal S_2 is high. The charge in C_4 is held constant to provide an output voltage corresponding to the frequency of the control signals. In the negative period T_1 of signal S_1 , all transistors M_1 , M_2 , and M_3 are turned OFF and the charge in C_4 is held constant. During the positive period T_2 of signal S_1 , transistor M_1 is turned ON. In this period, when signal S_2 is at a low voltage level and S_3 is high, capacitors C_3 and C_4 are charged by the current mirror. There is a charge redistribution in capacitors C_3 and C_4 at the beginning of this period when the charge of these two capacitors are not same. Once the charge of these two capacitors are the same, the redistribution procedure stops. When signal S_2 is at a high voltage level and S_3 is low, capacitor C_3 will be discharged and the voltage of C_4 is held constant. Since $C_3 = C_4 = C$. If the input frequency of the PD and the clock generator is f_{in} and f_{cg} , then the frequency of the signal S_3 is $f_{cg}/2=f_{in}/8$. We have:

$$V_{out} = \frac{I_c}{2C} T_4 = \frac{I_c}{2C} \left(\frac{2}{f_{cg}} \right) = \frac{I_c}{2C} \left(\frac{8}{f_{in}} \right) \quad (3.2)$$

Figure 3.19: Simulation results of output voltages with different input frequencies for uncompensated PD.

So the output voltage of the FVC is reversely proportional to the input frequency. The charging and discharging procedure of this FVC is different from the one published in [64]. In [64], capacitor C_3 is charged firstly and then the charge of C_3 and C_4 are redistributed which makes the whole procedure slower. In the proposed FVC, the redistribution procedure is accelerated by injecting the current of the current mirror at the same time. So the working frequency of this FVC is higher and the time for the FVC to reach a steady state is faster. The output voltage versus input frequency of the FVC is shown in Fig. 3.18.

To compensate the variation of input frequencies, output voltage versus

Figure 3.20: Simulation results of output voltages with different load resistances for uncompensated PD.

Figure 3.21: Schematic of the load resistor of the proposed power detector.

input power relationship with different input frequencies in an uncompensated PD are shown in Fig. 3.19. In this figure, simulation results of the PD working at 2 GHz-9 GHz are shown, so a clearer trend of output voltage variation while increasing input frequency can be observed. From the

Figure 3.22: Micrograph of the proposed power detector.

Figure 3.23: Measurement setup of the proposed power detector.

simulated results, we can see that with the increase of input frequency, the output voltages of PD also increase with the same input power. This is because with the frequency of the MOSFET switches turning ON and OFF increased, the charging and discharging frequency also increase, resulting in a higher output voltage. So to eliminate the effect of this charging current increase, we could reduce the load resistance instead. Simulation results

Figure 3.24: Measured performance of the PD without frequency compensation.

Figure 3.25: Measured performance of the PD with frequency compensation.

Figure 3.26: Measured error of the PD with frequency compensation.

for an uncompensated PD are shown in Fig. 3.20 that with a higher load resistance, the output voltage also increases. If we can reduce the load resistance while increasing the input frequency, the voltage-power curve may remain the same with different input frequencies.

To verify this idea, the output voltage of the FVC is digitized by a 2-bit ADC firstly in this design. For simplicity, the architecture of the ADC is a basic flash ADC using a resistor-constructed voltage ladder and comparators. The resistors in the ADC are tuned to be non-linear for the best performance. The output digital signals control the switches to short resistors as shown in Fig. 3.21. With higher frequency, more resistors are shorted to ground, reducing the load resistance of the power detector. The resolution of the ADC can be increased if higher accuracy is needed. With proper

Table 3.3: Comparisons with Previous wideband Power Detectors

Reference	Frequency Compensation	Variation of Output Voltage (dB/GHz)	Dynamic Range (dB)	Operating Frequency (GHz)	Power Consumption (mW)	Active Area (mm ²)	Process
[51]	NO	-	52	7-20	7.2	0.42	250-nm BiCMOS
[52]	NO	-	>40	0.7-4	5.8	0.15	28-nm CMOS
[53]	NO	-	42	0.3-10	0.55	0.113	180-nm CMOS
[63]	NO	<1.5 ^a	>30	4-6	0.7	0.0036	65-nm CMOS
[55]	NO	-	43	2-14	35.2	1.75	130-nm CMOS
[56]	NO	-	40	0-20	-	0.385	180-nm BiCMOS
[58]	NO	-	40	0.9-8	70	0.98	180-nm CMOS
[59]	NO	-	21	0.5-20	0.12	0.085	130-nm CMOS
[60]	NO	-	20	0.125-8.5	0.18	0.0126	130-nm CMOS
[61]	NO	-	20	3.1-10.6	3.8	0.36	180-nm CMOS
This work	YES	<0.25	20	3-5	2.04	0.014	65-nm CMOS

^aEstimated from measurement results.

load resistance, we can obtain the same performance of the PD for different input frequencies. In this PD, the load resistance is designed to be 800 Ω , 600 Ω , 550 Ω , 500 Ω , and 450 Ω for 2 GHz, 3 GHz, 4 GHz, 5 GHz, and 6 GHz respectively.

3.3.3 Measurement Results

The proposed frequency compensated power detector has been designed and fabricated in GlobalFoundries 65-nm CMOS process. Fig. 3.22 shows

the micrograph of the fabricated chip. The chip area is $580\text{ }\mu\text{m} \times 255\text{ }\mu\text{m}$ including the pads for measurement. The area of the power detector is only $200\text{ }\mu\text{m} \times 70\text{ }\mu\text{m}$. With a 1.2 V supply voltage, the current consumption of the switched-capacitor power detector is 1.7 mA. Cascade Elite 300 probe station is used to measure the power detector as shown in Fig. 3.23. Keysight E8257D signal generator providing continuous-wave (CW) signal is first connected to an amplifier and a hybrid coupler to convert to the single-ended signal to the differential. Then differential signals are applied to the input of the power detector. To de-embed the effect of the amplifier and coupler, before the measurement of the PD, the gain of the amplifier and the loss of the hybrid coupler and coaxial cables are measured at target frequencies. So after measurement of the PD, the actual input power of the PD can be calculated to obtain accurate measurement results. The losses of the RF probes are also de-embedded using the S-parameters provided by Cascade. Keysight 34401A multimeter is used to measure the output voltage of the PD.

Fig. 3.24 and Fig. 3.25 show the output voltages and maximum voltage difference versus input power at different frequencies with and without frequency compensation. In this design, since the resolution of ADC is only 2-bit, five different load resistance values can be obtained by changing the output voltage of the FVC. In the measurement results, two of the five load

resistances didn't compensate input frequency well. Therefore, only three frequency points which are well compensated are shown in Fig. 3.24 and Fig. 3.25. There are two reasons that two of the five load resistances were not able to compensate the input frequency. One of the reasons is due to the parasitic of circuit, another one is the load resistance step is not calculated to compensate the input frequency well enough. The maximum voltage difference is calculated by the output voltage difference of PD in a frequency range from 3 GHz to 5 GHz at the same input power. It is shown that with the frequency compensation circuit, the PD output voltage is more consistent at various input frequencies. However, with the frequency compensation circuit, the lowest detectable power is increased, and the dynamic range is also decreased. A possible reason is due to the increased parasitic and the loading effect of the frequency compensation circuit. The proposed frequency compensated power detector has an operating frequency range from 3 GHz to 5 GHz. The variations of the output voltage are reduced from more than 4 dB to ± 0.5 dB. The measurement results indicate that the power detector has more than 20 dB dynamic range. The error of the frequency compensated PD is within ± 2 dB as shown in Fig. 3.26. Compared with previous published PDs (Table 3.3), this PD features at frequency compensation technique with low power consumption, a compact area, and a reasonable DR.

3.4 Summary

In this chapter, firstly, we have demonstrated a high dynamic range, high input power, low power consumption diode power detector with an area of 0.0036 mm^2 using 65-nm CMOS process. The measurement results show that with a static power consumption of 0.7 mW, the dynamic range is more than 30 dB in the frequency range of 4-6 GHz with ± 1 dB error. The maximum input power is 35 dBm, which is the highest input power to the authors' knowledge. We also demonstrated a self-biased MOSFET version of the PD. By replacing the diode with self-biased MOSFET, the minimum detectable power is lower. The measured dynamic range is more than 32.5 dB in the frequency range from 4-6 GHz. The static power consumption is 0.144 mW.

Secondly, we have verified the idea of output voltage variation due to the input frequency can be compensated by changing the load resistance of the PD. The proposed PD is designed with an input frequency compensated, low power consumption, reasonable DR PD, an area of 0.014 mm^2 in a 65-nm CMOS process. The measurement results show that with a static power consumption of 2.04 mW, the dynamic range is more than 20 dB in the frequency range of 3-5 GHz. Applying frequency detection circuits, the variations of the output voltage are reduced from more than 4 dB to ± 0.5 dB, achieving a variation less than ± 0.25 dB/GHz. With low power

consumption, small area, and input frequency compensation technique, the proposed power detector is suitable for multi-standard wireless communication on-chip applications.

Chapter 4

Design of Linear Power Amplifier Using Adaptive Body Bias Technique

4.1 Introduction

To handle the increased demand of users in a dense area using a limited frequency spectrum, IEEE 802.11ax standard employs up to the 1024-QAM to achieve higher spectral efficiency. With large PAPR of the signal, the PA have to operate at a back-off power from the saturated power to satisfy the linearity requirements. Therefore, many studies have been dedicated to improve the linearity of power amplifier.

Besides the linearization techniques mentioned in Chapter 2, the effect of body bias and deep N-well on the linearity of PA is analyzed before [41, 65, 66]. In [41], it is shown that a CMOS PA on a deep n-well (DNW) can significantly improve the linearity without affecting power performances under Class AB operation. It reveals that the linearity improvement by the

DNW comes mainly from the reduced harmonic distortion of intrinsic gate-source capacitance and partially from the reduced harmonic distortion from drain junction capacitance. Besides, the DNW can suppress the noise coupling through the highly conductive Si substrate.

As the gate of PA has complicated bias and matching networks, a linearization method with body controls for an RF cascode CMOS PA was proposed in [65]. It is reported both the AM-AM and AM-PM distortions are reduced using dynamic body linearizers at the CS and CG stages according to the envelope signal. However, a negative bias is used to maximize the linearization effect, which is difficult to realize in CMOS process.

In this chapter, a novel linear power amplifier using adaptive body bias (ABB) technique is introduced for 802.11ax. An improvement in the linearity near the maximum linear power is also achieved by controlling the impedance at $2f_0$. The ABB technique improves the linearity with minimized affection on other performance of the PA. Compared to adaptive gate biasing technique, this method shows better performance and design freedom.

4.2 Analysis of the Proposed Linear Power Amplifier Architecture

The overall performance of a PA strongly depend on its operation class and the MOSFETs working region. Generally, a deep class-AB mode with low

quiescent-current operates more linearly and efficiently than that with class-AB or class-A mode at a high power region because the IMD minimum point (sweet-spot) moves towards near the compression point [2]. Therefore, deep class-AB operation is the most attractive operation for linear PAs design at a high power region[46].

Figure 4.1: Voltage waveforms of the CG device [5].

The stack of CS and CG amplifiers forms a cascode amplifier. The CS at the bottom is used as a main amplification stage, and the CG amplifiers at the top of CS stage function as a current buffer. The MOSFET of the two stages works at saturation region when the input signal is small, however, when the input power is increased, the MOSFET begins to enter triode region or cut-off region, shown in Fig. 4.1[5]. The operation conditions of cut-off and triode region are shown in 4.1 and 4.2. The variation of operation

region will change the intrinsic capacitance and transconductance, which are the dominant nonlinear sources of CMOS PA.

$$V_{GS} - V_{TH} < 0 : \text{cutoff region} \quad (4.1)$$

$$V_{DS} \leq V_{GS} - V_{TH} : \text{triode region} \quad (4.2)$$

Figure 4.2: Model of the ABB Technique.

The basic idea of the proposed linear PA is to reduce the time that MOSFET works in cut-off region, and works in saturation region as long as possible. This will improve the linearity by reducing the working time that the MOSFET has a lot of distortions. One way to reduce the work time in cut-off region is to decrease the threshold voltage V_{TH} of a MOSFET device. The V_{TH} of a MOSFET device is related to the source to body voltage by the following equation:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|} \right) \quad (4.3)$$

where V_{TH0} is the threshold voltage when the voltages of source and body are equal, γ is a coefficient related to body-effect, and V_{SB} is the source-bulk potential difference[67]. It shows that if V_B drops, V_{TH0} will be increase and vice versa. The working principle of the proposed linear power amplifier is shown in Fig. 4.2.

4.3 Implementation of Proposed Power Amplifier

The proposed power amplifier is shown in Fig. 4.3. It is composed of two envelope detector (ED), one power detector (PD) and the amplify unit of differential cascode structure.

As discussed in [30], in-band small signal MOSFET nonlinearity presents a very high lobe near turn-on, followed by another lobe of smaller amplitude. That is evidenced by the fact a FET presents a severe nonlinear regime near turn-on, and the small-signal nonlinearity decreases as V_{gs} bias is increased beyond turn-on, toward class-A operation. Thus, for PA biased at deep Class-AB region, the gate bias voltage is crucial for IMD behavior. Fig. 4.4 shows the IMD3 versus output power for different gate biases of CS stage while the gate voltage of CG stage is 2.5V in the proposed PA. We

Figure 4.3: Block diagram of the proposed PA.

can see that for bias voltage below threshold voltage, the linearity is deteriorated, while biased toward Class-A, the IMD performance at high output power is worse than the bias of Class-AB. In this design, we use $0.43V_{gs1}$ for the best performance of IMD and efficiency.

The simulation results of IMD3 versus output power for different body biases of CS stage while the body voltage of CG stage is 0V are shown in Fig. 4.5. We can see that with a positive body bias, the IMD3 behavior at low and mid power range is significantly improved. The IMD3 performance at high power range is firstly degraded and then only improved at higher

Figure 4.4: IMD3 versus output power for different gate biases V_{gs1} of CS stage while the gate voltage of CG stage is 2.5V.

body voltage. Thus, we can bias the body of CS stage according to the input power. At low input power range, the body bias voltage is low to have better efficiency. While as the power increased, the voltage of the body is also increased to have optimum IMD3 performance at mid and high power range. In this design, we used an ED to detect the input power and convert to output voltage accordingly.

The simulation results of IMD3 versus output power for different body biases of CG stage while the body voltage of CS stage is 0V are shown in

Figure 4.5: IMD3 versus output power for different body biases V_{bg1} of CS stage while the gate voltage of CG stage is 0V.

Fig. 4.6. It is shown that the positive body bias for CG stage improve the IMD3 performance of PA as well. However, the improvement is not as large as that in CS stage.

The switched-capacitor MOSFET PD described in the chapter 3 is used as ED and PD in the PA. The ED differs from the power detector is that there is no load resistor and low pass filter (LPF) in the it, since the body to drain and source capacitance works as LPF already.

Figure 4.6: IMD3 versus output power for different body biases V_{bg2} of CG stage while the gate voltage of CS stage is 0V.

4.3.1 Second Harmonic Short in Cascode PA

The memory effect is mainly caused by the reflections of the envelope frequency and second harmonics at the device terminals[68]. In a real application, to eliminate the envelope signal, it is preferable to make the impedance of envelope signal short circuit. It can be realized by a low-pass filter at the envelope frequency[69]. These filters has large time constant which will lead to AM-PM distortion in the PA. Therefore, it is more practical to control the second harmonic impedance to reduce the sideband asymmetries.

There are two common voltage nodes in a differential cascode amplifier. One of the nodes is at the source of the CS stage and another is at the gate of the CG stage. The common nodes functions as a virtual ground at fundamental frequency and odd harmonics. But it is not a ground at even harmonics. If the impedance for even harmonics is high, so is the gain of even harmonics. And the even harmonics will mix with fundamental frequency to create IMD3 distortions. In the real device, it is difficult to reduce harmonic frequency at the common nodes of amplifier if there is not a harmonic control circuit[70]. To eliminate the sideband asymmetries, there are two methods, one is to terminate the second harmonic load that it only has real part or shorted, another method is to terminate the envelop frequency load to be short circuit condition.

In this design, we added two second harmonic short circuits containing a series inductor and capacitor. That will reduce the gain of even harmonics including second harmonic thus reducing the mixing of second harmonic with fundamental frequency and IMD3. The values of inductor and capacitor are 741.4pH and 268.7fF, respectively.

4.3.2 Design Procedure of PA

Two series capacitors and resistors are connected from the drain of CG to the gate of CS stage, forming a feedback circuit to reduce the gain of PA

and make the PA unconditional stable. The value of capacitor and resistor is 100fF and 100 Ω , respectively. The size of MOSFET is decided by the load pull simulation and PAE results. The widths of CS and CG stage are 640 μm and 960 μm , respectively.

Figure 4.7: Output power simulation results of PA with and without adaptive body biasing.

The insertion loss of the input and output transformers in a differential structure are mainly dependent on a quality factor of the material to build it. The two top metals are used for the design of transformers. The optimum output impedance of the power cell is determined through the load-pull simulation. After the design of output transformer, the input transformer is designed based on conjugate matching.

Figure 4.8: Power gain simulation results of PA with and without adaptive body biasing.

Figure 4.9: PAE simulation results of PA with and without adaptive body biasing.

Figure 4.10: IMD3 simulation results of PA with and without adaptive body biasing.

The simulation results of the output power, power gain, PAE, and IMD3 of the proposed power amplifier with and without adaptive biasing technique are compared in Fig 4.7, Fig 4.8, Fig 4.9, and Fig. 4.10. It shows that the proposed linearization technique improves the linearity without affecting other figure of merits (FOM) of the PA. The output power, power gain, and PAE did not changed or is slightly better than the results without ABB. And the IMD3 is improved greatly in the middle input power range, more than 10dB at around 17dBm input power level.

4.4 Measurement Results

The proposed PA is implemented in GlobalFoundries 65-nm CMOS process. The chip area is $1180 \times 700 \mu\text{m}^2$. The micrograph of the PA is shown in Fig. 4.11. The PA is measured on probe station under room temperature.

Figure 4.11: The micrograph of the proposed PA.

The S-parameter of the PA is shown in Fig. 4.12. The small signal bandwidth of this PA satisfies the requirements of WLAN 802.11ax at 5GHz with a 3-dB bandwidth of 2GHz. The drain efficiency (DE), PAE, and power gain at 5GHz are shown in Fig. 4.13. From the measurement results, we could see that the the saturation power is 22dBm. The power gain is more than 10dB for small signal at 5GHz. The maximum PAE is above 26%. The large signal performance of the proposed PA from 4.5GHz to 6GHz are shown in Fig. 4.14.

Figure 4.12: The measured S-parameter of the proposed PA.

Figure 4.13: The measured DE (%), power gain, and PAE (%) of the proposed PA at 5GHz.

Figure 4.14: The measured maximum DE (%), power gain, and PAE (%) of the proposed PA for different operation frequencies between 4.5GHz and 6GHz.

Table 4.1: Comparisons with other published linear PA

Reference	Operating Frequency (GHz)	P _{out} (dBm)	Power Gain (dB)	PAE (%)	Output Power(@IMD3 = -30dBc)
[41]	2.45	20(Single-ended) 20.2(Differential)	18.7(Single-ended) 18.9(Differential)	31(Single-ended) 35(Differential)	19
[3]	1.75	24	23.9	28	24
[1]	2.5	28.1	10	46.8	20
[2]	1.85	27.8(Off-chip output matching) 27.5(On-chip output matching)	11*	41.0(Off-chip) 35.2(On-chip)	27
This work	4.5-6	22	10.5	26	16

* Simulated results.

The measured output power at which IMD3 is below -30dBc is 16dBm. The comparison table with other published PA are shown in Table 4.1. The key achievement is another applicable method to improve the linearity of the PA is proposed. The proposed method improved the linearity without changing much other performances of the PA. The major issue of this method is the linearity improvement is limited. Using this method alone is not guarantee we can achieve the demanded linearity. The proposed method is better to be used with other method at the same time. In this design, the ABB technique is used along with second harmonic short method.

4.5 Summary

In this chapter, a highly linear PA with adaptive body biasing technique for IEEE 802.11ax standard is reported. Through two EDs, the envelopes of the input signal and output of common-source stage are detected. After voltage shifting, the output voltages of EDs are applied to the body of the MOSFETs of CS and CG stages to improve the linearity of the cascode-structure PA. Implemented in 65-nm CMOS technology, the PA shows a saturation power is 22dBm from the measurement results. The power gain is 10.5dB for small signal. The maximum PAE is 26%. These FOMs remained or is slightly better than the results without ABB. And the IMD3 is improved in the middle to high input power range. The output power at which IMD3 is below -30dBc

is 16dBm.

Chapter 5

Conclusion and Future Works

5.1 Conclusion

This thesis illustrates the concept and design of high performance power detectors and high linearity power amplifiers for IEEE 802.11ax applications.

In Chapter 2, the fundamentals of the PA are introduced. The non-linearity effects and state-of-the-art linearization technique are reviewed.

In Chapter 3, a power detector with switched capacitor structure is introduced firstly, then the variation of this PD by replacing the diode with self-biased MOSFETs are presented. In this chapter, We have demonstrated a high dynamic range, high input power, low power consumption diode power detector with an area of 0.0036 mm^2 using 65-nm CMOS process. The measurement results show that with a static power consumption of 0.7 mW, the dynamic range is more than 30 dB in the frequency range of 4-6 GHz with ± 1 dB error. The maximum input power is 35 dBm, which is the highest input power to the authors' knowledge. We also demonstrated a self-biased

MOSFET version of the PD. By replacing the diode with self-biased MOSFET, the minimum detectable power is lower. The measured dynamic range is more than 32.5 dB in the frequency range from 4-6 GHz. The static power consumption is 0.144 mW. At last, a PD with input frequency compensation technique is introduced. In this work, we have verified the idea of the input frequency can be compensated by changing the load resistance of the PD by designing an input frequency compensated, low power consumption, reasonable DR power detector with an area of 0.014 mm² in a 65-nm CMOS process. The measurement results show that with a static power consumption of 2.04 mW, the dynamic range is more than 20 dB in the frequency range of 3-5 GHz. Applying frequency detection circuits, the variations of the output voltage are reduced from more than 4 dB to ± 0.5 dB, achieving a variation less than ± 0.25 dB/GHz. With low power consumption, small area, and input frequency compensation technique, the proposed power detector is suitable for multi-standard wireless communication on-chip applications.

In Chapter 4, a highly linear PA with adaptive body biasing technique for IEEE 802.11ax standard is reported. Through two EDs, the envelopes of the input signal and output of common-source stage are detected. After voltage shifting, the output voltages of EDs are applied on the body of the MOSFET of CS and CG stages to improve the linearity of the cascode-structure PA. Implemented in 65-nm CMOS technology, the PA shows a saturation power

of 22dBm from the measurement results. The power gain is 10.5dB for small signal. The maximum PAE is 26%. These FOMs is not changed or slightly better than the results without ABB. And the IMD3 is improved in the middle to high input power range. The output power at which IMD3 is below -30dBc is 16dBm.

5.2 Future Works

Although the PDs and PA presented in this thesis demonstrates state-of-the-art performance compared to previous works, there are still some improvements that can be implemented.

5.2.1 Improvement on the Proposed PD

For the frequency compensated PD presented in chapter 3, it is expected to work in a very wide frequency range so that the benefits of frequency variation compensation can be fully demonstrated. However, the working frequency range of this PD need to be improved as well as the dynamic range. The power detection circuit is same as the MOSFET PD without frequency compensation circuit, but the DR is deteriorated a lot. The reason for the reduction in dynamic range could be the loading effect of the frequency detection circuit. The working principle of the frequency compensated PD still need to be investigated to achieve wide DR. Besides, although

Figure 5.1: Simulated FVC output variations with temperatures at 1GHz input frequency.

the variations of input frequencies are compensated, the PVT variation is not considered. The frequency compensated PD presented utilize frequency-to-voltage converter which is relatively sensitive to PVT variations. A PVT compensation circuit should be added to solve this problem. A simulation result of the effect of temperature variation to the FVC is shown below to verify the sensitivity in Fig. 5.1. We would like to design temperature compensation circuit for the FVC and the PD in the future work.

5.2.2 Improvement on the Proposed PA

The linearity of PA with the ABB technique still can be further improved. Second harmonic traps are added at the gate of CS stage. However, as

reported in [1], second harmonic traps at the center tap of transformer and the gate of CG stage also improve the linearity. More second harmonic traps could be added in this design. Besides, the load resistor of the ED should be optimized. In the proposed PA, the body bias voltage of the MOSFET is determined by the output voltage of the ED which is directly related to the load resistor of the ED. The optimum relationship between load resistance and IMD3 performance of PA should be investigated and analyzed more. Moreover, PA is the most power-hungry component in the transmitters. To improve the efficiency of the proposed PA is very important as it will extend the battery life for mobile devices. There are several ways to improve the efficiency of PA. Among them the envelope tracking method seems very promising. It utilizes the supply modulator to track the envelope voltage of the input signal, then varies the supply of the PA accordingly. It will improve the efficiency tremendously. However, the bandwidth of traditional supply modulator is usually less than 20 MHz. To improve the bandwidth of the supply modulator, making it suitable for 160 MHz 802.11ax signal is a great challenge. Our goal is to design the supply modulator with more than 200 MHz bandwidth for Wi-Fi applications.

Figure 5.2: Simple block diagram of ET system [6].

Author's Publications

Journal Papers

- (i) **Chenyang Li**, Chirn Chye Boon, Xiang Yi, Zhipeng Liang, Kaituo Yang. "Compact Switched-Capacitor Power Detector with Frequency Compensation in 65-nm CMOS." *IEEE Access*, vol. 8, pp. 34197–34203, 2020.
- (ii) **Chenyang Li**, Xiang Yi, Chirn Chye Boon, Kaituo Yang. "A 34-dB Dynamic Range 0.7-mW Compact Switched-Capacitor Power Detector in 65-nm CMOS." *IEEE Trans. Power Electron.* vol. 34, no. 10, pp. 9365-9368, 2019.
- (iii) **Chenyang Li**, Chirn Chye Boon, Yongkui Yang, Enyi Yao, and Minoru Fujishima. "MOSFET Small-Signal Model Considering Hot-Carrier Effect for Millimeter-Wave Frequencies." *J. Infrared, Millimeter, Terahertz Waves*, vol.40, no. 4, pp. 419-428, 2019.
- (iv) Yi, Xiang, Zhipeng Liang, Guangyin Feng, Fanyi Meng, Cheng Wang, **Chenyang Li**, Kaituo Yang, Bei Liu, and Chirn Chye Boon. "A 93.4–104.8-GHz 57-mW Fractional-N Cascaded PLL With True In-Phase Injection-Coupled QVCO in 65-nm CMOS Technology." *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 6, pp. 2370-2381, 2019.

- (v) Yi, Xiang, Guangyin Feng, Zhipeng Liang, Cheng Wang, Bei Liu, **Chenyang Li**, Kaituo Yang, Chirn Chye Boon, and Quan Xue. "A 24/77 GHz Dual-Band Receiver for Automotive Radar Applications." *IEEE Access*, vol. 7, pp. 48053-48059, 2019.
- (vi) Khanna, Devrishi, Chirn Chye Boon, Pilsoon Choi, Liter Siek, Bei Liu, and **Chenyang Li**. "A Low-Noise, Positive-Input, Negative-Output Voltage Generator for Low-to-Moderate Driving Capacity Applications." *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3423-3436, 2019.
- (vii) Liang, Yuan, Chirn Chye Boon, **Chenyang Li**, Xiao-Lan Tang, Herman Jalli Ng, Dietmar Kissinger, Yong Wang, Qingfeng Zhang, and Hao Yu. "Design and Analysis of D-Band On-Chip Modulator and Signal Source Based on Split-Ring Resonator." *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 7, pp. 1513-1526, 2019.
- (viii) Liu, Bei, Xiang Yi, Kaituo Yang, Zhipeng Liang, Guangyin Feng, Pilsoon Choi, Chirn Chye Boon, and **Chenyang Li**. "A Carrier Aggregation Transmitter Front End for 5-GHz WLAN 802.11 ax Application in 40-nm CMOS." *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 1, pp. 264-276, 2019.
- (ix) Haohong Yu, Yong Chen, Chirn Chye Boon, **Chenyang Li**, Mak, Pui-In, Martins, Rui P. "A 0.044-mm 2 0.5-to-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3 ± 0.45 dB." *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 71-75, 2018.
- (x) Quan, Xing, Xiang Yi, Chirn Chye Boon, Kaituo Yang, **Chenyang Li**, Bei Liu, Zhipeng Liang, and Yiqi Zhuang. "A 52–57 GHz 6-bit phase shifter with hybrid of passive and active structures." *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 236-238, 2018.

- (xi) Feng, Guangyin, Chirn Chye Boon, Fanyi Meng, Xiang Yi, Kaituo Yang, **Chenyang Li**, and Howard C. Luong. "Pole-converging intrastage bandwidth extension technique for wideband amplifiers." *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 769-780, 2017.
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- (i) Liang, Yuan, Hao Yu, Chirn Chye Boon, **Chenyang Li**, Dietmar Kissinger, and Yong Wang. "D-band surface-wave modulator and signal source with 40 dB extinction ratio and 3.7 mW output power in 65 nm CMOS." in *Proc. IEEE Eur. Solid State Circuits Conf.*, pp. 142-145. Sep. 2018.
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