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TSV-integrated Surface Electrode Ion Trap for Scalable Quantum Information Processing

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In this study, we report about design, fabrication and operation of a Cu-filled through silicon via (TSV) integrated ion trap. TSVs are placed directly underneath electrodes as vertical interconnections between ion trap and a glass interposer, facilitating the arbitrary geometry design with increasing electrodes numbers and evolving complexity. The integration of TSVs reduces the form factor of ion trap by more than 80%, minimizing parasitic capacitance from 32 ± 2 to 3 ± 0.2 pF. A low RF dissipation is achieved in spite of the absence of ground screening layer. The entire fabrication process is on 12-inch wafer and compatible with established CMOS back end process. We demonstrate the basic functionality of the trap by loading and laser-cooling single $^{88}\text{Sr}^+$ ions. It is found that both heating rate (17 quanta/ms for an axial frequency of 300 kHz) and lifetime (~ 30 minutes) are comparable with traps of similar dimensions. This work pioneers the development of TSV-integrated ion traps, enriching the toolbox for scalable quantum computing.

Quantum information processing (QIP) platforms recently released from IonQ and Honeywell have highlighted the impressive development of surface electrode ion traps^{1,2}. Taking advantage of well-established microfabrication techniques (i.e., MEMS and CMOS), surface electrode ion traps exhibits flexible design associated to reproducible and mass production compatible fabrication³. More importantly, the possible integration with photonics components (i.e., waveguides, grating couplers^{4,6} and photodetectors⁷) enables precise control and measurement on individual trapped ion. These features make surface electrode ion trap highly promising for large scale QIP. To scale close or even beyond noisy intermediate-scale quantum regime (NISQ, ~ 100 ions)⁸, 1D arrays, 2D arrays^{9,10} and quantum charge-coupled device (QCCD) geometries^{11,12} have been proposed with evolving electrodes layout complexity. However, this strategy opens significant challenges for electric signal delivery, since conventional bonding wires are not able to access the isolated island-like electrodes, and large number of wires will further impede laser beams.

The previous approach to mitigate this challenge is to employ multilayer metallization, where patterned metal layers and dielectric materials are alternately overlapped beneath surface electrodes¹³⁻¹⁶. Small vias through dielectric layers are required to build interconnections between different metal layers, while a bottom metal layer is often used as a grounding plane to shield the silicon substrate from RF electric field. The incorporation of routing leads underneath allows for flexible design of surface electrodes geometry, especially in the case where extremely small electrodes are required (e. g. junctions in multi-track traps). However, this approach also comes with issues. First, the integration of photonics components, that requires stringent wafer flatness, has to be implemented below the multilayer metallization: this hampers waveguide realization and

thus degrades scalability. In addition, thick (~ 10 μm) dielectric layer formation and patterning necessitate non-standard fabrication techniques, limiting the compatibility with large-scale foundry manufacturing¹⁷. Eventually, the multilayer metallization may increase the coupling parasitics⁹, resulting in high RF losses and subsequent heating of the device.

Through substrate vias are another effective approach to ion trap integration. With relatively small form factor and large pitch, through substrate vias feature small parasitic and are more compatible with photonics integration. Moreover, this technology eliminates the requirement for thick dielectric layers: the patterning of a thin (~ 3 μm) SiO_2 layer between electrodes and substrate becomes foundry compatible. As reported by Guise *et al*¹⁸, polysilicon filled vias of ~ 50 μm diameter can be indeed used for surface electrode connection. However, due to the poor conductivity of polysilicon, only DC electrodes were contacted with vias. Moreover, platinum silicide growth was required to create ohmic contacts between electrodes and polysilicon. In another work (Li *et al*¹⁹), a ring trap was connected with 100 μm diameter electrical vias etched through a 70 μm glass substrate followed by 800 nm gold deposition. However, the reported customized process was not compatible with large-scale fabrication. In order to improve vias performance and further boost the scalability, we demonstrate in this work the effectiveness of a Cu-filled TSV integrated surface ion trap. With intrinsically small resistance, Cu-filled TSVs are used here as vertical connections between all the electrodes (including RF) and an interposer underneath. Besides, standard back end of line CMOS process on 12-inch wafer is used, facilitating high resolution and repeatability of traps fabrication. Additionally, as bonding wires are connected to an interposer underneath, the height difference between ion trap and the interposer may mitigate laser beam blocking issues.

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In the future, further optimization of both TSV and multilayer metallization technologies is foreseen. However, a combination of the two techniques will be probably necessary to realize larger-scale ion traps with lower RF losses, larger number of small electrodes, and higher density of photonic components.

FIG. 1. (a) 3D schematic of TSV-integrated ion trap (TSV trap, not to scale). The geometry is modified from wire bonding (WB) trap (inset). (b) Cross-sectional SEM image of TSV trap. The surface electrode and interposer RDL are interconnected by TSV and micro bumps.

We designed the TSV integrated ion trap (TSV trap) starting from a previous 5 wire design^{20,21} that includes bonding pads (WB, wire bonding trap). As shown in Fig. 1(a), TSV trap geometry only preserves the core region, eliminating the wire bonding pads and the connecting circuits present in the WB trap²². The original wire bonding pads are transferred to an interposer, drastically reducing the surface of the electrodes. This minimizes undesired parasitic couplings and mitigate the RF losses issues. The width and length of the three central electrodes are respectively 80 and 2920 μm , while the gap between them is 5 μm wide. TSVs are designed with a diameter of 20 μm and a depth of 100 μm . The pitch between TSVs is 100 μm . 10 TSVs are accommodated under RF electrodes, while 6 or 10 TSVs are accommodated under DC electrodes, depending on the electrode size. Micro bumps with a diameter of ~ 30 μm are located underneath every single TSV to allow for connection and assembling with the interposer. The interposer is designed with a redistribution layer (RDL), acting as a bridge between the ceramic pin grid array package (CPGA) and the TSV trap for electrical connection (Fig. 1(b)). The tested RDL geometry is a sort of extension of trap electrodes. Obviously, more complex routing can be implemented where necessary. While the TSV trap is made on a silicon substrate, we choose to use a glass substrate to fabricate the interposer, in order to minimize RF losses and simplify the fabrication process.

TSV die (silicon wafer) fabrication starts with the etching of blind vias through ~ 2.4 μm SiO_2 and 100 μm Si using Bosch process before wafer frontside patterning,

as shown in Fig. 2(a). To insulate the Cu cores from Si substrate, a 0.75 μm thick SiO_2 layer (TSV liner) is uniformly deposited onto vias sidewalls by plasma enhanced chemical vapor deposition (PECVD). The vias are then filled with Cu by electrochemical plating (ECP), as shown in Fig. 2(b). To completely remove Cu overburden induced by the coefficient of thermal expansion (CTE) mismatch between Cu and Si, two steps of chemical-mechanical polishing (CMP) before and after annealing (250 $^\circ\text{C}$, 30 minutes) are required. Fig. 2(c) shows the patterning of frontside SiO_2 , which has same geometry as electrodes, to avoid undesired dielectric charging issues possibly affecting ion trapping. Fig. 2(d) shows lithography defined ECP of 3 μm Cu with 0.3 μm Au finish (in the absence of a diffusion barrier between the two metals). After temporary bonding with a handle wafer, the device wafer is thinned to ~ 100 μm by grinding and dry etching. SiO_2 layer is then deposited on the backside, followed by polishing and etching to expose TSV, as shown in Fig. 2(e). The backside redistribution layer (RDL) is formed by lithography defined ECP of 3 μm Cu. Next, a polyamide layer with lithography defined openings is deposited to protect RDL from oxidization (Fig. 2(f)). The last lithography step is performed before ECP of micro bumps (10 μm Cu and 15 μm SnAg). Finally, the device wafer is de-bonded from handle wafer (Fig. 2(g)).

The fabrication of glass interposer is similar to that of the backside process of the TSV die, where three steps of lithography are required, but the last one is used to define under bump metallization (UBM) instead of micro bump. Note that fabrication processes of both glass wafer and silicon wafer are compatible with standard back end process in CMOS foundry, in which 12-inch wafer are used and $\sim 2,000$ single dies with different design dimensions are fabricated simultaneously (Fig. 3(a) and (b)). After wafer singulation, selected dies are bonded together. In order to perform this operation TSV dies and glass interposers are aligned according to three paired markers located on TSV die backside and glass interposer frontside. Eventually, bonded ion trap is assembled into CPGA, as shown in Fig. 3(c).

FIG. 2. Fabrication process of TSV die (silicon wafer). (a-d) Process on wafer frontside and (e-g) process on wafer backside.

FIG. 3. (a) Fabricated TSV die on 12-inch silicon wafer. (b) Fabricated interposer on 12-inch glass wafer. (c) Packaged TSV trap in a CPGA.

To assess the reliability of TSV liner, a voltage sweep from -200 to 200 V is applied to TSVs. It is found the maximum leakage current for a single TSV is about 7×10^{-12} A, suggesting that the $0.75 \mu\text{m}$ thick TSV liner is able to withstand a voltage of 200 V and will not breakdown. Also, a resistance measurement is performed between RF and central DC electrodes on both ion trap and glass interposer. The results shows a minimum resistance of $\sim 2 \times 10^8 \Omega$, which is sufficiently large for voltage insulation. In addition, we check the connection between interposer RDL and corresponding surface electrodes: no open circuit is found, indicating a reliable electrical connection path. In summary, the yield for silicon wafer is $\sim 80\%$, limited by the debonding process, during which some of dies at the wafer edge get cracks after peeling-off bonding material. The yield for glass wafer is $\sim 99\%$.

FIG. 4. (a) Resonance test of ion traps packaged into CPGA. We compare the resonance curves obtained with WB and TSV traps to those obtained with ultra-low ESR test capacitors (AVX SQ series) of 33 and 5.6 pF wire-bonded to another CPGA. The fit of the curves with the response of a model circuit (inset) allows us to estimate that, for the same driving RF voltage, the TSV trap dissipates 26 time less than WB trap. (b) On-chip S parameter test of TSV die before and after bonding with glass interposer. The curves from WB trap are also plotted for comparison, showing TSV trap can reduce the insertion loss from -2.2 to -0.1 dB (at 50 MHz). The inset shows a three-pin probe contacting on electrodes surface.

One of the major challenges for ion trap based on semiconductor substrates is the high RF dissipation²³⁻²⁵. To evaluate the RF performance of the TSV trap, a WB trap with silicon substrate but no grounding plane is used for comparison. Given that the power loss is largely determined by the parasitic capacitance of the trap²¹, a capacitance-voltage (C-V) test is first performed. The measurements shows that the TSV trap has a capacitance between an RF and the central DC electrode of 3 ± 0.2 pF, with respect to 32 ± 2 pF for that of WB trap. The error bars are dominated by chip to chip variations. This 90% capacitance decrease can be attributed to the significant reduction of electrode surfaces (from 4.5 to 0.2 mm², for single RF electrode). We also perform resonator tests of

the traps²⁶ to obtain information about the expected dissipation. In these tests packaged traps (i.e., traps wire bonded to CPGAs) are connected to a resonant transformer that can be schematized by a series LRC resonant circuit driven by an ac voltage source (Fig. 4a, inset). The resonance curves shown Fig. 4 (a) are then determined by the characteristics of two elements: 1) the resonant circuit + cabling + CPGA; 2) the trap itself. We perform comparative tests between the two traps and two ultralow equivalent series resistance (ESR) capacitances (AVX SQ series capacitors, ESR in the m Ω range) wire-bonded to another CPGA. In these conditions we can retrieve from a fit of the trap resonance curves the ESRs associated to the traps (of the order of 30 Ω) and then the ratio between the RF losses of the two traps (a TSV trap dissipates 26 time less than a WB trap), proportional to the ESR and to $\Omega_{RF}^2 \times C^2$ ²¹.

On-chip S parameter measurements are also carried out: the overlapping curves from TSV die (without interposer) and TSV trap (with interposer) in Fig. 4(b) indicate that negligible additional losses are induced by the incorporation of glass interposer.

The packaged TSV trap of Fig. 3(c) is tested in a laser-cooled trapped ion setup by loading it with single $^{88}\text{Sr}^+$ ions. Technical details of the setup are described elsewhere^{27,28}.

We insert the CPGA in the vacuum cell and then bake at 150°C for one week. The resulting base pressure is approximately 4×10^{-11} mbar, demonstrating the excellent ultra-high vacuum compatibility of the packaged ensemble (trap, interposer and micro-bumps). The two RF electrodes are driven by an impedance-matching toroidal resonant transformer at a frequency $\Omega_{RF}/2\pi = 30$ MHz. We only test the trap with amplitudes V_{RF} below 120 V. For V_{RF} larger than 85 V we notice a slight increase of the base pressure (of the order of some 10^{-11} mbar), probably associated to residual heat dissipation in the trap. We load the trap by two-colour photo-ionizing a thermally sublimated Sr atomic beam^{29,30}.

The $^{88}\text{Sr}^+$ ions are Doppler-cooled addressing the $5^2S_{1/2} \rightarrow 5^2P_{1/2}$ transition (422 nm, 711 THz). The wavevector of the cooling laser is parallel to the trap substrate and makes an angle of 45° with the axial direction (i.e., the laser is aligned along the horizontal direction of Fig. 5a). To avoid optical pumping into the metastable $4^2D_{3/2}$ state we use two additional lasers (“repumpers”) addressing the 1003 nm (299 THz) $4^2D_{3/2} \rightarrow 5^2P_{3/2}$ transition and the 1033 nm (290 THz) $4^2D_{5/2} \rightarrow 5^2P_{3/2}$ transition (incoherent repumping scheme³¹). 422 nm photons scattered by the ion are collected by a home-made objective with numerical aperture of 0.4 and detected by a photomultiplier in photon-counting mode. An overall collection efficiency of $(1.8 \pm 0.2 \times 10^{-3})$ is measured using sequential acquisitions that require the 1092 nm (275 THz) “readout” laser addressing the $4^2D_{3/2} \rightarrow 5^2P_{1/2}$ transition³².

We also acquire images of the trapped and cooled ions with an electron-multiplier CCD camera (Andor Luca), as shown in Fig. 5(a).

FIG. 5. (a) Image of a single $^{88}\text{Sr}^+$ laser-cooled ion trapped above the surface of the TSV trap; the image field covers a 1 mm^2 area, the trap is illuminated by a light emitting diode. (b) Counting rate as a function of the re-cooling time averaged over 120 realisations for a heating period duration $t_h = 20$ seconds (blue squares). The continuous black curve is the best one-parameter fit that allows us to retrieve a temperature increase $T=5.1\text{ K}$. Inset: fluorescence spectrum of the ion as a function of the detuning of a probe beam that scans the cooling transition (red circles); the continuous black curve is a Lorentzian fit that shows that the incoherent repumping scheme leads to a very good two-level atom approximation.

Excess of micromotion in the trap is minimized using a single photon time correlation method³³. The compensation DC voltages are found to be stable in a week basis. The lifetime of a laser-cooled ion in the trap is of the order of 30 minutes, compatible with the vacuum level.

We evaluate the trap performances by measuring the heating rate with the technique of Doppler re-cooling³⁴.

To this purpose we operate the trap with an axial frequency $\omega_z/2\pi = 300\text{ kHz}$ and radial frequencies around $\omega_r/2\pi = 2.6\text{ MHz}$. In this situation we expect that the re-cooling dynamics will be dominated by the temperature of the low frequency axial mode, even though the cooling laser wavevector has a non-negligible projection along the radial direction³⁵. A sequential acquisition first cools the ion during 500 ms, then switches-off the cooling laser defining a heating period duration t_h , and then switches-on again the cooling laser triggering the acquisition of single photons timestamped with their arrival times. The two-level-atom approximation needed for the analysis of the acquired data^{34,35} is well fulfilled by the incoherent repumping approach: we show in Fig. 5(b, inset) a single-ion fluorescence spectrum that displays a Lorentzian line-shape. We record single shot and average histograms of the scattered photons as a function of the emission time for different heating times t_h . An example of averaged histogram is plotted in Fig. 5(b) with the corresponding fit obtained with the hypothesis of a Maxwell-Boltzmann velocity distribution ($T=5.1\text{ K}$ for $t_h = 20\text{ s}$). From the analysis of all the experimental sets the heating rate of the trap is evaluated at $250 \pm 15\text{ mK/s}$ that corresponds to 17 axial quanta per millisecond. The calculated figure of merit corresponding to the noise spectral density times the motional frequency³⁶ is $\omega_z S_E(\omega_z) = 1.5 \times 10^{-4}\text{ (V/m)}^2$. Technical noise contribution to this figure is expected to be negligible, thanks to previous evaluations performed with the same setup. While it does not set a record, this result favorably compares to non-decontaminated non-cryogenics traps of similar dimensions³⁷.

In conclusion we demonstrate the fabrication in a CMOS foundry and the full functionality of a silicon-

substrate surface ion trap in which all the electric connections (i.e., DC and RF) are realized with through silicon vias. We load single $^{88}\text{Sr}^+$ ions into the trap and we find that the heating rate, lifetime and stability are comparable with other traps of similar dimensions. This work pioneers the development of TSV-integrated ion traps, enriching the toolbox for trapped ion based scalable quantum computing. In particular the TSV approach is compatible with photonic circuit integration⁴⁻⁶, insertion of a ground screening layer to eliminate trap-heating, and in the future could be extended to glass substrates²⁸.

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