Design of digital-intensive time-mode data converters based on delay correction utilising a time-to-digital converter

Kong, Junjie

2021

Kong, J. (2021). Design of digital-intensive time-mode data converters based on delay correction utilising a time-to-digital converter. Doctoral thesis, Nanyang Technological University, Singapore. <https://hdl.handle.net/10356/148431>

<https://hdl.handle.net/10356/148431>

<https://doi.org/10.32657/10356/148431>

This work is licensed under a Creative Commons Attribution-NonCommercial 4.0 International License (CC BY-NC 4.0).

Downloaded on 26 Apr 2023 11:47:25 SGT

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

SINGAPORE

**DESIGN OF DIGITAL-INTENSIVE TIME-MODE DATA
CONVERTERS BASED ON DELAY CORRECTION
UTILISING A TIME-TO-DIGITAL CONVERTER**

KONG JUNJIE

School of Electrical & Electronic Engineering

2021

**DESIGN OF DIGITAL-INTENSIVE TIME-MODE DATA
CONVERTERS BASED ON DELAY CORRECTION
UTILISING A TIME-TO-DIGITAL CONVERTER**

KONG JUNJIE

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2021

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

.....29-01-2021
Date

.....
Kong Junjie

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

.....29-01-2021

Date

.....

Assoc Prof Siek Liter

Authorship Attribution Statement

Please select one of the following; *delete as appropriate:

~~*(A) This thesis **does not** contain any materials from papers published in peer-reviewed journals or from papers accepted at conferences in which I am listed as an author.~~

*(B) This thesis contains material from 3 paper(s) published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 3 is published as J. Kong, L. Siek and C. Kok, "A 9-bit body-biased vernier ring time-to-digital converter in 65 nm CMOS technology," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 1650-1653. DOI: 10.1109/ISCAS.2015.7168967

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts. The manuscript was revised by A/Prof Siek Liter.
- All the design and simulation work was done at VIRTUS, IC Design Centre of Excellence at the School of Electrical and Electronics Engineering.
- Kok Chiangliang assisted in the presentation of the results.

Chapter 4 is published as J. Kong, S. Henzler, D. Schmitt-Landsiedel and L. Siek, "A 9-bit, 1.08ps resolution two-step time-to-digital converter in 65 nm CMOS for time-mode ADC," 2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, 2016, pp. 348-351. DOI: 10.1109/APCCAS.2016.7803972

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts. The manuscript was revised by A/Prof Siek Liter.

- Dr Stephan Henzler provided the guidance on the concept
- Prof. Dr. rer. nat. Doris Schmitt-Landsiedel provided the resources at the Technical University of Munich where the design was done with the UMC 65 nm PDK.
- All the design and simulation work was done at Technical University of Munich.
- A/Prof Siek Liter edited the manuscript drafts.

Chapter 6 is published as J. Kong, L. Siek and S. Henzler, "A novel voltage-to-time conversion technique based on delay mapping and correction for applications in time-mode analogue-to-digital converters," as submitted to The Journal of Engineering

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts. The manuscript was revised by A/Prof Siek Liter.
- All the design and simulation work was done at VIRTUS, IC Design Centre of Excellence at the School of Electrical and Electronics Engineering.
- Dr. Stephan Henzler facilitated the discussions regarding the initial concepts.
- A/Prof Siek Liter edited the manuscript drafts.

...29-01-2021.....
Date

.....

Kong Junjie

Table of Contents

Statement of Originality	3
Supervisor Declaration Statement.....	4
Authorship Attribution Statement.....	5
Acknowledgements	9
Abstract	10
List of Figures	13
List of Tables	18
1 Introduction	19
1.1 Motivation	19
1.2 Objectives.....	22
1.3 Major Contribution of the Thesis.....	22
1.4 Organization of the Thesis	23
2 Literature Survey.....	25
2.1 Time-to-Digital Conversion techniques.....	25
2.2 Variable Delay Cell.....	40
2.3 Voltage-to-Time conversion techniques	47
3 A 9-bit body-biased Vernier Ring Time-to-Digital Converter in 65 nm CMOS Technology.....	53
3.1 Introduction.....	53
3.2 Body-biasing.....	54
3.3 Vernier Ring TDC (VRTDC) Concept.....	55
3.4 Circuit implementation	57
3.5 Results and Discussion	69
3.6 Conclusion.....	95
4 A 9-bit 1.08ps resolution body-biased Two-Step Time-to-Digital Converter in 65 nm CMOS for Time-Mode ADC	97
4.1 Introduction.....	97
4.2 Concept of the proposed coarse-fine TDC	99
4.3 Circuit Implementation.....	108
4.4 Results and Discussion	116
4.5 Conclusion.....	151
5 TDC-based Voltage-to-Time Conversion	153

5.1	Introduction.....	153
5.2	Concept.....	154
5.3	Circuit Implementation.....	162
5.4	Results and Discussion	170
5.5	Conclusion.....	175
6	A 9-bit digital-intensive twin-mode Data Converter based on delay mapping and correction using TDC.....	177
6.1	Introduction.....	177
6.2	Concept.....	182
6.3	Circuit Implementation.....	197
6.4	Results and Discussion	212
6.5	Conclusion.....	239
7	Conclusion and Recommendations	241
7.1	Conclusion.....	241
7.2	Recommendations for future research	243
	Author's Publications	250
	Bibliography.....	251

Acknowledgements

This PhD journey has been an experience of a lifetime. But this journey would not have been possible without the people I have met these many years.

Firstly, many thanks to Global Foundries for the tape-out support in the 65 nm CMOS technology, permitting the realisation of the designs in silicon. I would also like to thank Nanyang Technological University for the PhD opportunity and the NPGS scholarship, with which I had the privilege to obtain various support for my research work. The bulk of the research work was done at VIRTUS, IC Design Centre of Excellence. I would like to thank the professors, staff and colleagues in the lab who have lent their technical support.

I would also like to extend my sincere appreciation to the members in the research group, with whom I have had multiple exchanges of experiences and sparring of ideas. And to the head of the research group and my supervisor, Prof. Siek Liter, to whom I am forever grateful, I would like to express my deepest thanks, gratitude and respect. He has shown us a great deal of intelligence, patience, empathy, selflessness, tolerance, and support and has been very open-minded to new ideas and sharing of experiences. I also want to thank him for the rare opportunity to embark on the Joint NTU-TUM PhD programme.

My sincere gratitude goes to the Chair of Circuit Design at the Technical University of Munich for the research residency and the exposure to the UMC 65 nm PDK. A big thank you to retired Prof. Dr. rer. nat. Doris Schmitt-Landsiedel and Dr. Stephan Henzler who have been very encouraging to the new idea of the TDC-based VTC.

Last but not least, I would like to extend my acknowledgement to the people who have stood by me these years, giving me the mental support, showing me unconditional love, care and concern as I find myself struggling from time to time in this journey – my family. To them I will always be deeply grateful. And to my wife who has shown me how one should never be deterred by difficulties in life, and who has been there for me throughout this journey, I will always be indebted.

Abstract

Traditional methods of analogue-digital conversion quantise data in the voltage domain. Device scaling makes it harder to resolve signals in the voltage domain with reasonable power consumption, due to down-scaling voltage supplies but stagnating noise levels, therefore reducing the Signal-to-Noise Ratio. Many designs rely on bulky calibration (backend and frontend) circuits to improve the analogue performance, with many taking the form of digital calibration.

On the other hand, switching time of a MOSFET has improved with advanced nodes, giving more accuracy in time-domain resolution of digital signal edge transitions. This opens up the possibility of implementing ADCs in time-mode, capitalizing on this advantage. Unconventional methods of using time-domain for quantisation are thus gaining popularity in the form of time-mode ADCs. In such approaches, analogue information is represented by time delay through a voltage-to-time converter (VTC) and processed by a time-to-digital converter (TDC) which is largely digital and can exploit the digital advantages of newer technologies.

Because the switching speed of transistors increases with smaller technology nodes, one could expect that the resolution of TDCs are heading in the range of femtoseconds. There are many well-known TDC architectures that are aimed at achieving this target. Amplifying time, interpolating between time pulses, or even subtracting delay between two cells (Vernier principle), just to name a few, are some of the reported techniques. On top of that, manipulating the bulk potential of the transistors vary the threshold voltage depending on the polarity of the source-bulk potential. This coupled with the Vernier principle was the method used in the proposed TDCs. But there are latency issues with high resolution TDCs, especially with Vernier TDCs, and therefore require some trick to enable a shorter quantisation time. Of the two TDCs, the Coarse-Fine TDC has a high resolution of 1.08 ps, and a sampling frequency of 278 MHz and consumes a relatively lower power of 1.8 mW. The non-linearity parameters are about 1 LSB, rather comparable to other TDC architectures, and the area could be kept to just

0.01 mm², thanks to the compact design achievable by the digital-intensive nature of the TDC.

Although time-domain quantisation leverages on the faster switching speed of transistors, voltage-to-time conversion in the most primitive form of capacitive charge and discharge is very time consuming. This becomes a bottleneck in the quantisation speed of a time-mode ADC. Moreover, the non-linear and inverted voltage-delay relationship limits most time-mode ADCs to a very small input voltage range. Unlike analogue and digital data, time data cannot be stored. Its one-use only characteristic requires it to be regenerated for repeated use and consequently lengthening the quantisation cycle.

This research work first explores a new method of linearising the voltage-to-time relationship by the use of linear converters to correct the generated time output. The proposed concept of implementing a time quantiser in a feedback loop is able to linearise output delays up to 700 mV input range, whose linear range was limited to originally just 500 mV, or 100 mV in one of the reported works. Moreover, the inverse voltage-to-time relationship could be avoided with a special delay cell structure that was first proposed in the TDC-based VTC.

To further increase this linear input range, a novel idea of mapping data from one domain to another was proposed as a new methodology for voltage-to-time conversion. In this new concept, the input voltage is instead mapped onto a representative output delay, and with the TDC as a feedback element for delay correction, the same input to full scale ratio in both voltage and time domains is maintained for linear V-T conversion. This output delay is then quantised by the same TDC for a digital representation of the input voltage, i.e. two output modes in a single device. Therefore, this data converter is able to leverage on the digital-intensive nature of the TDC and utilises only very little analogue blocks to convert input voltage into output data in two domains.

With the proposed data mapping technique, it was possible to achieve an input voltage range that is 100% of the supply voltage. However, the presence of a feedback loop increases the number of iterations and therefore reduces the sampling frequency of the proposed VTC. Nevertheless, a small area thanks to a rather digital-intensive design could be achieved. This thus allows various

techniques used in digital designs to increase the sampling frequency for example pipelining, time-interleaving, etc.

List of Figures

Figure 1-1 Figure 1 1 Digital core with an ADC for interfacing with the analogue environment as presented in [19].....	20
Figure 2-1 Principle of time interval measurement as presented in [25].....	26
Figure 2-2 Structure of a Flash TDC	27
Figure 2-3 Operation principle of a Flash TDC [26]. Delayed START signals are sampled on the arrival of the STOP signal, resulting in a thermometer code at the outputs of the flip-flops.....	27
Figure 2-4 Structure of a Vernier TDC	29
Figure 2-5 Time-to-digital converter based on parallel scaled delay elements as presented in [19]	30
Figure 2-6 Structure of a pulse-shrinking element as presented in [34]	31
Figure 2-7 Multi-stage Pulse-shrinking TDC with flip-flop detection [41]	31
Figure 2-8 Principle of time interpolation by creating intermediate rising edges between two equivalent signals skewed by an inverter delay [43].....	32
Figure 2-9 Differential delay-line illustrating the principle of LPI-TDC as presented in [37]	33
Figure 2-10 (a) A differential delay element and (b) a differential sense amplifier as a midlevel crossing comparator [20].....	34
Figure 2-11 (a) A Time Amplifier (TA) element using an SR latch or MUTEX and (b) on that comprises of two MUTEXs (right) [45]	34
Figure 2-12 DLL-based Time Amplifier as presented in [32]	36
Figure 2-13 A CMOS TA using cross-coupled differential pairs as presented in [47]	37
Figure 2-14 Schematic diagram of a (a) dynamic Time Amplifier with single cross-coupling and (b) a modified dual cross-coupling as presented in [9]	38
Figure 2-15 A cross-coupled variable delay line Time Amplifier [54].....	38
Figure 2-16 Structure of a Vernier Ring TDC.....	39
Figure 2-17 A single-stage VRTDC as presented in [4].....	40
Figure 2-18 Schematic diagram of analogue Voltage-Controlled Delay Cells implemented with (a) a current source and sink in [15] and (b) with only a current sink in [3]	41
Figure 2-19 Effect of current starving on rise and fall times.....	42
Figure 2-20 Schematic diagram of (a) a gated VCDU and (b) a digitally controlled VCDU.....	42
Figure 2-21 A simple Delay-locked Loop (DLL)	43
Figure 2-22 A Half-Transparent D Flip-Flop [28].....	44
Figure 2-23 A DLL with a reference clock and non-periodic inputs presented in [28]	44
Figure 2-24 Delay cell with capacitive delay control via digital means in [33]	45
Figure 2-25 Various implementations of a VCDU based on the control of the current used for charging/discharging via (a) MOS capacitor [32] and (b) MOS resistor (diode-connected MOS) [34]	45
Figure 2-26 Digitally Controlled Oscillator implemented with tristate buffers [10]	46
Figure 2-27 A trans-linear loop current controller presented in [61]	47
Figure 2-28 A block diagram and timing diagram of a voltage-controlled ring oscillator [63] ...	48
Figure 2-29 Schematic of (a) the fall time current starved inverter circuit [64] and (b) half circuit of the VTC [65]	48
Figure 2-30 An illustration of a capacitive control VTC	49
Figure 2-31 (a) Illustration of a switched capacitor VTC and (b) a waveform showing its operation	50
Figure 2-32 VTC in [68] where a charge pump is used to modify the bias current to keep the discharge strength same for all V_{IN} values.....	51
Figure 2-33 (a) A source degeneration resistor R_D is used to linearise the discharge of C1 in [69] but cannot overcome the issue of different discharge strength for different V_{IN} values as shown in (b)	52
Figure 3-1 Illustration of the VRTDC core	56
Figure 3-2 Schematic of a multiplexed-inverter with a delay inverter (insert)	59
Figure 3-3 Schematic of (a) an arbiter and (b) a pulse generator implemented in the Vernier Ring TDC for phase detection.....	62
Figure 3-4 Transient simulation of arbiter A with a time interval of 3 ps between Si and Fi.....	63
Figure 3-5 A 5-bit counter using JK flip-flops	63

Figure 3-6 Schematic of the FAT tree encoder used with a built-in 1-out-of-N decoder, shown here as an example of the decoding with a thermometer code of 111111110000000	65
Figure 3-7 Flowchart of the data evaluation block	66
Figure 3-8 Schematic of a 15-input NOR gate	67
Figure 3-9 Graph of (a) arbiters 8-12 at the point of coincidence of START and STOP, (b) output of the output latch, schematic of (c) Ctr_stop generation, and (d) output latch	68
Figure 3-10 Top view of the VRTDC layout with its building blocks shaded in various colours	69
Figure 3-11 (a) Photo of the monolithic IC and (b) the test concept	70
Figure 3-12 Effect of PMOS gate bias voltage on cell delay and TDC resolution (without body bias)	72
Figure 3-13 Effect of NMOS gate bias voltage on resolution (with no body bias)	73
Figure 3-14 Effect of PMOS body bias voltage on resolution (with maximum Vsg)	75
Figure 3-15 Effect of NMOS body bias voltage on resolution (with maximum Vgs)	76
Figure 3-16 Four-dimensional voltage sweep of the gate biases versus TDC resolution	77
Figure 3-17 A comparison of gate bias combinations for D_{OUT} vs. T_{IN} up to 600 ps in 30 ps step	78
Figure 3-18 Four-dimensional voltage sweep of the body biases versus TDC resolution	78
Figure 3-19 Impact of 50 mV shift in NMOS body bias for a given set of gate and body biases	79
Figure 3-20 Variation of VRTDC output and resolution over temperature	80
Figure 3-21 Two-dimensional gate voltage sweep of C1 versus TDC output at -40°C	82
Figure 3-22 Two-dimensional gate voltage sweep of C1 versus TDC output at 125°C	83
Figure 3-23 Two-dimensional gate voltage sweep of C1 versus TDC resolution at 125°C	83
Figure 3-24 Variation of VRTDC output and resolution over supply	84
Figure 3-25 Variation of VRTDC resolution as a result of variation in cell delay change over supply	85
Figure 3-26 Two-dimensional gate voltage sweep of C1 versus TDC output at low Vdd	86
Figure 3-27 Two-dimensional body bias voltage sweep of C1 versus TDC output at low Vdd	87
Figure 3-28 Two-dimensional gate voltage sweep of C1 versus TDC output at high Vdd	88
Figure 3-29 Two-dimensional body bias voltage sweep of C1 versus TDC output at high Vdd	89
Figure 3-30 Latency and current consumption of the VRTDC in one quantisation cycle for time inputs of 90 ps and 1.636 ns	90
Figure 3-31 Peak and average Supply and Ground currents with respect to change in PMOS body bias over the Vdd range	93
Figure 3-32 Peak and average Supply and Ground currents with respect to change in NMOS body bias over the Vdd range	94
Figure 3-33 Average Supply and Ground currents with respect to change in both PMOS and NMOS body bias over the Vdd range	95
Figure 4-1 Simplified block diagram of the coarse-fine TDC (CFTDC)	100
Figure 4-2 Timing diagram of the coarse arbiter outputs for a T_{IN} equal to 136 ps	101
Figure 4-3 Flash-Vernier structure is used in the coarse TDC to obtain the desired resolution	103
Figure 4-4 Vernier structure is used in the fine TDC to obtain sub-gate CFTDC resolution	104
Figure 4-5 Implementation of the coarse TDC delay stage	110
Figure 4-6 Delay stage of the fine TDC using the Vernier principle	111
Figure 4-7 Implementation of the coupling circuit showing the buffer block and MUX network	112
Figure 4-8 An array of XOR gates is added prior to the FAT Tree Encoder to perform a logic subtraction of the coarse data output	115
Figure 4-9 Layout of the CFTDC with the main building blocks highlighted	116
Figure 4-10 Influence of gate and body biasing voltage on coarse TDC stage delay	120
Figure 4-11 Influence of gate and body biasing voltage on fine TDC stage delay	121
Figure 4-12 Zoom in view of the gate voltages that gives a CFTDC resolution of up to 1.08 ps	122
Figure 4-13 Two-dimensional gate bias sweep versus CFTDC resolution	123
Figure 4-14 Two-dimensional body bias sweep versus CFTDC resolution	123
Figure 4-15 Variation of TDC resolution with temperature	125
Figure 4-16 Change in coarse TDC resolution, t_c with gate bias sweep at 125°C	126

Figure 4-17 Further tuning to coarse TDC resolution, t_C with gate bias sweep at 125°C between 0.38 V and 0.39 V with marked out pass/fail points	127
Figure 4-18 Change in fine TDC resolution, t_{res} with body and gate bias sweep at 125°C	127
Figure 4-19 Change in fine TDC resolution, t_{res} with body bias sweep at 125°C between 0.9 V and 1 V with marked out pass/fail points	128
Figure 4-20 Change in coarse TDC resolution, t_C with gate bias sweep at -40°C with focussed tuning range marked in the red box and marked out pass/fail points	129
Figure 4-21 Change in fine TDC resolution, t_{res} with gate bias sweep at -40°C (with chosen V_{biasp} values marked in red box)	130
Figure 4-22 Change in fine TDC resolution, t_{res} with body bias sweep at -40°C with marked out pass/fail points	131
Figure 4-23 Varying change of coarse TDC resolution with body bias sweep over temperature	132
Figure 4-24 Varying change of fine TDC resolution with body bias sweep over temperature	133
Figure 4-25 Variation in TDC resolution with respect to voltage supply	134
Figure 4-26 Change in coarse TDC resolution, t_C with gate bias sweep at V_{ddlow} and V_{ddnom} (as reference) with marked out pass/fail points	135
Figure 4-27 Change in fine TDC resolution, t_{res} with gate bias sweep at V_{ddlow} and V_{ddnom} (as reference) with marked out pass/fail points	136
Figure 4-28 Change in fine TDC resolution, t_{res} with body bias sweep at V_{ddlow} and new V_{biasp} at 0.09 V (with marked out pass/fail points)	136
Figure 4-29 Change in coarse TDC resolution, t_C with gate bias sweep at V_{ddhigh} and V_{ddnom} (as reference) with marked out pass/fail points	137
Figure 4-30 Change in fine TDC resolution, t_{res} with gate bias sweep at V_{ddhigh} and V_{ddnom} (as reference) with marked out pass/fail points	138
Figure 4-31 Change in coarse TDC resolution with gate and body bias sweep under process variation with marked out pass/fail points	140
Figure 4-32 Change in fine TDC resolution with gate and body bias sweep under process variation with marked out pass/fail points	141
Figure 4-33 Periodic T_{IN} generating periodic reset signals which are used to reset the CFTDC digital circuits as shown by the return-to-zero behaviour of the outputs and fine TDC inputs. Also shown is the V_{dd} current profile of the CFTDC	142
Figure 4-34 Latency of the coarse and fine TDCs across the entire time input range	143
Figure 4-35 Quantisation time of the CFTDC versus input range for sets C1 and C2	144
Figure 4-36 Output characteristics of the CFTDC for the full input range	145
Figure 4-37 Output characteristics of the fine TDC for the full input range	146
Figure 4-38 (a) DNL and (b) INL of the proposed CFTDC of sets C1 and C2	147
Figure 5-1 The proposed concept is intended to fit the red curve to the linear blue line	155
Figure 5-2 Block diagram of the proposed TDC-based VTC	155
Figure 5-3 Simplified diagram of the dual-mode delay generator to illustrate the two modes	156
Figure 5-4 Concept of delay trimming with respect to TDC input	158
Figure 5-5 Timing diagram of the low pulses in TDC_start and TDC_stop (not drawn to scale)	160
Figure 5-6 Concept of up-down encoding by shifting D_{in} bits right and left respectively	161
Figure 5-7 Schematic diagram of two delay cells, each with two input digital bits	163
Figure 5-8 Low pulse generation for TDC input signals	165
Figure 5-9 Delay buffer used in the low-pulse generator	166
Figure 5-10 Timing diagram of the TDC output and V_{DAC} (not drawn to scale)	167
Figure 5-11 Timing diagram of the TDC output and V_{DAC} with an output latch (not drawn to scale)	168
Figure 5-12 Output Latch is implemented as an array of D flip-flops	168
Figure 5-13 Single cell structures for the first 30 cells in the left box and last 30 cells of the shift register in the right box	169
Figure 5-14 Implementation of the overflow detection scheme and the related timing diagram	170
Figure 5-15 Output delay versus input voltage of the delay generator with fully loaded varactors	172
Figure 5-16 Real versus ideal T_{IN} over entire V_{dd} range	172
Figure 5-17 Number of trim steps required to correct the offset between the real and ideal T_{IN} over entire V_{dd} range	173

Figure 5-18 Number of trim steps required to correct the offset between the real and ideal T_{IN} for a reduced input range	174
Figure 5-19 Adjusted T_{IN} in comparison to the original T_{IN} and ideal $T_{IN,ideal}$ versus input voltage	175
Figure 6-1 Simplified block diagram of the twin-mode Data Converter	184
Figure 6-2 Process flow of the quantisation concept of the proposed twin-mode Data Converter	185
Figure 6-3 Concept of coarse-fine trimming.....	187
Figure 6-4 Three cases that determine the criteria for coarse-fine switching	189
Figure 6-5 Concept of time delay generation by the two delay sub-blocks in the digitally controlled delay line	192
Figure 6-6 Timing diagram of the TDC.....	196
Figure 6-7 Schematic of the coarse-fine switch	199
Figure 6-8 Simplified diagram of the delay cell group used in the delay line.....	200
Figure 6-9 Simplified diagram of the Up-down Encoder	201
Figure 6-10 Schematic diagram of the comparator.....	202
Figure 6-11 Simplified diagram of the P-input pair comparator	202
Figure 6-12 Timing diagram of the self-reset comparator	204
Figure 6-13 A novel edge-induced reset signal generator	205
Figure 6-14 Timing diagram of the reset signal generator	206
Figure 6-15 Layout of the self-reset comparator	207
Figure 6-16 V_{DAC} resets to 73mV after every quantisation without a latch (black solid line) – diagram is not drawn to scale	208
Figure 6-17 (a) a section of the R-2R network with the switch and connected voltage nodes and (b) the layout implementation of the R2R DAC	209
Figure 6-18 The schematic implementation of the wide-swing constant transconductance bias circuit from [94] that is used to provide the voltage biases	210
Figure 6-19 Layout implementation of the wide-swing constant transconductance bias circuit with the dummy resistors for poly etching protection at the boundaries	210
Figure 6-20 Layout of the complete twin-mode Data Converter design with the building blocks highlighted	211
Figure 6-21 T_{IN} and $T_{IN,F}$ versus coarse and fine sub-block gate bias sweep from table 6-2.	213
Figure 6-22 Block diagram of the setup for delay line measurement	215
Figure 6-23 T_{IN} versus fine sub-block voltage bias of sets (a) C1 and (b) C2	216
Figure 6-24 T_{IN} versus coarse sub-block voltage bias of sets C1 and C2	218
Figure 6-25 D_{OUT} versus (a) fine sub-block and (b) coarse sub-block voltage bias sets C1 and C2 with marked pass/fail points	219
Figure 6-26 Bootstrapping the sampling switch M11 by fixing its V_{GS} voltage as presented in [95]	220
Figure 6-27 V_{DAC} follows V_{IN} for most of the input samples	222
Figure 6-28 Segment of the input sine wave showing how V_{DAC} is trimmed to every sampled- V_{IN}	223
Figure 6-29 A segment of V_{OUT} (output code generated with ideal DAC) versus V_{IN} after activated RDY flag	224
Figure 6-30 Digital output code versus V_{IN} of the proposed data converter	225
Figure 6-31 Differential Non-Linearity (DNL) of the proposed converter	225
Figure 6-32 Adjusted T_{IN} in comparison to the ideal $T_{IN,ideal}$ versus input voltage, with the digital output code.....	226
Figure 6-33 Adjusted T_{IN} versus input voltage for two smaller ranges	226
Figure 6-34 Power consumption of the proposed data converter during one iteration of a complete sampling period	227
Figure 6-35 Output spectrum using discrete fourier transform of the output data	228
Figure 6-36 Block diagram of the proposed VTC with additional comparator offset	234
Figure 6-37 Comparator offset vs. V_{DAC} and V_{IN}	235
Figure 6-38 Fine delay sub-block output versus gate and body bias at low V_{dd} condition	236
Figure 6-39 Full delay block output versus coarse gate bias at low V_{dd} condition	237
Figure 6-40 Fine delay sub-block output versus gate and body bias at high temperature condition	238
Figure 6-41 Full delay block output versus coarse gate bias at high temperature condition ..	239

Figure 7-1 (a) Concept of built-in delay generator for TDC measurement, (b) Implementation of the delay cell in the delay generator	245
Figure 7-2 Multi-stage concept to increase sampling speed	247
Figure 7-3 Time-interleaving concept with a shared single feedback element	248

List of Tables

Table 3-1 Table of gate bias combinations for the desired TDC resolution of 3 ps	77
Table 3-2 Voltage values for combination C3 of gate and body bias	79
Table 3-3 Voltage values for combination C1 of gate and body bias	80
Table 3-4 Two-dimensional voltage sweep (in red) for combination C1 of gate bias at -40°C.	81
Table 3-5 Two-dimensional voltage sweep (in red) for combination C1 of gate bias at 125°C	82
Table 3-6 Two-dimensional voltage sweep (in red) for combination C1_Vddlow of gate bias at low Vdd supply	86
Table 3-7 Two-dimensional voltage sweep (in red) for combination C1_Vddlow of body bias at low Vdd supply	86
Table 3-8 Two-dimensional voltage sweep (in red) for combination C1_Vddhigh of gate bias at high Vdd supply.....	87
Table 3-9 Performance comparison of the proposed VRTDC with various TDC schemes	91
Table 3-10 Body bias voltage sweep for combination C3 (marked in red)	92
Table 4-1 Table of gate and body biases to achieve the target CFTDC resolution.....	124
Table 4-2 Table of swept voltage parameters of the fine TDC at 125°C	126
Table 4-3 Final Gate and body bias set for T=125°C (with changed values marked in red) ..	128
Table 4-4 Table of swept voltage parameters of the fine TDC at -40°C.....	130
Table 4-5 Final Gate and body bias set for T=-40°C (with changed values marked in red) ...	131
Table 4-6 Table of swept voltage parameters of the CFTDC over temperature.....	131
Table 4-7 Table of swept voltage parameters of the fine TDC at Vddlow	135
Table 4-8 Final Gate and body bias set for Vddlow (with changed values marked in red)....	137
Table 4-9 Table of swept voltage parameters of the fine TDC at Vddhigh	138
Table 4-10 Final Gate and body bias set for Vddhigh (with changed values marked in red) .	138
Table 4-11 Table of swept voltage parameters of the coarse TDC under process variations	139
Table 4-12 Table of swept voltage parameters of the fine TDC under process variations	140
Table 4-13 Final Gate and body bias set under process variation (with changed values marked in red)	140
Table 4-14 Comparison of the proposed CFTDC against the state-of-the-art TDC techniques	147
Table 6-1 An overview of the input ranges versus supply voltage for various VTC schemes	179
Table 6-2 Table of swept voltage parameters of the delay line	212
Table 6-3 Table of swept voltage parameters of the fine delay sub-block of sets C1 and C2	215
Table 6-4 Table of swept voltage parameters of the coarse delay sub-block of sets C1 and C2	217
Table 6-5 Final gate and body bias voltages for sets C1 and C2	220
Table 6-6 Performance comparison with other time-domain ADC architectures.....	231
Table 6-7 Final gate and body bias for the delay generator at low Vdd	237
Table 6-8 Final gate and body bias for the delay generator at high temperature	239

1 Introduction

1.1 Motivation

A device used to measure a time interval defined between two timing events is called a time counter. When the time interval is converted to a digital code word, this device becomes a Time-to-Digital Converter (TDC). Precise measurements of time intervals are needed in many industries and applications, and the digital output is even more useful with the coming of digital age.

In Time-of-flight laser range finder applications [1-3], TDCs have always been a fundamental building block where distance is measured by counting time. In another form of time measurement, TDCs have been used to measure jitter for on-chip circuitry [4, 5]. Jitter is the deviation of the signals from their ideal position. Almost all digital circuitry has some amount of jitter and the tolerance of it varies according to applications. Other form of timing measurement includes use in Positron Emission Tomography Imaging [6, 7]. TDCs used in Automatic Test Equipment (ATE) are used to measure arrival time of selected events from the device under test to a test clock [8]. In all-digital PLL applications, TDCs are employed in place of phase detectors to compare the delay error between the feedback and reference clocks, and perform correction [9-12]. In RF frequency synthesizers [13, 14], TDCs are used to replace the conventional phase detectors and charge pumps, allowing the replacement of large capacitors in loop filters with simple digital filters. Industrial uses of TDC include Ultrasonic liquid flowmeter [15], and in the field of physics for single-photon counting [16] and particle detection [17].

As technology enters the deep-submicron process, the reduction of gate oxide thickness forces the supply voltages to go lower, to prevent dielectric breakdown. Relatively higher threshold voltages thus mean that the voltage headroom gets smaller. While voltages scale with technology, noise does not. This results in poorer signal-to-noise ratio, making it harder to resolve signals in the voltage domain with reasonable power consumption. However as technology scales, switching time of a MOSFET has improved, where rise and fall times are now in the order of tens of picoseconds [12]. Time-domain resolution of a digital signal

edge transition now proves to be superior to voltage-domain resolution of analogue signals. Leveraging on this advantage, it is apparent why TDCs become increasingly useful in data conversion. TDCs developed in the 1990s have resolutions in the nanoseconds range and the lowest reported are often hundreds of ps [17, 18].

But why is there a need for data conversion? In most systems, digital circuits make up the processing core because of their advantages in speed, area, portability and power as shown in figure 1-1.

Figure 1-1 Figure 1 1 Digital core with an ADC for interfacing with the analogue environment as presented in [19]

Digital circuits operate at higher speed, consume less power and have higher packing density due to reduced transistor size. All these advantages mean that cost can be reduced for the same functionality. On the other hand, analogue circuit parameters degrade with technology, and design becomes more difficult with decreasing supply voltages. The number of stacked transistors is also capped by the reduced supply voltage and the gain that can be achieved is consequently limited [20]. This negative impact on analogue characteristics has thus pushed for more mixed-analogue-digital designs, leveraging on digital circuits take over certain processes that were initially done by analogue means. However, information in the external world is always in the analogue domain, and in order for the digital core to process these information (sound, communication signals, etc.), Analogue-to-Digital Converters (ADCs) are needed as the interface circuits. Some applications where ADCs are required are in I/O ports, RF front-end, image sensor, music recording, etc. In voltage-domain ADCs, the smaller intrinsic voltage gain as a result of decreasing early

voltage, lower overdrive voltage and larger noise makes analogue design more challenging [21].

Several topologies for high resolution TDCs have been proposed over these years. Vernier TDC uses a concept to improve the resolution obtainable from a Flash TDC. Time amplification stretches time interval to improve resolution. Local Passive Interpolation allows resolution of 4.7 ps [22]. Two-step TDCs make use of two TDCs like in a two-step ADC to obtain sub-gate resolution. Each TDC has its own advantage and uniqueness, but latency, area, power consumption and dynamic range are some of the drawbacks of modern day TDCs.

However, in order for TDCs to perform data conversion, the output of preceding circuits has to be in time domain, i.e. TDCs alone cannot function as a data converter for the interface between the analogue world and digital processing circuits. Moreover, most circuits do not have time output as usable data, but only as an input data form. Until this is available in the future, a Voltage-to-Time converter (VTC) will always be required. In other words, voltage input shall be converted to time information which is then fed into a TDC for digital conversion.

The use of VTC-TDC structure in data conversion is also known as time-mode ADCs, an application for TDCs that has become increasingly popular. While a TDC enjoys the benefits of digital-intensive designs, including improvement in speed (and resolution) with advancing technology, ease of implementation, smaller area and potentially power consumption and to some extent re-configurability, a VTC that comprises of mostly analogue circuits, does not have these advantages. Traditionally, VTCs make use of Voltage-controlled Oscillators (VCO) to convert voltage to time, but the V-I conversion results in an inherent non-linear relationship between input and output of a VTC, limiting the input to a small range where the relationship between voltage and delay is relatively linear. While the linearity can be increased by analogue or digital means of correction, it still is a bottleneck in the performance of a VTC, and consequently in a time-mode ADC. Moreover, reduced supply voltage is also a problem in VTCs, as with most analogue circuits. Nevertheless, there is a potential to reduce the amount of analogue blocks in the VTC and maximise the benefits of the time domain quantisation.

Most voltage-domain ADCs, regardless of the used architecture, can achieve rail-to-rail input range. But in a Voltage-to-Time-to-Digital implementation of an ADC, the input range is determined by the capability of the VTC, whose delay output determines the requirements of the TDC with regards to resolution, conversion speed and number of bits. Depending on the architecture of the V-T concept, the input range may or may not rail-to-rail and it makes such a two-domain implementation disadvantageous. A relationship between conversion speed and time interval, and linearity and voltage range is illustrated in [23]. Essentially, the relationship between linearity and range is a trade-off, where good linearity requires small dynamic range. While the relationship is drawn for a delay-line based VTC, the same can be observed for other VTC architectures in the literature. We show in Chapter 5 a comparison of the various VTC schemes versus the input range with respect to the supply voltage. This limitation is never raised as an issue but in the application of Voltage-to-Time-to-Digital Converters, this is clearly a disadvantage.

1.2 Objectives

The research goal is to develop a new technique for time-mode analog-to-digital conversion, to provide an alternative to the traditional method voltage-dependent oscillation. The VTC should maximise the input voltage range with respect to the supply voltage. The TDC is required for delay quantisation and is expected to have performance characteristics that leverage on its highly digital nature for small design, i.e. short conversion time and high resolution achievable through advancing technology nodes.

1.3 Major Contribution of the Thesis

This research work introduces body-biasing, a technique that is well-established in circuit design, as a method of varying delay in a delay cell to achieve finer delay tuning for use in TDCs or delay generators to obtain the desired delay resolution. This body bias technique is added on top of the well-known Vernier principle in TDCs to obtain even finer delay difference between two delay cells. This technique is not limited to just time quantisers. In fact, in chapter 6, the

technique is used again for time generation, and characterisation results will show the usefulness of this extra bias voltage in not only achieving fine resolution, but also overcome influence of PVT variation.

It is also proposed in this thesis a method to improve the quantisation time of a high resolution TDC that is slowed down by latency. It was possible to reduce the Q-time by ten-fold by employing a two-step structure. By using a coupling circuit rather than a multiplexer network which is common in two-step structures, the transfer of residual time from the coarse to the fine stage could be done while minimising any additional delay or delay loss to the residual time, with which results in erroneous quantisation output.

This thesis also introduces an idea to linearise the voltage-to-delay relationship by enforcing the linearity through the use of linear converters, with the objective of maximising the linear input range useable for voltage-to-time conversion. The proof-of-concept was shown in the characterisation simulation results, where the original non-linear output delay with respect to input voltage could be linearised via the proposed delay trimming.

Finally, this dissertation contributes to the area of data conversion with a novel methodology of data mapping to perform voltage-to-time conversion and optionally also voltage-to-digital conversion. Through the proposed method, it was possible to overcome the limitation of the input range a result of the non-linearity nature of the voltage-time relationship, by increasing it to the full supply voltage. This technique is not specifically intended for and limited to any particular application, but can be used generally as a conversion technique.

1.4 Organization of the Thesis

The following chapter discusses with the study of different TDC architectures and a discussion of the pros and cons in their implementations. A brief introduction on the methods used in generating and varying delay in a delay cell is also included in this chapter. Finally, a short discussion on the voltage-to-time conversion techniques in the literature is given in the last section to give an overview of the available techniques.

Equipped with the background concepts, chapter 3 describes in detail on the proposed Vernier Ring TDC (VRTDC) with emphasis on transistor-level implementation for all the blocks of the proposed design. Examples are provided wherever possible for ease of understanding. This discussion is based on the presented paper “A 9-bit body-biased Vernier ring time-to-digital converter in 65 nm CMOS technology”.

Chapter 4 discusses the development of the Coarse-Fine TDC (CFTDC), an improvement over the VRTDC, with the main reason for the design upgrade attributed to the large latency of the previous design. The CFTDC was intended for use in the TDC-based Voltage-to-Time Converter. This is based on the presented paper “A 9-bit, 1.08ps resolution two-step time-to-digital converter in 65 nm CMOS for time-mode ADC”.

Chapter 5 describes the proposed idea of a TDC-based Voltage-to-Time conversion technique that is intended to linearize the voltage-delay relationship over a wide input range. The building blocks of the proposed design are discussed in detail on how the desired outcome and operating principle of the data correction method in this VTC concept is achieved.

Chapter 6 first introduces the novel concept of data mapping and its background and advantages over the current methods in the literature. The design of a twin-mode data converter is described in detail with emphasis on the concepts and circuit realisation of the building blocks, to present the implementation of the data mapping. This design is based fundamentally on the previous design albeit the different operating principles, and developed to overcome issue of non-linear voltage-time relationship and extremely slow quantisation time. In short, this design is proposed to convert data from the voltage domain into two other domains by a completely new concept.

A final chapter which gives a summary of the entire research work and recommendation for future research concludes this thesis.

2 Literature Survey

This chapter covers the literature study of the various architectures of TDCs and VTCs and also the implementation of delay cells which are the fundamental building blocks in both converter architectures.

2.1 Time-to-Digital Conversion techniques

The advantages of using TDCs with technology scaling have been mentioned in the previous section. The superior properties of a TDC can only be maximised if its circuitry is fully digital. Therefore, all the converter architectures reviewed in the remainder of this report are largely digital in nature.

2.1.1 Counter

The simplest technique to quantise a time interval is to count the number of clock cycles that fit into the interval to be measured. In order to increase the resolution per bit, a higher clock frequency is needed. This in turn increases the power consumption for clock generation. For example, to obtain a resolution of 100 ps, a 10 GHz clock is required. Moreover, above an achievable maximum frequency, even higher resolutions require the subdivision of one clock period. This is performed by a TDC and the resolution distinguishes a counter from a TDC [19]. Counters have been mistakenly called as TDCs albeit performing time-to-digital conversion such as in the case of (DC-DC Converters) and temperature sensor [24]. The coarse resolution obtainable from a counter is sufficient to meet the demands of the design. TDCs mentioned henceforth are restricted to time quantisers with resolutions of sub-nanoseconds.

The time interval to be measured is defined to be the time delay between a *START* and a *STOP* signal as shown in figure 2-1. It will be casual to say that the rising and falling edges are sharp. Real pulses have finite rise and fall times, and the decision (or threshold) point is assumed to be at the half- V_{dd} point. Although *START* and *STOP* signals are used throughout the thesis, it should be made known that it refers to the rising edge of the signal unless otherwise stated.

Figure 2-1 Principle of time interval measurement as presented in [25]

2.1.2 Flash TDC

Perhaps the most basic TDC architecture is the Flash TDC. Figure 2-2 shows the structure of the Flash TDC. In its ADC counterpart, a resistor ladder is used to create uniformly distributed voltage levels. A series of comparators connected to each voltage level is used to determine the input voltage nearest to distributed voltage level. In the time domain, the resistor ladder and comparators are replaced by a series of buffers and arbiters or flip-flops respectively.

The *START* signal is fed into the buffer delay line and each buffer will displace the *START* signal by an amount equal to its time delay. Each displaced *START* signal is connected to the input of the flip-flop and the *STOP* signal is connected to all the clock (*CLK*) inputs of the flip-flop in parallel. As the *START* signal propagates through the delay line, the *STOP* signal captures the flip-flop's input or the rising edge of the displaced *START* signal. This results in a thermometer code where all the delay stages that have already been passed will see a logic-1 value at the corresponding flip-flop output, and all the delay stages which not been passed by the *START* signal will see a logic-0 value.

In figure 2-3, the "1-0" point in the thermometer code indicates how far the start signal has propagated down the line before the *STOP* signal appears which a measurement of the time interval. As the structure of a Flash TDC suggests, it is a form of delay line based TDC. Also, inverters can be used instead of buffers, but the arbiters or flip-flops will have to detect rising and falling edges alternatively. An inverter-chain based Flash TDC was first employed in [12] to have a minimum propagation gate delay obtainable with limited area and for simplicity. Ideally, the resolution obtainable using inverter based Flash TDC is twice that of the implementation with buffers.

Figure 2-2 Structure of a Flash TDC

The advantages of a Flash TDC are its high speed operation, simplicity and fully digital circuitry. However, the resolution is limited to the delay of the delay element which is dependent on the technology used. Using inverters instead of buffers doubles the resolution but both implementations have limited dynamic range. The maximum time that can be measured is limited to $t_{DR} = n \cdot t_D$, where n is the number of delay elements with a delay of t_D . This can be solved if a loop structure is used which will be mentioned later in the section.

Figure 2-3 Operation principle of a Flash TDC [26]. Delayed START signals are sampled on the arrival of the STOP signal, resulting in a thermometer code at the outputs of the flip-flops

A Flash TDC that uses the inherent random offset of flip-flops to quantise the time interval is able to achieve higher resolution than most standard Flash TDCs [27]. However, each flip-flop has to be individually calibrated and the calibration using additive temporal noise makes the circuit and operation complex.

2.1.3 Vernier TDC

The highest resolution obtainable from a Flash TDC is limited to a gate delay which depends on the technology used. Applications that require sub-gate delay resolution will have to look into other implementations, and one of them is the Vernier TDC. The Vernier structure consists of 2 delay lines, one for the *START* signal and one for the *STOP* signal. Both delay lines have an equal number of delay elements. However, the delay elements in the *START* signal delay line have a delay t_{D1} that is larger than the delay t_{D2} in the *STOP* signal delay line. A flip-flop or arbiter in between each pair of delay cells as seen in figure 2-4 will capture the moment *STOP* signal catches up with *START* signal. The timing resolution is determined by the delay difference between the delay cells in the two delay lines and is given as:

$$t_{res} = t_{D1} - t_{D2} \quad (2.1)$$

The maximum time that can be measured is limited to:

$$t_{DR} = n \cdot t_{res} \quad (2.2)$$

where n is the number of delay cells [15]. Similar to a Flash ADC, it can be seen that if the dynamic range is large, a large area with long delay chains and large number of delay stages are required [14, 28]. Loop structure in the form of Vernier Ring or a two-level Vernier delay line [29] are solutions to this problem.

The *START* signal is fed into the top delay line and the *STOP* signal into the bottom delay line. Each buffer will displace the *START* and *STOP* signals by an amount equal to its time delay; t_{D1} and t_{D2} respectively. Each displaced *START* and *STOP* signal is connected to the input and the clock input of the flip-flop respectively. As the two signals propagate through the delay lines, the *STOP* signal eventually catches up with the *START* signal. At that very moment, the corresponding displaced *STOP* signal captures the flip-flop's input or the rising edge of the displaced *START* signal. This results in a thermometer code similar to how a Flash TDC will output one. Inverters can also be used instead of buffers, but the arbiters or flip-flops will have to detect rising and falling edges alternatively.

The advantages of a Vernier TDC are in its realisation of a sub-gate delay resolution and possible loop structure implementation for high dynamic range. High resolution also reduces quantization noise [30]. However, two delay lines are needed, and latency and conversion time increase. In order to implement different delay times using the same delay cell, the use of current starving inverters [3, 14, 15, 19] with or without the use of Delay-Locked Loop (DLL) [28, 30-32], capacitive delay control [33-35], tri-state buffers [36], and current control [37].

Figure 2-4 Structure of a Vernier TDC

2.1.4 Parallel Scaled Delay Elements TDC

Instead of connecting the delay elements in a series or cascaded form, configuring them in parallel gives a TDC based on parallel scaled delay elements as shown in figure 2-5. The *START* signal is applied to all the gates of the delay elements in parallel. When the *STOP* signal arrives, it clocks the delayed_*START* signal into the corresponding flip-flop. The delay of each element differs from the preceding element by a known delay t_D [33]. In other words, $t_{D,n} = t_{D,0} + n \cdot t_D$. The delay t_D is generated by sizing of the width of the transistors or scaling the load capacitances. Although the differential non-linearity that is caused by the static delay difference between elements is not accumulated as in the case of cascaded structures, loop structure is not feasible; limiting the dynamic range. The delay is susceptible to process, supply voltage and temperature (PVT) variations and careful layout is critical in ensuring the same added delay.

Figure 2-5 Time-to-digital converter based on parallel scaled delay elements as presented in [19]

2.1.5 Pulse-Shrinking TDC

The use of Pulse-Shrinking delay line was first mentioned in [18], followed by a TDC using such a principle in [38]. The reported time resolution was 780 ps using 1.2 μm CMOS technology. Over the decade, attempts have been made to improve the resolution with smaller device technologies [39, 40] and the latest reported resolution is at 6 ps [41].

The concept of pulse-shrinking is based on unequally sized inverters. The pulse to be shrunk is the time interval between the *START* and *STOP* signal. In a pulse-shrinking element as seen in figure 2-6, the falling edge (rising edge) is slowed down but the speed of the rising edge (falling edge) remains. When the signal passes through an adjacent inverter that is not modified, the slowed-down falling edge is inverted at the same speed as the rising edge, resulting in the reduction of the pulse width. The amount of reduction that determines the resolution of the TDC is the difference of the high-to-low and low-to-high propagation delays. One way to implement the inverter that slows down the falling or rising edge is by adding a third transistor in series to the PMOS or NMOS and vary its gate voltage to starve the current. Another method is to design the aspect ratio, making the loads of the inverters asymmetrical [41].

Figure 2-6 Structure of a pulse-shrinking element as presented in [34]

Like the Flash and Vernier TDC, the Pulse-shrinking TDC can be implemented in a linear or loop fashion. A linear pulse-shrinking TDC has the pulse connected to the *CLK* input of the flip-flop, as shown in [38]. The point that the pulse finally vanishes along the delay line with the pulse-shrinking element as the delay element is captured with a "1-0" transition in the thermometer code. A loop configuration in [39] uses a single-stage pulse-shrinking element that is looped continuously until the pulse disappears. A counter counts the number of loops the pulse has made before it finally disappears, giving an approximation of the pulse width or the measured time interval. Figure 2-7 illustrates a loop pulse-shrinking TDC presented by Yue et al.

Figure 2-7 Multi-stage Pulse-shrinking TDC with flip-flop detection [41]

A TDC that provides sub gate-delay resolution, the Pulse-shrinking TDC offers high dynamic range in a loop structure but careful design of the transistors are needed to create asymmetry and a minimum pulse width (measured time interval) that is detectable by the flip-flops is needed. Indication of the end of measurement is tricky due to the absence of the *STOP* signal.

2.1.6 Local Passive Interpolation TDC

Another technique to achieve sub gate-delay resolution is the Local Passive Interpolation TDC (LPI-TDC). Its principle, illustrated in figure 2-8, is similar to the voltage interpolation in an Interpolating Flash ADC. The *START* signal is delayed by one inverter, giving two logically equivalent signals with a skew of an inverter delay, T_{inv} in figure 2-9. In between these two signals are a number of signals corresponding to the Interpolation Factor (IF). In the case of figure 2-10, the IF is 4 of the looped LPI-TDC is 4. Since a standard CMOS delay cell cannot give one inverter delay, the delay cell is implemented as a differential delay element as illustrated in figure 2-10. The multiplexer selects the input of the delay cell to take in the signal from the feedback path or the TDC input. This is however, only applicable to the first delay cell. In order to maintain the same delay in all the cells, the same structure is used throughout with dummy signals connected to the unwanted ports. Other implementation in the form of tri-state inverter is presented in [42].

The rise time of a single stage CMOS gates is in the order of the gate delay with a skew of one inverter delay. Hence, the second signal starts to rise while the first signal is still increasing. The interpolated signals are parallel to the two equivalent signals only in the middle of the transition region which is also the threshold of the comparators sampling the delay line. The delay between each delay cells has to be small enough to measure intervals tightly [42].

Figure 2-8 Principle of time interpolation by creating intermediate rising edges between two equivalent signals skewed by an inverter delay [43]

Interpolation is done by resistive voltage dividers or diodes with reset transistors [44]. In order for the LPI-TDC to work well, the rise time of the delay elements must be much larger than the time constant caused by the parasitic capacitances in between two interpolation resistors [19]

$$t_{rise} \gg \frac{n}{2}(n+1)RC \quad (2.3)$$

Hence, for the interpolated signals to follow the two equivalent signals instantaneously, the resistor values have to be small enough. Moreover, high switching speed usually requires very low resistance values. On the other hand, small resistors give rise to large crossing currents. There will be a trade-off between good linearity and low power consumption. On the arrival of the STOP signal, the differential comparators that are connected to each pair of interpolated complementary signals (R_i , F_i) capture the state of the delay line. Prior to the rising edge, the comparator is in reset mode by pre-charging the two outputs (Q_i and QN_i) to V_{dd} .

Figure 2-9 Differential delay-line illustrating the principle of LPI-TDC as presented in [37]

The advantages of an LPI-TDC are its reduced latency and PVT variation effects on the delay line due to the monotonic interpolation structure. The only disadvantage is the careful layout design that will compromise between linearity and power consumption due to the cross current.

Figure 2-10 (a) A differential delay element and (b) a differential sense amplifier as a midlevel crossing comparator [20]

2.1.7 Time Amplifier based TDC

All the TDCs mentioned so far use narrow timing events to achieve sub gate-delay resolution. By stretching the time interval along the time axis and quantizing it with a TDC relaxes the resolution requirement of the TDC in use. The accuracy of time interval measurement can be improved using a time amplifier (TA) by an amount before the measurement [45] or as a residue from a coarse TDC in a two-step time quantization process [46-49]. Placing a time amplifier at the input of a delay line will give high resolution but in a limited measurement range. Also, it is difficult to control the gain over PVT variations [46, 50]. Many ways to implement a Time Amplifier have been reported. [45, 51] first suggested leveraging on the metastability in SR latches as illustrated in figure 2-11.

Figure 2-11 (a) A Time Amplifier (TA) element using an SR latch or MUTEX and (b) on that comprises of two MUTEXs (right) [45]

If the time interval between “signal” and “reference” is large enough (assuming that “signal” arrives first), the corresponding NAND gate goes to low and with the same amount of delay, the NAND gate connected to “reference” goes to low. Consider the case when the time interval is narrow enough such that while the “signal” NAND gate is switching when the signal goes above the threshold of the gate, “reference” arrives. The corresponding gate goes to low as well. But due to the cross-coupled connection of the two gates, there is a contention between which output goes high and which goes low. The closer the signals are to each other, the harder is the contention. This period of time is also the metastability of the latch. The TA that uses this contention period uses metastability to stretch the time difference between the input signals. Furthermore, the period of contention is dependent on the strength of the transistors in the latch. This results in an offset when adjusted, changes the linear range and gain based on the equation given in [51]

$$t_{out} = \tau \cdot \ln(t_{offset} + \Delta t_{in}) - \tau \cdot \ln(t_{offset} - \Delta t_{in}) \quad (2.4)$$

, where τ is the MUTEX time constant and Δt_{in} is the input time difference.

An improvement in the TA in [46] with the use of two inverters to realise higher offset and the addition of load capacitances to increase the gain as a result of increased offset. This new method saw a practical use in a TDC to measure timing jitter [5].

Using the phase-locking mechanism of the DLL (see figure 2-12), Chin-Hsin et al. sets the voltage to control the variable delay line to give an output pulse that is N times of the input pulse, where N is the number of delay cells in the line [32]. The amplified time output is given as

$$t_{out} = N \cdot \Delta t_{in} \quad (2.5)$$

The phase difference is measured between the first delay elements of both delay lines using a dynamic-logic phase frequency detector for better linearity.

Figure 2-12 DLL-based Time Amplifier as presented in [32]

Another method to obtain t_{out} , known as the pulse-train TA [47, 48] utilizes a chain of delay cells to duplicate the input pulse by N times. The N replica pulses are merged together using an OR-gate. One requirement is that the delay of each delay cell must be longer than t_{in} such that the replicas are not overlapped. The advantages of this TA are an integer gain and a wide input linear range. The gain of a pulse-train TA is N , the number of delay cells. In this work, the residue time is amplified, and not the input time pulse. The residue time is the output of a coarse TDC that is the first of a two-stage TDC, obtained by a series of multiplexers and NOR gates. The amplified residue time is quantized by another TDC (fine-TDC) implemented using any of the TDCs mentioned in this section.

So far the time amplification methods have been quite digital in nature, but the implementation of a TA in analogue domain is not non-existent. Differential difference amplifiers in unity gain buffer configuration and two identical operational amplifiers [49] are just some of the examples available. Changing the output common-mode voltage in [52] controls the time difference gain by varying the delay of voltage controlled delay cells. Oulmane and Roberts designed a time amplifier that cross couples two differential pairs and leveraged on the contention of the outputs as in the case of the SR-latch TA as illustrated in figure 2-13 [53]. Again, the input time difference cannot be too large, or else there would not be a time amplification as the switching of the second signal does not affect that of the first signal that has already switched during that long interval (input time difference).

Employing a more dynamic approach of a differential amplifier, the TA in [9] as illustrated in figure 2-14 uses discharging times of two intermediate nodes to determine the output time. This TA was utilized in a cyclic TDC [54] and in a digital PLL. The use of the top cross-coupling configuration is to have a positive feedback such that the discharging path via M2 (or M4) is strengthened by the discharging status of the opposite node, B (or A). The first transition makes the other transition slower by reducing the strength of the M2 (or M4) path, resulting in an amplified time difference. Similarly, the bottom cross-coupling is to control the discharging strength of M1 and M3 in the TA in figure 2-14(b). The minimum discharge path is guaranteed due to the weakly turned on M1 and M3, such that the time increment will not be saturated when the input time interval is increased. In the case of the TA in figure 2-14(a), the discharge path through M1 (or M3) is still strong due the V_{dd} -connected gate.

Figure 2-13 A CMOS TA using cross-coupled differential pairs as presented in [47]

Finally, the last implementation of a TA in the form of cross coupled variable delay line [55-57] amplifies the input time interval by putting the input signals through a chain of delay cells with two delay values (see figure 2-15). As the input signals start off from opposite ends and cross each other, the delay of the variable cells change and this increases the phase seen by the signal, consequently amplifying the time interval. The gain is decided by the ratio of the number of variable delay cells in each delay line. The delay of each cell is varied by a current starving transistor.

Figure 2-14 Schematic diagram of a (a) dynamic Time Amplifier with single cross-coupling and (b) a modified dual cross-coupling as presented in [9]

Note that the TA gain variation and offset can be compensated using digital calibration technique, and the linearity of the converter can be improved using an INL look up table.

Figure 2-15 A cross-coupled variable delay line Time Amplifier [54]

2.1.8 Ring Oscillator TDC

Although the time amplifiers may seem like a good solution to increase the resolution, they must be carefully designed for good gain and linearity.

In order to increase the dynamic range for fine resolution, a coarse-fine (2-step) TDC approach has been used where the residue is quantized by another TDC, thus relaxing the performance requirements of both coarse and fine TDCs. Residue is obtained usually by a multiplexer which is controlled by the comparator results (in the coarse TDC) [19] but results in some latency and metastability. Time-amplifier based TDC uses time amplification with or without coarse-fine quantization as mentioned earlier.

As mentioned earlier, a loop configuration can also increase the dynamic range. The Flash and Vernier TDC has the easiest structures to implement them in a loop. Since a sub-gate delay resolution requires an increase in TDC area with resolution, it is advisable to implement a Vernier TDC in a looped structure. The

advantage of a Vernier Ring TDC (VRTDC) is that the delay cells are reused for large time intervals measurement for fine resolution, smaller area and lower power consumption. Further to that, Integrated Non-Linearity (INL) increases with delay line length [30].

The idea first came about in 1994 where a 16-channel TDC was designed by Ljuslin et al. [17]. A delay chain is voltage-controlled using a DLL and upon the arrival of a HIT signal, the position of the “1-0” transition is loaded into a register. The signal at the end of the delay chain is fed back into a phase detector, such that the output and input phase difference is one clock cycle. Therefore, each clock cycle is divided by 16 for quantization. A counter connected to the end of the delay chain is used to extend the dynamic range of the TDC and thereafter, a data evaluation logic block gives the digital output of the measured time interval.

Figure 2-16 Structure of a Vernier Ring TDC

The operation of a VRTDC is no different from that of a Vernier TDC. Figure 2-16 shows the structure of a Vernier Ring TDC. Note that there is an inclusion of a multiplexer at the start of the delay line and a counter at the end. The *START* and *STOP* signals at the end of the delay lines are fed back into the start of the delay lines in a loop configuration. Consequently, there are two ring oscillators with one at a slightly higher frequency. The slow ring oscillator (SRO) is activated upon the arrival of the *START* signal, and the fast ring oscillator (FRO) by the *STOP* signal. Since the FRO has a higher frequency or smaller delay time per delay cell, the *STOP* signal eventually catches up with the *START* signal while looping through each individual oscillator. A counter connected to the SRO counts the number of loops passed by the *START* signal before *STOP*

signal arrives. A second counter connected to the FRO then evaluates the number of loops passed by *STOP* signal before it coincides with the *START* signal. The “*point of coincidence*” is captured by arbiters or flip-flops and a thermometer code of the arbiter outputs is generated. The resolution is calculated using equation 2.1.

Thus, a very fine effective resolution can only be obtained if the period difference and not the oscillation periods is small enough [58].

Since a counter is used to count the number of laps between the *START* and *STOP* signals, and the arrival of the *STOP* signal only triggers the Vernier action, the latency and conversion time is reduced in a VRTDC as compared to that of a linear Vernier TDC [19].

In order to eliminate the mismatch problem between the delay elements, an innovative one-stage Vernier Ring TDC was first introduced by [4] in figure 2-17 and further improved by [16, 34, 59]. Although the mismatch problem was eliminated due to a single cell ring oscillator, the oscillation periods were PVT sensitive and calibration was needed. Moreover, the input range was limited to T_s , the oscillation period of the coarse ring oscillator.

Figure 2-17 A single-stage VRTDC as presented in [4]

2.2 Variable Delay Cell

As mentioned earlier in the previous section, there are numerous ways to implement a delay cell. According to [60], there are three popular techniques for designing a variable delay cell; shunt capacitor technique, current starved

technique, and variable resistor technique. This section will introduce the various methods used in the literature to implement a variable delay cell.

2.2.1 Current Starving Inverters

By adding a transistor to the source of the PMOS or NMOS in an inverter, the current to the inverter is limited by the drain current of the current-starving transistor. The latter is more accurately known as a current source if it is connected to the source of the inverter PMOS or a current sink if it is connected to the source of the inverter NMOS. A voltage bias should be applied to the gate of the current-starving transistor to regulate the current.

Figure 2-18 Schematic diagram of analogue Voltage-Controlled Delay Cells implemented with (a) a current source and sink in [15] and (b) with only a current sink in [3]

This essentially is an analogue implementation of a Voltage-Controlled Delay Unit (VCDU). Figure 2-18(a) shows an example where current is starved at the power and ground side of an inverter [15]. A single current sink implementation as presented in [3] is also shown for comparison in figure 2-18(b). The difference between using a single current sink or source and both is in the rise and fall times. By starving or limiting the current, we are essentially increasing the rise and/or fall time of the output signal. A pictorial description is shown in figure 2-19. Suppose an input signal to the inverter makes a "0-1" transition. Without current starving, the output will go to *low* with a fall time depending on the size of the NMOS of the inverter. However, when a current sink is used to starve the inverter, the current is limited and the fall time increases. Similarly, a current

source will increase the rise time of the output signal when the input makes a "1-0" transition. When both current source and sink are used, a pulse is inverted with increased rise and fall time.

Digitally, current starving could be done with series current sources or sinks or a combination of both. Just by enabling and disabling the current source and/or sink, the delay can be adjusted [48]. Extending this concept to a digital codeword is an example in [14] where the current starving transistors are turned on by a combination of digital codes. The VCDU is replicated in the figure below. In both figures 2-18 and 2-20, the diode-connected transistors are connected in parallel to the current source and sink to linearize the transfer characteristics of the delay cell.

Figure 2-19 Effect of current starving on rise and fall times

Figure 2-20 Schematic diagram of (a) a gated VCDU and (b) a digitally controlled VCDU

2.2.2 Delay-Locked Loop

Delay elements are unfortunately susceptible to PVT variations and calibration is usually required, whether in the background or foreground. However, the use of delay-locked loop is necessary if calibration is not done.

The essential building blocks of a delay-locked loop (DLL) as illustrated in figure 2-21, are a chain of delay elements, a phase detector and a charge pump. Somewhat similar to a Phase-locked loop (PLL), a DLL replaces a voltage-controlled oscillator (VCO) with a charge pump. A phase detector could simply be implemented as an arbiter, with flip-flops or using half-transparent D flip-flops [28, 50, 61] (see figure 2-22) and a charge pump charges and discharges the capacitor whose voltage is used to control the propagation delay of the delay cells. The input signal that drives the delay line is compared with the signal at the end of the delay line by the phase detector which outputs a phase error. This error is fed into a charge pump and a control voltage is generated that adjusts the propagation delay for the delay cells; performing a corrective action to match the phases of the two signals. Usually, a low-pass filter follows the charge pump to filter out the high frequency components.

Figure 2-21 A simple Delay-locked Loop (DLL)

In order to control the propagation delay of the delay cells, the current-starving topologies mentioned in the previous section can be used. In some situations, delay has been tuned by supply voltages and the charge pump must therefore be designed to draw large currents. Hence, a low-dropout voltage regulator (LDO) would be more advantageous. Current-starving gives the advantage of capacitively loading the charge pump and reduces the overall power consumption [19]. Obviously with a single current source or sink, the tuning range is limited. In order to increase this range, more delay elements can be connected in parallel, or increase the capacitive loading of the delay elements.

Figure 2-22 A Half-Transparent D Flip-Flop [28]

However attractive a DLL may be, the input signal has to be periodic. Otherwise, the phases of the input signal and the delayed version at the end of the delay line cannot be locked. A periodic reference signal is thus required as seen in figure 2-23 below.

Figure 2-23 A DLL with a reference clock and non-periodic inputs presented in [28]

2.2.3 Capacitive Control

A delay cell controlled capacitively, shown in figure 2-24, was used as part of a Vernier ring oscillator in where the frequency of the ring oscillator was tuned by controlling the thermometer-coded capacitor bank, allowing a fine-tuning of the resolution when used with the Vernier principle.

The issue here is that there will be a 2^n increase in the number of delay cells and a 15 times increase in the number of capacitors for every n -increment of bits. The capacitor bank required can therefore be potentially very big or the number of bits obtainable from the TDC implementing this delay cell will be limited.

Figure 2-24 Delay cell with capacitive delay control via digital means in [33]

An alternative capacitive delay control presented in [32] is shown in figure 2-25(a). Here, the delay is adjusted by regulating the amount of current charging the capacitor. The variable delay has a linear dependency on the voltage V_C , for a voltage range of 0.8 to 1.2 V. The delay is adjustable from 50 to 360 ps, which is sufficient when used to offset from the nominal delay of 220 ps. The linearity is ensured by keeping the current sink in strong inversion.

A variant of this capacitive delay control is to charge and discharge the node of a MOSFET diode as shown in figure 2-25(b). Current is steered away from the diode to charge or discharge the inverter output node. Again by simulation results, the linearity is ensured when the transistor regulating the current is kept in strong inversion.

Figure 2-25 Various implementations of a VCDU based on the control of the current used for charging/discharging via (a) MOS capacitor [32] and (b) MOS resistor (diode-connected MOS) [34]

2.2.4 Tristate buffers

The delay cell in figure 2-25 can also be a tristate inverter where it is turned on or off by the principle of power gating. Header and footer transistors have been used for better linearity as compared to just a single header or footer. Power gating has been used in digital circuits for low voltage operation where cells are switched off when idle to save power. The same architecture is used in [10] but in a different way. Eight buffers are placed in parallel in each digitally-controlled oscillator (DCO) stage, and the odd number of stages allows the ring oscillator to oscillate. They have been replicated in figure 2-26 below. A frequency control turns on and off the buffers, varying the driving strength of each stage and hence configures the frequency of the DCO.

The advantages of this delay control method are the simplicity of implementation and the digital nature. However, when the number of stages increases, the number of inverters will increase much more. Also, the delay obtainable is of a multiple of one delay cell and limits the minimum resolution obtainable when used with the Vernier principle.

Figure 2-26 Digitally Controlled Oscillator implemented with tristate buffers [10]

2.2.5 Current Control

In the last implementation method of a delay cell, the current control method exploits the trans-linear relationship between current and delay. The idea was first presented in [62] and used in [37] as shown in figure 2-27. A delay line has poor linearity due to the inverse relationship between delay time and control current or voltage. With a trans-linear loop, the delay time was made proportional to the control current by using the reciprocal of the control current instead of the actual current. The relationship of the transistors is given as

$$V_{GS1} - V_{GS2} = V_{GS4} - V_{GS3} \quad (2.6)$$

And with the assumption that all the transistors are working in weak inversion, the above equation was rewritten as

$$I_y = I_1(I_2/I_x) \propto 1/I_x \propto t_R \quad (2.7)$$

By making I_1 and I_2 constant, a more linear relationship between propagation delay and control current can be achieved.

Figure 2-27 A trans-linear loop current controller presented in [61]

2.3 Voltage-to-Time conversion techniques

In order for the Time-mode ADC to work, it requires a VTC such that the voltage input is translated to time information that is useful to the TDC. The output pulse width is directly related to the magnitude of the input voltage. The most common and traditional method used is by means of a VCO. Other methods will also be explained in detail in this section.

2.3.1 Voltage-controlled Oscillator

In a VCO, the input voltage V_{IN} directly changes the delay of the delay cell. A typical ring VCO is shown in figure 2-28. The delay is controlled using the same techniques explained in the previous section. The problem with a VCO is the non-linear relationship between V_{IN} and delay output. This is because as the input voltage (gate voltage) increases from 0 to V_{dd} , the transistor that controls the amount of current in the delay cell goes through different operating regions. Each region has a different drain current versus on gate-source voltage characteristics and thus produces different charging/discharging time for the same output load. This results in a non-linear increment in pulse width for a linear increment in V_{IN} .

Figure 2-28 A block diagram and timing diagram of a voltage-controlled ring oscillator [63]

2.3.2 Current starving

Current starving is done in the same fashion as a variable delay cell. Na2 in figure 2-29(a) is the current sink with the gate connected to V_{IN} . A weak Na1 is there to provide a path from the source of Na3 to Gnd for low V_{IN} values that are not able to turn Na2 on. It is obvious from the circuit that only the fall time is deliberately increased by limiting the current in the inverter made up of Pa1 and Na3.

Figure 2-29 Schematic of (a) the fall time current starved inverter circuit [64] and (b) half circuit of the VTC [65]

A slight modification to the current starving VTC is the circuit is shown in figure 2-29(b), with M1 and M2 making up the inverter, M5 as the current sink and M9 providing the path from source of M2 to Gnd . M7 is added as a source degeneration transistor to linearize the delay versus input voltage relationship. Parallel transistors M9 and M13 are biased in subthreshold to increase the sensitivity of the VTC and to mitigate the compression of the pulse delay time

versus input voltage characteristic at high input voltages. The VTC works over an input range of 200mV with a sensitivity of 2.5 ps/mV. Mostafa et al. designed a VTC that uses the fall time and rise time current starved inverters together to increase linearity and reduce power consumption [64], and the input range obtained was 150mV with a sensitivity of 3.47 ps/mV. Macpherson et al. designed a VTC in 90 nm CMOS [66] that was later used in a time-mode ADC that worked in an input range between 220 mV and 320 mV, giving a tuning range of 50 ps.

As seen in the examples provided for the current starving technique for a VTC, the input range is limited for a linear output, mainly due to the limited range of input voltages for the same operating region of the current starving transistor. The advantage is in the gain (output delay per unit input voltage), which can be adjusted by means of an additional MOSFET capacitor as proposed by Macpherson et al.

2.3.3 Capacitive control

A possible implementation for the VTC is through the use of capacitance controlled by V_{IN} is shown in figure 2-30. This is almost similar to the variable delay cell method shown in figure 2-24. The capacitances are implemented with MOSFETs. However, the capacitors have nonlinear delay-to-voltage characteristic. As such, a VTC implemented by this technique can only be used with a TDC of modest resolution. Also, it is not commonly used in the literature.

Figure 2-30 An illustration of a capacitive control VTC

2.3.4 Switched-capacitance

In a switched capacitor VTC, a sampling capacitor is first charged to V_{IN} and subsequently discharged by a constant current source. The voltage on the capacitor V_{cap} is continuously compared with a reference voltage, such that when it is equal or less than V_{ref} , the comparator output toggles. Figure 2-31

illustrates the operation. A similar implementation is done by Choi et al. for a Time-interleaved ADC [67]. The output pulse width t_{pulse} is proportional to the input voltage V_{IN} and is given by the following expression

$$t_{out} = \frac{C \times (V_{in} - V_{ref})}{I} \quad (2.8)$$

, where C is the sampling capacitor and I is the value of the constant current source.

The comparator used could be any comparator. Min et al. suggested the use of a Threshold Inverter Quantization (TIQ) – based comparator [20], very popular in TIQ-based Flash ADCs. While an inverter cannot be used as a general purpose comparator, several stages of inverters when cascaded together can be used as a threshold detector if the input is ramp signal. The problem is that threshold voltages can be achieved by sizing but precise threshold voltages cannot be controlled and is susceptible to PVT variations.

Figure 2-31 (a) Illustration of a switched capacitor VTC and (b) a waveform showing its operation

While the capacitor-discharge method seems to be able to provide a linear delay to voltage relationship over a larger input range than the current starving technique, the challenge is to keep the output impedance of the current source large. This is so that a constant current drain from the capacitor can be maintained. As such, a current source is the ideal solution but not practically feasible. Although cascade topologies can increase output impedance, the limited voltage swing at the output of the current source is a drawback, apart from all the charge-sharing, clock feedthrough problems of a switch.

Huang et al. proposed the use of a charge pump together with a current source to achieve a specific time range regardless of PVT variations [68]. The charge pump is used to change the current source value such that for different V_{IN} values, the discharge graph is in parallel; i.e. they have the same gradient as illustrated in figure 2-32. A comparator that detects the crossing of the discharge past the threshold value generates a low-to-high STOP signal, and thus creating a pulse with a width proportional to the input voltage. At the start of the discharge, a START signal is generated. A TDC that utilizes START and STOP signals mentioned in the previous section can be used. Unfortunately, the results were simulated and no physical chip was done to prove the linearity.

Figure 2-32 VTC in [68] where a charge pump is used to modify the bias current to keep the discharge strength same for all V_{IN} values

Agnes et al. proposed a time-domain comparator that uses two VTCs and a flip flop [69]. The sampling capacitor $C1$ is first pre-charged to V_{dd} , and is discharged through a current starving transistor $M5$. Using a source degeneration resistor, R_D , they were able to linearize the ramp discharge curve of the sampling capacitor $C1$, see figure 2-33. However, due to the same problem as a current starving method, $M5$ does not exhibit the same behaviour across different V_{IN} values, and thus the gradients of the capacitor discharge curves are not the same for different input voltages. Hence the pulse width versus input voltage is not a common factor, which results in non-linearity. However, the source degeneration resistor increases the output resistance by an amount equal to R_D and can be used in replacement of an ideal current source.

Figure 2-33 (a) A source degeneration resistor R_D is used to linearise the discharge of C_1 in [69] but cannot overcome the issue of different discharge strength for different V_{IN} values as shown in (b)

3 A 9-bit body-biased Vernier Ring Time-to-Digital Converter in 65 nm CMOS Technology

3.1 Introduction

Several schemes for high resolution TDCs have been proposed over these years. Vernier TDC uses a delay-difference concept to improve the resolution obtainable from a Flash TDC. Time amplification stretches time intervals to improve resolution. However, the dynamic range and linear region is small, and the time gain is uncertain due to PVT variations. Local Passive Interpolation allows resolution of 4.7 ps [22] but careful design is required for a compromise between linearity of interpolated signals and cross currents. Two-step TDCs make use of two TDCs as in a two-step ADC to obtain sub-gate resolution but require time registers since time data cannot be stored. Each TDC has its own advantages and uniqueness, but latency, area, power consumption and dynamic range are of particular concern in modern day TDCs. The Flash TDC is perhaps the simplest and fastest TDC. However, its resolution is limited to a gate delay.

By leveraging on the delay difference (usually achieved by different gate biases) between two delay lines, the Vernier TDC enables the ability to have a high resolution that is determined by this delay difference, usually tending towards a sub-gate delay. This Vernier principle is used in a Vernier scale, and can be applied also in TDC architecture to enable very fine measurements. In order to increase the dynamic range of the Vernier TDC, the output of the last delay stage is connected back to the first delay stage. This ring configuration gives a Vernier Ring TDC (VRTDC) its name. To further increase the resolution of a VRTDC, introducing voltage bias to the substrate of the delay cells is proposed. The dependence of the propagation delay on body bias will be examined.

3.2 Body-biasing

The simplest way of changing the propagation delay of an inverter is to increase or decrease its size. However, this propagation delay is fixed by design and is limited by the technology used.

A signal passing through two regular inverters in parallel will ideally be inverted after x -ps, and the difference in propagation delay between the two gates (ideally) is 0 ps. By increasing the propagation delay of one inverter to be y -ps and keeping the other to be x -ps, a delay difference of $(y-x)$ ps can be obtained. In order to overcome the limitation of a single-gate delay, two identical cells (in functionality) can be used in parallel to obtain sub-gate delay. This is known as the Vernier principle.

In order to obtain the desired x and y delays, the transistors can be sized – this has already been mentioned. Alternatively, changing the bias current or voltage of the transistors can also modify the propagation delay. The proposed method of varying the propagation delay is therefore to limit the maximum (drain) current flowing through the inverter through the use of stacked transistors. These stacked transistors are given bias voltages at their gates to set the desired amount of current and consequently setting the desired propagation delay.

$$I_d = \mu C_{OX} \frac{W}{L} \left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2 \right] \quad (3.1)$$

The amount of delay that can be achieved with this method is far greater than by saying due to the limited amount of current that can charge and discharge the load capacitance. A longer discharge time via a stacked NMOS means that the output falling edge slope is made less steep. A longer charging time is achieved via a stacked PMOS for controlling the output rising edge slope.

However, gate biasing usually results in a very coarse setting of the current. Therefore, an extra set of voltage bias is added to the bulk terminal to modify the threshold voltage of the stacked transistor, which results in a finer alteration of the current. The use of body biasing is not unfamiliar in mixed signal circuit design. It has been used as a low voltage technique and for faster switching. Introducing a potential difference between the body and source changes the threshold voltage as such:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad (3.2)$$

Therefore, the body can be seen as an extra gate to change the characteristics of a transistor. This voltage bias can be provided externally or internally. By raising the source potential higher than the body potential, the transistor is forward body biased (FBB). The depletion region increases and hence V_{TH} increases. This makes the transistor slower but there is less leakage current. A reverse body bias ($V_S < V_B$) increases the speed of the transistor at the expense of leakage current. Although limited, there is also some leakage reduction when reverse body bias is used to raise the threshold voltage. Forward and reverse body biases have been used in sleep transistors, power saving through leakage reduction, delay and threshold voltage compensation. Body biasing can be done in mainly three ways; static, adaptive and dynamic body biasing.

Static biasing is simply providing a fixed voltage to the bulk while adaptive biasing provides an FBB or RBB to different transistors depending on its requirement. Dynamic body biasing changes the bias voltage throughout duration of the circuit operation. One example is where the bulk is shorted to the gate and it changes in accordance to the input signal [70].

3.3 Vernier Ring TDC (VRTDC) Concept

A VRTDC architecture is used in this work with the consideration on resolution, dynamic range and latency. Body-biased inverters are used as delay cells to construct the VRTDC. By connecting the output of the delay line to the input, a ring oscillator is constructed and an odd number of delay cells (henceforth known as delay inverters) are used to ensure the rings oscillate. Two Vernier rings with slightly different time periods ensure the TDC works in accordance to the Vernier principle. One ring is fed with a *START* signal and the other with a *STOP* signal. In order to allow the first delay inverters to receive *START* / *STOP* signal and the returning signal from the end of the ring, they have been re-configured into a multiplexed-inverter. The entire VRTDC comprises of a VRTDC core, a counter, a Thermometer-to-Binary Encoder and a Data Evaluation Block. An illustration of the VRTDC core is given in the figure below.

Initially, the inputs to the slow and fast rings are pulled to ground before quantisation starts. The multiplexed inverter is switched to take in the *START* and *STOP* signals. When *START* signal arrives, the slow ring is activated. The rising edge is inverted after the first delay inverter, t_s and becomes a rising edge again after 2 delays, $2t_s$. No measurement takes place until *STOP* signal appears in the fast ring. All digital circuits and logical outputs related to the slow ring will henceforth have the word "slow" in the terms and "fast" for that related to the fast ring.

Figure 3-1 Illustration of the VRTDC core

When *STOP* signal arrives, the fast ring is activated. Quantisation starts from this point onwards where the Vernier principle comes into effect. It works on the principle of using the alignment of two different scales to make a fine measurement. Because the slow and fast rings have different delays, the *STOP* signal eventually catches up with *START* signal – the instance at which is called the "*point of coincidence*". For this principle to work, *START* must be connected to the slow ring, and *STOP* to the fast ring. Until then, the number of laps passed by the *STOP* signal is recorded in the fast counter.

A chain of arbiters is connected in between the rings. Each delay inverter from the slow and fast ring will form an inverter pair and each pair will be connected to two arbiters. Since each inverter will see signals in opposite phases every cycle, the arbiters must be able to process not only a rising edge signal but also a falling edge signal. Hence, arbiters A and B are used to detect rising edge signals and falling edge signals respectively. Arbiters A1 and B1 will compare the rising and falling edges *S1* and *F1* (corresponding to outputs of the first delay inverters of the slow and fast ring respectively) respectively. *S1* is the inverted-delayed signal of *START* after the first slow delay inverter and *F1* is the inverted-

delayed signal of *STOP* after the first fast delay inverter. Since both *START* and *STOP* signals are rising-edge signals, *S1* and *F1* will be falling edges and will be compared by arbiter B1. Consequently, arbiter A2 will compare rising edges of *S2* and *F2*.

Note that there is no external reset signal to the VRTDC to reset the arbiters. In fact, a global reset signal does not make sense here. Every arbiter arbitrates the rising/falling edges at a different time instant as the *START* and *STOP* signals propagate down the ring. Therefore, each arbiter would require an individual and unique reset signal, so that they are ready to compare a new set of signals. With the possibility that the arbitration time is longer than the propagation delay of one round in the ring, the reset signals must come after a reasonable amount of delay. Hence, arbiters A1 and B1 will be reset by *S13*, arbiters A2 and B2 are reset by *S14*, and so on.

The *STOP* signal chases the *START* signal and eventually passes it after some time. When it finally does, it freezes the output of the arbiters and generates a thermometer code.

$$T_{in} = (15N_f + TH) \cdot (t_{res}) = N \cdot t_{res} \quad (3.3)$$

$$N = 15N_f + TH \quad (3.4)$$

, where T_{IN} is the measured interval, and N_f is the number of loops in the fast ring, and t_{res} is given by $t_s - t_f$. TH is the thermometer code generated from the outputs of the 30 arbiters to determine the exact location of the instance *STOP* overtakes *START*. N will give the total number of delay stages *START* has propagated through before being overtaken by *STOP*.

3.4 Circuit implementation

In this section, the circuit implementation of the various building blocks in the VRTDC is discussed in further detail.

3.4.1 Delay inverter

As mentioned earlier, the resolution of a VRTDC is the difference between the propagation delays of the delay cells of the slow and fast rings.

$$t_{res} = t_S - t_F \quad (3.5)$$

When inverters are used, the propagation delay of each cell can halved, and the resolution now becomes

$$t_{res}' = t_S' - t_F' = \frac{1}{2}t_S - \frac{1}{2}t_F \quad (3.6)$$

$$t_{res}' = \frac{1}{2}(t_S - t_F) = \frac{1}{2}t_{res} \quad (3.7)$$

The above equation shows the potential of using inverters in reducing the resolution by half when a buffer is used as a delay element and thus the implementation of inverter-based VRTDC rings in this design.

Since the delay chains are inverting, it is best to implement a header and footer current starving transistor to reduce the difference in rise and fall times of the output signal by enabling both edges to be varied. This also has the benefit of reducing the chance of a disappearing pulse width due to asymmetry in edge delay. The propagation delay of each delay inverter can be adjusted by an external voltage bias (V_P and V_N), which are applied to the gates of the current source M3 and sink M5 as in figure 3-2.

According to the Vernier principle, the resolution is determined by the difference in the propagation delay. If the difference could be reduced further, then the resolution can be pushed higher. Hence, the two more external voltage biases ($V_{P,bd}$ and $V_{N,bd}$) are introduced to the body of M3 and M5.

A negative source-bulk voltage reduces the effective threshold voltage. This shifts the crossing point of an inverter slightly from its middle point. As a result, with the same gate bias voltage at the current source and sink, there is a small difference in propagation delays between an inverter that is not body-biased and one that is, with the same gate bias. This gives the advantage of driving the resolution even higher and in total, four degrees of freedom in resolution adjustment. The only limitation due to body-biasing is the need for triple-well NMOS for the current sink. While a triple-well NMOS is approximately twice

larger than a normal NMOS, the area of the entire VRTDC is still relatively small. Diode-connected transistors M4 and M6 are aimed at linearizing the transfer characteristics of the delay cell.

In both rings, the first delay inverter has to take in two inputs, namely *START* (or *STOP*) signal and the recycled signal from the last delay inverter of the ring oscillator. The objective is to make sure that the first delay inverter will first see a rising-edge *START* (or *STOP*) signal going through it in the first cycle, a falling-edge signal in the next cycle, a rising-edge signal in the third cycle and so on. This is due to the odd number of delay inverters necessary to provide a 180° phase shift between the input and the output of the ring oscillator to keep it oscillating. The easiest method is through the use of NAND gate.

One input to the NAND gate is the rising-edge signal and assumed to be "high" indefinitely after the rising edge. The other input is the return signal from the end of the delay ring. When one input of the NAND is a "high", it becomes an inverter. So a falling edge signal coming in from the end of the delay ring will be inverted by the first delay inverter, keeping the oscillation. However, the NAND gate has to have the same delay difference as the other delay inverters. If the propagation delay was fixed and non-adjustable during the operation, this could have been made possible by sizing. Even so, the driving strength of the NAND gate and the load capacitance seen by the last delay inverter will be different as the other inverters.

Figure 3-2 Schematic of a multiplexed-inverter with a delay inverter (insert)

Hence, a multiplexed-inverter was proposed, as illustrated in figure 3-2. In the multiplexer, two inverters identical to the other delay inverters are used. One is for the input signal, and the other for the return signal. The control signals for the multiplexer is the delayed version of *START* and *STOP* signal for the slow and fast ring respectively, such that after the arrival of *START/STOP*, the delay inverter is automatically switched to receive input from the end of the ring. The concept is similar to power gating the delay inverters.

Caution must be taken not to increase the body bias too much so as not to exceed the V_{BE} of the intrinsic bipolar junction transistor between the body and source/drain of the MOSFET. The conduction of the intrinsic BJTs (when $V_{BS} > V_{BE}$) will result in latch-up.

3.4.2 Arbiters

In order to detect the early and late arrival of the edges, a comparator is needed at every stage. Usually, a D flip-flop is used. However, D flip-flops have a rather poor metastability performance which impacts the frequency noise shaping of the quantisation time error. While an SR latch before a D flip-flop is used to improve the metastability of the early-late detector [33], it comes at a cost of higher power and area. Hence, an arbiter with symmetrical topology has been considered [71] as illustrated in figure 3-3(a). In order to detect inverted signals at the same inverter pair, two arbiters are required for every pair; one to compare rising edges and the other for falling edges. Both arbiters A and B are similar in structure and are triggered by the edges. Each arbiter consists of a pulse generator (see figure 3-3(b)), reset circuit and a cross-coupled inverter. The arbiters can be reset globally by *Rst_e*, or locally by *Rst_i*, the output of a delay inverter.

Before any arbitration, the arbiter is reset globally. Transistors M7 and M8 pull nodes *a* and *b* to ground. This low node voltage turns on transistors M3 and M4. Assuming that *Si* arrives before *Fi*, a low pulse turns on M1, charging the source of M3 to *Vdd*, and through M3 charges up node *b*. At the same time, a rising node *b* voltage slowly weakens the turning on strength of M4 and turns on M6, pulling node *a* together to *Gnd*. This decreasing node voltage turns on M3 even more, driving node *b* quickly to a "1". The short duration to reach a stable state

is achieved by the cross-coupled inverters (M3/M5 and M4/M6) in action. A set of buffers that follow boost the output SA_i to V_{dd} , indicating that Si arrived first. Arbiter B works in the same principle. However, in order to reset the latter, Rst_i must be inverted as a falling edge signal will be the Si that will turn on the NMOS to pull nodes a and b to Gnd , resetting arbiter B. This is not a problem for arbiter A as the reset signals are rising edge signals. Figure 3-4 shows the transient response of the arbiter when Si arrives 3 ps before Fi . The low pulse is generated about 15 ps after the arrival of the signals and it takes about 140 ps for the arbiter to decide which signal arrived first.

FA_i is denoted as the *Ffirst* output of arbiter A and FB_i is the *Ffirst* output of arbiter B, where i is the arbiter number, corresponding to the inverter pair number. The two *Ffirst* outputs are the outputs that concern us more than the *Sfirst* outputs because we are looking for the instance *STOP* is earlier than *START*. That would mean that *STOP* has caught up with *START*, in accordance to the Vernier principle.

The pulse generator in figure 3-3(b) creates a pulse of a short time period upon the arrival of an edge. Without a pulse and when the arbiter is reset, there is a path from V_{dd} to Gnd resulting in short circuit current and a waste of power. This low pulse width is long enough to drive node a or b to a high value so that the correct output of the arbiter is driven high according to the input. The width of the pulse can be adjusted by the delay of the inverter chain; five inverters have been used here to create a pulse width of approximately 80 ps as seen in figure 3-4.

Figure 3-3 Schematic of (a) an arbiter and (b) a pulse generator implemented in the Vernier Ring TDC for phase detection

3.4.3 5-bit counter

In order to keep track of the number of loops passed by *STOP* signal, a counter is needed in the fast ring. The nature of the inverting delay chain requires the counter to be edge-triggered positively and negatively. An asynchronous counter using JK flip-flops has been designed, see figure 3-5. Each JK flip-flop is made with a D flip-flop and a few gates. To give the counter the ability to be triggered on both edges, the first JK flip-flop (corresponding to output E or LSB) is made dual-edge triggered. This is done by modifying the D flip-flop structure inside the JK flip-flop.

The counter is clocked by *F15* so that N_F can represent accurately the number of laps passed by *STOP* in the fast ring. The *J* and *K* inputs are tied together to

Ctr_stop for the fast counter. The detection of the coincidence of *START* and *STOP* signals will halt the count of the fast counter.

Figure 3-4 Transient simulation of arbiter A with a time interval of 3 ps between Si and Fi

Figure 3-5 A 5-bit counter using JK flip-flops

3.4.4 Thermometer-to-Binary Encoder

The encoder is implemented with a FAT tree encoder is illustrated in figure 3-6. Since the thermometer code from the flip-flop array is 15 bits long, the expected binary code should be 4 bits. An *AND*-array precedes the FAT tree encoder to identify the “100” point in the thermometer code.

The encoder is made up of only *OR* gates. All input nodes are separated from the output nodes by four stages of gates, creating some sort of pipelining effect without the use of registers. The circuit is digital and mostly symmetrical, and does not require a *CLK* signal and any flip-flops. A full static CMOS

implementation of the *OR* gates prevents leakage due to the stacking effect in its structure.

Each Q and $\bar{Q}$ output is named $Out-i$ and $Out-ib$, where i is the flip-flop number. For example, the first flip-flop will have two outputs, $Out1$ and $Out1b$, corresponding to the Q and $\bar{Q}$ outputs of the first D flip-flop. The thermometer code is '0' on the $Out1$ side and "1" on the $Out15$ side. From the point a bit in a thermometer code is "1", the subsequent bits are all "1". The signals $Out-i$ and $Out-ib$ will be explained later.

For now, they are treated as inputs to the encoder. It is obvious from the same figure that

$$LSB = a_0 + a_2 + a_4 + a_6 + a_8 + a_{10} + a_{12} + a_{14} \quad (3.8)$$

$$Bit1 = b_0 + b_2 + b_4 + b_6 \quad (3.9)$$

$$Bit2 = c_0 + c_2 \quad (3.10)$$

$$MSB = c_1 + c_2 \quad (3.11)$$

The array of 3-input *AND* gates is used as a 1-out-of-N decoder, to detect "100" in the input bits as well as for simple bubble error detection. Sometimes due to metastability, crosstalk and noise, an accidental "0" appears in a series of "1"s. For example if the thermometer code was 111010000, and only a 2-input *AND* gate was used for "10" detection, then there will be two "1"s in the input to the FAT Tree encoder, and the output will be erroneous.

Figure 3-6 Schematic of the FAT tree encoder used with a built-in 1-out-of-N decoder, shown here as an example of the decoding with a thermometer code of 1111111100000000

3.4.5 Data evaluation block

This block consists of a *Ctr_stop* generator, an *OR*-array and an output latch. It comes before the Thermometer-to-Binary encoder as seen in the flow chart in figure 3-7. To explain the operation of the data evaluation block, it is assumed that the *START* and *STOP* signals coincide at the 8th inverter pair with a rising edge.

Consequently, arbiter 8A will be the first to output a “1” at *FA8* because now *STOP* comes before *START*. Since the ring oscillators have not stopped, the arbiters continue to toggle between *Vdd* and *Gnd*, creating a train of pulses. After *START* and *STOP* passed the 8th inverter pair, they are inverted, and arbiter 9B detects a falling-edge *STOP* arriving before *START* and therefore outputs a “1” at *FB9*. This event is illustrated in the graph in figure 3-9.

In order to generate the *Ctr_stop* signal for the fast counter, two 15-input *NOR* gates figure 3-8 are used. One *NOR* gate takes in the 15 arbiter A inputs and the other the 15 arbiter B inputs. This is for quick detection of the moment of coincidence. Since the arbiter outputs are trains of pulses, they need to be latched such that a stable “1” or “0” can be used to be the J & K inputs for the fast counter. This *Ctr_stop* signal doubles as a clock signal for the output latch as will be explained later.

In the meantime when the lap count in the fast ring is frozen, the thermometer code has to be extracted to encode it into its binary form. Arbiters 8A and 8B will reveal the point of coincidence at the 8th inverter pair.

The information whether it was rising - or falling edged upon coincidence is not crucial, only the location is. Hence, both outputs from each arbiter pair are *OR*-ed together. The resulting 15 outputs from the *OR*-array are fed into the output latch for the same reason as in the *Ctr_stop* generator; to provide stable “1” or “0” signals for the Thermometer-to-Binary Encoder.

Figure 3-7 Flowchart of the data evaluation block

Figure 3-8 Schematic of a 15-input NOR gate

The output latch is made up of 15 D flip-flops clocked by a single signal, *Ctr_stop*. The output latch forces each arbiter pair output, $(FA+FB)_i$, to become a step-function as illustrated in figure 3-9. All the *Out-i* signals are “0” before the point of coincidence. *Out8* first goes to high and the subsequent *Out-i* signals until *Out7* follow suit with a delay shift. *Out-ib* (*Out-i* bar) is the inverse signal for *Out-i* which is necessary for the *AND*-array preceding the FAT Tree encoder.

Using an *OR*-array for the 30 arbiter outputs reduces the number of flip-flops required by half and reduces the number of signals to be processed at the output latch. It is evident now that *Ctr_stop* is a crucial signal that halts the fine counter as well as clocking the output latch at the correct moment, the moment of coincidence.

MSB is “1” through *AND*-8, then through *OR*-4, *OR*-11 and *OR*-15. The “10” point causes A8 to have all inputs (*Out6b*, *Out7b*, *Out8*) to be equal to ‘1’. This is clearly illustrated in figure 3-6.

For a “00” point at *Out6* and *Out7*, *AND*-7 will have inputs *Out5b*, *Out6b*, *Out7* equal to “1”, “1”, “0” respectively, and thus the output is “0”.

For a “11” point at *Out8* and *Out9*, *AND*-9 will have inputs *Out7b*, *Out8b*, *Out9* equal to “1”, “0”, “1” respectively, and thus the output is also “0”.

Figure 3-9 Graph of (a) arbiters 8-12 at the point of coincidence of START and STOP, (b) output of the output latch, schematic of (c) Ctr_stop generation, and (d) output latch

The 15-input *NOR* gate looks for the first instance of a “1” in its inputs which are the *First* outputs of the arbiters. With this implementation, a “1” in any of the inputs will pull *Out* to ground immediately. With any of the two *NOR* outputs at a “0”, the output of the *NAND* gate rises to a “1”, creating a bistable *Ctr_stop* required as mentioned earlier. In the latency period when the circuit is waiting for the moment of coincidence of START and STOP, the output of the *NAND* is always at a “0” since both outputs of the *NOR* gates are “1”.

3.4.6 Layout of the VRTDC

The layout of the VRTDC was done with the Global Foundries CMOS 65nm PDK, and is shown in figure 3-10, with the various blocks shaded in various colours. The two inverter rings are separated from each other to reduce the switching noise on each other. Between them are the two arbiter arrays, one for the rising edge and the other for falling edge detection. To the right of these four blocks is the data processing unit where it encompasses the two counters, a FAT Tree Encoder and an output latch. Some other reset and control circuitry fall under the “Other digital Logic” block.

Other than the delay cells which are half analogue-digital, the remainder of the VRTDC core is all digital circuit, allowing the design to be built in modules with “standard” cells, and achieve some form of compactness. Since the layout was drawn by hand, the density of inter-circuitry wiring could be alleviated by using place-and-route, or even synthesis.

The entire VRTDC measures only $173 \times 81 \mu\text{m}^2$. The drawback of body biasing is the use of a triple-well NMOS, which requires an extra N-well to separate the p-well from the p-substrate, so that a potential other than 0 V can be applied to the p-well of the NMOS. The triple-well requires has large spacing rules between two triple wells and between a triple well and N-well, which makes the inverter ring rather large. Fortunately, the triple well could be shared between two NMOS, since the N-well potential was the same, i.e. Vdd. Therefore the huge area could be avoided while adhering to design rules. The top level layout is shown in figure 3-10 below. The VRTDC core measures $173 \times 81 \mu\text{m}^2$.

Figure 3-10 Top view of the VRTDC layout with its building blocks shaded in various colours

3.5 Results and Discussion

The VRTDC was produced in silicon with GF 65 nm CMOS technology. A picture of the monolithic IC is shown in figure 3-11 (a) below, with a block diagram of the test concept in figure 3-11 (b). The VRTDC is highlighted in white in figure 3-11 (a), which shows that it is smaller than two adjacent pads. The idea of the test concept is to have a built-in delay generator which is made up of an inverter

chain with an independent bias voltage, V_{biasn_gen} . The input to the delay generator is a single rising edge signal, IN . From this signal, another TDC input signal $IN1$ is generated, according to the bias voltage V_{biasn_gen} . Both IN and $IN1$ are connected to the TDC as $START$ and $STOP$ respectively. Due to the limited number of pads, not all 9 output bits could be connected to a pad. Therefore, only 3 of the Thermometer-to-Binary Encoder and 2 of the Counter outputs have pads.

(a)

(b)

Figure 3-11 (a) Photo of the monolithic IC and (b) the test concept

Unfortunately, due to the fact that the delay generator itself cannot be verified for functionality, this TDC was not measured. Therefore, only simulation results of the VRTDC are discussed here with emphasis on the dependence of the TDC resolution on voltage biasing of the delay cells and the effect of supply voltage

and temperature variation on the resolution. Furthermore, results to the performance of the VRTDC are also shared in this section.

3.5.1 Effect of gate biasing

As shown in figure 3-2, two transistors alter the delay of each delay cell via the applied gate and body biases. The current source PMOS transistor M3 has a gate- and body voltage bias, V_P and $V_{P,bd}$, while the current sink NMOS transistor M5 has a gate- and body voltage bias, V_N and $V_{N,bd}$. We first explore the effect of V_P and V_N on the cell propagation delay and effective TDC resolution.

In figure 3-12, the effect of PMOS gate biasing is first investigated. V_N is fixed at 1.2 V that yields the maximum V_{gs} or minimum current limitation, and V_P is swept from 0 to 0.4 V. The orange line shows the delay change in 1 delay cell of *START* line, t_S versus V_{biasp} , the V_P of *START* line delay cells, and the grey line for the delay change per cell of the *STOP* line, t_F versus V_{biasp1} . Looking at both curves, increasing V_{biasp} (V_{biasp1}) increases t_S (t_F) delay, where a huge increment occurs from 0.25 V onwards. It is also evident that the delay vs. V_P change is somewhat exponential. Notice that for the same V_{biasp} and V_{biasp1} , the t_S and t_F values are never the same, this is because the T_{IN} of the VRTDC was set at 20 ps. The first conclusion is that decreasing the V_{sg} of the PMOS current source M3 increases the delay of the delay cells.

We look further at the effect of gate biasing on resolution, as shown by the blue curve. Negative delays can be observed on the y-axis. Recall that since the resolution of the VRTDC is determined by the difference in the delay between two cells, as intended with the vernier principle. The resolution t_{res} is therefore the difference of t_S and t_F , as mentioned in equation 3.5. Therefore, it is expected that for some gate biases, it is possible to obtain negative t_{res} , should the t_F be larger than t_S . While this is undesirable for the operation of the VRTDC, it is meaningful to be presented as an investigation of the dependency of the resolution on the gate voltage bias on both delay cells (lines).

Figure 3-12 Effect of PMOS gate bias voltage on cell delay and TDC resolution (without body bias)

An inverted exponential behaviour in the blue curve is seen the two-dimensional voltage sweep. This reflects the characteristics of t_F , albeit inverted, and is to be expected. To explain this observation, take $V_{biasp} = 0.4$ V and V_{biasp1} is swept up to 0.4 V. Since t_S is not influenced by V_{biasp1} , it remains flat but is large due to the V_{sg} of only 0.8 V. Also, t_F does not exceed t_S for V_{biasp1} voltages even up to 0.4 V. Given that t_{res} is the difference of t_S and t_F , t_{res} remains positive. On the other hand, take $V_{biasp} = 0$ V for comparison. Again, t_S is not influenced by the V_{biasp1} sweep and it remains flat. It is however observed that t_{res} becomes negative for the last 3 voltage points of V_{biasp1} , where t_F becomes larger than t_S with increasing V_{biasp1} and V_{biasp} at 0 V giving the lowest t_S .

All in all, notice that as V_{biasp} increases, t_{res} increases primarily due to t_S . However, if V_{biasp1} was increased together with V_{biasp} , t_{res} starts to decrease. Therefore, with a fixed V_N , it is possible to obtain a desired resolution by varying only both PMOS gate biases, where it has been shown that t_{res} is influenced by both V_P as a result of the vernier principle.

Further to that, it is also necessary to investigate the dependency of the resolution on NMOS gate bias. In this case, V_P was fixed at 0 V, which will yield

the maximum V_{sg} for the current source transistor M3. Similarly, V_{biasn} and V_{biasn1} are gate bias voltages to the transistor M5 in the *START* and *STOP* delay lines respectively.

The same observation to t_S and t_F can be made for V_{biasn}/V_{biasn1} variation. As the V_{gs} of M5 decreases due to decreasing V_{biasn} or V_{biasn1} , the respective cell propagation delay also decreases, with a huge change from 0.95 V and below, as shown in figure 3-13.

The same observation could also be done for t_{res} . At the lowest V_{biasn} of 0.8 V, t_S is at its maximum and t_F does not exceed t_S . As a result, t_{res} always stays positive. On the other hand, at the highest V_{biasn} of 1.2 V, t_S is at its minimum, and t_F exceeds t_S for V_{biasn1} less than 0.95 V. At the last three voltage points, t_{res} tends to negative. Therefore, a decreasing V_{biasn} increases t_{res} due to an increasing t_S , but a simultaneous decrease of V_{biasn1} pulls t_{res} towards 0 ps.

Figure 3-13 Effect of NMOS gate bias voltage on resolution (with no body bias)

3.5.2 Effect of body biasing

As elaborated earlier, the concept of body biasing does a finer tuning to the propagation of the delay cell as compared to the gate biasing. Again, we explore the dependency of t_{res} on $V_{P,bd}$ and $V_{N,bd}$ on both *START* and *STOP* delay lines. For this investigation, V_P and V_N of both delay lines are fixed at 0 V and 1.2 V respectively.

$V_{N,bd}$ shall first be fixed at 0 V which gives M5 no source-bulk bias. The source potential of M3 is fixed at Vdd and the body voltage is varied from 0.6 V to 1.2 V. The body bias voltages for *START* and *STOP* lines are called V_{bd_biasp} and V_{bd_biasp1} in figure 3-14 respectively. The influence of body bias on cell delay is first explained. The orange and grey curves represent t_S and t_F with V_{bd_biasp} and V_{bd_biasp1} variation. Unlike gate biasing, body biasing yields a more linear change in cell delay as observed by the two curves. Similar to gate bias, t_S increases with increasing V_{bd_biasp} , and the same could be observed for t_F with V_{bd_biasp1} . A decreasing V_{bd_biasp} means that the source potential is higher than the bulk potential, or a reverse body-bias, which decreases the threshold voltage of M3 as described in equation 3.2. Note that the equation is valid for NMOS, thus for PMOS, the sign of the V_{SB} and $V_{TH(0)}$ must be observed. This results in a decreasing propagation delay of the current-starved inverter, as proven in this investigation.

How do we ensure that $|V_{bs}|$ does not exceed BJT forward bias? This is elaborated at the end of this section.

By observing the gap between t_S and t_F , it is apparent that an increment in t_{res} occurs with V_{bd_biasp} , while a decrement in t_{res} occurs with a simultaneously increasing V_{bd_biasp1} .

Note that the change in t_{res} is in the range of 4 ps as compared to gate bias voltage change in figure 3-12, which gives approximately 10 times as much change. This affirms that body biasing provides a much finer tuning capability than gate biasing.

Figure 3-14 Effect of PMOS body bias voltage on resolution (with maximum V_{sg})

It would appear that the lowest t_{res} obtainable for the given gate biases is by giving *START* line delay cells the maximum source-bulk voltage possible and *STOP* line delay cells none. This trend shall also be observed for the NMOS body bias investigation.

Figure 3-15 shows the dependency of t_{res} on $V_{N,bd}$ of M5. Both $V_{P,bd}$ are fixed at 1.2 V, giving no source-bulk potential to M3. *START* line delay cells have body bias voltage V_{bd_biasn} and *STOP* delay cells V_{bd_biasn1} . Again, an increasing V_{bd_biasn} yields an increasing reverse bias of the source-bulk potential of M5, which results in reducing t_s . The same is observed for V_{bd_biasn1} and t_f .

By calculating the difference of t_s and t_f , t_{res} is plotted against a two-dimensional variation of V_{bd_biasn} and V_{bd_biasn1} in blue in figure 3-14. A linear saw-tooth relationship is observed as in the case of PMOS body bias. Increasing V_{bd_biasn} increases the source-bulk voltage and reduces the propagation delay of the cell. Similarly, increasing V_{bd_biasn1} simultaneously gives rise to an opposite effect.

Figure 3-15 Effect of NMOS body bias voltage on resolution (with maximum V_{gs})

3.5.3 TDC resolution

By using various combinations of all gate and body biases, it is possible to obtain the desired resolution, which is 3 ps. But to determine the body biases, the gate biases which play a huge role in determining the approximate t_{res} must first be decided. For that, a four-dimensional voltage sweep of all gate biases was done from 0 to 0.6 V and 0.6 V to 1.2 V for V_P and V_N respectively. Figure 3-16 shows the results of the voltage sweep. A V_P higher than 0.6 V and V_N lower than 0.6 V makes no sense due to the large t_{res} obtained as a result of very small $|V_{gs}|$, which cannot be tuned by body bias.

Therefore we limit the V_P and V_N to 0.3 V and 0.9 V respectively and perform a further voltage sweep with a finer step size. It was then possible to obtain multiple combinations of gate biases that could give single digit t_{res} , and for the purpose of illustration, four combinations are tabulated in Table 3-1 to show the various gate bias values. In the voltage sweep of this smaller voltage range, a 5 mV step change was used as compared to the 200 mV step earlier.

Figure 3-16 Four-dimensional voltage sweep of the gate biases versus TDC resolution

Table 3-1 Table of gate bias combinations for the desired TDC resolution of 3 ps

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1	0	0.195	1.2	1.095
C2	0	0.19	1.2	1.09
C3	0	0.19	1.2	1.095
C4	0	0.195	1.2	1.1

In order to illustrate the difference the gate biases make, a sweep of the input delay, T_{IN} was done from 30 ps to 600 ps in 30 ps step with all four combinations and plotted against the digital output of the TDC, D_{OUT} . The result is shown in figure 3-17. A resolution of 3 ps shall mean that every 30 ps step corresponds to 10_{10} shift in D_{OUT} .

It is evident from the figure that some offsets exist between various combinations and also to the ideal D_{OUT} . However, the body bias can and is intended to fine tune t_{res} to remove this offset. This is shown in figure 3-18 below where another four-dimensional voltage sweep on the body bias was done with a 100 mV step change. Recall that the influence of body bias is smaller in

comparison to gate bias, and a small step will not be meaningful to bring about much change to t_{res} .

Figure 3-17 A comparison of gate bias combinations for D_{OUT} vs. T_{IN} up to 600 ps in 30 ps step

Figure 3-18 Four-dimensional voltage sweep of the body biases versus TDC resolution

Finally, the complete gate- and body-bias combination could be determined as follows:

Table 3-2 Voltage values for combination C3 of gate and body bias

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C3	0	0.19	1.2	1.095
Combination	V_bd_biasp (V)	V_bd_biasp1 (V)	V_bd_biasn (V)	V_bd_biasn1 (V)
C3	1.2	1	0.6	0

The chosen combination C3 was chosen for a sweep of the T_{IN} versus D_{OUT} . For the purpose of showing the impact of body bias, two values of V_bd_biasn voltages were used for this input delay sweep. The determined V_bd_biasn of 600 mV was compared with 550 mV and the results are shown in figure 3-19.

The orange curve which has a V_bd_biasn of 600 mV has a smaller t_{res} value than for 550 mV (the blue curve). Therefore, the dynamic range of the VRTDC with the former value is smaller for the same number of output digital bits, which is about 81 ps, and reaches maximum D_{OUT} first.

Figure 3-19 Impact of 50 mV shift in NMOS body bias for a given set of gate and body biases

3.5.4 Temperature variation on resolution

The impact of temperature variation on the VRTDC is investigated in this section. The room temperature of 27°C was used for the earlier investigation on voltage biases. How will the t_{res} vary across the temperature range? For this investigation, combination C1 is taken as an example. The voltage biases are shown as follows:

Table 3-3 Voltage values for combination C1 of gate and body bias

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1	0	0.195	1.2	1.095
Combination	V_bd_biasp (V)	V_bd_biasp1 (V)	V_bd_biasn (V)	V_bd_biasn1 (V)
C1	1.2	1.2	0.02	0.01

Figure 3-20 shows the impact of temperature on D_{OUT} and t_{res} , for a T_{IN} of 90 ps. The supply voltage was fixed at the nominal 1.2 V. D_{OUT} is represented by the blue curve and the orange curve is the number of counts by the counter in the VRTDC.

Figure 3-20 Variation of VRTDC output and resolution over temperature

The grey curve shows t_{res} , where it is at the highest at 125°C and lowest at -40°C. This trend corresponds to that of the D_{OUT} curve, where the highest value

is obtained at low temperature and the lowest value at high temperature. The variation of t_{res} is also smaller between room and high temperature, as compared to the colder temperature range. This difference in variation is also seen in D_{OUT} . With regards to the counter output, the value does not change much, which is to be expected since t_{res} does not vary too much. At -40°C , the resolution is small enough, about 2.7 ps to force the counter count to 3, which otherwise should be 2.

We then take the minimum and maximum temperatures and attempt to calibrate the VRTDC via the voltage biases such that the t_{res} is tuned back to the desired value. However, this should be observed via the D_{OUT} since t_{res} is not measurable. For record purposes, D_{OUT} at -40°C and 125°C are 57_{10} and 21_{10} respectively. This means that the resolution at low temperature must be increased, and that at high temperature must be reduced.

3.5.4.1 Low temperature calibration

The gate bias voltages are first modified to achieve the D_{OUT} at room temperature, which is 31_{10} . Recall from the voltage bias investigation, in order to increase the t_{res} , Vbiasp should be increased and Vbiasn should be decreased. Alternatively, Vbiasp1 could be reduced towards 0 V, and Vbiasn1 could be increased towards 1.2 V.

A two-dimensional voltage sweep of Vbiasp and Vbiasn is performed from 0 to 0.4 V and from 0.8 V to 1.2 V respectively in 50 mV step, with emphasis on D_{OUT} . The results are presented in figure 3-21, where the initial D_{OUT} is circled in red. As Vbiasp increases or Vbiasn decreases, D_{OUT} decreases in varying amounts. A decreasing D_{OUT} represents an increasing t_{res} . It is possible to obtain 31_{10} by just increasing Vbiasp by 50 mV and keeping Vbiasn at 1.2 V.

Table 3-4 Two-dimensional voltage sweep (in red) for combination C1 of gate bias at -40°C

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1	0 -> 0.4	0.195	0.8 -> 1.2	1.095

Figure 3-21 Two-dimensional gate voltage sweep of C1 versus TDC output at -40°C

3.5.4.2 High temperature calibration

Recall from the voltage bias investigation, in order to decrease the t_{res} , Vbiasp should be decreased and Vbiasn should be increased. However, both are at the minimum and maximum values, and thus Vbiasp1 and Vbiasn1 should be modified instead. The former should be increased and the latter should be decreased. Vbiasp1 is varied from 195 mV to 295 mV, and Vbiasn1 is decreased from 1.09 V to 1 V, both in 10 mV steps.

Table 3-5 Two-dimensional voltage sweep (in red) for combination C1 of gate bias at 125°C

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1	0	0.195 -> 0.285	1.2	1 -> 1.09

The change in D_{OUT} with the voltage variation is shown in figure 3-22 below. The huge variation in D_{OUT} from 245 mV onwards seems to be a result of the trend in t_{res} towards a negative value, as shown in figure 3-23. To obtain the ideal D_{OUT} , there exists as illustrated by the orange points in figure 3-22, five possibilities.

Figure 3-22 Two-dimensional gate voltage sweep of C1 versus TDC output at 125°C

Figure 3-23 Two-dimensional gate voltage sweep of C1 versus TDC resolution at 125°C

3.5.5 Supply variation on resolution

The impact of voltage supply variation on the VRTDC is investigated in this section. How will the t_{res} vary across the supply range? For this investigation, combination C1 is also taken as an example.

Figure 3-24 shows the impact of voltage supply on D_{OUT} and t_{res} , for a T_{IN} of 60 ps. The supply voltage was varied between 1 V and 1.4 V, with the nominal supply at 1.2 V. Again, D_{OUT} is represented by the blue curve and the orange curve is the number of counts by the counter in the VRTDC. The grey curve shows t_{res} , where it is at the highest at 1.2 V and lowest (negative) at 1 V. However, the supply voltages of 1 V was too low such that D_{OUT} was too high to correct with via voltage bias. For that reason, the lowest voltage for the range was set at 90% of the nominal value, or 1.08 V. With reference to table 3-3, the PMOS body biases and one of the NMOS gate bias are at the nominal supply. When the supply voltage is varied, these voltages are adjusted accordingly such that they take this new value. In the case of Vbiasn1 where the gate bias is larger than the varied supply voltage, the latter shall be used instead. Within the defined range of 1.08 V to 1.4 V, the t_{res} trend corresponds to that of the D_{OUT} curve, where a parabolic behaviour can be observed.

Figure 3-24 Variation of VRTDC output and resolution over supply

As the supply increases beyond the nominal supply, the $|V_{gs}|$ of M3 and M5 also increases, reducing the t_{res} further. In figure 3-25, the gap between t_S and t_F in blue and red respectively appears to be the widest at the nominal supply. As the supply decreases below the nominal supply, the decreasing t_{res} could be a result of smaller increment in t_S as compared to t_F , since the $|V_{gs}|$ of t_F cells is smaller than that of t_S cells.

Figure 3-25 Variation of VRTDC resolution as a result of variation in cell delay change over supply

We then take the minimum and maximum supply values and attempt to calibrate the VRTDC via the voltage biases such that the t_{res} is tuned back to the desired value. Again, the D_{OUT} is observed at 1.08 V and 1.4 V supply are 37₁₀ and 41₁₀ respectively. This means that the resolution at both conditions must be increased.

3.5.5.1 Low Supply Voltage calibration

In order to increase the t_{res} , V_{biasp1} and V_{biasn1} should be increased and decreased respectively, with the other two gate biases kept the same. V_{biasp1} was increased from 0.1 V to 0.5 V in 50 mV step, and with a 5 mV step between 0.15 V and 0.2 V. On the other hand, V_{biasn1} was reduced from 1.08 V to 0.95

V in 10 mV step, and further down to 0.6 V in 50 mV step. This is tabulated in table 3-6 below.

Table 3-6 Two-dimensional voltage sweep (in red) for combination C1_Vddlow of gate bias at low Vdd supply

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1_Vddlow	0	0.1 -> 0.5	1.08	0.6 -> 1.08

As shown in figure 3-26, there exists twelve possibilities to achieve D_{OUT} of ± 1 LSB, marked in orange dots. Furthermore, there is the possibility of using body bias to further fine tune this accuracy. Therefore, we need to first select the desired gate biases, and this is marked in the red box in figure 3-26. Then the body biases are varied in two dimensions (as shown in table 3-7).

Table 3-7 Two-dimensional voltage sweep (in red) for combination C1_Vddlow of body bias at low Vdd supply

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1_Vddlow	0	0.175	1.08	1.06
Combination	V_bd_biasp (V)	V_bd_biasp1 (V)	V_bd_biasn (V)	V_bd_biasn1 (V)
C1_Vddlow	1.05 -> 1.08	1.08	0.02 -> 0.05	0.01

Figure 3-26 Two-dimensional gate voltage sweep of C1 versus TDC output at low Vdd

In order to confirm the efficacy of the body bias sweep, two more T_{IN} values are simulated, and the final body bias combination that can achieve the target D_{OUT} for the corresponding T_{IN} values is marked in the red box in figure 3-27 below.

Figure 3-27 Two-dimensional body bias voltage sweep of C1 versus TDC output at low Vdd

3.5.5.2 High Supply Voltage calibration

In the case of high supply voltage, the t_{res} also has to be increased, which again could be done by just increasing and decreasing Vbiasp1 and Vbiasn1 respectively. As shown in table 3-8, Vbiasp1 was increased from 0 to 0.2 V in 50 mV step, and with a 10 mV step up to 0.3 V. On the other hand, Vbiasn1 was reduced from 1.4 V to 1 V in 50 mV step, with a finer step of 10 mV between 1.2 V and 1.3 V.

Table 3-8 Two-dimensional voltage sweep (in red) for combination C1_Vddhigh of gate bias at high Vdd supply

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1_Vddhigh	0	0 -> 0.3	1.4	1 -> 1.4

As compared to figure 3-25, there are more combinations that is able to achieve D_{OUT} of +/- 1 LSB, (marked in orange dots in figure 3-28). Again, we want to

check the effectiveness of body biasing to increase the accuracy. Hence, the gate biases marked in the red box were chosen, and reiterated in table 3-9.

Figure 3-28 Two-dimensional gate voltage sweep of C1 versus TDC output at high Vdd

Since the D_{OUT} was already at the target value, the body biases were not varied too much from the original values at nominal supply. Also, other T_{IN} were tested for confirmation. A single sweep of V_{bd_biasn} was necessary.

Table 3-9 Two-dimensional voltage sweep (in red) for combination C1_Vddhigh of body bias at high Vdd supply

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C1_Vddhigh	0	0.27	1.4	1.28
Combination	V_bd_biasp (V)	V_bd_biasp1 (V)	V_bd_biasn (V)	V_bd_biasn1 (V)
C1_Vddhigh	1.4	1.4	0.02 -> 0.1	0.01

The results of the body bias sweep at high Vdd is shown in figure 3-29 below, with the three target D_{OUT} values for the corresponding T_{IN} marked out in red.

Figure 3-29 Two-dimensional body bias voltage sweep of C1 versus TDC output at high Vdd

3.5.6 Performance comparison

The VRTDC was designed to achieve a resolution of 3 ps. A full-scale T_{IN} sweep has already been presented in figure 3-19.

To check the time taken for one quantisation cycle, a time input of 90 ps and 1.6 ns was applied to the VRTDC. Due to the dependency of latency of the VRTDC on time input, the latter requires a longer quantisation time than the former, which is approximately 34.508 ns in comparison to 2.387 ns. The latency is defined as the time delay between *STOP* signal and the availability of the D_{OUT} , defined as */IN1* and */STOP* in figure 3-30. The first set of top two graphs in the figure corresponds to T_{IN} of 90 ps, and the second set of bottom two graphs corresponds to the largest T_{IN} of 1.636 ns.

If we define the quantisation period as 35 ns, sufficient for the full-scale T_{IN} , the simulated average current during one quantization for both 90 ps and 1.636 ns inputs is approximately 402.879 μ A and 389.815 μ A, with a peak current of 923.207 μ A and 884.21 μ A respectively. The peak current occurs at the rising edge of */STOP*, where D_{OUT} is made available. Taking the higher value of the

two, the average power consumption could then be calculated to be 483.4548 μ W, and a peak power consumption of 1.11 mW. Since the quantisation period is 35 ns, the sampling frequency is 28.57 MHz. And the energy dissipated per quantisation period is therefore calculated to be 16.922 μ W/MHz.

Figure 3-30 Latency and current consumption of the VRTDC in one quantisation cycle for time inputs of 90 ps and 1.636 ns

Differential Nonlinearity (DNL) error describes the deviation of each step from the ideal step for every LSB. Ideal converters have 0 DNL errors. With the DNL defined as follows:

$$DNL = \frac{T_{i+1} - T_i}{t_{res}} - 1 \quad (3.12)$$

a DNL of +/- 0.3LSB is calculated for this VRTDC.

Some degree of uncertainty happens during the time interval conversion. One cause could be the metastability of the arbiter and the flip flops that are inside the data evaluation block.

A summary of the performance comparison between the proposed body-biased VRTDC and other TDC schemes in the literature is shown in Table 3-9.

Table 3-9 Performance comparison of the proposed VRTDC with various TDC schemes

Ref.	[72] ISCAS '10	[46] JSSC '08	[73] VSLIC '12	[48] JSSC '14	[54] JSSC '12	[74] TCAS II '11	[71] JSSC '10	[75] ESSCIR C '11	This work
Scheme	Flash	Time Amp.	Two Step	Pipeline	Cyclic	Floatin g Point	VR	VR	VR
Supply [V]	1	1	1.2	1.2	1.3	1.8	1.5	1.2	1.2
Res. [ps]	6.25 (sim.)	1.25	3.75	1.12	1.25	3	2 (sim.) 8 (meas)	1.2	3 (sim.)
Bits	3	9	7	9	8	6	12	4	9
f_s [MHz]	5000	10	200	250	5	75	15	30	28.57
Power [mW]	9	3	3.6	15.4	4.3	18	7.5	3.6	0.4835
FoM [pJ/(conv. Step)]	0.225	0.586	0.141	0.12	0.336	3.75	0.122	7.5	0.033
Area [mm ²]	0.032	0.66	0.02	0.14	0.07	-	0.2625	0.027	0.014
Tech. [nm]	90	90	65	65	130	180	130	90	65

In comparison to the other works, the 1.2 V supply used in the VRTDC is the same as one of the other two Vernier Ring designs. It could be modified to operate under lower voltages, like the Flash or Time Amplification TDC.

The resolution and the number of bits of the VRTDC is comparable to the other presented works. The digital-intensive nature and possibly also the simpler design of the VRTDC made it possible to keep the size of the TDC small. Although triple-wells are used, the sharing of the wells for adjacent delay cells in layout helped reduced the area as well.

However, the issue with Vernier Ring designs is the long latency, and this is observed in the three VR designs in the table above, including this work, where the frequency is at the lower end. On the other extreme, the Flash TDCs are the fastest and two-step or pipeline can increase the sampling frequency due to their “parallel” approach.

Note that the power for the VRTDC is only a simulated value, thus the FoM shall only be used as an approximation.

3.5.7 Current consumption check for forward biased BJT

When the $|V_{SB}|$ applied to the PMOS M3 and/or NMOS M5 is too high, we expect a forward-biased body diode and a large current will flow through the affected transistors. But what is the limit? And what should be the determining factor for this limit?

We investigate the current consumption of the VRTDC with respect to body bias voltage to the PMOS, NMOS and both transistors, and look at the peak currents which are for very short time (within 1 ns as seen in figure 3-29) and the average current consumption per quantisation period. If the body diode is forward biased enough, according to the IV curve, an exponential current will flow through the transistor beyond the threshold of the body diode. This current will have an impact on the average consumption, which can be measured much easier in comparison to the peak current. For this investigation, only one of the two PMOS or NMOS body voltages are varied, with the other at the supply rail. The swept parameters and the range are listed in the table 3-10.

Table 3-10 Body bias voltage sweep for combination C3 (marked in red)

Combination	Vbiasp (V)	Vbiasp1 (V)	Vbiasn (V)	Vbiasn1 (V)
C3	0	0.19	1.2	1.095
Combination	V_bd_biasp (V)	V_bd_biasp1 (V)	V_bd_biasn (V)	V_bd_biasn1 (V)
C3	1.2	0 -> 1.2	0 -> 1.2	0

3.5.7.1 PMOS-only body bias voltage sweep

The $V_{P,bd}$ of the t_F delay cells, V_bd_biasp1, is swept from 0 to 1.2 V with a step of 10 mV. With reference to the current profile in figure 3-30, the highest current value from a time window of 35 ns, i.e. one quantisation period is taken as the peak current. The average current over this entire 35 ns is taken as the average current. This applies to both Vdd and Ground. Also, a T_{IN} of 90 ps was used for the investigation, therefore the peak current is that at 4 ns in figure 3-30. Figure 3-31 shows that the peak and average Ground currents are not so much affected by the PMOS body bias voltage.

Figure 3-31 Peak and average Supply and Ground currents with respect to change in PMOS body bias over the Vdd range

In fact, the average and peak Vdd and Ground currents are the same beyond 0.5 V. The biggest difference is from 0 to 0.5 V, which means the $|V_{SB}|$ is between 1.2 V and 0.7 V respectively, where a large Vdd peak current is observed in an exponential form. The average Vdd current is thus primarily the peak Vdd current because its magnitude is so large.

3.5.7.2 NMOS-only body bias voltage sweep

The same observation can be made about the V_{bd_biasn} sweep from 0 to 1.2 V, and again with a step of 10 mV. This is the $V_{N,bd}$ of the t_S delay cells. The peak and average currents versus V_{bd_biasn} is shown in figure 3-32.

Figure 3-32 Peak and average Supply and Ground currents with respect to change in NMOS body bias over the Vdd range

Up to 0.7 V, the average and peak Vdd and Ground currents are equal. However, as the V_{bd_biasn} increases beyond 0.7 V, i.e. $|V_{SB}|$ is between 0.7 V to 1.2 V, the peak Ground current increases in an exponentially, very much like the diode I-V curve, and becomes the main component of the average ground current. In contrary, the Vdd currents are not affected by the increasing source-bulk potential.

3.5.7.3 PMOS and NMOS body bias voltage sweep

Figure 3-33 below shows the average currents based on two-dimensional voltage sweep of the aforementioned voltages. Only the average currents of Vdd (in blue) and Ground (in orange) are shown, where it is clear which body voltage has an effect on which average current. For example, when both V_{bd_biasn} and V_{bd_biasp1} are 0 V, the Vdd average current is 358 mA, and the Ground average current is 0.3 mA. On the other hand, when both voltages are 1.2 V, the average Vdd and Ground currents are 0.3 mA and 287 mA respectively. The PMOS M3 is larger than NMOS M5, therefore the peak/average currents for Vdd are larger than for Ground.

Figure 3-33 Average Supply and Ground currents with respect to change in both PMOS and NMOS body bias over the Vdd range

3.6 Conclusion

A body-biased TDC technique has been presented, where the source-body junction is reverse-biased to achieve a better resolution. In other words, the transistor is made to switch faster, thus reducing the propagation delay of the delay cell. The resolution of the VRTDC is determined by the difference in the propagation delay of each cell in two delay lines. This vernier principle allows the VRTDC to achieve sub-gate delay.

By utilising gate biasing on the delay cells, it was possible to vary the propagation delay of the two main delay cells to achieve a desired resolution. However, the step change of the propagation delay is largely dependent on the size of the current-starving transistors. For that reason, body-biasing was further added to the said transistors to vary the delay in smaller steps. Hence, it is possible to say that body-biasing provides a fine tuning capability to the VRTDC, and it can also be extended to other TDCs where voltage-controlled delay cells are used.

Under temperature and supply voltage variations, the resolution of the VRTDC can change greatly as already shown. With gate and body biasing voltages, the resolution can be calibrated, thus providing some degree of immunity against VT variations.

Other than the delay cells which are half analogue-digital, the remainder of the VRTDC core is digital-intensive, allowing the design to be built based on cells and modular blocks, and achieve some form of compactness. However, the trade-off is the density of inter-circuitry wiring, which could be alleviated by using place-and-route. Nevertheless, simultaneous switching of multiple digital parts could result in large dynamic power consumption.

4 A 9-bit 1.08ps resolution body-biased Two-Step Time-to-Digital Converter in 65 nm CMOS for Time-Mode ADC

4.1 Introduction

Device scaling has made it harder to resolve signals in the voltage domain with reasonable power consumption, due to poorer signal-to-noise ratio (SNR). The reduced voltage headroom is a result of reduced supply voltage for reduced gate oxide thickness and a relatively higher threshold voltage. Noise on the other hand, does not scale with technology. This makes conventional voltage-mode implementation of ADCs increasingly difficult. Fortunately, switching time of a MOSFET has improved, giving more accuracy in time-domain resolution of digital signal edge transitions. This opens up the possibility of implementing ADCs in time-mode, capitalizing on this advantage. In such approaches, analogue information is represented by time delay through a voltage-to-time converter (VTC) and processed by a time-to-digital converter (TDC) which is inherently digital and can exploit the digital advantages of newer technologies.

The Vernier Ring TDC (VRTDC) allows for a high resolution but has the shortcoming of having a long latency every quantisation cycle. Implementing a TDC in the proposed TDC-based VTC (see chapter 5) requires multiple iterations (time quantisation cycles) per analogue quantisation cycle. Here, voltage input and time input quantisation are referred to as analogue and time quantisation respectively. The n number of time quantisation cycles results in n multiples of the latency per time quantisation. It has been shown earlier that the quantisation period is 35 ns, and if the VRTDC was used in the proposed time-mode data converter, the entire analogue quantisation cycle will be slowed down due to the extensive latency. Therefore, an alternative to the VRTDC is required to keep the time resolution high yet reducing the time wastage. The limitation on time was the first consideration to re-design the TDC. The second consideration was the amount of area used by the triple well due to the need for an NMOS body potential that is not ground, i.e. it requires a body in a P-well

sitting in an N-well, whose potential can be varied. While smart layout placement of the transistors in shared wells can be done to make the layout as compact as possible, there is still the issue with the complexity of too many voltage biases. Therefore, there is a motivation to move to a delay cell concept where no triple well is used, and only the PMOS body needs to be varied. Because the PMOS sits in an N-well, the N-well voltage can be varied with respect to the P-diffusion of the transistor and the p-substrate.

Other architectures of TDCs have to be considered to avoid the long latency yet high resolution. Time amplification TDC stretches time intervals to improve resolution, but the time gain can be uncertain due to PVT variations. Time amplification has been achieved using SR latch metastability, pulse train and even replicating delay cells [76]. Interpolating TDC requires a compromise between linearity of interpolated signals and cross currents. In a pipelined TDC in [48], the time interval is quantized for a fraction of the number of output bits. The quantization result is converted back to time and a residue is obtained. This residue is used in the next pipeline stage with the same fraction of output bits and same process. Pipelining helps to increase the conversion rate.

For quantization of long time intervals with high resolution TDCs, the conversion takes a long time. A two-step TDC allows the time interval to be first coarsely quantized and the residue finely quantized by a high resolution TDC. There are largely two schemes of fine time quantization used in two-step TDCs: time-amplification of residue [47, 76-78] or simply a high resolution TDC with dynamic range equal to the quantization interval of the coarse TDC. In any case, a multiplexer logic is needed to couple both stages, and there are many variants in the literature, for example pseudo-NMOS OR gate in [73] or a metastability-free selection logic in [79].

For its usage in the twin-mode converter, the TDC must be fast with short latency, and a two-step architecture is perhaps the easiest to implement. Leveraging on the technique of body-biasing for delay tuning, it is possible to adopt a two-step architecture without having the need to amplify the residual time. The requirement of a dynamic range of fine TDC ideally equal to the coarse TDC quantization interval can thus be met. However, the injection of unwanted time delay through the coupling remains challenging. The proposed design first

performs a coarse quantization conversion through a Flash-Vernier TDC, followed by a fine quantization using a linear body-biased Vernier TDC.

This chapter describes the proposed design with the following organization: in Section 2, an overview of the working principle is presented. Section 3 details the circuit implementation of the proposed design. Results and performance comparison with other TDCs are revealed in Section 4. Finally, Section 5 summarizes the work presented.

4.2 Concept of the proposed coarse-fine TDC

The proposed coarse-fine TDC (CFTDC) is a two-step TDC that first quantises the time input, T_{IN} coarsely or in low resolution, then residually by a finer, higher resolution TDC. It utilises the Vernier concept in the fine TDC for high resolution, and a pseudo-Vernier concept in the coarse TDC to obtain delay matching. Shown in figure 4-1 is the simplified diagram of the CFTDC.

The proposed 9-bit CFTDC has 4 and 5 bits from the coarse and fine TDCs respectively, equivalent to 16 stages in the coarse TDC and 32 in the fine. Both TDC stages are fully functional TDCs and independent of each other. The relationship between the two stages that should be maintained is that the full detectable range of the fine TDC must be equal to a single delay stage of the coarse TDC. A simplified block diagram of the proposed CFTDC is shown below in figure 4-1.

T_{IN} , the delay defined between two rising edge signals, *START* and *STOP*, is first quantised by the low-resolution coarse TDC without latency, thanks to the flash nature of the architecture. As a result of dividing T_{IN} by fixed delays, t_C , the remaining time delay that does not fit completely as t_C becomes the residual time, $T_{RESIDUE}$. In principle, this is a simple number division, where there is a dividend, T_{IN} , the divisor, t_C , the quotient which is the counts of t_C , and the remainder $T_{RESIDUE}$. The timing diagram in figure 4-2 illustrates this concept of the CFTDC, where $T_{RESIDUE}$ is highlighted in red between c4 and *STOP*. In this case, the quotient is 4, i.e. 4 counts of t_C .

This $T_{RESIDUE}$ is then transferred from the coarse TDC to the fine TDC which has a smaller resolution, or divisor than the coarse TDC. This transfer is made possible by a coupling circuit or a multiplexer network that exists between the coarse and fine TDCs. This residual time, $T_{RESIDUE}$ is the input time for the fine TDC. In reality, since lost time cannot be captured, the presence of all the delayed *START* signals, c_i before *STOP* in figure 4-2 are no longer known to the fine TDC. However, only *STOP* signal and the next delayed *START* signal, i.e. c_5 is known. This amount of delay between *STOP* and c_5 is called $T_{RESIDUE}'$, which is also the amount of delay that will make up a full t_C with $T_{RESIDUE}$. Therefore, we define $T_{RESIDUE}'$ as the delay difference between *START_v* and *STOP_v*, the input signals to the fine TDC. This means that the resulting fine TDC output is inverted.

Suppose T_{IN} is 136 ps and coarse TDC resolution is 32 ps. Therefore,

$$T_{IN} = 4 * t_C + 8 \text{ ps} \quad (4.1)$$

Figure 4-1 Simplified block diagram of the coarse-fine TDC (CFTDC)

Note that the counting of each block of 32 ps is done by a series of arbiters, i.e. recognising a full 32 ps is done by detecting the crossing of an edge against a reference edge. Obviously, no time information can be stored or has been stored. However, the instance an edge crosses a reference edge can be stored in the form of a digital bit “1” or “0” - as a flag. Therefore, by using the information from

each arbiter, the instance that *STOP* crosses a delayed-*START* is captured, which defines the end of T_{IN} and can be further used to generate the inverted residual time $T_{RESIDUE'}$.

Figure 4-2 Timing diagram of the coarse arbiter outputs for a T_{IN} equal to 136 ps

4.2.1 Flash-Vernier Coarse TDC

The coarse TDC has 16 delay stages, each comprising of an arbiter and one accompanying delay cell connected to the arbiter as shown in figure 4-1. In other words, a delayed *START* signal, *ci* and *STOP* signal are inputs to an arbiter at each stage. As the *START* signal delays by one t_c each time, it is compared with *STOP*, which is not delayed, via the arbiter to decide whether *ci* or *STOP* arrives first. If it arrives first, the *F* output of each arbiter will be a logic 1, otherwise a logic 0. With reference to the timing diagram in figure 4-2, *F1* to *F4*, which are outputs of the first 4 arbiters are logic 0, simply because *STOP* never arrived before *c1* to *c4*. On the other hand, the former arrives before *c5*, and subsequently *c6* and so on. Therefore, arbiter outputs *F5* to *F16* are logic high. All 16 arbiter outputs reveal when does *STOP* arrive, and as a digital output of the coarse TDC, it gives us the quotient, or the number of counts of t_c .

One important consideration of the coarse TDC is that the delay per coarse stage (or coarse TDC resolution), t_C must be kept equal to the full range of the fine TDC. It has been elaborated earlier that the residual time, $T_{RESIDUE}$ is what does not make up a full t_C , and is the input of fine TDC. Therefore, it must be ensured that t_C is not less than the maximum $T_{RESIDUE}$. Knowing that the fine TDC has five bits output, we set the condition for the coarse TDC resolution as:

$$t_C = 32 * t_{res} \quad (4.2)$$

, where t_{res} is the fine TDC resolution. But in a flash TDC, the t_C or delay per stage is determined and limited by the transistor sizes. A small delay requires that the transistors in the delay stages be small, but yet needs to be large enough to drive the other circuits that are load it. To enable the flexibility of a tuneable t_C , the delay cells of the coarse TDC are modified with additional biasing capability, achieved through the means of a stacked PMOS to tune t_C through gate and body biasing, similar to what was presented in the VRTDC. However, the addition of a stacked PMOS limits the current through the delay cell and increases unintentionally the propagation delay. Consequently, t_C will flout the requirement in equation 4.2.

Therefore, a tweak to the flash structure is needed, by adding a similar voltage-biased delay cell to the *STOP* line as shown in figure 4-3. Recall the structure of the VRTDC, and that the TDC resolution is determined by the Vernier principle. Therefore, a *STOP* line with added delays is used to create an offset, such that the resultant delay of the coarse TDC is the difference of the two delay lines. Like the VRTDC, varying the gate and bulk voltages of the stacked PMOS varies the current to the delay cell, and therefore alters the delay of the cell. This gives us the ability to tune the coarse stage delay to fit the fine stages delay.

However the resolution required for the coarse TDC is not small, i.e. 32 times the resolution of CFTDC, t_{res} , and thus there is no need for varying bias voltages on the *STOP* line. In other words, the delay elements in the said line will have a fixed delay, t_{C2} , and via the Vernier principle, the coarse TDC can now achieve the desired time resolution defined as $t_C = t_{C1} - t_{C2}$, where t_{C1} is the delay per cell of the *START* line.

Figure 4-3 Flash-Vernier structure is used in the coarse TDC to obtain the desired resolution

Since the resolution is determined from stage to stage, both delay lines must have the same number of delay cells and all delay cells in each line must be the same. *START* is delayed through the tuneable delay line and *STOP* is delayed through the fixed delay line. Here, we identify *START* and *STOP* as the two reference edges that define T_{IN} , and *delayed-START* and *delayed-STOP* as a consequence of *START* and *STOP* propagating down their individual delay lines, or ca_i and ce_i in the figure, where i represents the delay stage.

In other words, a pair of *delayed-START* and *delayed-STOP* signals are generated at every delay stage. The time difference between each pair decreases after every stage because $t_{c1} > t_{c2}$. Therefore, *delayed-STOP* eventually “catches” up with *delayed-START* somewhere along the delay line, and when it does, the arbiter output of that stage switches to logic 1, indicating the location where this had happened.

In this modified Flash-Vernier structure, the arbiter in each stage has two inputs, connected to each of the two delay cells per stage. It determines if the ca_i or ce_i arrived first in its stage. Its pair of active-high complementary “F” and “S” outputs indicate if ce_i and ca_i arrived first respectively.

4.2.2 Vernier Fine TDC

Of the 9 bits of the CFTDC, 5 bits are from the second stage - the fine TDC. The implemented Vernier TDC (see figure 4-4) will have its own set of two input signals, named as $START_v$ and $STOP_v$. The delay difference between both signals defines the residual time from the coarse TDC. Unlike the coarse TDC, the fine TDC has two tuneable delay lines, each with 32 delay stages. The resolution of the fine TDC (and also the resolution of the CFTDC) is defined as the difference in the propagation delay per delay stage from each delay line, as

in the VRTDC. Since the required resolution is very high, both delay lines must be made tuneable because there is a limit to how high the resolution can be achieved with only one tuneable delay line, as is the case for the coarse TDC.

Figure 4-4 Vernier structure is used in the fine TDC to obtain sub-gate CFTDC resolution

Assume the delay in the top delay line with $START_v$ as the input is t_S and the bottom delay line with $STOP_v$ as the input has t_F per delay stage. The resolution of the fine TDC and the CFTDC is thus defined as:

$$t_{res} = t_S - t_F \quad (4.3)$$

$START_v$ and $STOP_v$ are delayed by t_S and t_F from one stage to another respectively. Since t_S is intentionally made larger than t_F , the delayed version of $START_v$ eventually catches up with that of $STOP_v$.

Similar to the coarse TDC, every delay stage has two delay cells connected to an arbiter connected to determine if *delayed-START_v* (vs_i) or *delayed-STOP_v* (vf_i) arrived first in its stage. Its true and complementary outputs, F and S give the logic value of the first arrival of fi and si respectively.

4.2.3 Coupling circuit

Conceptually, a two-stage TDC is easy to implement, but every signal processing logic contributes an unknown amount of propagation delay and result in a +/- delay offset by means of injecting unwanted time delay or removing time information through the coupling from the coarse to the fine stage. In order to avoid the offset, the paths that cai and cei take must be kept as similar as possible all the way till the generation of $START_v$ and $STOP_v$. The idea behind is to implement a single open-path that feeds the delayed signals through. These signals are not fed into combinational logic, whose tendencies to output logic-1 and -0, dependent also on other inputs can affect the slope and

propagation delay. A coupling circuit block is added between the coarse and fine TDCs.

Using the previous example of $T_{IN} = 136$ ps and figure 4-2 for the explanation of this concept, *STOP* arrives 136 ps after the arrival of *START*. The first 4 arbiters in the coarse TDC will have a logic one in the S output, and from the 5th arbiter onwards, a logic one in the F output. This means that *STOP* has arrived before *c5* at the 5th delay stage. $T_{RESIDUE'}$ is evaluated from the *STOP* in the delay stage where F first becomes “1” to the *c5* in the same delay stage. Therefore, the remaining 8 ps residual time is taken as $T_{RESIDUE'} = 24$ ps. This parameter is defined as the delay between *START_v* and *STOP_v* for fine time quantisation.

The coupling circuit is made up of three blocks; a digital signal buffer block, a multiplexer network and a $T_{RESIDUE'}$ generator. The digital signal buffers come before the multiplexer network and the $T_{RESIDUE'}$ generator follows the latter.

4.2.3.1 Digital Signal Buffer block

From every delay stage in the coarse TDC, the pair of *delayed_START* (or *cai*) and *delayed_STOP* (or *cel*) signals are connected to the coupling circuit. From each signal's point of view, it has a load of one delay cell, one arbiter and some logic gates in the coupling circuit. The signals are heavily loaded and the rising and falling edges are slowed down. The amount of delay added due to the loading differs for *delayed_START* and *delayed_STOP* due to the different drivability of the delay cells, which is a consequence of varying the propagation delay via body-biasing.

Therefore, a digital signal buffer has to be added to each incoming *delayed_START* (*_STOP*) signal to improve the slope of its falling or rising edge and also to isolate the loading from the subsequent stage of logic gates. Thirty-two digital signal buffers are in the buffer block for all the *delayed_START* (*_STOP*) edges.

4.2.3.2 Multiplexer Network

The multiplexer network has two independent blocks - the S-F output detector and a multiplexer tree.

All the *delayed_START* (*_STOP*) signals are connected to the multiplexer tree via the signal buffers. However, only one branch (or path) of the multiplexer tree is open at any one time, such that only one of the 16 *delayed_START* (*_STOP*) signals can propagate down the tree to the output. The select signals for the multiplexers at every hierarchy of the tree are generated by the S-F output detector.

The S-F output detector has the primary task of identifying which delay stage has the first instance of an activated arbiter F output. Depending on the position in the delay line the first F output occurs, it decides which select signals should be activated to open the path for the corresponding *delayed_START* (*_STOP*), while the rest remain closed (by default).

There are two main considerations in this multiplexer tree concept, i.e. identifying the correct delayed signal and ensuring the timely propagation of the identified signal. To determine if a signal has propagated through a logic gate, the signal edge is used as the point of reference. If a logic gate is selected to pass through the signal, the latter's edge should only arrive after the gate has been enabled. Otherwise, the propagated edge will not be seen at the output, since the signal edge has already passed and time information cannot be stored, i.e. the instance that an edge takes place cannot be "memorised" and kept for later use. What appears at the output then is only the final voltage level. Two consequences arise from this situation - first, the original edge from the input signal is not seen by the subsequent stage. Second, at the instance when the gate is finally enabled, the output voltage level may be switched, and this becomes the new edge input for the subsequent stages. In a logic circuit where only the high and low state of the signal is of importance, this is not an issue. However in this design, the fake edge results in an erroneous interpretation of the time information. Capturing the instance of the edge is hence very crucial. For the same reason, the delay in generating the select signals also has to be taken into account.

In order to ensure that no additional unwanted time delay is injected between the coarse and fine mode switch, the same coupling circuit must be implemented for both *START* and *STOP*. Both signals should go through similar paths for *START_v* and *STOP_v* signal generation. Both signals are inputs for

the Vernier fine TDC, whose delay difference define the $T_{RESIDUE}$. Due to the configuration of the fine TDC delay stages, the $START_v$ and $STOP_v$ signals are made to be falling edge signals, unlike those for the coarse TDC.

4.2.4 Output Encoder

The output data of both TDCs are in the form of thermometer code. Before $STOP$ ($STOP_v$) catches up with $START$ ($START_v$), the arbiters' S- and F- outputs are logic-one and -zero respectively. When the latter catches up with the former, all the arbiters from that instance onwards will have S- and F-outputs as logic-zero and -one respectively. Since most digital circuits use binary code for logic evaluation, it makes more sense to present the output data in its 9-bit form. An output encoder is necessary to convert the 16-bit coarse data and 32-bit fine data into binary form for efficient representation of the output data.

Again using the example in figure 4-2 earlier, the F output of 5th coarse arbiter onwards F5 – F16 are raised high. Taking all sixteen F (and S) outputs for binary data generation gives the following coarse thermometer code 16'hFFE0 with ten 1s. A converted binary output will yield 4'b0101, but is an erroneous result since $D_{coarse}[3:0]$ should be 4₁₀. So the output encoder has to remove a "1" from the coarse thermometer code. This can be done by shifting the 1s towards the LSB by one step but requires 16 registers for a 16-bit thermometer code. A simpler method is to drop F1 logic value in the data conversion, but requires some extra gates for correct data representation. This will be covered in the circuit implementation.

The conversion of the 32-bit fine TDC output from thermometer code to binary is also done by the output encoder. Here, it is necessary to invert the binary output data, $D_{fine}[4:0]$ to obtain the correct representation of $T_{RESIDUE}$. This also becomes a limitation of the design, where the 9-bit CFTDC output data is upon reset given a default value $DOUT[8:0] = (D_{coarse}[3:0], D_{fine}[4:0]) = 9'b000011111$.

4.2.5 Resetting the TDC

At the end of every quantisation, the digital circuitry in the TDC has to be reset, i.e. the arbiter, the flip flops, etc. This means that the output states are set to the designed default values. For this design, the rising edges of $START$ and $STOP$

define the time input interval. In other words, when both signals are in the low state, no time information is available. Therefore, the TDC recognises the low state of the said input signals as a reset signal. In other words, only upon the arrival of the rising edge of either of the two input signals is the TDC ready for quantisation. As long as the two signals do not fall back to a low state, the TDC is never reset. Should a new input time sample T_{IN} need to be quantised, *START* and *STOP* are first returned to zero, before rising to Vdd again. Consequently, the TDC is reset for the next quantisation cycle. From the rising edges of both input signals, an internal global reset signal is generated for the digital circuitry in the CFTDC. Therefore, this CFTDC is made to be self-reset-capable with no external reset signal necessary.

4.3 Circuit Implementation

4.3.1 Body-biased inverter

The delay cells in the coarse and fine TDCs are made differently, but have one common circuit - the body-biased inverter. The concept of body-biasing the inverter has already been elaborated in the earlier chapter. Having two delay lines with a different set of voltage biases to control the propagation delay through the delay cells, the time resolution can be adjusted as desired. The CFTDC uses primarily the same body-biased inverter but with modifications to the delay cell. Every tuneable delay line will contain n number of body-biased delay cells, depending on the bit count.

Unlike in the VRTDC, the body-biased inverter in the CFTDC only has one stacked PMOS which is body-biased. To keep the area small due to the larger coupling logic circuit in the CFTDC, varying the bulk voltage of a stacked NMOS in the VRTDC is avoided so that there is no need for a triple-well structure. The design rule requires a 1 μm spacing between two triple wells of different potential, and this will take up a relatively large area. Also, keeping the biasing to just the PMOS reduces the number of biases by half and simplifies the delay tuning.

Body-biasing on the stacked PMOS only affects the propagation delay of the inverter when it switches from Vout-low to Vout-high, or on the rising edge. In

other words, the threshold point where the body-biased inverter output switches from low-to-high is modified with the source-bulk voltage, which results in an alteration in the propagation delay.

Placing body-biased inverters one after another renders every second inverter redundant since the falling edge is not affected by the voltage biasing. Instead, a second regular inverter can be placed after a body-biased inverter. The high-to-low switching in the regular inverter takes place at the innate threshold, which will have the same effect as two cascaded body-biased inverters, since the current through the NMOS transistor of both inverter types is not limited by a stack transistor as in the VRTDC. The advantage of cascading a regular inverter is saving space since the body-biased inverter is much larger.

Similarly in the CFTDC, the set of bias voltages allows the flexibility to obtain the required time resolution, i.e. the same resolution is obtainable through different voltage combinations. However, the body bias should not be increased too much to exceed the V_{BE} of the intrinsic bipolar junction transistor between the body and source/drain. Allowing so results in the conduction of the intrinsic BJT and consequently latch-up and short-circuit of the power rails.

4.3.2 CFTDC delay stages

As mentioned earlier, the delay cells for the coarse and fine TDC are made up differently. The delay stages are also slightly different, because the coarse TDC uses a flash-Vernier structure. The implementation of the delay stages are explained in detail here.

4.3.2.1 Coarse TDC

Since the coarse TDC is a flash-Vernier TDC, the two delay cells per stage are built differently. The *START* delay line has delay cells that are each made up of an inverter, a body-biased inverter and a buffer. The *STOP* delay line on the other hand only has a buffer. The implementation of the coarse TDC delay stage is shown in figure 4-5. Note that the body of the other transistors whose connections are not shown in the figure are connected to the rails.

Without a buffer after the body-biased inverter, the output gain as a result of limiting the current via the stacked PMOS is insufficient to drive the load - the subsequent delay cell, an arbiter and some gates in the coupling circuit. For this reason, the inverter is placed before the body-biased inverter, and a buffer is placed after it. Placing the regular inverter in front also inverts the $(delayed_START)$ and $(delayed_STOP)$ signals which are all rising edge signals. Inverting their polarities ensure that the signal edge going through the body-biased inverter is a falling one, so that the stacked PMOS can alter the propagation delay.

Figure 4-5 Implementation of the coarse TDC delay stage

With the buffer in the delay stage, the propagation delay becomes too large to keep the coarse TDC resolution 32 times of the fine TDC resolution. Therefore, the same buffer has also been added to the bottom delay line where *STOP* propagates through to reduce the delay difference between both delay lines.

The time resolution of the coarse TDC is thus primarily determined by the propagation delay of the inverter plus that of the body-biased inverter, which is tuneable. Given earlier the resolution of the coarse TDC,

$$t_c = t_{c1} - t_{c2} \quad (4.4)$$

$$t_c = (t_{inv} + t_{bias-inv} + t_{buf}) - t_{buf} \quad (4.5)$$

$$t_c = t_{inv} + t_{bias-inv} \quad (4.6)$$

4.3.2.2 Fine TDC

In the Vernier TDC, the delay cells in each delay stage have the same elements - a body-biased inverter followed by an inverter. Each of the body-biased inverter in the two delay cells per stage have a different set of voltage biases in order to achieve the final CFTDC resolution. The inputs of the fine TDC, $START_v$ and $STOP_v$ are generated from the coupling circuit and are falling edge signals. The arbiters in the fine TDC must be able to arbitrate the $delayed_START_v$ ($_STOP_v$) based on falling edges. A regular inverter is added after the body-biased inverter to strengthen the load drive. The structure of the fine TDC delay stage is shown in figure 4-6. Note that the body of the other transistors whose connections are not shown in the figure are connected to the rails.

Figure 4-6 Delay stage of the fine TDC using the Vernier principle

4.3.3 Coupling circuit

A simplified schematic of the coupling circuit is shown in figure 4-7 below. Two sets of data are crucial, namely the $delayed_START$ ($_STOP$) signals that will be buffered, and the coarse S- and F-outputs from the arbiters, $S[15:0]$ and $F[15:0]$. The multiplexer network has two independent blocks - the S-F output detector implemented by a 1-out-of-N decoder and a multiplexer tree.

The buffer block is an array of digital signal buffers comprising of a digital buffer and two D flip-flops. In the simplified circuit, the buffers are shown only as a flip-flop. Since the $delayed_START$ ($_STOP$) signals (shown as $c13...c16$) have to arrive after a certain path in the multiplexer network is open, the flip-flops also

help to extend the “waiting” time. The *delayed_START* (*_STOP*) signals are taken from the coarse TDC delay line, buffered, and are used as clock signals for the flip-flops that have a logic one as their inputs. The output of the flip-flops are then used in the multiplexer tree in the generation of *start_v* and *stop_v*. With this configuration, no clock input is necessary for the regeneration of the *delayed_START* (*_STOP*) signals, and no need for timing synchronization.

Figure 4-7 Implementation of the coupling circuit showing the buffer block and MUX network

There are four levels in the multiplexer tree and the multiplexer select signals for each level are a combinational logic of the S-F outputs cumulatively. Note that only 2 levels are shown in the figure. It illustrates the example used in figure 4-2, where *delayed_STOP* passes *delayed_START*, *c5*. Arbitrer output F5 is switched to logic 1, and S5 is switched to logic 0. For this reason, only select signal *o5b* is logic 0, while the rest are at logic 1.

Level 1:

$$\overline{sel_1[a]} = \overline{F[a].S[a-1].S[a-2]} \quad (4.7)$$

where $16 \leq a \leq 1$. Followed by Level 2:

$$sel_2[b_(b+1)] = \overline{sel_1[b].sel_1[b+1]} \quad (4.8)$$

where $b = 1, 3, 5, 7, 9, 11, 13$. Followed by Level 3:

$$sel_3[c_(c+3)] = \overline{sel_2[c_(c+1)].sel_2[(c+2)_(c+3)]} \quad (4.9)$$

where $c = 1, 5$. And finally Level 4:

$$sel_4 = \overline{sel_3[d_(d+3)].sel_3[e_(e+3)]} \quad (4.10)$$

where $d = 1$ and $e = 5$. Therefore for the example illustrated in figure 4-7,

Level 1:

$$\overline{o5} = \overline{F[5].S[4].S[3]} \quad (4.11)$$

$$\overline{o6} = \overline{F[6].S[5].S[4]} \quad (4.12)$$

Level 2:

$$o5_6 = \overline{o5}.\overline{o6} \quad (4.13)$$

Level 3:

$$o5_8 = \overline{o5_6}.\overline{o7_8} \quad (4.14)$$

Level 4:

$$o1_8 = \overline{o1_4}.\overline{o5_8} \quad (4.15)$$

This means that from the first to fourth level of the multiplexer network, there are 16, 7, 2 and 1 select signals available respectively. In order to generate the required select signals, the minimum number of select signals must be generated at every level, given as a , b , and c in the equations above.

The first level of select signals are generated by a one-out-of-N circuit from the S- and F-outputs in thermometer code form to generate only a single “0” and sixteen “1”s in $\overline{sel_1}[16:1]$. F-outputs are in thermometer code form, and will contain n number of 0s and $(16-n)$ number of 1s. On the other hand, the S-thermometer code will have n number of 1s and $(16-n)$ number of 0s. The first occurrence of $F=1$ is the location (delay stage) of *delayed_STOP* crossing *delayed_START*.

The second level of select signals are generated from that in the first level, third level select signals from second level and so forth. Because the first level select signals are a product of the NAND3 function, the “0” as a result of all three inputs “1” is generated. The second level select signals onwards use AND2 functions, and the “0” is carried forward.

Since two buffered signals are connected to one multiplexer at every level, only 8 multiplexers are needed at the first level, 4 at the second, 2 at the third and 1 at the last level. It follows then that the required number of select signals is less

than what is made available. For example, although 16 first level select signals are needed to generate the 7 second level select signals, only 8 will be used to control the multiplexers in the first level.

The final output of the multiplexer tree network is the *START_v* and *STOP_v* signals, inputs to the Vernier fine TDC. From the moment the *delayed_START* and *delayed_STOP* signals enter the coupling circuit, they go through the same logical path in order to limit the uncertainty added during the signal processing. Moreover, using multiplexers in the coupling circuit limits the tendency of inverting the signals multiple times, only the select signals are inverted by NAND or AND functions. If a signal is inverted at different threshold points at every occasion, the resulting rising or falling edges will take place at different points and possibly with different slope gradients. This adds to the uncertainty of additional delay to the buffered *delayed_START* (*_STOP*) signals.

4.3.4 Output Encoder

The same FAT-tree encoder as in VRTDC is used here to translate thermometer code to binary form. It has two stages, a one-out-of-N code generator followed by an AND-OR array. As mentioned earlier in the concept, the TDC coarse output has to be reduced by one. This can be simply achieved by dropping F1 from the 15 inputs of the encoder. For example, when F2 is the first F output to be “1”, F3...F16 are also “1”, only F1 is “0”. The one-out-of-N code generator as the pre-stage gives I0...I15 = 100000000000000 to the input of the AND-OR array, resulting in an output D_{coarse}[3:0]=4'b0001. Similarly, if F3 is the first F output to be “1”, D_{coarse}[3:0] will be 4'b0010, and so on. However, if F1=1, the FAT-tree encoder will never output 4'b0000, since F1 is dropped from the logic evaluation.

To avoid this, F1 could be used as an enable signal for an array of XOR gates instead, whose 2nd inputs are connected to F16...F2 as shown in figure 4-8 below. So if F1=1, the other F outputs are expected to be 1 as well. Therefore, the outputs of the fifteen XOR gates will be “0”, giving a D_{coarse}[3:0] output of 4'b0000. Otherwise, the values of F2...F16 will take precedence to decide the fifteen XOR outputs.

Figure 4-8 An array of XOR gates is added prior to the FAT Tree Encoder to perform a logic subtraction of the coarse data output

4.3.5 Complete design

All designs were carried out on Cadence Virtuoso using GF 65 nm CMOS technology. The full layout of the CFTDC is shown in figure 4-9, with the various building blocks marked out in different colours.

The core area size of the CFTDC is 0.00969mm². The layout has been optimised to ensure that the delay stages in the coarse and fine TDCs have as much similarity from cell-to-cell as possible. The empty spaces surrounding the blocks are filled with other building blocks from the Voltage-to-Time Converter. Without optimising the layout for combination with the VTC, the core area can be reduced to just 0.00697mm². The use of slightly larger-than-minimal transistors in the digital circuitry is the principle reason for the small area consumption. Also, the absence of triple-well for the NMOS also helps reduce the area for the TDC core. In fact, if the area is to be compared with the proposed VRTDC in table 3-9, the area of the CFTDC is indeed smaller by a bit. Moreover, the latter has more building blocks in the design.

Figure 4-9 Layout of the CFTDC with the main building blocks highlighted

4.4 Results and Discussion

The proposed CFTDC was taped out in GF 65 nm CMOS technology. Unlike the VRTDC, this IC did not have a built-in delay generator, because there is no possibility to prove the functionality of the delay generator with a reference external clock. The concept of TDC measurements using two ramp signals that is the common methodology is described.

4.4.1 TDC measurement method

To measure the resolution of the TDC, two input ramp signals with a slightly different frequency is applied to the two inputs of the TDC. For example in [47], a 200 and 199.99 MHz clock input is used to generate the ramp inputs for the TDC. The time difference at the start is 0 and at the end of the ramp, a finite delay difference that corresponds to the 10 kHz frequency difference. This results in a 250 fs/cycle time input ramp for the 3.75 ps TDC measurement. A logic analyzer collects the TDC output data as a result of the ramp input.

To determine the clock frequency needed, one can easily describe the relationship between the TDC resolution and frequencies by the equation below:

$$\frac{1}{F_2} - \frac{1}{F_1} = \frac{t_{res}}{N} \quad (4.16)$$

Where N represents the fraction of the TDC resolution for a meaningful measurement, and where F_2 and F_1 are the frequencies of the two ramp signals. Note that F_2 should be lower than F_1 and where the difference is the frequency difference to obtainable from the test system.

Following that, suppose that N is set at 5 and the resolution is 1.1 ps, F_1 and F_2 can be selected as 300 MHz and 299.99 MHz respectively for the CFTDC measurement. To measure the DNL and INL, the finer ramp signal that is a fraction of the above input must be generated. A reasonable fraction should be 1/10 or smaller.

4.4.1.1 Effect of Jitter on TDC measurement

Therefore, the measurement of the TDC can be affected by the jitter of the two input clocks. If the jitter of the test system is larger than the TDC resolution, it can be the dominant error in the TDC measurement. To measure the jitter noise, a one-shot precision test can be performed by applying a constant time input to the TDC. The single-shot precision is defined as the standard deviation of the measurement results for every input time interval that is measured repeatedly. By definition, it describes the reproducibility of a TDC measurement in the presence of noise. To do this, a single clock signal is split by a T-connector into two pulses. One is fed into the TDC as start signal, and the other is delayed by a cable of a different length and then fed into the TDC as stop signal. Therefore, the input jitter directly affects the results of this single-shot test, which comes from the cable length and PCB routing from a single clock source. This standard deviation parameter can be corroborated by the jitter measurement of the two input signals without the TDC as performed in [80].

Further to that, the same test can be performed for multiple time intervals. In some measurements, a range for each input time interval with a fixed time step is also measured and repeated is also performed. The goal is to collect sufficient statistics to obtain the single-shot precision value.

By knowing the jitter from the single-shot precision measurement, it is possible to eliminate it from the measured results by post-processing. Alternatively, the TDC measurement described earlier can be repeated by a number of cycles, for e.g. one million to eliminate the effect of jitter on the results. The output data is collected with a logic analyser and by measuring the cumulative code counts, the output count versus input delay can be obtained with noise averaged out [48].

The test setups described earlier use varying cable lengths to obtain various time intervals, which is the most common and widely accepted test setup. A more predictable method of generating varying time intervals is described in [54]. A single clock signal, provided externally, is fed into a Time Amplifier of known gain, whose dual outputs are fed to the TDC for quantisation. Since a single clock is used, the effect of jitter is minimized. The amplified time measurement is performed multiple times to collect the single-shot precision value of the TDC like before. While the jitter effect is reduced, as observed by the smaller standard deviation than that of the earlier described test method, the test was only performed once, i.e. only one time interval is possible. This concept can however be developed further to generate more time intervals.

4.4.1.2 Proposed TDC measurement method

There is clearly a need to have a more predictable approach for TDC measurement which can cover the dynamic range of the device under test. A concept for on-chip time generator for TDC measurement was started but could not be completed due to insufficient time. The concept is briefly explained in the chapter of Future Work.

A part of this concept is also utilised in the proposed VTC in chapter 6, where the time generation is explained in detail. Nevertheless, the CFTDC is available in silicon and the commonly accepted test setup may be used to perform the TDC characterisation. However, in-depth simulation results of the CFTDC shall be discussed here with emphasis on the dependence of the TDC resolution on voltage biasing of the delay cells and the effect of supply voltage and temperature variation on the resolution. Furthermore, results to the performance of the CFTDC are also shared in this section.

4.4.2 Effect of biasing on coarse TDC

In comparison to the VRTDC, the CFTDC only uses one current starving transistor implemented as a current source with a PMOS, as shown in figure 4-5. Therefore, the need for NMOS gate and body bias is no longer necessary. From the implementation point of view, the use of triple well is avoided, saving more area and enabling a more compact layout. From the system point of view, the number of voltage biases is reduced and the complexity of bias combinations is also reduced.

Similarly to the VRTDC, the current starving PMOS will have a gate- and body voltage bias, V_P and $V_{P,bd}$. Both the coarse and fine TDCs have the same structure and without the NMOS biases, it is possible to already check the influence of the PMOS biases, both gate and body, on the cell delay t_{Ci} and TDC resolution t_C . We first investigate the coarse TDC.

V_P is swept from 0 to 1.2 V and $V_{P,bd}$ is swept from 0.6 V to 1.2 V. It has been seen earlier that the cell delay, t_{Ci} increases with increasing gate voltage, due to the reduced V_{sg} of the current starving PMOS, thus reducing the current flowing through the inverter. It should also be expected to see a decreasing cell delay with decreasing body voltage, which brings the p-n diode between source and bulk deeper into the reverse-bias condition. Figure 4-10 shows the result of the two-dimensional sweep against the stage delay. The x-axis represents the gate bias voltage, and the different colours on the graph represent the seven body bias voltages. For all $V_{P,bd}$ voltages, the change in t_{Ci} becomes significant for V_P voltages above 0.45 V. With regards to the body bias voltages, the difference in t_{Ci} is not huge for V_P below 0.45 V. However, this changes in the middle of the entire V_P range, where a seemingly linear difference in t_{Ci} is observed between the $V_{P,bd}$ voltages. Moreover, the lower the $V_{P,bd}$ voltage, the smaller is the t_{Ci} . This is in agreement with the VRTDC results and the understanding of body bias. The disparity is apparent up till 0.8 V where the difference in t_{Ci} starts to decrease, pointing to the fact that the effect of body bias is decreases as the V_{sg} decreases further. In other words, the stage delay becomes very dependent on V_P (or V_{sg}), and is significantly large.

Nevertheless, this large t_{Ci} is not desirable for a high resolution TDC where the t_{res} is expected to be in the range of 1 to 3 ps. Since the coarse stage has 16 stages, it should be expected that the t_{Ci} should not exceed 48 ps, which limits the V_P (V_{biasp_c}) to be less than 0.55 V for $V_{P,bd}$ ($V_{bd_biasp_c}$) at 0.6 V.

Figure 4-10 Influence of gate and body biasing voltage on coarse TDC stage delay

Since the coarse TDC is designed as a pseudo Vernier TDC, i.e. the *START* line has a delay dependent on the gate and body bias, while the *STOP* line has a fixed delay. Therefore, the stage delay t_{Ci} , which has already taken into account the delay difference between the *START* and *STOP* delay cells per stage, is in fact the resolution of the coarse TDC, t_C .

4.4.3 Effect of biasing on fine TDC

The fine TDC is a pure Vernier TDC like the VRTDC, where the stage delay is defined as the delay difference both cells of each delay line per stage. This stage delay is also the resolution of the fine TDC and of the CFTDC, t_{res} . Referring to figure 4-6, the *START* line cell delay shall be called t_S and that of the *STOP* line called t_F . For the investigation of the influence of biasing on the t_{res} , the set of V_P and $V_{P,bd}$ of t_F shall be fixed at 0 and 1.2 V respectively. Therefore, the V_P and $V_{P,bd}$ of t_S , otherwise annotated as V_{biasp} and V_{bd_biasp} hereinafter shall

be swept from 0 to 1.2 V, and from 0.6 V to 1.2 V respectively, similar to that of the coarse TDC.

Figure 4-11 shows the results of the voltage sweep against the stage delay, or t_{res} . A similar trend from the coarse TDC is observed here, where a large t_{res} difference between all the $V_{P,bd}$ is observed in the middle of the V_P range, which starts very small at the start and ends with a slightly large distribution at the end of the V_P range. It is also observed that the maximum t_{res} of the fine TDC in figure 4-11 seems to be higher than that of the coarse TDC in figure 4-10. This is not an error, but is the effect of the Vernier principle. The coarse TDC has a *STOP cell* delay that is higher than that of t_F . Therefore, by subtracting t_{STOP} and t_F from t_{START} and t_S , it is no wonder that a larger maximum t_{res} is observed in the fine TDC. This can obviously be avoided by varying t_F , as is shown later in this section.

Figure 4-11 Influence of gate and body biasing voltage on fine TDC stage delay

The resolution of the CFTDC is targeted to be 1.08 ps, therefore Vbiasep should not exceed 0.2 V for Vbiasep1 at 0 V, even with the lowest V_{bd_biasep} of 0.6 V, and a zoomed-in view of the lower V_P range is shown in figure 4-12.

Figure 4-12 Zoom in view of the gate voltages that gives a CFTDC resolution of up to 1.08 ps

4.4.4 Effect of biasing on TDC resolution

In order to determine the voltage biases for the desired t_{res} , a pre-characterisation is necessary in two steps, first sweeping the gate voltage then the body bias voltage, for the reason that the range of t_{res} is largely dependent on the two V_P voltages. Therefore, both V_{biasp} and V_{biasp1} are first swept together (but not simultaneously) from 0 to 0.15 V, and the influence on the t_{res} .

Figure 4-13 shows the two-dimensional gate bias sweep where the body bias voltages are fixed at 1.2 V. We first see the starting point of both voltages at 0 V, which gives 0 t_{res} . As V_{biasp} increases, t_{res} increases due to t_S . As V_{biasp1} increases simultaneously, the t_{res} decreases due to rising t_F . This trend is similar to that in the VRTDC. Therefore, the increasing V_{biasp} (V_{biasp1}) reduces the V_{sg} on the PMOS, limiting the current through the inverter and therefore has a longer propagation delay. Increasing V_{biasp1} increases the t_F , therefore t_{res} decreases when both V_{biasp} and V_{biasp1} are increased together, i.e. the difference gets smaller until some point when t_F becomes larger than t_S and the resultant t_{res} goes negative.

Figure 4-13 Two-dimensional gate bias sweep versus CFTDC resolution

From figure 4-13, we pick two V_{biasp} values that will give some tuneability via body bias, 0.1 V and 0.11 V, and V_{biasp1} shall stay at 0 V. Next, the body biases of both t_s and t_F are swept from 0.6 V to 1.2 V, with a step of 50 mV. They shall be called V_{bd_biasp} and V_{bd_biasp1} respectively.

Figure 4-14 Two-dimensional body bias sweep versus CFTDC resolution

To re-emphasize, a higher Vbiasp will give a larger t_S , and with t_F being a constant, we expect t_{res} to be larger with Vbiasp = 110 mV. This is true as shown in figure 4-14. For the same $V_{P,bd}$ values, t_{res} is always about one y-axis division (or 0.5 ps) higher at Vbiasp = 110 mV (in orange) as compared to Vbiasp 10 mV less (in blue). By sweeping V_bd_biasp from 0.6 V to 1.2 V, t_S increases, and consequently so does t_{res} . This is observed in figure 4-14 by taking the first of the 13 points per V_bd_biasp and comparing them, the t_{res} increases (linearly) by slightly less than 0.5 ps. When V_bd_biasp1 increases from that first point of 0.6 V to the last point of 1.2 V, a linear decrement in t_{res} is observed. The same linear change in t_{res} due to body bias voltage is also seen in the VRTDC.

4.4.4.1 Determining the TDC resolution

As a target for the CFTDC, the resolution should be approximately 1.08 ps. To determine the correct bias values, a characterisation can be done by sweeping all four biases together. But it appears from figure 4-14 that both body biases must be adjusted. Is it possible to adjust only 1 body bias instead? And preferably that of the t_S cells since the gate bias is already adjusted from 0 V?

Vbiasp1 is fixed at 0 V anyway, so what value should Vbiasp and the two body biases take in order to achieve a resolution close to the target, with the goal of having only 1 varied body bias and the other at Vdd? Table 4-1 below shows 3 of the multiple possibilities.

Table 4-1 Table of gate and body biases to achieve the target CFTDC resolution

Set	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp (V)	V_bd_biasp1 (V)	t_{res} (ps)
1	0.15	0	0.86	1.2	1.079
2	0.06	0	1.2	0.8	1.076
3	0.1	0	1.2	1.2	1.062

4.4.5 Performance of CFTDC vs. temperature variation

We investigate the performance of the TDC under temperature variation, from -40 °C to 125 °C. An input of 211.2 ps was applied to the CFTDC for this investigation. Also, set 1 from table 4-1 was used. The variation of both TDC resolutions with respect to temperature are shown in figure 4-15. The orange

curve represents the fine TDC resolution, t_{res} and the blue curve represents the coarse TDC resolution which is $32 * t_{res}$, for ease of notation, it shall be referred to as t_C .

Figure 4-15 Variation of TDC resolution with temperature

The same trend is observed in both t_{res} and t_C , that the resolution becomes higher (or smaller in picoseconds) as the temperature increases. At high temperature, we expect that the threshold voltage to be lower than at cold temperatures, thus under the same supply condition, transistors tend to switch faster at higher temperatures and hence the smaller t_{res} .

Note that the V_{biasp_c} and $V_{bd_biasp_c}$ are 362 mV and 1.2 V respectively. Under room temperature and with these biases, t_C is 35.471 ps.

4.4.5.1 High Temperature calibration

It appears from figure 4-15 that both t_C and t_{res} are lower at high temperature than at room temperature, and need to be increased. Therefore, we first vary V_{biasp_c} in order to achieve the $t_{C,RT}$ under at 125°C. Since $t_{C,HT}$ is less than $t_{C,RT}$, the V_{biasp_c} has to be increased, this has already been elaborated earlier. Therefore, the gate bias voltage is swept from 360 mV to 460 mV in steps of 5 mV, and the change in $t_{C,HT}$ with V_{biasp_c} is shown in figure 4-16 below.

Figure 4-16 Change in coarse TDC resolution, t_C with gate bias sweep at 125°C

The required V_{biasp_c} has to be between 380 mV and 390 mV to achieve 35.471 ps. Therefore, this range is zoomed-in with a 1 mV step and shown in figure 4-17. The new V_{biasp_c} is 389 mV as shown by the orange dot in figure 4-17. No change in $V_{bd_biasp_c}$ was necessary.

Next, the $t_{res,HT}$ also needs to be increased. Therefore, according to the investigation results of biasing on TDC resolution, V_{biasp} has to increase, and V_{bd_biasp} has to increase. For that, the former is swept from the initial 0.15 V to 0.5 V, and V_{bd_biasp} is swept from 0.6 V to 1.2 V with a step of 50 mV and 100 mV respectively. The gate bias variation is represented by the various colours (as legend) in figure 4-18, and the body bias variation is shown in the x-axis.

Table 4-2 Table of swept voltage parameters of the fine TDC at 125°C

Set	V_{biasp} (V)	V_{biasp1} (V)	V_{bd_biasp} (V)	V_{bd_biasp1} (V)
1_HT	0.15 -> 0.5	0	0.6 -> 1.2	1.2

Figure 4-17 Further tuning to coarse TDC resolution, t_C with gate bias sweep at 125°C between 0.38 V and 0.39 V with marked out pass/fail points

Figure 4-18 Change in fine TDC resolution, t_{res} with body and gate bias sweep at 125°C

With reference to figure 4-15, it seems that $t_{res,HT}$ only has to be increased from 0.86 ps to 1.08 ps, which is about 0.22 ps. A 50 mV step in gate bias could well be too much, and for such a small improvement in the resolution, perhaps only

a body bias adjustment is necessary. This is observed in the results in figure 4-18. Firstly, the linear increment in Vbiasp results in a seemingly exponential increase in $t_{res,HT}$. This exponential increase is amplified as V_bd_biasp increases towards 1.2 V. This can be explained by the idea that t_{res} tends towards zero with a decreasing V_bd_biasp as seen in figure 4-14, and thus a smaller change in $t_{res,HT}$. Looking at all the Vbiasp results, clearly there is no need to raise Vbiasp to beyond 0.2 V where the smallest $t_{res,HT}$ is already above at 1.32 V. Thus, the Vbiasp should be kept at 0.15 V and V_bd_biasp shall be varied between 0.9 V and 1 V with a smaller step of 10 mV, as shown in figure 4-19. With that, it was possible to fix V_bd_biasp at 0.94 V (marked in orange). The final gate and body bias values at 125°C are tabulated in table 4-3.

Figure 4-19 Change in fine TDC resolution, t_{res} with body bias sweep at 125°C between 0.9 V and 1 V with marked out pass/fail points

Table 4-3 Final Gate and body bias set for T=125°C (with changed values marked in red)

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_HT	0.389	0.15	0	1.2	0.94	1.2

4.4.5.2 Low Temperature calibration

The same investigation so far on t_C and t_C should also be done at -40°C . At this extreme low temperature from figure 4-15, both t_C and t_{res} are higher than at room temperature, and need to be decreased. Therefore, we first vary V_{biasp_c} towards a lower value in order to achieve the $t_{C,RT}$ under at -40°C . The gate bias voltage is swept from 160 mV to 360 mV in steps of 5 mV, and the change in $t_{C,LT}$ with V_{biasp_c} is shown in figure 4-20 below. Similar to the case at high temperature, there is a range where $t_{C,LT}$ gets in the range of 35.471 ps, which is between 340 mV and 350 mV. For this purpose, V_{biasp_c} is further varied with a 1 mV step in this 10 mV range, and is marked by the red box in the figure. The final V_{biasp_c} (equal to 0.346 V) is marked in orange, and as in the case of high temperature calibration, the $V_{bd_biasp_c}$ does not need to be adjusted, i.e. it can remain unchanged at 1.2 V.

Figure 4-20 Change in coarse TDC resolution, t_C with gate bias sweep at -40°C with focussed tuning range marked in the red box and marked out pass/fail points

Next, the $t_{res,LT}$ also needs to be decreased. Therefore, according to the investigation results of biasing on TDC resolution, both V_{biasp} has to decrease. For that, we split the sweep in two steps to first check how much change V_{biasp} can bring to $t_{res,LT}$. V_{biasp} is swept from 0 to the initial 0.15 V while the other

three voltage biases remain the same. The result of the voltage sweep is shown in figure 4-21. It appears that the Vbiasp can be limited to just 0.14 V and 0.15 V, with some variation performed on V_bd_biasp. For the initial 0.15 V Vbiasp, the V_bd_biasp should be lower than 0.86 V, with little room before the 0.6 V limit. On the other hand, if Vbiasp was set at 0.14 V, then the corresponding V_bd_biasp must be increased between 0.87 V and 1.2 V.

Figure 4-21 Change in fine TDC resolution, t_{res} with gate bias sweep at -40°C (with chosen Vbiasp values marked in red box)

Table 4-4 Table of swept voltage parameters of the fine TDC at -40°C

Set	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_LT	0.15	0	0.6 -> 0.86	1.2
2_LT	0.14	0	0.86 -> 1.2	1.2

For the mentioned body bias sweep listed in the table below, the results are shown in figure 4-22. The orange curve represents Vbiasp at 0.15 V and the blue curve represents the Vbiasp at 0.14 V. Both curves are linear with change in V_bd_biasp, and have an offset of approximately 0.15 ps. The passed values for 0.15 V and 0.14 V are shown in yellow and orange colours respectively.

Figure 4-22 Change in fine TDC resolution, t_{res} with body bias sweep at -40°C with marked out pass/fail points

The final gate and body bias values at -40°C are tabulated in table 4-5.

Table 4-5 Final Gate and body bias set for $T=-40^{\circ}\text{C}$ (with changed values marked in red)

Set	Vbiasep_c (V)	Vbiasep (V)	Vbiasep1 (V)	V_bd_biasep_c (V)	V_bd_biasep (V)	V_bd_biasep1 (V)
1_LT	0.346	0.15	0	1.2	0.82	1.2
2_LT	0.346	0.14	0	1.2	0.88	1.2

4.4.5.3 Body bias as a function of temperature

We examine in this section body biasing as a function of temperature. The three body biases $V_{bd_biasep_c}$ of the coarse TDC, and V_{bd_biasep} and $V_{bd_biasep1}$ of the fine TDC are varied from 0.6 V to 1.2 V over a temperature range from -40°C to 125°C . The gate biases are not changed. The values are listed in table 4-6 below. The idea is to examine to what extent the body biases vary over temperature and their impact on the respective resolutions of the TDC.

Table 4-6 Table of swept voltage parameters of the CFTDC over temperature

Set	Vbiasep_c (V)	Vbiasep (V)	Vbiasep1 (V)	V_bd_biasep_c (V)	V_bd_biasep (V)	V_bd_biasep1 (V)
1	0.362	0.15	0	0.6 -> 1.2	0.6 -> 1.2	0.6 -> 1.2

We first look at t_c with respect to $V_{bd_biasp_c}$ and temperature. Figure 4-23 shows the change in t_c as temperature increases from -40°C to 125°C . The difference $V_{bd_biasp_c}$ are colour-coded and described in the legend. First it is clear that t_c decreases with temperature for most body bias voltages except 0.6 V and 0.7 V which increases and stays relatively stagnant over temperature. As the temperature increases, the gap between the various body biases also decreases. This means that the effected amount of change in t_c decreases as the temperature increases, but it does not mean that body biasing becomes more useless with higher temperatures.

Figure 4-23 Varying change of coarse TDC resolution with body bias sweep over temperature

The same trend could be observed in the fine TDC, where the gap between body biases is the smallest at 125°C and the biggest at -40°C . Figure 4-24 shows the results of a two-dimensional sweep of the body bias voltages in the fine TDC. In the x-axis, V_{bd_biasp1} is swept from 0.6 V to 1.2 V with every of the nine temperature points. At every temperature, the various seven colours represent the swept V_{bd_biasp} from 0.6 V to 1.2 V.

Another similar observation that can be made is the body bias voltage of 0.6 V at the temperature points at 105°C and 125°C . Firstly, as shown earlier, t_{res} decreases with increasing V_{bd_biasp1} at every temperature point and every

fixed V_{bd_biasp} voltage. On the change in t_{res} with respect to V_{bd_biasp} , it decreases with decreasing V_{bd_biasp} . As the temperature increases, t_{res} also decreases up to 85°C, where t_{res} for V_{bd_biasp} equal to 0.6 V starts to increase towards that at 0.8 V.

Figure 4-24 Varying change of fine TDC resolution with body bias sweep over temperature

4.4.6 Performance of CFTDC vs. supply variation

The CFTDC is put under voltage supply variation from 1 V to 1.4 V to investigate the change in resolutions due to changes in supply voltages. For the simplification of the investigation on supply influence, both $V_{bd_biasp_c}$ and V_{bd_biasp1} are fixed at 1.2 V. Figure 4-25 shows the change in t_C and t_{res} in blue and orange respectively. First, a common Voltage-Delay trend is seen, where the lower voltages result in highest delay and vice versa. However, it seems that t_{res} is already close to 100 ps at 1 V supply. Due to the fact the delay cells are designed to work at 1.2 V, the resolution as a result of 0.2 V below the nominal supply becomes too large to be tuned. Such low voltage operation is nevertheless possible, but requires some re-characterisation of the delay cell by varying the transistor sizes that make up the cell or simply just the current starving PMOS.

For that reason, the supply is lowered to only 90 % of the nominal supply, i.e. 1.08 V, and shall be called Vddlow. The maximum supply 1.4 V shall be called Vddhigh.

Figure 4-25 Variation in TDC resolution with respect to voltage supply

4.4.6.1 Low supply voltage calibration

Since t_C and t_{res} are higher at Vddlow than at nominal supply, it is necessary to reduce the gate and body bias voltages applied to both the coarse and fine TDCs. Vbiasp_c is first varied to improve t_C and shall be decreased from 0.362 V to 0 V in 5 mV step. In order to be more realistic with the calibration, both V_bd_biasp_c and V_bd_biasp1 are set the Vddlow value of 1.08 V.

The results are shown in figure 4-26, with t_C at nominal supply ($t_{C,Vddnom}$) shown in grey as reference, and the pass and fail $t_{C,Vddlow}$ in orange and blue respectively. The pass condition is set at ± 0.1 ps from $t_{C,Vddnom}$. It is also apparent that Vbiasp_c at 0.4 V and above only results in a higher $t_{C,Vddlow}$, which drifts further away from $t_{C,Vddnom}$. Of the two possible Vbiasp_c, 0.13 V is chosen for fine TDC calibration.

Figure 4-26 Change in coarse TDC resolution, t_C with gate bias sweep at Vddlow and Vddnom (as reference) with marked out pass/fail points

In order to lower $t_{res, Vddlow}$, Vbiasp and V_bd_biasp should be decreased, but in two steps. The former is first varied from 0 to 0.15 V in steps of 10 mV, and the resulting $t_{res, Vddlow}$ is plotted in figure 4.27. As a reference, $t_{res, Vddnom}$ is shown in orange. The Vbiasp at 0.09 V seems to be promising, with enough room for body bias to fine tune $t_{res, Vddlow}$. This is just slightly higher than $t_{res, Vddnom}$, so not much change is expected for V_bd_biasp.

Therefore, V_bd_biasp is swept from 0.8 V to the initial 0.86 V to lower $t_{res, Vddlow}$, and the corresponding resolutions are shown in figure 4-28 with the pass/fail criteria.

Table 4-7 Table of swept voltage parameters of the fine TDC at Vddlow

Set	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_Vddlow	0 -> 0.15	0	0.8 -> 0.86	1.08

Figure 4-27 Change in fine TDC resolution, t_{res} with gate bias sweep at Vddlow and Vddnom (as reference) with marked out pass/fail points

Figure 4-28 Change in fine TDC resolution, t_{res} with body bias sweep at Vddlow and new Vbiasp at 0.09 V (with marked out pass/fail points)

It is finally decided that the following bias set as listed in table 4-7 shall be used under Vddlow operation.

Table 4-8 Final Gate and body bias set for Vddlow (with changed values marked in red)

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_Vddlow	0.13	0.09	0	1.08	0.84	1.08

4.4.6.2 High supply voltage calibration

In contrary to Vddlow condition, both t_C and t_{res} are lower at Vddhigh, and it is necessary to increase the gate and body bias voltages applied to both the coarse and fine TDCs. Again, Vbiasp_c is first varied to improve t_C and shall be increased from 0.6 V to 0.7 V in 5 mV step. This range was chosen because an approximate estimation was made based on $t_C = 20$ ps at Vddhigh in figure 4-23. In order to be more realistic with the calibration, both V_bd_biasp_c and V_bd_biasp1 are set the Vddhigh value of 1.4 V. Figure 4-29 shows the Vbiasp_c sweep versus t_C for supply voltage at 1.4 V. As a reference, the $t_{C,Vddnom}$ is shown in blue

Figure 4-29 Change in coarse TDC resolution, t_C with gate bias sweep at Vddhigh and Vddnom (as reference) with marked out pass/fail points

Again, the pass criteria is set as ± 0.1 ps of $t_{C,Vddnom}$. While no pass $t_{C,Vddhigh}$ are observed in the swept range, one can narrow down Vbiasp_c to be approximately between 0.635 V and 0.64 V. A further interpolation reveals that Vbiasp_c should be set at 0.637 V, but not shown in figure 4-29.

Average of tres_ave

Fine TDC resolution @ Vddhigh

Y-axis: Fine TDC resolution [ps]

X-axis: Swept parameter: Gate bias voltage [V]

Fixed parameter: Body bias voltage [V]

Legend:

- Vdd: 1.2 - P (Blue)
- PF_tres: 1.4 - F (Orange)
- 1.4 - P (Grey)

Gate bias voltage [V]	Fine TDC resolution [ps]	Series
0.15	0.2	1.4 - F
0.25	0.8	1.4 - F
0.255	0.82	1.4 - F
0.26	0.85	1.4 - F
0.265	0.88	1.4 - F
0.27	0.92	1.4 - F
0.275	0.95	1.4 - F
0.28	0.98	1.4 - F
0.285	1.02	1.4 - F
0.29	1.1	1.4 - F
0.295	1.15	1.4 - F
0.3	1.18	1.4 - F
0.305	1.22	1.4 - F
0.31	1.28	1.4 - F
0.315	1.32	1.4 - F
0.32	1.35	1.4 - F
0.325	1.4	1.4 - F
0.33	1.45	1.4 - F
0.335	1.5	1.4 - F
0.34	1.55	1.4 - F
0.345	1.6	1.4 - F
0.35	1.65	1.4 - F

Table 4-9 Table of swept voltage parameters of the fine TDC at Vddhigh

For the operation under Vddhigh condition, i.e. Vdd at 1.4 V, the set of gate and body biases needed are listed in table 4-7.

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp 1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_Vddhigh	0.637	0.285	0	1.4	0.86	1.4

4.4.7 Performance of CFTDC vs. process variation

In order to determine the performance of the CFTDC under process variation, a Monte Carlo simulation was performed with a small number of 300 points. The idea was to check the variation in the resolution of the CFTDC under process variation and mismatch conditions, and to re-adjust the voltage biases in order to achieve the resolutions, t_C and t_{res} under typical process conditions. The lowest and highest D_{OUT} obtained were 102_{10} and 287_{10} with set 1 of gate and body biases described in table 4-1 respectively. In order to prove that the biases could overcome process variations and mismatch, the slowest corner was extracted for further simulation.

For the slowest corner with the lowest D_{OUT} , (i.e. corner 295), t_C and t_{res} of both the coarse and fine TDCs were too large. In order to reduce the resolutions, the applied biases have to be reduced. Therefore, we attempt this in two steps, first for the coarse TDC, then the fine.

The t_C before calibration under process variation is shown in figure 4-31, where the gate bias voltage is 0.362 V. For the coarse TDC to have a lower t_C , the gate bias V_{biasp_C} is reduced from 0.35 V to 0 V in 50mV steps, and the body bias voltage $V_{bd_biasp_C}$ from 1.2 to 0.6V in 100mV steps, as shown in table 4-10. The voltage sweep of both gate and body biases of the coarse TDC versus t_C is shown in figure 4-31 below. It requires that V_{biasp_C} be reduced to 0.25 V and $V_{bd_biasp_C}$ to 1.1 V.

Table 4-11 Table of swept voltage parameters of the coarse TDC under process variations

Set	V_{biasp_c} (V)	$V_{bd_biasp_c}$ (V)
1_MC	0 -> 0.35	0.6 -> 1.2

The t_{res} before calibration under process variation is shown in figure 4-32, where the gate and body bias voltages are 0.15 V and 0.86 V respectively. This is shown as the grey dot in the figure. In comparison, the yellow dot represents the target under no process variation. It is hence apparent that the t_{res} must be reduced, and this shall be done via V_{biasp} and V_{bd_biasp} , which are reduced from 0.35 V to 0 V, and 0.85 V to 0.6 V respectively, both in 50 mV steps. Table 4-11 shows the varied parameters and the ranges.

Figure 4-31 Change in coarse TDC resolution with gate and body bias sweep under process variation with marked out pass/fail points

Table 4-12 Table of swept voltage parameters of the fine TDC under process variations

Set	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_MC	0 -> 0.35	0	0.6 -> 0.85	1.2

Figure 4-32 shows how t_{res} changes with Vbiasp and V_bd_biasp variation. As expected, t_{res} increases as the former increases. And it is further increased, but in smaller steps, as V_bd_biasp increases. The Vbiasp_c is 0.25 V as already mentioned earlier.

In the figure are two orange dots which represent the voltage combination of Vbiasp and V_bd_biasp for a pass condition of t_{res} . Therefore, no adjustment to the other two voltage parameters are necessary. Either of the two orange points can be chosen, and the final set of voltages are given in table 4-12 below.

Table 4-13 Final Gate and body bias set under process variation (with changed values marked in red)

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
1_MC	0.25	0.05	0	1.1	0.65	1.2

Figure 4-32 Change in fine TDC resolution with gate and body bias sweep under process variation with marked out pass/fail points

4.4.8 Output characteristics of the CFTDC

The 9-bit CFTDC has a resolution of 1.08 ps and a dynamic range of 567.3 ps. The input signals *START* and *STOP* either be one-time triggered inputs or more useful as periodic signals as shown in figure 4-33. The time input, i.e. the delay between the rising edges of *START* and *STOP* for the results in this figure is 350 ps. A 100 ps low pulse in the periodic input signals is used to generate multiple reset signals via tree networks to not only reset all the digital circuitry in the TDC, but also *start_vernier* and *stop_vernier* input signals of the fine TDC. The rising edges of the said signals define the residual time from the coarse TDC, $t_{residue}$. Two of the multiple reset signals are shown in the figure, Rc1 and Rf1 which are generated from the low pulses of *START* and *STOP* respectively.

Also shown in the figure are two of the nine output bits of the TDC, of which MSB belongs to the four bits of the coarse TDC, and B2 the five bits of the fine TDC. Notice that MSB, B2, *start_vernier* and *stop_vernier* are all returned to zero with the reset signals. The last curve in the figure is the Vdd current profile, where two huge current spikes occur periodically. These two spikes are aligned to the reset signals Rc1 and Rf1. Recall that the mentioned signals are just two

of the many reset signals generated in the TDC, and the reset is done simultaneously to all the digital circuits, with the Rf-signals resetting more circuits. Therefore, we see a huge current spike in the Vdd for slightly more than the duration of the low pulse width. On the contrary, the two Vdd current spikes before 1 ns are a result of reduced resetting of circuits. The periodic peak currents are approximately 4.788 mA and 6.438 mA respectively.

Figure 4-33 Periodic T_{IN} generating periodic reset signals which are used to reset the CFTDC digital circuits as shown by the return-to-zero behaviour of the outputs and fine TDC inputs. Also shown is the Vdd current profile of the CFTDC

A characterisation of the latency of both TDC parts was done to check the maximum latency for the entire time input range with a step of 0.1 ps. This is the time delay between the input *STOP* signal of the respective TDCs and the last availability of the relevant output bits. For the coarse TDC, this is the delay between *STOP* and the last of upper four D_{OUT} bits, and for the fine TDC, between *stop_vernier* and last of the lower five D_{OUT} bits. The graphs are shown in figure 4-34. Voltage bias sets 1 and 2 from table 4-1 are used for comparison, notated as C1 and C2 respectively in the figure.

Figure 4-34 Latency of the coarse and fine TDCs across the entire time input range

The latency of the coarse and fine TDCs are shown in blue and orange, with the scales on the left and right of the graph respectively. Latency with a value of “-1” means that there was no change to the output bit. Recall that the initialised output is always 9'b000011111. Therefore, for the first 35 ps, the coarse output bits are always at logic zero, and should stay so. From the figure, the maximum latency of the coarse TDC is approximately 1.4664 ns, and that of the fine TDC is approximately 2.7589 ns. Due to the fact that the fine TDC is purely a vernier-based TDC, it naturally has a longer latency than the coarse TDC.

Notwithstanding, the total latency of the CFTDC is not a summation of both maximum latencies, and the maximum quantisation time is also not a summation of both values. This is because the maximum latency for both TDCs occur for different time input, as evident in the figure. In order to determine the sampling period of the TDC, the maximum time taken between *STOP* signal and the last of the five lower *D_{OUT}* bits must be checked for the entire time input range. Similarly, both sets 1 and 2 from table 4-1 are used, and notated as C1 and C2 respectively. The results are shown in figure 4-35, where the quantisation time for C1 and C2 are in blue and orange respectively.

Figure 4-35 Quantisation time of the CFTDC versus input range for sets C1 and C2

The longest quantisation time for C1 and C2 is 3.0917 ns and 3.4842 ns respectively. Notice that there is a 0 ns at two input points. Recall again the initial D_{OUT} , this is the same output value as that at input 35 ps. Therefore, for the first input point, there is no change in output value, and thus quantisation time is 0 ns. For the second input point of 567.6 ps, which is 0.1 ps more than the $T_{IN,max}$ of the TDC, there is an overflow, thus the D_{OUT} is also at 31₁₀, the initialised value. Therefore the Q-time is also 0 ns. This applies to both sets C1 and C2. Given the maximum quantisation time of 3.484 ns, and the additional 100 ps low pulse for the self-reset, the sampling period could be rounded to 3.6 ns.

Referring back to figure 4-33, the average current consumption is 1.49075 mA and the equivalent power consumption is 1.7889 mW. The sampling frequency can be calculated from the determined sampling period to be 277.778 MHz and the energy dissipated per mega-Hertz is therefore 6.44 μ W/MHz.

In terms of Figure-of-Merit (FOM) where it is defined as follows:

$$FOM = \frac{Power}{(2^N \times F_s)} \quad (4.17)$$

, where $Power$ is the average power consumption, N is the number of bits and F_S is the sampling frequency, the FOM for the proposed CFTDC is 0.01258 pJ/conv.

The results of the full range input sweep under room temperature and nominal supply is shown in figure 4-36. A time step of 0.108 ps (one-tenth of the TDC resolution) was used and a zoom-in view of the fine TDC characteristics is shown in figure 4-37.

Figure 4-36 Output characteristics of the CFTDC for the full input range

To investigate the DNL and INL of the fine TDC, an input sweep from 0 ps to 567.5 ps was applied to the CFTDC with a step of 0.1 LSB. The DNL and INL were assessed based on equations 3.12 and 4.17 respectively.

$$INL = \left(\frac{T_D - T_{zero}}{T_{LSB-ideal}} \right) - D \quad (4.17)$$

, where T_D is the time value represented by the output code D , T_{zero} is the minimum time input that corresponds to output code 0, and $T_{LSB-ideal}$ is the ideal LSB of the TDC, or ideal spacing between two adjacent output codes.

Figure 4-37 Output characteristics of the fine TDC for the full input range

The non-linearity results are shown graphically against output code for sets C1 and C2 in figure 4-38. A DNL of -0.9 LSB and an INL of 0.5/-1.4 LSB is obtained from the input sweep. The non-linearity parameters do not differ much between both bias sets.

(a)

(b)

Figure 4-38 (a) DNL and (b) INL of the proposed CFTDC of sets C1 and C2

Table 4-14 Comparison of the proposed CFTDC against the state-of-the-art TDC techniques

Reference	[76] CICC '15	[47] JSSC '13	[77] VLSI '07	[78] NEWSCA S '15	[48] JSSC '14	[81] JSSC '13	[54] JSSC '12	This work
Scheme	Time Amp.	Time Amp.	Two-step + Time Amp.		Pipelin e	Stocha stic	Cyclic	Two- step
Supply [V]	1.2	1.2	1	-	1.2	1.2	1.3	1.2
Resolution [ps]	2.6	3.75	1.25	1.2	1.12	4	1.25	1.08
No. of bits	8	7	9	9	9	10	8	9
f_s [MHz]	80	200	10	150/10	250	20	50	278
DNL [LSB]	1.84	0.9	± 0.8	0.67	± 0.6	-	± 0.7	-0.9
INL [LSB]	2.36	2.3	± 2	0.62	± 1.7	-	1/-3	0.5/-1.4
Power [mW]	2	3.6	3	8.299/0 .602 (sim.)	15.4	4.4	4.3	1.789 (sim.)
FoM [pJ/(conv. Step)]	0.098	0.463	0.586	0.108	0.325	0.215	0.336	0.013
Area [mm ²]	0.07	0.02	0.6	-	0.14	0.028	0.07	0.01
Tech. [nm]	65	65	90	65	65	130	130	65

One of the main motivation for the proposed CFTDC design was to decrease the quantisation period from 35 ns in the previously proposed VRTDC. By decreasing the quantisation period using the two-step approach, the sampling frequency was increased to 278 MHz. Similar to a parallel or pipeline operation, multiple-stage TDCs generally allow a higher sampling rate as seen in table 4-14.

Picoseconds resolutions are generally desired in current TDCs, and all the works presented do not have resolutions more than 5 ps. The CFTDC uses the Vernier principle coupled with gate and body biasing to achieve this high resolution. Theoretically the resolution could be reduced to femtoseconds, but the arbiters will set the limitation on the resolution for this design. The digital-intensive design of the CFTDC made it possible to keep the area small, and in comparison to the VRTDC in chapter 3, the use of triple-well NMOS is removed here.

The non-linearity parameters are comparable with other designs, with the DNL slightly higher, in absolute terms. Granted that the power consumption is a simulated value and the FoM may not be the best point of comparison. Nevertheless, together with the energy consumption per Megahertz, it gives an insight to the dynamic performance of the CFTDC.

In comparison to the other works, the operating supply voltage is more or less the commonly used value. Note that the supply voltage has a direct impact on resolution performance. Schemes that utilise delay cells whose propagation delay is directly dependent on V_{dd} will have a $1/V_{dd}$ influence on its delay and hence resolution. The use of the Vernier Principle reduces this influence to an indirect way, whereby through the delay difference of two delay cells per stage, some V_{dd} -dependency is removed through this offset. For operations under lower supply voltages, a re-adjustment of the delay cells is required for optimal re-centring of the delay to cater for further supply variation.

One of the biggest trade-off for the proposed TDC is the necessity to provide multiple voltage biases to achieve the desired resolution. On the other hand, this disadvantage is useful when it comes to PVT variation to resolve the

influence on resolution. The PVT influence on the TDC resolution is not mentioned in some of the works listed in Table 4-14, and/or how it can be resolved.

A discussion of the power and area trade-off is perhaps interesting because the TDC boasts of full-digital architecture designs and the difference in the TDC quantisation methodology certainly plays a role in the area and power consumption.

In [76], the sampling frequency of 80 MHz is achieved because of the use of two VCOs for time stretching. The TDC stretches T_{IN} by N , the number of parallel NAND gates per delay stage. Similar to a Vernier Ring TDC in the previous chapter, the latency is long because it was necessary to wait for N times the input time interval before the quantisation could be started. The use of NAND gates, and the simplicity of the design enables the area consumption to be kept small. The power consumption is low due to its digital means in time amplification.

In comparison, the approach used to amplify time in [77, 78] is more analogue, where the metastability of an SR latch is used, with some capacitors or MOS-capacitors used to achieve the amplification factor. One of the shortfalls of using metastability as described earlier is the unpredictable gain. What is to be observed here is the also the shift to the time amplification method towards digital means, which is one of the reasons for more predictable gain, smaller area and lower power consumption. This is shown in figure 5 presented in [76] and the comparison of its TDC performance in figure 12 of the paper.

The area consumption in [77] is relatively large not only due to the 90 nm technology used, but also because of the use of switchable NMOS and PMOS capacitors at the output of the SR latch to achieve the high gain required. The sampling frequency of 10 MHz yields a power consumption of 3 mW which is relatively high as compared to other works. On the other hand, the power consumption in [78] is lower. Two sampling frequencies and the corresponding power consumption are given. Based on the two points, it is not possible to predict if the relationship between sampling frequency and power consumption is linear or not. Therefore, it is only possible to predict that the latter has a higher

power consumption than the digital approach for time amplification, but not how much more.

Another method digital time amplification is also presented in [47] via N pulses. This pulse-train time amplification TDC could achieve high sampling frequency because the TDC actively and simultaneously quantises the T_{IN} as it gets amplified. In this case, the latency is minimised. Similar to [76], the design is simple and the area consumption is only a fraction. One possible reason is the use of pseudo-nMOS structures in most of the logic circuits other than the delay cells.

A similar concept in [47] was used in [48] with the additional use of pipelining. The use of pipelining was aimed at increasing the sampling frequency while performing time addition and subtraction. The proposed 4-stage pipeline TDC has an increased power consumption, with three pipeline stages and one stage delay line TDC. When compared to a single-stage Time Amplification TDC in the former, the latter has a power consumption 4.28 times higher. This roughly correlates to the number of stages used. The use of Digital-to-Time Converter (DTC) in every of the pipeline stage for time addition and subtraction has also resulted in an increased area consumption.

In [81], the sampling frequency is at 20 MHz, not because of the capability of the Stochastic TDC, but the application of the TDC in the digital PLL which only requires 20 MHz as the reference frequency. The TDC alone consumes only 0.028 mm² area. A capacitor bank with differential MOS-capacitors is used to achieve the programmable delay under process variations. Even for the used technology node of 130 nm, the area consumption of the TDC core is rather small. The large part of the power consumption comes from the 5-bit fine Stochastic TDC due to the simultaneous switching of all 32 arbiters, leveraging on the metastability nature to achieve the TDC resolution.

The cyclic TDC in [54] adopts the cyclic ADC concept, where a DAC in a feedback loop is used to perform the time-digital-time conversion, data subtraction and residue amplification, similar to the analog-digital approach except that the data is in the time-domain. A maximum of 100 MHz sampling frequency can be achieved with the open-loop time amplification, despite the

cyclic approach which in the ADC architectures is relatively slow. The power consumption is actually not very much higher than the other TDCs that have sampling frequency below 100 MHz, but the FoM is slightly at the higher end of the spectrum due to the lower number of bits and higher power consumption.

4.5 Conclusion

The proposed Coarse-Fine TDC was intended to be used in a time-based ADC, where a shorter sampling period was needed. The VRTDC presented in the previous chapter has the problem of latency and due to the Vernier principle and ring structure. But the Vernier principle coupled with voltage biasing is a good strategy to achieve very small picosecond resolution, where it has been shown that by bringing t_S and t_F close to each other, single digit picosecond resolutions can be achieved. Where voltage biasing is concerned, reverse biasing the source-body potential can help bring about some linear voltage-time relationship. Also, when gate biasing becomes too limited in achieving very minute difference in t_S and t_F (which determines the resolution of the TDC), the body-biasing technique can achieve that. That is why it is a fine tuning mechanism to the TDC. The proposed CFTDC does away with NMOS body-biasing, thus reducing the size of the delay cells and the need and complexity of multiple biases. It also shortens the sampling period by breaking up the quantisation into two steps, reducing the number of bits per TDC and therefore reducing the latency that is dependent on bit size.

The biasing in the CFTDC also provides for a calibration to the resolution under PVT variations. Under different process, temperature and supply voltage variations, the resolution of the CFTDC can be influenced greatly as already shown. With gate and body biasing voltages, the resolution can be re-calibrated, thus providing some degree of immunity against PVT variations.

With regards to the chosen architecture of the TDC, time amplification could have also been implemented in a two-step TDC. However, there is much uncertainty in the amplification factor under PVT variations. A two-step architecture requires the maximum time input of the fine TDC to be exactly one-bit of the coarse TDC, otherwise this leads to linearity issues. The proposed

CFTDC uses a multiplexer network that minimises the addition of delay into the residual time to the fine TDC, and is a copy for both input signals, thus reducing mismatch and additional delay.

Apart from the current starving delay cells, the entire TDC core is implemented with digital circuits, allowing the design to be built on modular blocks for compactness. Nevertheless, the simultaneous switching of multiple digital circuits in parallel, for example multiple resets can result in large dynamic current consumption. The proposed 9-bit CFTDC has an average power consumption of 1.7889 mW with a sampling frequency of 333.333 MHz.

5 TDC-based Voltage-to-Time Conversion

5.1 Introduction

Traditional methods of analogue-digital conversion quantise data in the voltage domain. With advanced (scaled) CMOS technologies, the voltage domain quantisation becomes more difficult with down-scaling voltage supplies but stagnating noise levels, therefore reducing the SNR. Many designs rely on bulky calibration (backend and frontend) circuits to improve the analogue performance, with many taking the form of digital calibration. On the other hand, unconventional method of using time-domain for quantisation is gaining popularity in the form of VCO-based ADC. Time-domain quantisation leverages on the faster switching speed of transistors with advanced nodes,

In order to use the TDCs for data conversion, a preceding block is necessary to first convert voltage to time to maximise the potential of time quantisation. “Time-mode ADC” is another name is given to such data conversion architecture. Many Voltage-to-Time Converter (VTC) designs in the literature mainly revolve around voltage-controlled oscillator (by means of a voltage-controlled current source), ramp signal generation (with a constant current source) and voltage-controlled capacitance with the aim of producing high linearity of voltage against time.

Traditional voltage-to-time conversion uses a voltage-controlled oscillator (VCO) to generate pulses from sampled input voltages, somewhat like a pulse-width modulation (PWM). These pulses are then quantised by the TDC to obtain a digital representation of the sampled voltages. However, the voltage-time relationship is inherently non-linear and becomes a bottleneck to the linearity of a time-mode ADC. The linearity of the time-mode ADC can be solved by calibration or in many cases restricting the input voltage to a very small range that exhibits an acceptable amount of linearity between voltage and time.

Alternatively, ramp signal generation is gaining popularity in generating time delay from a reference time point. The ramp technique is used because of its higher linearity over the other two techniques. A ramp signal is usually generated by a current source and compared against the input voltage which is set as the threshold. When the ramp voltage exceeds the input voltage, the

output of the comparator is switched. The time taken from the start of the ramp until the comparator output is switched is recognised as the time delay representation of the input voltage, T_{IN} . In this design, the output response time of the comparator for the desired range of input voltages is added to the represented time T_{IN} . Two considerations are necessary for using the ramp technique for voltage-to-time conversion. First, the output response time of a comparator that is usually voltage level-dependent must be voltage level-independent, i.e. constant response delay. This allows then the response delay to be systematically removed from T_{IN} for all input voltages. Second, the maximum ramp time must fit the maximum T_{IN} of the TDC used. If a high resolution TDC is used, a ramp-up time in the range of nanoseconds is usually more than $T_{IN,max}$ of the TDC.

5.2 Concept

The proposed TDC-based VTC uses a TDC in its feedback loop to tune a raw generated T_{IN} . The graph in figure 5-1 shows the objective of this concept. The red curve which represents the non-linear voltage-to-time relationship will be fitted to the blue line that represents a linear relationship between delay and digital. $T_{IN,max}$ is defined for some $V_{IN,min}$ and $D_{OUT,max}$. Figure 5-2 shows the block diagram of the proposed TDC-based VTC. The building blocks of the proposed VTC includes:

- Dual-mode delay generator
- Time-to-Digital Converter (TDC)
- Output Data Latch
- Digital-to-Analogue Converter (DAC)
- Comparator
- Up-Down Encoder

The dual-mode delay generator first generates a raw delay representation T_{IN} of the input voltage in analogue-mode. This delay is fed into the TDC to obtain a digital representation of the input voltage, D_{OUT} . This binary data is converted back into an analogue voltage V_{DAC} and compared with V_{IN} . The result of the comparison determines how the T_{IN} should be adjusted so that V_{DAC} eventually

5.2.1 Dual-mode delay generator

155

in the analogue mode and this results in a coarse generated delay, this is a raw time representation of the input voltage $T_{IN,raw}$. This delay generator also has varactors that are controlled by digital bits in the digital mode to load the delay line, and add or remove a much finer delay than the coarse delay from the raw $T_{IN,raw}$. Figure 5-3 illustrates simply the two modes in the delay generator.

In the analogue mode, the input to the delay generator is the input voltage, while in the digital mode, the input are the sixty digital input bits, $D_{in}[59:0]$ that switch on and off all the varactors in the delay line. The output of the delay generator is a pair of two rising edge signals, $start_out$ and TDC_stop that serve as input to the TDC. The delay difference between the two signals define $T_{IN,gen}$:

$$T_{IN,gen} = TDC_stop - out_start \quad (5.1)$$

where out_start and TDC_stop are two rising edge signals.

Figure 5-3 Simplified diagram of the dual-mode delay generator to illustrate the two modes

The purpose of the dual-mode delay generator is to first establish an approximate voltage-time relationship between V_{IN} and $T_{IN,gen}$. However this initial generated delay is not linear with respect to V_{IN} and cannot be used to represent the input voltage accurately. Therefore, using some digital bits from the feedback system to “fine tune” $T_{IN,gen}$, this relationship can be linearized as much as possible.

The second issue with V-T conversion is the non-inverse relationship. A low V_{IN} will yield a large $T_{IN,gen}$, and vice versa. The structure of the delay generator cells is also aimed at resolving this non-inverse relationship, which will be explained in more details in the section on circuit implementation. For now, note that the delay generator will yield a low $T_{IN,gen}$ for a low V_{IN} , and a high $T_{IN,gen}$ for a high V_{IN} . Together with the digital D_{in} bits, the maximum $T_{IN,gen}$ is obtained by having

a maximum V_{IN} and all bits set to “1”. On the other hand, a minimum $T_{IN,gen}$ is obtained by having a minimum V_{IN} and all bits set to “0”.

5.2.2 Time-to-Digital Converter

A TDC is connected to the delay generator for time quantisation in the feedback loop for the purpose of converting time data into digital data. As already mentioned, voltage and time are inherently inversely-proportional, i.e. minimum V_{IN} results in maximum delay, and vice versa. Therefore, the output of the TDC has to be inverted to generate a $D_{OUT}[8:0]$ that correctly represents the voltage input and generated time delay. But the delay generator is built in such a way that the non-inverse V-T relationship is applied, thus removing the need to manipulate the output of the TDC, whose relationship between input time and output data is inherently non-inverse.

A consideration is that with the maximum $T_{IN,gen}$ should match to the maximum $T_{IN,max}$ of the TDC. If the maximum $T_{IN,gen}$ exceeds $T_{IN,max}$, the TDC no longer quantises time inputs more than its maximum value, which is an overflow condition. Recall from the previous chapters that the T_{IN} of the TDC is defined as the delay difference between two rising edge signals, TDC_start and TDC_stop . The first rising edge signal, TDC_start passes through a delay line with fixed propagation delay and waits for TDC_stop to overtake it somewhere along the delay line. Should this never happen within the maximum delay of the delay line, no time quantisation can take place. For this reason, $T_{IN,max}$ must be obtainable from the delay line.

However, because the delay generator has some room of delay tuning, the real condition for $T_{IN,max}$ is that the $T_{IN,gen}$ as a result of maximum V_{IN} and all D_{in} bits set to “0” should not be larger than $T_{IN,max}$. On the other hand, the $T_{IN,gen}$ as a result of minimum V_{IN} and all D_{in} bits set to “0”, should not be larger than $T_{IN,min}$. These two conditions ensure some tuneability for $T_{IN,gen}$. Figure 5-4 illustrates this concept graphically.

Figure 5-4 Concept of delay trimming with respect to TDC input

$$T_{IN,max} \geq V_{IN,max} \& \min(D_{IN}) \quad (5.2)$$

$$T_{IN,min} \leq V_{IN,min} \& \max(D_{IN}) \quad (5.3)$$

The number of D_{in} bits is decided based on the amount of delay obtainable across the entire V_{IN} range and the amount of trimming that can be applied to $T_{IN,gen}$, while ensuring that it is kept within the TDC range.

5.2.3 TDC offset

At the minimum V_{IN} , the minimum delay is obtained, but it is never equal to zero. In other words, some finite delay exists even if V_{IN} is set to minimum, with minimum D_{in} , which should otherwise ideally reflect 0 ps T_{IN} . This finite delay will result in some TDC output value which must be offset away. It also means that $T_{IN,gen}$ will always have this finite delay regardless the V_{IN} value.

Therefore, a delay offset, T_{offset} must be added between the delay generator and the TDC to remove that non-zero delay at minimum V_{IN} . This offset is necessary in nulling $T_{IN,gen}$ at $V_{IN,min}$ so that the generated delay is independent of the finite delay, and will fit into the dynamic range of the TDC for all valid V_{IN} . Doing so also ensures that maximum V_{IN} generates a delay that is within the TDC quantisable range, assuming that maximum T_{IN} matches to $T_{IN,max}$. Given that:

$$TDC_start = out_start - T_{offset} \quad (5.4)$$

$$T_{IN,gen} = TDC_stop - out_start \quad (5.5)$$

$$T_{IN,gen} = (TDC_stop - TDC_start) + T_{offset} \quad (5.6)$$

$$T_{IN,gen} = T_{IN} + T_{offset} \quad (5.7)$$

5.2.4 Low pulse generator

The TDC requires its input signals to be on the rising edge; *TDC_start* and *TDC_stop* input signals should always start from a low logic level, so that the rising edges can be recognised. Therefore, the output signals generated by the delay generator must include low pulses, so that they appear to the TDC as refresh signals every time after a T_{IN} is generated. Low pulses in the input signals are also necessary to reset the internal circuitry of the TDC to remove the logic states from the previous quantisations.

This low pulse should be implemented in the input signal to the delay generator, *in_delayed* so that both *TDC_start* (*out_start*) and *TDC_stop* will also have the low pulses. Referring to figure 5-2, *in_recycled* is a clock signal for the up-down encoder and is also used to feed the delay generator. Therefore the low pulse should only appear in the chain of high and low pulses when $T_{IN,gen}$ is completely defined by the delay generator. For that reason, *TDC_stop* signal is used to activate the low pulse generator which generates the low pulse after some picoseconds. If *TDC_start* or *out_start* was used instead, the low pulse will be generated before *TDC_stop* can be generated and half the TDC internal circuitry that uses the low level of *TDC_start* signal to be reset (primarily the coarse stage circuitry) will be reset to initial state, and no quantisation can take place.

Another consideration is that the delay between the rising edge of *TDC_stop* and the falling edge when the low pulse occurs should be long enough for *TDC_stop* to be arbitrated by the arbiters in the TDC. Without meeting this requirement, the arbiters will be reset by the low pulse before the output states can be decided.

Figure 5-5 below shows a timing diagram of the low pulse generation in *TDC_start* and *TDC_stop*. The rising edge of the latter activates the reset sequence on the *in_delayed*. Due to some finite delay between *out_start* and *TDC_stop*, the fine TDC will have time to quantise the residual time before the circuitry related to the fine TDC is reset by the falling edge of *TDC_stop*. Note that *TDC_start* is a result of *out_start* less the T_{offset} .

Figure 5-5 Timing diagram of the low pulses in TDC_start and TDC_stop (not drawn to scale)

5.2.5 Comparator

The comparator primarily compares V_{IN} , the input voltage of the VTC and V_{DAC} , the feedback voltage. The output of the comparator is a one-bit digital signal, LR . The comparator constantly monitors the two voltages and its output determines how V_{DAC} should be tuned. The goal is to equalise V_{DAC} with V_{IN} , with the latter as the reference. The logical expression for the output signal is as follows: $LR == 1$ IF ($V_{IN} < V_{DAC}$). LR is used as an input parameter by the up-down encoder to determine the direction of change of the $D_{in}[59:0]$. When LR is at a logic high state, V_{IN} is less than V_{DAC} , and the latter should be decreased. On the contrary, when LR is a logic low state, V_{DAC} must be increased. This is done through the Up-down Encoder.

Due to a large $T_{IN,gen}$ obtained from low input voltages, this places a limit to the input voltage range of the proposed VTC, from 0.5V to 1.2V. Therefore, the comparator only has to operate within this input voltage range. Unlike the issues pertaining to the propagation delay in a ramp generator VTC, this design has immunity against varying output response time as a result of different input voltages. Notwithstanding, the output response time also cannot be too long, which will lengthen the quantisation cycle, resulting in a lower sampling frequency.

5.2.6 Up-Down Encoder

The up-down encoder sets the high or low states of the 60 digital input bits. It requires as its input the comparator output, a global clock signal, a reset signal and an overflow flag. The latter is generated by the TDC when T_{IN} exceeds $T_{IN,max}$, hereinafter referred to as $S16$. The overflow detection scheme will be explained later in this section.

As explained earlier, the fine tuning of the delay $T_{IN,gen}$ is done via digital means, and it is intended that every tuning step only sees one bit change in the TDC. In other words, no more than one bit should change its state at any instance. The bits are shifted either left or right, one bit per tuning step. Whether the bits are shifted left or right is determined by the comparator output, LR . If the comparator output is high, i.e. $V_{IN} < V_{DAC}$, the D_{in} bits have to shift left, illustrated by the red arrow in figure 5-6. Shifting the bits to the left increases the number of 1s in the 60-bit thermometer code, and therefore increases $T_{IN,gen}$ from the delay generator. A longer $T_{IN,gen}$ results in a lower TDC output $D_{OUT}[8:0]$ due to the inversion of the data as mentioned earlier. Consequently, the DAC generates a lower V_{DAC} voltage, until it equalises with V_{IN} . Essentially, the up-down encoder is a 60-bit shift register that shifts one bit at a time, depending on the comparator output.

The sixty shift registers are given default logic states during a global reset. Half of them are reset to 0, and the other half are preset to 1, i.e. $D_{in}[59:0] = 60'h000_0000_2FFF_FFFF$, laid out in thermometer code form. The purpose of doing so is that the left and right extreme are equidistance away and takes less effort and time to shift than if all bits were set to 0 and 1s had to be shifted left till the end, or vice versa.

Figure 5-6 Concept of up-down encoding by shifting D_{in} bits right and left respectively

5.2.6.1 Overflow detection scheme

When T_{IN} exceeds $T_{IN,max}$, flag $S16$ is raised high, and the TDC is unable to quantise the time input data. $S16$ is obtained from the arbiter output in the TDC from the last delay element. $T_{IN,gen}$ should thus be reduced so that T_{IN} falls back into the range of $T_{IN,max}$. Reducing $T_{IN,gen}$ is done only in digital mode. The

analogue component of $T_{IN,gen}$ is not modified because the delay generator has been characterised to ensure that the input voltage range will never exceed the $T_{IN,max}$ for a certain D_{in} value. An overflow detection scheme has been built into the Up-down Encoder because it is known that maximum V_{IN} and maximum D_{in} bit settings will yield $(T_{IN,gen} - T_{offset}) > T_{IN,max}$, and with the maximum V_{IN} and minimum D_{in} , $T_{IN,gen}$ will not exceed $T_{IN,max}$.

In order to reduce $T_{IN,gen}$, the encoder resets all D_{in} bits to logic-0, to generate zero delay via digital mode with whatever V_{IN} in analogue mode. In the presence of a logic-high $S16$, all the sixty registers are reset to 0 any time during a quantisation, regardless of the state of shifting inside the encoder. In other words, an activated $S16$ will overwrite $D_{in}[59:0]$ immediately with 64'h0.

5.3 Circuit Implementation

This section explains the circuit implementation of the key blocks in this VTC concept and how the individual concepts that have been elaborated in the earlier section are fulfilled.

5.3.1 Dual-mode delay generator

The input to the delay generator is a single rising edge signal, $in_delayed$, and the outputs are $start_out$ and TDC_stop . The delay between both signals define the TDC input, $T_{in,gen}$ before offset. Principally, the delay generator extends the input rising edge by x -volts and y -bits. Therefore, $start_out$ (in figure 5-2) is a buffered output of $in_delayed$, and TDC_stop is the output at the end of the delay line – two outputs generated from one input.

In order to achieve the capability of setting delay by V_{IN} and tuning D_{in} , each of the thirty delay cells in the delay line must have its propagation delay adjustable by two means. It is primarily made up of an inverter, whose output is connected to an NMOS switch connected to a MOS capacitor, and two varactors connected in parallel to load the inverter via V_{IN} and the digital bits respectively.

Figure 5-7 Schematic diagram of two delay cells, each with two input digital bits

In the analogue mode, the V_{IN} is the gate voltage that sets the rate of charging current to the load capacitor. The MOS capacitor is implemented with an NMOS whose gate is connected to the source of the shunt NMOS and its other terminals to ground. The MOS capacitor is sized such that with the minimum V_{IN} , the cumulative propagation delay from all the cells will be less than the maximum time input to the TDC; voltage and delay have an inverse relationship. The shunt NMOS should be sized large enough to provide sensitivity of the added delay with respect to change in V_{IN} . On the rising edge of In , the current from the output node of the first inverter is sunk through the NMOS of the inverter. If the V_{IN} voltage is large, a large current from the same output node is sunk through the shunt NMOS, leaving a small current for the NMOS of the inverter. On the contrary, if the V_{IN} voltage is small, then thus current through the shunt NMOS is smaller in comparison, and more current is sunk through the inverter NMOS. Based on this, the output node of the inverter thus switches faster if V_{IN} is smaller than if V_{IN} was larger. The same principle works also for a falling edge of In . Therefore, adding a MOS capacitor also enables a non-inverse V-T relationship for every delay cell.

For the digital mode, two varactors are connected to the output of the inverter to tune the delay time of each delay cell in addition to the analogue input control. The varactors are implemented as a two-input NAND gate [82]. One input of the NAND gate is connected to the output of the inverter, and the other is to a D_{IN} bit. Therefore, one delay cell will have two D_{IN} bits connected to it.

The tuning delay step has to match the resolution of the TDC. If the tuning delay is twice the TDC resolution, half the number of TDC bits are wasted, i.e. 4.5 bits of the used 9-bit TDC, since every step change in the delay generator will result in two step changes in the TDC. If the tuning delay is half the TDC resolution, then D_{IN} has to increase (or decrease) two steps to effect one step increment (decrement) in the TDC, i.e. half the number of D_{IN} bits are wasted. The output of the NAND2 gate is not connected to any node. With one of the input connected to the inverter output, setting the other input (D_{IN} bit) to high increases the load capacitance of the inverter, but in a much finer way than in the analogue mode. The transistors in the NAND2 gates are sized in a way that the tuning delay can be obtained as close to the TDC resolution, as compared to the other logic gate topologies.

The maximum T_{IN} must match $T_{IN,max}$, and given the inverse voltage-time relationship, maximum $T_{IN,gen}$ will be obtained at maximum V_{IN} . For the maximum input voltage of 1.2 V, the $T_{IN,max}$ of the TDC determines the number of delay cells necessary in the delay generator with such a structure, i.e. with a shunt NMOS and MOS capacitor at the inverter output. The determination of the number of delay cells and trim bits is clarified in the Results section.

It is also important for the delay generator to have a defined input range, for the range determines if the number of trim steps are enough to adjust $T_{IN,gen}$ to fit within $T_{IN,max}$. Also, the range defines not only the operating range of the DAC, but also the required reference voltage of the TDC offset.

As mentioned earlier, a delay offset (TDC offset) block is added between the delay generator and the TDC to remove the non-zero delay. This offset block is implemented by replicating the same delay line with the same delay cell in figure 5-7. However, V_{IN} of this block, or the reference voltage is permanently connected to the lowest V_{IN} , and all digital input bits are set to low. Ideally, since the same delay line is used, a zero T_{IN} can be expected under the aforementioned conditions.

Since T_{IN} is defined between the rising edges of TDC_start and TDC_stop , the offset should be implemented on the $start_out$ signal. Delaying the rising edge of $start_out$ signal by T_{offset} reduces the delay difference between TDC_start and

TDC_stop , and can therefore achieve the maximum T_{IN} allowed by the TDC. For this reason, only $start_out$ passes through the TDC offset circuit.

5.3.2 Low pulse generation

In order to generate the low pulses for TDC_start and TDC_stop , a pulse generator comprising of some delay cells and a NAND gate is used. TDC_stop activates the pulse generator and there are two requirements: first, the pulse width should be long enough to reset the TDC circuitry and second, the time between the rising edge of TDC_stop and falling edge of the pulse should be long enough for the arbiters in the TDC to correctly determine their output states.

Figure 5-8 Low pulse generation for TDC input signals

In the implementation of the pulse generator in figure 5-8, a D flip-flop, a cascade of delay buffers, an inverter and a two-input NAND gate are used. The output of the pulse generator, $in_recycled$ is a clock signal for the up-down encoder and also feeds the delay generator after some delay. It is also used to reset the D flip-flop which has an active-low reset.

5.3.2.1 Delay buffers

A delay buffer in the pulse generator is made up of a current-starved inverter with PMOS and NMOS stack transistors and a 2-input NAND gate as a load – same NAND2 gate used in the dual-mode delay generator.

To provide the gate biases, the drain of a diode-connected PMOS is connected to an NMOS whose gate voltage is supplied externally shown in figure 5-9. For this design, the gate bias shall be connected to V_{dd} . This is sufficient to provide the required low pulse width.

One of the two inputs of the NAND gate is connected to the output of the delay buffer and the other is connected to LOGIC0 (or ground) to obtain D amount of delay. The low pulse width is set as $2D$, which is approximately 270 ps.

Figure 5-9 Delay buffer used in the low-pulse generator

5.3.2.2 Pulse refresher

Usually a low pulse generation requires only some inverters and a logic gate. However in this design, since the *TDC_stop* is a “recycled” signal between the delay generator and the pulse generator, the low pulse slowly reduces after every cycle and finally disappears, possibly due to the ever-decreasing gradient of the rising edge of the *TDC_stop* signal. Therefore, a pulse refresher is needed to keep the integrity of the low pulse. This is achieved by inserting a positive edge-triggered D flip-flop before the buffers, and connecting the input of the flip-flop to LOGIC1 and using *TDC_stop* as the clock signal. With this configuration, the pulse generator works exactly as it should with and without a flip-flop, with the benefit of an always consistent rising edge slope generated by the flip-flop.

The flip-flop output has to return to zero when the low pulse is generated. Since the flip-flop is positive edge-triggered, a falling edge does not trigger an output. Therefore, the NAND2 output is connected to the active-low reset of the flip-flop so that the output can return to zero.

5.3.3 Output Data Latch

When the TDC is reset, the output of the TDC $D_{OUT}[8:0]$ will be 9'b111100000. The coarse TDC bits are all set to logic-1 while the fine TDC bits are all set to logic-0. This means that whatever the result of the time quantisation was, the TDC 9 bits are reset to the default value on the falling edges of *TDC_start* and *TDC_stop*. This is shown in figure 5-10. It follows that V_{DAC} is reset to 480₁₀ or

1.156V at every reset phase. The dotted line in the V_{DAC} curve shows the reset voltage. Note that the timing diagram is not drawn to scale. These peaks may result in the comparator making a wrong assessment of the V_{DAC} voltage levels.

Figure 5-10 Timing diagram of the TDC output and V_{DAC} (not drawn to scale)

On the other hand, figure 5-11 shows the how V_{DAC} only changes when the $D_{OUT}[8:0]$ change. The dotted grey lines show the TDC output bits and V_{DAC} without an output data latch for comparison. The output latch is implemented as an array of D flip-flops, with the clock signals generated from the TDC input signals (see figure 5-12). CLK_C that is inverted from TDC_start will latch the four coarse TDC bits, while CLK_F that is inverted from TDC_stop will latch the five fine TDC bits. Intuitively, one can expect that the D_{OUT} from the current time quantisation cycle will only be latched on the next time input sample. Therefore, the V_{DAC} value is always one cycle slower than D_{OUT} .

The DAC used here is an R-2R architecture which has to work within the determined input voltage range. This range is discussed in the Results section.

Figure 5-11 Timing diagram of the TDC output and V_{DAC} with an output latch (not drawn to scale)

Figure 5-12 Output Latch is implemented as an array of D flip-flops

5.3.4 Up-down Encoder

The sixty D_{in} bits are in thermometer code form. The Up-down Encoder decides how many 1s and 0s should be in the string of 60 bits. There are 60 shift register cells in the Up-down Encoder, each with an active-low reset $clrb$, active-low preset $preb$, shift flag LR and two inputs.

Each shift register cell is made up of a D flip-flop with $preb$ and $clrb$, and three two-input NAND gates. The combinational logic for the D-input of the flip-flop is determined in the following way and implemented by only NAND2 gates:

$$D_i = LR \cdot Q_{i-1} + \overline{LR} \cdot Q_{i+1} \quad (5.8)$$

The two inputs for every shift register cell come from the output of the proceeding and subsequent shift register cell, i.e. cell_i takes inputs from Q_{i-1} and Q_{i+1}, where $i = (2, 3, \dots, 59)$, with the exception of cell₁ and cell₆₀. Cell₁ (LSB cell) has one input from cell₁ output (Q₁) and has the other input tied to LOGIC1, so that a “1” is always shifted into the 60-bit thermometer code when left shift is required. Similarly, SR₆₀ has one input from cell₅₉ (Q₅₉) output and the other input is tied to LOGIC0, for a “0”-shift when shifting right.

Figure 5-13 shows that the last 30 shift registers cells cell₃₁₋₆₀ have their preset nodes tied to LOGIC1 and reset nodes tied to *clrb*₃₁₋₆₀. The first 30 shift registers cells cell₁₋₃₀ on the other hand have their preset tied the global reset signal *Reset*, and reset tied to *clrb*₁₋₃₀— explained later in this section. Therefore with a one-time global reset, *D*_{in}[59:0] is preset with the value 60'h000_0000_2FFF_FFFF.

Right shift is performed when the shift flag *LR* is high and left shift when it is low. The shift flag is obtained from the output of the comparator.

Figure 5-13 Single cell structures for the first 30 cells in the left box and last 30 cells of the shift register in the right box

5.3.4.1 Overflow detection scheme

In the event that T_{IN} exceeds $T_{IN,max}$, *S16* flag is raised high by the TDC. This flag generates two low pulses *clrb*₁₋₃₀ and *clrb*₃₁₋₆₀. These two low pulses are used to reset all *D*_{in} bits to logic-0. Resetting all 60 bits to 0 will result in the lowest $T_{IN,gen}$ for any V_{IN} . Even if V_{IN} equals to 1.2 V, this will ensure that $(T_{IN,gen} - T_{offset}) < T_{IN,max}$. Note that $T_{IN,gen} - T_{offset} = T_{IN}$.

The circuit implementation of the overflow detection scheme is shown in figure 5-14. In a normal operation, *S16* is at a low state, and *clrb*₁₋₃₀ and *clrb*₃₁₋₆₀ are at logic-1. During a global reset that is enabled by a low *Reset*, *clrb*₁₋₃₀ remains

[illegible]

of the TDC such that it cannot be trimmed. The number of trim steps also determines many varactors are needed per delay cell.

The first step is to determine the $T_{IN,gen}$ over the entire Vdd range. Suppose there are 30 delay cells, with 2 varactors per delay cell. Therefore, 60 D_{in} bits are needed. In order to check the maximum $T_{IN,gen}$, the maximum analogue voltage must be applied to the delay cells, which is Vdd, and all 60 bits must have a logic “1”, loaded to the maximum. The input voltage to the delay cell is then swept from 0 V to Vdd, with a step of 1 mV.

Figure 5-15 below shows the output delay versus input voltage. Firstly, $T_{IN,gen}$ increases with V_{IN} , this proves that the delay cell structure enables a non-inverse V-T relationship. Next, non-linearity is observed, but is not unexpected. If we extrapolate the line from the upper half-Vdd range to the lower half-Vdd range, the point where the V-T transfer function changes is approximately around 330 mV. Therefore, one can imagine that any V_{IN} below this voltage requires quite a lot of delay adjustment. Using the V-T transfer function from the lower half-Vdd range would not make sense since the increment in $T_{IN,gen}$ is much faster in the upper half range, and even much more delay adjustment is required for V_{IN} above 330 mV.

Recall that a zero V_{IN} does not yield a zero $T_{IN,gen}$, and an offset is necessary. Suppose the TDC offset block is given a reference voltage of 0 V with fully unloaded varactors, the generated delay should be the finite delay that exists in all $T_{IN,gen}$ for all V_{IN} , also known earlier as T_{offset} . This value is approximately 1.0414 ns.

This T_{offset} is applied to the $T_{IN,gen}$ from the voltage sweep to give T_{IN} , and shown in figure 5-16 in blue. The requirement for the delay generator is to achieve $T_{IN,max}$. Therefore, suppose the T_{IN} for $V_{IN}=1.2V$ is set to $T_{IN,max}$ of 567.5 ps, and T_{IN} for $V_{IN}=0V$ is set to 0 ps, then it is possible to plot an ideal $T_{IN,ideal}$ curve with respect to V_{IN} . This is shown in orange in the figure for comparison with T_{IN} .

Figure 5-15 Output delay versus input voltage of the delay generator with fully loaded varactors

Figure 5-16 Real versus ideal T_{IN} over entire Vdd range

Furthermore, if each trim step is approximately 1.5 ps, one can calculate the number of steps required to fit the blue curve to the orange curve. Note that the T_{IN} blue curve is obtained under the condition that all varactors are fully loaded. By taking the difference between T_{IN} and $T_{IN,ideal}$ for each V_{IN} , and dividing each

difference with 1.5 ps, the number of trim steps is shown in grey in figure 5-17. Firstly, a negative number is good since it represents the number of varactors that need to be unloaded, and a positive number means extra varactors are required. The highest number of trim steps occurs at the range of 570 mV, where 70 extra varactors on top of the loaded 60 are required. This is primarily due to the fact that the $V_{IN}=0V$ is used as the minimum reference, and the huge offset at the 570 mV range requires extra varactors to increase its corresponding T_{IN} delay. The highest negative number is -50, which is within 60 trim steps allowed. One could simply increase the number of delay cells and the number of trim steps, but it does not solve the fundamental issue of the huge offset in the middle of the V_{IN} range that is caused by the non-linear V-T relationship.

Figure 5-17 Number of trim steps required to correct the offset between the real and ideal T_{IN} over entire Vdd range

Alternatively, one can increase the minimum V_{IN} such that the huge offset is removed. Note that the $T_{IN,gen}$ from figure 5-15 does not change, only T_{offset} has to be recalculated which is 1.1023 ns for $V_{IN} = 0.5$ V. The same number of trim steps can be recalculated for the new minimum reference, and the results are shown in figure 5-18.

Figure 5-18 Number of trim steps required to correct the offset between the real and ideal T_{IN} for a reduced input range

Clearly, the number of trim steps falls within ± 60 , and are all negative, which acceptable since no extra varactors are required on top of the 60. Also, more trimming effort is required for the lower V_{IN} values, but generally there already exists some good matching between T_{IN} and $T_{IN,ideal}$. Therefore, for the TDC offset block and DAC, the reference voltage is 0.5 V, the minimum V_{IN} value.

5.4.2 V-T relationship linearisation

In this section, the proof-of-concept of the linearization of the Voltage-Time relationship is discussed. From figure 5-18, the non-linear relationship between V_{IN} and T_{IN} is already described and shown with the voltage sweep. The proposed VTC aims to linearize the V-T relationship, i.e. adjusting T_{IN} to fit it to $T_{IN,ideal}$ by checking the T_{IN} and adjusting it via a feedback loop. The main idea is for every V_{IN} -generated T_{IN} , the offset between T_{IN} and $T_{IN,ideal}$ is removed bit by bit. This is made possible by quantising T_{IN} , converting the output digital bits to V_{DAC} and comparing it with V_{IN} as reference.

Figure 5-19 shows the original V_{IN} -generated T_{IN} (in blue) and the trimmed T_{IN} (in orange). As a reference, the ideal $T_{IN,ideal}$ is shown in grey for comparison. Firstly, the orange line is not exactly monotonic, small dips occur throughout the

ever-increasing V_{IN} . This arises from the ambiguity of the point in time where the output delay is measured. There is no flag to indicate that the generated T_{IN} is ready, and therefore the measurement of T_{IN} is based solely on the switching of the comparator output. In other words, since the T_{IN} is constantly generated and depending on how the comparator output switches based on the corresponding V_{DAC} with respect to V_{IN} , the trim code generated from the Up-down encoder keeps changing too. Also, the time taken for the latching of the D_{OUT} after the TDC and V_{DAC} conversion is longer than the comparator response time. No flag exists in this VTC to stop T_{IN} generation or to freeze the trim code. Therefore, the measurement instance of T_{IN} may not be correct, and sometimes this may happen after the correct trim code suddenly changes, which is the case for some of the T_{IN} values seen in the figure.

Nevertheless, it is evident here that the non-linear offset between the original T_{IN} and $T_{IN,ideal}$ is now more uniform, by comparing it to the offset between the adjusted T_{IN} and $T_{IN,ideal}$. There is also some extent of good matching between T_{IN} and $T_{IN,ideal}$, which proves that the delay adjustment works, and it is possible to linearize the V-T relationship with the proposed concept.

Figure 5-19 Adjusted T_{IN} in comparison to the original T_{IN} and ideal $T_{IN,ideal}$ versus input voltage

5.5 Conclusion

A new concept of voltage-to-time conversion with a TDC in a feedback loop has been proposed to linearise the voltage-to-delay relationship. The TDC and DAC enforce the linearity by trimming the output delay from the analogue-delay line, generated from V_{IN} . The trimming is performed via the varactors in the digital part of the delay line with control signals generated as a result of the comparison of V_{IN} and the feedback voltage, V_{DAC} obtained from the cascading of the TDC and DAC.

Due to the long latency of the VRTDC, an upgraded high speed, high resolution CFTDC was eventually chosen for the implementation of the TDC in the feedback loop for delay trimming. It has been shown that this concept can indeed resolve two issues of V-T conversion, one being the non-linearity relationship, and the other is the inverse transfer function. However, the input range is limited to 700 mV due to the huge offset between the generated and ideal output delay versus input voltage in the 570 mV range that requires a lot of trimming than the delays at the extreme ends of the input range.

Given a non-zero minimum input voltage, a non-zero delay output is expected but has to be removed, otherwise the maximum input voltage will yield an output delay larger than the input range of the TDC. A delay offset block is required that assumes a certain reference voltage and digital input setting. However, there is no possibility to calibrate the delay generator and the offset block because both use fixed delays by design. Furthermore, the output delay is generated actively and constantly and any slight variation in the trim code may shift the output delay from its correct value. This lies primarily also in the way the data is latched and converted to V_{DAC} . Therefore, the measurement of the delay output may occur at the wrong instance, thus giving an incorrect T_{IN} .

For this reason, no further development was made to the TDC-based VTC, and a new concept shall be introduced to generate delay or time. However, the concept of linearizing V-T relationship using a TDC has proven to be useful. In principle, this TDC-based VTC forms the foundation for the new voltage-to-time conversion concept in the next chapter.

6 A 9-bit digital-intensive twin-mode Data Converter based on delay mapping and correction using TDC

6.1 Introduction

Most, if not all of the architectures in the recent developments of Voltage-to-Time Converters and Time-mode Analogue-to-Digital Converters employ the discharging of a sampling capacitor for voltage-to-time conversion. The capacitor is discharged via a current source that is biased with the input voltage. The discharging voltage is sensed against a threshold voltage for time output generation. The sensing of the threshold crossing could be implemented by a regular voltage comparator or in some cases, a simple digital inverter with threshold voltage set at half-V_{dd} [83, 84] or a NOR gate [85]. In order to generate two time input signals for the TDC, a reference voltage is used; usually V_{dd} to generate the START signal and V_{IN} will result in the STOP signal upon crossing the threshold voltage. In some cases, the start of the capacitor discharge is used to generate a START signal, while V_{IN} crossing the threshold voltage event will generate a STOP signal. In some designs, a differential pair of input voltages (V_{IN+} , V_{IN-}) was available. Each input voltage discharges a sampling capacitor to generate a time differential pair of signals when both voltages cross a specified threshold voltage.

Linearization of the discharge V-T curve is achieved by calibrating the current source in accordance to the input voltages or by forcing/limiting the bias/source currents [86]. Santos used source degeneration resistors to increase the output resistance of the cross-coupled inverter cells such that the V-T relationship could be linearized [87]. Another form of source degeneration was implemented by cascoding two NMOS transistors operating in linear region to limit the discharge current of the sampling capacitor [85]. In another variant, an extra set of differential transistor pair in parallel to the output nodes with controlled bias voltages to force a constant current during capacitor discharge is used [83, 88].

In other presented designs, current-starving technique is used for time generation, whereby the V_{IN} is used as a gate bias of a sink NMOS or source PMOS to limit the bias current through an inverter with an input clock signal. Furthermore, a weak NMOS is added in parallel to the drain NMOS with a constant gate bias to improve the linearity at certain input voltage range by providing a secondary source current [65, 89]. The increased propagation delay as a result of the current starving defines the TDC input, T_{IN} .

A variant of the current starving is the use of differential input MOS transistors to create a pair of differential control voltages for a subsequent voltage-controlled delay block [90, 91]. T_{IN} is obtained as the relative difference of the two increased propagation delay, where the V-T relationship no longer depends on V_{IN} as a function of Vdd, which has an exponential behaviour. V_{IN+} and V_{IN-} are centred at the common-mode voltage to ensure similar voltage-time behaviour. Linearization in these cases is brought about by having a fixed bias voltage for the current bias NMOS transistor.

Y. Kim used the dual-mode delay line technique presented in the previous chapter for voltage and digital control of a single delay line. In this case, a bank of capacitors controlled by digital bits varies the strength of the positive feedback for the differential input voltage transistor pair to achieve the desired output delay via two modes.

Finally in rare cases, Voltage-Controlled Oscillators are still used as a VTC, using voltage-controlled differential delay cells in a ring structure [92], or simply static CMOS inverters with variable Vdd supply voltages for increased sensitivity and larger tuning range [93]. It is evident here that the sampling frequency is at best one-tenth of the previous two techniques.

In general, very high-speed (in Giga-hertz) sampling is achieved in most cases, with good linearity range of from half-Vdd to full-Vdd. It is also obvious where the trend of voltage-to-trend conversion technique lies. In the sampling capacitor method, heavy-weight analogue circuitry is employed with one or more capacitors. While it has been proven that through calibration means and certain techniques, high speed conversion can be obtained, it has not shown a way forward into more digital-intensive designs. But clearly the analogue designs are

unavoidable because in all of the examples given, the input voltage is used for quantisation. It is inevitable that analogue blocks must be used in the design of analogue-digital interfaces. But as long as the voltage domain data is processed, the percentage of analogue blocks in the design will be substantial. The previous chapter has also shown the need for some analogue blocks wherever the input voltage is used.

Table 6-1 below gives an overview of the input range versus supply voltage for the various VTC schemes in the literature. What appears to be a common attribute in the schemes is the domain in which the input voltage operates in – voltage. As long as V_{IN} is processed in the voltage domain, there is always a limitation on the operating range due to the intrinsic and inherent V-T relationship that cannot be avoided. As mentioned in the introduction, good linearity is achieved at the expense of input range. Such a compromise makes Voltage-to-Time-to-Digital conversion disadvantageous over the traditional Voltage-to-Digital conversion.

Table 6-1 An overview of the input ranges versus supply voltage for various VTC schemes

Reference	[65] ISCAS '06	[83] JSSC '19	[86] DCAS '09	[90] TCAS II '14	[92] ASSCC '16	[93] TCAS I '14
Scheme	current-starving	Samp Cap	Samp Cap	Diff. pair	VCO	VCO
Supply [V]	1.2	1	1.5	0.6	1.2	1.3
Input range [V]	0.2	0.88	1.2	0.6	0.7	0.6

A summary of the shortcomings in the previous design is as follows:

1. **Non-linear voltage-delay relationship** – Conversion from voltage to time is usually done via charging RC circuits. The increment in voltage usually results in a monotonic decrement in delay, an inverse relationship that has already been discussed. However, given the current equation $i_C = i_{max}e^{-t/RC}$, there is an exponential function between delay and current. A step increment in voltage is not linear to a step decrement in delay. Nevertheless, there exists some voltages where this relationship is linear, but it is limited to a very small range. Therefore, the V_{in} -range for conversion is usually very small in a time-domain voltage converter.

2. **Limited voltage range** – The other issue related to non-linearity is the amount of trimming necessary in the lower half-V_{dd} range if the entire V_{dd} range is intended to be converted, which has been shown in the results discussed in the previous chapter. This issue stems primarily from the existence of two different transfer functions, each dominating one half of the V_{dd} scale. As the two transfer functions are different in terms of magnitude, trying to equalise them comes at the expense of the upper region of the lower half V_{dd}-range, which has the biggest offset between the equalised and real transfer functions. Therefore, the number of trimming steps required explodes. Alternatively, the voltage range can be reduced to a range where the number of trimming steps is reduced to a sizeable amount, as is the case in the proposed voltage-mode VTC.
3. **Inverse voltage-delay relationship** – The innate relationship between voltage and delay is inverse-proportional. In digital circuits, a lower supply voltage increases the propagation delay of transistors, while a higher supply voltage enables the transistors to switch faster.

Since

$$\tau = RC \quad (6.1)$$

$$R = \frac{1}{k_n \left(\frac{W}{L}\right) (V_{gs} - V_{th})} \quad (6.2)$$

Therefore, delay with respect to voltage can be represented as:

$$\tau = \frac{C}{k_n \left(\frac{W}{L}\right) (V_{gs} - V_{th})} \quad (6.3)$$

In VTCs where input voltage is used to generate output delay, the same inversion is expected between input and output. One way of overcoming this inverse relationship is to invert the TDC output, but this creates some conflict with the initialised state of the TDC. Alternatively, the delay cell can be designed in a way that enforces a non-linear relationship as shown in the previous chapter. Nevertheless, this inverse relationship exists inherently and perhaps there is a methodology to entirely avoid the inverse outcome of V-T conversion without circuit manipulation.

4. **Non-zero delay output** – Time is real and is the one thing that keeps changing, i.e. does not stop. Therefore, unlike voltage or current, or digital bits, it is impossible to generate zero time. For zero input voltage, or minimum input voltage, it is possible to generate data output of 0, but not with output delay. But it is possible to achieve zero output delay using offsets, and this was done in the proposed VTC to implement a replica of the delay generator with a defined input voltage and digital trim code to create an offset delay. As long as voltage is used to generate delay directly, it is never possible to generate zero delay without an offset.
5. **Time quantisation can be slow** for converters with desired large dynamic ranges and high resolution, particularly determined by the latency of the used architecture. But high-resolution time quantisers are desired because the input range can be kept small for high number of bits. Compare for example an 8-bit TDC with a resolution of 20 ps and 2 ps, the input range of the former is up to 2.56 ns in comparison to just 256 ps. This means that the delay generator must generate up to 2.56 ns when needed. Note that every delay counts, and generating time inputs of 2.56 ns adds that much time into the quantisation time of a VTC that uses a TDC, for just one iteration.
6. **Time data cannot be stored** and later retrieved unlike voltage or digital data, i.e. data can only be used one time and has to be regenerated for repeated use. With the circuit implementation of the proposed VTC, there is a problem of the exact point of delay output measurement due to the absence of a flag that freezes the converter, which otherwise keeps updating itself in a feedback loop.

In this chapter, a new methodology is introduced to convert voltage to time delay. The main motivation is to ensure good voltage-time linearity over a huge input range, while keeping the core area as small as possible, reduce the use of calibration techniques, front-end or back-end, and also increase the digital intensity in voltage-to-time conversion architectures. Digital design can also leverage on the use of synthesis tools with standard library cells not only for easy realisation of Verilog hardware description that could have many hierarchical levels, for example building a state machine, but also with the

advantage of timing, power and area optimization. The former is especially important for delay-sensitive circuit designs such as TDCs. Such benefit is small when a large part of the design is analogue-based. Such concerns are also minimal when it comes to analogue design.

6.2 Concept

While the TDC-based Voltage-to-Time Converter seeks to linearise the voltage-time non-linearity through the use of TDCs in the feedback loop, it has the shortcomings of a lengthy time generation and an input voltage range limited by the TDC input range.

The proposed twin-mode data converter primarily aims to resolve these two issues, by using a new concept in data conversion. Rather than converting data from the voltage domain to time domain, the concept of mapping the full range of input voltage to a full range of delay is applied here.

Mapping data gives the following advantages:

1. Because the input voltage data is not used to generate delay, the relationship between voltage and delay is kept linear.
2. References in both domains are independent of each other, i.e. the references do not have to be fitted by calibration. When an RC circuit is allowed to charge to a certain voltage, the delay taken to do so depends on the size of the transistors. This means that depending on the time-input range of the time quantiser, the delay generator of voltage-time converter (or VTC) has to be sized such that the minimum input voltage results in a delay exactly equal to the maximum allowable time input. With PVT variations, this creates an uncertainty.
3. Since references of both domains are just matched together, one voltage LSB is therefore mapped to one delay LSB without a conversion factor that usually has to be calibrated.

The delay data is then quantised and compared with the input voltage while at the same time generating the quantized digital output.

The twin-mode Data Converter uses the concept of matching between two domains, voltage and delay, in their full-scales. The full scale of the voltage domain is defined by the DAC, which does not pose a limit on the input voltage scale. And the full scale domain of the delay or time domain is defined by the TDC, i.e. by how much delay the TDC can quantise.

In the previous VTC concept, the TDC full-scale is forced to match as wide an input voltage scale as possible by means of calibration and sizing of the delay line. Even so, the VTC input range was limited to minimum 0.5V, less than which, the dual-mode delay line will generate a delay output greater than the maximum input of the TDC. In this new concept, data from the two domains are simply matched to each other, by also utilizing a third domain – the digital domain. A full-scale delay input will result in maximum digital output, and this is therefore converted into maximum input voltage. This applies to zero delay input to minimum digital output and zero input voltage.

A comparator in the data converter determines the voltage LSB, and the TDC determines the time LSB. It is important to note that the former will be the bottleneck, because voltage cannot be scaled as well as delay.

The data converter has two outputs, time delay and binary bits, and the input is in voltage mode. The main idea is to generate a delay that represents the input voltage that can also be represented in digital bits, essentially a voltage-to-time converter and an analogue-to-digital converter in one device.

However, the input voltage is never processed, i.e. it is never converted but used only as a reference voltage. A delay is first generated and converted into a voltage that is compared against the reference (input voltage). The initial delay is generated based on half of the full-scale of the input voltage range upon reset. This concept requires a feedback loop, where the initial delay is adjusted and checked until the representing feedback voltage matches the input voltage. In this feedback loop, a delay generator, a TDC and a DAC monitors and trims the output delay, which is simultaneously obtained as a binary output.

This proposed twin-mode Data Converter is largely made up of digital blocks and allows quick modifications to increase/decrease desired bit count. Since

delay trimming is performed with neither varactors (very commonly used) nor capacitors, the area can be kept small.

The figure above shows the block diagram of the twin-mode Data Converter with the following building blocks:

- Digitally-controlled delay line
- Time-to-Digital Converter (TDC)
- Output Data Latch
- Digital-to-Analogue Converter (DAC)
- Comparator
- Voltage bias
- Coarse-fine switch
- Up-Down Encoder

Without knowing what the input voltage is, the most effective to start the trimming from the mid-level of the input range. Therefore at every reset, the Data Converter is designed to start quantisation from its half-input range value.

Figure 6-1 Simplified block diagram of the twin-mode Data Converter

Figure 6-2 Process flow of the quantisation concept of the proposed twin-mode Data Converter

6.2.1 Usage of building blocks

For the mapping of two domains to work, references are needed in each domain. Each reference marks the full range that can be quantised in each domain. By quantising the delay data to the reference delay, and quantising a voltage input to the reference voltage, the ratio of the data to the full range in each domain is essentially the same. And comparing the two data together while keeping the ratio, data in two domains are essentially mapped to each other.

The simplified block diagram of the twin-mode Data Converter and the concept is illustrated in figures 6-1 and 6-2 respectively. An initial delay is generated by the tuneable delay line, independent of the input voltage to be quantized. The delay is then quantized by the TDC which generates a digital output. This digital data is converted back into voltage by a DAC, V_{DAC} and compared with the input voltage V_{IN} . The result of the comparison ($V_{IN} > V_{DAC}$) determines how the delay line should be tuned. The resultant delay is converted back to digital bits via the

TDC and V_{DAC} via the DAC for further comparison with V_{IN} . This iteration goes on until V_{IN} and V_{DAC} are within $\pm 1\text{LSB}$ difference.

This loop thus allows the input data to be represented in two output forms, delay and digital, and corrected or trimmed in the time domain. The delay trimming is used to achieve the same T_{IN}/T_{REF} and V_{IN}/V_{REF} ratio. One voltage LSB is thus mapped to one delay LSB without a conversion factor that usually has to be calibrated. Therefore theoretically, any input within the full-Vdd range can be quantized, with ground and Vdd as the minimum and maximum V_{IN} respectively.

This section explains in detail on the concept and use of the individual blocks in the TDC-based ADC concept.

6.2.1.1 Coarse-fine switching block

The goal of the feedback loop is to trim V_{DAC} to within $\pm 1\text{LSB}$ of V_{IN} . Assuming each feedback loop quantisation step takes 12 ns, and if two consecutive V_{IN} samples are half input range apart, the quantisation time required is approximately 3.1 μs for 256 steps, potentially limiting the sampling frequency to kilo-hertz range.

In order to speed up the quantisation, the data converter has to work in two steps, i.e. coarse and fine modes. The coarse mode broadly maps the V_{DAC} to coarse levels of delay, and the fine mode trims this delay to an accuracy of one LSB. By trimming in two modes, only 468 ns for 8 coarse and 31 fine steps are required, potentially cutting the quantization time by approximately 85%.

To operate in two modes, a coarse-fine switch is used to identify when the switch between both modes should take place. In principle, the coarse mode is switched to the fine mode when V_{DAC} rises above V_{IN} , regardless if the latter was initially higher or lower than V_{DAC} . Figure 6-3 below illustrates how trimming is done. The crosshair and the dot represent V_{IN} and V_{DAC} respectively. The left scale represents the input full scale coarsely divided into 16 levels, and the right

scale represents the space between coarse levels 1c and 2c divided further into 31 fine levels.

Figure 6-3 Concept of coarse-fine trimming

When the coarse mode is in operation, the fine mode is disabled, and vice versa. Assuming V_{DAC} was trimmed in the coarse mode with an arbitrary fine level, the remaining fine levels might not suffice for trimming in the fine mode, and the coarse level can no longer be changed until the next V_{IN} is sampled. This will result in a DNL error for the sampled V_{IN} . Therefore, V_{DAC} should always maintain zero or full fine levels when compared with V_{IN} in the coarse mode. For the trimming concept in this design, the fine trimming shall be performed downwards, towards the next lower coarse level. Consequently, the fine levels are initialised to the maximum value, i.e. 31f.

In figure 6-3, it was assumed that V_{DAC} was initially higher than V_{IN} , and the latter is in between the first and second coarse levels, and approximately at the 2nd fine level. V_{DAC} is at coarse level 14c and fine level 31f. Since V_{DAC} (V_-) is greater than V_{IN} (V_+), the comparator output CMP_out (see figure 6-1) is set to logic zero, which means that V_{DAC} has to be reduced. From its initial coarse level 14c, it drops down to 13c. The comparator senses that V_{DAC} is still higher than V_{IN} , and CMP_out remains low. V_{DAC} is again reduced by one level to level 12c and so on until it reaches coarse level 0c. Upon reaching this level, V_{DAC} is sensed to be less than V_{IN} , and CMP_out is switched to logic one. At this instance, the coarse quantisation has gone one step too far and must be returned one step, otherwise the fine trimming will not bring V_{DAC} any closer to V_{IN} , keeping in mind that fine trimming is performed downwards. Since CMP_out is high, V_{DAC} is raised to coarse level 1c. V_{DAC} is compared again with V_{IN} , and since V_{DAC} is

now greater than V_{IN} , CMP_out switches back to low. This 0-1-0 switch in CMP_out raises the coarse-fine switching flag, ENf to logic 1, and the coarse mode is disabled.

In the fine mode, the coarse level 1c is captured and cannot be changed. V_{DAC} starts from fine level 31f and is trimmed downwards towards level 0f. As V_{DAC} approaches within $\pm 1\text{LSB}$ of V_{IN} , the flag RDY is raised high.

Until the next V_{IN} is sampled, the coarse-fine switch and the entire converter remains in fine mode. Once a new V_{IN} sample is taken, the ENf flag is reset, coarse mode is reactivated, fine mode is disabled and fine level is initialised back to 31f.

If instead V_{IN} was initially higher than V_{DAC} , CMP_out would have initially been logic one. V_{DAC} moves up the coarse levels until it becomes greater than V_{IN} . CMP_out switches to low because V_{DAC} was trimmed too high. This 1-0 switch will then activate the coarse-fine switching, i.e. ENf is raised high.

In the event of an accidental high-low switch in CMP_out due to unforeseen circumstances, the fine mode can be falsely enabled. As an additional safety feature, the coarse-fine switch checks for a repeated 1-0 switch in CMP_out twice, i.e. to confirm that V_{IN} has indeed become greater than V_{IN} through coarse trimming. In other words, V_{DAC} is forced to first return to a coarse level higher than that of V_{IN} , then lower, then higher once more, before coarse-fine switch occurs.

It follows that there are three situations that determine when the coarse-fine switching should occur:

1. CMP_out switches from high to low
2. CMP_out stuck-at-zero (see figure 6-4)
3. CMP_out stuck-at-one (see figure 6-4)

Figure 6-4 Three cases that determine the criteria for coarse-fine switching

Imagine V_{IN} being at the lowest coarse 0c and some arbitrary fine level. In this situation, CMP_out is assumed to be low and V_{DAC} is reduced until coarse level 0c and fine level 31f (the default fine level in coarse mode). Despite reaching the lowest coarse level, CMP_out remains low. Under the condition that CMP_out switches 1-0, a coarse-fine switch will never take place, and V_{DAC} will be stuck at 0c+31f level and until the next V_{IN} sample lies between coarse levels 0c and 1c. Therefore, the coarse-fine switching block has to recognise the condition that CMP_out can be stuck at zero and still allow fine mode to be enabled, by simply detecting that the lowest coarse level is reached. In other words, a flag, *end_down* is required to be raised high when coarse level 0c is reached. Upon a raised *end_down*, the switch checks if CMP_out is held low for the next few clock periods. If so, a coarse-fine switch takes place, i.e. *ENf* is raised high. In case of a toggling in CMP_out during the few clock periods, the 1-0 condition for a switch resumes precedence.

For the exact opposite situation that CMP_out is stuck high, a flag *end_up* is raised high when the highest coarse level is reached, and CMP_out is checked if it remains high for a few clock periods. If so, coarse-fine switch takes places, i.e. *ENf* is raised high, and fine mode is enabled. As long as CMP_out toggles to low during these clock periods, the 1-0 condition for coarse-fine switch kicks in immediately.

The implementation of these requirements in circuit is explained later in the section of Circuit Implementation.

6.2.1.2 Digitally-tuneable Delay Line

In voltage-mode delay generation designs that utilise V_{IN} for voltage biasing, the output delay of a delay line is dependent on the size of the transistors in the delay cells that make up the delay line. Depending on the maximum allowable time input range of the TDC, $T_{IN,max}$, the delay cells have to be sized precisely such that the maximum generated output delay fits to $T_{IN,max}$. PVT variations will result in uncertainty which thus requires either front-end or back-end calibration. Such voltage-mode methods also introduce the non-linear V-T relationship into the transfer function.

In this design, T_{IN} is intended to be a linear representation of V_{IN} , and will not be used to generate T_{IN} . And since the digitally-tuneable delay line is intended to be trimmable down to one LSB step size, a total of 512 trimming steps can be time-costly. Therefore the delay line is broken down into two stages in order to speed up the entire process. The delay generator shall consist of two parts, coarse delay and fine delay sub-blocks, corresponding to the coarse and fine modes of the coarse-fine switch. In each sub-block, the output delay is changed by amounts that are determined by the unit delay cells used, which are also controllable by the trimming code.

The input to the delay line (st in figure 6-1) is a single rising edge signal generated externally in the Up-down encoder. From this rising edge signal, two rising edge signals are obtained at the end of the delay line. They are *START* and *STOP*, which serve as inputs to the TDC. The *START* signal is a buffered rising edge signal generated from the trigger pulse with an arbitrary propagation delay. The *STOP* signal is a delayed rising edge signal generated from the trigger pulse plus the arbitrary propagation delay plus the delay controlled digitally via the digital inputs. The propagation delay between these two signals determines the output delay of the delay line and the input delay of the TDC, T_{IN} . The arbitrary propagation delay in both signals is cancelled by each other when the delay difference between *START* and *STOP* signals is taken. T_{IN} is intended to be a linear representation of the input voltage of the ADC, which circumvents the conventional non-linear relationship between voltage and time delay.

The other inputs to the delay generator are 46 binary bits that are sub-divided into two groups. These two sets of digital bits are used to trim the coarse and fine sub-block, independent of each other, which are obtained from the Up-down

Encoder. A 15-bit thermometer-code input sequence controls the output delay of the coarse delay block, T_{IN_C} while a 31-bit thermometer-code input sequence controls the fine delay block output, T_{IN_F} . The summation of both sub-delays give the final output delay T_{IN} . The single rising edge input signal passes through the fine delay sub-block that to produce two intermediate rising edge signals (called *out_start* and *out_stop* in figure 6-1), whose delay difference defines T_{IN_F} . These two intermediate signals that pass through the coarse delay sub-block to have their delay difference extended further to give the final T_{IN} . At the output of the coarse sub-block are the two signals, *START* and *STOP*. Figure 6-5 below illustrates this concept.

In the initial state, the 15 coarse bits are all at logic-zero, and the 31 coarse bits are all at logic-one. This is seen as $qc = 0$ and $qf = 31$ in figure 6-5. Therefore, T_{IN_F} is at its maximum, defined by the delay between the rising edges of *out_start* and *out_stop* (in blue). Since $qc = 0$, there is no T_{IN_C} , and the total T_{IN} is effectively just T_{IN_F} . As qc changes with coarse trimming, T_{IN_C} changes accordingly. In this mode, flag *ENf* remains at logic-zero (active-high flag), and the converter is in the coarse mode. The resultant T_{IN} is a summation of an ever-changing T_{IN_C} and a maximum T_{IN_F} , whose value is effectively between the rising edges of *TDC_start* and *TDC_stop* (in red). Every coarse trimming step effectively changes T_{IN} in large amounts.

At the end of the coarse mode, *ENf* is raised high, the qc value is frozen (shown as 11₁₀ in the figure), and qf starts to change with fine trimming. Consequently, T_{IN_F} changes and T_{IN} is again a summation of a fixed T_{IN_C} and an ever-changing T_{IN_F} . Every fine trimming step changes T_{IN} in small amounts. Figure 6-5 illustrates how T_{IN} changes according to T_{IN_F} and T_{IN_C} in each mode and how the latter two parameters react to qf and qc .

Figure 6-5 Concept of time delay generation by the two delay sub-blocks in the digitally controlled delay line

Since the $T_{IN,max}$ is determined by the TDC characteristics and the D_{max} is defined in the overall Data Converter specification, the transfer function, T_{DL} of the tuneable delay line can be written as follows:

$$t_{res} = T_{IN,max}/(2^N - 1), \quad (6.4)$$

$$D_{res} = D_{max}/(2^N - 1), \quad (6.5)$$

$$T_{DL} = t_{res}/D_{res} \quad (6.6)$$

Clearly, there is no voltage-dependency on the T_{IN} , which ensures that no non-linear behaviour exists in the transfer function.

6.2.1.3 Up-down Encoder and TDC trigger

The Up-down Encoder sets the digital trim sequence to the delay line for T_{IN} generation. It requires two input signals, the comparator output, CMP_out and the coarse-fine switching flag, ENf . The output of the encoder is the array of coarse and fine bits that are used to digitally tune the delay line. The coarse fine bits are grouped in the box with a dashed line, and the fine bits are grouped in the box with a dotted line as shown in figure 6-1.

Both the trim sequences, i.e. 15-bit coarse trim and 31-bit fine trim sequences are outputs of the up-down encoder, and are used for T_{IN} generation. Both the trim sequences are in thermometer code form. The Up-Down Encoder shifts the

“1”s in the digital trim sequences up and down when CMP_out is logic-one and -zero respectively. An additional logic-high bit in the thermometer sequence extends the delay per cell, while an additional logic-low bit shortens the delay. Therefore, the output delay is increased with increasing number of 1s, and decreased with decreasing number of 1s or increasing number of 0s. Upon an initial reset, the coarse thermometer code is set to a default value of “0”, and the fine code to all “1”s. By encoding in the upward direction, a “1” is introduced into the thermometer codes at the LSB and all bits are shifted to the left towards the MSB. In the downward direction, a “0” is introduced into the thermometer codes at the MSB and all bits are shifted to the right towards the LSB. In other words, every left shift introduces a “1” into the sequence, while every right shift introduces a “0” into the sequence. Increasing the number of “1”s in the thermometer sequences increases the number of delay cells with extended delay and hence total delay per delay sub-block.

The other input of the encoder, ENf , determines if the fine mode should be enabled, and consequently disabling the coarse mode; both modes are complementary and do not operate simultaneously. A raised-high ENf flag freezes the coarse trim sequence and sets the fine trim sequence according to the input CMP_out . A logic-low ENf does the exact opposite.

As explained before, the fine bits of the delay generator are always initialised to logic one. This sets a maximum fine T_{IN_F} for any coarse T_{IN_C} in the coarse mode. When the criteria for switching between the coarse and fine modes is achieved, the setting for the 15 coarse bits is captured, i.e. no further changes are allowed, and T_{IN_C} is fixed. The fine mode is then set into operation and T_{IN} is further adjusted according to T_{IN_F} . At the end of each sampled- V_{IN} quantization, the coarse delay sub-block is once again enabled, and the fine delay sub-block is disabled with all 31 fine bits reset to logic-one.

A reference clock is used by the up-down encoder to shift the thermometer bits, coarse-fine switch for checking the stuck-at conditions and for the TDC triggering. From the reference clock edge, a pulse with very narrow pulse-width is generated, which is needed for the generation of the two TDC input signals via the digitally-tuneable delay line. Since the rising edge of the trigger pulse is utilised, the pulse width only has to be long enough such that the rising edge is

guaranteed between V_{dd} and ground even under the loading influence of the connected digital circuitry.

6.2.1.4 Self-reset comparator

The input voltages of the comparator are the input voltage of the ADC, V_{IN} and the feedback voltage from the DAC, V_{DAC} . The output of the comparator is a one-bit digital signal, CMP_out . The logical expression for the output signal is as follows: $CMP_out == 1$ IF ($V_{IN} > V_{DAC}$). This output signal is used as an input parameter by the up-down encoder to determine the direction of change of the thermometer code sequences, and by the coarse-fine switch.

As the resultant T_{IN} changes in coarse steps, the TDC and DAC convert it into V_{DAC} that is constantly compared with V_{IN} . In other words, V_{DAC} is regulated against V_{IN} . The output of this comparison is the input to the Up-down Encoder, CMP_out , which determines the direction of the delay change. A logic one means that V_{IN} is greater than V_{DAC} and the latter should be raised by increasing T_{IN} . On the other hand, a logic zero occurs when V_{IN} is less than V_{DAC} , which needs to be decreased by reducing T_{IN} .

In order to compare V_{IN} and V_{DAC} for the entire V_{dd} range, the comparator must have a rail-to-rail input voltage range capability. Doing this in the analogue way increases the area and effort. Moreover, different output response time is expected in certain mid-ranges where the n-input and p-input pairs are at their weakest. Alternatively, using digital comparators require an input clock signal. The complementary and true phases of the clock signals are used to pre-set nodes, and compare and output data respectively. However, glitches are generated at the rising and falling edges of the clock signals, which are capacitively-coupled onto the DAC as noise. This will result in an undesired offset in the DAC output voltage. Furthermore, suppose the duty cycle of the clock signal is 50%, thus CMP_out switches between its preset state and true output state every half period. Therefore, the other blocks in the data converter will require a clock signal that is synchronised with the comparator clock to read the CMP_out logic value anytime during the second half comparator clock period. The response time of the comparator must then be taken into account to allow CMP_out to settle before reading its logic value. However since the

delta- V_{IN} of the comparator, i.e. $V_{IN} - V_{DAC}$ plays a significant role in the output response time, the extreme fast and slow response times of the comparator must be taken into consideration. For this reason, a clock shall not be used with this comparator.

To avoid the mentioned issues, the mixed-signal comparator is made up of two individual analogue comparators, each to take care of one of the two half-ranges of the input voltage, i.e. lower and upper half- V_{dd} . This enables the comparator to achieve full-scale input voltage comparison.

Under different input voltage conditions, the two comparator outputs inevitably response differently. Therefore, extra digital logic is necessary to be built into the comparator to analyse the two outputs and generate the final one-bit data, *CMP_out*. Without an input clock, the digital logic has to be pre-set or reset by an external reset signal, which has to be periodic, i.e. at the onset of every V_{IN} sample. This external signal still has to be synchronised with other edge signals in the other building blocks of the circuit. For the simplicity of things and self-containment of the control signals within the comparator, the reset signal is generated internally based on the rising and falling edges of the two comparator outputs. This removes the need for synchronisation. The implementation of the self-reset comparator will be explained in the next section.

6.2.1.5 Time-to-Digital Converter

Multiple iterations are necessary since one iteration per V_{IN} sample is insufficient for the proposed concept. N number of iterations reduces the data converter's sampling speed by N , which is time-costly. As explained earlier, time quantization can be slow for high-resolution TDCs like the Vernier-based TDCs can have high latencies. For example, the VRTDC in Chapter 3 has a sampling period of 35 ns. Therefore, the CFTDC presented in Chapter 4 which quantises T_{IN} in two-stages to shorten the entire quantization cycle to just 3.6 ns, is preferred.

The TDC input T_{IN} is obtained from the delay line, and the digital output is sent to the DAC for V_{DAC} conversion. The TDC works in two modes, coarse and fine modes, which are not the same coarse and fine modes as the other building blocks, i.e. it is intended for the TDC to work independently of other blocks.

Coarse mode is started when *START* arrives. The *START* signal is then delayed multiple times by coarse delay cells, shown here as the propagation delay t_{coarse} between *delayed-START₁₅* and *delayed-START₁₆*. The resolution of the coarse TDC is t_{coarse} . In principle, the TDC chops up T_{IN} into 16 coarse delays. The edges of *STOP* and *delayed-START₁₋₁₆* are compared by arbiters to see which arrives first. As long as *STOP* arrives later, the F_{1-16} flag stays at logic zero. In the example given in figure 6-6, *STOP* arrives before *delayed-START₁₆*. Therefore, F_{16} rises to logic one. The delay difference between *STOP* and *delayed-START₁₅* is known as $T_{residue}$. However, since *delayed-START₁₆* is captured instead, $T_{residue}'$ is taken for the fine quantisation instead.

Figure 6-6 Timing diagram of the TDC

Fine mode quantises the $T_{residue}'$, defined between the input signals of the fine TDC, *START_v* and *STOP_v*. *STOP* signal, input to the coarse TDC is used as *START_v* of the fine TDC, while *delayed-START₁₆* from the coarse TDC is used as *STOP_v*. Sub-gate delay t_{res} is obtained in the fine TDC via the Vernier principle. Note that $T_{residue}'$ is effectively the difference of t_{coarse} and the actual residual time $T_{residue}$. By quantising $T_{residue}'$ and inverting the data, the digital output equivalent of $T_{residue}$ can be obtained.

The four bits of the coarse TDC output contribute to the upper four bits of D_{OUT} , while the five bits from the fine TDC contribute to the lower five. Each t_{coarse} corresponds to thirty-one multiples of t_{res} , which is the resolution of the CFTDC. t_{res} is therefore mapped to 1 LSB of the data converter.

The TDC has a self-reset structure that is dependent on the two input signals. On the rising edges of the *START* and *STOP* signals, a short low-active pulse is generated to reset the digital circuits related to the coarse and fine TDC respectively, especially the arbiters. For this reason, D_{OUT} is always reset to 9'b000011111 or 31_{10} , its default value just before the next quantization starts. Using equations (6.5) and (6.6), and since

$$V_{res} = V_{max}/(2^N - 1) = V_{dd}/(2^N - 1), \quad (6.7)$$

Any input voltage, V_{IN} can thus be described mathematically as follows:

$$V_{IN} = n * V_{res} = (n * V_{dd} * T_{max}) / (D_{max} * t_{res}) \quad (6.8)$$

6.3 Circuit Implementation

This section explains the circuit implementation of the key blocks in this data converter concept and how the individual concepts that have been elaborated in the earlier section are fulfilled.

6.3.1 Coarse-fine switch

The coarse-fine switch consists of 4 sets of logic (see figure 6-7), to check for 0-1-0 switch, stuck-at-zero, stuck-at-one and *RDY* flag generation. The output of the first 3 sets give the final *ENf* flag.

1. “0-1-0” switch: *CMP_out* is used as a clock signal to a set of four cascaded flip-flops. The true *CMP_out* clocks the first and third flip-flops while the complementary *CMP_out* clocks the even numbered flip-flops. A LOGIC1 (L1) is connected to the D input of the first flip-flop. When *CMP_out* rises and falls in sequential order, the L1 value is shifted from the first to the last flip-flop. The toggling of *CMP_out* does not have to be one comparator quantisation period apart. It is only important that the 0-1-0 transaction occurs for coarse-fine switch to take place. The outputs of the third and fourth flip-flops will go high at the 0-1 and 1-0 transition of *CMP_out* respectively.

2. stuck-at-zero: Unlike the previous set of flip-flops, this set requires extra logic gates in between stages to check for stagnant *CMP_out* value. *End_down*

is a flag from the up-down encoder that is raised high when the encoder counts to the lowest coarse bit. The flip-flops are in synchronous mode. Should *CMP_out* remain low for three clock periods, *ENf_00* is switched to high through the carried raised *end_down* flag and L1 as D input. Otherwise, the clock input of the last flip-flop is switched to zero and *ENf_00* will not be switched high. In this case, the logic for 0-1-0 switch which is running in parallel will change *ENf_01* and *ENf_10* values, i.e. takes precedence.

3. stuck-at-one: Similar to stuck-at-zero, the *end_up* flag is raised high when the coarse bit is counted to the maximum, and *CMP_out* must stay high. The *end_up*=1 value will be carried to the last flip flop to act as a clocking signal to raise *ENf_11* high. The final *ENf* flag is an OR-combination of all three *ENf_10*, *ENf_00* and *ENf_11* flags. If any of the above-mentioned three situations occur, the coarse-fine switch will take place.

4. RDY flag: The RDY flag is generated by the fourth set of logic in the coarse-fine switch. It first requires the *ENf* flag to be generated, because the logic can only be activated in the fine mode. The structure is similar to the 0-1-0 switch logic, for the search of 0-1 and 1-0 transitions. The comparator output *CMP_out* is also used as a clock signal. The exception is the addition of an AND gate between cascade stages. The AND gate ensures that only an activated *ENf* flag will set off the 0-1-0 transaction detection in the logic.

Figure 6-7 Schematic of the coarse-fine switch

6.3.2 Tuneable Delay Line

The two delay line segments are made of up of a similar structure. The coarse segment has 15 delay stages while the fine segment has 31 delay stages. Both work on the principle of bypassing cells when a logic zero is set through D_i to the corresponding delay stage. Each stage is made of two delay cells and two multiplexers as shown in figure 6-8. The delay cells used in the tunable delay line are the same as those used in the TDC. The vernier principle is used to achieve sub-gate propagation delay per stage in both the TDC and the delay line, and a very fine delay tuning can be achieved. The total delay in the fine segment should correspond to one coarse delay stage delay. Therefore, by using external voltage biasing as in the TDC, the desired delays can be achieved. The figure below shows a simplified diagram of the delay cell group.

Figure 6-8 Simplified diagram of the delay cell group used in the delay line

There are two inputs, $in1$ and $in2$, two outputs $out1$ and $out2$ and one digital input D per delay stage. When a logic zero is applied to the delay stage via D -input, $in1$ is connected to $out1$ and $in2$ to $out2$ respectively, bypassing both delay cells. When a logic one is applied to D , $out1$ is connected to the output of the delay cell and is equal to $in1 + delay1$. The same is for $out2$. Selecting “1” or “0” thus decides if the delay cell in each group is bypassed. Since the Vernier structure is used in all the delay stages in the coarse and fine segments, the delay difference between the two delay cells $delay1$ and $delay2$ in each stage corresponds to the respective resolution of the coarse and fine TDCs. The coarse and fine segments will each have its own set of $delay1$ and $delay2$ to obtain the desired delay per stage via voltage biasing. This tuning is similar to that in the TDC to obtain t_{coarse} and t_{res} , the desired coarse and fine TDC resolution respectively.

When the delay groups are cascaded, and setting all 46 D -inputs to “0” means that all the delay cells are bypassed, i.e. inx_i are connected to $outx_i$ and ideally there will not be a delay difference the input and output of the delay line which is defined as

$$t_{DL,OUT} = STOP - START = T_{TDC,IN} \quad (6.9)$$

Setting all inputs to “1” results in a maximum contribution from the delay cells to the propagation delay line to obtain the maximum delay $T_{IN,max}$. If $T_{IN,max}$ is not the same as the maximum output delay of the delay line, there will be an upper range that cannot be quantised by the TDC. This is also why the voltage biasing is necessary

6.3.3 Up-down Encoder

The Up-down Encoder is made up of a sequential up-down counter and two binary-to-thermometer decoders. A simplified diagram of the circuit is shown in figure 6-9 below.

The first up-down counter is for the generation of the coarse bits for the delay line. The direction of count is determined by the logic value of *CMP_out*. A logic zero sets the counter in count-down mode and vice versa. By default, the entire quantiser is in the coarse mode, i.e. *ENf* flag = logic zero. Therefore the coarse counter is enabled. The reference clock is used for the counters. The fine counter is disabled in the coarse mode, and the output *B_F[4:0]* is preset to 5'b11111, with emphasis to the trimming concept presented earlier.

Figure 6-9 Simplified diagram of the Up-down Encoder

The binary output *B_C[3:0]* of the counter is simultaneously decoded into a 15-bit thermometer code *qc[15:1]* for the digital delay line. When the coarse count *B_C[3:0]* reaches 4'b0000 or 4'b1111, the counter generates two flags *end_down* and *end_up* respectively. These flags are used in the coarse-fine switch to indicate the end of coarse count.

Upon the activation of the fine mode, i.e. *ENf* flag set to logic high, the coarse counter is disabled and the fine counter is enabled. The active-low preset of the fine counter is disabled and the fine counter first counts down and subsequently counting in a direction dependent on the logical value of *CMP_out*. The binary output *B_F[4:0]* is simultaneously decoded into the 31-bit thermometer code *qf[31:1]*. Together, the two thermometer code determine which delay cells in the digital delay line are turned on or bypassed.

The TDC trigger pulse generator is made up of delay cells and logic gates to generate a short pulse on the rising edge of the reference clock. The duration of the pulse is characterised based on the loading the trigger pulse and is achieved by cascading some delay cells. Such a structure is also implemented in the arbiters.

6.3.4 Self-reset comparator

The comparator in this design, as shown in figure 6-10, is made up of a P-input pair comparator (see figure 6-11) and N-input pair comparator. The basic structure of the comparator is the same – a simple two-stage comparator. The target for each of the comparator is to achieve a 2 mV resolution with output response time in the range of below 10 ns. Since the comparator outputs are further processed digitally, the gain of the comparator is not the biggest concern. The bias voltages are provided from a separate voltage bias block.

Figure 6-10 Schematic diagram of the comparator

Figure 6-11 Simplified diagram of the P-input pair comparator

Since the two comparators have a specified input voltage range, and are targeted to work optimally in either of the half-Vdd range, the response time of

the comparator working in the other non-optimal half-Vdd range is much longer than that in the optimal half-Vdd range.

In other words, the P comparator can resolve $V_{IN} > V_{DAC}$ much faster if at least one of both voltages are in the lower half-Vdd range, as compared to if both voltages are in the upper half-Vdd range where the N comparator works more optimally. Therefore, given any V_{IN} and V_{DAC} voltages, it can be expected that $outP$ and $outN$ will be resolved at different times, i.e. one after the other. The comparators have a limit of 12ns to resolve $V_{IN} > V_{DAC}$. This limit is set by the clock period of the up-down encoder. If $outP$ or $outN$ is not resolved within 12 ns, it is assumed that the logical value has not changed from the previous comparator quantisation. Note that the change in logical value is recognised as a rising or falling edge of both signals.

The digital logic that processes the $outP$ and $outN$ data needs to detect rising and falling edges to check for the transition between the two logical values. The use of flip-flops as edge detectors require a clock signal which is not available to the comparator. On the other hand, arbiters are used in the TDCs described in the earlier chapters to detect which of the two input edges arrives first. These arbiters do not require an input clock signal, which can be a good alternative.

Two arbiters are thus required, one to detect rising and falling edges. Each arbiter has two inputs, $outP$ and $outN$, and each arbiter has two active-high outputs to indicate if $outP$ or $outN$ has risen (fallen) first. Arbiter A checks if the falling edge of $outP$ or $outN$ arrives first. If so, the corresponding output P_down or N_down will switch to high. Similarly, arbiter B checks for the rising edge switch either P_up or N_up to high.

In the operation of the ADC, the digital logic of the comparator has to consider the four possible cases that could possibly happen:

1. Both $outP$ and $outN$ toggle to the same logic level one after another
2. Either $outP$ or $outN$ toggles, while the other has no change from the previous state
3. Both $outP$ and $outN$ stay at 0 or 1

The timing diagram in figure 6-12 illustrates how the digital logic is supposed to process $outP$ and $outN$ to give the correct CMP_out based on the four cases

mentioned earlier. In the first two periods, *outP* and *outN* switch to the same logic level one after the other, thus *CMP_out* takes the value of *outP/outN* at the first. The deciding edge is marked in red in every period. To simplify the explanation, the term “period” is used loosely to refer to the 12ns between the two vertical dotted lines. In reality, there is no period per se, and the comparator digital logic works on edge-triggered events.

In the third to sixth periods, only one of the two outputs switches while the other keeps the logic value from the previous quantisation. Therefore, *CMP_out* takes the new data at every period at the rising or falling edge. For the third and fourth cases, the digital logic recognises that neither *outP* nor *outN* has had a change in logic value, and thus holds the value from the previous period.

Arbiters are used for edge arrival detection in the digital logic. Unlike a flip-flop where a rising or falling clock edge “propagates” the input data to the output, arbiter outputs do not change on clock edges. Once either of the arbiter outputs is switched, it stays high regardless the sequence of arrival of the inputs in the subsequent periods. The blue dotted line shows an example of what *CMP_out* will look like without resetting the arbiters after every edge detection.

Figure 6-12 Timing diagram of the self-reset comparator

Therefore, a periodic reset signal is necessary to reset all the outputs before each comparator quantisation period. However, the use of a periodic reset signal on an asynchronous digital logic circuit risks resetting the intermediate signals before they are captured by the subsequent logic, thus losing data. To

circumvent this problem, a novel edge-induced reset is introduced into the comparator. The reset signal generator is shown in figure 6-13 with the rising and falling edge detectors marked out in dotted lines.

The edge-induced reset signal generator consists of a rising and falling edge detector. *outP* and *outN* are fed through a NOR and AND gate for an exclusive-NOR and OR function on their positive pulses, named as *x1* and *x2* respectively. As a result, these two signals toggle alternately at every edge of *outP* and *outN*, regardless rising or falling, as observed in figure 6-14.

Figure 6-13 A novel edge-induced reset signal generator

A time period of 12 ns given to the comparator for every input voltage sample to make a decision. With the help of delay cells, 4 pulsed signals are generated with the *x1* and *x2* signals and their inverted signals. These four pulses are products of the two edge detectors in the reset generator. *P_rise* and *N_rise* pulses occur on the rising edges of *outP* and *outN* respectively, and *P_fall* and *N_fall* on the falling edges. Each active-high pulse is long enough to reset the arbiters in the comparator via pull-down to ground. In the absence of an external active-low reset signal, the two reset signals *R_u* and *R_d* are given by the logical expressions $OR(P_rise, N_rise)$ and $OR(P_fall, N_fall)$ respectively. The timing diagram in figure 6-14 shows the reset generation with the *outP* and *outN* from the previous example.

Figure 6-14 Timing diagram of the reset signal generator

As a result of the edge-induced reset signals, the arbiter outputs *P_up(down)* and *N_up(down)* switch and keep the logic value for a short pulse starting from the rising/falling edge of *outP* and *outN* before they are reset, shown in the figure below. The short pulse width corresponds to the short delay before the reset pulses are generated.

Finally, the 2-input NOR gates logically combine the four arbiter output signals together for the NAND SR latch in the last stage, to generate the *CMP_out* response for rail-to-rail output swing. With the combination of the NOR gates and the latch, *CMP_out* switches high only on *P_up* OR *N_up* and low only on *P-down* OR *N_down*. In the event that both *outP* and *outN* remain low or high from the previous state, no reset pulse is generated and the latch holds *CMP_out* at its previous state. However, extra pull-up and pull-down gates are added in the event both *outP* and *outN* are stuck-at-one and –zero respectively. Two signals *PD* and *PU* act as the 3rd input to the SR latch NAND gates. Should *outP* and/or *outN* stagnate, an active-low *PD* and *PU* will pull *CMP_out* down and up respectively. Otherwise, they act as inverting signals for the other two inputs of the NAND gates.

In light of all the possible *outP* and *outN* behaviour, the digital logic in the comparator must be able to process the two data regardless of the situation the comparator is in. Unfortunately, this requires a reasonable amount of digital

circuitry, in which the arbiters take up as a single cell the largest share of the digital area.

The layout of the comparator is shown in figure 6-15 with the building blocks marked out. It measures approximately $(20.95 \times 23.245) \mu\text{m}^2$. The two blocks outlined in red are the analogue comparators, with the P comparator in black and N comparator in green. They take up approximately 60% of the entire area. Of the remaining 40% area taken up by the digital circuitry, the two largest single building blocks are the arbiters marked in yellow.

In conclusion, through the use of the edge-induced reset generator, the comparator can be self-reset based on trigger events. The comparator uses both analogue and digital circuitry to achieve rail-to-rail performance with reasonable minimum input difference and output response time. Moreover, external clock is redundant for the digital stages of the comparator, avoiding the unnecessary noise and periodical power spikes during clock switching.

Figure 6-15 Layout of the self-reset comparator

6.3.5 Latch array and DAC

Assuming D_{OUT} takes the value of 105_{10} after the first quantisation, and 106_{10} , 107_{10} and 108_{10} after the subsequent quantisation. However, due to the reset in the TDC prior to every quantisation, D_{OUT} switches to 31_{10} . The DAC converts D_{OUT} to V_{DAC} . With the periodic switching to 31_{10} , V_{DAC} will not sequentially increase from 246.1 mV to 253.1 mV, but instead has a dip to 72.7 mV between every step increase. The dips are shown in figure 6-16 as the black solid line. On the other hand, the red dotted line shows the goal of the latch array.

To remove the dips, a latch is added between the TDC and the DAC. All 9 bits of D_{OUT} are latched after every quantisation before they are converted to V_{DAC} . The latch array is made up of 9 flip-flops to latch each bit of D_{OUT} . The latches use a clock signal that is synchronised with the clock signal used in the up-down encoder.

Figure 6-16 V_{DAC} resets to 73mV after every quantisation without a latch (black solid line) – diagram is not drawn to scale

The R2R architecture is used for the DAC. A fragment of the schematic implementation is shown in figure 6-16(a). The unit R is chosen to be $10\text{k}\Omega$, implemented with p-poly resistors. Common centroid structures are used in the layout (see figure 6-16(b)) to ensure the uniformity of the poly stripes to reduce the gradient error and dummy resistors are added to the sides to avoid the over etching the two sides of the poly stripe array. The switches are made as big as possible to reduce the ON-resistance and thus the voltage drop across the switch when enabled. The transistors also use a common centroid structure in the layout.

Figure 6-17 (a) a section of the R-2R network with the switch and connected voltage nodes and (b) the layout implementation of the R2R DAC

6.3.6 Voltage bias

As mentioned earlier, the pseudo-dynamic comparator is made up of two analogue comparators. Unlike a dynamic comparator that uses the input clock signal as a biasing signal by pre-setting and resetting voltage nodes in the various nodes of every stage, an analogue comparator requires voltage bias. In order to generate bias voltages for the two analogue comparators, a biasing block is needed.

This bias circuit is intended to be self-biased and should provide the voltage biases as long as the comparator is in operation. The wide-swing constant transconductance voltage bias shown in figure 6-18 is used to generate the two voltage biases required for the P- and N-comparators. The layout implementation of this voltage bias block is shown in figure 6-19.

Extra poly stripes acting as dummy resistors are added to the layout for poly etching protection at the boundaries. The resistor R1 is key to obtaining the desired voltage biases and any undesired etching should be avoided. The transistors in each stage are grouped together and implemented in an interdigitized manner with multiple fingers to improve matching. As the voltage biasing block is one of the only two analogue blocks in the entire design, a

complete guard ring by itself is necessary to reduce any coupling effect from nearby digital circuitry.

Figure 6-18 The schematic implementation of the wide-swing constant transconductance bias circuit from [94] that is used to provide the voltage biases

Figure 6-19 Layout implementation of the wide-swing constant transconductance bias circuit with the dummy resistors for poly etching protection at the boundaries

6.3.7 Complete Design

The entire design measures $(127.2 \times 148.4) \mu\text{m}^2$, and is shown in figure 6-20. The digital and analogue blocks are highlighted in yellow and red respectively, while the mixed-signal block is highlighted in orange. As mentioned at the start of this chapter, one of the motivations was to keep the analogue blocks at a minimal. Most of the area in this design is taken by digital circuitry, with the TDC being the largest block.

Figure 6-20 Layout of the complete twin-mode Data Converter design with the building blocks highlighted

The analogue circuits are kept to the minimal and for only necessary applications, in this case the voltage biases for the comparator and DAC for D_{OUT} conversion to V_{DAC} . Already shown in figure 6-15, approximately half of the comparator area is taken by the two-stage comparators for the P-input and N-input pair comparators. The remaining half belongs to the arbiters and digital logic for the self-reset structure, edge comparison and output stage. Each of the blocks in the complete design is built with their own guard rings for isolation,

especially necessary between the analogue and digital blocks. The analogue circuitry takes up only approximately 4.45% of the entire design area.

6.4 Results and Discussion

Results are presented and discussed in this chapter, with emphasis first on the characterisation on the delay generator, followed by the dynamic results from the data converter.

6.4.1 Delay line characterisation

The coarse and fine sub-blocks of the delay line have their own bias voltages and needs to be characterised in the same way as the TDC. It is necessary to first understand how the delay cells behave in the delay line with respect to that in the TDC. To do that, all the digital inputs to the delay line are set to logic high to obtain the maximum delay output, T_{IN} for any set of gate and body bias voltages, hereinafter referred to as voltage set. Note that the maximum delay output of the fine sub-block and the entire delay line should not exceed the maximum input time of the fine TDC and the CFTDC respectively.

The gate bias voltages are first swept with a limited range, since the values from the set should not defer too much from that of the CFTDC in Table 4-1. Sets 1 and 2 are taken and the two swept parameters are listed in table 6-2.

Table 6-2 Table of swept voltage parameters of the delay line

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
C1	0.355 ->	0.05 -> 0.15	0	1.2	1.2	0.77
C2	0.365	0 -> 0.06	0	1.2	0.86	1.2

The result of the voltage sweep is shown in figure 6-21 below. Four lines are shown in the figure, with the green and orange lines representing the full T_{IN} , the output of the delay line, and the two blue lines the output of the fine delay sub-block, T_{IN_F} (notated as " T_{IN_f} " in the figure).

Figure 6-21 T_{IN} and T_{IN_F} versus coarse and fine sub-block gate bias sweep from table 6-2

On each line is one coloured dot where the T_{IN} or T_{IN_F} of the un-swept parameters are shown as reference. In order to simplify the notation, un-swept parameters of sets 1 and 2 (in table 4-1) are hereinafter referred to as C1_ref and C2_ref respectively, and the sets with swept parameters as C1 and C2 respectively as per table 6-2.

On the top two lines which represent the T_{IN} values of the full delay line, there is a dependency of T_{IN} on Vbiasp_c, as observed by the multiple minor increments per Vbiasp value. As the Vbiasp value increases, so does T_{IN} , simply because T_{IN} is a summation of T_{IN_F} and the T_{IN_C} , the delay output of the coarse delay sub-block that is influenced by Vbiasp_c. With the reference value for Vbiasp_c at 0.362 V and Vbiasp_c swept until 0.365 V, the highest T_{IN} values naturally do not correspond to the C1_ref or C2_ref sets. The purpose of the above voltage sweep is to narrow down the voltage range of Vbiasp voltages of each set should have. The Vbiasp_c sweep might not have been necessary, but it was necessary to show the influence of this parameter on various T_{IN} parameters.

6.4.1.1 Delay line output measurement

To determine the right biases for the delay line, T_{IN} needs to be monitored. It is possible to do so by isolating the delay line and TDC from the other parts of the design and focussing only on the TDC output, D_{OUT} , by switching to the calibration mode. In this mode, the ENf flag will not have influence on the Up-down encoder, and the 46 bits are switched to the required logic levels for T_{IN} generation. A single rising edge signal is applied to the delay line, st , and T_{IN} is generated based on the applied bias voltages. The TDC automatically generates D_{OUT} , which will not change until the next rising edge since the TDC resets itself only on subsequent rising edges. Set the input st to low before the next rising edge to restart T_{IN} generation. This makes the observation of D_{OUT} with voltage sweep possible.

1. Switch to fine / coarse calibration mode
2. Set the desired voltages
3. Set input st to low
4. Apply rising edge signal to input st
5. Observe D_{OUT}
6. Repeat steps 1 to 4 for voltage sweep

Figure 6-22 gives an overview of the concept of the characterisation of the delay line. In normal operation and by default, the calibration mode is off, represented as $cal[1:0]=0$ in figure 6-22. A “1” represents the fine calibration mode, and a “2” the coarse calibration mode. When the fine calibration mode is active, the 15 coarse bits are all set to logic-zero, so that there is no contribution of T_{IN_C} to T_{IN} . T_{IN_F} is generated based on all 31 fine bits set to logic-one, and the resultant T_{IN} is effectively T_{IN_F} . This mode can be held active as long as it is necessary to obtain the correct T_{IN_F} , i.e. multiple iterations of voltage bias combinations can be performed as long as a repetitive input pulse is provided.

After the fine calibration is performed, the coarse calibration mode sets all 15 coarse bits to logic-one. The contribution of T_{IN_C} is at its maximum, and T_{IN} shall be the summation of both T_{IN_C} and T_{IN_F} . Again, multiple iterations are allowed as long as a repetitive input pulse is provided, and the calibration mode is held active. Finally, the T_{IN} is therefore provided to the TDC via the two input signals

of the TDC, *START* and *STOP* (notated as *TDC_start* and *TDC_stop* in the figure).

Figure 6-22 Block diagram of the setup for delay line measurement

The first step of the characterisation is to check the T_{IN_F} contribution to T_{IN} . Without the contribution from T_{IN_C} , T_{IN} comprises entirely of only T_{IN_F} , which is quantised by the TDC. From the previous results, it was possible to narrow down V_{biasp} for C1 to 0.025 V and 0.03 V, and for C2 to 0.12 V, 0.125 V and 0.13 V. It follows then that it is possible to vary the V_{bd_biasp1} of C1 and V_{bd_biasp} of C2 within a small range to achieve the correct T_{IN} (T_{IN_F}). But for the purpose of showing how much T_{IN} changes, the entire 600 mV range of body bias is swept as shown in table 6-3. T_{IN} should neither be larger than maximum time input of the fine TDC, nor should it be too much smaller. Thus we set the maximum T_{IN} equal to the maximum input of the fine TDC (from characterisation results in Chapter 4), and minimum value at 1% (0below the maximum value. This minimum and maximum values define the pass criteria for T_{IN} .

Table 6-3 Table of swept voltage parameters of the fine delay sub-block of sets C1 and C2

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
C1	0.362	0.12 -> 0.13	0	1.2	0.6 -> 1.2	1.2
C2		0.025, 0.03			1.2	0.6 -> 1.2

The results of the two-dimensional voltage bias sweep are shown in figures 6-23(a) and (b) for sets C1 and C2 respectively. The gate and body bias voltage combinations that result in a passed T_{IN} are also shown in orange distinguish them from the failed points. From these two graphs, there is only one passed combination for set C1, and three for set C2, of which only one shall be chosen.

(a)

(b)

Figure 6-23 T_{IN} versus fine sub-block voltage bias of sets (a) C1 and (b) C2

In the second step of the characterisation, we check both T_{IN_C} and T_{IN_F} contribution to T_{IN} . It may not be useful to check just T_{IN_C} because T_{IN_F} is an always-present element in T_{IN} , and the maximum value of T_{IN} must be checked.

For this, all the 46 digital inputs to the delay line are set to logic-high. We take the determined combinations for the fine sub-block from the first step of characterisation and apply them permanently in this step without sweep. The gate and body bias of the coarse delay sub-block shall be swept as shown in table 6-4 below. By performing a two-dimensional sweep of V_{biasp_c} and $V_{bd_biasp_c}$, a finer tuning of the coarse delay sub-block is made possible. Similarly for the full T_{IN} with contribution of T_{IN_C} , the maximum allowed value of T_{IN} is set as that of the CFTDC, while the minimum value set as 1 ps below the maximum value.

Table 6-4 Table of swept voltage parameters of the coarse delay sub-block of sets C1 and C2

Set	V_{biasp_c} (V)	V_{biasp} (V)	V_{biasp1} (V)	$V_{bd_biasp_c}$ (V)	V_{bd_biasp} (V)	V_{bd_biasp1} (V)
C1	0.36 ->	0.13	0	0.6 -> 1.2	0.84	1.2
C2	0.37	0.03			1.2	0.76

Figure 6-24 below show the results of the two-dimensional voltage sweep of the coarse sub-block bias voltages, with the passed combinations marked in orange for sets C1 and C2 respectively.

Both sets require the same V_{biasp_c} and $V_{bd_biasp_c}$ of 0.364 V and 1.2 V respectively. It appears that set C2 has a lower T_{IN} than C1 due to the small difference in T_{IN_F} which is 34.64 ps versus 34.75 ps. Since the pass range has a maximum value of $T_{IN,max}$ of the TDC, the highest T_{IN} per V_{biasp_c} from 0.365 V to 0.37 V seems to be out-of-range, or higher than $T_{IN,max}$. It can be checked later against the D_{OUT} data.

Another observation here is also the linear increment in T_{IN} with increasing $V_{bd_biasp_c}$. This has already been observed in the CFTDC and VRTDC characterisation. Together with V_{biasp_c} , various combinations of both voltage biases can be used to achieve a desired T_{IN} . The same could also be said for the fine delay sub-block that generates T_{IN_F} .

Figure 6-24 T_{IN} versus coarse sub-block voltage bias of sets C1 and C2

Finally, D_{OUT} values are cross-checked with T_{IN} versus the swept parameters for both sets C1 and C2. The D_{OUT} values are shown in figure 6-25 for both the fine and coarse sub-block voltage sweep. The voltage combinations that pass the criteria for T_{IN} are also marked here for comparison.

(a)

(b)

Figure 6-25 D_{OUT} versus (a) fine sub-block and (b) coarse sub-block voltage bias sets C1 and C2 with marked pass/fail points

In both figures 6-25 (a) and (b), the D_{OUT} for both sets C1 and C2 are shown together, for the fine sub-block and coarse sub-block biases respectively. The pass/fail condition for T_{IN} and D_{OUT} are applied. The pass criteria for D_{OUT} is simply 31_{10} for (a) and 511_{10} for (b). An orange dot represents a pass in D_{OUT} , but a fail in T_{IN} , and a grey dot represents a pass in both conditions. In figure 6-25 (a), C2 and C1 each have a grey dot, while only C1 has an orange dot. The T_{IN} for the orange dot is 35.03 ps, which is not too far off from the resolution of the TDC, which is acceptable. In figure 6-25 (b), there is a grey dot each in both sets, and an orange dot in C2. The T_{IN} for the orange dot is 567.508 ps, which is 0.008 ps more than the $T_{IN,max}$ of the TDC, which is also acceptable. Therefore, the voltage bias combinations for both orange dots could also be used for T_{IN} generation.

In figure 6-25 (b), D_{OUT} drops to 31_{10} for a handful of voltage values. Recall in chapter 4 where the TDC was characterised up to 0.1 ps more than the $T_{IN,max}$, the quantisation time was 0 ns because the D_{OUT} never changed from its initialised value of 31_{10} . These are the points where the T_{IN} is larger than $T_{IN,max}$, and thus represent an overflow condition. In comparison to figure 6-24, these

are the highest T_{IN} values for every V_{biasp_c} after the orange dot. As expected, they are out-of-range. The smallest out-of-range value is 568.579 ps from C2 and the highest is 575.116 ps from C1.

The final voltages for C1 and C2 are given in table 6-5.

Table 6-5 Final gate and body bias voltages for sets C1 and C2

Set	V_{biasp_c} (V)	V_{biasp} (V)	V_{biasp1} (V)	$V_{bd_biasp_c}$ (V)	V_{bd_biasp} (V)	V_{bd_biasp1} (V)
C1	0.364	0.13	0	1.2	0.84	1.2
C2	0.364	0.03		1.2	1.2	0.76

Therefore, it is important to note that the voltage biases provide some form of calibration between the TDC and delay line. And it is also important that the TDC shall be used to check the output of the delay line, so that any offset from the delay cell structure is eventually cancelled out.

6.4.2 Dynamic results

The design was simulated with an input sine wave that has a dc level of 0.6V and a peak-to-peak voltage of 600mV. The frequency of the signal is 29.3 kHz and is sampled at 1 MHz clock via a bootstrapped sample-and-hold circuit presented by Razavi shown in figure 6-26 below.

Figure 6-26 Bootstrapping the sampling switch M11 by fixing its V_{GS} voltage as presented in [95]

Figure 6-27 shows the V_{DAC} as a result of a sampled full sine wave input. The sampled- V_{IN} and V_{DAC} signals are shown as red and blue curves respectively. Generally, it shows that V_{DAC} tracks V_{IN} well except at the top and bottom peak

values of V_{IN} . The V_{DAC} signal appears to be noisy but this is not a result of the DAC architecture. Rather, this is due to the coarse trimming that causes the V_{DAC} to jump with $\pm 75\text{mV}$ per step. Therefore one should expect to see steps on every sampled V_{IN} in two sizes, one for each tuning mode. A zoomed-in view of this trimming is available later in this section.

Comparing both V_{IN} and V_{DAC} curves, there appears to be a gap in the upper peak V_{DAC} values due to a saturation of the TDC output at the input value very close to V_{DD} . This was due to a non-optimal voltage bias provided to the coarse delay sub-block that resulted in a T_{IN} larger than $T_{IN,max}$ of the TDC at the time when this input sine wave was simulated.

There are two lower peak V_{IN} values ($24\text{ }\mu\text{V}$ and 2.13 mV) where the correct V_{DAC} values could not be achieved within the given sampling period. By looking closer at V_{DAC} , it springs back to a certain value. This voltage is 73.61 mV . At the lower V_{IN} values, the end of coarse count is activated and the converter jumps directly into the fine mode after three clock cycles. This explains why the initial value seems to always start at 73.61 mV , which is equivalent to the initialised D_{OUT} of 31_{10} . The converter attempted to trim V_{DAC} down to as low as possible, as proven by the existence of a saw-tooth line heading towards 0 V . Recall that the maximum number of steps for V_{DAC} in the fine mode is 31, and the total time required including some coarse trimming takes is in reality longer than $1\text{ }\mu\text{s}$. But due to the fact that most trimming do not require all 31 fine and 15 coarse steps, the quantisation time was limited to just $1\text{ }\mu\text{s}$. Therefore, in the cases of these two V_{IN} values, there was unfortunately not enough time for V_{DAC} to finally arrive within $\pm 1\text{ LSB}$. The V_{DAC} values before and after show that $1\text{ }\mu\text{s}$ is sufficient even for low V_{IN} values. While increasing the period increases the chances of obtaining D_{OUT} equivalent of the two voltage inputs, it comes at the expense of a longer sampling time for the majority of the V_{IN} samples.

Figure 6-27 V_{DAC} follows V_{IN} for most of the input samples

Figure 6-28 below shows a segment of the V_{DAC} vs V_{IN} curves, where the two modes of trimming can be observed. The activation of the RDY flag is also shown when the conditions are met. Also shown in the figure are the coarse-fine switch flag, ENf and the equivalent D_{OUT} in unsigned decimal at the bottom of the graph.

The V_{DAC} (annotated as DACout in the figure) in blue appears to have two behaviour for every V_{IN} sample in red. Initially there are huge steps followed by very fine steps that stick rather close to V_{IN} . Next, the ENf (annotated as $/ENf<0>$ in the figure) in pink toggles between logic-zero and –one throughout. Recall that when ENf is raised high, the fine mode is active. Therefore, the logic-zero and –one represent the coarse and fine modes respectively. Compare this with the V_{DAC} line, the big steps happen during the low pulse of ENf , and the fine steps occur during the high pulse of ENf . Each coarse step is 31 times that of a fine step, thus in the coarse mode, any adjustment in the T_{IN} and consequently V_{DAC} is naturally huge, otherwise the two-mode does not work correctly. Recall also that the switching of modes require CMP_out to be 0-1-0, therefore some switch between higher and lower levels are expected to be seen on V_{DAC} in the coarse mode. Also, the coarse mode is only active for a much shorter time than

the fine mode, because the conditions for the coarse-fine switch could be met within a few coarse steps.

Figure 6-28 Segment of the input sine wave showing how V_{DAC} is trimmed to every sampled- V_{IN}

In the fine mode where the step size is much smaller, V_{DAC} changes less drastically. For example the first D_{OUT} of 426₁₀, after the data converter switches to the fine mode, V_{DAC} is reduced in very fine steps to where its corresponding V_{IN} is. When V_{DAC} finally reaches ± 1 LSB of V_{IN} , the RDY flag switches to logic-one. It is also evident that although V_{IN} changes periodically every 1 μs , the low pulse duration of RDY is much shorter than 1 μs , which means that the data converter does not need the full sampling period to have the final D_{OUT} , at least for the shown segment of V_{IN} . The sampling period of V_{IN} could theoretically be shorter than 1 μs , but this was not done so as to give sufficient time for enough loop iterations to take place, in consideration of the worst case number of steps needed to be taken for V_{DAC} to arrive within ± 1 LSB value of V_{IN} . While the sampling frequency can nevertheless be increased, there is a risk of some missed data, i.e. RDY not switched to logic-high.

So, V_{DAC} in figure 6-28 is not the real analogue-converted voltage of D_{OUT} , but rather the ever-changing D_{OUT} before and after an activated RDY flag. To show

a glimpse of how D_{OUT} looks like upon ready, figure 6-29 shows a segment of D_{OUT} converted back to an analogue voltage (V_{OUT}) with an ideal DAC, after the activation of RDY . As a comparison, the red curve in the sampled V_{IN} data, and the black curve represents the converted V_{DAC} .

Figure 6-29 A segment of V_{OUT} (output code generated with ideal DAC) versus V_{IN} after activated RDY flag

The digital output code for the entire input range is plotted in figure 6-30. Notice that the low V_{IN} values in figure 6-30 start at 31 instead of 0 due to the issue of restricted quantization period of $1\ \mu\text{s}$ that is insufficient for extreme low V_{IN} values, and this is already seen in the V_{DAC} in figure 6-27. The DNL of the initial V_{IN} values have been set as 0 in the DNL graph in figure 6-31. The minimum and maximum DNL of the proposed converter is calculated to be $-0.573/1.133$ LSB.

Figure 6-30 Digital output code versus V_{IN} of the proposed data converter

Figure 6-31 Differential Non-Linearity (DNL) of the proposed converter

The adjusted (calibrated) output delay T_{IN} is also plotted against the input voltage, V_{IN} in figure 6-32. The digital output data is also added into the figure to show how the latter changes with T_{IN} against V_{IN} . For comparison sake, the ideal $T_{IN,ideal}$ is shown as a function between $T_{IN,max}$ and $V_{IN,max}$.

Figure 6-32 Adjusted T_{IN} in comparison to the ideal $T_{IN,ideal}$ versus input voltage, with the digital output code

The V-T results are zoomed into two smaller ranges for in the lower and half Vdd-range. Figure 6-33 below shows the results for 200 mV to 300 mV in orange and 900 mV to 1 V in blue.

Figure 6-33 Adjusted T_{IN} versus input voltage for two smaller ranges

The V-T lines are not perfect straight lines, meaning that some non-linearity exist in the transfer function. This could lie in the measurement points of the output delay. Nevertheless, the monotonic increment of D_{OUT} and T_{IN} with V_{IN} is similar to figure 5-19, meaning that a linear Voltage-to-Time relationship is obtainable via the proposed methodology of data mapping.

A typical power consumption of the entire converter for one quantization cycle or one V_{IN} sample is shown in figure 6-32. The breakdown of the peak is illustrated in the figure. The peaks occur at a periodic 12 ns, which is the time interval between every loop of complete time quantization cycle and feedback. In each quantization step, the high peak currents occur during the TDC quantization and a lower peak current is a result of all nine bits being latched by the flip-flop array simultaneously. The data converter consumes an average power of 976.121 μW during quantization and a static power consumption below 400 μW at standby mode.

Figure 6-34 Power consumption of the proposed data converter during one iteration of a complete sampling period

For a 29.3 kHz full-scale sinusoidal input, the discrete fourier transform of the twin-mode data converter digital output is shown in figure 6-33. The frequency of the input signal is chosen as follows:

$$F_{IN} = \frac{N_{prime}}{No.of\ samples} x F_S \quad (6.10)$$

, where the number of samples is chosen to be 1024, and N_{prime} shall be a prime number, in this case 11. This is to avoid aliasing for harmonics.

The SNDR given by the spectrum tool in cadence is approximately 52.35 dB, which will give an effective number of bits (ENOB) of 8.4 using the equation below:

$$ENOB = (SNDR - 1.76)/6.02 \quad (6.11)$$

Figure 6-35 Output spectrum using discrete fourier transform of the output data

Finally, a comparison with the other VTC schemes in the literature is shown in Table 6-6.

One of the main motivation for the proposed design is to increase the quantisable input range while ensuring linear V-T conversion. The proposed VTC uses the data mapping scheme and delay trimming to achieve full-V_{dd} input range. From the table 6-6, it can be seen what the various input ranges are in comparison to the supply voltage. The current starving approach used in [96] uses both PMOS and NMOS current starving transistors to increase the range up to twofold of what was presented in [28]. The linearity is improved with

the weak transistor in parallel to the current starving transistors. Due to the simultaneous V-T conversion using PMOS and NMOS, the input range achieved was between 384 mV and 675 mV. A fast sampling rate is obtainable via this approach, but the input range is reduced for a very focussed and narrow linearity region for the rail-to-rail range. An even faster VTC is presented in [84], where the V-T conversion takes only 100 ps, giving it a sampling frequency capability of 10 GHz. Similarly, a weak shunt transistor is added in parallel to the current starving transistor for low V_{IN} values as in the former. The input range is not given, but it is unlikely to be very large since the sampled V_{IN} drives the NMOS current starving transistor.

In comparison, the Time-mode SAR ADC in [90] uses both digital- and voltage controlled delay line (DCDL, VCDL), an approach similar to the previous TDC-based VTC in Chapter 5. However, the V_{IN} is “sampled” via a capacitive DAC and used as a reference for to tune the VDAC which eventually drives the VCDL. In the former’s design, the V_{IN} determines the T_{OUT} , therefore limiting the region where the transfer function is rather linear with reasonable number of trimming steps. Using high V-T gain Thyristor-based delay cells in the VCDL, the input range in [90] could reach 100 % of the Vdd Supply which is at a reduced 0.6 V. This approach however requires a lot of calibration at the start to align the phases of the VTC output with the main clock signal. The FoM is small due to the lower switching activity which results in lower power consumption.

The sampling capacitor approach, which is by far most popular and widely used is presented in [83, 86, 88]. This approach was chosen in [88] for high-speed operation. The VTC design is relatively simple, using a current starving structure to discharge the sampling capacitor. An external voltage bias limits the current and consequently the discharge time. Since a differential input is used, the VTC output is an absolute time difference, and not with respect to zero time. It is asserted that this improves the linear range although not given. The range is unlikely to be high since the differential inputs are connected to the drain of two cascoded NMOS. A similar VTC structure is found in [83] but the input range is about 80 % of the supply voltage, thanks to the constant current pairs implemented to improve the voltage-current gain and also overcome PVT influence. Finally in [86], a charge pump and a phase detector are used to

modify the capacitor discharge current source to achieve a specific time range even under PVT variation. An automatic calibration of the current source is performed by sampling constantly the reference voltage, the input voltage and ground voltage in a loop. This comes at the expense of a higher power consumption. A negative voltage source is necessary to perform the discharge of all three voltages to the same voltage level. Since the longest time taken to discharge the sampling capacitors is equal to the dynamic range of the TDC, there is no latency, and a relatively fast discharge time is necessary for TDCs with high resolution. Therefore, the sampling capacitor approach tends to result in short conversion time.

Another approach to V-T conversion is the use of traditional VCO in both [92, 93]. The latter uses simply a Ring Oscillator built with CMOS inverters from the standard cell library with its supply voltage varied through the VTC input range. The obtainable VTC input range is between 0.7 V and 1.3 V for a 1.3 V Vdd Supply. In the former, a programmable 1-bit folded VCO, capable of providing a wide tuning range with high linearity is used. A higher input range of 0.7 V for a 1.2 V Vdd Supply was obtainable.

One drawback of the proposed design is the need for multiple iterations to obtain the final output delay. The idea of the loop is to adjust the initially generated delay to obtain a V_{IN} -equivalent T_{OUT} . This occurs at the expense of the conversion speed because of the time necessary for delay trimming. Unfortunately, the sampling frequency is one of the lowest in table with other compared works.

As a result of the high activity needed to perform delay correction, the power consumption is relatively high for a rather low sampling frequency. This arises from the high switching activity in the TDC, one of the major power contributors, that is quantising the time inputs in multiple iterations per voltage sample and also the flip-flop array where all 9 bits are latched in parallel resulting in large peak currents. In comparison to the other works, the power consumption seems to be high for a design with lower sampling frequency. When the FoM is considered, the proposed design is in the range of pico-Joules per conversion step while the other designs achieve up to only hundreds of femto-Joules per conversion step.

The supply voltage used in this work is not the lowest, but it is possible for the proposed mapping concept to operate at 1 V. One of the advantages of this data mapping concept is the reconfigurability. This may be in terms of number of bits or the supply voltage. This reconfiguration is relatively easy to implement, because of the modular nature of the building blocks. Some characterisation is necessary at the design stage to ensure the boundary conditions with regards to the time generator and time quantiser. In order for the proposed VTC to work at lower supply voltages, some readjustment of the delay cells that were characterised to work at 1.2 V will be necessary too.

With regards to the area consumption, the proposed design is not the smallest in the table, but is one of the smallest for the designs in 65 nm technology. In comparison to the delay line approach, whose delay trimming is performed by NMOS-enabled capacitors as varactors, the proposed design has a much smaller area consumption. This is partly due to omission of varactors, but using the idea of bypassing delay cells to achieve delay variation. The other designs have no delay trimming, and thus have very competitive area consumption. Moreover, the amount of analogue circuitry in the proposed design was reduced to the bare minimum required, in this case the comparator and the DAC.

Therefore, the proposed VTC offer the following advantages:

1. Ease of implementation
2. Reconfigurability
3. Small area consumption

And the disadvantages of relatively high power consumption and slow conversion speed are obvious in this design. Both parameter metrics may be improved by sharpening the trimming process which is the primary reason for the high switching activity and time taken within the loop.

Table 6-6 Performance comparison with other time-domain ADC architectures

Reference	[96] JECEC C '16	[84] CICC '15	[90] TCAS II '14	[88] ISSC Letters '19	[86] DCAS '09	[83] JSSC '19	[93] TCAS I '14	[92] ASSCC '16	This work
Scheme	Cur. starve	Cur. starve	DCDL/ VCDL	Samp. cap	Samp. cap	Samp. cap	VCO	VCO	Mappi ng

Supply [V]	1.2	1.3	0.6	1	1.5	1	1.3	1.2	1.2
Input range [V]	0.291 (sim.)	-	0.6	-	1.2	0.8	0.6	0.7	1.2
f _s [MHz]	200	10,000	0.1	4000	227	1000	205	50	1
SNDR [dB]	-	27.2	-	39.9	-	44.4	50.3	65	52.35
Power [mW]	-	98	0.002	11.7	22 (sim.)	2.3	3.3	11.65	0.976 (sim)
ENOB	7.6	4.3	8.02	7	11	8	8.1	10.5	8.4
FoM [pJ/(conv. Step)]	-	0.48	0.065	0.023	0.047	0.009	0.059	0.161	2.889
Area [mm ²]	-	0.073	0.127	0.017	-	0.007	0.026	0.047	0.019
Tech. (nm)	65	65	110	28	130	65	65	65	65

ADCs with sampling frequencies of 5 MSPs (Samples per second) or less are generally of SAR and Multi-slope ADC architectures. Such ADCs can be used in the following applications:

1. Precision Measurement and Sensor Conditioning
2. Multichannel Data Acquisition Systems
3. Digital Audio
4. Precision Analogue Microcontrollers
5. System Supervision and Control
6. Industrial Control and Automation
7. Power-Supply Monitoring
8. Portable Systems

The first four applications are from Analog Devices [97] and the next four applications are typical applications used with sub-5 MSPs ADCs from Maxim Integrated.

Measurement and Sensor applications require wide dynamic range, and some do not require high sampling rate unlike Radio systems. ADCs are used in test systems for example where the measurement of a high programming and erase voltages in an EEPROM IP is down-converted to lower voltages and converted to digital codes. This aids not only in the measurement of generated high voltages in the analogue supply domain but also provides digital bits for trimming the charge pump generated voltages. Data acquisition systems in measurement and process control have multiple channels to digitise analogue signals for processing by ADCs have lower sampling and throughput rates in kHz to single

digit MHz. But these systems require ADCs with input range capability up to the V_{dd} Supply. Digital Audio applications that have varying sample rates from 32 kSPS in FM Stereo to 192 kSPS in DVD Audio and high number of bits. The proposed time-domain ADC has the advantage of reconfigurability whose number of output bits is dependent on the TDC performance. One of the key requirement for audio application is the SNR which can be reduced if the input range is sufficiently large. In the application of analogue microcontrollers, data is not only converted from analog to digital, but also processed by local embedded processing units. These microcontrollers generally need only hundreds of kSPS sampling frequency but also wide input range for features like on-chip V_{dd} monitor.

A highlight in Maxim Integrated's recent ADC development is the programmable Mixed-signal I/O ports that allows ADC, DAC or general purpose IO functionalities, which have use in power-supply monitoring or control for optical components. For these ADCs, the input ranges are either at the internally generated reference voltage or at the full V_{dd} supply, indicating the need to have a wide-input range feature regardless which ADC architecture is used.

The use of voltage-domain ADCs in the applications mentioned so far are generally of SAR, Multi-slope and even sigma-delta architectures. The use of Voltage-Time-Digital ADCs are not available in the industry yet, most probably due to the bottleneck of the VTC.

6.4.3 Non-idealities

This section describes some of the non-idealities that the VTC may operate it. This includes non-zero comparator offset, variation in supply voltage and temperature. It was shown in chapters 3 and 4 that the TDC resolution can be affected by temperature and supply variations, and this should be expected as well for the VTC. Under varying temperature and supply conditions, the digital part of the VTC will work faster or slower than at typical conditions. However, because the delay generator whose output delay is dependent on these two parameters, it is important to investigate the effects on non-idealities on the former, and how the bias adjustment can be performed to achieve the ideal output delay.

6.4.3.1 Comparator Offset

Figure 6-36 Block diagram of the proposed VTC with additional comparator offset

A comparator offset is introduced to the proposed VTC as shown in figure 6-36 to investigate the functionality of the proposed VTC under the influence of comparator offset. The comparator offset is added to the sampled- V_{IN} and is varied from -50mV to +50mV. The observation is that the VTC simply takes the new V_{IN} , which is effectively the sampled- V_{IN} in addition to the comparator offset as the new reference and adjusts V_{DAC} towards it, as seen in figure 6-37. Therefore, any comparator offset becomes a systematic offset to the whole converter. This offset can be removed by first characterising the VTC with defined V_{IN} values and calculating the systematic difference between the known V_{IN} and output V_{DAC} .

Figure 6-37 Comparator offset vs. VDAC and VIN

6.4.3.2 Voltage supply variation

In the earlier chapters, it has been shown that the delay is dependent on supply voltage, and more influenced by lower supply voltage where the delay output can increase too much. A higher supply voltage is less critical and requires only a bit of bias voltage adjustment. Therefore, using the same low Vdd condition of 1.08 V for the proposed VTC, we attempt to calibrate via the existing supplied biases in order to achieve an output delay that is within the TDC specification.

The same steps are taken as described in section 6.4.1.1 for the delay line characterization. The Vdd low biases from the TDC have to be used here, i.e. Table 4-8, and the fine delay sub-block is first adjusted before the coarse delay sub-block. Based on the mentioned table, it is possible to narrow down the sweep range of the gate and body biases of the fine delay sub-block. A gate bias range of 0.08V to 0.1V shall be necessary, and a body bias sweep from 0.6V to 1.2V.

Figure 6-38 below shows T_{IN_F} with fine sub-block voltage bias sweep. As a reference, the T_{IN_F} under nominal supply condition is marked in orange, and the value at low Vdd without change in biases is shown in the blue point directly above it. This is approximately 37 ps against 44 ps respectively as shown in the figure.

To reduce the T_{IN_F} , the decrement of Vbiasp is to be expected, and a good combination of the gate and body bias shall be 0.09V and 1.03V respectively, in comparison to the TDC's 0.09V and 0.84V respectively.

Using the fine delay sub-block biases, the final T_{IN} can be checked against voltage sweep. The results of the sweep are plotted in figure 6-39, where the orange point again shows the nominal supply T_{IN} , and the T_{IN} without low Vdd calibration is shown in the blue point directly below it. While T_{IN_F} is longer at low Vdd than at nominal Vdd, T_{IN} on the other hand is shorter. Therefore, T_{IN_C} needs to be increased, and this should be done via an increment in Vbiasp_c. The final gate bias voltage shall be 0.377 V in comparison to the TDC's 0.389 V.

Figure 6-38 Fine delay sub-block output versus gate and body bias at low Vdd condition

Figure 6-39 Full delay block output versus coarse gate bias at low Vdd condition

The final bias values for low Vdd supply condition are shown in Table 6-6 below.

Table 6-7 Final gate and body bias for the delay generator at low Vdd

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
C1_Vdd low	0.377	0.09	0	1.08	1.03	1.08

6.4.3.3 Temperature variation

Higher temperatures result in lower threshold voltages and higher leakage, and the resolution of the TDC is smaller (in terms of picoseconds) as a result of increasing temperature. Therefore, using the same high temperature condition of 125°C for the proposed VTC, we attempt to calibrate via the existing supplied biases in order to achieve an output delay that is within the TDC specification.

Again, the same steps are taken as described in section 6.4.1.1 for the delay line characterization. The HT biases from the TDC have to be used here, i.e Table 4-3, and the fine delay sub-block is first adjusted before the coarse delay sub-block.

Figure 6-40 below shows T_{IN_F} with fine sub-block voltage bias sweep. As a reference, the T_{IN_F} under room temperature condition is marked in blue, and

the value at high temperature without change in biases is shown in the orange point directly below it. This is approximately 37 ps against 31 ps respectively as shown in the figure.

To increase the T_{IN_F} , the increment of V_{biasp} is to be expected, and a good combination of the gate and body bias shall be 0.13V and 0.91V respectively, in comparison to the TDC's 0.15V and 0.94V respectively.

Using the fine delay sub-block biases, the final T_{IN} can be checked against voltage sweep. The results of the sweep are plotted in figure 6-41, where the blue point shows the room temperature T_{IN} , and the T_{IN} without HT calibration is shown in the orange point directly below it.

An increment in V_{biasp_c} is expected to increase the T_{IN} , and the final gate bias voltage shall be 0.394 V in comparison to the TDC's 0.389 V.

Figure 6-40 Fine delay sub-block output versus gate and body bias at high temperature condition

Figure 6-41 Full delay block output versus coarse gate bias at high temperature condition

The final bias values for high temperature condition are shown in Table 6-7 below.

Table 6-8 Final gate and body bias for the delay generator at high temperature

Set	Vbiasp_c (V)	Vbiasp (V)	Vbiasp1 (V)	V_bd_biasp_c (V)	V_bd_biasp (V)	V_bd_biasp1 (V)
C1_HT	0.394	0.13	0	1.2	0.91	1.2

6.5 Conclusion

A novel technique of converting voltage input to a delay and digital equivalent has been presented. The objective was to leverage on the fast switching time of transistors in advanced technologies and thus faster quantization time in a Time-to-Digital Converter and to overcome the limitations of a voltage-to-time conversion technique related to lengthy conversion time and inherent non-linear and inverted conversion factor between the two domains. The design was also intended to be a digital-intensive implementation, to reduce area consumption.

In the proposed technique of matching the full ranges of the voltage and time domains, no conversion factor is required between voltage and delay, which

otherwise depends heavily on the architecture of the VTC and calibration techniques to linearize the relationship. Instead, only the ratios of the input voltage to its input full range of each domain are of interest here. This allows individual converters in each domain to work independently yet together in a feedback loop, i.e. the TDC and DAC, to tune the output delay to achieve the desired output equivalent of the sampled input voltage.

It was also proposed in this design to generate delay with a different method, where no digitally-controlled varactors or delay elements are used to (un)load the delay line to achieve the desired output delay. Instead, the delay cells in the delay line are either bypassed or passed through to achieve variable delay, essentially achieving the same goal as loading a delay line with delay elements or capacitor banks. Moreover, since the Vernier principle and body-biasing technique are used in the delay line as in the TDC, sub-gate delay and essentially fine delay tuning could be achieved. Together with a mixed analog-digital comparator, a TDC and a DAC, the feedback loop allows the converter to quantise a full- V_{DD} input range and linearly represent the input voltages in both delay and digital domains.

The proposed design was tested for concept feasibility with a 29.3 kHz sinusoidal input and a 1 MHz sampling frequency. The results show that the V_{DAC} has been able to follow the sampled V_{IN} throughout the entire sinusoidal period. An output spectrum of the proposed design suggests an SNDR of 52.35 dB with a calculated ENOB of 8.4 bits for the 9-bit converter. Unfortunately, the need for multiple iterations adds to the time required for quantisation, and thus limits the sampling frequency. This could be tackled with some methods that are suggested in the next chapter for future research.

7 Conclusion and Recommendations

7.1 Conclusion

This research was set out to suggest an alternative to the traditional VCO method of voltage-to-time quantisation and to overcome the inherent non-linear voltage-to-time relationship for time-mode ADCs. Initially, the idea of using sampling capacitor was also considered but there were issues with regards to the time-varying comparison of input and threshold voltages for delay pulse generation over an input range as wide as possible. Solutions with the use of constant- g_m structure in the comparator could not overcome this problem completely. Moreover, capacitive sampling was already a mature idea with many good examples shown earlier. The difference between those methods was significant in the way the input voltages were sampled and processed, with fundamentally similar ideas but different approaches to linearise the capacitor discharge. Current starving methods were also considered in the initial designs but had shown little potential in overcoming the non-linearity of voltage-to-time conversion.

There was thus a need to find a novel way of representing voltage samples as delay time. The initial idea was to put a TDC in a feedback loop in a TDC-based Voltage-to-Time Converter. The raw delay output that is generated by an analogue-mode delay line is trimmed by digital varactors until the final delay output is a linear representation of the input voltage. The linearity is defined as the linear increment of output delay for a linear increment in input voltage, which is in its raw form exponential. Since a TDC is a linear time-to-digital converter and a DAC is a linear digital-to-voltage converter, they give a linear representation of the generated delay in digital bits and voltage. Therefore, the linearity of the VTC is simply enforced by the two converters when they are implemented in a feedback loop.

In the implementation of time-mode ADC, a TDC needs to follow a VTC. A TDC using the Vernier principle in a ring form, called a Vernier Ring TDC (VRTDC) was developed for this purpose. In varying the resolution of the TDC, gate voltage biasing has always been used to alter the current flowing through the

delay cells. But this method of biasing is very coarse. For this reason, a novel voltage tuning method via body-biasing was added to provide a 2nd and finer degree of resolution adjustment. Body-biasing consequently became the default method to obtain very fine delay differences in a delay cell, which was especially useful in TDCs.

It is intuitive to note that the VRTDC could also be used in the feedback loop of the TDC-based VTC. Although the VRTDC has the benefits of a sub-gate delay resolution and variable input range (depending on the digital counter), it has a large latency, defined as the time delay between the availability of the input to the output. Using the VRTDC in the feedback loop thus slows down the voltage-to-time conversion cycle. The latency increases by 2^n as the n -number of output bits increases. Therefore, a new TDC concept to quantise time in two-steps, CFTDC was developed to overcome the latency issue. The CFTDC uses the body-biasing technique to calibrate the resolution of the coarse and fine TDCs such that both TDCs adhere to the basic rule of the full input range of the fine TDC equals to the resolution of the coarse TDC. The violation of this rule will result in quantisation error in any two-step TDC architectures. It was also developed for this TDC the idea of transferring the residual time input from the coarse to the fine TDC without additional propagation delay added to the residual time. The result is a 9-bit CFTDC with a resolution of 1.08 ps with a sampling speed of up to 0.4 GHz.

Even with a faster TDC, the major contributor to the bottleneck in the quantisation speed of the TDC-based VTC was still the generation of the output delay via V_{IN} . Also, the non-linearity characteristics of the voltage-to-time relationship meant that for certain values of V_{IN} , the output delay was far from its ideal (linear) value and for some others, it was close. For this reason, some range of the input voltages required in comparison a very high number of corrections, and consequently limits the maximum sampling speed of the VTC. Also, the maximum ranges of the voltage and delay domains had to be matched with great effort, through delay cells sizing, voltage biasing, etc.

Understanding the shortcomings of the initial TDC-based VTC, it would be a better solution to not involve V_{IN} for the conversion between data domains. Therefore the TDC correction system in the VTC evolved into a novel idea of

mapping data from one domain to another. This meant that no conversion factor is required between data types, but instead, only a common reference is needed. In this idea, the full scale of the input voltage $V_{IN,max}$ was matched to the full scale of the input time $T_{IN,max}$ by reusing the TDC delay cells. With the matched full scales, the sampled input voltage is simply used as a reference to compare with the feedback voltage from the TDC correction system. Using V_{IN} as a reference is also generally what gives voltage-mode ADCs the edge in speed over time-mode ADCs. Through the means of matching, the ratio of V_{IN} -to- $V_{IN,max}$ is kept the same as T_{IN} -to- $T_{IN,max}$ by only trimming T_{IN} .

The final product is a converter that converts V_{IN} into its equivalent value in two domains, time and digital. The new voltage-to-time conversion technique has been implemented as a 9-bit converter and simulated for concept feasibility. The design was tested at a sampling frequency of 1 MS/s, with an average power consumption of 976.121 μ W.

The twin-mode data converter also has the added advantage of interchangeability if less number of data bits and higher sampling frequency is desired. Since the delay cells in the delay generator are the same as that in the TDC, the “plug-and-play” idea can easily be realised by interchanging the delay quantiser and generator for another set. With the initial TDC-based VTC concept, the delay line needs to be re-calibrated at the design stage with great effort for different performance requirements.

7.2 Recommendations for future research

Some of the areas of further improvement for the novel concept of voltage-to-time conversion include the operating speed, the calibration of the voltage biases and the implementation of standard library cells for performance optimisation.

7.2.1 TDC measurement circuit

For extensive TDC measurements, it is necessary to be able to measure inputs that are a fraction of the TDC resolution. As long as an external circuit is used to input time to the TDC, not even the input times that are equivalent to one LSB

can be measured for TDCs with high resolutions, i.e. single digit picoseconds. Consider also the fact that rising times of externally supplied signals are in the range of nanoseconds, and through a buffer in the monolithic IC, one is able to reduce the rising time to just picoseconds. However, two rising edge signals are needed for TDC, and the offset between both buffers is unknown, which adds an unknown offset to the T_{IN} .

It is probably meaningful to have a built-in delay generator, where T_{IN} is generated internally. Figure 7-1 (a) below shows the concept of the Delay Generator for TDC measurement that was developed but could not be completed.

(a)

(b)

Figure 7-1 (a) Concept of built-in delay generator for TDC measurement, (b) Implementation of the delay cell in the delay generator

This concept was then used in the proposed twin-mode VTC in chapter 6 for delay generation. Note that there is no analogue input required, which was one of the main goals of the proposed design. The delay generator works simply by doing a count from 0 to $2^{(N-1)}$, where N is the number of bits of the counter, and T_{IN} is automatically generated between *START* and *STOP*. Of course to achieve very fine delay, body biasing is needed, and once again proves itself useful in time circuits. Also the counter generates a thermometer code to bypass delay cells as shown in figure 7-1 (b). Hence no varactors or capacitor banks are required whose delay is unknown and whose cell-to-cell offset can add to the unknown offset of T_{IN} .

However, one consideration here is the reference. How is it possible to ensure that the generated T_{IN} is correct? Perhaps a Delay-Locked Loop concept could be added to the given concept to achieve zero phase difference with different T_{IN} values. Therefore, this requires further work on the concept, but seems to be a promising idea.

7.2.2 Standard Library cells

Implementation of standard cells for the digital logic could be used to optimise area and power consumption. This requires not only a standard cell library that is usually available in Process Design Kits (PDKs), but also scripts for automatic place and route and digital synthesis of behavioural codes. The intended behaviour of the digital logic should be described in Verilog or Verilog-A. This not only aids in the initial conceptualisation and reduction of design costs but also allows a much faster simulation of the design proof-of-concept, which otherwise is slowed down greatly by the transistor implementation of huge digital blocks. Parametric cells that are also available in standard PDKs can be used additionally to customise the transistor sizes to achieve certain design goals, for example an intentional mismatch in rise and fall times of the logic gate output signal.

Usage of standard library cells for design is not uncommon, such as an all-digital VCO-based ADC in [93] that occupies only 0.026mm^2 and also a cyclic Vernier

TDC fully synthesized from a standard cell library for application in ADPLL in [10].

7.2.3 Automatic calibration

Automated calibration of the delay line can be done by means of a DAC to adjust the voltage biases of the delay cells in the twin-mode data converter. The delay difference between the delay cells or lines could be quantised by the TDC to generate a digital output. This output gives the information on the delay difference of the two cells or lines in the same way the generated T_{IN} from the digital controlled delay line is trimmed to the expected ideal T_{IN} in the proposed voltage-to-time concept. Preferably, a high resolution TDC and the same TDC should be used such that any offset in the time-to-digital conversion is kept the same in calibration and operating modes.

7.2.4 Sampling speed increment

In order to increase the sampling speed, the following options can be considered. They are not exclusive to each other, which means that a solution using a single or mixture of the suggestions can be implemented. A mixture of two or more solutions however increases the complexity.

7.2.4.1 Parallel implementation

The use of parallel delay generators and TDCs can be considered to increase the sampling speed. The bottleneck in the speed of this design is the generation of the output delay. Using multiples of the same circuit in operation can increase the operating speed at the expense of area. For example, four TDCs in parallel were used [84] to achieve a final 10GS/s sampling speed, which otherwise operated at 2.5GS/s individually.

7.2.4.2 Multi stages

The speed advantage in a flash TDC or a flash ADC is that the input is broken down into many smaller blocks for quantisation. The twin-mode Data Converter is an ideal candidate for such means because the entire quantisation operation

is independent of the input voltage – only a reference (full scale) is required, which can be differently defined for each stage, as in the case of a flash ADC.

Figure 7-2 gives an idea how this can be achieved. The input voltage is sampled and broken down into segments (depicted by the resistor ladder). Each VTC stage will obtain its own input sample. It is intended here to have TDCs and DACs with lower bit count. Therefore, the full ranges are reduced accordingly. An adder at the last stage will add up all the output bits from the various stages to give the final D_{OUT} .

Note that this method can also be used for higher number of output bits where the increased bit count requirement might be too time-demanding on the current 9-bit converters. It is recommended that two or more stages be used to go further than the designed 9 bits.

Figure 7-2 Multi-stage concept to increase sampling speed

7.2.4.3 Time-interleaving for multiple T_{IN} generation

Moreover in this design, T_{IN} generation is based on a single rising clock edge. Therefore, it allows the use of time-interleaving technique to generate multiple sets of T_{IN} on different clock phases. Either multiple TDCs or a single (very high speed) TDC can be used to quantise the multiple sets of T_{IN} . Illustrated in figure 7-3 is the idea where the delay generators are time-interleaved by sampling V_{IN} at different clock phases. The feedback block is also time-interleaved to perform

the delay-digital-analogue conversion. Note that t_q is the time catered for the generation of the output delay (including generating the digital trim codes) and arbitration of the comparator inputs.

Alternatively, a single sample-and-hold circuit with faster sampling clock frequency can also be used to obtain more samples. Therefore, there would not be a need to have multiple sampling circuits.

Figure 7-3 Time-interleaving concept with a shared single feedback element

7.2.4.4 Pipelining

Pipelining is also a popular method to increase operating speed. By breaking down the entire structure into multiple stages, each stage only needs to carry out a smaller and perhaps different operation simultaneously with other stages. For example, while the comparator arbitrates V_{IN} and V_{DAC} , the delay line can simultaneously generate a delay, and the TDC could be quantising some delay, with the DAC converting the TDC output to V_{DAC} . Such an implementation requires some form of handshaking between each stage and index tab to separate the data sets. It is obvious here that the complexity might be an overkill for a simple system design.

7.2.5 Different trimming concept

At the moment, the fine trimming bits are always reset to a default value of 32_{10} regardless of the coarse trimming bits upon every new sampling phase. This

also means that for every new input voltage sample, the fine trimming code has to start from the top and work all the way down the 32 steps in the worst-case. This adds to the total quantisation time. Instead of setting the fine trimming bits back to its default value, the trimming could continue from its last position. However, extra logic is necessary to detect the crossing of the lower and upper coarse levels, and update the coarse bits correspondingly. Further to this, the coarse trimming bits must not be frozen when the fine mode is enabled, as in the case of the current design. In other words, the coarse trimming logic must detect the carry-in and carry-out (like in a full adder) when the overflow in the fine trimming occurs. Otherwise, V_{DAC} will not reflect the updated coarse trimming levels.

7.2.6 Increase output bit count

The number of output bits can be increased relatively easily by replacing the TDC with a higher bit count. Assuming the same TDC resolution is used, the input dynamic range of a higher bit count TDC will increase, and therefore requires a change in the delay generator. Fortunately, since the delay elements are the same as those in the TDC, the change only requires extra delay stages to implement. This is also the advantage of this design where it allows easy replacement of building blocks to achieve different design goals.

Alternatively, the idea of using multi-stage elements can also be used as described earlier in this section.

Author's Publications

J. Kong, L. Siek and C. Kok, "A 9-bit body-biased vernier ring time-to-digital converter in 65 nm CMOS technology," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 1650-1653. DOI: 10.1109/ISCAS.2015.7168967

C. Kok, X. Li, L. Siek, D. Zhu and J. J. Kong, "A switched capacitor deadtime controller for DC-DC buck converter," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 217-220. DOI: 10.1109/ISCAS.2015.7168609

J. Kong, S. Henzler, D. Schmitt-Landsiedel and L. Siek, "A 9-bit, 1.08ps resolution two-step time-to-digital converter in 65 nm CMOS for time-mode ADC," *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Jeju, 2016, pp. 348-351. DOI: 10.1109/APCCAS.2016.7803972

J. Kong, L. Siek and S. Henzler, "A novel conversion technique for Voltage-to-Time Converters for application in time-mode Analog-to-Digital Converters," – submitted to The Journal of Engineering

Bibliography

- [1] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A 9-channel integrated time-to-digital converter with sub-nanosecond resolution," in *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on*, 1997, pp. 189-192 vol.1.
- [2] K. Maatta and J. Kostamovaara, "A high-precision time-to-digital converter for pulsed time-of-flight laser radar applications," *Instrumentation and Measurement, IEEE Transactions on*, vol. 47, pp. 521-536, 1998.
- [3] I. Nissinen and J. Kostamovaara, "On-Chip Voltage Reference-Based Time-to-Digital Converter for Pulsed Time-of-Flight Laser Radar Measurements," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, pp. 1938-1948, 2009.
- [4] A. H. Chan and G. W. Roberts, "A jitter characterization system using a component-invariant Vernier delay line," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, pp. 79-95, 2004.
- [5] K. Niitsu, M. Sakurai, N. Harigai, T. J. Yamaguchi, and H. Kobayashi, "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier With Duty-Cycle Compensation," *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 2701-2710, 2012.
- [6] B. K. Swann, B. J. Blalock, L. G. Clonts, D. M. Binkley, J. M. Rochelle, E. Breeding, *et al.*, "A 100-ps time-resolution CMOS time-to-digital converter for positron emission tomography imaging applications," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 1839-1852, 2004.
- [7] A. S. Yousif and J. W. Haslett, "A Fine Resolution TDC Architecture for Next Generation PET Imaging," *Nuclear Science, IEEE Transactions on*, vol. 54, pp. 1574-1582, 2007.
- [8] J. Rivoir, "Fully-Digital Time-To-Digital Converter for ATE with Autonomous Calibration," in *Test Conference, 2006. ITC '06. IEEE International*, 2006, pp. 1-10.
- [9] L. Seon-Kyoo, S. Young-Hun, S. Yunjae, P. Hong-June, and S. Jae-Yoon, "A 1GHz ADPLL with a 1.25ps minimum-resolution sub-exponent TDC in 0.18 μ m CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, 2010, pp. 482-483.
- [10] P. Youngmin and D. D. Wentzloff, "A Cyclic Vernier TDC for ADPLLs Synthesized From a Standard Cell Library," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, pp. 1511-1517, 2011.
- [11] R. B. Staszewski, J. L. Wallberg, S. Rezek, H. Chih-Ming, O. E. Eliezer, S. K. Vemulapalli, *et al.*, "All-digital PLL and transmitter for mobile phones," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2469-2482, 2005.
- [12] R. B. Staszewski, K. Muhammad, D. Leipold, H. Chih-Ming, H. Yo-Chuol, J. L. Wallberg, *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 2278-2291, 2004.
- [13] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, pp. 220-224, 2006.

- [14] V. Ramakrishnan and P. T. Balsara, "A wide-range, high-resolution, compact, CMOS time to digital converter," in *VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on*, 2006, p. 6 pp.
- [15] G. S. Jovanovic and M. K. Stojcev, "Vernier's Delay Line Time-to-Digital Converter," *Series A: Applied Mathematics, Informatics & Mechanics*, vol. 1, pp. 11-20, 2009.
- [16] D. Tamborini, B. Markovic, S. Tisa, F. A. Villa, and A. Tosi, "TDC with 1.5% DNL based on a single-stage vernier delay-loop fine interpolation," in *Time-to-Digital Converters (NoMe TDC), 2013 IEEE Nordic-Mediterranean Workshop on*, 2013, pp. 1-6.
- [17] C. Ljuslin, J. Christiansen, A. Marchioro, and O. Klingsheim, "An integrated 16-channel CMOS time to digital converter," *Nuclear Science, IEEE Transactions on*, vol. 41, pp. 1104-1108, 1994.
- [18] T. E. Rahkonen and J. T. Kostamovaara, "The use of stabilized CMOS delay lines for the digitization of short time intervals," *Solid-State Circuits, IEEE Journal of*, vol. 28, pp. 887-894, 1993.
- [19] S. Henzler, *Time-to-Digital Converters*: Springer (2010), 2010.
- [20] P. Min and M. H. Perrott, "A single-slope 80MS/s ADC using Two-Step Time-to-Digital Conversion," in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, 2009, pp. 1125-1128.
- [21] A. Matsuzawa, "Design Challenges of Analog-to-Digital Converters in Nanoscale CMOS," *IEICE Transactions on Electronics*, vol. E90C, 04/01 2007.
- [22] S. Henzler, S. Koeppe, W. Kamp, H. Mulatz, and D. Schmitt-Landsiedel, "90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 548-635.
- [23] G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari, "Delay-Line-Based Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, pp. 464-468, 2009.
- [24] T. Xian, P. Kong-Pang, and N. Wai-Tung, "A 0.9V 5kS/s resistor-based time-domain temperature sensor in 90nm CMOS with calibrated inaccuracy of $-0.6^{\circ}\text{C}/0.8^{\circ}\text{C}$ from -40°C to 125°C ," in *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*, 2013, pp. 169-172.
- [25] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, pp. 17-32, 10 December 2003.
- [26] N. Minas, D. Kinniment, K. Heron, and G. Russell, "A High Resolution Flash Time-to-Digital Converter Taking Into Account Process Variability," in *Asynchronous Circuits and Systems, 2007. ASYNC 2007. 13th IEEE International Symposium on*, 2007, pp. 163-174.
- [27] P. M. Levine and G. W. Roberts, "A calibration technique for a high-resolution flash time-to-digital converter," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, 2004, pp. I-253-I-256 Vol.1.
- [28] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 240-247, 2000.

- [29] H. Chorng-Sii, C. Poki, and T. Hen-Wai, "A high-precision time-to-digital converter using a two-level conversion scheme," in *Nuclear Science Symposium Conference Record, 2003 IEEE*, 2003, pp. 174-176 Vol.1.
- [30] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1286-1296, 2006.
- [31] K. Mino, S. Woo-Yeol, H. Gi-Moon, P. Jihwan, C. Joo-Hyung, X. Nan, *et al.*, "High-resolution and wide-dynamic range time-to-digital converter with a multi-phase cyclic Vernier delay line," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, 2013, pp. 311-314.
- [32] L. Chin-Hsin and M. Syrzycki, "Pico-second time interval amplification," in *SoC Design Conference (ISOCC), 2010 International*, 2010, pp. 201-204.
- [33] L. Ping, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps," *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 1626-1635, 2012.
- [34] B. Markovic, S. Tisa, F. A. Villa, A. Tosi, and F. Zappa, "A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 60, pp. 557-569, 2013.
- [35] L. Ping, W. Ying, and P. Andreani, "A 90nm CMOS digital PLL based on Vernier-Gated-Ring-Oscillator Time-to-Digital Converter," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, 2012, pp. 2593-2596.
- [36] P. Youngmin and D. D. Wentzloff, "A cyclic vernier time-to-digital converter synthesized from a 65nm CMOS standard library," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, 2010, pp. 3561-3564.
- [37] C. Wei and C. Papavassiliou, "A Low Power 10-Bit Time-to-Digital Converter Utilizing Vernier Delay Lines," in *Computer Modelling and Simulation (UKSim), 2013 UKSim 15th International Conference on*, 2013, pp. 774-779.
- [38] E. Raisanen-Ruotsalainen, T. Rahkonen, and J. Kostamovaara, "A low-power CMOS time-to-digital converter," *Solid-State Circuits, IEEE Journal of*, vol. 30, pp. 984-990, 1995.
- [39] C. Poki, L. Shen-Iuan, and W. Jingshown, "A CMOS pulse-shrinking delay element for time interval measurement," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 954-958, 2000.
- [40] S. Tisa, A. Lotito, A. Giudice, and F. Zappa, "Monolithic time-to-digital converter with 20ps resolution," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 465-468.
- [41] L. Yue, U. Vollenbruch, C. Yangjian, C. Wicpalek, L. Maurer, T. Mayer, *et al.*, "A 6ps resolution pulse shrinking Time-to-Digital Converter as phase detector in multi-mode transceiver," in *Radio and Wireless Symposium, 2008 IEEE*, 2008, pp. 163-166.
- [42] K. Moon Seok, K. Yong-Bin, and K. Kyung-Ki, "All-digital phased-locked loop with local passive interpolation time-to-digital converter based on a tristate inverter," in *Circuits and Systems (MWSCAS), 2012 IEEE 55th International Midwest Symposium on*, 2012, pp. 326-329.
- [43] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "Variation tolerant high resolution and low latency time-to-digital converter," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, 2007, pp. 194-197.

- [44] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A Local Passive Time Interpolation Concept for Variation-Tolerant High-Resolution Time-to-Digital Conversion," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 1666-1676, 2008.
- [45] A. M. Abas, A. Bystrov, D. J. Kinniment, O. V. Maevsky, G. Russell, and A. V. Yakovlev, "Time difference amplifier," *Electronics Letters*, vol. 38, pp. 1437-1438, 2002.
- [46] L. Minjae and A. A. Abidi, "A 9 b, 1.25 ps Resolution Coarse-Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 769-777, 2008.
- [47] K. Kim, Y. H. Kim, W. Yu, and S. Cho, "A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 48, pp. 1009-1017, 2013.
- [48] K. KwangSeok, Y. WonSik, and C. SeongHwan, "A 9 bit, 1.12 ps Resolution 2.5 b/Stage Pipelined Time-to-Digital Converter in 65 nm CMOS Using Time-Register," *Solid-State Circuits, IEEE Journal of*, vol. 49, pp. 1007-1016, 2014.
- [49] M. H. Chung and H. P. Chou, "A time-to-digital converter using vernier delay line with time amplification technique," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE*, 2011, pp. 772-775.
- [50] B. Seung-Jun, C. Hyung-Joon, S. Young-Soo, and P. Hong-June, "A VCDL-based 60-760-MHz dual-loop DLL with infinite phase-shift capability and adaptive-bandwidth scheme," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1119-1129, 2005.
- [51] M. A. Abas, G. Russell, and D. J. Kinniment, "Design of sub-10-picoseconds on-chip time measurement circuit," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings, 2004*, pp. 804-809 Vol.2.
- [52] M. H. Chung, W. S. Liu, and H. P. Chou, "Time amplification using closed-loop differential amplifier," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE*, 2012, pp. 789-792.
- [53] M. Oulmane and G. W. Roberts, "A CMOS time amplifier for Femto-second resolution timing measurement," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, 2004, pp. I-509-12 Vol.1.
- [54] S. Young-Hun, K. Jun-Seok, P. Hong-June, and S. Jae-Yoon, "A 1.25 ps resolution 8b cyclic TDC in 0.13 μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 736-743, 2012.
- [55] T. Nakura, S. Mandai, M. Ikeda, and K. Asada, "Time difference amplifier using closed-loop gain control," in *VLSI Circuits, 2009 Symposium on*, 2009, pp. 208-209.
- [56] S. Mandai, T. Nakura, M. Ikeda, and K. Asada, "Cascaded Time Difference Amplifier using Differential Logic Delay Cell," in *SoC Design Conference (ISOC), 2009 International*, 2009, pp. 194-197.
- [57] S. Mandai, T. Iizuka, T. Nakura, M. Ikeda, and K. Asada, "Time-to-digital converter based on time difference amplifier with non-linearity calibration," in *ESSCIRC, 2010 Proceedings of the*, 2010, pp. 266-269.
- [58] C. Poki, C.-C. Chen, Z. Jia-Chi, and S. You-Sheng, "A PVT Insensitive Vernier-Based Time-to-Digital Converter With Extended Input Range and High Accuracy," *Nuclear Science, IEEE Transactions on*, vol. 54, pp. 294-302, 2007.
- [59] C. Poki, Z. Jia-Chi, and C.-C. Chen, "A monolithic vernier-based time-to-digital converter with dual PLLs for self-calibration," in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, 2005, pp. 321-324.

- [60] M. Maymandi-Nejad and M. Sachdev, "A digitally programmable delay element: design and analysis," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 11, pp. 871-878, 2003.
- [61] K. C. Kuo and Y. H. Hsu, "A 120-240 MHz delay-locked loop with multi-band voltage-controlled delay unit," *International Journal of Circuit Theory and Applications*, vol. 40, pp. 49 - 63, January 2012 2012.
- [62] B. A. Minch, "MOS Translinear Principle for All Inversion Levels," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, pp. 121-125, 2008.
- [63] K. Jaewook and C. SeongHwan, "A time-based analog-to-digital converter using a multi-phase voltage controlled oscillator," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, 2006, pp. 4 pp.-3937.
- [64] H. Mostafa and Y. I. Ismail, "Highly-linear voltage-to-time converter (VTC) circuit for time-based analog-to-digital converters (T-ADCs)," in *Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on*, 2013, pp. 149-152.
- [65] H. Pekau, A. Yousif, and J. W. Haslett, "A CMOS integrated linear voltage-to-pulse-delay-time converter for time based analog-to-digital converters," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, 2006, pp. 4 pp.-2376.
- [66] A. R. Macpherson, K. A. Townsend, and J. W. Haslett, "A 5GS/s voltage-to-time converter in 90nm CMOS," in *Microwave Integrated Circuits Conference, 2009. EuMIC 2009. European*, 2009, pp. 254-257.
- [67] C. Hyoung-Taek, K. Young-Hwa, K. KwangSeok, K. Jaewook, and C. SeongHwan, "Time-interleaved single-slope ADC using counter-based time-to-digital converter," in *Radio-Frequency Integration Technology (RFIT), 2011 IEEE International Symposium on*, 2011, pp. 185-188.
- [68] H. Huihua and C. Sechen, "A 22mW 227Msps 11b self-tuning ADC based on time-to-digital conversion," in *Circuits and Systems Workshop,(DCAS), 2009 IEEE Dallas*, 2009, pp. 1-4.
- [69] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8MHz 100kS/s SAR ADC with Time-Domain Comparator," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 246-610.
- [70] H. Hong-Yi and L. Jing-Fu, "CMOS bulk input technique," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, 2002, pp. III-III.
- [71] Y. Jianjun, D. Fa Foster, and R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 μ m CMOS Technology," *Solid-State Circuits, IEEE Journal of*, vol. 45, pp. 830-842, 2010.
- [72] K. A. Townsend, A. R. Macpherson, and J. W. Haslett, "A fine-resolution Time-to-Digital Converter for a 5GS/S ADC," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, 2010, pp. 3024-3027.
- [73] K. KwangSeok, K. YoungHwa, Y. WonSik, and C. SeongHwan, "A 7b, 3.75ps resolution two-step time-to-digital converter in 65nm CMOS using pulse-train time amplifier," in *VLSI Circuits (VLSIC), 2012 Symposium on*, 2012, pp. 192-193.

- [74] S. Young-Hun, L. Seon-Kyoo, and S. Jae-Yoon, "A 1-GHz Digital PLL With a 3-ps Resolution Floating-Point-Number TDC in a 0.18- μ m CMOS," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 58, pp. 70-74, 2011.
- [75] L. Ping, P. Andreani, and A. Liscidini, "A 90nm CMOS gated-ring-oscillator-based Vernier time-to-digital converter for DPLLs," in *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, 2011, pp. 459-462.
- [76] B. Kim, H. Kim, and C. H. Kim, "An 8bit, 2.6ps two-step TDC in 65nm CMOS employing a switched ring-oscillator based time amplifier," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1-4.
- [77] M. Lee and A. A. Abidi, "A 9b, 1.25ps Resolution Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue," in *2007 IEEE Symposium on VLSI Circuits*, 2007, pp. 168-169.
- [78] A. Hamza, S. Ibrahim, M. El-Nozahi, and M. Dessouky, "A low-power, 9-Bit, 1.2 ps resolution two-step time-to-digital converter in 65 nm CMOS," in *2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)*, 2015, pp. 1-4.
- [79] S. Chung, K. Hwang, W. Lee, and L. Kim, "A high resolution metastability-independent two-step gated ring oscillator TDC with enhanced noise shaping," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, 2010, pp. 1300-1303.
- [80] K. Jun-Seok, S. Young-Hun, S. Yunjae, P. Hong-June, and S. Jae-Yoon, "A 300-MS/s, 1.76-ps-Resolution, 10-b Asynchronous Pipelined Time-to-Digital Converter With on-Chip Digital Background Calibration in 0.13- μ m CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 48, pp. 516-526, 2013.
- [81] A. Samarah and A. C. Carusone, "A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 1829-1841, 2013.
- [82] C. Pao-Lung, C. Ching-Che, and L. Chen-Yi, "A portable digitally controlled oscillator using novel varactors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, pp. 233-237, 2005.
- [83] K. Ohhata, "A 2.3-mW, 1-GHz, 8-Bit Fully Time-Based Two-Step ADC Using a High-Linearity Dynamic VTC," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 2038-2048, 2019.
- [84] S. Zhu, B. Xu, B. Wu, K. Soppimath, and Y. Chiu, "A 0.073-mm² 10-GS/s 6-bit time-domain folding ADC in 65-nm CMOS with inherent DEM," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1-4.
- [85] P. Osheroff, G. S. L. Rue, and S. Gupta, "A highly linear 4GS/s uncalibrated voltage-to-time converter with wide input range," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 89-92.
- [86] H. Huang and C. Sechen, "A 22mW 227Msps 11b self-tuning ADC based on time-to-digital conversion," in *2009 IEEE Dallas Circuits and Systems Workshop (DCAS)*, 2009, pp. 1-4.
- [87] M. Santos, N. Horta, and J. Guilherme, "An 8bit logarithmic AD converter Using cross-coupled inverters and a time-to-digital converter," in *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2016, pp. 1-4.
- [88] Y. Lyu and F. Tavernier, "A 4GS/s 39.9dB SNDR 11.7mW Hybrid Voltage-Time Two-Step ADC with Feed-Forward Ring Oscillator Based TDCs," *IEEE Solid-State Circuits Letters*, pp. 1-1, 2019.

- [89] S. Jia, L. Weng, W. Wang, and Y. Wang, "A highly linear 5GS/s voltage-to-time converter for time-based analog-to-digital converters," in *2017 IEEE Asia Pacific Microwave Conference (APMC)*, 2017, pp. 714-717.
- [90] Y. Kim and C. Yoo, "A 100-kS/s 8.3-ENOB 1.7- μs Time-Domain Analog-to-Digital Converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, pp. 408-412, 2014.
- [91] Y. Lin and H. Tsao, "A high-speed high-accuracy voltage-to-time-difference converter for time domain analog-to-digital converters," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 2285-2288.
- [92] W. El-Halwagy, P. Mousavi, and M. Hossain, "A 79dB SNDR, 10MHz BW, 675MS/s open-loop time-based ADC employing a 1.15ps SAR-TDC," in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2016, pp. 321-324.
- [93] V. Unnikrishnan and M. Vesterbacka, "Time-Mode Analog-to-Digital Conversion Using Standard Cells," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, pp. 3348-3357, 2014.
- [94] D. A. J. Tony Chan Carusone, Kenneth W. Martin, *Analog Integrated Circuit Design*: John Wiley & Sons, Inc., 2011.
- [95] B. Razavi, "The Bootstrapped Switch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, pp. 12-15, 2015.
- [96] M. Abdelkader, A. Ali, A. Abdelaziz, M. W. Ismail, M. Refky, Y. Ismail, *et al.*, "A 200MS/s, 8-bit Time-based Analog to Digital Converter (TADC) in 65nm CMOS technology," in *2016 Fourth International Japan-Egypt Conference on Electronics, Communications and Computers (JEC-ECC)*, 2016, pp. 25-28.
- [97] W. Kester, *Analog-Digital Conversion*, 2004.